TPS7A53-Q1 3A、高精度、車載グレード、低ノイズ、LDO電圧レギュレータ

1 特長

- **車載アプリケーションに対応**
- **車載アプリケーション用にAEC-Q100認定済み**
  - 温度グレード1: －40℃≦T_A≦＋125℃
  - HBM ESD分類レベル2
  - CDM ESD分類レベルC4A
- **拡張接合部温度範囲(T_J): -40℃～+150℃**
- **入力電圧範囲:**
  - BIASなし: 1.4V～6.5V
  - BIASあり: 1.1V～6.5V
- **可変出力電圧範囲:** 0.8V～5.15V
- **低いドロップアウト:** 3A、BIAS使用で180mV (最大値)
- **出力電圧ノイズ:** 4.4μV_{RMS}
- **ライン、負荷、温度範囲にわたって1% (最大値)の精度(BIAS使用時)**
- **電源リップル除去:**
  - 500kHz時に40dB
- **可変のソフトスタート突入電流制御**
- **オープン・ドレインのパワー・グッド(PG)出力**
- **パッケージ**
  - 3.5mm×3.5mm、20ピンのVQFN
  - ウェッタブル・フランク付きで高CTE (12ppm/℃)の複合金型を使用した4mm×4mm、20ピンのVQFNP

2 アプリケーション

- **テレマティクス制御ユニット**
- **インフォテインメントおよびクラスタ**
- **高速インターフェイス(PLLおよびVCO)**

3 概要

TPS7A53-Q1デバイスは低ノイズ(4.4μV_{RMS})、低ドロップアウトのリニア・レギュレータ(LDO)で、3Aを供給でき、ドロップアウトは最大でわずか180mVです。デバイスの出力電圧は、外付けの分圧抵抗によって0.8V～5.15Vの範囲で調整可能です。

低ノイズ(4.4μV_{RMS})、高PSRR、大出力電流の能力の組み合わせにより、TPS7A53-Q1はレーダーの電源やインフォテイメント・アプリケーションなどに使用される、ノイズに敏感な部品への電源供給に理想的です。このデバイスは高性能で、電源に起因する位相ノイズやクロック・ジッタを制限することにより、RFアンプ、レーダー・センサ、チップセットの電源として非常に優れています。特に、RFアンプにはこのデバイスの高い性能と5.0V出力能力が役立ちます。

ASIC (Application-Specific Integrated Circuit)、FPGA (Field-Programmable Gate Array)、DSP (Digital Signal Processor)などのデジタル負荷で低入力電圧、低出力電圧(LILO)の動作を必要とする場合、TPS7A53-Q1の非常に優れた精度(負荷および温度範囲にわたって1%)、リモート・センシング、優れた過渡性能、ソフトスタート機能によって、最適のシステム性能が保証されます。

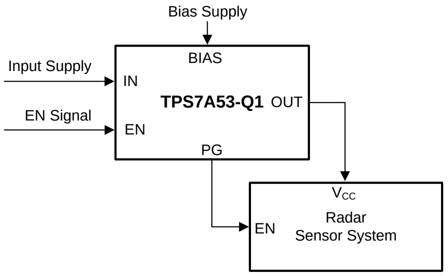
多用途なTPS7A53-Q1デバイスは、要求の厳しい多くのアプリケーションの部品として最適な選択肢です。

製品情報[(1)]

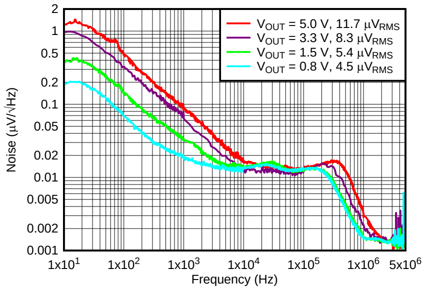
型番	パッケージ	本体サイズ(公称)
TPS7A53-Q1	VQFN (20)	3.50mm×3.50mm
	ウェッタブル・フランク付きVQFNP (20)	4.00mm×4.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

RFコンポーネントの電源



出力電圧ノイズと周波数および出力電圧との関係



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4 改訂履歴

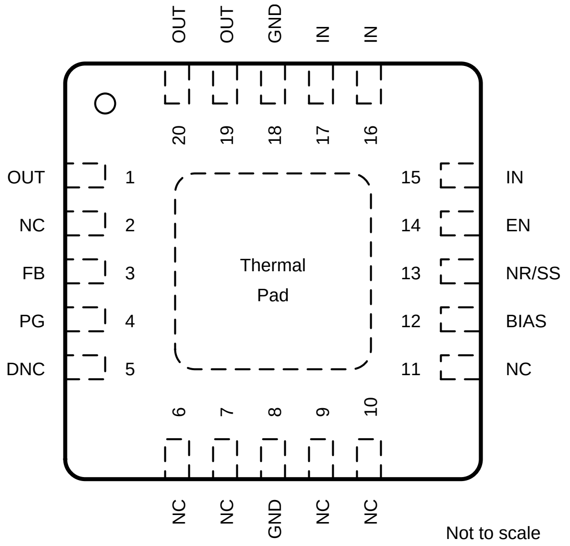
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (February 2018) から Revision B に変更	**Page**
• 新しいRTKパッケージ(ウェッタブル・フランク付きVQFNP) 追加	1

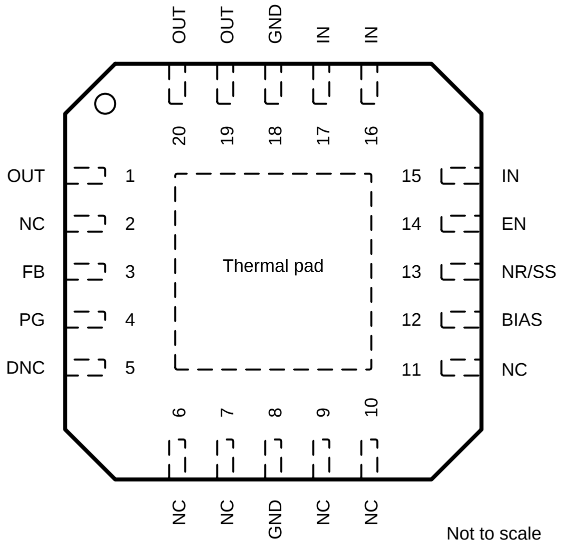
2017年9月発行のものから更新	**Page**
• 製品プレビューから量産データ(アクティブ)に 変更	1

5 Pin Configuration and Functions

RGR Package
3.5-mm × 3.5-mm, 20-Pin VQFN
Top View



RTK Package
4-mm × 4-mm, 20-Pin VQFNP
Top View



Pin Functions

PIN			DESCRIPTION
NAME	NO.	I/O	
BIAS	12	I	BIAS supply voltage. This pin enables the use of low-input voltage, low-output (LILO) voltage conditions (that is, V_{IN} = 1.2 V, V_{OUT} = 1 V) to reduce power dissipation across the die. The use of a BIAS voltage improves dc and ac performance for $V_{IN} \leq 2.2$ V. A 10-µF capacitor or larger must be connected between this pin and ground. If not used, this pin must be left floating or tied to ground.
DNC	5		Do not connect. Leave this pin floating or connect this pin to ground.
EN	14	I	Enable pin. Driving this pin to logic high enables the device; driving this pin to logic low disables the device. If enable functionality is not required, this pin must be connected to IN or BIAS.
FB	3	I	Feedback pin connected to the error amplifier. Although not required, a 10-nF feed-forward capacitor from FB to OUT (as close to the device as possible) is recommended to maximize ac performance. The use of a feed-forward capacitor can disrupt PG (power good) functionality.
GND	8, 18	—	Ground pin. These pins must be connected to ground, the thermal pad, and each other with a low-impedance connection.
IN	15-17	I	Input supply voltage pin. A 10-µF or larger ceramic capacitor (5 µF or greater of capacitance) from IN to ground is recommended to reduce the impedance of the input supply. Place the input capacitor as close to the input as possible.
NC	2, 6, 7, 9, 10, 11		No internal connection
NR/SS	13	—	Noise-reduction and soft-start pin. Connecting an external capacitor between this pin and ground reduces reference voltage noise and also enables the soft-start function. Although not required, a 10-nF or larger capacitor is recommended to be connected from NR/SS to GND (as close to the pin as possible) to maximize ac performance.
OUT	1, 19, 20	O	Regulated output pin. A 47-µF or larger ceramic capacitor (25 µF or greater of capacitance) from OUT to ground is required for stability and must be placed as close to the output as possible. Minimize the impedance from the OUT pin to the load.
PG	4	O	Active-high, power-good pin. An open-drain output indicates when the output voltage reaches $V_{IT(PG)}$ of the target. The use of a feed-forward capacitor may disrupt PG (power good) functionality.
Thermal pad		—	Connect the thermal pad to a large-area ground plane. The thermal pad is internally connected to GND.

6 Specifications

6.1 Absolute Maximum Ratings

over junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	IN, BIAS, PG, EN	–0.3	7.0	V
	OUT	–0.3	V_{IN} + 0.3(2)	
	NR/SS, FB	–0.3	3.6	
Current	OUT	Internally limited		A
	PG (sink current into device)		5	mA
Operating junction temperature, T_J		–55	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is V_{IN} + 0.3 V or 7.0 V, whichever is smaller.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002((1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage range(1)	1.1		6.5	V
V_{BIAS}	Bias supply voltage range(1)	3.0		6.5	V
V_{EN}	Enable voltage range	0		6.5	V
I_{OUT}	Output current	0		3	A
C_{IN}	Input capacitor	10	47		µF
C_{OUT}	Output capacitor(2)	47	47 || 10 || 10		µF
C_{BIAS}	Bias capacitor (3)	10			µF
R_{PG}	Power-good pullup resistance	10		100	kΩ
$C_{NR/SS}$	NR/SS capacitor		10		nF
C_{FF}	Feed-forward capacitor		10		nF
R_1	Top resistor value in feedback network for adjustable operation(4)		12.1		kΩ
R_2	Bottom resistor value in feedback network for adjustable operation(5)		160		kΩ
T_J	Operating junction temperature	–40		150	°C

(1) BIAS supply is required when the V_{IN} supply is below 1.4 V. Conversely, no BIAS supply is required when the V_{IN} supply is higher than or equal to 1.4 V. A BIAS supply helps improve dc and ac performance for $V_{IN} \leq 2.2$ V.
(2) The recommended output capacitors are selected to optimize PSRR for the frequency range of 400 kHz to 700 kHz. This frequency range is a typical value for dc-dc supplies.
(3) If BIAS is used, a 10-µF capacitor is required. If BIAS is not used, a capacitor on the BIAS pin is not needed.
(4) The 12.1-kΩ resistor is selected to optimize PSRR and noise by matching the internal R_1 value.
(5) The upper limit for the R_2 resistor is to provide accuracy by making the current through the feedback network much larger than the leakage current into the feedback node.

6.4 Thermal Information

THERMAL METRIC(1)		TPS7A53-Q1		UNIT
		RGR (VQFN)	RTK (VQFNP)	
		20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	43.4	39.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.8	32.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.6	16.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	17.6	16.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.4	1.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating junction temperature range (T_J = –40°C to +150°C), V_{IN} = 1.4 V or $V_{IN} = V_{OUT(nom)}$ + 0.4 V (whichever is greater), V_{BIAS} = open, $V_{OUT(nom)}$ = 0.8 V(1), OUT connected to 50 Ω to GND(2), V_{EN} = 1.1 V, C_{IN} = 10 µF, C_{OUT} = 47 µF, $C_{NR/SS}$ = C_{FF} = open, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FB}	Feedback voltage				0.8		V
$V_{NR/SS}$	NR/SS pin voltage				0.8		V
$V_{UVLO1+(IN)}$	Rising input supply UVLO with BIAS		V_{IN} rising with V_{BIAS} = 3.0 V		1.02	1.09	V
$V_{HYS1(IN)}$	$V_{UVLO1(IN)}$ hysteresis		V_{BIAS} = 3.0 V		320		mV
$V_{UVLO1-(IN)}$	Falling input supply UVLO with BIAS		V_{IN} falling with V_{BIAS} = 3.0 V	0.55	0.711		V
$V_{UVLO2+(IN)}$	Rising input supply UVLO without BIAS		V_{IN} rising		1.31	1.39	V
$V_{HYS2(IN)}$	$V_{UVLO2(IN)}$ hysteresis				253		mV
$V_{UVLO2-(IN)}$	Falling input supply UVLO without BIAS		V_{IN} falling	0.65	1.064		V
$V_{UVLO+(BIAS)}$	Rising bias supply UVLO		V_{BIAS} rising, V_{IN} = 1.1 V		2.83	2.9	V
$V_{UVLO-(BIAS)}$	Falling bias supply UVLO		V_{BIAS} falling, V_{IN} = 1.1 V	2.45	2.531		V
$V_{HYS(BIAS)}$	$V_{UVLO(BIAS)}$ hysteresis		V_{IN} = 1.1 V		290		mV
V_{OUT}	Output voltage	Range	Using external resistors(3)	0.8		5.15	V
		Accuracy	0.8 V ≤ V_{OUT} ≤ 5.15 V, 5 mA ≤ I_{OUT} ≤ 3 A, over V_{IN}, –40℃ < T_J < 150℃	–2%		1%	
		Accuracy with BIAS	V_{IN} = 1.1 V, 5 mA ≤ I_{OUT} ≤ 3 A,3.0 V ≤ V_{BIAS} ≤ 6.5 V, –40℃ < T_J < 150℃	–1.75%		0.75%	
		Accuracy	0.8 V ≤ V_{OUT} ≤ 5.15 V, 5 mA ≤ I_{OUT} ≤ 3 A, over V_{IN}, –40℃ < T_J < 125℃	–1%		1%	
		Accuracy with BIAS	V_{IN} = 1.1 V, 5 mA ≤ I_{OUT} ≤ 3 A, 3.0 V ≤ V_{BIAS} ≤ 6.5 V, –40℃ < T_J < 125℃	–0.75%		0.75%	
$\Delta V_{OUT}/ \Delta V_{IN}$	Line regulation		I_{OUT} = 5 mA, 1.4 V ≤ V_{IN} ≤ 6.5 V		0.0035		mV/V
$\Delta V_{OUT}/ \Delta I_{OUT}$	Load regulation		5 mA ≤ I_{OUT} ≤ 3 A, 3.0 V ≤ V_{BIAS} ≤ 6.5 V, V_{IN} = 1.1 V		0.07		mV/A
			5 mA ≤ I_{OUT} ≤ 3 A		0.08		
			5 mA ≤ I_{OUT} ≤ 3 A, V_{OUT} = 5.0 V		0.04		

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(1) $V_{OUT(nom)}$ is the expected V_{OUT} value set by the external feedback resistors.
(2) This 50-Ω load is disconnected when the test conditions specify an I_{OUT} value.
(3) When the device is connected to external feedback resistors at the FB pin, external resistor tolerances are not included.

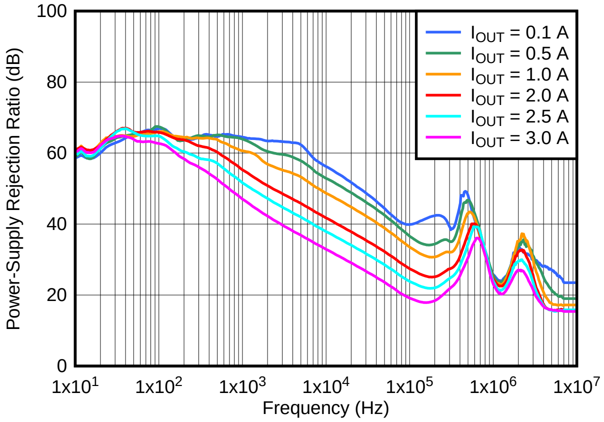
Electrical Characteristics (continued)

over operating junction temperature range (T_J = –40°C to +150°C), V_{IN} = 1.4 V or $V_{IN} = V_{OUT(nom)}$ + 0.4 V (whichever is greater), V_{BIAS} = open, $V_{OUT(nom)}$ = 0.8 V[1], OUT connected to 50 Ω to GND[2], V_{EN} = 1.1 V, C_{IN} = 10 µF, C_{OUT} = 47 µF, $C_{NR/SS}$ = C_{FF} = open, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DO}	Dropout voltage	RGR package	V_{IN} = 1.4 V, I_{OUT} = 3 A, V_{FB} = 0.8 V – 3%			157	285	mV
			V_{IN} = 5.4 V, I_{OUT} = 3 A, V_{FB} = 0.8 V – 3%			215	370	
			V_{IN} = 5.6 V, I_{OUT} = 3 A, V_{FB} = 0.8 V – 3%			255	475	
			V_{IN} = 1.1 V, 3.0 V ≤ V_{BIAS} ≤ 6.5 V, I_{OUT} = 3 A, V_{FB} = 0.8 V – 3%			110	195	
		RTK package	V_{IN} = 1.4 V, I_{OUT} = 3 A, V_{FB} = 0.8 V – 3%			170	310	
			V_{IN} = 5.4 V, I_{OUT} = 3 A, V_{FB} = 0.8 V – 3%			241	415	
			V_{IN} = 5.6 V, I_{OUT} = 3 A, V_{FB} = 0.8 V – 3%			291	515	
			V_{IN} = 1.1 V, 3.0 V ≤ V_{BIAS} ≤ 6.5 V, I_{OUT} = 3 A, V_{FB} = 0.8 V – 3%			126	220	
I_{LIM}	Output current limit		V_{OUT} forced at 0.9 × $V_{OUT(nom)}$, $V_{IN} = V_{OUT(nom)}$ + 0.4 V		3.55	4.2	4.9	A
I_{SC}	Short-circuit current limit		R_{LOAD} = 20 mΩ			1.0		A
I_{GND}	GND pin current		V_{IN} = 6.5 V, I_{OUT} = 5 mA			3	4	mA
			V_{IN} = 1.4 V, I_{OUT} = 3 A			4.3	5.5	
			Shutdown, PG = open, V_{IN} = 6.5 V, V_{EN} = 0.5 V				25	µA
I_{EN}	EN pin current		V_{IN} = 6.5 V, V_{EN} = 0 V and 6.5 V		–0.5		0.5	µA
I_{BIAS}	BIAS pin current		V_{IN} = 1.1 V, V_{BIAS} = 6.5 V, $V_{OUT(nom)}$ = 0.8 V, I_{OUT} = 3 A			2.4	3.5	mA
$V_{IL(EN)}$	EN pin low-level input voltage (disable device)						0.5	V
$V_{IH(EN)}$	EN pin high-level input voltage (enable device)				1.1			V
$V_{IT-(PG)}$	PG pin threshold		For falling V_{OUT}		$0.82V_{OUT}$	$0.88V_{OUT}$	$0.93V_{OUT}$	V
$V_{HYS(PG)}$	PG pin hysteresis					$0.02V_{OUT}$		V
$V_{IT+(PG)}$	PG pin threshold		For rising V_{OUT}		$0.84V_{OUT}$	$0.90V_{OUT}$	$0.95V_{OUT}$	V
$V_{OL(PG)}$	PG pin low-level output voltage		$V_{OUT} < V_{IT(PG)}$, I_{PG} = –1 mA (current into device)				0.4	V
$I_{lkg(PG)}$	PG pin leakage current		$V_{OUT} > V_{IT(PG)}$, V_{PG} = 6.5 V				1	µA
$I_{NR/SS}$	NR/SS pin charging current		$V_{NR/SS}$ = GND, V_{IN} = 6.5 V		4.0	6.5	10	µA
I_{FB}	FB pin leakage current		V_{IN} = 6.5 V		–100		100	nA
PSRR	Power-supply ripple rejection		$V_{IN} – V_{OUT}$ = 0.4 V, I_{OUT} = 3 A, $C_{NR/SS}$ = 100 nF, C_{FF} = 10 nF, C_{OUT} = 47 µF || 10 µF || 10 µF	f = 10 kHz, V_{OUT} = 0.8 V, V_{BIAS} = 5.0 V		42		dB
				f = 500 kHz, V_{OUT} = 0.8 V, V_{BIAS} = 5.0 V		39		
				f = 10 kHz, V_{OUT} = 5.0 V		40		
				f = 500 kHz, V_{OUT} = 5.0 V		25		
V_n	Output noise voltage		BW = 10 Hz to 100 kHz, V_{IN} = 1.1 V, V_{OUT} = 0.8 V, V_{BIAS} = 5.0 V, I_{OUT} = 3 A, $C_{NR/SS}$ = 100 nF, C_{FF} = 10 nF, C_{OUT} = 47 µF || 10 µF || 10 µF			4.4		$µV_{RMS}$
			BW = 10 Hz to 100 kHz, V_{OUT} = 5.0 V, I_{OUT} = 3 A, $C_{NR/SS}$ = 100 nF, C_{FF} = 10 nF, C_{OUT} = 47 µF || 10 µF || 10 µF			7.7		
T_{SD}	Thermal shutdown temperature		Shutdown, temperature increasing			160		°C
			Reset, temperature decreasing			140		

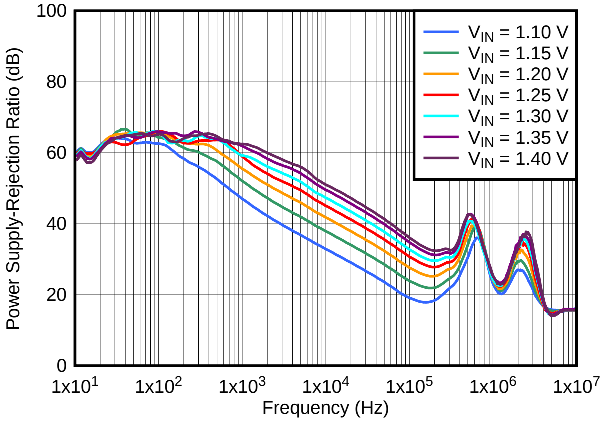
6.6 Typical Characteristics

at T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(NOM)}$ + 0.4 V (whichever is greater), V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{OUT} = 47 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted)



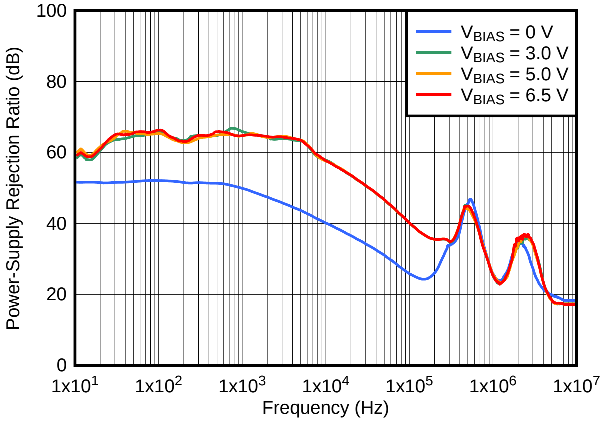
V_{IN} = 1.1 V, V_{BIAS} = 5 V,
C_{OUT} = 47 µF || 10 µF || 10 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

図 1. PSRR vs Frequency and I_{OUT}



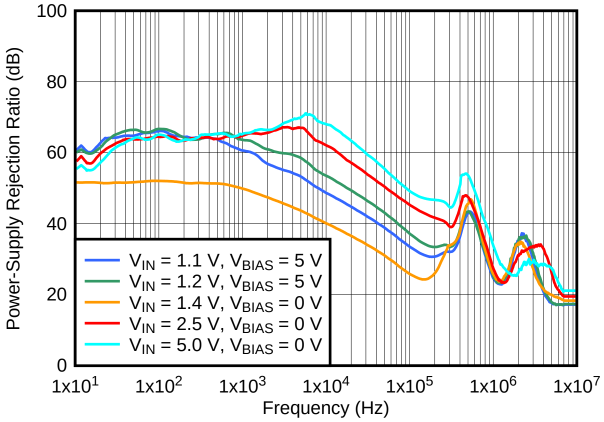
I_{OUT} = 3 A, V_{BIAS} = 5 V,
C_{OUT} = 47 µF || 10 µF || 10 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

図 2. PSRR vs Frequency and V_{IN} With Bias



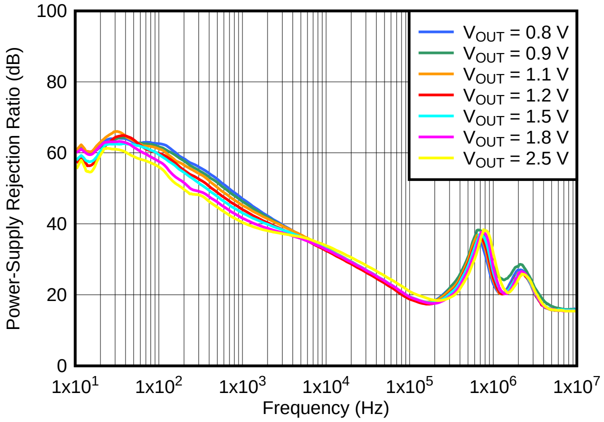
V_{IN} = 1.4 V, I_{OUT} = 1 A,
C_{OUT} = 47 µF || 10 µF || 10 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

図 3. PSRR vs Frequency and V_{BIAS}



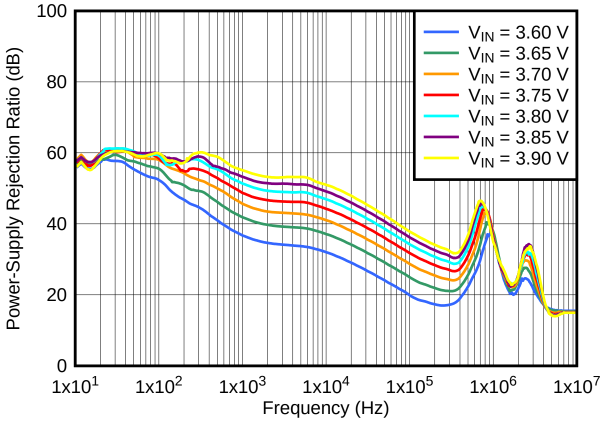
I_{OUT} = 1 A,
C_{OUT} = 47 µF || 10 µF || 10 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

図 4. PSRR vs Frequency and V_{IN}



V_{IN} = V_{OUT} + 0.3 V, V_{BIAS} = 5.0 V, I_{OUT} = 3 A,
C_{OUT} = 47 µF || 10 µF || 10 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

図 5. PSRR vs Frequency and V_{OUT} With Bias

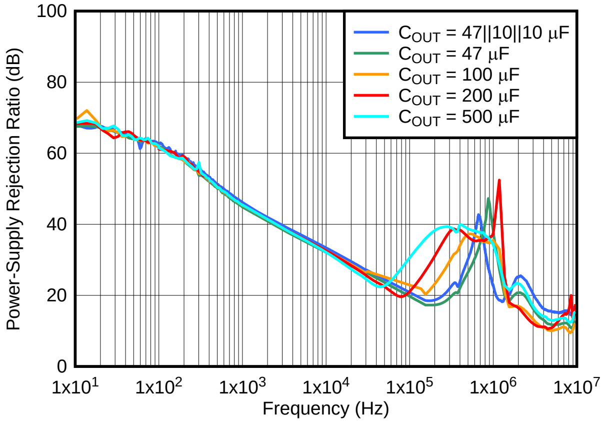


I_{OUT} = 3 A, C_{OUT} = 47 µF || 10 µF || 10 µF, $C_{NR/SS}$ = 10 nF,
C_{FF} = 10 nF

図 6. PSRR vs Frequency and V_{IN} for V_{OUT} = 3.3 V

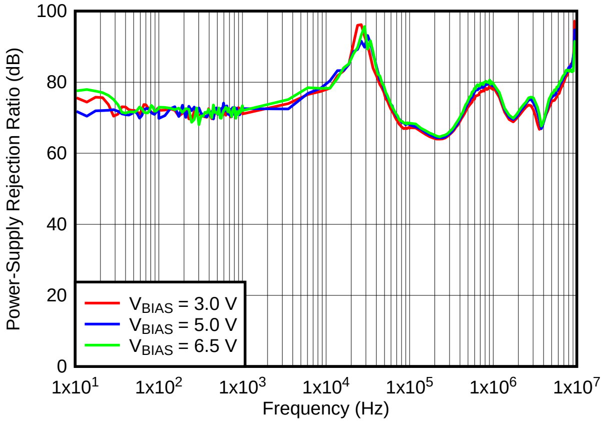
Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(NOM)}$ + 0.4 V (whichever is greater), V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{OUT} = 47 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted)



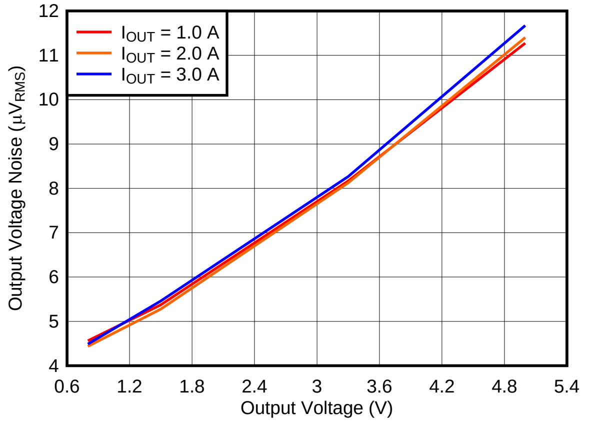
V_{IN} = V_{OUT} + 0.3 V, V_{OUT} = 1 V, I_{OUT} = 3 A, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

図 7. PSRR vs Frequency and C_{OUT}



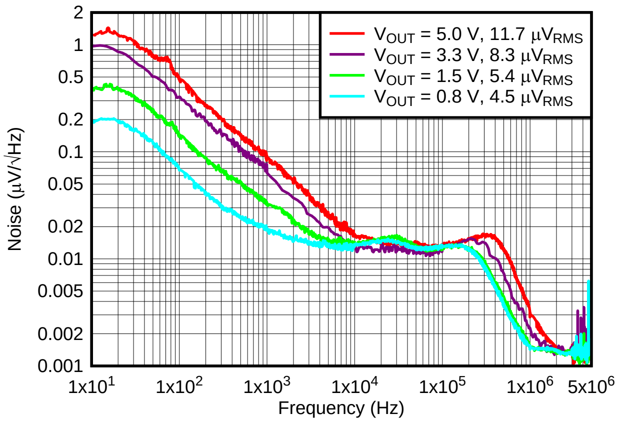
V_{IN} = V_{OUT} + 0.3 V, V_{OUT} = 1 V, I_{OUT} = 3 A, C_{OUT} = 47 µF || 10 µF || 10 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

図 8. V_{BIAS} PSRR vs Frequency and V_{BIAS}



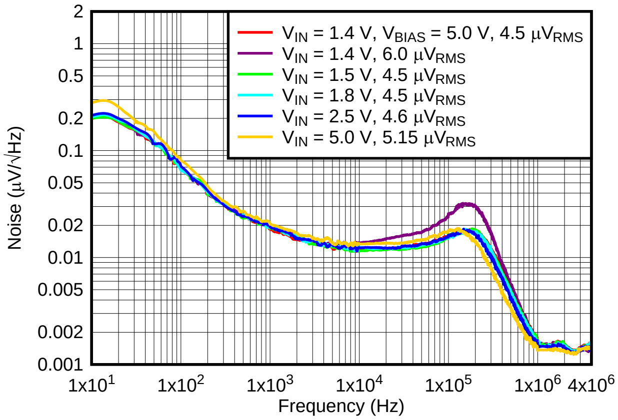
V_{IN} = V_{OUT} + 0.3 V and V_{BIAS} = 5 V for V_{OUT} ≤ 2.2 V, C_{OUT} = 47 µF || 10 µF || 10 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF, RMS noise BW = 10 Hz to 100 kHz

図 9. Output Voltage Noise vs Output Voltage



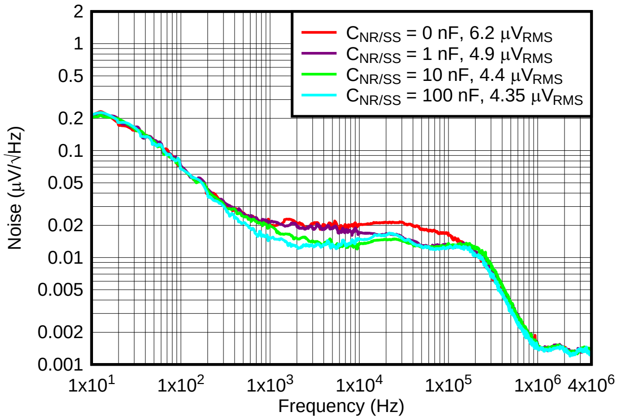
V_{IN} = V_{OUT} + 0.3 V and V_{BIAS} = 5 V for V_{OUT} ≤ 2.2 V, I_{OUT} = 3 A, C_{OUT} = 47 µF || 10 µF || 10 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF, RMS noise BW = 10 Hz to 100 kHz

図 10. Output Noise vs Frequency and V_{OUT}



I_{OUT} = 3 A, C_{OUT} = 47 µF || 10 µF || 10 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF, RMS noise BW = 10 Hz to 100 kHz

図 11. Output Noise vs Frequency and V_{IN}

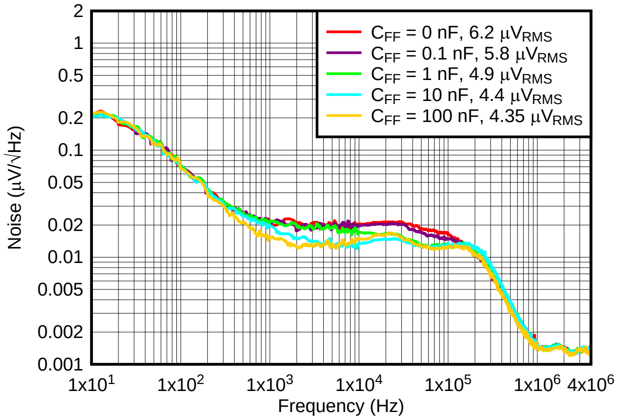


V_{IN} = V_{OUT} + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 3 A, C_{OUT} = 47 µF || 10 µF || 10 µF, C_{FF} = 10 nF, RMS noise BW = 10 Hz to 100 kHz

図 12. Output Noise vs Frequency and $C_{NR/SS}$

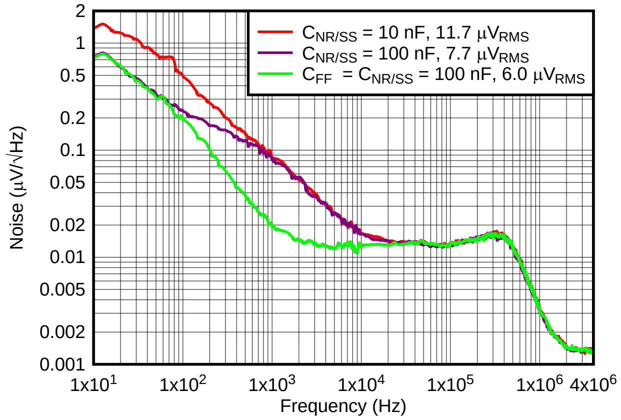
Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(NOM)}$ + 0.4 V (whichever is greater), V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{OUT} = 47 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted)



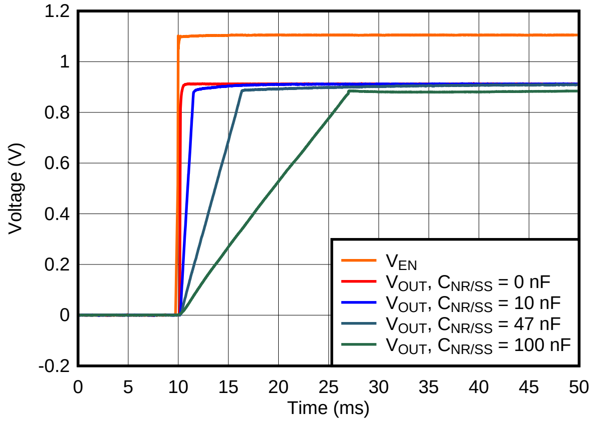
V_{IN} = V_{OUT} + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 3 A, sequencing with a dc-dc converter and PG, C_{OUT} = 47 µF || 10 µF || 10 µF, $C_{NR/SS}$ = 10 nF, RMS noise BW = 10 Hz to 100 kHz

図 13. Output Noise vs Frequency and C_{FF}



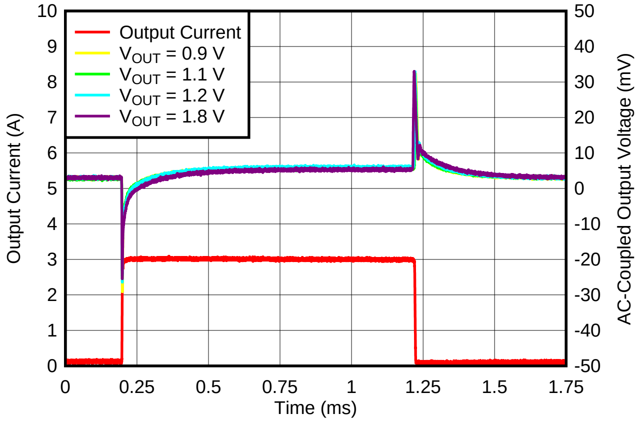
I_{OUT} = 3 A, C_{OUT} = 47 µF || 10 µF || 10 µF, C_{FF} = 10 nF, RMS noise BW = 10 Hz to 100 kHz

図 14. Output Noise at 5.0-V Output



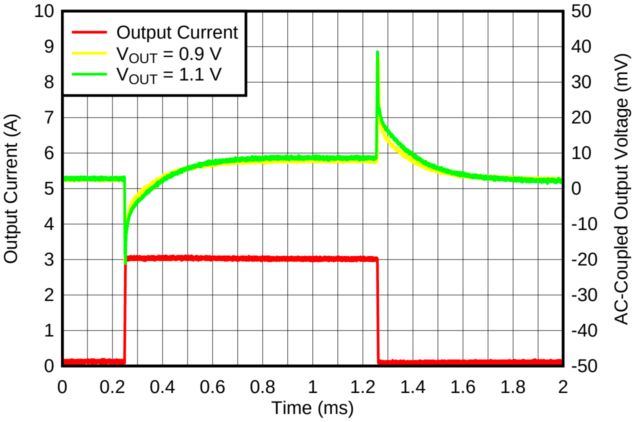
V_{IN} = 1.2 V, V_{OUT} = 0.9 V, V_{BIAS} = 5.0 V, I_{OUT} = 3 A, C_{OUT} = 47 µF || 10 µF || 10 µF, C_{FF} = 10 nF

図 15. Start-Up Waveform vs Time and $C_{NR/SS}$



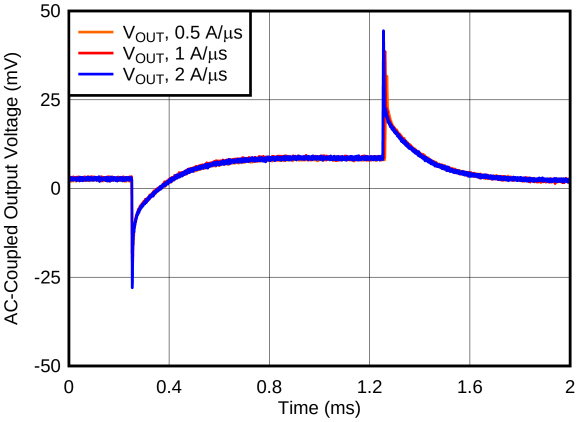
V_{IN} = V_{OUT} + 0.3 V, V_{BIAS} = 5 V, $I_{OUT,\ DC}$ = 100 mA, slew rate = 1 A/µs, $C_{NR/SS}$ = C_{FF} = 10 nF, C_{OUT} = 47 µF || 10 µF || 10 µF

図 16. Load Transient vs Time and V_{OUT} With Bias



$I_{OUT,\ DC}$ = 100 mA, C_{OUT} = 47 µF || 10 µF || 10 µF, $C_{NR/SS}$ = C_{FF} = 10 nF, slew rate = 1 A/µs

図 17. Load Transient vs Time and V_{OUT} Without Bias

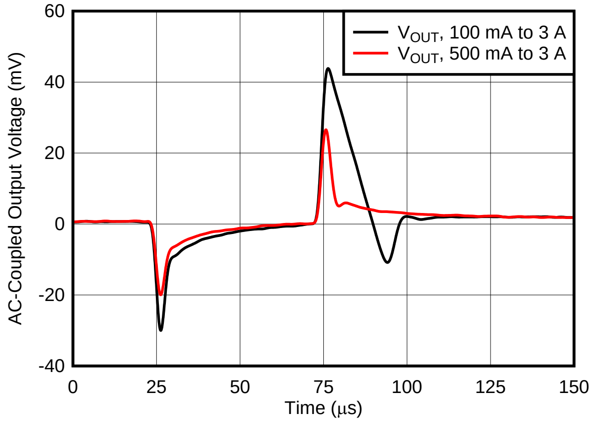


V_{OUT} = 5 V, $I_{OUT,\ DC}$ = 100 mA, I_{OUT} = 100 mA to 3 A, C_{OUT} = 47 µF || 10 µF || 10 µF, $C_{NR/SS}$ = C_{FF} = 10 nF

図 18. Load Transient vs Time and Slew Rate

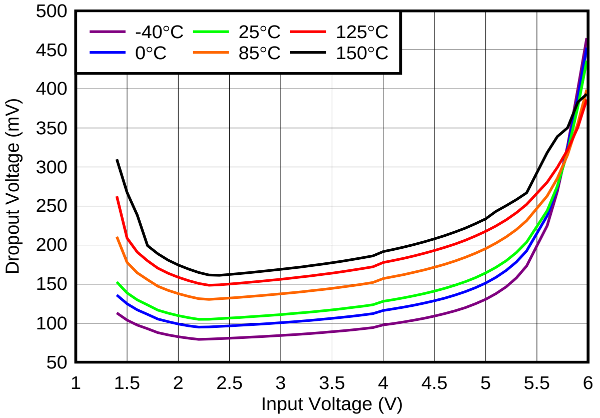
Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(NOM)}$ + 0.4 V (whichever is greater), V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{OUT} = 47 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted)



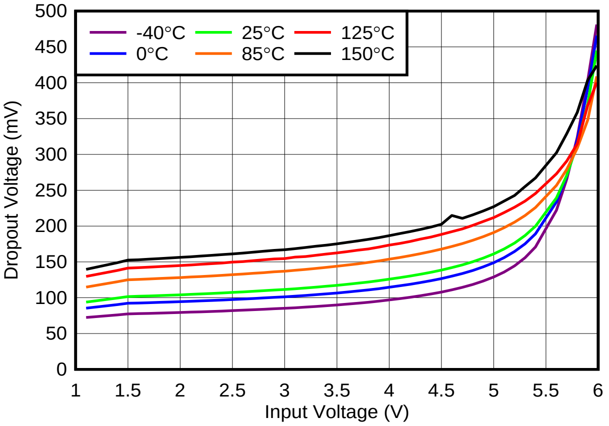
V_{IN} = 1.2 V, V_{BIAS} = 5.0 V, C_{OUT} = 47 µF || 10 µF || 10 µF, $C_{NR/SS}$ = C_{FF} = 10 nF, slew rate = 1 A/µs

図 19. Load Transient vs Time and DC Load (V_{OUT} = 0.9 V)



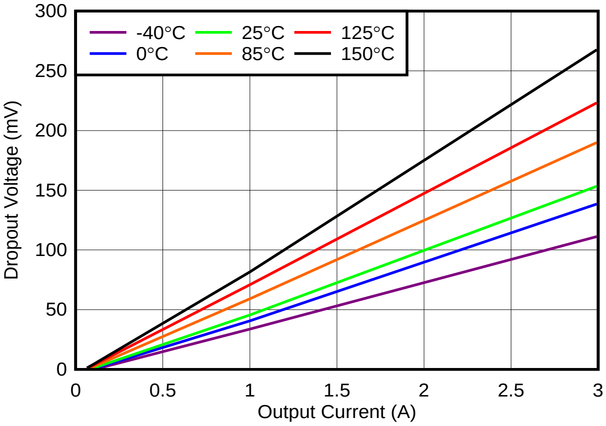
I_{OUT} = 3 A, V_{BIAS} = 0 V

図 20. Dropout Voltage vs Input Voltage Without Bias



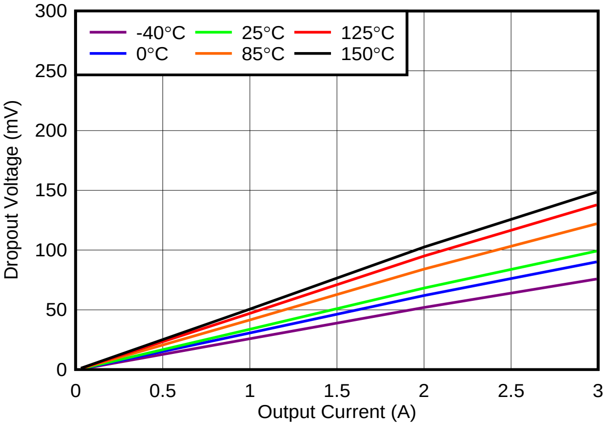
I_{OUT} = 3 A, V_{BIAS} = 6.5 V

図 21. Dropout Voltage vs Input Voltage With Bias



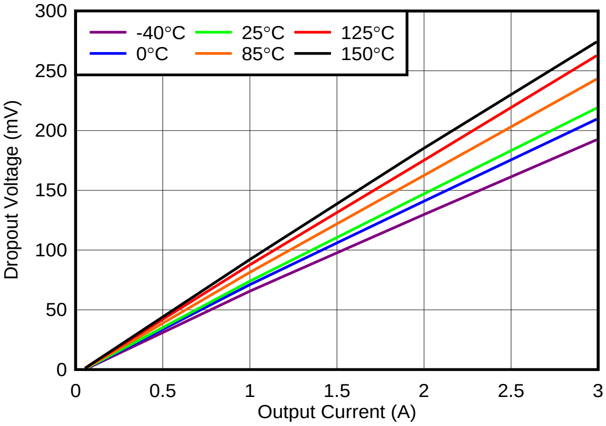
V_{IN} = 1.4 V, V_{BIAS} = 0 V

図 22. Dropout Voltage vs Output Current Without Bias



V_{IN} = 1.1 V, V_{BIAS} = 3 V

図 23. Dropout Voltage vs Output Current With Bias

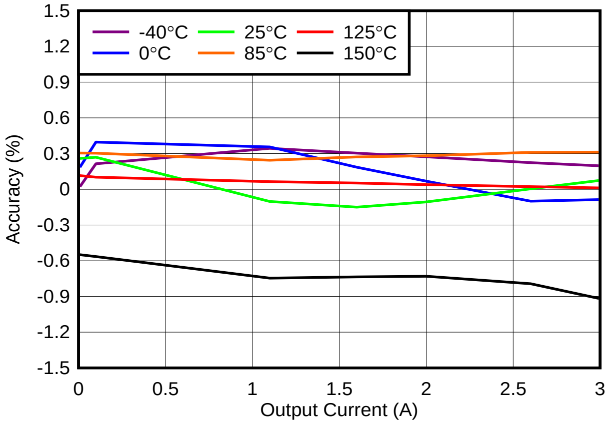


V_{IN} = 5.5 V

図 24. Dropout Voltage vs Output Current (High V_{IN})

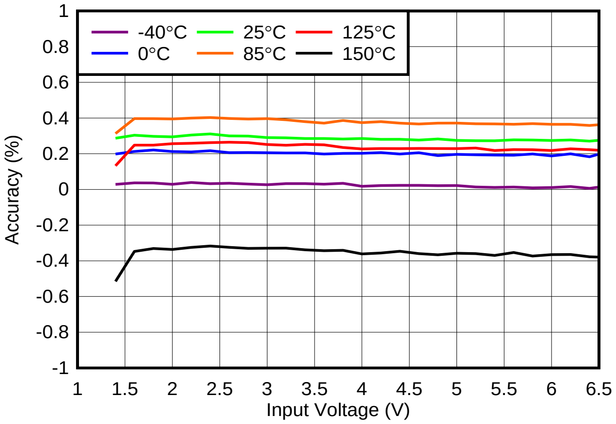
Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(NOM)}$ + 0.4 V (whichever is greater), V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{OUT} = 47 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted)



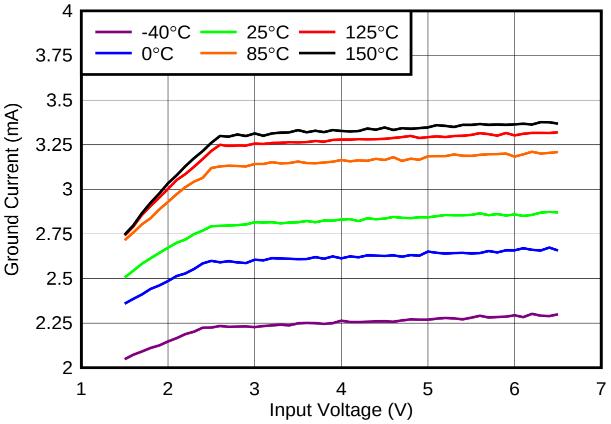
V_{IN} = 1.4 V, V_{BIAS} = 0 V

図 25. Load Regulation With Bias



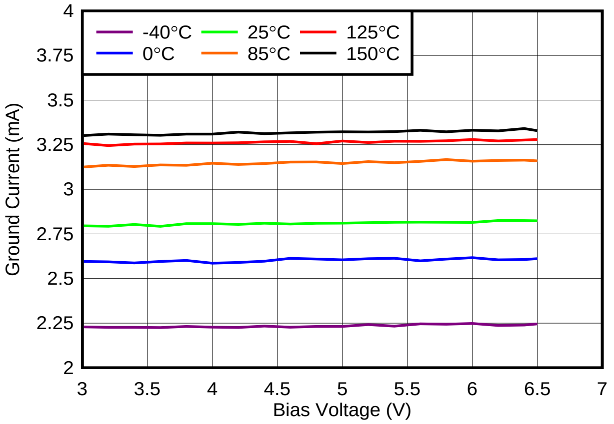
V_{OUT} = 0.8 V, V_{BIAS} = 0 V, I_{OUT} = 5 mA

図 26. Line Regulation Without Bias



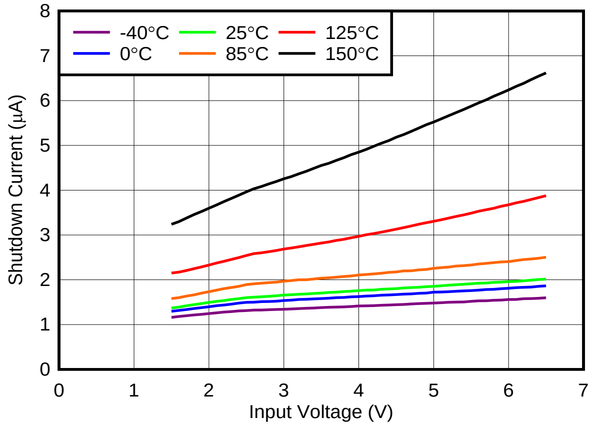
V_{BIAS} = 0 V, I_{OUT} = 5 mA

図 27. Quiescent Current vs Input Voltage



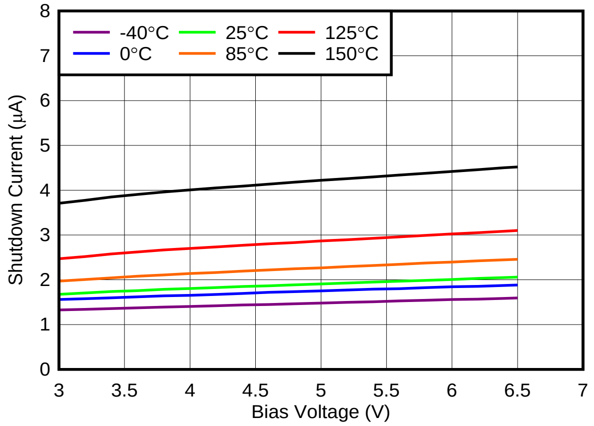
V_{IN} = 1.1 V, I_{OUT} = 5 mA

図 28. Quiescent Current vs Bias Voltage



V_{BIAS} = 0 V

図 29. Shutdown Current vs Input Voltage

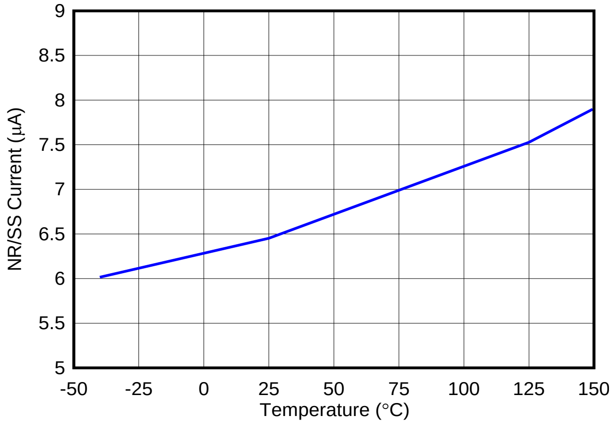


V_{IN} = 1.1 V

図 30. Shutdown Current vs Bias Voltage

Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(NOM)}$ + 0.4 V (whichever is greater), V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{OUT} = 47 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted)



V_{BIAS} = 0 V

図 31. NR/SS Current vs Temperature

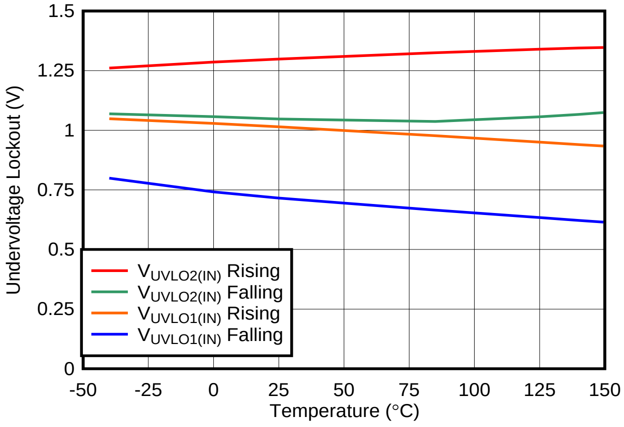
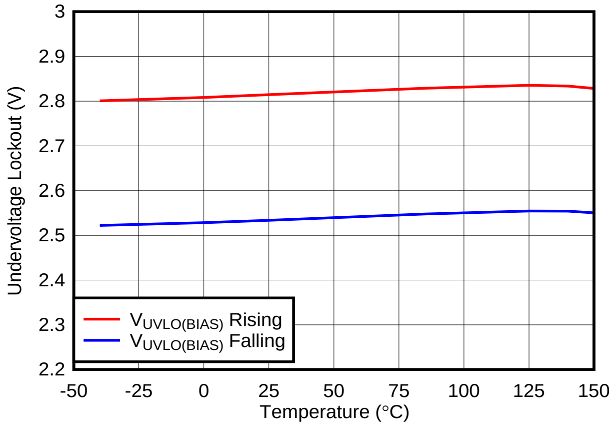
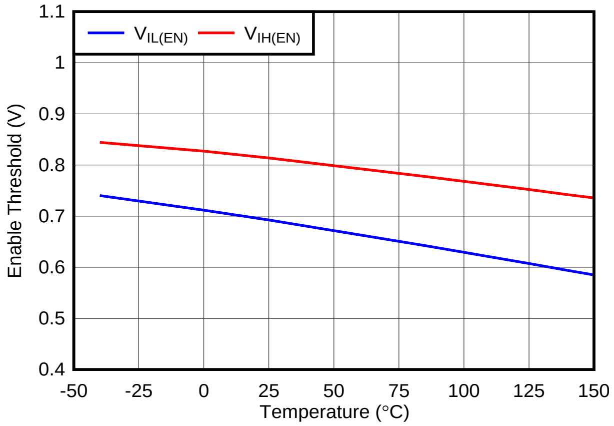


図 32. V_{IN} UVLO vs Temperature



V_{IN} = 1.1 V

図 33. V_{BIAS} UVLO vs Temperature



V_{IN} = 1.4 V, 6.5 V

図 34. Enable Threshold vs Temperature

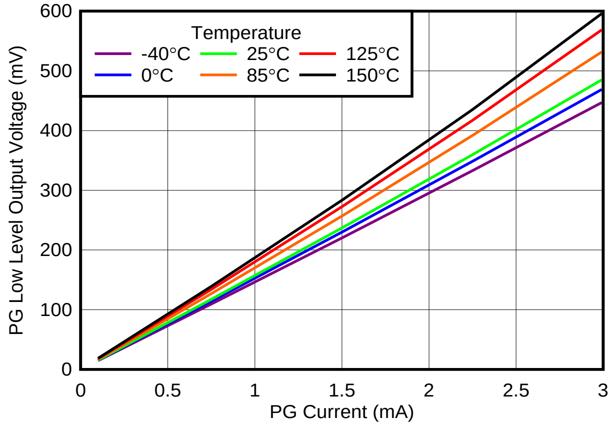
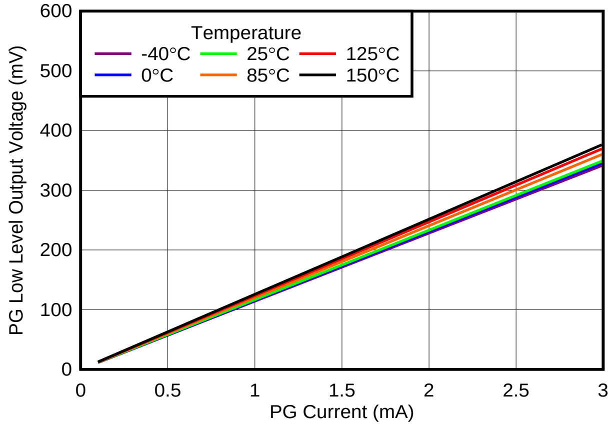


図 35. PG Voltage vs PG Current Sink



V_{IN} = 6.5 V

図 36. PG Voltage vs PG Current Sink

Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(NOM)}$ + 0.4 V (whichever is greater), V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{OUT} = 47 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted)

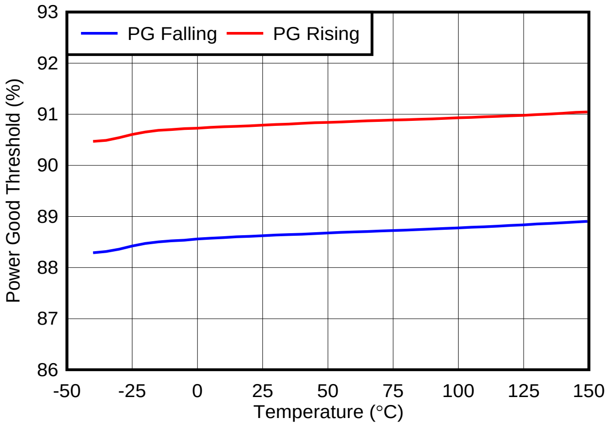
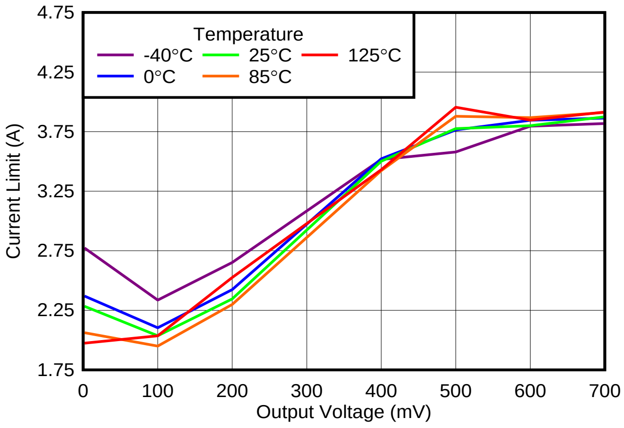


図 37. PG Threshold vs Temperature



Temperature limited because of power dissipation

図 38. Foldback Current Limit vs Output Voltage

7 Detailed Description

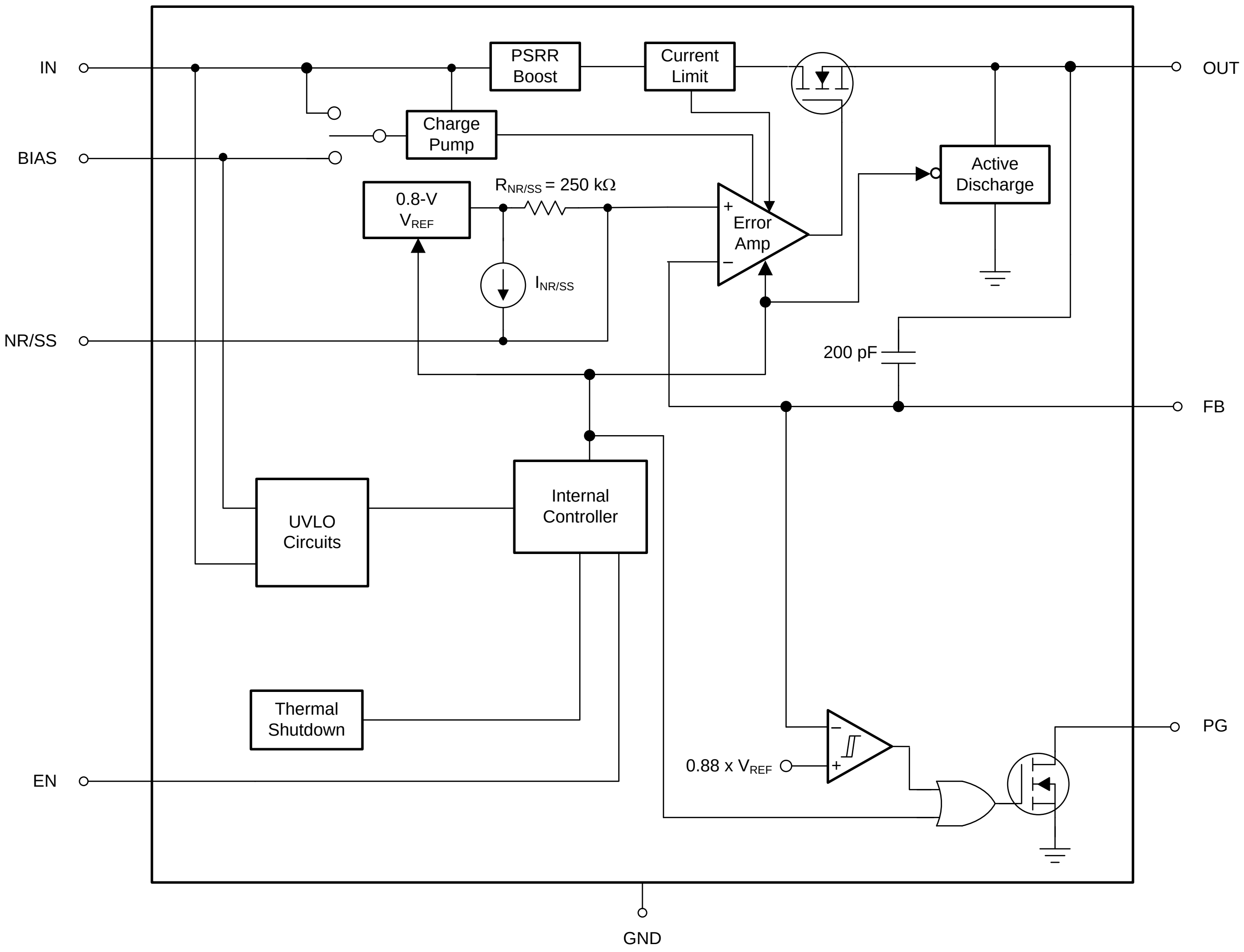
7.1 Overview

The TPS7A53-Q1 is a high-current (3 A), low-noise (4.4 µV_{RMS}), high-accuracy (1%), low-dropout linear voltage regulator with an input range of 1.1 V to 6.5 V and an output voltage range of 0.8 V to 5.15 V. The TPS7A53-Q1 has an integrated charge pump for ease of use, and an external bias rail to allow for the lowest dropout across the entire output voltage range. 表 1 categorizes the functions shown in the *Functional Block Diagram*. These features make the TPS7A53-Q1 a robust solution to solve many challenging problems by generating a clean, accurate power supply in a variety of applications.

表 1. Device Features

VOLTAGE REGULATION	SYSTEM START-UP	INTERNAL PROTECTION
High accuracy	Programmable soft start	Foldback current limit
Low-noise, high-PSRR output	No sequencing requirement between BIAS, IN, and EN	Thermal shutdown
Fast transient response	Power-good output	
	Start-up with negative bias on OUT	

7.2 Functional Block Diagram



7.3 Feature Description

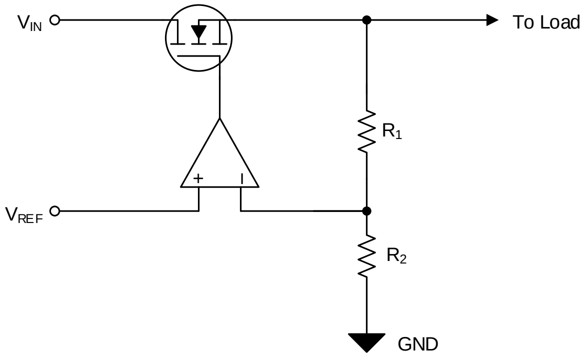
7.3.1 Voltage Regulation Features

7.3.1.1 DC Regulation

An LDO, as shown in 図 39, functions as a class-B amplifier in which the input signal is the internal reference voltage (V_{REF}). V_{REF} is designed to have a very low bandwidth at the input to the error amplifier through the use of a low-pass filter ($V_{NR/SS}$).

As such, the reference can be considered as a pure dc input signal. The low output impedance of an LDO comes from the combination of the output capacitor and pass element. The pass element also presents a high input impedance to the source voltage when operating as a current source. A positive LDO can only source current because of the class-B architecture.

This device achieves a maximum of 1% output voltage accuracy primarily because of the high-precision band-gap voltage (V_{BG}) that creates V_{REF}. The low dropout voltage (V_{DO}) reduces the thermal power dissipation required by the device to regulate the output voltage at a given current level, thereby improving system efficiency. These features combine to make this device a good approximation of an ideal voltage source.



NOTE: $V_{OUT} = V_{REF} \times (1 + R_1 / R_2)$.

図 39. Simplified Regulation Circuit

7.3.1.2 AC and Transient Response

The LDO responds quickly to a transient (large-signal response) on the input supply (line transient) or the output current (load transient) resulting from the LDO high-input impedance and low output-impedance across frequency. This same capability also means that the LDO has a high power-supply rejection ratio (PSRR) and, when coupled with a low internal noise-floor (V_n), the LDO approximates an ideal power supply in ac (small-signal) and large-signal conditions.

The choice of external component values optimizes the small- and large-signal response. The NR/SS capacitor ($C_{NR/SS}$) and feed-forward capacitor (C_{FF}) easily reduce the device noise floor and improve PSRR.

Feature Description (continued)

7.3.2 System Start-Up Features

In many different applications, the power-supply output must turn on within a specific window of time to either provide proper operation of the load or to minimize the loading on the input supply or other sequencing requirements. The LDO start-up is well-controlled and user-adjustable, solving the demanding requirements faced by many power-supply design engineers in a simple fashion.

7.3.2.1 Programmable Soft Start (NR/SS Pin)

Soft start directly controls the output start-up time and indirectly controls the output current during start-up (inrush current).

The external capacitor at the NR/SS pin ($C_{NR/SS}$), as shown in 図 40, sets the output start-up time by setting the rise time of the internal reference ($V_{NR/SS}$).

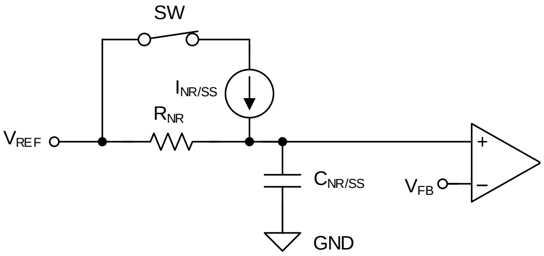


図 40. Simplified Soft-Start Circuit

7.3.2.2 Internal Sequencing

Controlling when a single power supply turns on can be difficult in a power distribution network (PDN) because of the high power levels inherent in a PDN, and the variations between all of the supplies. As shown in 図 41 and 表 2, the LDO turnon and turnoff time is set by the enable circuit (EN) and undervoltage lockout circuits ($UVLO_{1,2(IN)}$ and $UVLO_{BIAS}$).

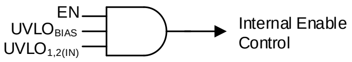


図 41. Simplified Turnon Control

表 2. Internal Sequencing Functionality Table

INPUT VOLTAGE	BIAS VOLTAGE	ENABLE STATUS	LDO STATUS	ACTIVE DISCHARGE	POWER GOOD
$V_{IN} \geq V_{UVLO\_1,2(IN)}$	$V_{BIAS} \geq V_{UVLO(BIAS)}$	EN = 1	On	Off	PG = 1 when $V_{OUT} \geq V_{IT(PG)}$
		EN = 0	Off	On	PG = 0
	$V_{BIAS} < V_{UVLO(BIAS)} + V_{HYS(BIAS)}$	EN = don't care	Off	On (1)	
$V_{IN} < V_{UVLO\_1,2(IN)} - V_{HYS1,2(IN)}$	BIAS = don't care		Off		
IN = don't care	$V_{BIAS} \geq V_{UVLO(BIAS)}$		Off		

(1) The active discharge remains on as long as V_{IN} or V_{BIAS} provide enough headroom for the discharge circuit to function.

7.3.2.2.1 Enable (EN)

The enable signal (V_{EN}) is an active-high digital control that enables the LDO when the enable voltage is past the rising threshold ($V_{EN} \geq V_{IH(EN)}$) and disables the LDO when the enable voltage is below the falling threshold ($V_{EN} \leq V_{IL(EN)}$). The exact enable threshold is between $V_{IH(EN)}$ and $V_{IL(EN)}$ because EN is a digital control. Connect EN to V_{IN} if enable functionality is not desired.

7.3.2.2.2 Undervoltage Lockout (UVLO) Control

The UVLO circuits respond quickly to glitches on IN or BIAS and attempt to disable the output of the device if either of these rails collapse.

7.3.2.2.3 Active Discharge

When either EN or UVLO are low, the device connects a resistor of several hundred ohms from V_{OUT} to GND, discharging the output capacitance.

Do not rely on the active discharge circuit for discharging large output capacitors when the input voltage drops below the targeted output voltage. Current flows from the output to the input (reverse current) when $V_{OUT} > V_{IN}$, which can cause damage to the device (when $V_{OUT} > V_{IN} + 0.3$ V).

7.3.2.3 Power-Good Output (PG)

The PG signal provides an easy solution to meet demanding sequencing requirements because PG signals when the output nears its nominal value. PG can be used to signal other devices in a system when the output voltage is near, at, or above the set output voltage ($V_{OUT(nom)}$). 図 42 shows a simplified schematic.

The PG signal is an open-drain digital output that requires a pullup resistor to a voltage source and is active high. The PG circuit sets the PG pin into a high-impedance state to indicate that the power is good.

Using a large feed-forward capacitor (C_{FF}) delays the output voltage and, because the PG circuit monitors the FB pin, the PG signal can indicate a false positive.

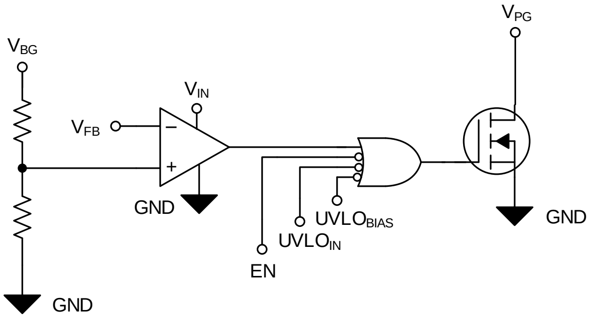


図 42. Simplified PG Circuit

7.3.3 Internal Protection Features

In many applications, fault events can occur that damage devices in the system. Short circuits and excessive heat are the most common fault events for power supplies. The TPS7A53-Q1 implements circuitry to protect the device and its load during these events. Continuously operating in these fault conditions or above a junction temperature of 140°C is not recommended because the long-term reliability of the device is reduced.

7.3.3.1 Foldback Current Limit (I_{CL})

The internal current limit circuit is used to protect the LDO against high load-current faults or shorting events. During a current-limit event, the LDO sources constant current; therefore, the output voltage falls with decreased load impedance. Thermal shutdown can activate during a current limit event because of the high power dissipation typically found in these conditions. For proper operation of the current limit, minimize the inductances to the input and load. Continuous operation in current limit is not recommended.

7.3.3.2 Thermal Protection (T_{sd})

The thermal shutdown circuit protects the LDO against excessive heat in the system, either resulting from current limit or high ambient temperature.

The output of the LDO turns off when the LDO temperature (junction temperature, T_J) exceeds the rising thermal shutdown temperature. The output turns on again after T_J decreases below the falling thermal shutdown temperature.

A high power dissipation across the device, combined with a high ambient temperature (T_A), can cause T_J to be greater than or equal to T_{sd}, triggering the thermal shutdown and causing the output to fall to 0 V. The LDO can cycle on and off when thermal shutdown is reached under these conditions.

7.4 Device Functional Modes

表 3 provides a quick comparison between the regulation and disabled operation.

表 3. Device Functional Modes Comparison

OPERATING MODE	PARAMETER				
	V_{IN}	V_{BIAS}	EN	I_{OUT}	T_J
Regulation (1)	$V_{IN} > V_{OUT(nom)} + V_{DO}$	$V_{BIAS} \geq V_{UVLO(BIAS)}$ (2)	$V_{EN} > V_{IH(EN)}$	$I_{OUT} < I_{CL}$	$T_J \leq T_{J(maximum)}$
Disabled (3)	$V_{IN} < V_{UVLO\_1,2(IN)}$	$V_{BIAS} < V_{UVLO(BIAS)}$	$V_{EN} < V_{IL(EN)}$	—	$T_J > T_{sd}$

(1) All table conditions must be met.
(2) V_{BIAS} is only required for $V_{IN} < 1.4$ V.
(3) The device is disabled when any condition is met.

7.4.1 Regulation

The device regulates the output to the nominal output voltage when all the conditions in 表 3 are met.

7.4.2 Disabled

When disabled, the pass device is turned off, the internal circuits are shut down, and the output voltage is actively discharged to ground by an internal resistor from the output to ground. See the *Active Discharge* section for additional information.

7.4.3 Current Limit Operation

During a current-limit event, the LDO regulates the output current instead of the output voltage; therefore, the output voltage falls with decreased load impedance.

8 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Successfully implementing an LDO in an application depends on the application requirements. This section discusses key device features and how to best implement them to achieve a reliable design.

8.1.1 Recommended Capacitor Types

The TPS7A53-Q1 is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input, output, and noise-reduction pin (NR, pin 13). Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and COG-rated dielectric materials provide relatively good capacitive stability across temperature. The use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, ceramic capacitance varies with operating voltage and temperature. Make sure to derate ceramic capacitors by at least 50%. The input and output capacitors recommended herein account for a capacitance derating of approximately 50%, but at high V_{IN} and V_{OUT} conditions (V_{IN} = 5.5 V to V_{OUT} = 5.0 V), the derating can be greater than 50%, and must be taken into consideration.

8.1.1.1 Input and Output Capacitor Requirements (C_{IN} and C_{OUT})

The TPS7A53-Q1 is designed and characterized for operation with ceramic capacitors of 47 µF or greater (22 µF or greater of capacitance) at the output and 10 µF or greater (5 µF or greater of capacitance) at the input. Use at least a 47-µF capacitor at the input to minimize input impedance. Place the input and output capacitors as near as practical to the respective input and output pins in order to minimize trace parasitics. If the trace inductance from the input supply to the TPS7A53-Q1 is high, a fast current transient can cause V_{IN} to ring above the absolute maximum voltage rating and damage the device. This situation can be mitigated by additional input capacitors to dampen and keep the ringing below the device absolute maximum ratings.

A combination of multiple output capacitors boosts the high-frequency PSRR. The combination of one 0805-sized, 47-µF ceramic capacitor in parallel with two 0805-sized, 10-µF ceramic capacitors with a sufficient voltage rating, in conjunction with the PSRR boost circuit, optimizes PSRR for the frequency range of 400 kHz to 700 kHz, a typical range for dc-dc supply switching frequency. This 47-µF || 10-µF || 10-µF capacitor combination also makes certain that at high input voltage and high output voltage configurations, the minimum effective capacitance is met. Many 0805-sized, 47-µF ceramic capacitors have a voltage derating of approximately 60% to 80% at 5.0 V, so the addition of the two 10-µF capacitors makes sure that the capacitance is at or above 22 µF.

Application Information (continued)

8.1.1.2 Noise-Reduction and Soft-Start Capacitor ($C_{NR/SS}$)

The TPS7A53-Q1 features a programmable, monotonic, voltage-controlled soft start that is set with an external capacitor ($C_{NR/SS}$). Use an external $C_{NR/SS}$ to minimize inrush current into the output capacitors. This soft-start feature eliminates power-up initialization problems when powering field-programmable gate arrays (FPGAs), digital signal processors (DSPs), or other processors. The controlled voltage ramp of the output also reduces peak inrush current during start-up, minimizing start-up transients to the input power bus.

To achieve a monotonic start-up, the TPS7A53-Q1 error amplifier tracks the voltage ramp of the external soft-start capacitor until the voltage approaches the internal reference. The soft-start ramp time depends on the soft-start charging current ($I_{NR/SS}$), the soft-start capacitance ($C_{NR/SS}$), and the internal reference ($V_{NR/SS}$). 式 1 calculates soft-start ramp time:

$$t_{SS} = (V_{NR/SS} \times C_{NR/SS}) / I_{NR/SS} \tag{1}$$

$I_{NR/SS}$ is provided in the *Electrical Characteristics* table and has a typical value of 6.2 µA.

The noise-reduction capacitor, in conjunction with the noise-reduction resistor, forms a low-pass filter (LPF) that filters out the noise from the reference before being gained up with the error amplifier, thereby reducing the device noise floor. The LPF is a single-pole filter and 式 2 can calculate the cutoff frequency. The typical value of R_{NR} is 250 kΩ. Increasing the $C_{NR/SS}$ capacitor has a greater affect because the output voltage increases when the noise from the reference is gained up even more at higher output voltages. For low-noise applications, a 10-nF to 1-µF $C_{NR/SS}$ is recommended.

$$f_{cutoff} = 1 / (2 \times \pi \times R_{NR} \times C_{NR/SS}) \tag{2}$$

8.1.1.3 Feed-Forward Capacitor (C_{FF})

Although a feed-forward capacitor (C_{FF}) from the FB pin to the OUT pin is not required to achieve stability, a 10-nF external feed-forward capacitor optimizes the transient, noise, and PSRR performance. A higher capacitance C_{FF} can be used; however, the start-up time is longer and the power-good signal can incorrectly indicate that the output voltage is settled. For a detailed description, see *Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator*.

8.1.2 Soft Start and Inrush Current

Soft start refers to the ramp-up characteristic of the output voltage during LDO turnon after EN and UVLO achieve threshold voltage. The noise-reduction capacitor serves a dual purpose of both governing output noise reduction and programming the soft-start ramp during turnon.

Inrush current is defined as the current into the LDO at the IN pin during start-up. Inrush current then consists primarily of the sum of load current and the current used to charge the output capacitor. This current is difficult to measure because the input capacitor must be removed, which is not recommended. However, 式 3 can estimate this soft-start current:

$$I_{OUT(t)} = \left[\frac{C_{OUT} \times dV_{OUT}(t)}{dt}\right] + \left[\frac{V_{OUT}(t)}{R_{LOAD}}\right]$$

where:

- $V_{OUT}(t)$ is the instantaneous output voltage of the turnon ramp
- $dV_{OUT}(t)$ / dt is the slope of the V_{OUT} ramp
- R_{LOAD} is the resistive load impedance (3)

Application Information (continued)

8.1.3 Optimizing Noise and PSRR

Improve the ultra-low noise floor and PSRR of the device by careful selection of:

- $C_{NR/SS}$ for the low-frequency range
- C_{FF} in the midband frequency range
- C_{OUT} for the high-frequency range
- $V_{IN} – V_{OUT}$ for all frequencies, and
- V_{BIAS} at lower input voltages

A larger noise-reduction capacitor improves low-frequency PSRR by filtering any noise coupling from the input into the reference. To improve midband PSRR, use the feed-forward capacitor to place a pole-zero pair near the edge of the loop bandwidth and push out the loop bandwidth. Use larger output capacitors to improve high-frequency PSRR.

A higher input voltage improves the PSRR by giving the device more headroom to respond to noise on the input. A bias rail also improves the PSRR at lower input voltages because greater headroom is provided for the internal circuits.

The noise-reduction capacitor filters out low-frequency noise from the reference, and the feed-forward capacitor reduces output voltage noise by filtering out the midband frequency noise. However, a large feed-forward capacitor can create new issues that are discussed in *Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator*.

Use a large output capacitor to reduce high-frequency output voltage noise. Additionally, a bias rail or higher input voltage improves the noise because greater headroom is provided for the internal circuits.

表 4 lists the output voltage noise for the 10-Hz to 100-kHz band at a 5.0-V output for a variety of conditions with an input voltage of 5.4 V, an R_1 of 12.1 kΩ, and a load current of 3 A. The 5.0-V output is used because this output is the worst-case condition for output voltage noise.

表 4. Output Noise Voltage at a 5.0-V Output

OUTPUT VOLTAGE NOISE (μV_{RMS})	$C_{NR/SS}$ (nF)	C_{FF} (nF)	C_{OUT} (µF)
11.7	10	10	47 || 10 || 10
7.7	100	10	47 || 10 || 10
6	100	100	47 || 10 || 10
7.4	100	10	1000
5.8	100	100	1000

8.1.4 Charge Pump Noise

The device internal charge pump generates a minimal amount of noise. Use a bias rail to minimize the internal charge pump noise when the internal voltage is clamped, thereby reducing the overall output noise floor.

The high-frequency components of the output voltage noise density curves are filtered out in most applications by using 10-nF to 100-nF bypass capacitors close to the load. Using a ferrite bead between the LDO output and the load input capacitors forms a pi-filter, further reducing the high-frequency noise contribution.

8.1.5 Current Sharing

Current sharing is possible through the use of external operational amplifiers. For more details, see TI Design, *Current-Sharing Dual LDOs*, and verified reference design *6 A Current-Sharing Dual LDO*.

8.1.6 Adjustable Operation

As shown in 図 43, the output voltage of the TPS7A53-Q1 is set using external resistors.

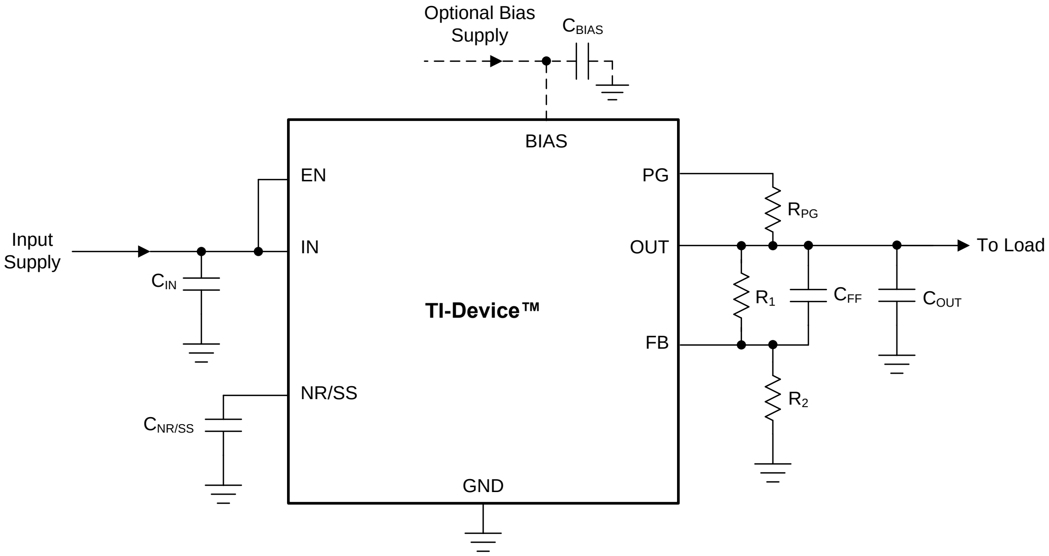

図 43. Adjustable Operation

Use 式 4 to calculate R_1 and R_2 for any output voltage range. This resistive network must provide a current equal to or greater than 5 µA for dc accuracy. To optimize the noise and PSRR, use an R_1 of 12.1 kΩ.

$$V_{OUT} = V_{NR/SS} \times (1 + R_1 / R_2) \quad (4)$$

表 5 shows the resistor combinations required to achieve several common rails using standard 1%-tolerance resistors.

表 5. Recommended Feedback-Resistor Values

TARGETED OUTPUT VOLTAGE (V)	FEEDBACK RESISTOR VALUES[1]		CALCULATED OUTPUT VOLTAGE (V)
	R_1 (kΩ)	R_2 (kΩ)	
0.9	12.4	100	0.899
0.95	12.4	66.5	0.949
1.00	12.4	49.9	0.999
1.10	12.4	33.2	1.099
1.20	12.4	24.9	1.198
1.50	12.4	14.3	1.494
1.80	12.4	10	1.798
1.90	12.1	8.87	1.89
2.50	12.4	5.9	2.48
2.85	12.1	4.75	2.838
3.00	12.1	4.42	2.990
3.30	11.8	3.74	3.324
3.60	12.1	3.48	3.582
4.5	11.8	2.55	4.502
5.00	12.4	2.37	4.985

(1) R_1 is connected from OUT to FB; R_2 is connected from FB to GND.

8.1.7 Power-Good Operation

For proper operation of the power-good circuit, the pullup resistor value must be between 10 kΩ and 100 kΩ. The lower limit of 10 kΩ results from the maximum pulldown strength of the power-good transistor, and the upper limit of 100 kΩ results from the maximum leakage current at the power-good node. If the pullup resistor is outside of this range, then the power-good signal may not read a valid digital logic level.

Using a large C_{FF} with a small $C_{NR/SS}$ causes the power-good signal to incorrectly indicate that the output voltage has settled during turnon. The C_{FF} time constant must be greater than the soft-start time constant for proper operation of the PG during start-up. For a detailed description, see *Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator*.

The state of PG is only valid when the device operates above the minimum supply voltage. During short UVLO events and at light loads, power-good does not assert because the output voltage is sustained by the output capacitance.

8.1.8 Undervoltage Lockout (UVLO) Operation

The UVLO circuit makes sure that the device remains disabled before the input or bias supplies reach the minimum operational voltage range, and that the device shuts down when the input supply or bias supply falls too low.

The UVLO circuit has a minimum response time of several microseconds to fully assert. During this time, a downward line transient below approximately 0.8 V causes the UVLO to assert for a short time; however, the UVLO circuit does not have enough stored energy to fully discharge the internal circuits inside of the device. When the UVLO circuit does not fully discharge, the internal circuits of the output are not fully disabled.

The effect of the downward line transient can be mitigated by either using a larger input capacitor to limit the fall time of the input supply when operating near the minimum V_{IN}, or by using a bias rail.

図 44 shows the UVLO circuit response to various input voltage events. The diagram can be separated into the following regions:

- Region A: The device does not turn on until the input reaches the UVLO rising threshold.
- Region B: Normal operation with a regulated output.
- Region C: Brownout event above the UVLO falling threshold (UVLO rising threshold – UVLO hysteresis). The output may fall out of regulation but the device is still enabled.
- Region D: Normal operation with a regulated output.
- Region E: Brownout event below the UVLO falling threshold. The device is disabled in most cases and the output falls because of the load and active discharge circuit. The device is reenabled when the UVLO rising threshold is reached by the input voltage and a normal start-up then follows.
- Region F: Normal operation followed by the input falling to the UVLO falling threshold.
- Region G: The device is disabled when the input voltage falls below the UVLO falling threshold to 0 V. The output falls because of the load and active discharge circuit.

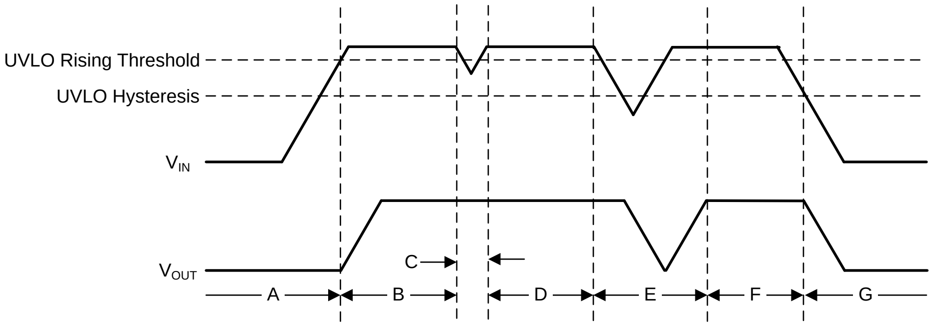

図 44. Typical UVLO Operation

8.1.9 Dropout Voltage (V_{DO})

Generally speaking, the dropout voltage often refers to the minimum voltage difference between the input and output voltage ($V_{DO} = V_{IN} – V_{OUT}$) that is required for regulation. When V_{IN} drops below the required V_{DO} for the given load current, the device functions as a resistive switch and does not regulate output voltage. Dropout voltage is proportional to the output current because the device is operating as a resistive switch.

Dropout voltage is affected by the drive strength for the gate of the pass element, which is nonlinear with respect to V_{IN} on this device because of the internal charge pump. The charge pump causes a higher dropout voltage at lower input voltages when a bias rail is not used.

For this device, dropout voltage increases exponentially when the input voltage nears its maximum operating voltage because the charge pump is internally clamped to 8.0 V.

8.1.10 Device Behavior During Transition From Dropout Into Regulation

Some applications have transients that place the device into dropout, especially with a device such as a high-current linear regulator. A typical application with these transient conditions may require setting $V_{IN} \leq (V_{OUT} + V_{DO})$ in order to keep the device junction temperature within the specified operating range. A load transient or line transient with these conditions can place the device into dropout; for example, a load transient from 1 A to 4 A at 1 A/µs when operating with a V_{IN} of 5.4 V and a V_{OUT} of 5.0 V.

The load transient saturates the error amplifier output stage when the gate of the pass element is driven as high as possible by the error amplifier, thus making the pass element function like a resistor from V_{IN} to V_{OUT}. The error amplifier response time to this load transient (I_{OUT} = 4 A to 1 A at 1 A/µs) is limited because the error amplifier must first recover from saturation, and then place the pass element back into active mode. During the recovery from the load transient, V_{OUT} overshoots because the pass element is functioning as a resistor from V_{IN} to V_{OUT}. If operating under these conditions, apply a higher dc load or increase the output capacitance in order to reduce the overshoot.

8.1.11 Load Transient Response

The load-step transient response is the output voltage response by the LDO to a step in load current, whereby output voltage regulation is maintained. There are two key transitions during a load transient response: the transition from a light to a heavy load, and the transition from a heavy to a light load. The regions shown in 図 45 are broken down in this section. Regions A, E, and H are where the output voltage is in steady-state regulation.

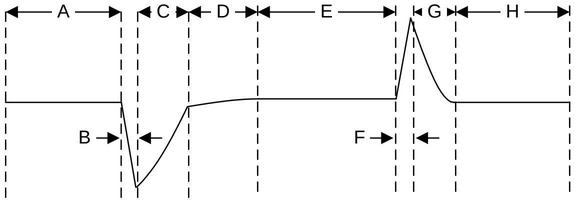

図 45. Load Transient Waveform

During transitions from a light load to a heavy load:

- Initial voltage dip is a result of the depletion of the output capacitor charge and parasitic impedance to the output capacitor (region B)
- Recovery from the dip results from the LDO increasing its sourcing current, and leads to output voltage regulation (region C)

During transitions from a heavy load to a light load:

- Initial voltage rise results from the LDO sourcing a large current, and leads to the output capacitor charge to increase (region F)
- Recovery from the rise results from the LDO decreasing its sourcing current in combination with the load discharging the output capacitor (region G)

Transitions between current levels changes the internal power dissipation because the TPS7A53-Q1 is a high-current device (region D). The change in power dissipation changes the die temperature during these transitions, and leads to a slightly different voltage level. This different output voltage level shows up in the various load transient responses.

A larger output capacitance reduces the peaks during a load transient but slows down the response time of the device. A larger dc load also reduces the peaks because the amplitude of the transition is lowered and a higher current discharge path is provided for the output capacitor.

8.1.12 Reverse Current Protection Considerations

As with most LDOs, this device can be damaged by excessive reverse current.

Conditions where excessive reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} > V_{IN} + 0.3$ V:

- If the device has a large C_{OUT}, then the input supply collapses quickly and the load current becomes very small
- The output is biased when the input supply is not established
- The output is biased above the input supply

If an excessive reverse current flow is expected in the application, then external protection must be used to protect the device. 図 46 shows one approach of protecting the device.

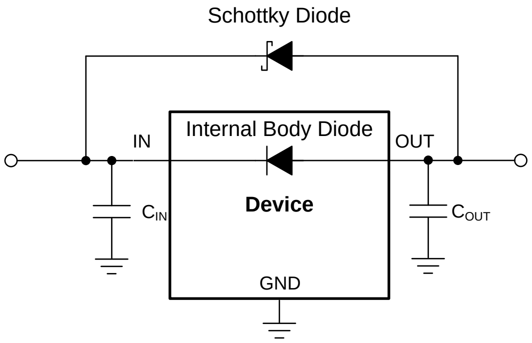

図 46. Example Circuit for Reverse Current Protection Using a Schottky Diode

8.1.13 Power Dissipation (P_D)

Circuit reliability demands that proper consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Use 式 5 to calculate P_D:

$$P_D = (V_{OUT} – V_{IN}) \times I_{OUT} \tag{5}$$

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Power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the TPS7A53-Q1 allows for maximum efficiency across a wide range of output voltages.

The primary heat conduction path for the package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. According to 式 6, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A). 式 6 is rearranged in 式 7 for output current.

$$T_J = T_A + (R_{\theta JA} \times P_D) \tag{6}$$

$$I_{OUT} = (T_J – T_A) / [R_{\theta JA} \times (V_{IN} – V_{OUT})] \tag{7}$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Electrical Characteristics* table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the VQFN package junction-to-case (bottom) thermal resistance ($R_{\theta JC(bot)}$) plus the thermal resistance contribution by the PCB copper.

8.1.14 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are used in accordance with 式 8 and are given in the *Electrical Characteristics* table.

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \times P_D$$

$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \times P_D$$

where:

- P_D is the power dissipated as explained in 式 5
- T_T is the temperature at the center-top of the device package, and
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge (8)

8.2 Typical Application

This section discusses the implementation of the TPS7A53-Q1 using an adjustable feedback network to regulate a 3-A load requiring good PSRR at high frequency with low-noise at an output voltage of 5.0 V. 図 47 provides a schematic for this typical application circuit.

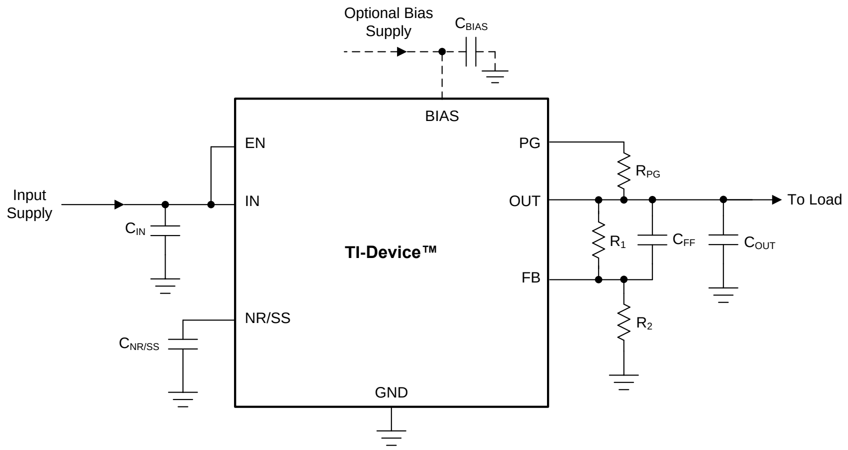

図 47. Typical Application for a 5.0-V Rail

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 6 as the input parameters.

表 6. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	5.50 V, ±1%, provided by the dc-dc converter switching at 500 kHz
Bias voltage	Not used because $V_{OUT} \geq 2.20$ V
Output voltage	5.0 V, ±1%
Output current	3.0 A (maximum), 10 mA (minimum)
RMS noise, 10 Hz to 100 kHz	< 10 μV_{RMS}
PSRR at 500 kHz	> 40 dB
Start-up time	< 25 ms

8.2.2 Detailed Design Procedure

At 3.0 A and 5.0 V_{OUT}, the dropout of the TPS7A53-Q1 has a 340-mV maximum dropout over temperature; thus, a 500-mV headroom is sufficient for operation over both input and output voltage accuracy. At full load and high temperature on some devices, the TPS7A53-Q1 can enter dropout if both the input and output supply are beyond the edges of the respective accuracy specification.

For a 5.0-V output. use external adjustable resistors. See the resistor values in listed 表 5 for choosing resistors for a 5.0-V output.

Input and output capacitors are selected in accordance with the *Recommended Capacitor Types* section. Ceramic capacitances of 47 µF for the input and one 47-µF capacitor in parallel with two 10-µF capacitors for the output are selected.

To satisfy the required start-up time and still maintain low noise performance, a 100-nF $C_{NR/SS}$ is selected. 式 9 calculates this value.

$$t_{SS} = (V_{NR/SS} \times C_{NR/SS}) / I_{NR/SS} \quad (9)$$

At the 3.0-A maximum load, the internal power dissipation is 1.5 W and corresponds to a 53.1°C junction temperature rise for the RGR package on a standard JEDEC board. With an 55°C maximum ambient temperature, the junction temperature is at 108.1°C. To further minimize noise, a feed-forward capacitance (C_{FF}) of 10 nF is selected.

8.2.3 Application Curves

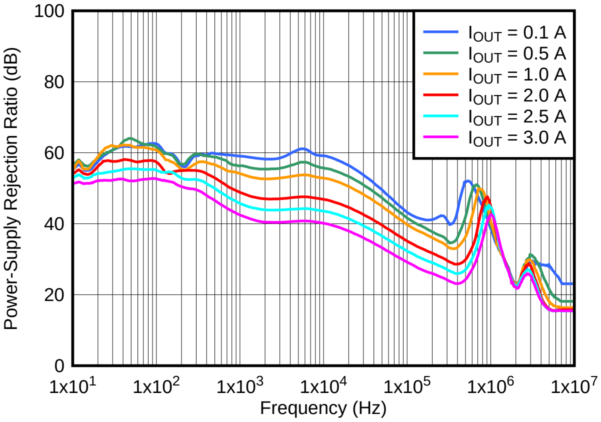

図 48. PSRR vs Frequency and I_{OUT} for V_{OUT} = 5.0 V

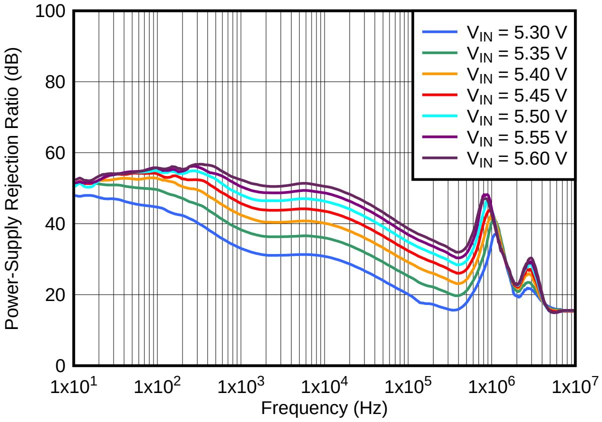

図 49. PSRR vs Frequency and V_{IN} for V_{OUT} = 5.0 V at I_{OUT} = 3.0 A

9 Power Supply Recommendations

The TPS7A53-Q1 is designed to operate from an input voltage supply range between 1.1 V and 6.5 V. If the input supply is less than 1.4 V, then a bias rail of at least 3.0 V must be used. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, use additional input capacitors with low ESR to help improve output noise performance.

10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. To avoid negative system performance, do not use of vias and long traces to the input and output capacitors. The grounding and layout scheme illustrated in 図 50 minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability.

To improve performance, use a ground reference plane, either embedded in the PCB itself or placed on the bottom side of the PCB opposite the components. This reference plane serves to provide accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device when connected to the thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

10.1.2 RTK Package — High CTE Mold Compound

The RTK package uses a mold compound with a high coefficient of thermal expansion (CTE) of 12 ppm/°C. This mold compound allows for the CTE of the packaged IC to more closely match the CTE of a conventional FR4 PCB (~14 ppm/°C to 17 ppm/°C). This CTE match is important when considering the effects that temperature swings can induce on a board with large differences in CTE values. Package and board combinations with widely dissimilar CTEs can experience mechanical cracking or fracturing of the solder joints caused by frequent changes in temperature, and the corresponding differences in expansion. Devices with normal mold compounds in similar packages typically have CTE values that are 25% lower than values found with the RTK package.

10.2 Layout Example

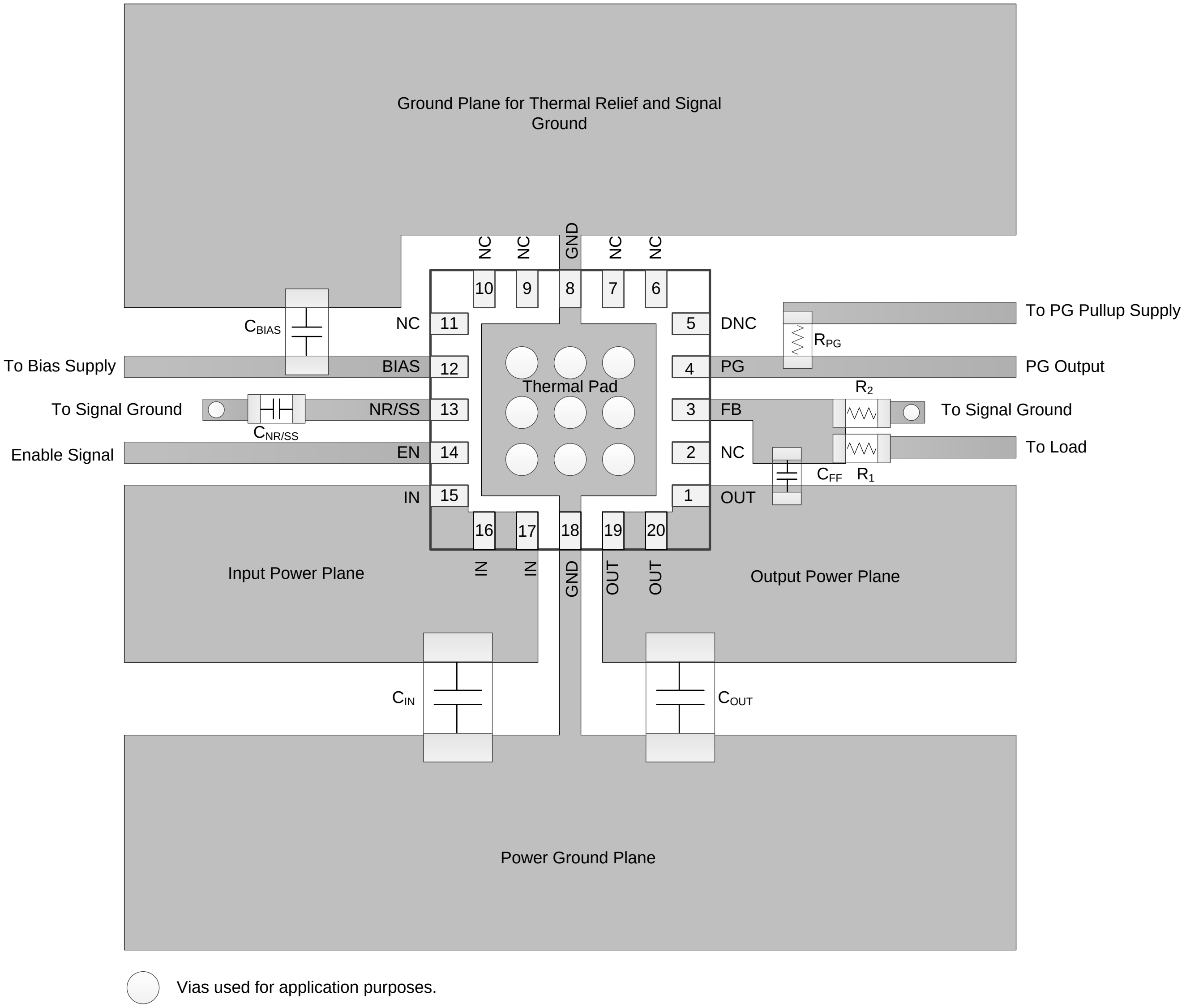

図 50. Example Layout

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

11.1.1.1 リファレンス・デザイン

関連するTIリファレンス・デザインについては、以下を参照してください。

TI Design - 電流共有のデュアルLDO (TIDA-00270)

11.1.2 デバイスの項目表記

表 7. 製品情報(1)

製品名	概要
TPS7A5301Q**YYYZ** Q1	**YYY**はパッケージ指定子です。 **Z**はパッケージ数量です。

(1) 最新のパッケージと発注情報については、このデータシートの末尾にあるパッケージ・オプションの付録を参照するか、www.ti.comにあるデバイスの製品フォルダをご覧ください。

11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下を参照してください。

- *『TPS3702 高精度の過電圧および低電圧モニタ』*
- *『低ドロップアウト・レギュレータでフィードフォワード・コンデンサを使用することの長所と短所』*
- *『6A電流共有デュアルLDO』*

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E（Engineer-to-Engineer）コミュニティ。***エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。

設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

11.5 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A5301QRGRRQ1	ACTIVE	VQFN	RGR	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	A5301	Samples
TPS7A5301WQRTKRQ1	ACTIVE	VQFN	RTK	20	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	5301WQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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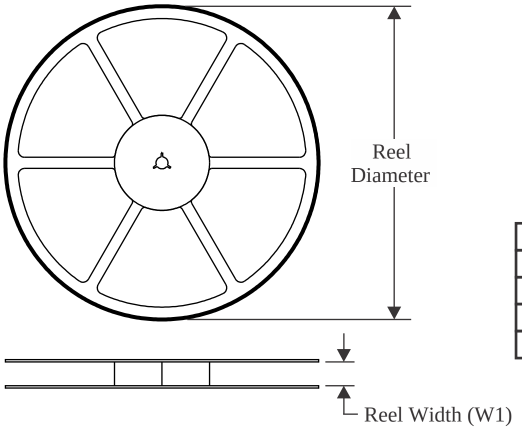
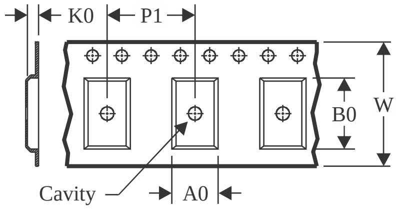
TAPE AND REEL INFORMATION

REEL DIMENSIONS

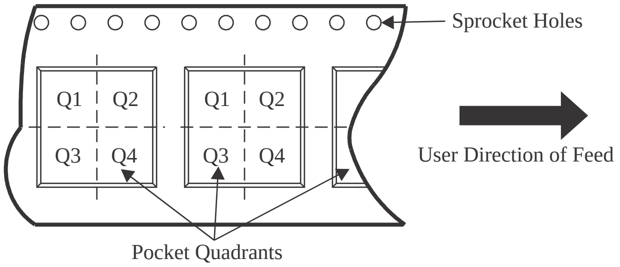


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

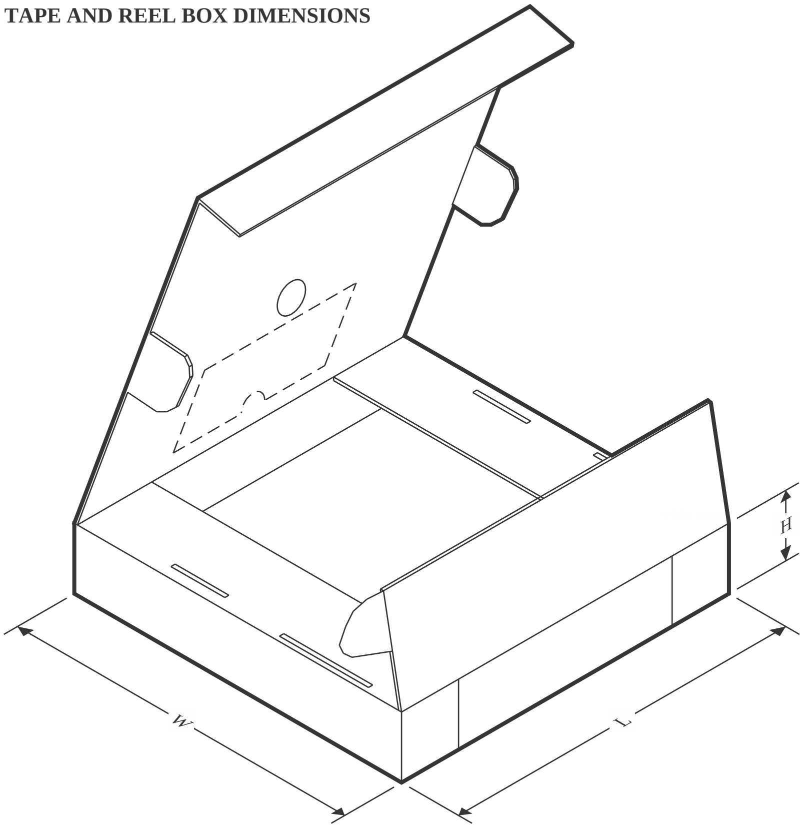
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A5301QRGRRQ1	VQFN	RGR	20	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2
TPS7A5301WQRTKRQ1	VQFN	RTK	20	3000	330.0	15.4	4.3	4.3	1.1	8.0	12.0	Q1

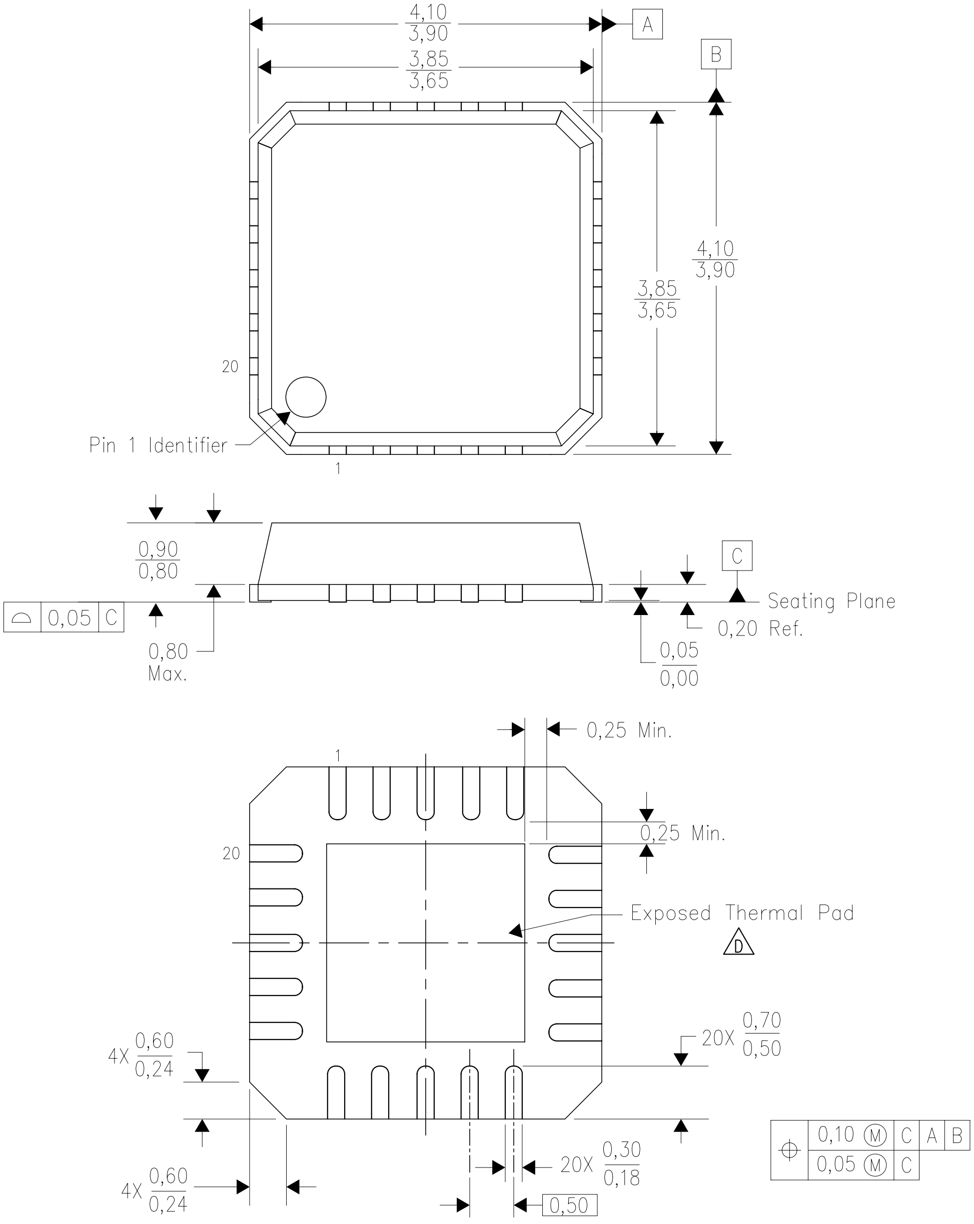
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A5301QRGRRQ1	VQFN	RGR	20	3000	367.0	367.0	35.0
TPS7A5301WQRTKRQ1	VQFN	RTK	20	3000	336.6	336.6	41.3

RTK (S-PVQFN-N20) PLASTIC QUAD FLATPACK NO-LEAD



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NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) Package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

GENERIC PACKAGE VIEW

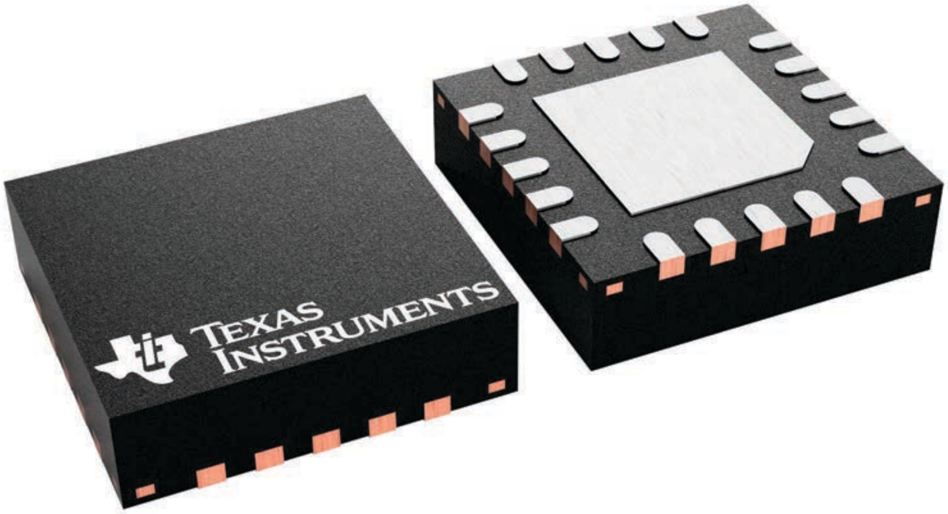
RGR 20

VQFN - 1 mm max height

3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



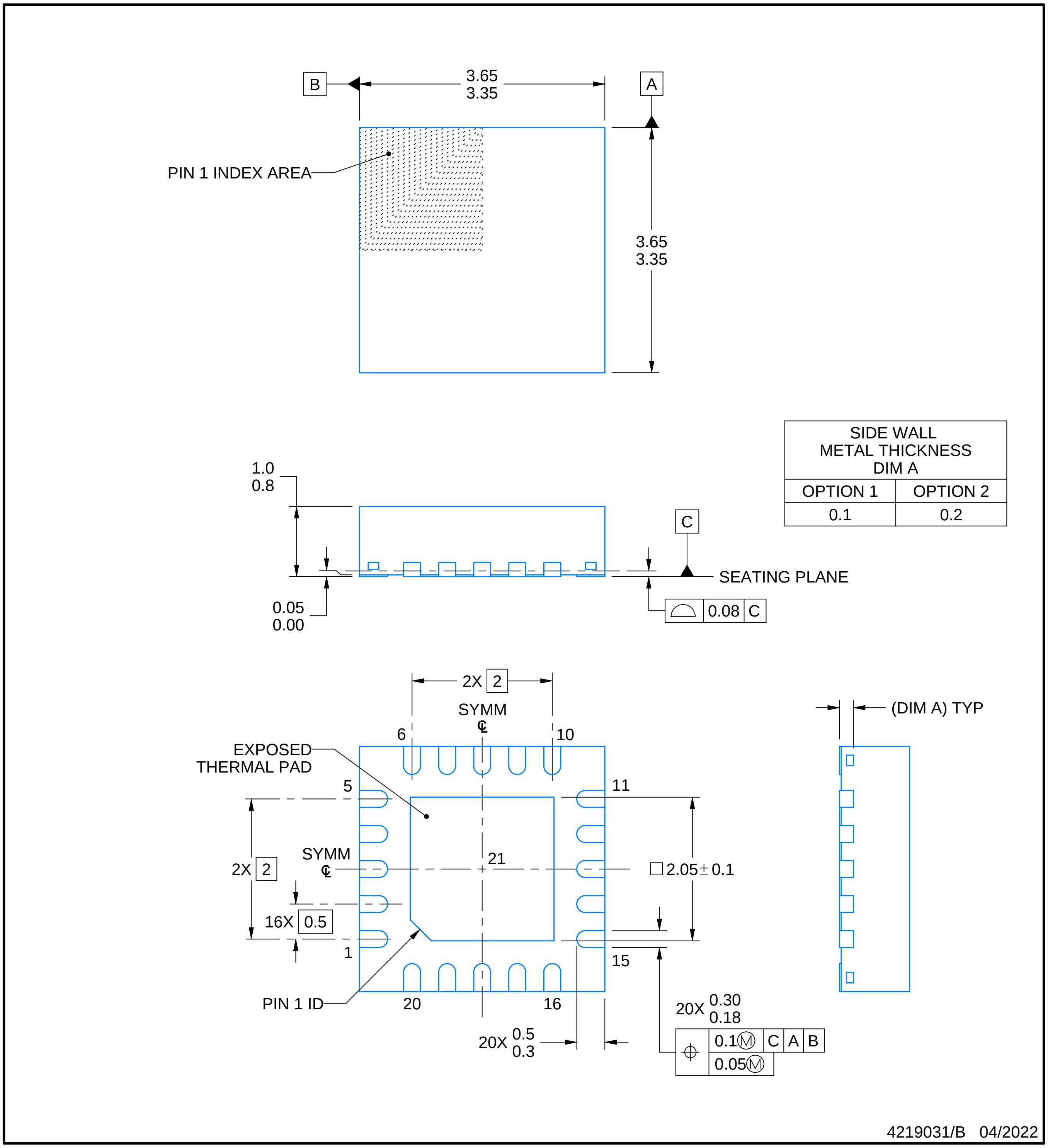
4228482/A

PACKAGE OUTLINE

RGR0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

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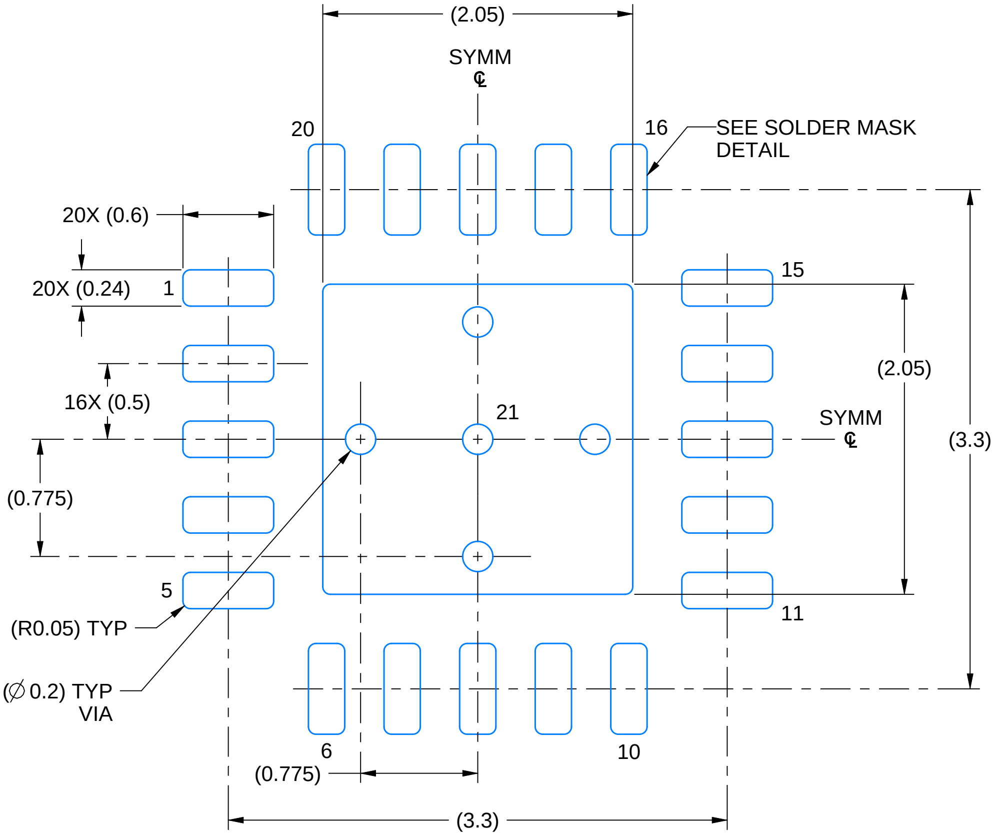
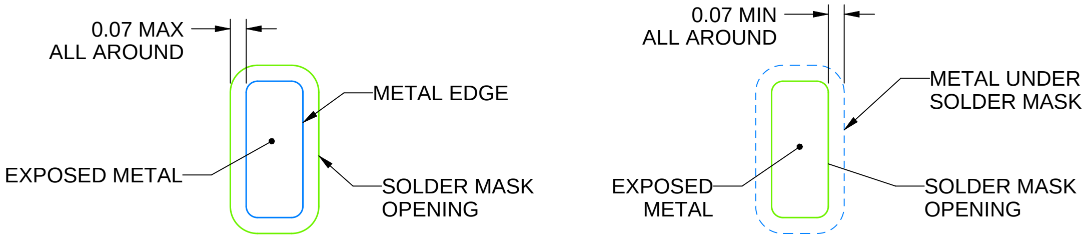
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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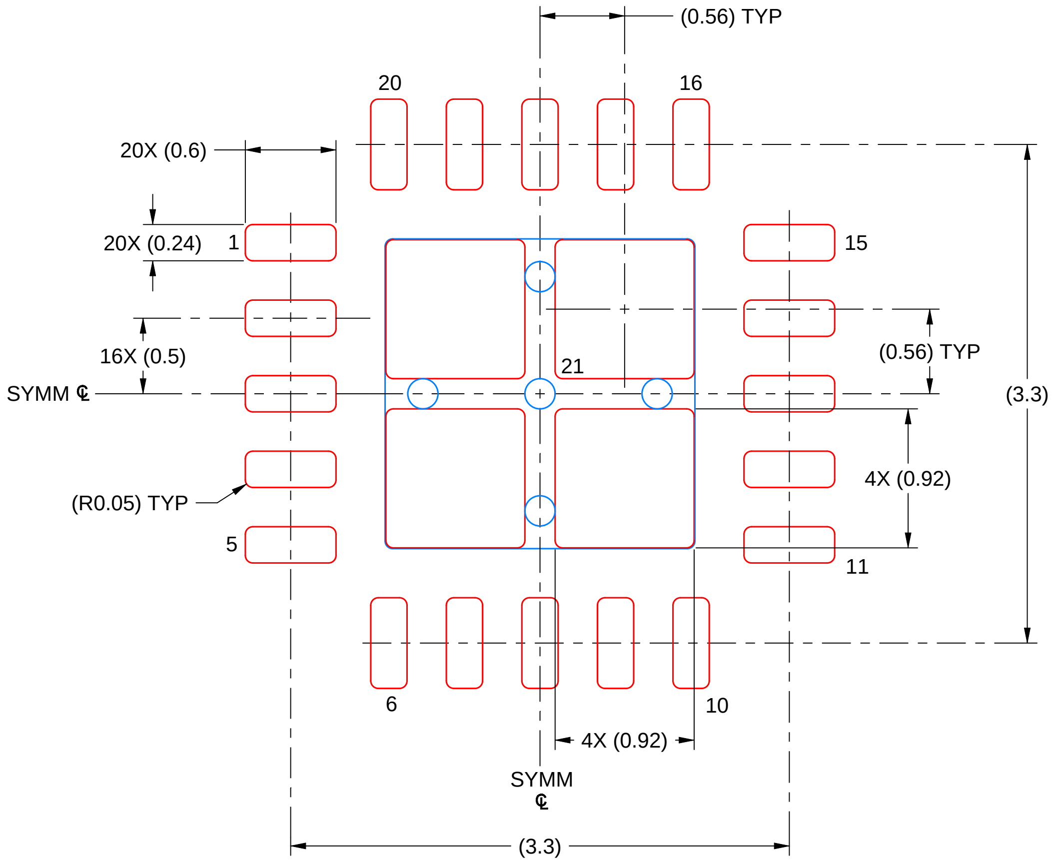
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 21
81% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265