

TPS7A65-Q1 静止電流25 μ A、300mA、40V、低ドロップアウト・レギュレータ

1 特長

- 低いドロップアウト電圧：
 - $I_{OUT} = 150\text{mA}$ で300mV
- 7V~40V の広い入力電圧範囲
最大 45V の過渡電圧に対応
- 最大出力電流：300mA
- 軽負荷時の非常に低い静止電流：25 μ A (標準値)
- 3.3V および 5V の固定出力電圧、許容誤差 $\pm 2\%$
- 低 ESR のセラミック出力安定コンデンサ
- フォルト保護機能を搭載
 - 短絡保護と過電流保護
 - サーマル・シャットダウン
- 低入力電圧トラッキング
- 熱的に強化された Power パッケージ
 - 3 ピンの TO-252 (KVU、DPAK)

2 アプリケーション

- ハイブリッド・インストルメント・クラスタ
- シフト・システム
- ヘッドアップ・ディスプレイ
- 車載用クラスタ・ディスプレイ

3 概要

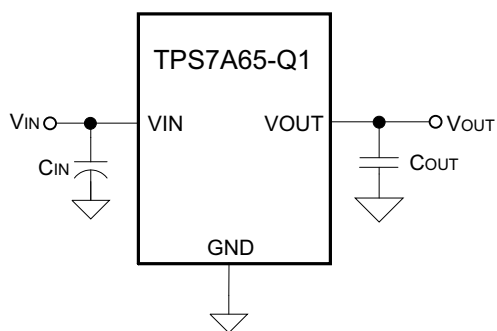
TPS7A65-Q1は低ドロップアウト・リニア電圧レギュレータで、消費電力が低く、軽負荷アプリケーションで静止電流が25 μ A未満に設計されています。このデバイスには過電流保護機能が搭載されており、低ESRのセラミック出力コンデンサでも安定して動作するよう設計されています。低電圧トラッキング機能により、小型の入力コンデンサを使用でき、コールド・クランク状況では多くの場合に昇圧コンバータが不要になります。これらの機能から、このデバイスは各種の車載アプリケーション用の電源に最適です。

製品情報⁽¹⁾

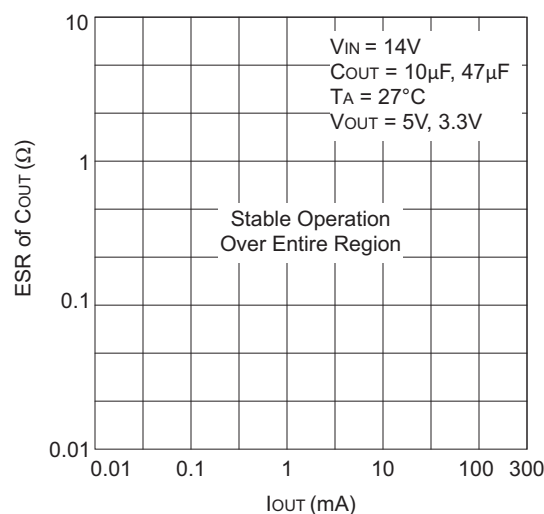
型番	パッケージ	本体サイズ(公称)
TPS7A65-Q1	TO-252 (3)	6.60mmx6.10mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

標準アプリケーション回路図



レギュレータの標準的な安定性



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision E (May 2018) から Revision F に変更	Page
• 「特長」セクションの入力電圧範囲の特長項目で 11V を 7V に変更	1
• 「アプリケーション」セクションを変更	1
• Changed V_{IN} parameter minimum specification in <i>Recommended Operating Conditions</i> table from 11 V to 7 V and added footnote	5
• Changed V_{IN} parameter minimum specification in <i>Electrical Characteristics</i> table from 11 V to 7 V and added footnote	6
• Changed 11 V to 7 V in <i>Input voltage range</i> row in <i>Design Parameters</i> table	14
• Changed input voltage range from 11 V to 40 V to 7 V to 40 V in <i>Power Supply Recommendations</i> section	16
Revision D (December 2015) から Revision E に変更	Page
• 入力電圧範囲の特長項目で 4V を 11V に変更	1
• Changed V_{IN} parameter min specifications to 11 V from 5.3 V and 3.6 V	6
• Changed 4 V to 11 V in <i>Input voltage range</i> row in <i>Design Parameters</i> table	14
• Changed 4 V to 40 V in first sentence of <i>Power Supply Recommendations</i> section	16
Revision C (December 2011) から Revision D に変更	Page
• 「ピン構成および機能」セクション、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加	1
Revision B (November 2011) から Revision C に変更	Page
• TPS7A6533QKVURQ1 を削除	1
• Changed the Regulated Output Voltage (5.1). Added to Test Conditions "10mA to 300mA, $V_{IN} = V_{OUT} + 1V$ to 16V"	6

Revision A (November 2011) から Revision B に変更**Page**

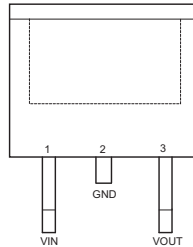
- Changed the θ_{JP} value in the Abs Max Table From: 12.7 To: 1.2°C/W 5
-

2010年5月発行のものから更新**Page**

- Removed all KKT information..... 5
-

5 Pin Configuration and Functions

**KVU Package
3-Pin TO-252
Top View**



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VIN	I	Input voltage pin: The unregulated input voltage is supplied to this pin. A bypass capacitor is connected between VIN pin and GND pin to dampen input line transients.
2	GND	I/O	Ground pin: This is signal ground pin of the IC.
3	VOUT	O	Regulated output voltage pin: This is a regulated voltage output ($V_{OUT} = 3.3\text{ V}$ or 5 V , as applicable) pin with a limitation on maximum output current. To achieve stable operation and prevent oscillation, an external output capacitor (C_{OUT}) with low ESR is connected between this pin and the GND pin.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{IN}	Unregulated input ⁽²⁾⁽³⁾		45	V
V _{OUT}	Regulated output		7	V
θ _{JP}	Thermal impedance junction to exposed pad		1.2	°C/W
T _A	Operating ambient temperature		125	°C
T _{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Absolute negative voltage on these pins not to go below -0.3 V.
- (3) Absolute maximum voltage for duration less than 480 ms.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000 V

- (1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V _{IN}	Unregulated input voltage	7 ⁽¹⁾	40	V
V _{EN}	Enable pin voltage	4	40	V
T _J	Operating junction temperature	-40	150	°C

- (1) V_{IN} can go down to 4 V for 130 ms or less and remain functional. If V_{IN} is less than 7 V for longer than 130 ms, then some devices may turn off until the input voltage rises above 7 V.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS7A65-Q1	UNIT	
		KVU (TO-252)		
		3 PINS		
R _{θJA}	Junction-to-ambient thermal resistance	High-K profile ⁽²⁾	29.3	°C/W
		Low-K profile ⁽³⁾	38.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	N/A		°C/W
R _{θJB}	Junction-to-board thermal resistance	8.2		°C/W
ψ _{JT}	Junction-to-top characterization parameter	3.4		°C/W
ψ _{JB}	Junction-to-board characterization parameter	8.1		°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	1.1		°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.
- (2) The thermal data is based on JEDEC standard high-K profile – JESD 51-5. The copper pad is soldered to the thermal land pattern. Also correct attachment procedure must be incorporated.
- (3) The thermal data is based on JEDEC standard low-K profile – JESD 51-3. The copper pad is soldered to the thermal land pattern. Also correct attachment procedure must be incorporated.

6.5 Electrical Characteristics

 $V_{IN} = 14\text{ V}$, $T_J = -40^\circ\text{C}$ to $+150^\circ\text{C}$ (unless otherwise noted)

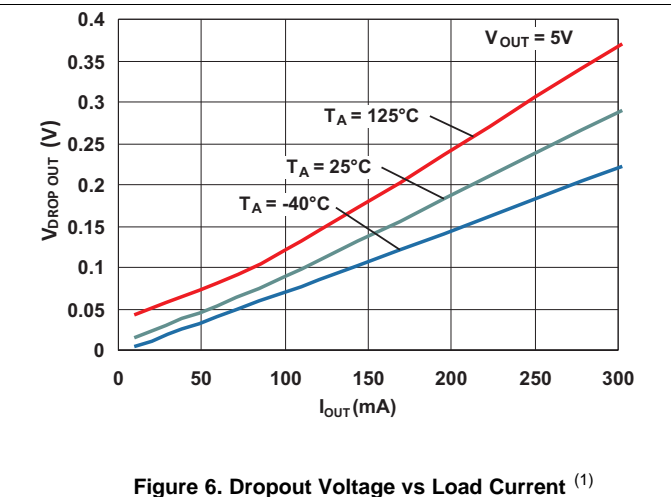
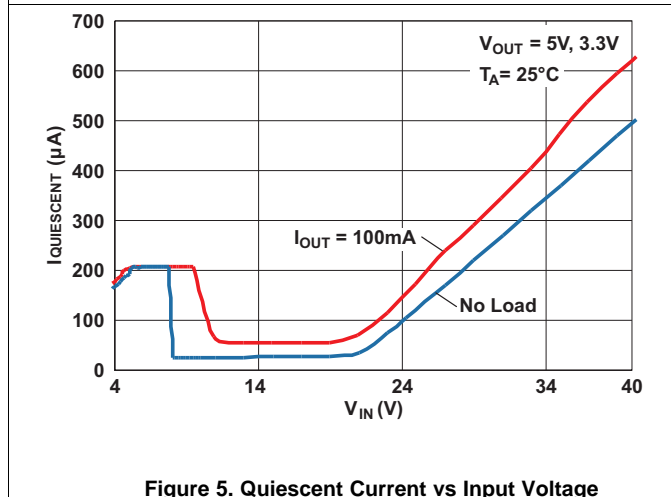
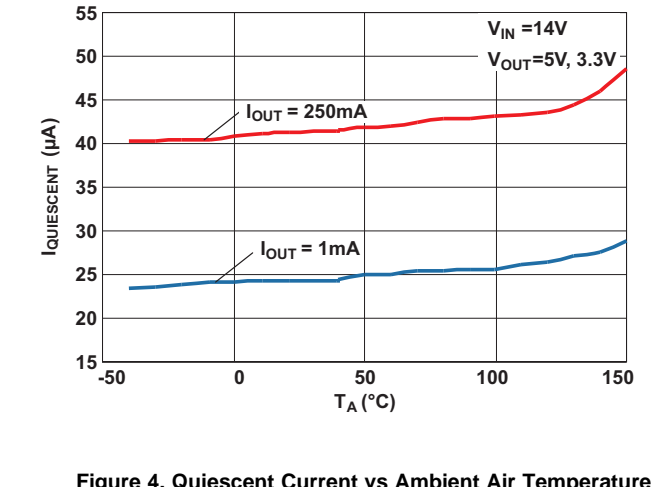
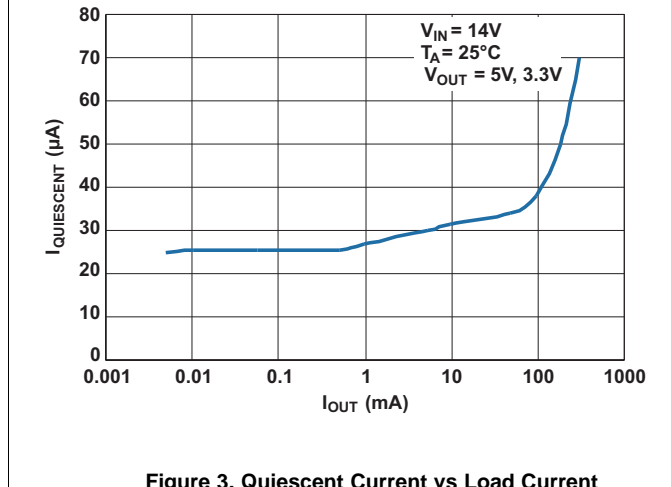
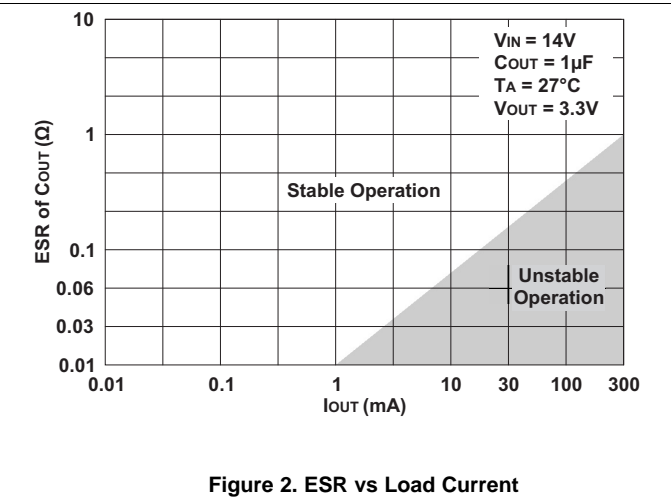
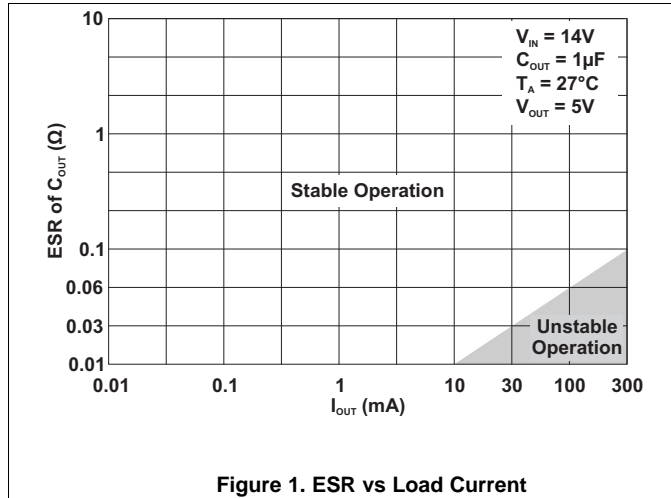
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE (VIN Pin)						
V_{IN}	Input voltage	Fixed 5-V output, $I_{OUT} = 1\text{ mA}$	7 ⁽¹⁾		40	V
		Fixed 3.3-V output, $I_{OUT} = 1\text{ mA}$	7 ⁽¹⁾		40	
$I_{QUIESCENT}$	Quiescent current	$V_{IN} = 8.2\text{ V}$ to 18 V , $I_{OUT} = 0.01\text{ mA}$ to 0.75 mA		25	40	μA
$V_{IN-UVLO}$	Undervoltage lockout voltage	Ramp V_{IN} down until output is turned OFF		3.16		V
$V_{IN(PowerUP)}$	Power-up voltage	Ramp V_{IN} up until output is turned ON		3.45		V
REGULATED OUTPUT VOLTAGE (VOUT Pin)						
V_{OUT}	Regulated output voltage	Fixed V_{OUT} value (3.3 V or 5 V as applicable), $I_{OUT} = 10\text{ mA}$, 10 mA to 300 mA, $V_{IN} = V_{OUT} + 1\text{ V}$ to 16 V	-2%		2%	
$\Delta V_{LINE-REG}$	Line regulation	$V_{IN} = 6\text{ V}$ to 28 V , $I_{OUT} = 10\text{ mA}$, $V_{OUT} = 5\text{ V}$			15	mV
		$V_{IN} = 6\text{ V}$ to 28 V , $I_{OUT} = 10\text{ mA}$, $V_{OUT} = 3.3\text{ V}$			20	
$\Delta V_{LOAD-REG}$	Load regulation	$I_{OUT} = 10\text{ mA}$ to 300 mA , $V_{IN} = 14\text{ V}$, $V_{OUT} = 5\text{ V}$			25	mV
		$I_{OUT} = 10\text{ mA}$ to 300 mA , $V_{IN} = 14\text{ V}$, $V_{OUT} = 3.3\text{ V}$			35	
$V_{DROPOUT}^{(2)}$	Dropout voltage ($V_{IN} - V_{OUT}$)	$I_{OUT} = 250\text{ mA}$			500	mV
		$I_{OUT} = 150\text{ mA}$			300	
$R_{SW}^{(3)}$	Switch resistance	V_{IN} to V_{OUT} resistance			2	Ω
I_{OUT}	Output current	V_{OUT} in regulation	0		300	mA
I_{CL}	Output current limit	$V_{OUT} = 0\text{ V}$ (V_{OUT} pin is shorted to ground)	350		1000	mA
PSRR ⁽³⁾	Power-supply ripple rejection	$V_{IN-RIPPLE} = 0.5\text{ Vpp}$, $I_{OUT} = 300\text{ mA}$, frequency = 100 Hz, $V_{OUT} = 5\text{ V}$, $V_{OUT} = 3.3\text{ V}$		60		dB
		$V_{IN-RIPPLE} = 0.5\text{ Vpp}$, $I_{OUT} = 300\text{ mA}$, frequency = 150 kHz, $V_{OUT} = 5\text{ V}$, $V_{OUT} = 3.3\text{ V}$		30		
TEMPERATURE						
$T_{SHUTDOWN}$	Thermal shutdown trip point			165		$^\circ\text{C}$
T_{HYST}	Thermal shutdown hysteresis			10		$^\circ\text{C}$

- V_{IN} can go down to 4 V for 130 ms or less and remain functional. If V_{IN} is less than 7 V for longer than 130 ms, then some devices may turn off until the input voltage rises above 7 V.
- This test is done with V_{OUT} in regulation and $V_{IN} - V_{OUT}$ parameter is measured when V_{OUT} (3.3 V or 5 V) drops by 100 mV at specified loads.
- Specified by design; not tested.

6.6 Dissipation Ratings

JEDEC STANDARD	PACKAGE	$T_A < 25^\circ\text{C}$ POWER RATING (W)	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ ($^\circ\text{C}/\text{W}$)	$T_A = 85^\circ\text{C}$ POWER RATING (W)
JEDEC Standard PCB - low K, JESD 51-3	3-pin KVU	3.24	38.6	1.68
JEDEC Standard PCB - high K, JESD 51-5	3-pin KVU	4.27	29.3	2.22

6.7 Typical Characteristics



(1) Dropout voltage is measured when the output voltage drops by 100 mV from the regulated output voltage level. (For example, the drop out voltage for TPS7A6550 is measured when the output voltage drops down to 4.9 V from 5 V.)

Typical Characteristics (continued)

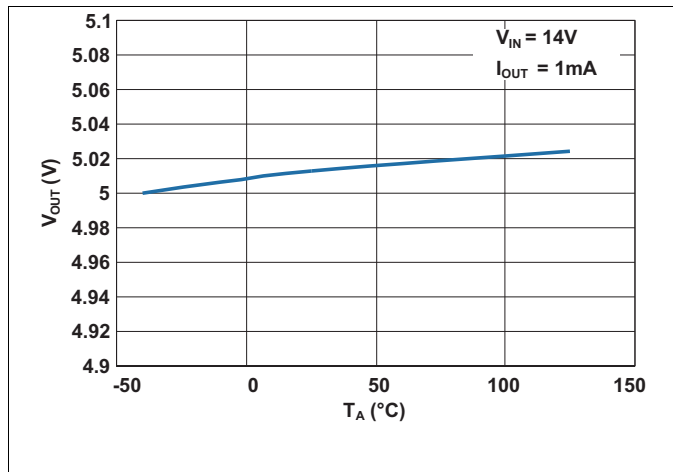


Figure 7. Output Voltage vs Ambient Air Temperature

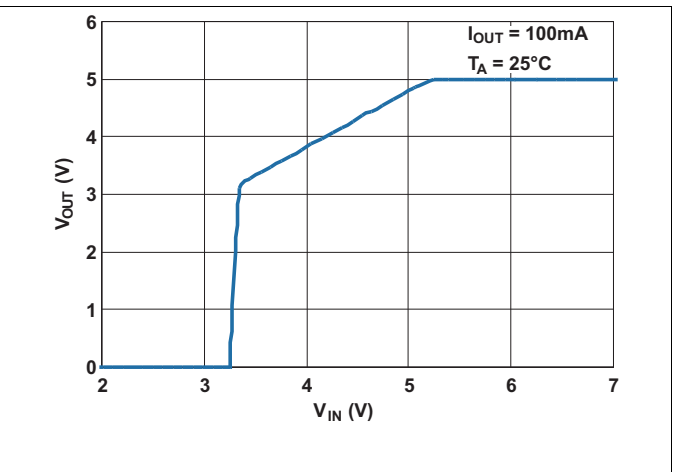


Figure 8. Output Voltage vs Input Voltage

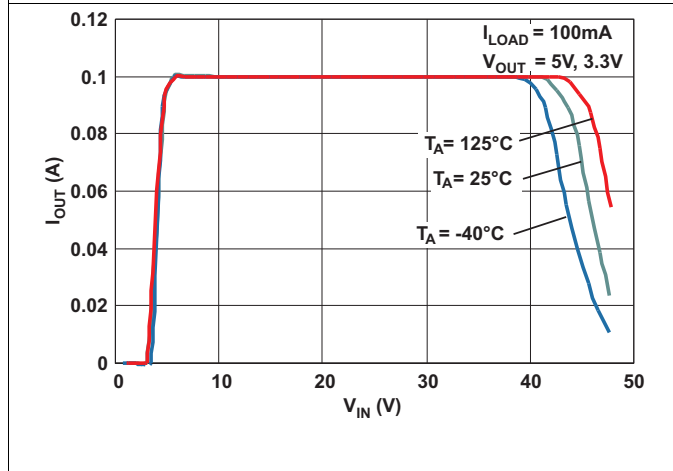


Figure 9. Output Current vs Input Voltage

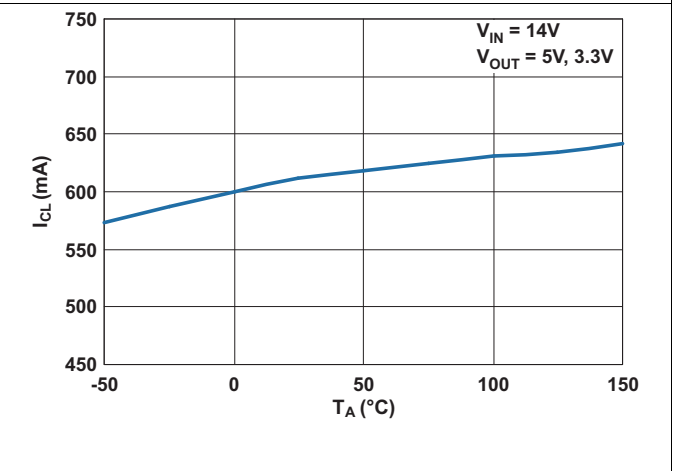


Figure 10. Output Current Limit vs Ambient Air Temperature

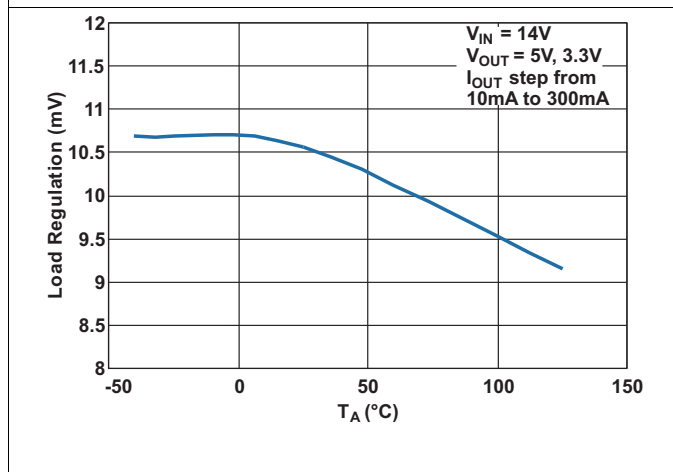


Figure 11. Load Regulation vs Ambient Air Temperature

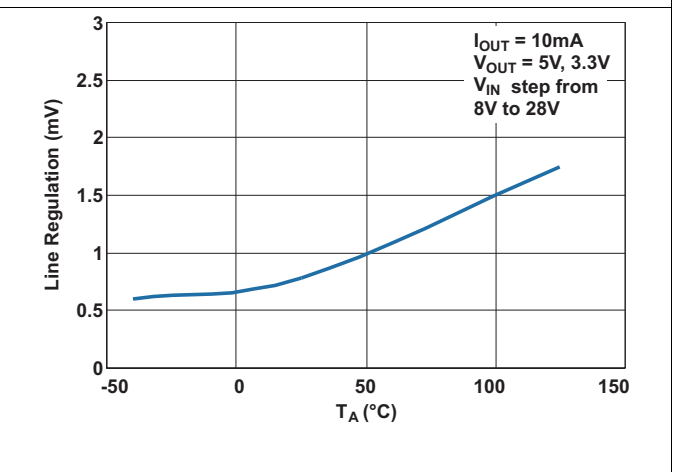
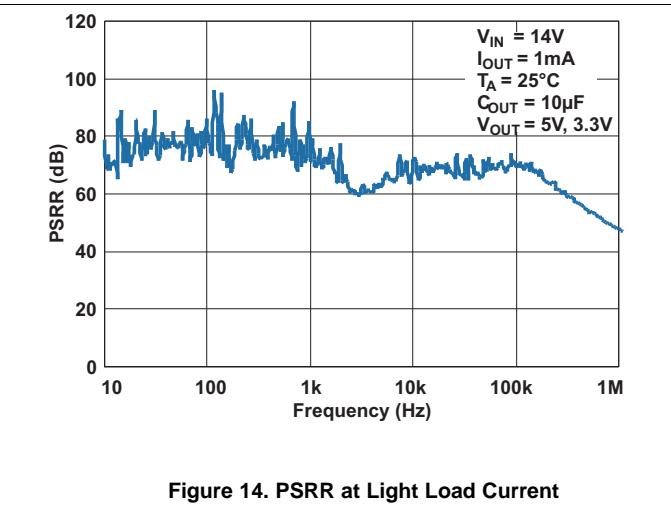
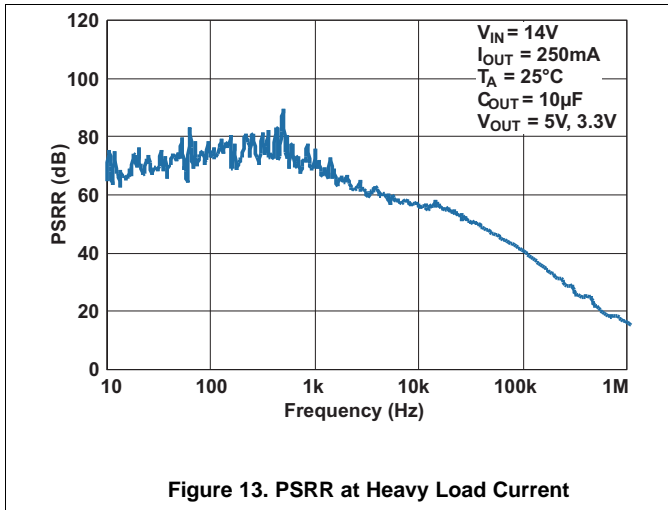


Figure 12. Line Regulation vs Ambient Air Temperature

Typical Characteristics (continued)



7 Detailed Description

7.1 Overview

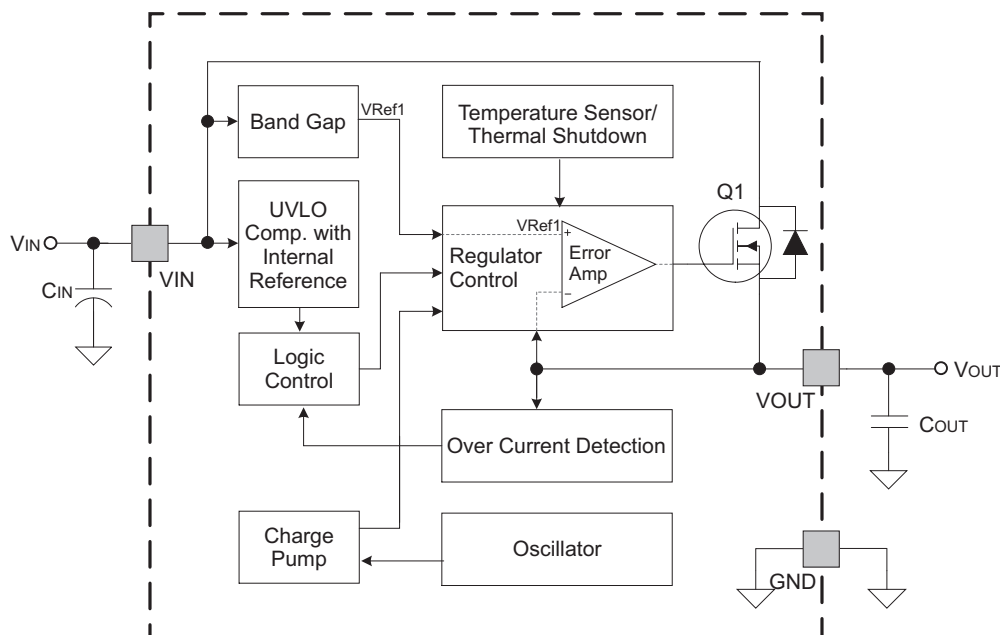
The TPS7A65-Q1 is a monolithic low-dropout linear voltage regulator designed for low-power consumption and quiescent current less than 25 μA in light-load applications. Because of an integrated fault protection, this device is well-suited in power supplies for various automotive applications.

This device is available in two fixed-output-voltage versions as follows:

- 5-V output version (TPS7A6550-Q1)
- 3.3-V output version (TPS7A6533-Q1)

See [Feature Description](#) for full descriptions of the features of the TPS7A65-Q1 voltage regulator.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power Up

During power up, the regulator incorporates a protection scheme to limit the current through the pass element and output capacitor. When the input voltage exceeds a certain threshold ($V_{\text{IN(POWERUP)}}$) level, the output voltage begins to ramp up; see [Figure 15](#).

Feature Description (continued)

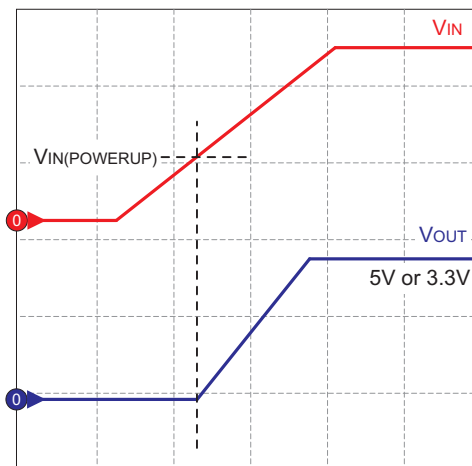


Figure 15. Power-Up Sequence

7.3.2 Charge-Pump Operation

This device has an internal charge pump that turns on or off depending on the input voltage and the output current. The charge pump switching circuitry does not cause conducted emissions to exceed required thresholds on the input voltage line. For a given output current, the charge pump stays on at lower input voltages and turns off at higher input voltages. The charge-pump switching thresholds are hysteretic. Figure 16 and Figure 17 show typical switching thresholds for the charge pump at light ($I_{OUT} < \text{approximately } 2 \text{ mA}$) and heavy ($I_{OUT} > \text{approximately } 2 \text{ mA}$) loads, respectively.

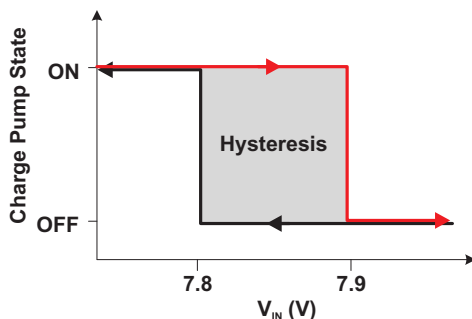


Figure 16. Charge-Pump Operation at Light Loads

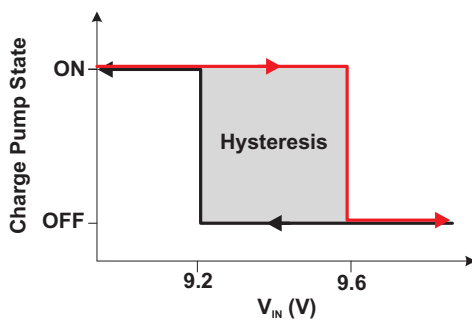


Figure 17. Charge-Pump Operation at Heavy Loads

Feature Description (continued)

7.3.3 Low-Power Mode

At light loads and high input voltages ($V_{IN} >$ approximately 8 V such that charge pump is off) the device operates in the low-power mode and the quiescent current consumption decreases to 25 μ A (typical) as shown in Table 1.

Table 1. Typical Quiescent Current Consumption

I_{OUT}	CHARGE PUMP ON	CHARGE PUMP OFF
$I_{OUT} <$ approximately 2 mA (light load)	250 μ A	25 μ A (low-power mode)
$I_{OUT} >$ approximately 2 mA (heavy load)	280 μ A	70 μ A

7.3.4 Undervoltage Shutdown

This device has an integrated undervoltage lockout (UVLO) circuit to shut down the output if the input voltage (V_{IN}) falls below an internally fixed UVLO threshold level ($V_{IN-UVLO}$) as shown in Figure 18. This ensures that the regulator does not latch into an unknown state during low input-voltage conditions. The regulator normally powers up when the input voltage exceeds the $V_{IN(POWERUP)}$ threshold.

7.3.5 Low-Voltage Tracking

At low input voltages, the regulator drops out of regulation, and the output voltage tracks input minus a voltage based on the load current (I_{OUT}) and switch resistance (R_{SW}) as shown in Figure 18. This allows for a smaller input capacitor and can possibly eliminate the need of using a boost converter during cold-crank conditions.

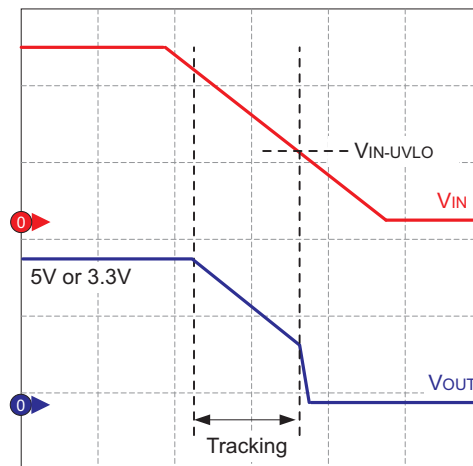


Figure 18. Undervoltage Shutdown and Low-Voltage Tracking

7.3.6 Integrated Fault Protection

This device features integrated fault protection to make them ideal for use in automotive applications. To keep the device in a safe area of operation during certain fault conditions, the device uses internal current limit protection and current limit foldback to limit the maximum output current. This protects the device from excessive power dissipation. For example, during a short-circuit condition on the output, limiting current through the pass element to I_{CL} protects the device from excessive power dissipation.

7.3.7 Thermal Shutdown

This device incorporates a thermal shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the TSD trip point. If the junction temperature exceeds the TSD trip point, the output turns off. When the junction temperature falls below the TSD trip point, the output turns on again. Figure 19 shows this.

Feature Description (continued)

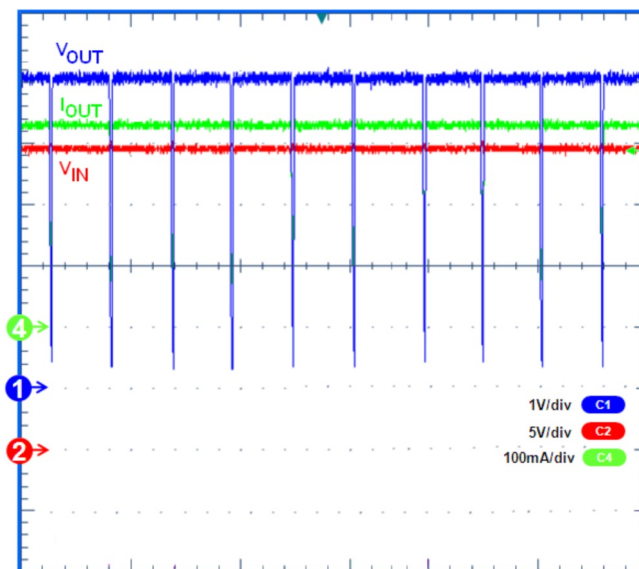


Figure 19. Thermal Cycling Waveform for TPS7A6550-Q1 ($V_{IN} = 24\text{ V}$, $I_{OUT} = 300\text{ mA}$, $V_{OUT} = 5\text{ V}$)

7.4 Device Functional Modes

7.4.1 Operation With V_{IN} Lower Than 4 V

The TPS7A65-Q1 device operates with input voltage above 4 V. The typical UVLO voltage is 3.16 V, the device can operate at input voltage lower than 4 V. But at input voltage below the actual UVLO, the device shuts down.

7.4.2 Operation With V_{IN} Larger Than 4 V

When V_{IN} is greater than 4 V, if the input voltage is higher than V_{OUT} plus the dropout voltage, the output voltage is equal to the set value. Otherwise, the output voltage is equal to V_{IN} minus the dropout voltage.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7A65-Q1 is a low-dropout linear voltage regulator designed for low power consumption and quiescent current less than 25 μA in light-load applications. This device features integrated overcurrent protection and a design to achieve stable operation even with low-ESR ceramic output capacitors. A low-voltage tracking feature allows for a smaller input capacitor and can possibly eliminate the need of using a boost converter during cold crank conditions. Because of these features, this device is well-suited in power supplies for various automotive applications.

8.2 Typical Application

A typical application circuit for TPS7A65-Q1 is [Figure 20](#). Depending on the end application, one may use different values of external components. An application may require a larger output capacitor during fast load steps to prevent the output from temporarily dropping down. TI recommends a low-ESR ceramic capacitor with dielectric of type X5R or X7R. The user can additionally connect a bypass capacitor at the output to decouple high-frequency noise as per the end application.

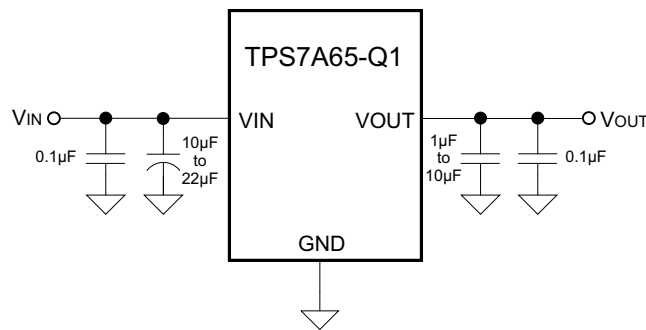


Figure 20. Typical Application Schematic

8.2.1 Design Requirements

Table 2 lists the parameters for this design example.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	7 V to 40 V
Output voltage	3.3 V, 5 V
Output current rating	300 mA maximum
Output capacitor range	1 μF to 10 μF

8.2.2 Detailed Design Procedure

When using the TPS7A6533-Q1, TPS7A6550-Q1, TI recommends adding a 10- μ F to 22- μ F capacitor to the input to keep the input voltage stable. TI also recommends adding a 1- μ F to 10- μ F low ESR ceramic capacitor to get a stable output.

8.2.3 Application Curve

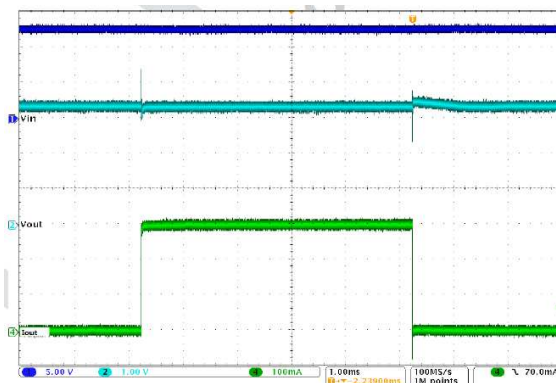


Figure 21. TPS7A6533-Q1 Load Transient Waveform

9 Power Supply Recommendations

The device is designed to operate from an input-voltage supply range from 7 V to 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7A65-Q1 device, TI recommends adding an electrolytic capacitor with a value of 10 μ F and a ceramic bypass capacitor at the input.

10 Layout

10.1 Layout Guidelines

For the LDO power supply, especially these high voltage and large current ones, layout is an important step. If layout is not carefully designed, the regulator could not deliver enough output current because of the thermal limitation. To improve the thermal performance of the device, and maximize the current output at high ambient temperature, TI recommends spreading the thermal pad as large as possible and putting enough thermal vias on the thermal pad.

10.1.1 Power Dissipation and Thermal Considerations

Calculate the power dissipated in the device using [Equation 1](#).

$$P_D = I_{OUT} \times (V_{IN} - V_{OUT}) + I_{QUIESCENT} \times V_{IN}$$

where

- P_D = continuous power dissipation
- I_{OUT} = output current
- V_{IN} = input voltage
- V_{OUT} = output voltage
- $I_{QUIESCENT}$ = quiescent current.

(1)

$I_{QUIESCENT} \ll I_{OUT}$; therefore, ignore the term $I_{QUIESCENT} \times V_{IN}$ in [Equation 1](#).

For a device under operation at a given ambient air temperature (T_A), calculate the junction temperature (T_J) using [Equation 2](#).

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where

- θ_{JA} = junction-to-ambient air thermal impedance.

(2)

Calculate the rise in junction temperature due to power dissipation using [Equation 3](#).

$$\Delta T = T_J - T_A = (\theta_{JA} \times P_D)$$

(3)

For a given maximum junction temperature (T_{J-Max}), calculate the maximum ambient air temperature (T_{A-Max}) at which the device can operate using [Equation 4](#).

$$T_{A-Max} = T_{J-Max} - (\theta_{JA} \times P_D)$$

(4)

Example

If $I_{OUT} = 100$ mA, $V_{OUT} = 5$ V, $V_{IN} = 14$ V, $I_{QUIESCENT} = 250$ μ A and $\theta_{JA} = 30^\circ\text{C/W}$, the continuous power dissipated in the device is 0.9 W. The rise in junction temperature due to power dissipation is 27°C . For a maximum junction temperature of 150°C , maximum ambient air temperature at which the device can operate is 123°C .

For adequate heat dissipation, TI recommends soldering the power pad (exposed heat sink) to the thermal land pad on the PCB. Doing this provides a heat conduction path from the die to the PCB and reduces overall package thermal resistance. [Figure 22](#) shows power derating curves for the TPS7A65-Q1 family of devices in the KVU (DPAK) package.

Layout Guidelines (continued)

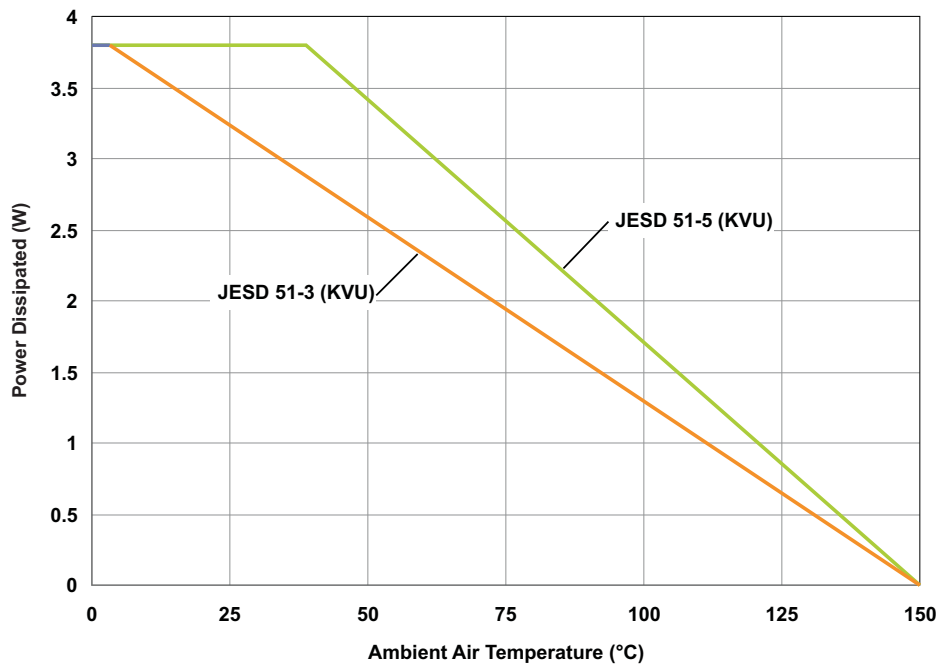


Figure 22. Power Derating Curves

For optimum thermal performance, TI recommends using a high-K PCB with thermal vias between the ground plane and solder pad or thermal land pad. [Figure 23](#) (a) and (b) show this. Further, a design can improve the heat-spreading capabilities of a PCB considerably by using a thicker ground plane and a thermal land pad with a larger surface area.

Layout Guidelines (continued)

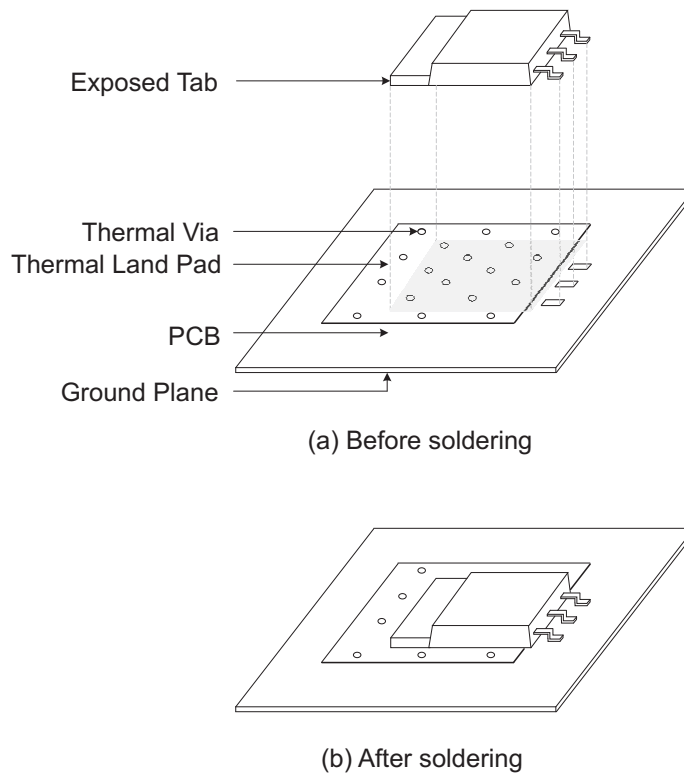


Figure 23. Using a Multilayer PCB and Thermal Vias for Adequate Heat Dissipation

Keeping other factors constant, the surface area of the thermal land pad contributes to heat dissipation only to a certain extent. Figure 24 shows the variation of θ_{JA} with surface area of the thermal land pad (soldered to the exposed pad) for the KVV package.

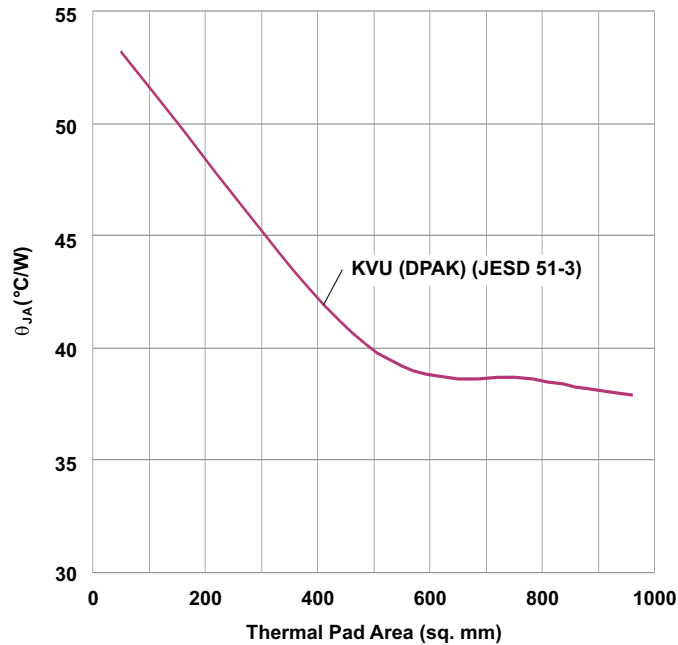


Figure 24. θ_{JA} vs Thermal Pad Area

10.2 Layout Example

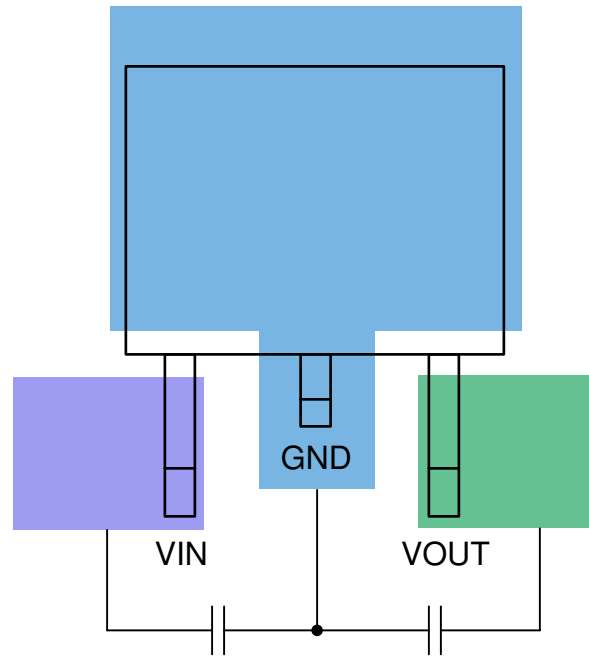


Figure 25. Layout Recommendation

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントの更新通知を受け取る方法

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11.2 コミュニティ・リソース

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7A6533QKVURQ1	Active	Production	TO-252 (KVU) 3	2500 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	7A6533Q1
TPS7A6533QKVURQ1.A	Active	Production	TO-252 (KVU) 3	2500 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	7A6533Q1
TPS7A6550QKVURQ1	Active	Production	TO-252 (KVU) 3	2500 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	7A6550Q1
TPS7A6550QKVURQ1.A	Active	Production	TO-252 (KVU) 3	2500 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	7A6550Q1

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

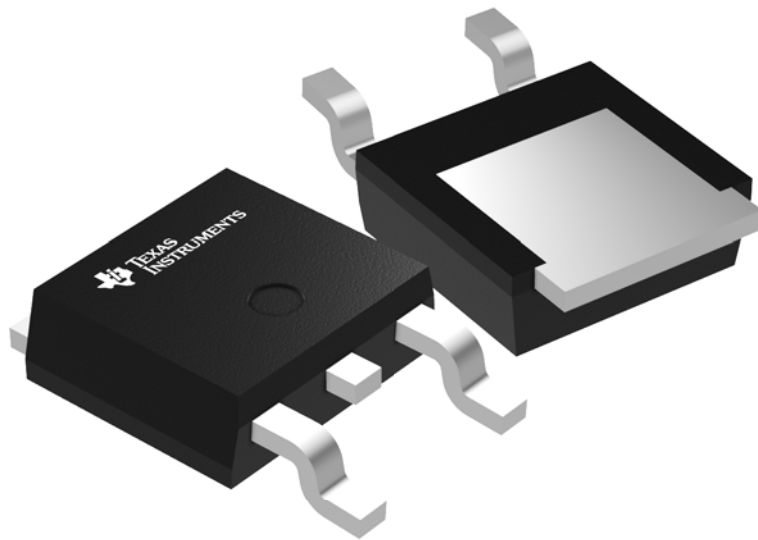

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A6533QKVURQ1	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TPS7A6550QKVURQ1	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A6533QKVURQ1	TO-252	KVU	3	2500	340.0	340.0	38.0
TPS7A6550QKVURQ1	TO-252	KVU	3	2500	340.0	340.0	38.0



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

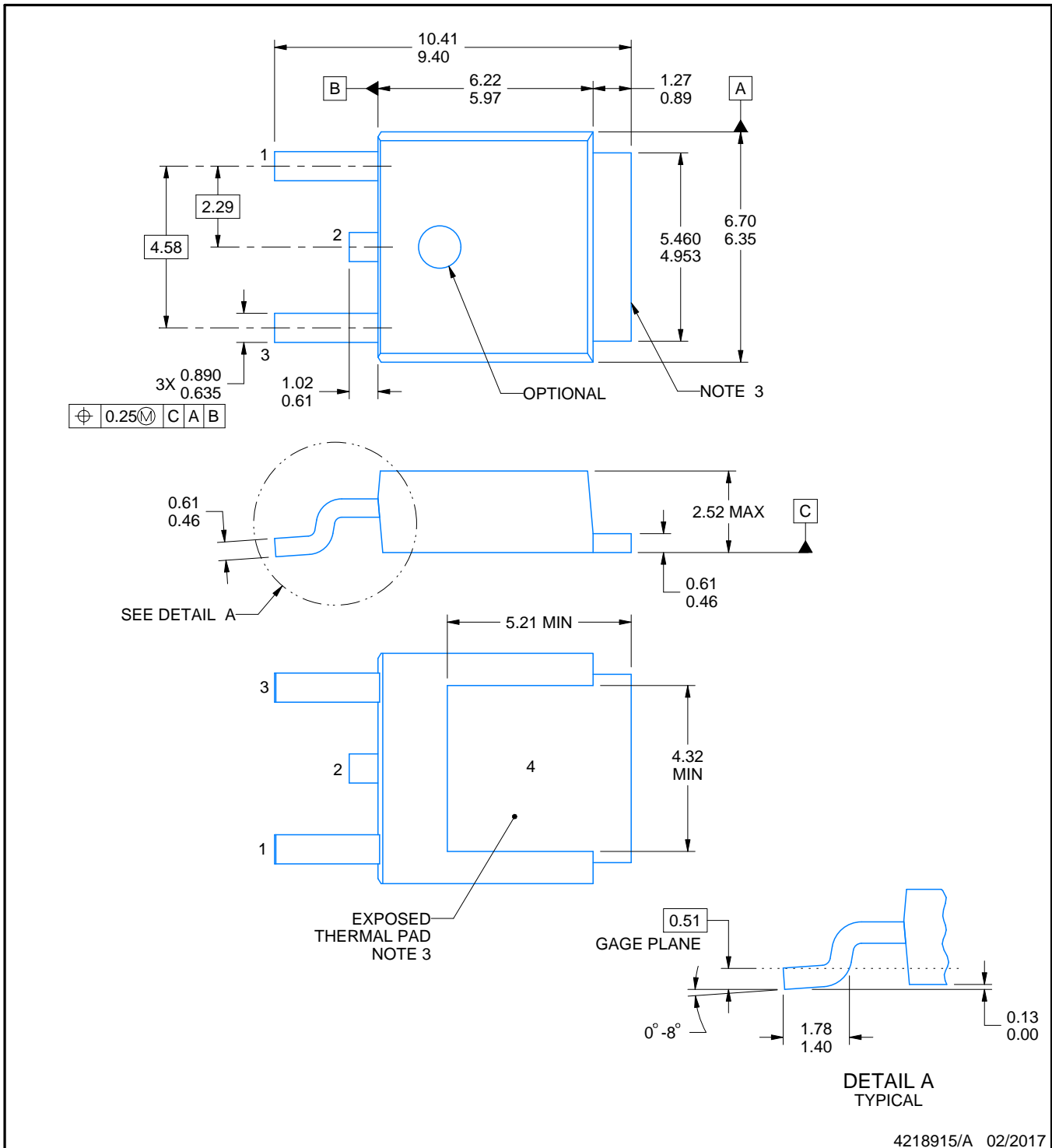


PACKAGE OUTLINE

KVVU0003A

TO-252 - 2.52 mm max height

TO-252



4218915/A 02/2017

NOTES:

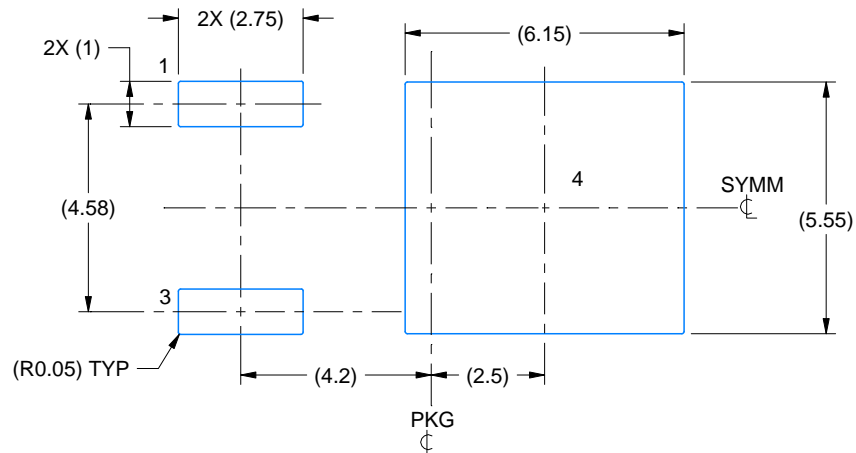
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Shape may vary per different assembly sites.
4. Reference JEDEC registration TO-252.

EXAMPLE BOARD LAYOUT

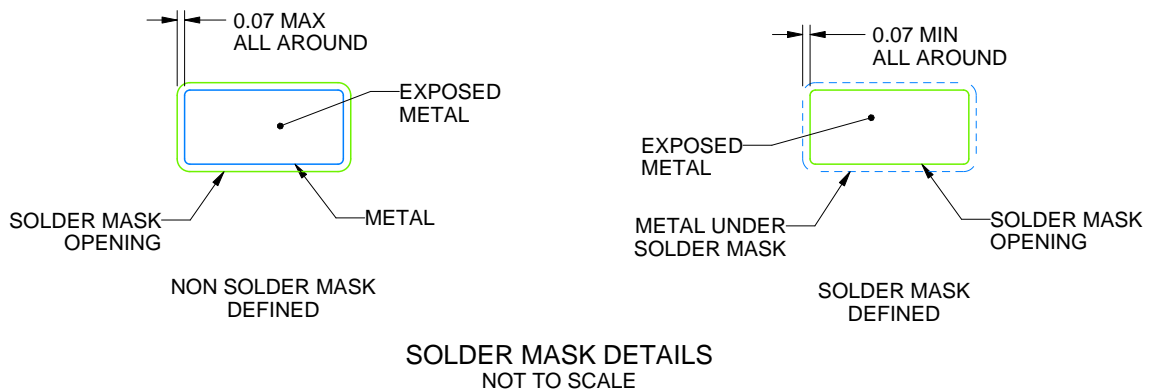
KVU0003A

TO-252 - 2.52 mm max height

TO-252



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS
NOT TO SCALE

4218915/A 02/2017

NOTES: (continued)

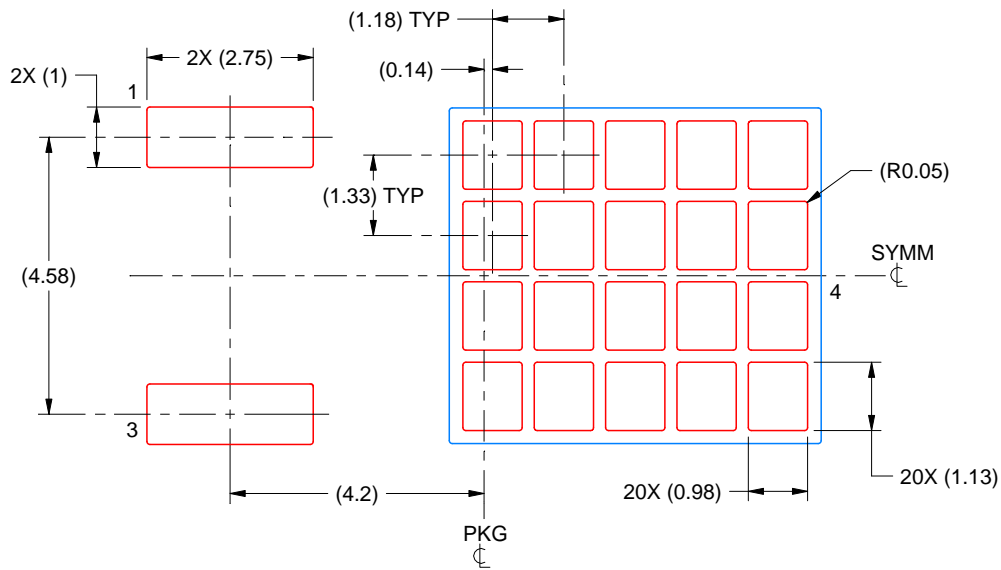
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
6. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

KVU0003A

TO-252 - 2.52 mm max height

TO-252



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
65% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

4218915/A 02/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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