TEXAS INSTRUMENTS

TPS7A74
JAJSM31 – MAY 2022

TPS7A74 プログラマブル・ソフトスタート機能付き、1.5A 低ドロップアウト・リニア・レギュレータ

1 特長

- V_{OUT} 範囲：0.65V～3.6V
- 非常に低い V_{IN} にも対応：0.8V～5.5V
- V_{BIAS} 範囲：2.7V～5.5V
- 低いドロップアウト：60mV (標準値、1.5A / V_{BIAS} = 5V 時)
- ノイズ：7µV$_{RMS}$
- PSRR：
  - 1kHz 時に 65dB
  - 10kHz 時に 60dB
  - 100kHz 時に 51dB
  - 1MHz 時に 42dB
- ライン、負荷、温度の各範囲にわたって 2% の精度
- プログラム可能なソフトスタートにより、直線的に電圧が立ち上がるようにスタートアップさせることが可能
- V_{BIAS} を使うことで、過渡応答性に優れた低 V_{IN} 動作を実現
- 任意のタイプのコンデンサ (≥ 10µF) で安定に動作
- 小型の 3mm × 3mm × 0.8mm WSON-8 で供給

2 アプリケーション

- 高性能コンピューティング
- マイクロサーバー
- デスクトップ PC マザーボード
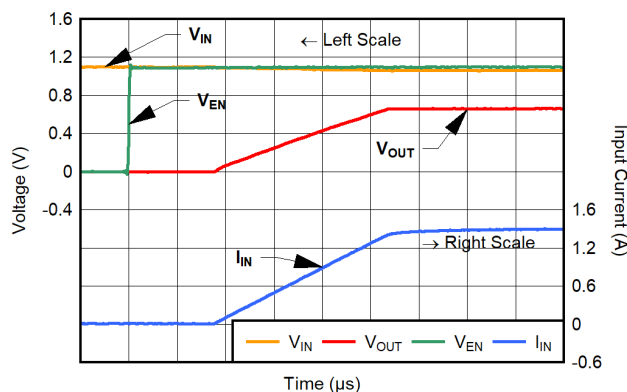- データ・コンセントレータ
- 高耐久性 PC とラップトップ
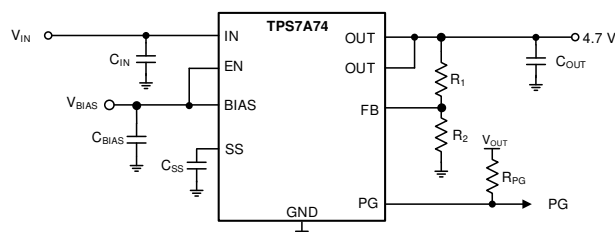
3 概要

TPS7A74 低ドロップアウト (LDO) リニア・レギュレータは、広範なアプリケーション向けの使いやすく堅牢な電力管理ソリューションです。ソフトスタートをユーザーがプログラム可能なため、スタートアップ時の容量性負荷電流を低減して、入力電源のストレスを最小限に抑えることができます。ソフトスタートは単調性で、多くの種類のプロセッサおよび特定用途向け IC (ASIC) の電源に適しています。イネーブル入力とパワー・グッド出力により、外部レギュレータとの間でシーケンシングを簡単に実行できます。このような高い柔軟性により、FPGA や DSP、その他の特殊なスタートアップ条件を持つアプリケーションのシーケンス制御条件を満たすソリューションを構成できます。

高精度の基準電圧およびエラー・アンプは、負荷、ライン、温度、プロセスの範囲全体にわたって 2% の精度を維持します。本デバイスは 10µF 以上の任意のタイプのコンデンサで安定に動作し、T_J = -40℃～+125℃で仕様規定されています。TPS7A74 は小型の 3mm × 3mm WSON-8 パッケージで供給されるため、非常に小さいトータル・ソリューション・サイズを実現できます。

製品情報 (1)

部品番号	パッケージ	本体サイズ (公称)
TPS7A74	WSON (8)	3.00mm × 3.00mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。

代表的なアプリケーション回路 (可変)

負荷を接続した状態でのスタートアップ

ADVANCE INFORMATION

English Data Sheet: SBVS416

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
May 2022	*	Initial Release

ADVANCE INFORMATION

5 Pin Configuration and Functions
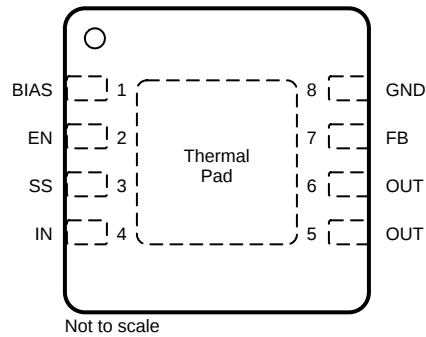
図 5-1. DSD Package, 8-Pin WSON With Thermal Pad (Top View)

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	BIAS	I	Bias input voltage for error amplifier, reference, and internal control circuits. A 1-µF or larger input capacitor is recommended for optimal performance. If IN is connected to BIAS, a 4.7-µF or larger capacitor must be used.
2	EN	I	Enable pin.
3	SS	I	Soft-start pin. This pin must be connected to a capacitor to GND.
4	IN	I	Input to the device. A 1-µF or larger input capacitor is recommended for optimal performance.
5, 6	OUT	O	Regulated output voltage. A small capacitor (total typical capacitance of ≥ 10 µF, ceramic) is required from this pin to ground to assure stability.
7	FB	I	Feedback pin. The feedback connection to the center tap of an external resistor divider network that sets the output voltage. This pin must not be left floating.
8	GND	—	Ground.

ADVANCE INFORMATION

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	6.5	V
V_{BIAS}	Bias voltage	–0.3	6.5	V
V_{EN}	Enable voltage	–0.3	6.5	V
V_{SS}	Soft-start voltage	–0.3	6.5	V
V_{FB}	Feedback voltage	–0.3	2	V
V_{OUT}	Output voltage	–0.3	V_{IN} + 0.3	V
I_{OUT}	Maximum output current	Internally limited		
	Output short-circuit duration	Indefinite		
P_{DISS}	Continuous total power dissipation	See Thermal Information		
Junction, T_J	Junction Temperature	–40	150	°C
Storage, T_{stg}	Storage Temperature	–55	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Product Folder Links: *TPS7A74*

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	0.65		6	V
V_{BIAS} [1]	BIAS supply voltage	1.7		6	V
V_{EN}	Enable voltage			6	V
V_{OUT}	Output voltage	0.65		3.6	V
I_{OUT}	Output current	0		1.5	A
C_{OUT}	Output capacitor	10			µF
C_{IN}	Input capacitor [2]	1			µF
C_{BIAS}	Bias capacitor	0.1	1		µF
T_J	Operating junction temperature	−40		125	°C

(1)   BIAS supply is required when V_{IN} is below V_{OUT} + 1.62 V.
(2)   If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for the supply is 4.7 µF.

6.4 Thermal Information

THERMAL METRIC[1]		TPS7A74		UNIT
		DSD (WSON) [2]	DSD (WSON) [3]	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.3	34.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55.3		°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.3		°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.9	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	21.3	18.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.8		°C/W

(1)   For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.
(2)   JEDEC standard. (2s2p, no vias to internal planes and bottom layer).
(3)   TPS7A74 thermal characteristics on EVM.

ADVANCE INFORMATION

6.5 Electrical Characteristics

At V_{EN} = 1.1 V, V_{IN} = V_{OUT} + 0.3 V, C_{BIAS} = 0.1 µF, C_{IN} = C_{OUT} = 10 µF, C_{NR} = 10 nF, I_{OUT} = 10 mA, V_{BIAS} = 5.0 V [(4)], and T_J = −40°C to 125°C, (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	Internal reference (adj.)		0.641	0.65	0.659	V
	Output accuracy [(1) (5) (6)]	2.97 V ≤ V_{BIAS} ≤ 6 V, 0 mA ≤ I_{OUT} ≤ 1.5 A	−1.5	±0.5	1.5	%
	Line regulation (V_{BIAS})	Max(2.7 V, V_{OUT} + 1.6 V) ≤ V_{BIAS} ≤ 6 V		0.2	0.32	%/V
	Line regulation (V_{IN})	$V_{OUT(nom)}$ + 0.15 V ≤ V_{IN} ≤ 6 V		0.01	0.05	%/V
	Load regulation	0 mA ≤ I_{OUT} ≤ 1.5 A		0.33		%/A
$V_{DO(IN)}$	V_{IN} dropout voltage[(2)]	I_{OUT} = 1.5 A, V_{BIAS} − $V_{OUT(nom)}$ ≥ 2.8 V[(3)]		150	180	mV
$V_{DO(BIAS)}$	V_{BIAS} dropout voltage[(2)]	I_{OUT} = 1.5 A, V_{IN} = V_{BIAS}		1.1	1.3	V
I_{CL}	Output current limit	V_{OUT} = 80% × $V_{OUT(nom)}$	2	2.7	3.3	A
I_{BIAS}	BIAS pin current	I_{OUT} = 10 mA		0.25	0.33	mA
I_{SHDN}	Shutdown supply current (I_{GND})	V_{EN} ≤ 0.4 V, V_{IN} = 6 V, V_{BIAS} = 6 V		1	55	µA
I_{FB}	Feedback pin current		−1	0.15	1	µA
$V_{BIAS(UVLO)}$	Bias rail UVLO rising threshold		1.04	1.4	1.65	V
$V_{BIAS(UVLO),HYST}$	Bias rail UVLO hysteresis		0.02	0.06	0.07	V
$V_{IN(UVLO), rising}$	In rail UVLO rising threshold		0.39	0.455	0.5	V
$V_{IN(UVLO), falling}$	In rail UVLO falling threshold		0.21	0.26	0.3	V
t_{STR}	Minimum start-up time	R_{LOAD} for I_{OUT} = 1.0 A, C_{SS} = open	55		310	µs
I_{SS}	Soft-start charging current	V_{SS} = 0 V	8	17	31	µA
V_{SS}	Soft-start pin disable voltage	V_{EN} = 0 V		0	50	mV
$V_{EN(hi)}$	Enable input high level		1.1		5.5	V
$V_{EN(lo)}$	Enable input low level		0		0.4	V
$V_{EN(hys)}$	Enable pin hysteresis			55		mV
$V_{EN(dg)}$	Enable pin deglitch time			20		µs
I_{EN}	Enable pin current	V_{EN} = 5 V		0.1	0.2	µA
$R_{PULLDOWN(OUT)}$	V_{BIAS} = 5 V, V_{EN} = 0 V			0.6	1	kΩ
$R_{PULLDOWN(FB)}$	V_{BIAS} = 5 V, V_{EN} = 0 V			120		Ω
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		165		°C
		Reset, temperature decreasing		140		

(1) Adjustable devices tested at 0.65 V; resistor tolerance is not taken into account.
(2) Dropout is defined as the voltage from V_{IN} to V_{OUT} when V_{OUT} is 3% below nominal.
(3) 3.25 V is a test condition of this device and can be adjusted.
(4) V_{BIAS} = $V_{DO\_MAX(BIAS)}$ + V_{OUT} for V_{OUT} ≥ 3.4 V
(5) The device is not tested under conditions where V_{IN} > V_{OUT} + 1.65 V and I_{OUT} = 1.5 A, because the power dissipation is higher than the maximum rating of the package. Also, this accuracy specification does not apply on any application condition that exceeds the power dissipation limit of the package under test.
(6) The device is not tested under conditions where V_{IN} > V_{OUT} + 1.65 V and I_{OUT} = 1.5 A, because the power dissipation is higher than the maximum rating of the package. Also, this accuracy specification does not apply on any application condition that exceeds the power dissipation limit of the package under test.

ADVANCE INFORMATION

6.6 Typical Characteristics

at $T_J = 25°C$, $V_{IN} = V_{OUT(nom)} + 0.3$ V, $V_{BIAS} = 5$ V, $V_{EN} = V_{IN}$, $C_{IN} = 10$ µF, $C_{BIAS} = 1$ µF, and $C_{OUT} = 10$ µF (unless otherwise noted)
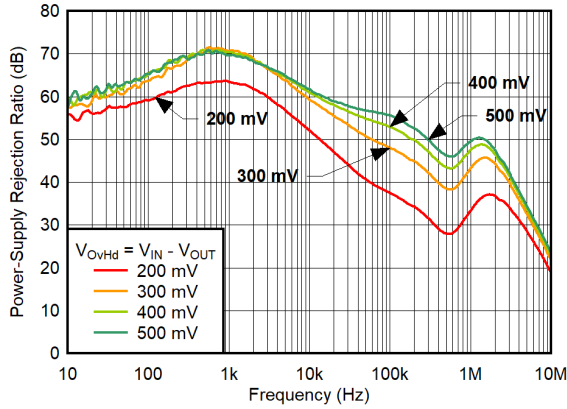
$C_{IN} = C_{OUT} = 10$ µF, $C_{BIAS} = 1$ µF

図 6-1. PSRR vs Frequency and Overhead (OvHd) Voltage for $I_{OUT} = 400$ mA, $V_{OUT} = 1.8$ V
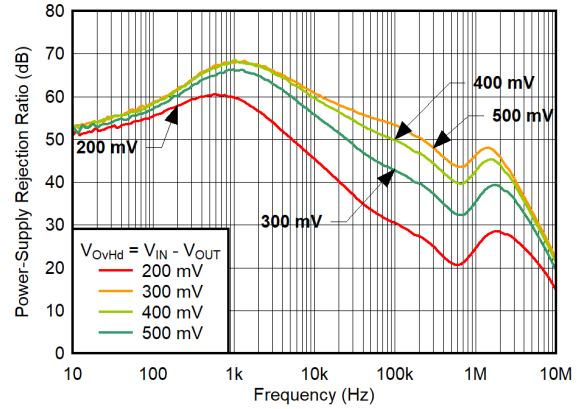
$C_{IN} = C_{OUT} = 10$ µF, $C_{BIAS} = 1$ µF

図 6-2. PSRR vs Frequency and Overhead (OvHd) Voltage for $I_{OUT} = 750$ mA, $V_{OUT} = 1.8$ V
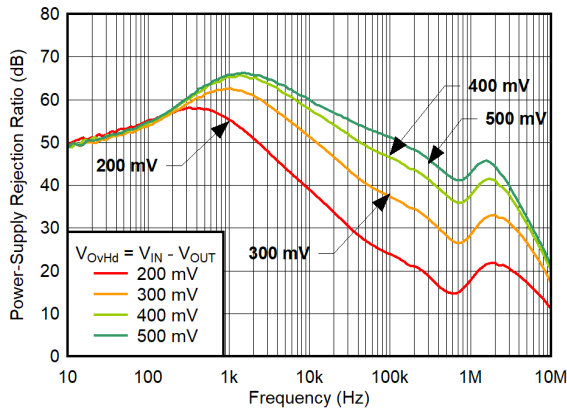
$C_{IN} = C_{OUT} = 10$ µF, $C_{BIAS} = 1$ µF

図 6-3. PSRR vs Frequency and Overhead (OvHd) Voltage for $I_{OUT} = 1.1$ A, $V_{OUT} = 1.8$ V
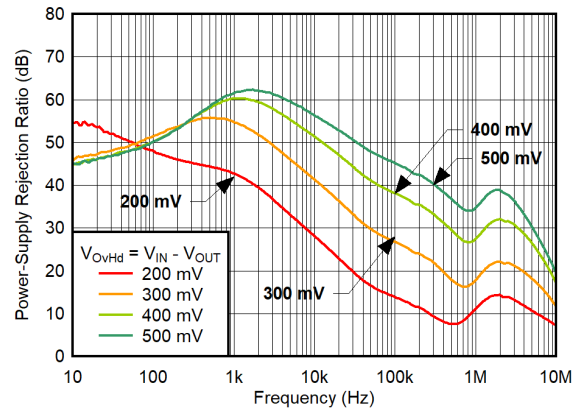
$C_{IN} = C_{OUT} = 10$ µF, $C_{BIAS} = 1$ µF

図 6-4. PSRR vs Frequency and Overhead (OvHd) Voltage for $I_{OUT} = 1.5$ A, $V_{OUT} = 1.8$ V
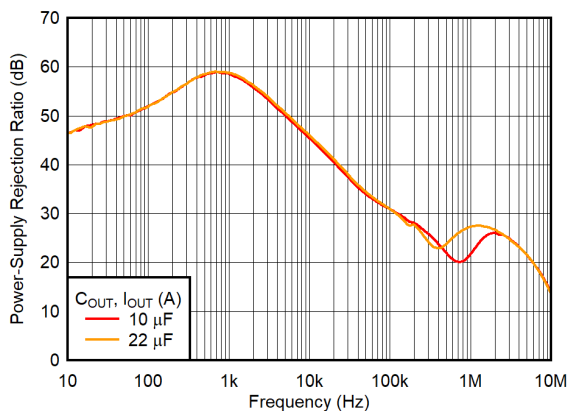
$C_{IN} = C_{OUT} = 10$ µF, $C_{BIAS} = 1$ µF, $I_{OUT} = 1.5$ A

図 6-5. PSRR vs Frequency and C_{OUT} for $V_{OUT} = 1.8$ V
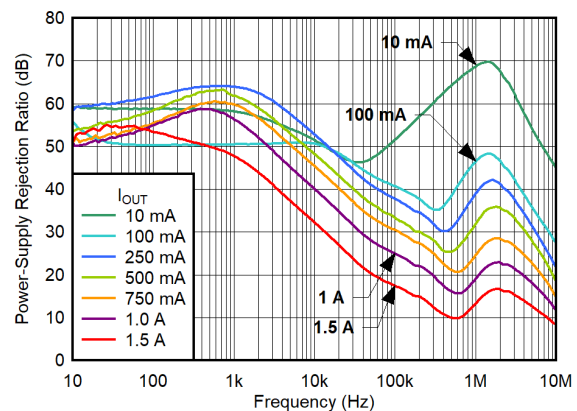
$C_{IN} = C_{OUT} = 10$ µF, $C_{BIAS} = 1$ µF

図 6-6. PSRR vs Frequency and I_{OUT} for $V_{OvHd} = 200$ mV

ADVANCE INFORMATION

6.6 Typical Characteristics (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, V_{EN} = V_{IN}, C_{IN} = 10 μF, C_{BIAS} = 1 μF, and C_{OUT} = 10 μF (unless otherwise noted)

ADVANCE INFORMATION
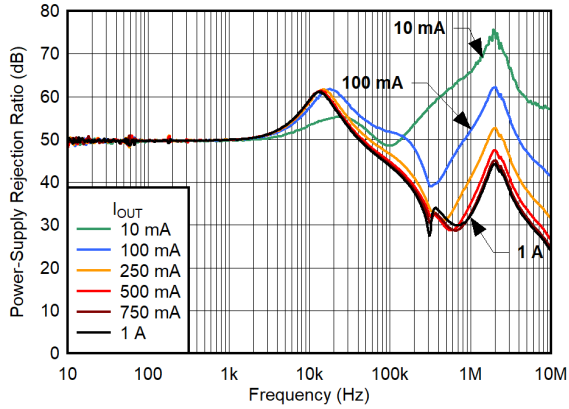
V_{IN} = V_{OUT} + 0.3 V, C_{IN} = C_{OUT} = 10 μF, C_{BIAS} = 1 μF

図 6-7. Bias Rail PSRR vs Frequency and I_{OUT}

C_{IN} = C_{OUT} = 10 μF, C_{BIAS} = 1 μF

図 6-8. Noise vs Frequency and I_{OUT} for V_{OUT} = 0.65 V
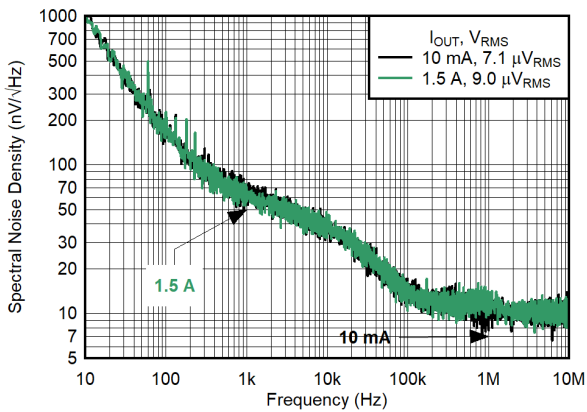
C_{IN} = C_{OUT} = 10 μF, C_{BIAS} = 1 μF

図 6-9. Noise vs Frequency and I_{OUT} for V_{OUT} = 3.3 V
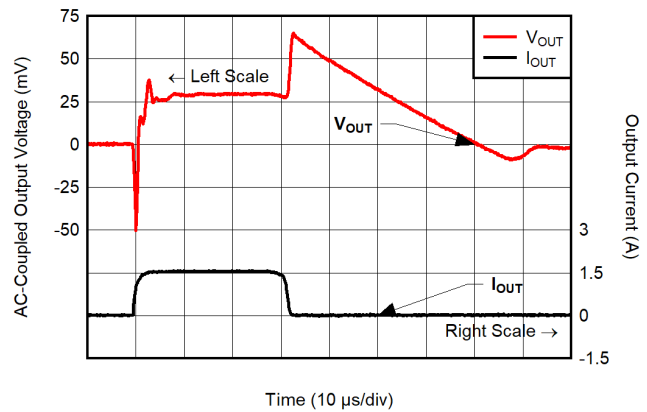
C_{IN} = C_{OUT} = 10 μF, C_{BIAS} = 1 μF, I_{OUT} = 10 mA to 1.5 A to 10 mA

図 6-10. Load Transient for V_{OUT} = 0.65 V

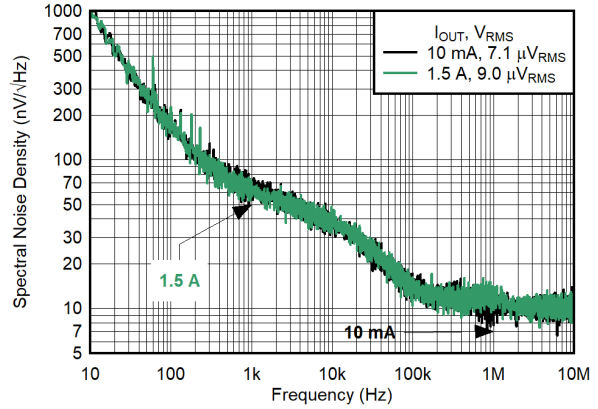## 6.6 Typical Characteristics (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, V_{EN} = V_{IN}, C_{IN} = 10 µF, C_{BIAS} = 1 µF, and C_{OUT} = 10 µF (unless otherwise noted)

C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, I_{OUT} = 10 mA to 1.5 A to 10 mA

図 6-11. Load Transient for V_{OUT} = 3.3 V

C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, I_{OUT} = 1.5 A, V_{IN} = 0.95 V to 6 V to 0.95 V

図 6-12. Line Transient for V_{OUT} = 0.65 V

C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, I_{OUT} = 1.5 A, V_{IN} = 3.9 V to 5.8 V to 3.9 V

図 6-13. Line Transient for V_{OUT} = 3.3 V

C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, I_{OUT} = 1.5 A, V_{BIAS} = 5 V

図 6-14. Input Ramp-Up and Ramp-Down

C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, I_{OUT} = 1.5 A, V_{IN} = 1.1 V, V_{BIAS} = 5 V

図 6-15. Input Ramp With Fast Soft-Start

ADVANCE INFORMATION
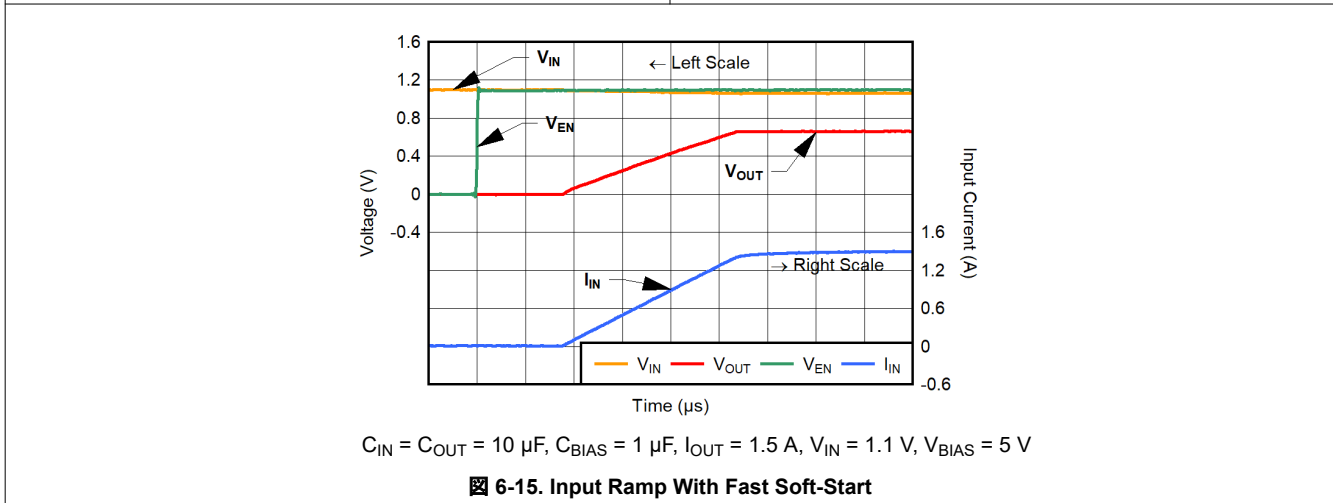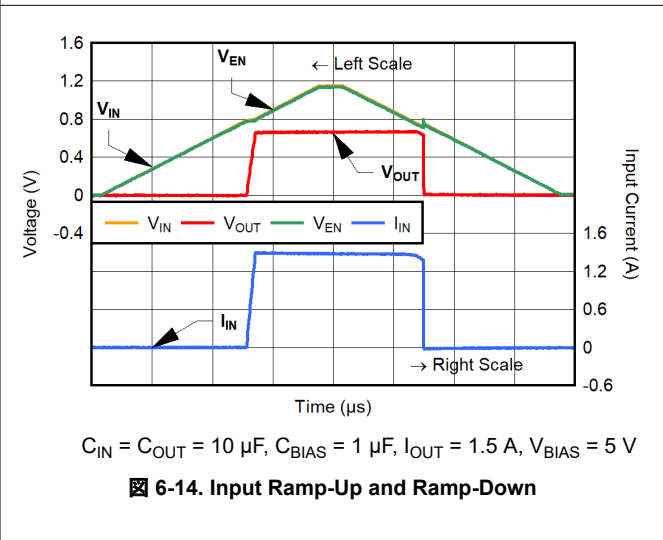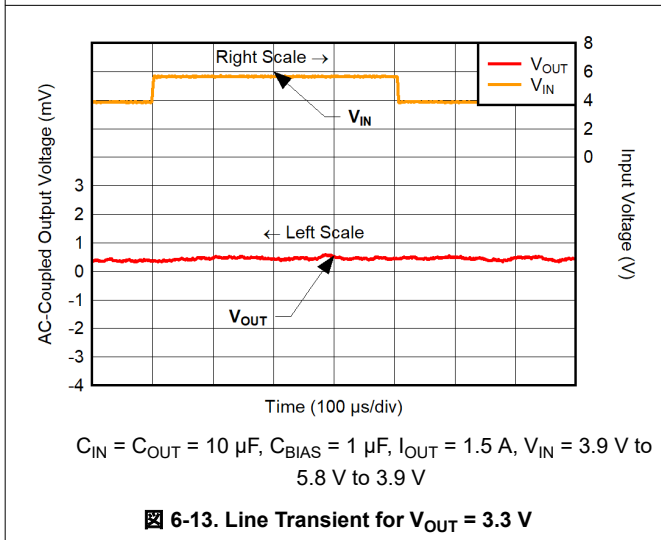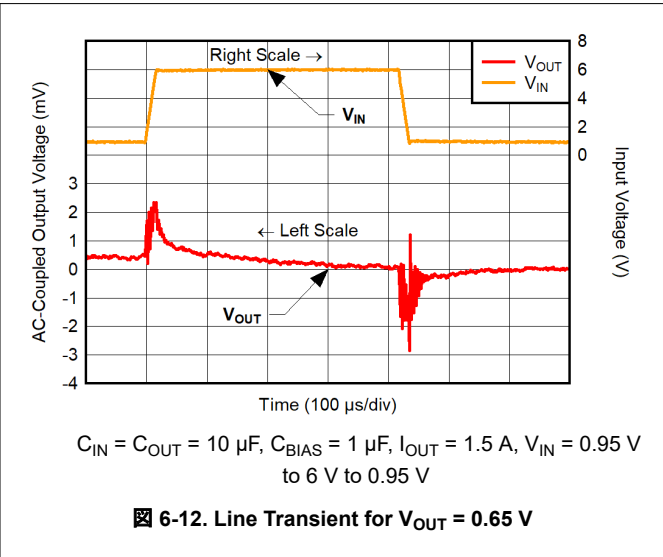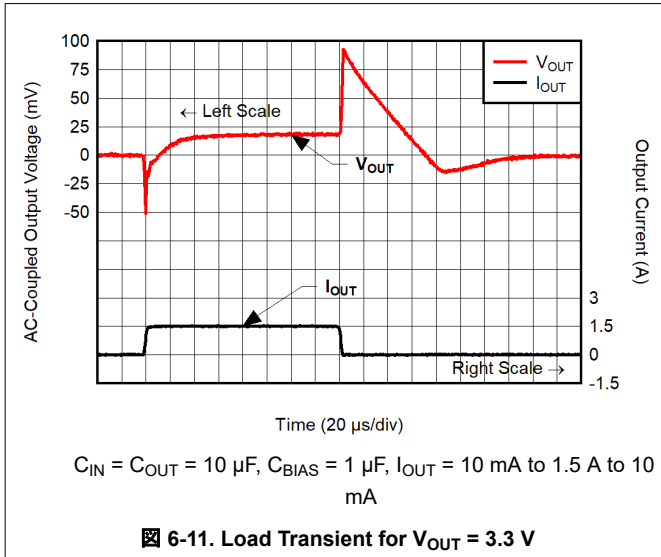
7 Detailed Description

7.1 Overview

The TPS7A74 is a low-input, low-output, low-quiescent-current linear regulator that is optimized for excellent transient performance. This regulator uses a low current bias input to power all internal control circuitry, allowing the n-type field effect transistor (NMOS) pass transistor to regulate very low input and output voltages.

Using an NMOS-pass transistor offers several critical advantages for many applications. Unlike a p-channel metal-oxide-semiconductor field effect transistor (PMOS) topology device, the output capacitor has little effect on loop stability. This architecture allows the TPS7A74 to be stable with any capacitor type that is 10 µF or greater. Transient response is also superior to PMOS topologies, particularly for low V_{IN} applications.

The TPS7A74 features a programmable voltage-controlled, soft-start circuit that provides a smooth, monotonic start-up and limits start-up inrush currents that can be caused by large capacitive loads. An enable (EN) pin with hysteresis and deglitch allows slow-ramping signals to be used for sequencing the device. The low V_{IN} and V_{OUT} capability allows for inexpensive, easy-to-design, and efficient linear regulation between the multiple supply voltages often required by processor-intensive systems.

7.2 Functional Block Diagram
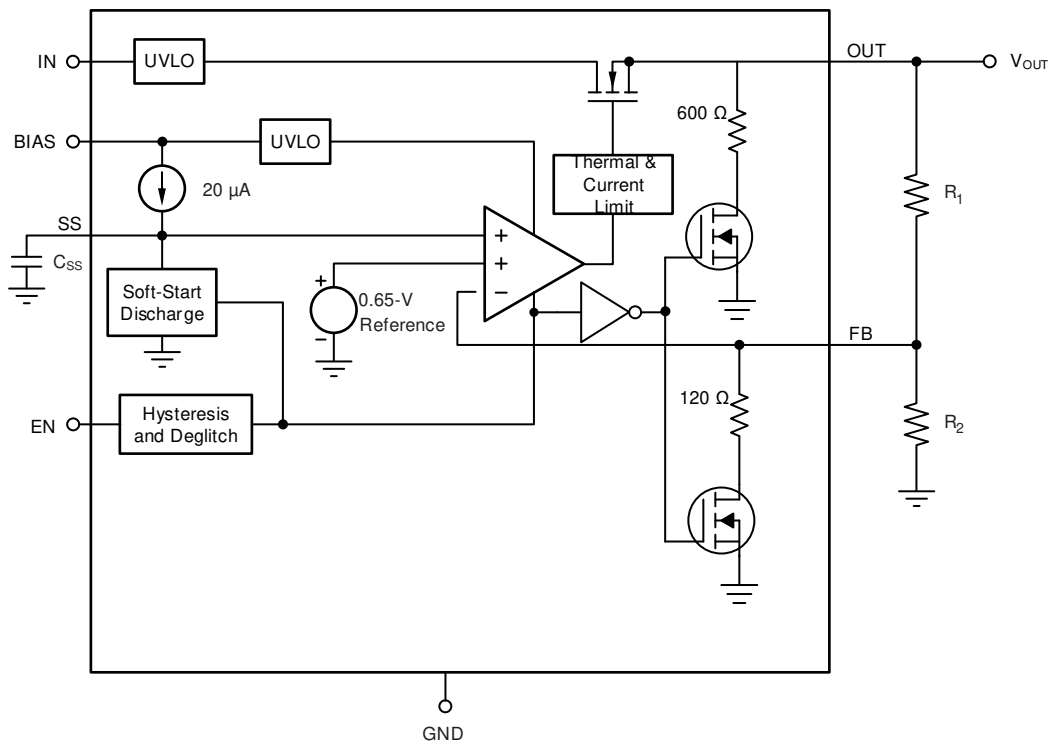
7.3 Feature Description

7.3.1 Enable and Shutdown

The enable (EN) pin is active high and compatible with standard digital-signaling levels. Setting V_{EN} below 0.4 V turns the regulator off, and setting V_{EN} above 1.1 V turns the regulator on. Unlike many regulators, the enable circuitry has hysteresis and deglitching for use with relatively slowly ramping analog signals. This configuration allows the device to be enabled by connecting the output of another supply to the EN pin. The enable circuitry typically has 50 mV of hysteresis and a deglitch circuit to help avoid on-off cycling as a result of small glitches in the V_{EN} signal.

The enable threshold is typically 0.8 V and varies with temperature and process variations. Temperature variation is approximately –1 mV/°C; process variation accounts for most of the rest of the variation to the 0.4-V and 1.1-V limits. If precise turn-on timing is required, a fast rise-time signal must be used.

If not used, EN can be connected to BIAS. Place the connection as close as possible to the bias capacitor.

7.3.2 Active Discharge

The TPS7A74 has two internal active pulldown circuits: one on the FB pin and one on the OUT pin.

Each active discharge function uses an internal metal-oxide-semiconductor field-effect transistor (MOSFET) that connects a resistor ($R_{PULLDOWN}$) to ground when the low-dropout resistor (LDO) is disabled in order to actively discharge the output voltage. The active discharge circuit is activated when the device is disabled by driving EN to logic low, when the voltage at IN or BIAS is below the UVLO threshold, or when the regulator is in thermal shutdown.

The discharge time after disabling the device depends on the output capacitance (C_{OUT}) and the load resistance (R_L) in parallel with the pulldown resistor.

The first active pulldown circuit connects the output to GND through a 600-Ω resistor when the device is disabled.

The second circuit one connects FB to GND through a 120-Ω resistor when the device is disabled. This resistor discharges the FB pin. 式 1 calculates the output capacitor discharge time constant when OUT is shorted to FB, or when the output voltage is set to 0.65 V.

$$\tau_{OUT} = (600 \parallel 120 \times R_L / (600 \parallel 120 + R_L) \times C_{OUT} \tag{1}$$

If the LDO is set to an output voltage greater than 0.65 V, a resistor divider network is in place and minimizes the FB pin pulldown. 式 2 and 式 3 calculate the time constants set by these discharge resistors.

$$R_{DISCHARGE} = (120 \parallel R_2) + R_1 \tag{2}$$

$$\tau_{OUT} = R_{DISCHARGE} \times R_L / (R_{DISCHARGE} + R_L) \times C_{OUT} \tag{3}$$

Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can flow from the output to the input and can cause damage to the device. Limit reverse current to no more than 5% of the device-rated current.

ADVANCE INFORMATION

7.3.3 Global Undervoltage Lockout (UVLO) Circuit

Two undervoltage lockout (UVLO) circuits are present to prevent the TPS7A74 from turning on with an insufficient rail. One circuit is present on the BIAS pin and the other circuit is on the IN pin. The two UVLO signals are connected internally through an AND gate, as shown in 図 7-1, that turns off the device when the voltage on either input is below their respective UVLO thresholds.

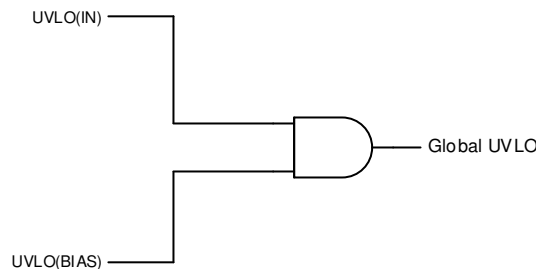UVLO(IN) ————————

Global UVLO

UVLO(BIAS) ————————

図 7-1. Global UVLO Circuit

7.3.4 Internal Current Limit

The device has an internal current-limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brick-wall foldback scheme. The current limit transitions from a brick-wall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brick-wall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current when the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the *short-circuit current limit* (I_{SC}). I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK}$ is approximately 60% × $V_{OUT(nom)}$.

The output voltage is not regulated when the device is in current limit. When a current-limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in a brick-wall current limit, the pass transistor dissipates power [($V_{IN} − V_{OUT}$) × I_{CL}]. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power [($V_{IN} − V_{OUT}$) × I_{SC}]. If thermal shutdown is triggered, the device turns off. When the device sufficiently cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application report. 図 7-2 illustrates a diagram of the foldback current limit.

ADVANCE INFORMATION
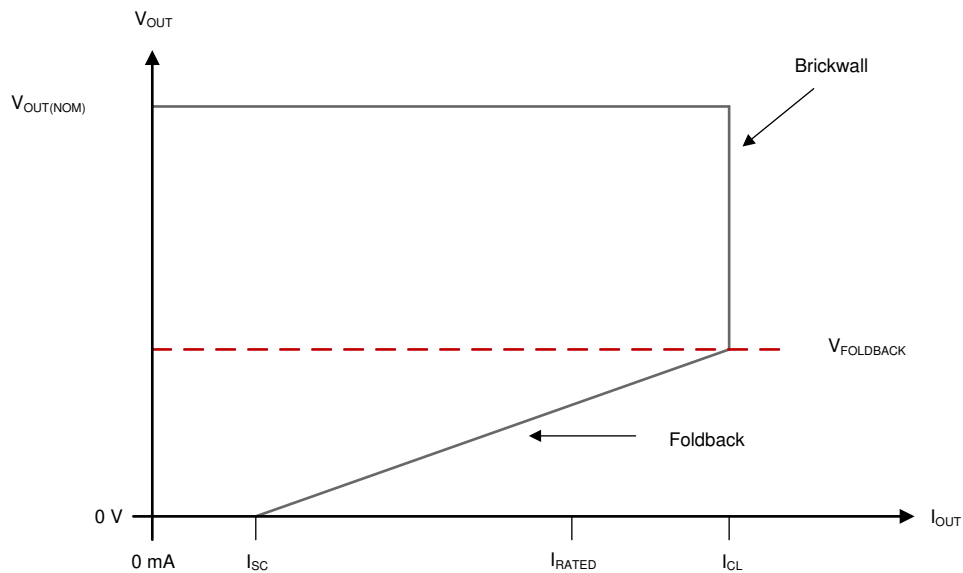
図 7-2. Foldback Current Limit

7.3.5 Thermal Shutdown Protection (T$_{SD}$)

The internal thermal shutdown protection circuit disables the output when the thermal junction temperature (T$_J$) of the pass transistor rises to the thermal shutdown temperature threshold, T$_{SD(shutdown)}$ (typical). The thermal shutdown circuit hysteresis ensures that the LDO resets (turns on) when the temperature falls to T$_{SD(reset)}$ (typical).

The thermal time constant of the semiconductor die is fairly short; thus, the device may cycle on and off when thermal shutdown is reached until the power dissipation is reduced. Power dissipation during start up can be high from large V$_{IN}$ − V$_{OUT}$ voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed its operational specifications. Although the internal protection circuitry is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the regulator into thermal shutdown, or above the maximum recommended junction temperature, reduces long-term reliability.

ADVANCE INFORMATION

7.4 Device Functional Modes

表 7-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

表 7-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER				
	V_{IN}	V_{BIAS}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} \geq V_{OUT(nom)} + V_{DO}$ and $V_{IN} \geq V_{IN(min)}$	$V_{BIAS} \geq V_{OUT} + V_{DO(BIAS)}$	$V_{EN} \geq V_{HI(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$ for shutdown
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO(IN)}$	$V_{BIAS} < V_{OUT} + V_{DO(BIAS)}$	$V_{EN} > V_{HI(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$ for shutdown
Disabled mode (any true condition disables the device)	$V_{IN} < V_{UVLO(IN)}$	$V_{BIAS} < V_{BIAS(UVLO)}$	$V_{EN} < V_{LO(EN)}$	—	$T_J \geq T_{SD}$ for shutdown

7.4.1 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The bias voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD(shutdown)}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. Similarly, if the bias voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode as well. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and functions as a switch. Line or load transients in dropout can result in large output voltage deviations.

When operating in dropout, the ground current may increase.

When the device is in a steady dropout state, defined as when the device is in dropout, ($V_{IN} < V_{OUT} + V_{DO}$ or $V_{BIAS} < V_{OUT} + V_{DO}$ directly after being in normal regulation state, but not during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short time when the device pulls the pass transistor back into the linear region.

7.4.3 Disabled

The output of the device can be shutdown by forcing the voltage of the enable pin to less than $V_{IL(EN)}$ (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

The device is disabled under the following conditions:

- The input or bias voltages are below the respective minimum specifications
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold
- The device junction temperature is greater than the thermal shutdown temperature

7.5 Programming

7.5.1 Programmable Soft-Start

The TPS7A74 features a programmable, monotonic, voltage-controlled soft-start that is set with an external capacitor (C_{SS}). This feature is important for many applications because the soft-start eliminates power-up initialization problems when powering FPGAs, DSPs, or other processors. The controlled voltage ramp of the output also reduces peak inrush current during start-up, minimizing start-up transient events to the input power bus.

To achieve a linear and monotonic soft-start, the error amplifier tracks the voltage ramp of the external soft-start capacitor until the voltage exceeds the internal reference. The soft-start ramp time depends on the soft-start charging current (I_{SS}), soft-start capacitance (C_{SS}), and the internal reference voltage (V_{REF}). 式 4 calculates the soft-start ramp time.

$$t_{SS} = \frac{(V_{REF} \times C_{SS})}{I_{SS}}$$

(4)

If large output capacitors are used, the device current limit (I_{CL}) and the output capacitor may set the start-up time. The start-up time is given by 式 5 in this case.

$$t_{SSCL} = \frac{(V_{OUT(NOM)} \times C_{OUT})}{I_{CL(MIN)}}$$

(5)

where:

- $V_{OUT(nom)}$ is the nominal output voltage
- C_{OUT} is the output capacitance
- $I_{CL(min)}$ is the minimum current limit for the device

In applications where monotonic start up is required, the soft-start time given by 式 4 must be set greater than 式 5.

The maximum recommended soft-start capacitor is 15 nF. Larger soft-start capacitors can be used and do not damage the device; however, the soft-start capacitor discharge circuit may not be able to fully discharge the soft-start capacitor when enabled. Soft-start capacitors larger than 15 nF can be a problem in applications where the enable pin must be rapidly pulsed and the device must soft-start from ground. C_{SS} must be low-leakage; X7R, X5R, or C0G dielectric materials are preferred. 表 7-2 lists suggested soft-start capacitor values.

表 7-2. Standard Capacitor Values for Programming the Soft-Start Time[1]

C_{SS}	SOFT-START TIME
Open	0.1 ms
1 nF	0.032 ms
5.6 nF	0.182 ms
10 nF	0.325 ms

(1) $t_{SS}(s) = \dfrac{V_{REF} \cdot C_{SS}}{I_{SS}} = \dfrac{0.65V \cdot C_{SS}(F)}{20\mu A}$, where $t_{SS}(s)$ = soft-start time in seconds.

Another option to set the start-up rate is to use a feedforward capacitor; see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application report for more information.

ADVANCE INFORMATION

7.5.2 Sequencing Requirements

V_{IN}, V_{BIAS}, and V_{EN} can be sequenced in any order without causing damage to the device. However, for the soft-start function to work as intended, certain sequencing rules must be applied. Connecting EN to IN is acceptable for most applications, as long as V_{IN} is greater than 1.1 V and the ramp rate of V_{IN} and V_{BIAS} is faster than the set soft-start ramp rate.

There are several different start-up responses that are possible, but not typical:

- If the ramp rate of the input sources is slower than the set soft-start time, the output tracks the slower supply minus the dropout voltage until reaching the set output voltage
- If EN is connected to BIAS, the device soft-starts as programmed, provided that V_{IN} is present before V_{BIAS}
- If V_{BIAS} and V_{EN} are present before V_{IN} is applied and the set soft-start time has expired, then V_{OUT} tracks V_{IN}
- If the soft-start time has not expired, the output tracks V_{IN} until V_{OUT} reaches the value set by the charging soft-start capacitor

図 7-3 shows the use of an RC-delay circuit to hold off V_{EN} until V_{BIAS} has ramped. This technique can also be used to drive EN from V_{IN}. An external control signal can also be used to enable the device after V_{IN} and V_{BIAS} are present.
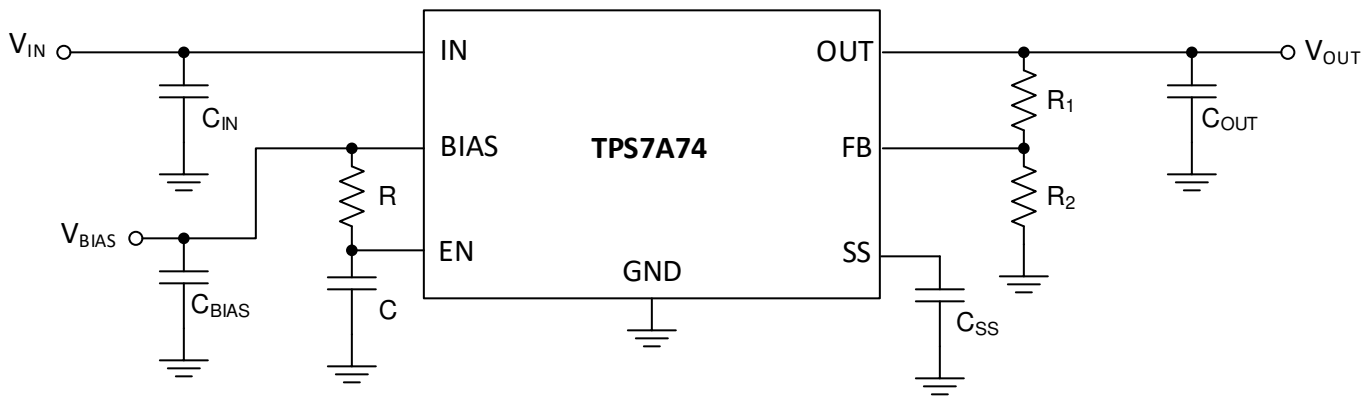

図 7-3. Soft-Start Delay Using an RC Circuit to Enable the Device

8 Application and Implementation

> **Note**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS7A74 is a low-input, low-output (LILO) low-dropout regulator (LDO) that feature soft-start capability. This regulator uses a low-current bias input to power all internal control circuitry, allowing the NMOS pass transistor to regulate very low input and output voltages.

The use of an NMOS pass transistor offers several critical advantages for many applications. Unlike a PMOS topology device, the output capacitor has little effect on loop stability. This architecture allows stability with ceramic capacitors of 10 µF or greater. Transient response is also superior to PMOS topologies, particularly for low V_{IN} applications.

A programmable voltage-controlled, soft-start circuit provides a smooth, monotonic start-up and limits start-up inrush currents that can be caused by large capacitive loads. An enable (EN) pin with hysteresis and deglitch allows slow-ramping signals to be used for sequencing the device. The low V_{IN} and V_{OUT} capability allows for inexpensive, easy-to-design, and efficient linear regulation between the multiple supply voltages often required by processor-intensive systems.

8.1.1 Adjusting the Output Voltage

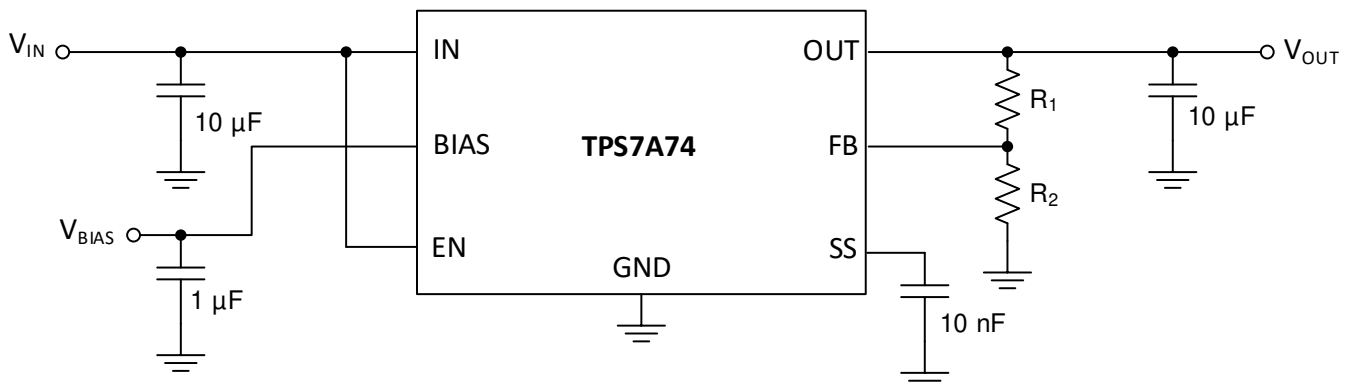図 8-1 shows the typical application circuit for the adjustable output device.

図 8-1. Typical Application Circuit for the TPS7A74 (Adjustable)

R_1 and R_2 can be calculated for any output voltage using the formula shown in 図 8-1. 表 8-1 lists sample resistor values of common output voltages. In order to achieve the maximum accuracy specifications, R_2 must be ≤ 4.99 kΩ.

ADVANCE INFORMATION

表 **8-1. Standard 1% Resistor Values for Programming the Output Voltage**[1]

R$_1$ (kΩ)	R$_2$ (kΩ)	Targeted V$_{OUT}$ (V)
Short	Open	0.65
0.768	4.99	0.75
2.43	4.53	1.00
2.72	4.42	1.05
3.48	4.99	1.10
4.22	4.99	1.20
4.99	3.83	1.50
4.99	2.80	1.80
4.99	1.74	2.51
4.99	1.21	3.33

(1) $V_{OUT} = 0.65 \times (1 + R_1/R_2)$.

Note

When V$_{BIAS}$ and V$_{EN}$ are present and V$_{IN}$ is not supplied, this device outputs approximately 50 μA of current from OUT. Although this condition does not cause any damage to the device, the output current can charge the OUT node if total resistance between OUT and GND (including external feedback resistors) is greater than 10 kΩ.

8.1.2 Input, Output, and Bias Capacitor Requirements

The device is designed to be stable for ceramic capacitor of values ≥ 10 μF. The device is also stable with multiple capacitors in parallel, which can be of any type or value.

The capacitance required on the IN and BIAS pins strongly depends on the input supply source impedance. To counteract any inductance in the input, the minimum recommended capacitor for V$_{IN}$ is 1 μF and the minimum recommended capacitor for V$_{BIAS}$ is 0.1 μF. If V$_{IN}$ and V$_{BIAS}$ are connected to the same supply, the recommended minimum capacitor for V$_{BIAS}$ is 4.7 μF. Use good quality, low equivalent series resistance (ESR) and equivalent series inductance (ESL) capacitors on the input; ceramic X5R and X7R capacitors are preferred. Place these capacitors as close the pins as possible for optimum performance.

Low ESR, ESL capacitors improve high-frequency PSRR.

8.1.3 Transient Response

The TPS7A74 is designed to have excellent transient response for most applications with a small amount of output capacitance. In some cases, the transient response can be limited by the transient response of the input supply. This limitation is especially true in applications where the difference between the input and output is less than 300 mV. In this case, adding additional input capacitance improves the transient response more than just adding additional output capacitance. With a solid input supply, adding additional output capacitance reduces undershoot and overshoot during a transient event; see 図 6-10 in the *Typical Characteristics* section. Because the TPS7A74 is stable with output capacitors as low as 10 μF, many applications may then need very little capacitance at the LDO output. For these applications, local bypass capacitance for the powered device may be sufficient to meet the transient requirements of the application. This design reduces the total solution cost by avoiding the need to use expensive, high-value capacitors at the LDO output.

8.1.4 Dropout Voltage

The TPS7A74 offers very low dropout performance, making the device well-suited for high-current, low V$_{IN}$ and low V$_{OUT}$ applications. The low dropout allows the device to be used in place of a dc/dc converter and still achieve good efficiency. 式 6 provides a quick estimate of the efficiency.

$$\text{Efficiency} \approx \frac{V_{OUT} \times I_{OUT}}{\left[V_{IN} \times (I_{IN} + I_Q) \right]} \approx \frac{V_{OUT}}{V_{IN}} \text{ at } I_{OUT} >> I_Q \tag{6}$$

This efficiency provides designers with the power architecture for their applications to achieve the smallest, simplest, and lowest cost solutions.

For this architecture, there are two different specifications for dropout voltage. The first specification (see 図 8-2) is referred to as V_{IN} *dropout* and is used when an external bias voltage is applied to achieve low dropout. This specification assumes that V_{BIAS} is at least 2.8 V above V_{OUT}, which is the case for V_{BIAS} when powered by a 5.0-V rail with 5% tolerance and with V_{OUT} = 1.5 V. If V_{BIAS} is higher than V_{OUT} + 2.8 V, the V_{IN} dropout is less than specified.

> **Note**
> 2.8 V is a test condition of this device and can be adjusted by referring to the *Electrical Characteristics* table.

The second specification (illustrated in 図 8-2) is referred to as V_{BIAS} *dropout* and applies to applications where IN and BIAS are tied together. This option allows the device to be used in applications where an auxiliary bias voltage is not available or low dropout is not required. Dropout is limited by BIAS in these applications because V_{BIAS} provides the gate drive to the pass transistor; therefore, V_{BIAS} must be 1.6 V above V_{OUT}. Because of this usage, having IN and BIAS tied together become a highly inefficient solution that can consume large amounts of power. Pay attention not to exceed the power rating of the device package.

8.1.5 Output Noise

The TPS7A74 provides low output noise when a soft-start capacitor is used. When the device reaches the end of the soft-start cycle, the soft-start capacitor serves as a filter for the internal reference. By using a 1-nF, soft-start capacitor, the output noise is reduced by half and is typically 7 μV_{RMS} for a 0.65-V output (10 Hz to 100 kHz). Further increasing C_{SS} has little effect on noise. Because most of the output noise is generated by the internal reference, the noise is a function of the set output voltage. 式 7 gives the RMS noise with a 1-nF, soft-start capacitor:

$$V_N(\mu V_{RMS}) = 7.1 \cdot \left(\frac{\mu V_{RMS}}{V} \right) \cdot V_{OUT} (V) \tag{7}$$

The low output noise makes this LDO a good choice for powering transceivers, phase-locked loops (PLLs), or other noise-sensitive circuitry.

8.1.6 Estimating Junction Temperature

Using the thermal metrics Ψ_{JT} and Ψ_{JB}, as shown in the *Thermal Information* table, the junction temperature can be estimated with corresponding formulas (given in 式 8). For backwards compatibility, an older $\theta_{JC(top)}$ parameter is listed as well.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \cdot P_D$$
$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \cdot P_D \tag{8}$$

Where P_D is the power dissipation shown by 式 9, T_T is the temperature at the center-top of the package, and T_B is the PCB temperature measured 1 mm away from the package *on the PCB surface*.

> **Note**
> Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

ADVANCE INFORMATION

For more information about measuring T_T and T_B, see the *Using New Thermal Metrics application note*, available for download at www.ti.com.

For a more detailed discussion of why TI does not recommend using $\theta_{JC(top)}$ to determine thermal characteristics, see the *Using New Thermal Metrics application report*, available for download at www.ti.com. For further information, see the *IC Package Thermal Metrics application report*, also available on the TI website.

8.2 Typical Application

8.2.1 FPGA I/O Supply at 1.8 V With a Bias Rail

V_{BIAS} = 5V ±5%
V_{IN} = 2.1V
V_{OUT} = 1.8V
I_{OUT} = 1.5A
Efficiency = 83.3%
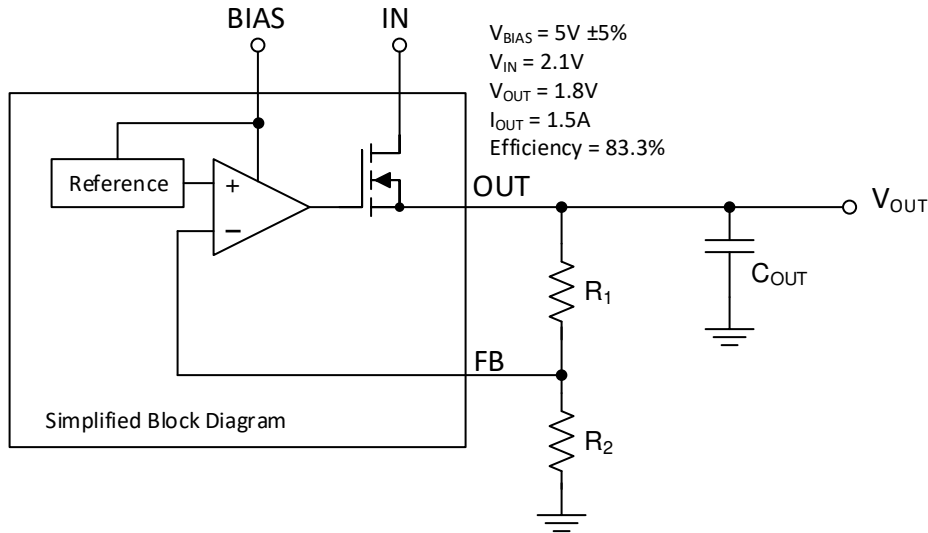
図 8-2. Typical Application Using an Auxiliary Bias Rail

8.2.1.1 Design Requirements

This application powers the I/O rails of an FPGA , at $V_{OUT(nom)}$ = 1.8 V and $I_{OUT(dc)}$ = 1.5 A. The available external supply voltages are 2.1 V, 3.3 V, and 5 V.

表 8-2 lists the parameters for this design example.

表 8-2. Design Parameters

| DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	2.1 V
V_{BIAS}	2.4 V to 5.5 V
V_{OUT}	1.8 V
I_{OUT}	600 mA (typical), 900 mA (peak)

8.2.1.2 Detailed Design Procedure

First, determine what supplies to use for the input and bias rails. A 2.1-V input can be stepped down to 1.5 V at 1.5 A if an external bias is provided, because the maximum dropout voltage is 180 mV if V_{BIAS} is at least 2.8 V higher than V_{OUT}. To achieve this voltage step, the bias rail is supplied by the 5-V supply. The approximation in 式 6 estimates the efficiency at 83.3%.

The output voltage then must be set to 1.5 V. As 表 8-1 describes, set R_1 = 4.99 kΩ and R_2= 3.82 kΩ to obtain the required output voltage. The minimum capacitor sizing requires the total solution size footprint to be reduced; see the *Input, Output, and Bias Capacitor Requirements* section for C_{IN} = 1 µF, C_{BIAS} = 1 µF, and C_{OUT} = 2.2 µF. Use C_{SS} = 1 nF for a typical 0.032-ms start-up time.

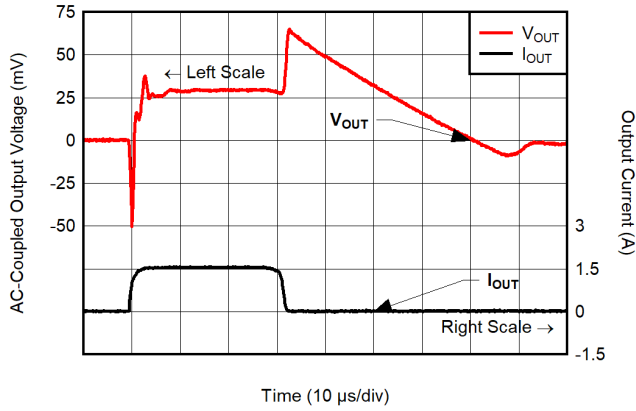図 8-2 shows a simplified version of the final circuit.

ADVANCE INFORMATION

8.2.1.3 Application Curves
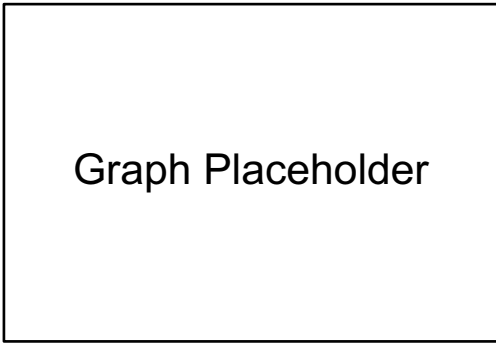
図 8-3. V$_{BIAS}$ Line Transient
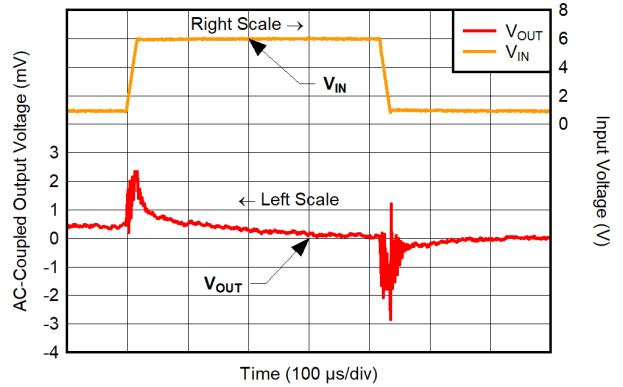
C$_{IN}$ = C$_{OUT}$ = 10 µF, C$_{BIAS}$ = 1 µF, I$_{OUT}$ = 1.5 A, V$_{IN}$ = 0.95 V to 6 V to 0.95 V

図 8-4. V$_{IN}$ Line Transient for V$_{OUT}$ = 0.65 V

C$_{IN}$ = C$_{OUT}$ = 10 µF, C$_{BIAS}$ = 1 µF, I$_{OUT}$ = 10 mA to 1.5 A to 10 mA

図 8-5. Output Load Transient Response for V$_{OUT}$ = 0.65 V
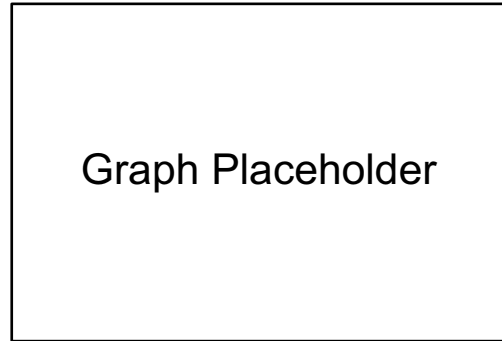
図 8-6. Turn-On Response
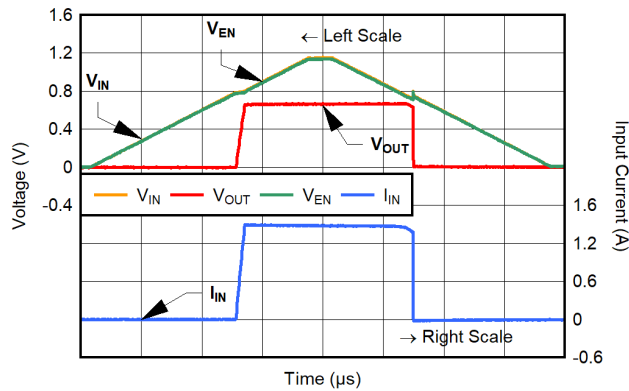
C$_{IN}$ = C$_{OUT}$ = 10 µF, C$_{BIAS}$ = 1 µF, I$_{OUT}$ = 1.5 A, V$_{IN}$ = 3.9 V to 5.8 V to 3.9 V

図 8-7. Power-Up, Power-Down for V$_{OUT}$ = 0.65 V

ADVANCE INFORMATION

ADVANCE INFORMATION

9 Power Supply Recommendations

The TPS7A74 is designed to operate from an input voltage up to 6.0 V, provided the bias rail is at least 1.6 V higher than the input supply and dropout requirements are met. The bias rail and the input supply must both provide adequate headroom and current for the device to operate normally. Connect a low output impedance power supply directly to the IN pin. This supply must have at least 1 µF of capacitance near the IN pin for optimal performance. A supply with similar requirements must also be connected directly to the bias rail with a separate 1-µF or larger capacitor. If the IN pin is tied to the bias pin, a minimum 4.7-µF capacitor is required for performance. To increase the overall PSRR of the solution at higher frequencies, use a pi-filter or ferrite bead before the input capacitor.

10 Layout

10.1 Layout Guidelines

An optimal layout can greatly improve transient performance, PSRR, and noise. To minimize the voltage drop on the input of the device during load transients, the capacitance on IN and BIAS must be connected as close as possible to the device. This capacitance also minimizes the effects of parasitic inductance and resistance of the input source and can, therefore, improve stability. To achieve optimal transient performance and accuracy, the top side of R_1 in 図 8-1 must be connected as close as possible to the load. If BIAS is connected to IN, connect BIAS as close to the sense point of the input supply as possible. This connection minimizes the voltage drop on BIAS during transient conditions and can improve the turn-on response.

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the thermal pad is critical to avoiding thermal shutdown and ensuring reliable operation. Power dissipation (P_D) of the device depends on input voltage and load conditions. 式 9 calculates P_D.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

(9)

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On the WSON (DSD) package, the primary conduction path for heat is through the exposed pad to the printed circuit board (PCB). The pad can be connected to ground or left floating; however, this pad must be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device. 式 10 calculates the maximum junction-to-ambient thermal resistance.

$$R_{\theta JA} = \frac{(+125°C - T_A)}{P_D}$$

(10)

Product Folder Links: *TPS7A74*

The minimum amount of PCB copper area required for appropriate heat sinking can be estimated using 図 10-1 by knowing the maximum $R_{\theta JA}$.

Graph Placeholder
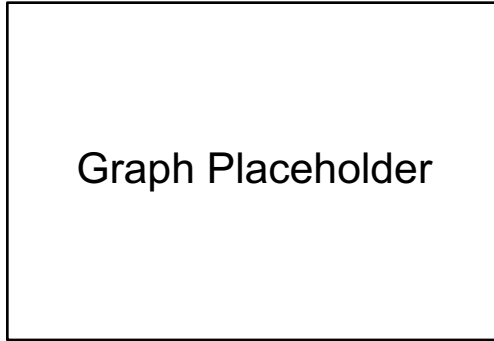
The $R_{\theta JA}$ value at a board size of 9 in^2 (that is, 3 in × 3 in) is a JEDEC standard.

図 10-1. $R_{\theta JA}$ vs Board Size

図 10-1 shows the variation of $R_{\theta JA}$ as a function of ground plane copper area in the board. This figure is intended only as a guideline to demonstrate the effects of heat spreading in the ground plane and is not be used to estimate actual thermal performance in real application environments.

Note

When the device is mounted on an application PCB, TI strongly recommends using Ψ_{JT} and Ψ_{JB}, as explained in the *Estimating Junction Temperature* section.

10.1.1 Estimating Junction Temperature

Using the thermal metrics Ψ_{JT} and Ψ_{JB}, as shown in the *Thermal Information* table, the junction temperature can be estimated with corresponding formulas (given in 式 11). For backwards compatibility, an older $\theta_{JC(top)}$ parameter is listed as well.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$
$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D$$

(11)

Where P_D is the power dissipation shown by 式 9, T_T is the temperature at the center-top of the package, and T_B is the PCB temperature measured 1 mm away from the package *on the PCB surface*.


Note

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the *Using New Thermal Metrics* application note, available for download at www.ti.com.

For a more detailed discussion of why TI does not recommend using $\theta_{JC(top)}$ to determine thermal characteristics, see the *Using New Thermal Metrics* application report, available for download at www.ti.com. For further information, see the *IC Package Thermal Metrics* application report, also available on the TI website.

ADVANCE INFORMATION

10.2 Layout Example
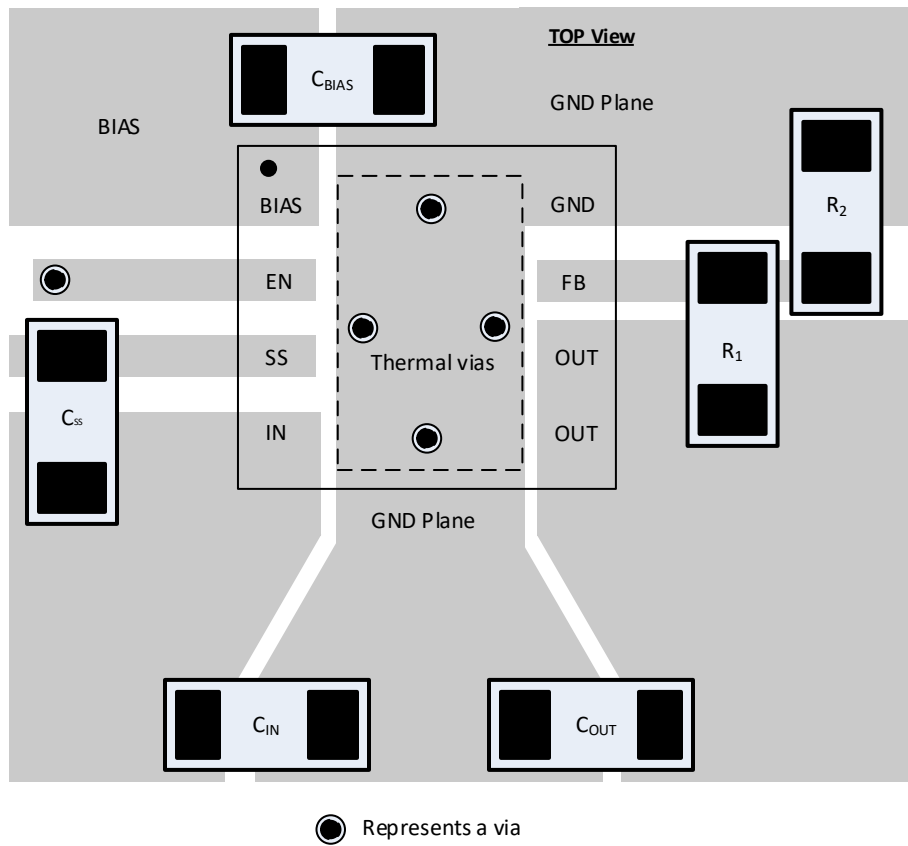
図 **10-2. Layout Example (DSD Package)**

Product Folder Links: *TPS7A74*

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS7A74. The evaluation module(and related user guide user's guide) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

11.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS7A74 is available through the product folders under *Tools & Software*.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Using New Thermal Metrics application report*
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics application report*
- Texas Instruments, *Ultimate Regulation with Fixed Output Versions of TPS742xx, TPS743xx, and TPS744xx application report*
- Texas Instruments, *Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator application report*
- Texas Instruments, *TPS74701EVM-177 and TPS74801EVM-177 user's guide*

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

11.5 Trademarks
TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

ADVANCE INFORMATION

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A7401DSDR	ACTIVE	SON	DSD	8	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7A7401	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DSD 8

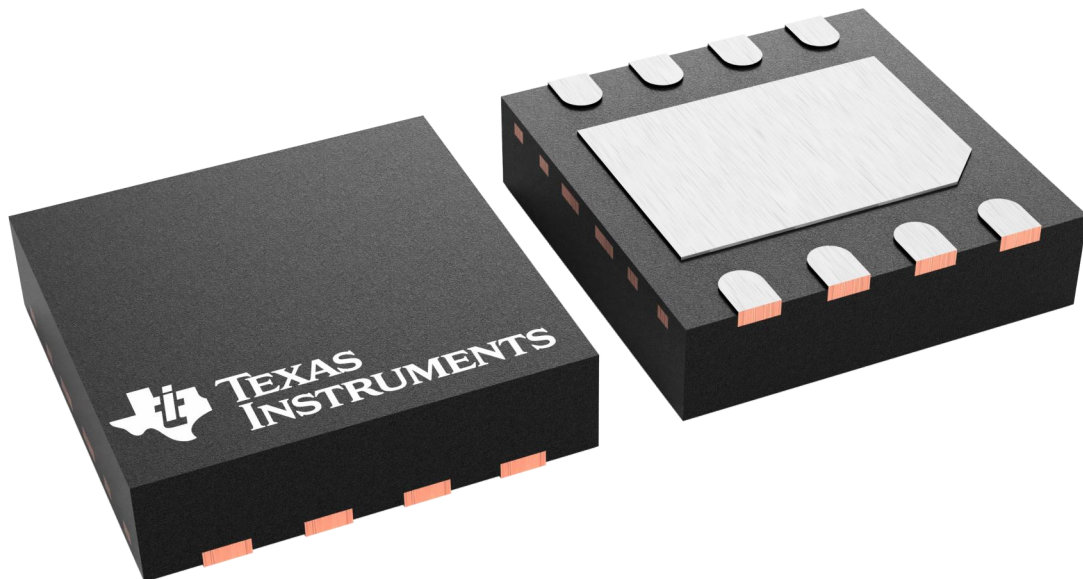**3 X 3, 0.8 mm pitch**
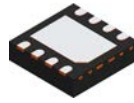
This image is a representation of the package family, actual package may vary.
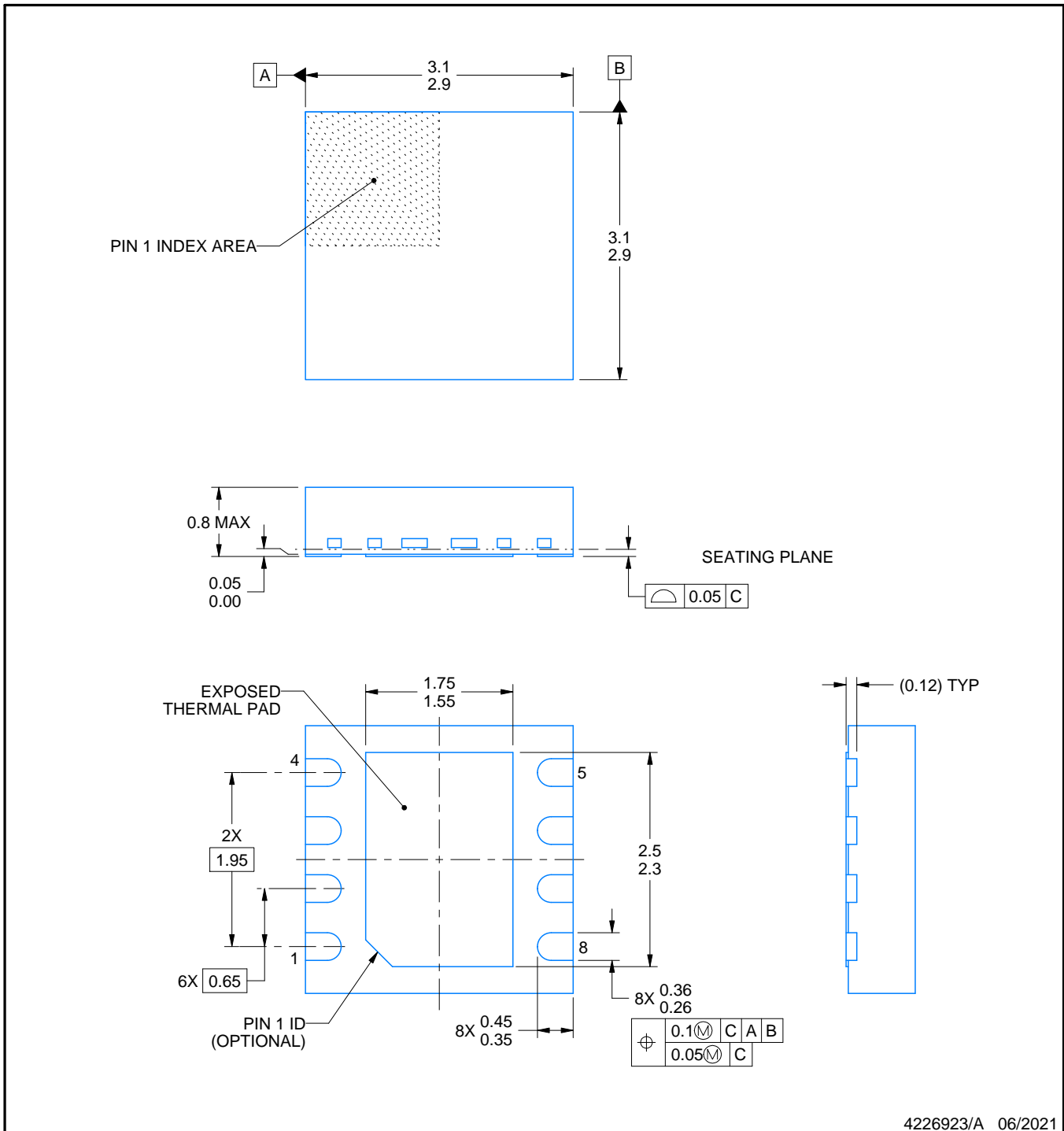Refer to the product data sheet for package details.

4227007/A

A

3.1
2.9

B

3.1
2.9

PIN 1 INDEX AREA

0.8 MAX

0.05
0.00

SEATING PLANE

0.05 C

EXPOSED
THERMAL PAD

1.75
1.55

4

5

2X
1.95

2.5
2.3

1

8

6X 0.65

PIN 1 ID
(OPTIONAL)

8X 0.45
0.35

8X 0.36
0.26

0.1 Ⓜ C A B

0.05 Ⓜ C

(0.12) TYP

4226923/A 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

TEXAS
INSTRUMENTS
www.ti.com

8X (0.6)

(1.65)

SYMM

1

8X (0.31)

8

6X (0.65)

(2.4)

4

(0.95)

(R0.05) TYP

5

(⌀ 0.2) VIA
TYP

(0.575)

(2.8)
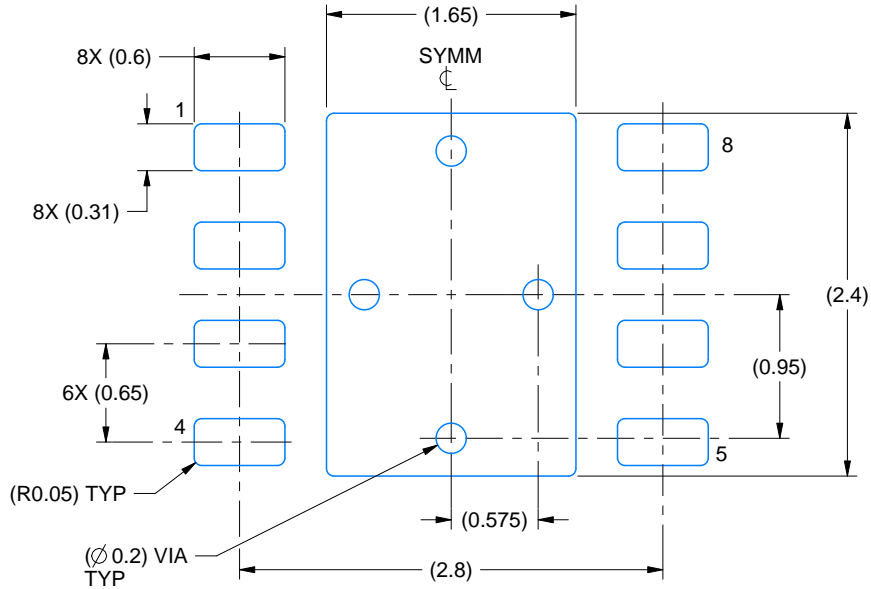
LAND PATTERN EXAMPLE
SCALE:20X

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED
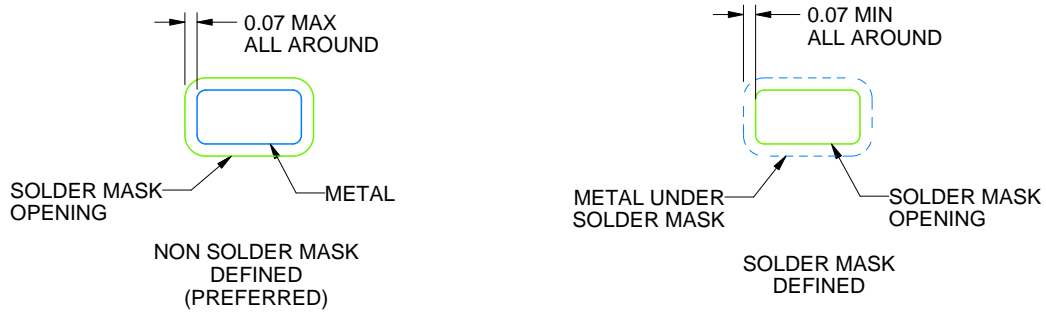
SOLDER MASK DETAILS

4226923/A   06/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

8X (0.6)

1

8X (0.31)

SYMM

6X (0.65)

4

(R0.05) TYP

SYMM

METAL
TYP

8

(0.635)

(1.07)

5

(1.47)

(2.8)
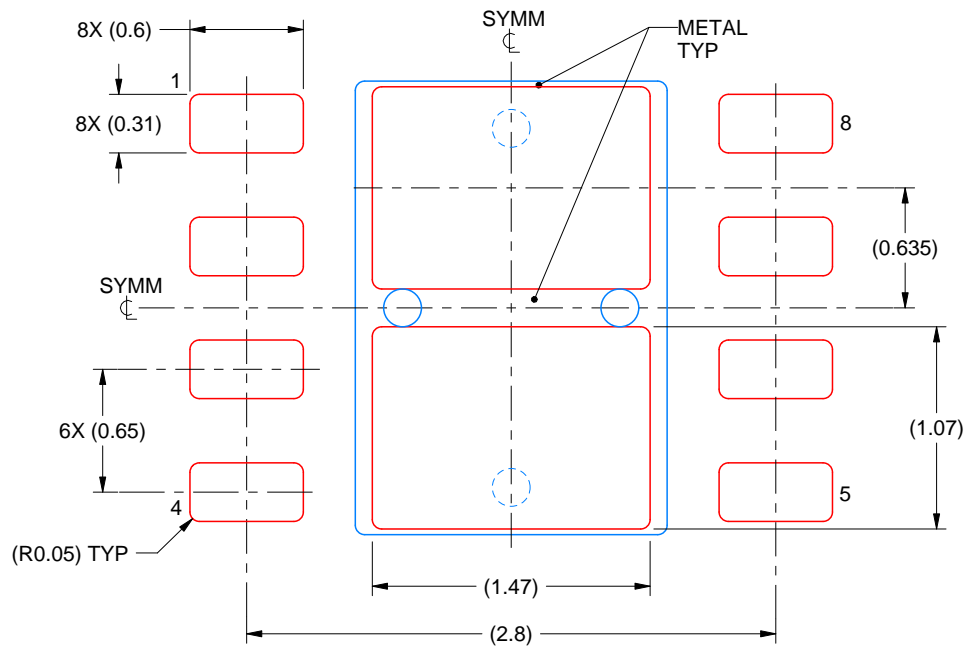
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
82% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4226923/A   06/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.