TPS7B68-Q1 500mA、40V の高電圧、超低静止電流ウォッチドッグ LDO

1 特長

- 車載アプリケーションに対応
- 下記内容で AEC-Q100 認定済み
  - デバイス温度グレード 1:動作時周囲温度範囲 –40°C～+125°C
  - デバイス HBM ESD 分類レベル 2
  - デバイス CDM ESD 分類レベル C4B
- 最大出力電流：500mA
- 4V～40V の 広い V_{IN} 入力電圧範囲、最大 45V の過渡電圧に対応
- 3.3V および 5V の固定出力
- 最大ドロップアウト電圧：600mV (500mA 時)
- 広範囲の容量 (4.7µF～500µF) および ESR (0.001Ω～20Ω) の出力コンデンサで安定動作
- 低静止電流 ($I_{(Q)}$)：
  - EN が LOW のとき (シャットダウン・モード) 4µA 未満
  - 軽負荷で $\overline{\text{WD\_EN}}$ が HIGH (ウォッチドッグ無効) のとき 19µA (標準値)
- ウィンドウ・ウォッチドッグまたは標準ウォッチドッグに構成可能
- オープンとクローズのウィンドウ比率を 1:1 または 8:1 に構成可能
- ウォッチドッグ期間を完全に調整可能 (10ms～500ms)
- 10% 精度のウォッチドッグ期間
- 専用 $\overline{\text{WD\_EN}}$ ピンによるウォッチドッグのオン/オフ制御
- パワー・グッド・スレッショルドおよびパワー・グッド遅延時間を完全に調整可能
- UVLO までの低入力電圧トラッキング
- フォルト保護機能を搭載
  - 過負荷電流制限保護
  - サーマル・シャットダウン
- 28 ピン HTSSOP パッケージ

2 アプリケーション

- 車載 MCU 電源
- 車体制御モジュール (BCM)
- ボディ・コンフォート・モジュール
- EV および HEV のバッテリ管理システム (BMS)
- 電子変速装置
- トランスミッション制御ユニット (TCU)
- 電動パワー・ステアリング (EPS)

3 概要

車載用マイクロコントローラやマイクロプロセッサの電源用途には、マイクロコントローラの動作状態を監視し、ソフトウェアの暴走を防止するためにウォッチドッグが使用されます。ウォッチドッグは、信頼性の高いシステムではマイクロコントローラから独立している必要があります。

TPS7B68-Q1 は、最大 40V の電圧で動作するように設計された 500mA ウォッチドッグ LDO であり、軽負荷時の静止電流はわずか 19µA (標準値) です。ウィンドウ・ウォッチドッグまたは標準ウォッチドッグを選択するためのプログラム可能な機能が内蔵されており、外付け抵抗によって 10% 精度でウォッチドッグ時間を設定できます。

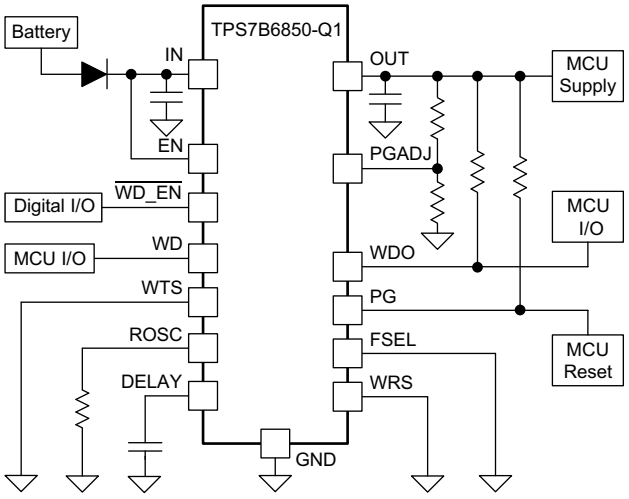
TPS7B68-Q1 の PG ピンは、出力電圧が安定し、レギュレートされていることを通知します。パワー・グッド遅延時間およびパワー・グッド・スレッショルドは、外付け部品により調整できます。また、短絡および過電流保護機能も内蔵されています。これらの機能の組み合わせにより、本デバイスは特に柔軟性に優れており、車載用途のマイクロコントローラ・システムへの電源供給に適しています。

製品情報(1)

型番	パッケージ	本体サイズ (公称)
TPS7B68-Q1	HTSSOP (28)	9.70mm×4.40mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

代表的なアプリケーションの回路図



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision B (September 2017) から **Revision C** に変更 — **Page**

- ドキュメント全体でウォッチドッグの精度を 9% から 10% に 変更 ... 1
- 「*製品情報*」表 変更 ... 1
- Changed test conditions of V_{OUT} parameter ... 7
- Added second row to V_{OUT} parameter ... 7
- Changed $V_{(dropout)}$ parameter maximum specifications from 600 mV to 800 mV at 500 mA and changed 260 mV to 325 mV at 200 mA ... 7
- Added footnote indicating dropout is not tested for the 3.3-V option at 200 mA ... 7
- Changed first row test conditions of $I_{(LIM)}$ parameter: changed V_{IN} = *5.6 V to 40 V* to V_{IN} = *5.6 V* and added voltage option ... 7
- Added second row to $I_{(LIM)}$ parameter for the 3.3-V option ... 7
- Changed $t_{(DEGLITCH)}$ parameter minimum specification from 100 µs to 55 µs ... 9
- Changed $t_{(DLY\_FIX)}$ parameter specifications: deleted minimum specification and changed maximum specification from 550 µs to 900 µs ... 9
- Changed $t_{(WD\_TOL)}$ parameter: changes test conditions, changed minim specification from –9% to –10%, and changed maximum specification from 9% to 10% ... 9
- 変更 *Several Typical Periods of Watchdog Window* table to reflect change in watchdog duration accuracy from 9% to 10% ... 17

Revision A (December 2016) から **Revision B** に変更 — **Page**

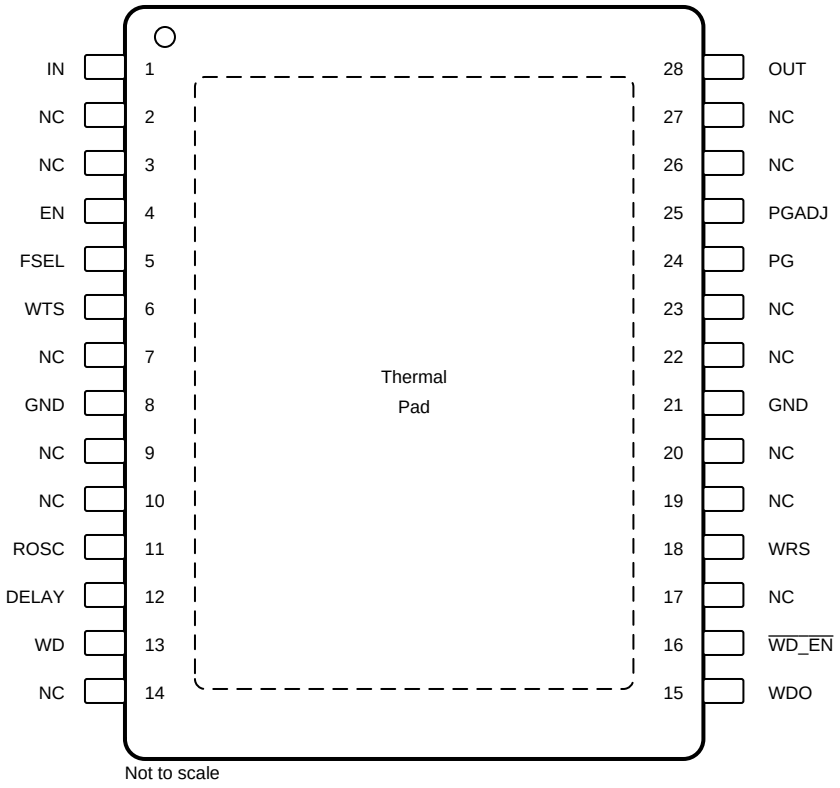
- Changed $V_{(PG\_TH)}$ symbol to $V_{(PG\_TH)\ rising}$ and $V_{(PGADJ\_TH)}$ symbol to $V_{(PGADJ\_TH)\ falling}$ in *Electrical Characteristics* table ... 8
- Added $V_{(PGADJ\_HYST)}$ parameter to *Electrical Characteristics* table ... 8
- 変更 *Adjustable Power-Good Threshold* section: updated symbols and changed Equation 1 ... 15
- 変更 parameter symbols in *Power Up and Conditions for Activation of Power Good* figure and added footnote ... 16
- 変更 parameter symbols in *Window Watchdog Operation* figure and added footnote ... 20
- 変更 parameter symbols in *Standard Watchdog Operation* figure and added footnote ... 21

2016年6月発行のものから更新 **Page**

- TPS7B6850-Q1の状態を「*製品プレビュー*」から「*量産データ*」に変更 1

5 Pin Configuration and Functions

PWP PowerPAD™ Package
28-Pin HTSSOP With Exposed Thermal Pad
Top View



Not to scale

NC - No internal connection

Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
DELAY	12	O	Power-good delay-period adjustment pin. Connect this pin via a capacitor to ground to adjust the power-good delay time.
EN	4	I	Device enable pin. Pull this pin down to low-level voltage to disable the device. Pull this pin up to high-level voltage to enable the device.
FSEL	5	I	Internal oscillator-frequency selection pin. Pull this pin down to low-level voltage to select the high-frequency oscillator. Pull this pin up to high-level voltage to select the low-frequency oscillator.
GND	8, 21	G	Ground reference
IN	1	I	Device input power-supply pin
NC	2, 3, 7, 9, 10, 14, 17, 19, 20, 22, 23, 26, 27	—	Not connected
OUT	28	O	Device 3.3-V or 5-V regulated output voltage pin
PG	24	O	Power-good pin. Open-drain output pin. Pull this pin up to V_{OUT} or to a reference through a resistor. When the output voltage is not ready, this pin is pulled down to ground.
PGADJ	25	O	Power-good threshold-adjustment pin. Connect a resistor divider between the PGADJ and OUT pins to set the power-good threshold. Connect this pin to ground to set the threshold to 91.6% of output voltage V_{OUT}.

(1) I = input, O = output, G = ground.

Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
ROSC	11	O	Watchdog timer adjustment pin. Connect a resistor between the ROSC pin and the GND pin to set the duration of the watchdog monitor. Leaving this pin open or connecting this pin to ground results in the watchdog reporting a fault at the watchdog output (WDO).
WD	13	I	Watchdog service-signal input pin.
WDO	15	O	Watchdog status pin. Open-drain output pin. Pull this pin up to OUT or a reference voltage through a resistor. When watchdog fault occurs, this pin is pulled down to a low-level voltage.
$\overline{\text{WD\_EN}}$	16	I	Watchdog enable pin. Pull this pin down to a low level to enable the watchdog. Pull this pin up to a high level to disable the watchdog.
WRS	18	I	Window ratio selection pin (only applicable for the window watchdog). Pull this pin down to a low level to set the open:closed window ratio to 1:1. Pull this pin up to high level to set the open:closed window ratio to 8:1.
WTS	6	O	Watchdog type-selection pin. To set the window watchdog, connect this pin to the GND pin. To set the standard watchdog, pull this pin high.

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Unregulated input	IN, EN	–0.3	45	V
Internal oscillator reference voltage	ROSC	–0.3	7	V
Power-good delay-timer output	DELAY	–0.3	7	V
Regulated output	OUT	–0.3	7	V
Power-good output voltage	PG	–0.3	7	V
Watchdog status output voltage	WDO	–0.3	7	V
Watchdog frequency selection, watchdog-type selection	FSEL, WTS	–0.3	45	V
Watchdog enable	$\overline{\text{WD\_EN}}$	–0.3	7	V
Watchdog service signal voltage	WD	–0.3	7	V
Window ratio selection	WRS	–0.3	7	V
Power good threshold adjustment voltage	PGADJ	–0.3	7	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to ground.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 14, 15, and 28)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Unregulated input	IN	4	40	V
40-V pins	EN, FSEL, WTS	0	V_{IN}	V
Regulated output	OUT	0	5.5	V
Power good, watchdog status, reference oscillator	PG, WDO, ROSC	0	5.5	V
Low voltage pins	WD, $\overline{WD\_EN}$, PGADJ, DELAY, WRS	0	5.5	V
Output current		0	500	mA
Operating junction temperature, T_J		–40	150	°C
Ambient temperature, T_A		–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPS7B68-Q1 PWP (HTSSOP) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	18.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

V_{IN} = 14 V, C_{OUT} ≥ 4.7 µF, 1 mΩ < ESR < 20 Ω, and T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT (IN)						
V_{IN}	Input voltage		4		40	V
$I_{(SLEEP)}$	Input sleep current	EN = OFF			4	µA
$I_{(Q)}$	Input quiescent current	V_{IN} = 5.6 V to 40 V for fixed 5-V V_{OUT}; V_{IN} = 4 V to 40 V for fixed 3.3-V V_{OUT}; EN = ON; watchdog disabled; I_{OUT} < 1 mA; T_J < 80°C		19	29.6	µA
		V_{IN} = 5.6 V to 40 V for fixed 5-V V_{OUT}; V_{IN} = 4 V to 40 V for fixed 3.3-V V_{OUT}; EN = ON; watchdog enabled; I_{OUT} < 1 mA		28	42	
		V_{IN} = 5.6 V to 40 V for fixed 5-V V_{OUT}; V_{IN} = 4 V to 40 V for fixed 3.3-V V_{OUT}; EN = ON; watchdog enabled; I_{OUT} < 100 mA		78	98	
$V_{(UVLO)}$	Undervoltage lockout, falling	Ramp V_{IN} down until output is turned off			2.6	V
$V_{(UVLO\_HYST)}$	UVLO hysteresis			0.5		V
ENABLE INPUT, WATCHDOG TYPE SELECTION AND FSEL (EN, WTS, AND FSEL)						
V_{IL}	Low-level input voltage				0.7	V
V_{IH}	High-level input voltage		2			V
V_{hys}	Hysteresis			150		mV
WATCHDOG ENABLE ($\overline{WD\_EN}$ PIN)						
V_{IL}	Low-level input threshold voltage for watchdog enable pin	Watchdog enabled			0.7	V
V_{IH}	High-level input threshold voltage for watchdog enable pin	Watchdog disabled	2			V
I_{WD_EN}	Pulldown current for watchdog enable pin	V_{WD_EN} = 5 V			3	µA
REGULATED OUTPUT (OUT)						
V_{OUT}	Regulated output	V_{IN} = V_{OUT} + 1 V to 40 V, I_{OUT} = 0 to 500 mA	–2%		2%	
		V_{IN} = 5.4 V, I_{OUT} = 250 mA T_J = –40°C to 85°C	–2%		2%	
ΔV_{OUT} (ΔVIN)	Line regulation	V_{IN} = 5.6 V to 40 V			10	mV
ΔV_{OUT} (ΔIOUT)	Load regulation	I_{OUT} = 1 mA to 500 mA			20	mV
$V_{(dropout)}$	Dropout voltage (V_{IN} – V_{OUT})(1)	I_{OUT} = 500 mA		350	800	mV
		I_{OUT} = 200 mA(2)		170	325	
I_{OUT}	Output current	V_{OUT} in regulation	0		500	mA
$I_{(LIM)}$	Output short-circuit current limit	V_{OUT} shorted to ground, V_{IN} = 5.6 V, TPS7B6850QPWPRQ1	550	690	1000	mA
		V_{OUT} shorted to ground, V_{IN} = 5.6V, TPS7B6833QPWPRQ1	490	690	1000	
PSRR	Power supply ripple rejection(3)	I_{OUT} = 100 mA; C_{OUT} = 10 µF; frequency (f) = 100 Hz		60		dB
		I_{OUT} = 100 mA; C_{OUT} = 10 µF; frequency (f) = 100 kHz		40		

(1) This test is done with V_{OUT} in regulation, measuring the V_{IN} – V_{OUT} when V_{OUT} drops by 100 mV from the rated output voltage at the specified load.
(2) Dropout is not measured for V_{OUT} = 3.3 V in this test because V_{IN} must be 4 V or greater for proper operation.
(3) Design Information – Not tested, determined by characterization.

Electrical Characteristics (continued)

V_{IN} = 14 V, C_{OUT} ≥ 4.7 µF, 1 mΩ < ESR < 20 Ω, and T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER GOOD (PG, PGADJ)						
$V_{OL(PG)}$	PG output, low voltage	I_{OL} = 5 mA, PG pulled low			0.4	V
$I_{lkg(PG)}$	PG pin leakage current	PG pulled to V_{OUT} through a 10-kΩ resistor			1	µA
$V_{(PG\_TH)}$ rising	Default power-good threshold	V_{OUT} powered above the internally set tolerance, PGADJ pin shorted to ground	89.6	91.6	93.6	% of V_{OUT}
$V_{(PG\_HYST)}$	Power-good hysteresis	V_{OUT} falling below the internally set tolerance hysteresis		2		% of V_{OUT}
PGADJ						
$V_{(PGADJ\_TH)}$ falling	Switching voltage for the power-good adjust pin	V_{OUT} is falling	1.067	1.1	1.133	V
$V_{(PGADJ\_HYST)}$	PGADJ hysteresis			26		mV
POWER-GOOD DELAY						
$I_{(DLY\_CHG)}$	DELAY capacitor charging current		3	5	10	µA
$V_{(DLY\_TH)}$	DELAY pin threshold to release PG high	Voltage at DELAY pin is ramped up	0.95	1	1.05	V
$I_{(DLY\_DIS)}$	DELAY capacitor discharging current	V_{DELAY} = 1 V	0.5			mA
CURRENT VOLTAGE REFERENCE (ROSC)						
V_{ROSC}	Voltage reference		0.95	1	1.05	V
WATCHDOG (WD, WDO, WRS)						
V_{IL}	Low-level threshold voltage for the watchdog input and window-ratio select	For WD and WRS pins			30	% of V_{OUT}
V_{IH}	High-level threshold voltage for the watchdog input and window-ratio select	For WD and WRS pins	70			% of V_{OUT}
$V_{(HYST)}$	Hysteresis			10		% of V_{OUT}
I_{WD}	Pulldown current for the WD pin	V_{WDO} = 5 V		2	4	µA
V_{OL}	Watchdog output pulled low	I_{WDO} = 5 mA			0.4	V
I_{lkg}	WDO pin leakage current	WDO pin pulled to V_{OUT} through 10-kΩ resistor			1	µA
OPERATING TEMPERATURE RANGE						
T_J	Junction temperature		–40		150	°C
$T_{(SD)}$	Junction shutdown temperature			175		°C
$T_{(HYST)}$	Hysteresis of thermal shutdown			25		°C

6.6 Switching Characteristics

V_I = 14 V, C_O ≥ 4.7 µF, 1 mΩ < ESR < 20 Ω, and T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER-GOOD DELAY (DELAY)						
$t_{(DEGLITCH)}$	Power-good deglitch time		55	180	250	µs
$t_{(DLY\_FIX)}$	Fixed power-good delay	No capacitor connect at DELAY pin		248	900	µs
$t_{(DLY)}$	Power-on-reset delay	Delay capacitor value: $C_{(DELAY)}$ = 100 nF		20		ms
WATCHDOG (WD, WDO, WRS)						
$t_{(WD)}$	Watchdog window duration	$R_{(ROSC)}$ = 20 kΩ ±1%, FSEL = LOW	9	10	11	ms
		$R_{(ROSC)}$ = 20 kΩ ±1%, FSEL = HIGH	45	50	55	
$t_{(WD\_TOL)}$	Tolerance of watchdog window duration using external resistor	$R_{(ROSC)}$ = 20 kΩ ±1% to 50 kΩ ±1%	–10%		10%	
$t_{p(WD)}$	Watchdog service-signal duration		100			µs
$t_{(WD\_HOLD)}$	Watchdog output resetting time (percentage of settled watchdog window duration)			20		% of $t_{(WD)}$
$t_{(WD\_RESET)}$	Watchdog output resetting time	$R_{(ROSC)}$ = 20 kΩ ± 1%, FSEL = LOW	1.8	2	2.2	ms
		$R_{(ROSC)}$ = 20 kΩ ± 1%, FSEL = HIGH	9	10	11	

6.7 Typical Characteristics

V_{IN} = 14 V, V_{EN} ≥ 2 V, T_J = –40°C to +150°C (unless otherwise noted)

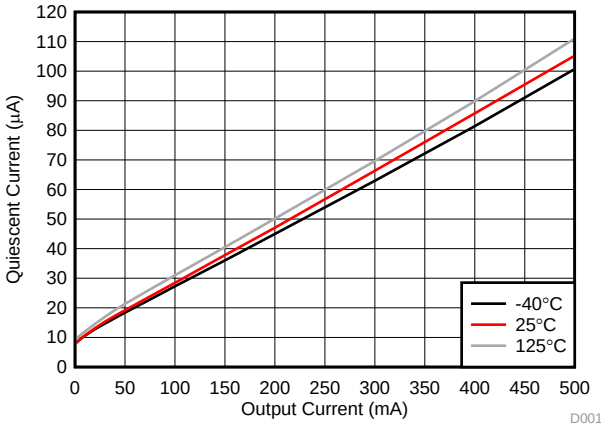


図 1. Quiescent Current vs Output Current

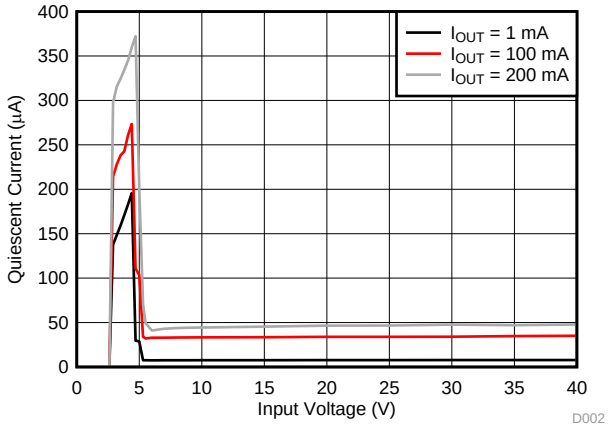


図 2. Quiescent Current vs Input Voltage

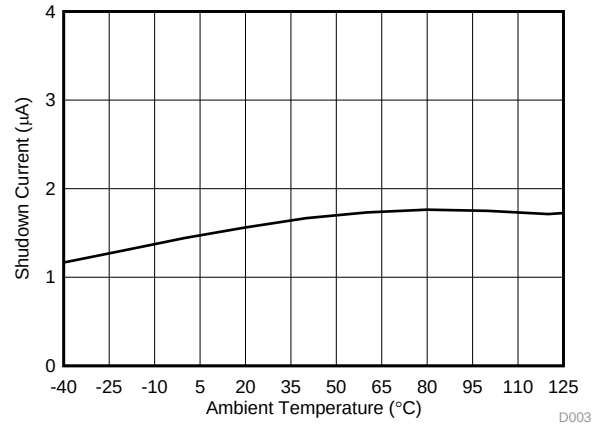


図 3. Shutdown Current vs Ambient Temperature

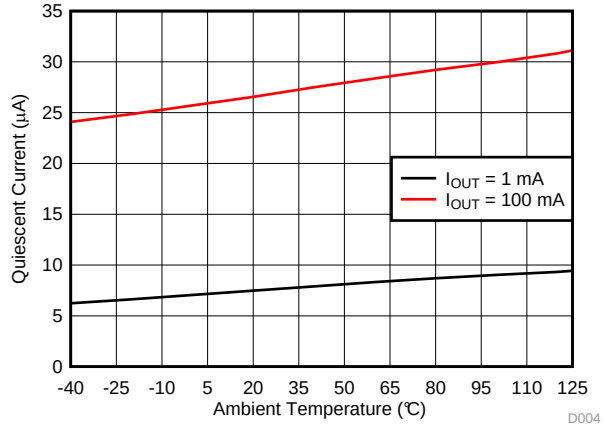


図 4. Quiescent Current vs Ambient Temperature

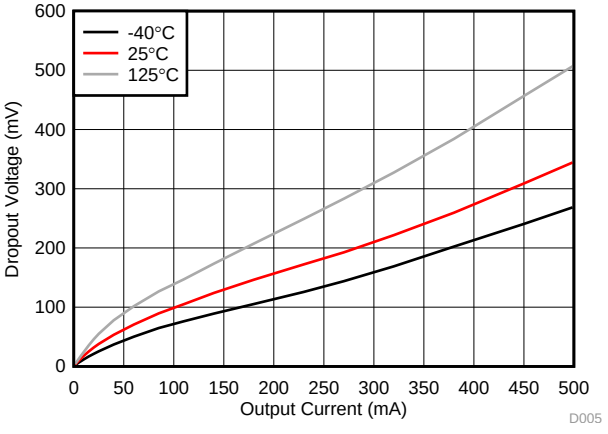
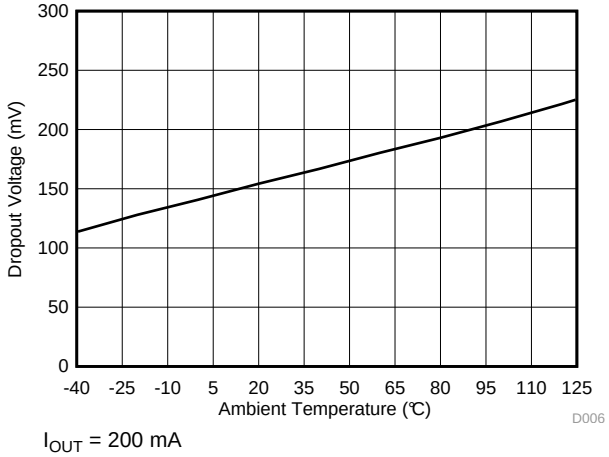


図 5. Dropout Voltage vs Output Current

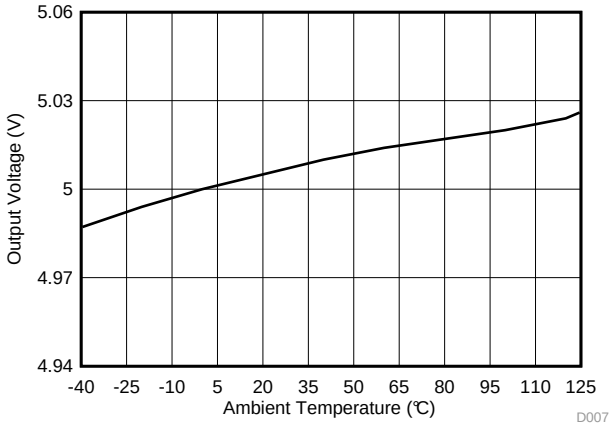


I_{OUT} = 200 mA

図 6. Dropout Voltage vs Ambient Temperature

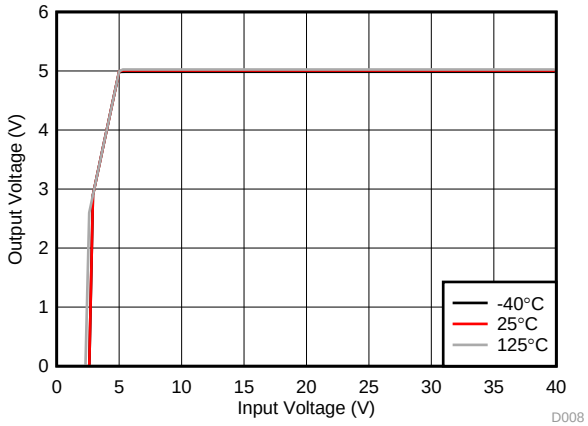
Typical Characteristics (continued)

V_{IN} = 14 V, V_{EN} ≥ 2 V, T_J = –40°C to +150°C (unless otherwise noted)



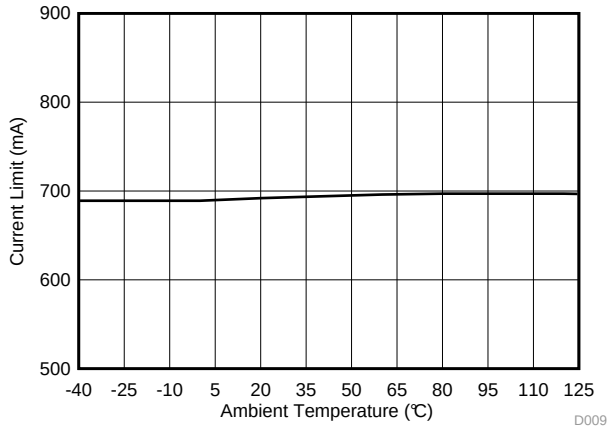
V_{OUT} = 5 V

図 7. Output Voltage vs Ambient Temperature



V_{OUT} = 5 V

図 8. Output Voltage vs Input Voltage



V_{IN} = 5.6 V

図 9. Output Current Limit (I_{LIM}) vs Ambient Temperature

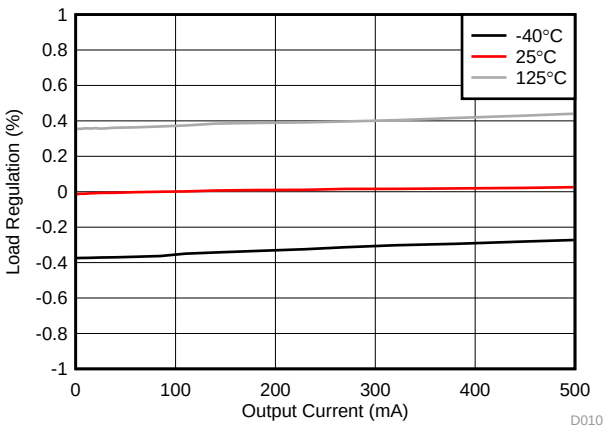


図 10. Load Regulation

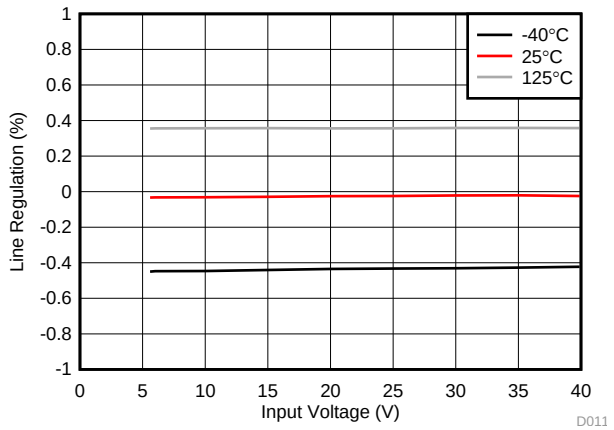
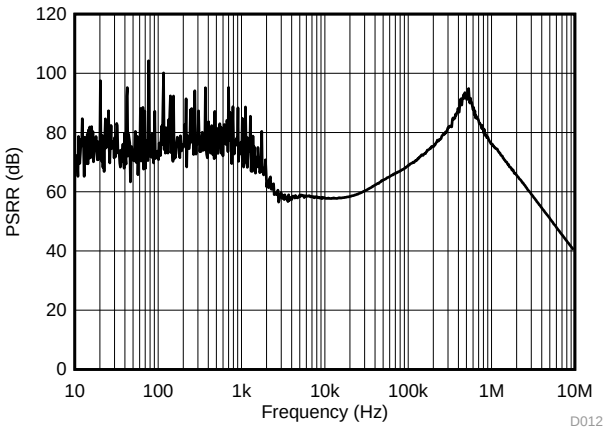


図 11. Line Regulation

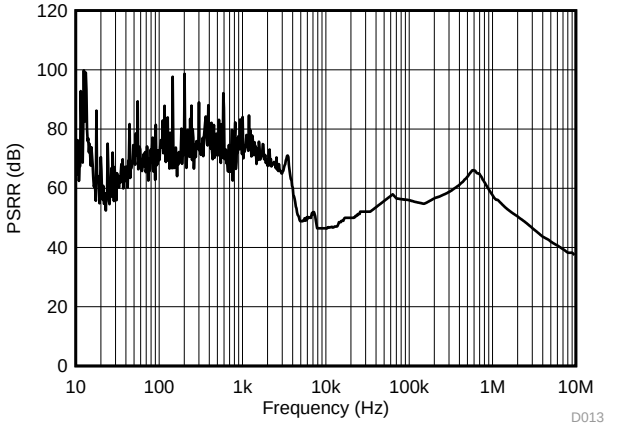


C_{OUT} = 10 µF I_{OUT} = 1 mA T_A = 25°C

図 12. PSRR vs Frequency

Typical Characteristics (continued)

V_{IN} = 14 V, V_{EN} ≥ 2 V, T_J = –40°C to +150°C (unless otherwise noted)



C_{OUT} = 10 µF I_{OUT} = 100 mA T_A = 25°C

図 13. PSRR vs Frequency

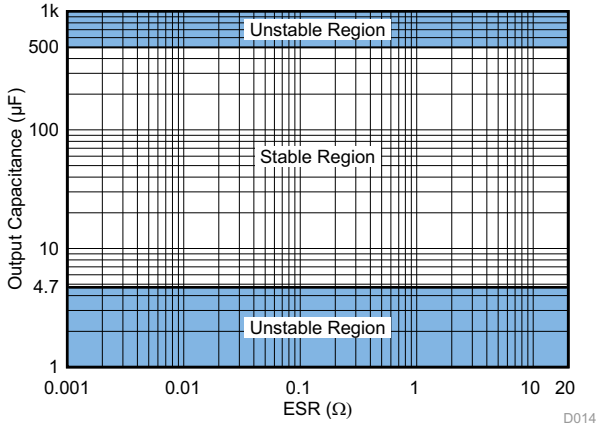
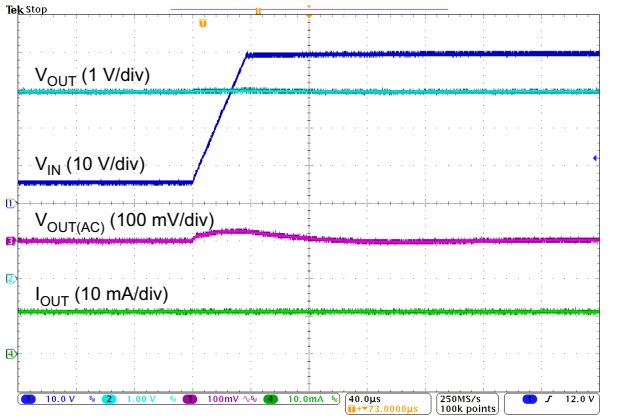
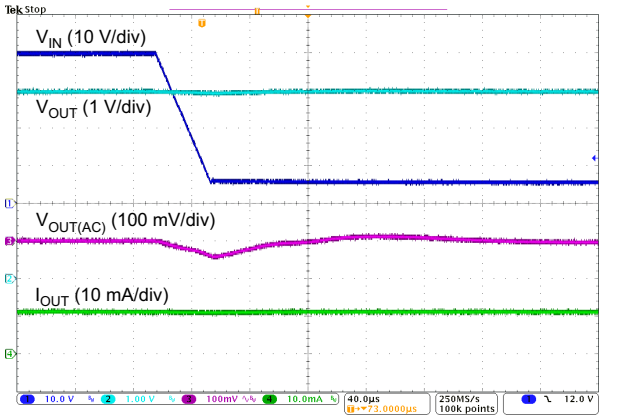


図 14. ESR Stability vs Output Capacitance



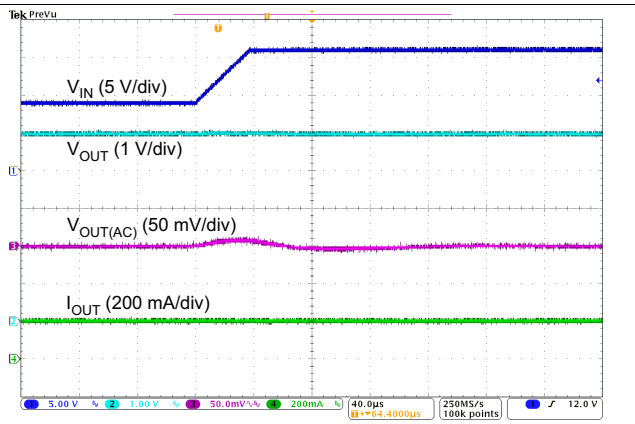
V_{IN} = 6 V to 40 V V_{OUT} = 5 V C_{OUT} = 10 µF
I_{OUT} = 1 mA

図 15. Line Transient



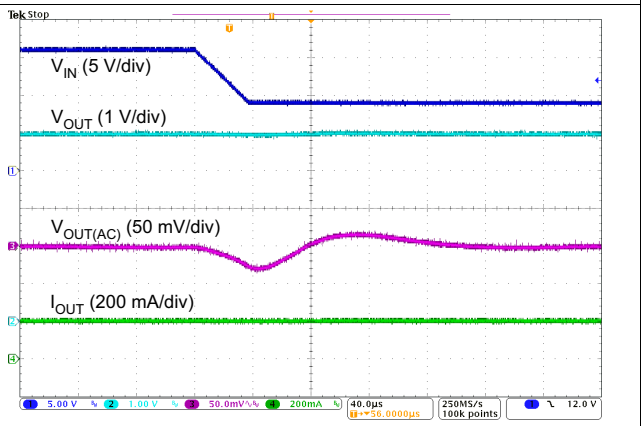
V_{IN} = 40 V to 6 V V_{OUT} = 5 V C_{OUT} = 10 µF
I_{OUT} = 1 mA

図 16. Line Transient



V_{IN} = 6 V to 40 V V_{OUT} = 5 V C_{OUT} = 10 µF
I_{OUT} = 200 mA

図 17. Line Transient

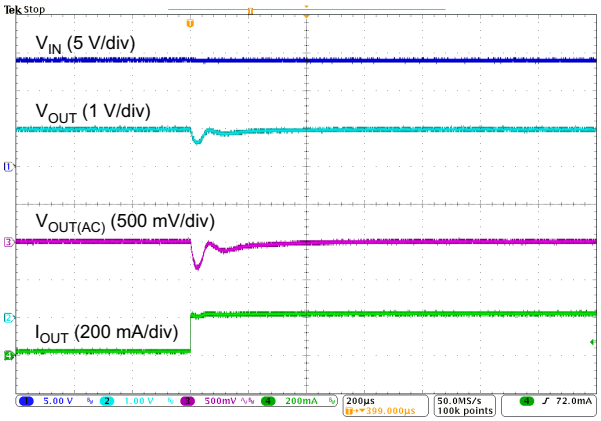


V_{IN} = 40 V to 6 V V_{OUT} = 5 V C_{OUT} = 10 µF
I_{OUT} = 200 mA

図 18. Line Transient

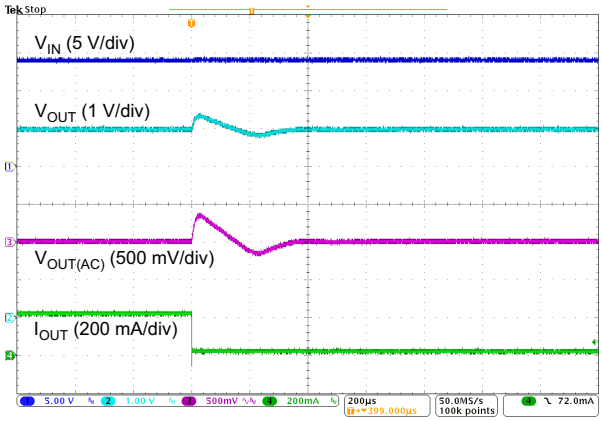
Typical Characteristics (continued)

V_{IN} = 14 V, V_{EN} ≥ 2 V, T_J = –40°C to +150°C (unless otherwise noted)



V_{OUT} = 5 V C_{OUT} = 10 µF I_{OUT} = 1 mA to 200 mA

図 19. Load Transient



V_{OUT} = 5 V C_{OUT} = 10 µF I_{OUT} = 200 mA to 1 mA

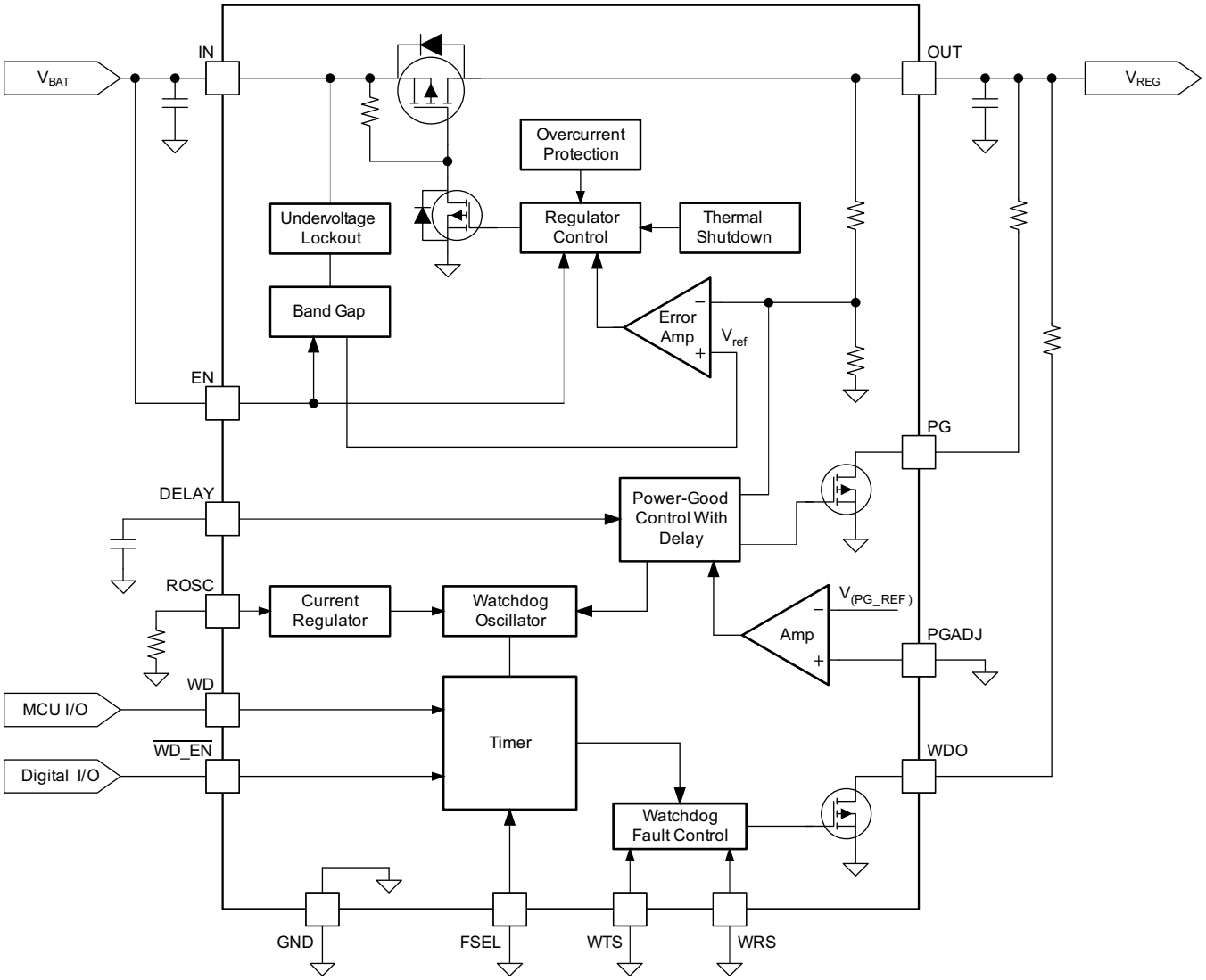
図 20. Load Transient

7 Detailed Description

7.1 Overview

The TPS7B68-Q1 is a 500-mA, 40-V monolithic low-dropout linear voltage regulator with integrated watchdog and adjustable power-good threshold functionality. This voltage regulator consumes only 19-µA quiescent current in light-load applications. Because of the adjustable power-good delay (also called power-on-reset delay) and the adjustable power-good threshold, this device is well-suited as power supplies for microprocessors and microcontrollers in automotive applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Device Enable (EN)

The EN pin is a high-voltage-tolerant pin. High input activates the devices and turns the regulators ON. Connect this input pin to an external microcontroller or a digital control circuit to enable and disable the devices, or connect to the IN pin for self-bias applications.

Feature Description (continued)

7.3.2 Adjustable Power-Good Threshold (PG, PGADJ)

The PG pin is an open-drain output with an external pullup resistor to the regulated supply, and the PGADJ pin is a power-good threshold adjustment pin. Connecting the PGADJ pin to GND sets the power-good threshold value to the default, $V_{(PG\_TH)\ rising}$. When V_{OUT} exceeds the default power-good threshold, the PG output turns high after the power-good delay period has expired. When V_{OUT} falls below $V_{(PG\_TH)\ rising} - V_{(PG\_HYST)}$, the PG output turns low after a short deglitch time.

The power-good threshold is also adjustable from 1.1 V to 5 V with external resistor divider between PGADJ and OUT. The threshold can be calculated using 式 1:

$$V_{(PG\_ADJ)\,falling} = V_{(PGADJ\_TH)\,falling} \times \frac{R1 + R2}{R2}$$

$$V_{(PG\_ADJ)\,risng} = \left[V_{(PGADJ\_TH)\,falling} + 26\ mV\ (typ) \right] \times \frac{R1 + R2}{R2}$$

where

- $V_{(PG\_ADJ)\ rising}$, $V_{(PG\_ADJ)\ falling}$ is the adjustable power-good threshold
- $V_{(PGADJ\_TH)\ falling}$ is the internal comparator reference voltage of the PGADJ pin, 1.1 V typical, 3% accuracy specified under all conditions (1)

By setting the power-good threshold $V_{(PG\_ADJ)\ rising}$, when V_{OUT} exceeds this threshold, the PG output turns high after the power-good delay period has expired. When V_{OUT} falls below $V_{(PG\_ADJ)\ falling}$, the PG output turns low after a short deglitch time.

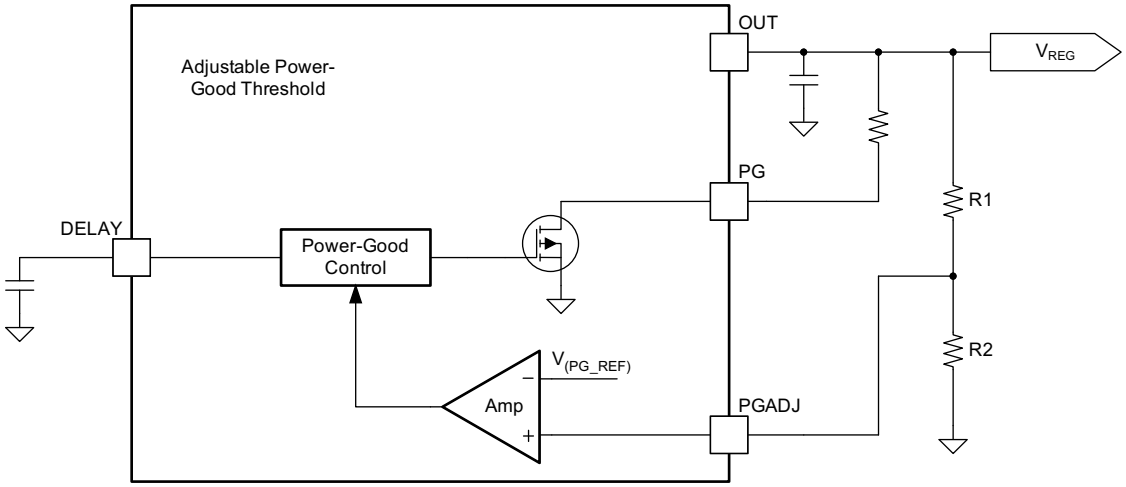


図 21. Adjustable Power Good Threshold

7.3.3 Adjustable Power-Good Delay Timer (DELAY)

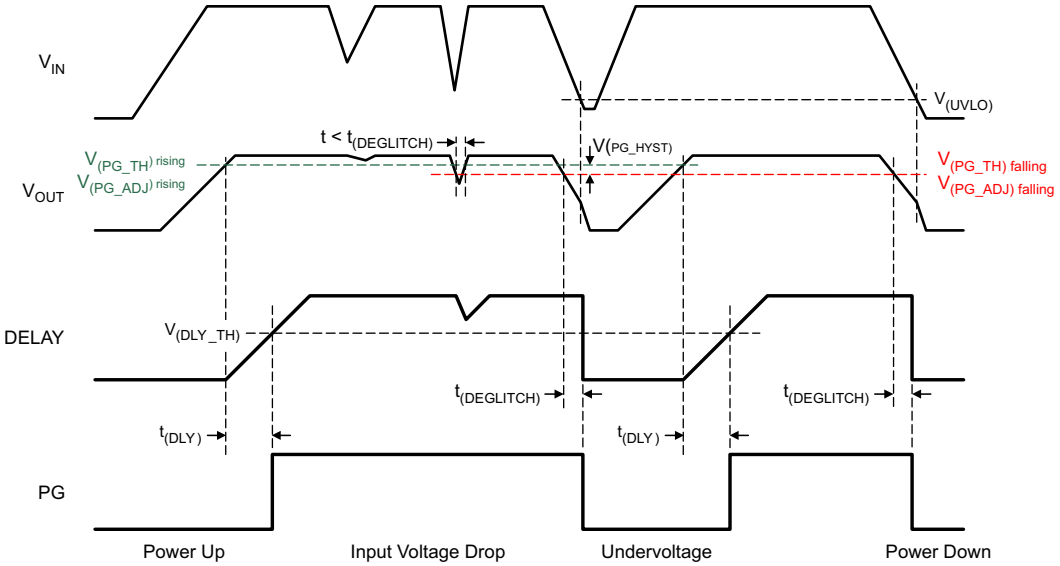
The power-good delay period is a function of the value set by an external capacitor on the DELAY pin before turning the PG pin high. Connecting an external capacitor from this pin to GND sets the power-good delay period. The constant current charges an external capacitor until the voltage exceeds a threshold to trip an internal comparator, and 式 2 determines the power-good delay period:

$$t_{(DLY)} = \frac{C_{DELAY} \times 1\ V}{5\ \mu A}$$

where

- $t_{(DLY)}$ is the adjustable power-good delay period
- C_{DELAY} is the value of the power-good delay capacitor (2)

Feature Description (continued)



NOTE: $V_{(PG\_TH)\ falling} = V_{(PG\_TH)\ rising} - V_{(PG\_HYST)}$.

図 22. Power Up and Conditions for Activation of Power Good

If the DELAY pin is open, the default delay time is $t_{(DLY\_FIX)}$.

7.3.4 Undervoltage Shutdown

This device has an integrated undervoltage lockout (UVLO) circuit to shut down the output if the input voltage falls below an internal UVLO threshold, $V_{(UVLO)}$. This ensures that the regulator does not latch into an unknown state during low input-voltage conditions. If the input voltage has a negative transient which drops below the UVLO threshold and recovers, the regulator shuts down and powers up with a normal power-up sequence when the input voltage is above the required levels.

7.3.5 Current Limit

This device features current-limit protection to keep the device in a safe operating area when an overload or output short-to-ground condition occurs. This protects the device from excessive power dissipation. For example, during a short-circuit condition on the output, fault protection limits the current through the pass element to $I_{(LIM)}$ to protect the device from excessive power dissipation.

7.3.6 Thermal Shutdown

This device incorporates a thermal shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the thermal shutdown trip point. The junction temperature exceeding the TSD trip point causes the output to turn off. When the junction temperature falls below the $T_{(SD)} - T_{(HYST)}$, the output turns on again.

7.3.7 Integrated Watchdog

This device has an integrated watchdog with fault (WDO) output option. Both window watchdog and standard watchdog are available in one device. The watchdog operation, service fault conditions, and differences between window watchdog and standard watchdog are described as follows.

Feature Description (continued)

7.3.7.1 Window Watchdog (WTS, ROSC, FSEL and WRS)

This device works in the window watchdog mode when the watchdog type selection (WTS) pin is connected to a to low voltage level. The user can set the duration of the watchdog window by connecting an external resistor (R_{ROSC}) to ground at the ROSC pin and setting the voltage level at the FSEL pin. The current through the R_{ROSC} resistor sets the clock frequency of the internal oscillator. The user can adjust the duration of the watchdog window (the watchdog timer period) by changing the resistor value. A high voltage level at the FSEL pin sets the watchdog window duration to 5 times as long as that of a low voltage level with same external component configuration.

The duration of the watchdog window and the duration of the fault output are multiples of the internal oscillator frequency, as shown by the following equations:

FSEL low	$t_{(WD)} = R_{ROSC} \times 0.5 \times 10^{-6}$	(3)
FSEL high	$t_{(WD)} = R_{ROSC} \times 2.5 \times 10^{-6}$	(4)
Watchdog initialization	$t_{(WD\_INI)} = 8 \times t_{(WD)}$	(5)
Open and closed windows	$t_{(WD)} = t_{(OW)} + t_{(CW)}$	(6)
WRS low	$t_{(OW)} = t_{(CW)} = 50\% \times t_{(WD)}$	(7)
WRS high	$t_{(OW)} = 8 \times t_{(CW)} = (8 / 9) \times t_{(WD)}$	(8)

where:

- $t_{(WD)}$ is the duration of the watchdog window
- R_{ROSC} is the resistor connected at the ROSC pin
- $t_{(WD\_INI)}$ is the duration of the watchdog initialization
- $t_{(OW)}$ is the duration of the open watchdog window
- $t_{(CW)}$ is the duration of the closed watchdog window

For all the foregoing items, the unit of resistance is Ω and the unit of time is s.

表 1 illustrates several periods of watchdog window with typical conditions.

表 1. Several Typical Periods of Watchdog Window

FSEL	$R_{(ROSC)}$ (kΩ)	$I_{(ROSC)}$ (µA)	$t_{(WD)}$ (ms)	WATCHDOG PERIOD TOLERANCE
High	200	5	500	15%
	100	10	250	10%
	50	20	125	
	40	25	100	
	25	40	62.5	
	20	50	50	
Low	100	10	50	10%
	50	20	25	
	40	25	20	
	25	40	12.5	
	20	50	10	

As shown in 図 23, each watchdog window consists of an open window and a closed window. While the window ratio selection (WRS) pin is low, each open window ($t_{(OW)}$) and closed window ($t_{(CW)}$) having a width approximately 50% of the watchdog window ($t_{(WD)}$). While the WRS pin is high, the ratio between open window and closed window is about 8:1. However, there is an exception to this; the first open window after watchdog initialization ($t_{(WD\_INI)}$) is eight times the duration of the watchdog window. The watchdog must receive the service signal (by software, external microcontroller, and so forth) during this initialization open window.

A watchdog fault occurs when servicing the watchdog during a closed window, or not servicing during an open window.

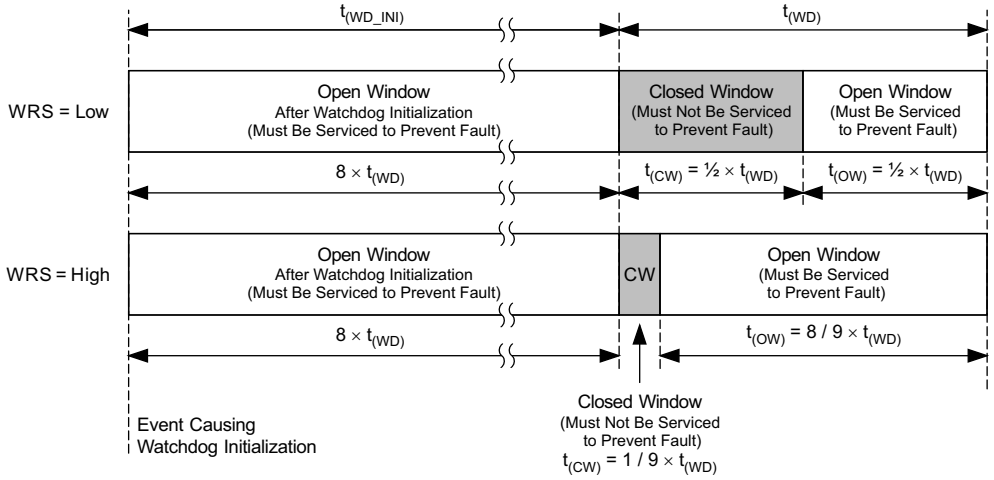


図 23. Watchdog Initialization, Open Window and Closed Window

7.3.7.2 Standard Watchdog (WTS, ROSC and FSEL)

This device works in the standard watchdog mode when the watchdog type selection (WTS) pin is connected to a high voltage level. The same as in window watchdog mode, the user can set the duration of the watchdog window by adjusting the external resistor (R_{ROSC}) value at the ROSC pin and setting the voltage level at the FSEL pin. The current through the R_{ROSC} resistor sets the clock frequency of the internal oscillator. The user can adjust the duration of the watchdog window (the watchdog timer period) by changing the resistor value. A high voltage level at the FSEL pin sets the watchdog window duration to 5 times as long as that of a low voltage level with same external component configuration.

The duration of the watchdog window and the duration of the fault output are multiples of the internal oscillator frequency as shown by the following equations:

FSEL low	$t_{(WD)} = R_{ROSC} \times 0.5 \times 10^{-6}$	(9)
FSEL high	$t_{(WD)} = R_{ROSC} \times 2.5 \times 10^{-6}$	(10)
Watchdog initialization	$t_{(WD\_INI)} = 8 \times t_{(WD)}$	(11)

where:

- $t_{(WD)}$ is the duration of the watchdog window
- R_{ROSC} is the resistor connected at the ROSC pin
- $t_{(WD\_INI)}$ is the duration of the watchdog initialization

For all the foregoing items, the unit of resistance is Ω and the unit of time is s

Compared with window watchdog, there is no closed window in standard watchdog mode. The standard watchdog receives a service signal at any time within the watchdog window. The watchdog fault occurs when not servicing watchdog during the watchdog window.

7.3.7.3 Watchdog Service Signal and Watchdog Fault Outputs (WD and WDO)

The correct watchdog service signal (WD) must stay high for at least 100 µs. The WDO pin is the fault output terminal and is tied high through a pullup resistor to a regulated output supply. When a watchdog fault occurs, the device momentarily pulls WDO low for a duration of $t_{(WD\_HOLD)}$.

$$t_{(WD\_HOLD)} = 20\% \times t_{(WD)} \quad (12)$$

7.3.7.4 ROSC Status Detection (ROSC)

When a watchdog function is enabled, if the ROSC pin is shorted to GND or open, the watchdog output (WDO) pin remains low, indicating a fault status. If watchdog function is disabled, ROSC pin status detection does not work.

7.3.7.5 Watchdog Enable (PG and $\overline{\text{WD\_EN}}$)

When PG (power good) is high, an external microcontroller or a digital circuit can apply a high or low logic signal to the $\overline{\text{WD\_EN}}$ pin to disable or enable the watchdog. A low input to this pin turns the watchdog on, and a high input turns the watchdog off. If PG is low, the watchdog is disabled and the watchdog-fault output (WDO) pin stays in the high-impedance state.

7.3.7.6 Watchdog Initialization

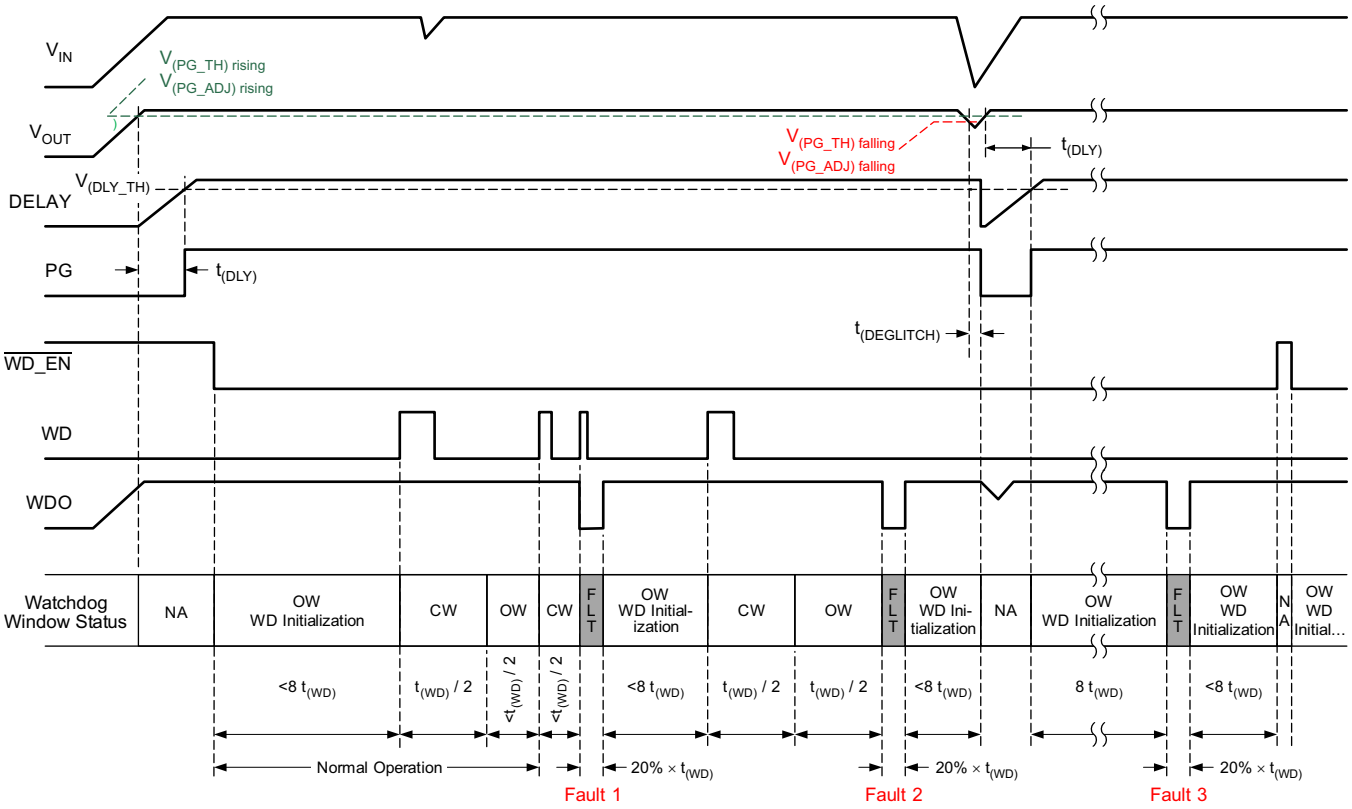
On power up and during normal operation, the watchdog initializes under the conditions shown in 表 2.

表 2. Conditions for Watchdog Initialization

EDGE	WHAT CAUSES THE WATCHDOG TO INITIALIZE
↑	Rising edge of PG (power good) while the watchdog is in the enabled state, for example, during soft power up
↓	Falling edge of $\overline{\text{WD\_EN}}$ while PG is already high, for example, when the microprocessor enables the watchdog after the device is powered up
↑	Rising edge of WDO while PG is already high and the watchdog is in the enabled state, for example, right after a closed window is serviced

7.3.7.7 Window Watchdog Operation (WTS = Low)

The window watchdog is able to monitor whether the frequency of the watchdog service signal (WD) is within certain ranges. A watchdog low-voltage fault is reported when the frequency of the watchdog service signal is out of the setting range. 図 24 shows the window watchdog initialization and operation for the TPS7B68-Q1 (WRS is low). After the output voltage is in regulation and PG is high, the window watchdog becomes enabled when an external signal pulls $\overline{\text{WD\_EN}}$ (the watchdog enable pin) low. This causes the watchdog to initialize and wait for a service signal during the first initialization window for 8 times the duration of $t_{(WD)}$. A service signal applied to the WD pin during the initialization open window resets the watchdog counter and a closed window starts. To prevent a fault condition from occurring, watchdog service must not occur during the closed window. Watchdog service must occur during the following open window to prevent a fault condition from occurring. The fault output (WDO), externally pulled up to V_{OUT} (typical), stays high as long as the watchdog receives a proper service signal and there is no other fault condition.



NOTE: $V_{(PG\_TH)\ rising} = V_{(PG\_TH)\ falling} + V_{(PG\_HYST)}$.

図 24. Window Watchdog Operation

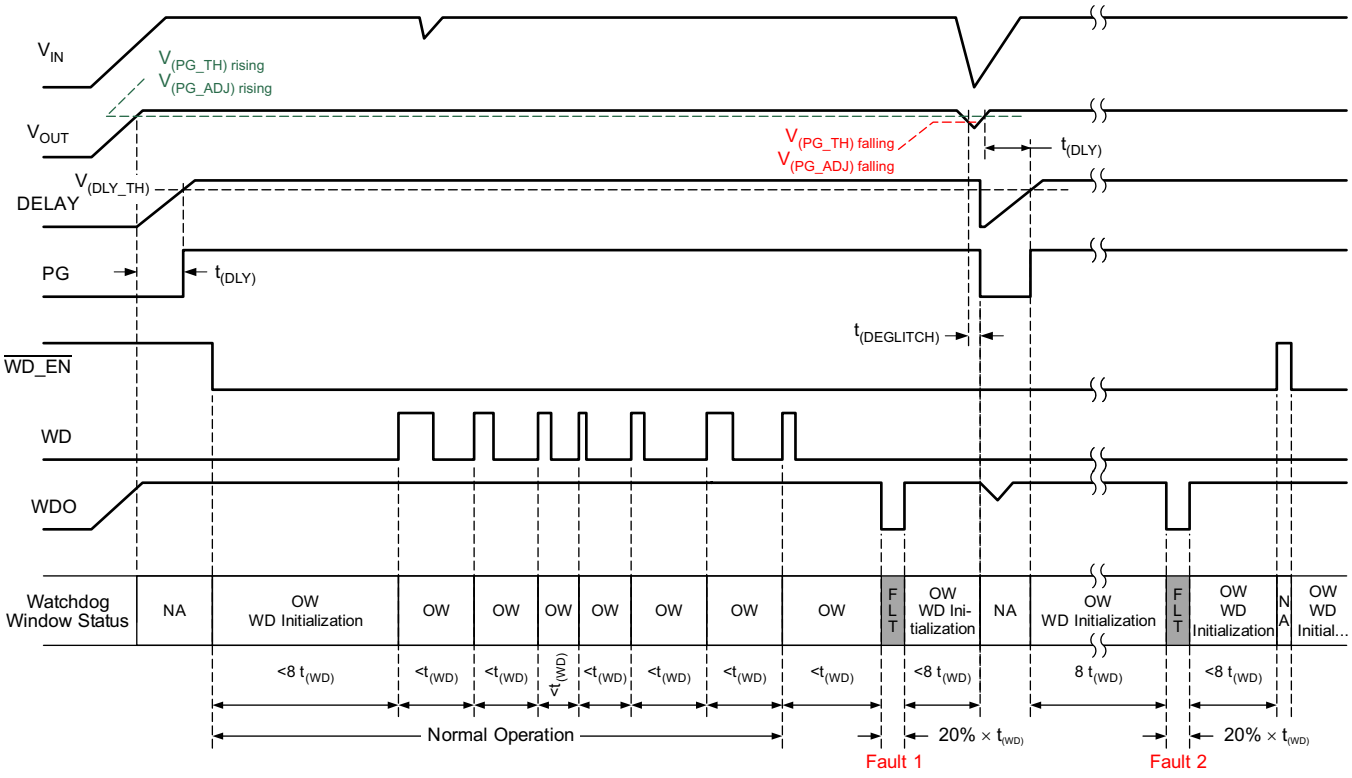
Three different fault conditions occur in 図 24:

- Fault 1: The watchdog service signal is received during the closed window. The WDO is triggered one time, receiving a WD rising edge during the closed window.
- Fault 2: The watchdog service signal is not received during the open window. WDO is triggered after the maximum open-window duration $t_{(WD)}$ / 2.
- Fault 3: The watchdog service signal is not received during the WD initialization. WDO is triggered after the maximum initialization window duration 8 × $t_{(WD)}$.

7.3.7.8 Standard Watchdog Operation (WTS = High)

The standard watchdog is able to monitor whether the frequency of the watchdog service signal (WD) is lower than a certain value. A watchdog low-voltage fault is reported when the frequency of the watchdog service signal is lower than the set value.

図 25 shows the standard watchdog initialization and operation for the TPS7B68-Q1. Similar to the window watchdog, after output the voltage is in regulation and PG asserts high, the standard watchdog becomes enabled when an external signal pulls $\overline{WD\_EN}$ low. This causes the standard watchdog to initialize and wait for a service signal during the first initialization window for 8 times the duration of $t_{(WD)}$. A service signal applied to the WD pin during the first open window resets the watchdog counter and another open window starts. To prevent a fault condition from occurring, watchdog service must occur during the every open window to prevent a fault condition from occurring. The fault output (WDO), externally pulled up to V_{OUT} (typical), stays high as long as the watchdog receives proper service and there is not fault condition.



NOTE: $V_{(PG\_TH)\ rising} = V_{(PG\_TH)\ falling} + V_{(PG\_HYST)}$.

図 25. Standard Watchdog Operation

Two different fault conditions occur in 図 25:

- Fault 1: The watchdog service signal is not received during the open window. WDO is triggered after the maximum open-window duration $t_{(WD)}$ / 2.
- Fault 2: The watchdog service signal is not received during the WD initialization. WDO is triggered after the maximum initialization window duration 8 × $t_{(WD)}$.

7.4 Device Functional Modes

7.4.1 Operation With Input Voltage Lower Than 4 V

The device normally operates with input voltages above 4 V. The device can also operate at lower input voltages; the maximum UVLO voltage is 2.6 V. At input voltages below the actual UVLO voltage, the device does not operate.

7.4.2 Operation With Input Voltage Higher Than 4 V

When the input voltage is greater than 4 V, if the input voltage is higher than the output set value plus the device dropout voltage, then the output voltage is equal to the set value. Otherwise, the output voltage is equal to the input voltage minus the dropout voltage.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7B68-Q1 device is a 500-mA low-dropout watchdog linear regulator with ultralow quiescent current. The PSpice transient model is available for download on the product folder and can be used to evaluate the basic function of the device.

8.2 Typical Application

図 26 shows a typical application circuit for the TPS7B68-Q1. Different values of external components can be used, depending on the end application. An application may require a larger output capacitor during fast load steps to prevent a large drop on the output voltage. TI recommends using a low-ESR ceramic capacitor with a dielectric of type X7R.

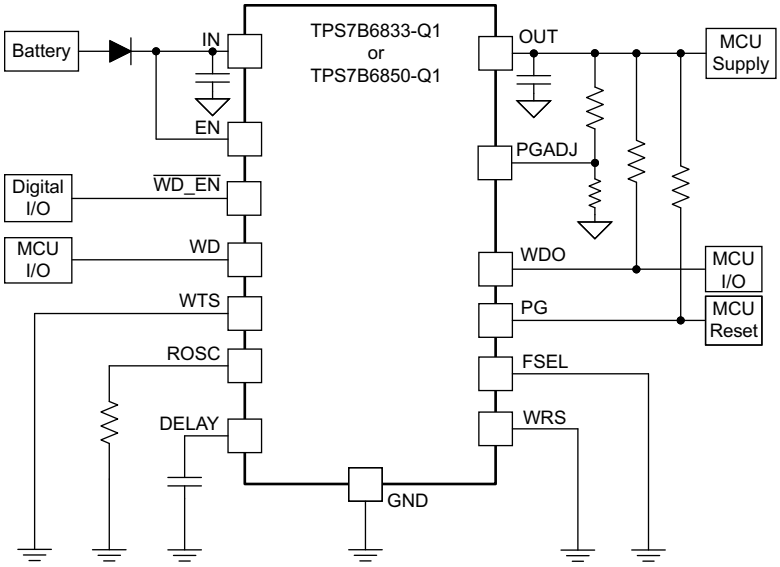


図 26. TPS7B68-Q1 Typical Application Schematic

Typical Application (continued)

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 3.

表 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUES
Input voltage range	4 V to 40 V for TPS7B6833-Q1 5.6 V to 40 V for TPS7B6850-Q1
Input capacitor range	10 μF to 22 μF
Output voltage	3.3 V, 5 V
Output current rating	500 mA maximum
Output capacitor range	4.7 μF to 500 μF
Power-good threshold	Adjustable or fixed
Power-good delay capacitor	100 pF to 100 nF
Watchdog type	Standard watchdog or window watchdog
Watchdog window periods	10 ms to 500 ms

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Output current
- Power-good threshold
- Power-good delay capacitor
- Watchdog type
- Watchdog window period

8.2.2.1 Input Capacitor

When using a TPS7B68-Q1 device, TI recommends adding a 10-μF to 22-μF capacitor with a 0.1 μF ceramic bypass capacitor in parallel at the input to keep the input voltage stable. The voltage rating must be greater than the maximum input voltage.

8.2.2.2 Output Capacitor

Ensuring the stability of the TPS7B68-Q1 requires an output capacitor with a value in the range from 4.7 μF to 500 μF and with an ESR range from 0.001 Ω to 20 Ω. TI recommends selecting a ceramic capacitor with low ESR to improve the load transient response.

8.2.2.3 Power-Good Threshold

The power-good threshold is set by connecting PGADJ to GND or to a resistor divider from OUT to GND. The *Adjustable Power-Good Threshold (PG, PGADJ)* section provides the method for setup the power-good threshold.

8.2.2.4 Power-Good Delay Period

The power-good delay period is set by an external capacitor (C_{DELAY}) to ground, with a typical capacitor value from 100 pF to 100 nF. Calculate the correct capacitance for the application using 式 2.

8.2.2.5 Watchdog Setup

The *Integrated Watchdog* section discusses the watchdog type selection and watchdog window-period setup method.

8.2.3 Application Curves

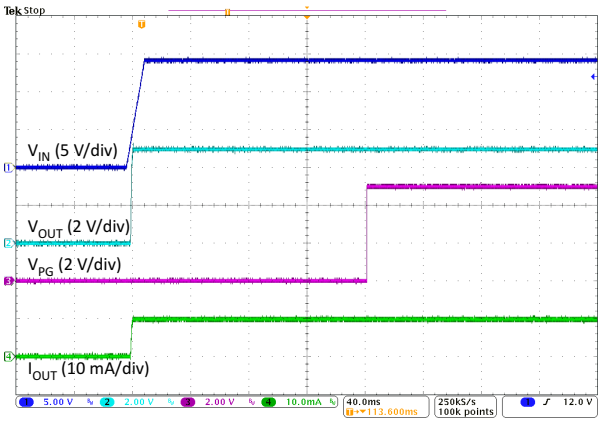


図 27. TPS7B6850-Q1 Power-Up Waveform

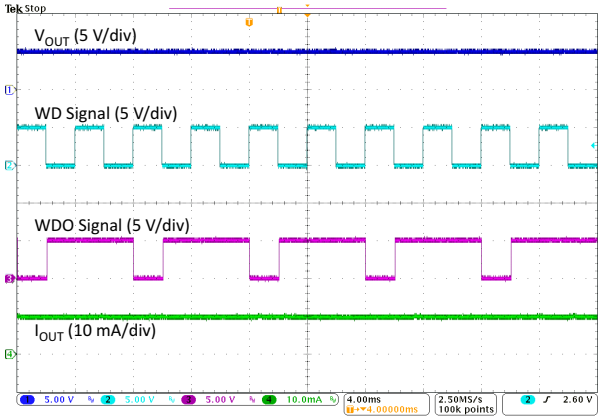


図 28. TPS7B6850-Q1 Watchdog Fault (High Frequency Watchdog Service Signal)

9 Power Supply Recommendations

The device is designed to operate from an input-voltage supply range from 4 V to 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7B68-Q1 device, TI recommends adding a capacitor with a value of ≥10 μF with a 0.1 μF ceramic bypass capacitor in parallel at the input.

10 Layout

10.1 Layout Guidelines

For LDO power supplies, especially high-voltage and high-current ones, layout is an important step. If layout is not carefully designed, the regulator could not deliver enough output current because of thermal limitation. To improve the thermal performance of the device and maximize the current output at high ambient temperature, TI recommends spreading the thermal pad as much as possible and put enough thermal vias on the thermal pad. 図 29 shows an example layout.

10.2 Layout Example

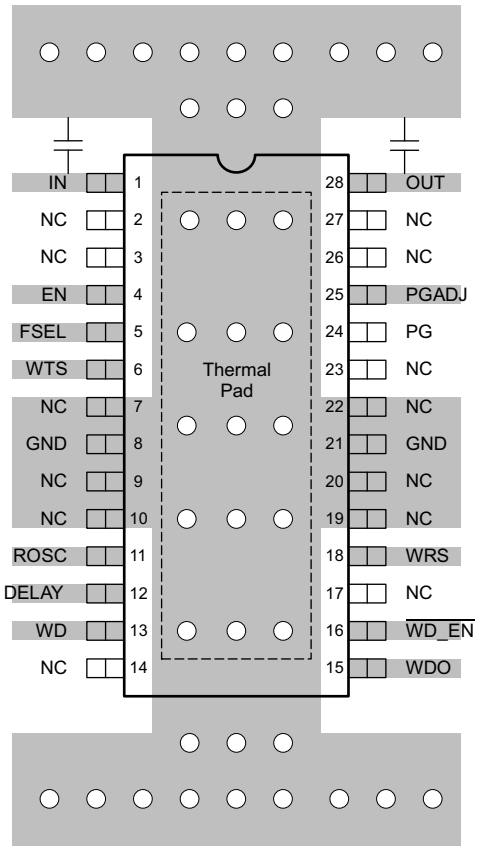


図 29. Layout Recommendation

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください。

テキサス・インスツルメンツ、*『TPS7B68-Q1 評価基板』ユーザー・ガイド*

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商標

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7B6833QPWPRQ1	ACTIVE	HTSSOP	PWP	28	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	7B6833Q	Samples
TPS7B6850QPWPRQ1	ACTIVE	HTSSOP	PWP	28	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	7B6850Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

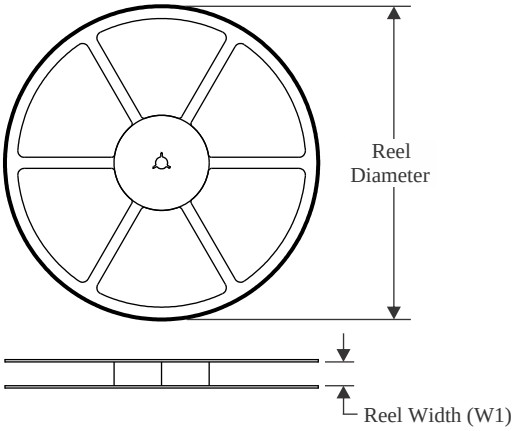
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

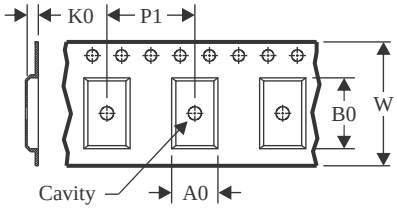
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

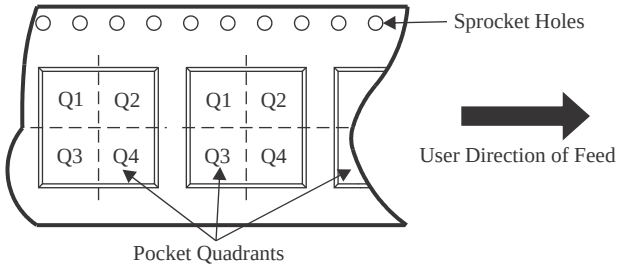


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

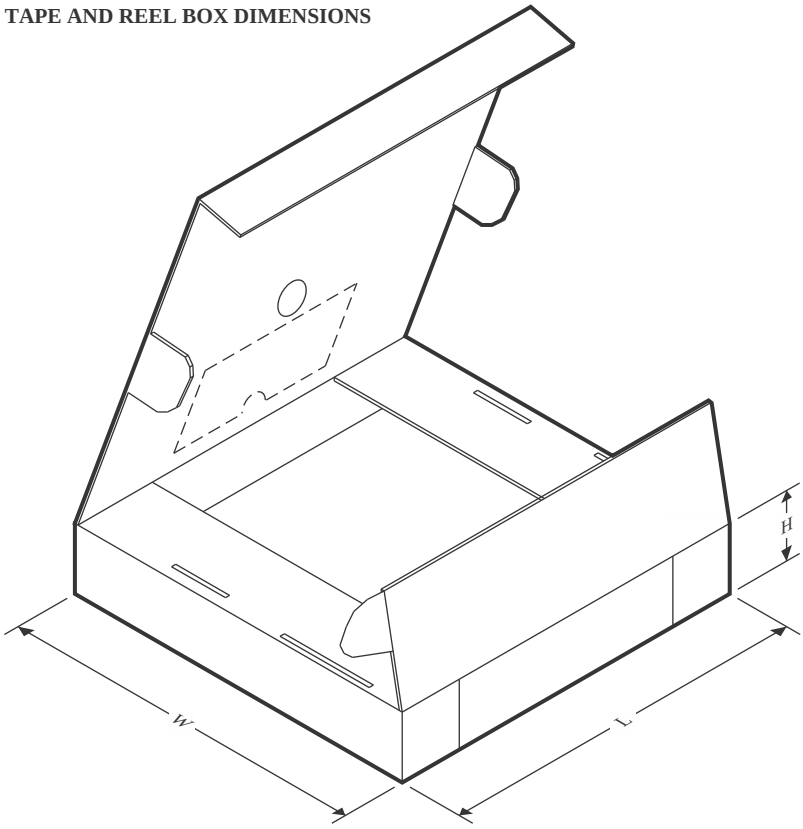
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7B6833QPWPRQ1	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TPS7B6850QPWPRQ1	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7B6833QPWPRQ1	HTSSOP	PWP	28	2000	350.0	350.0	43.0
TPS7B6850QPWPRQ1	HTSSOP	PWP	28	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

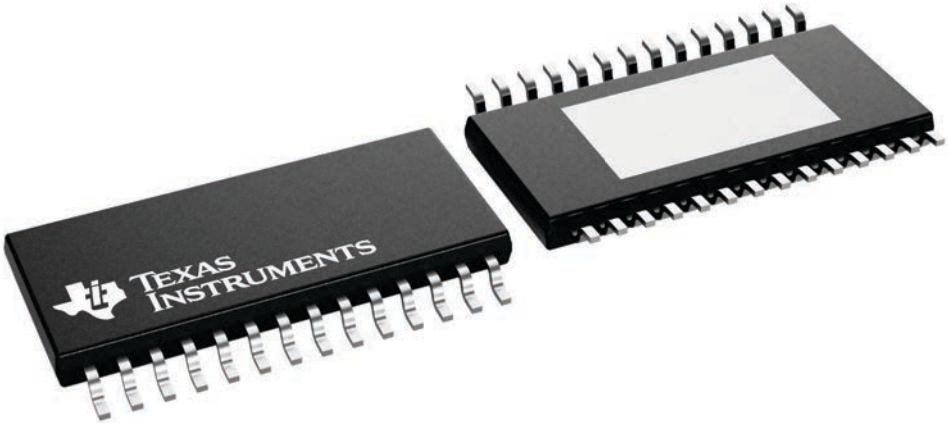
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

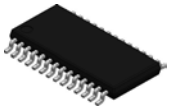
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

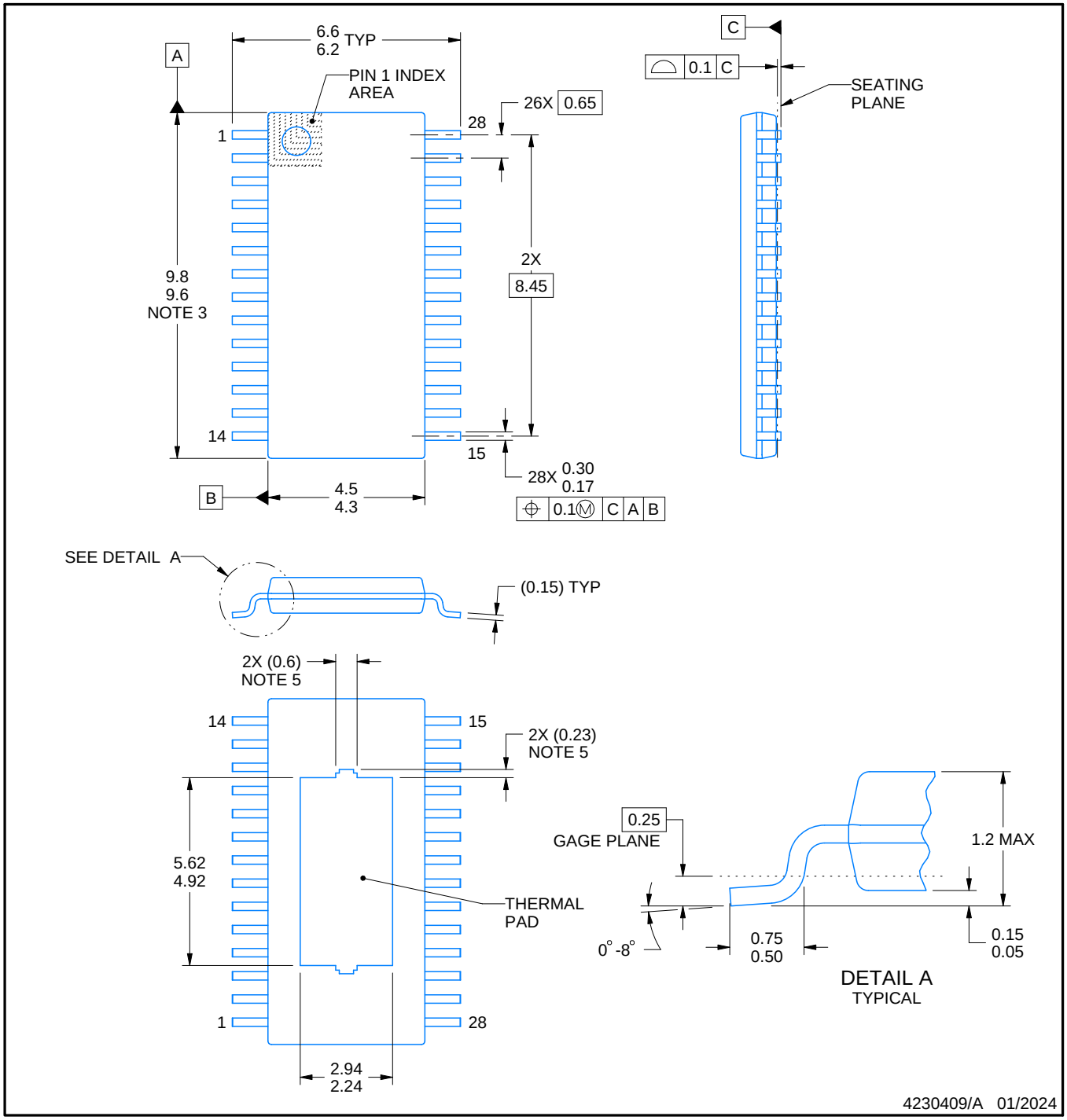
PACKAGE OUTLINE

PWP0028V



PowerPAD™ TSSOP - 1.2 mm max height

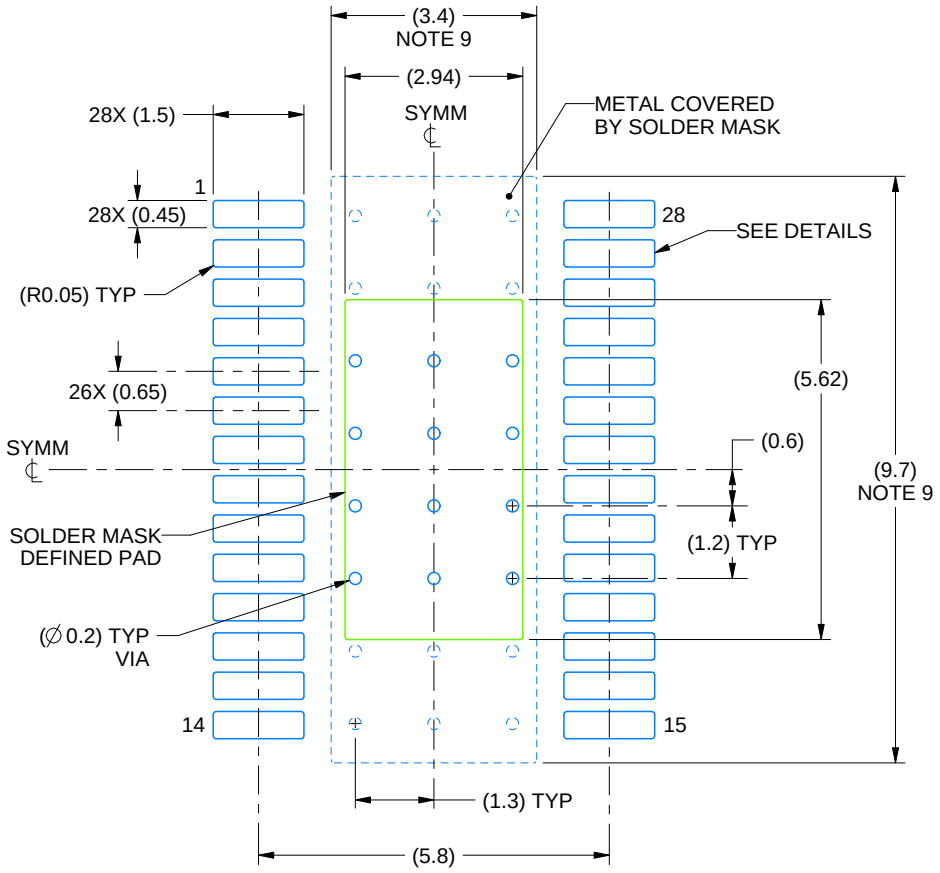
SMALL OUTLINE PACKAGE



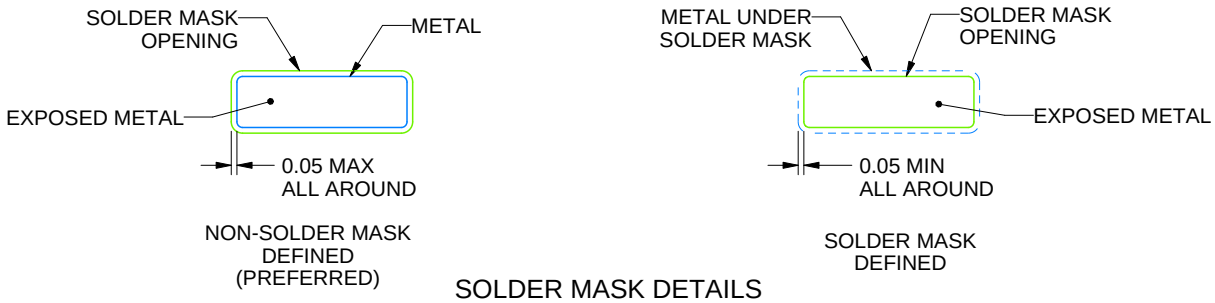
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS

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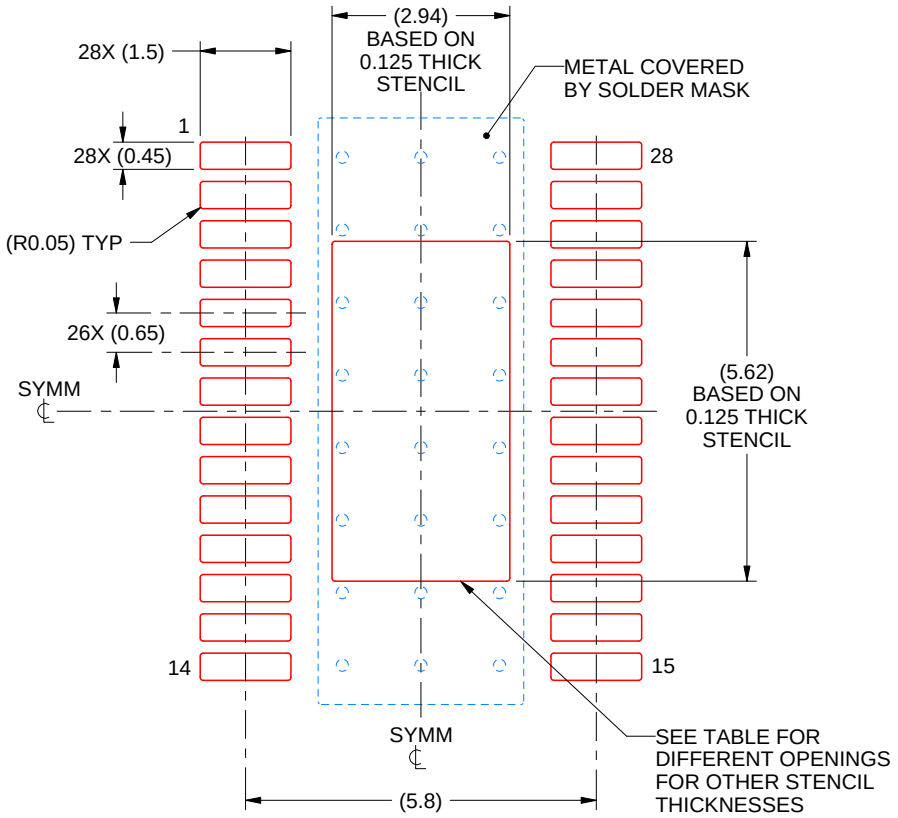
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.29 X 6.28
0.125	2.94 X 5.62 (SHOWN)
0.15	2.68 X 5.13
0.175	2.48 X 4.75

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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