

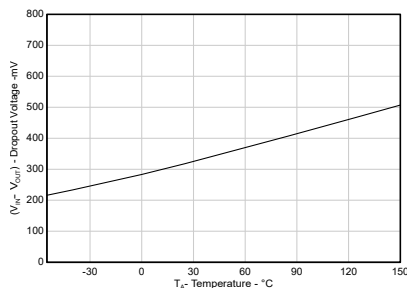
TPS7C84-Q1 車載用、150mA、40V、可変低ドロップアウトレギュレータ、パワーグッド付き

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
 - 温度グレード 1: $-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$ 、 T_A
 - 接合部温度: $-40^{\circ}\text{C} \sim +150^{\circ}\text{C}$ 、 T_J
- 幅広い入力電圧範囲:
 - V_{IN} 範囲: $2.1\text{V} \sim 40\text{V}$
- 広い出力電圧範囲 (V_{OUT}):
 - 固定オプション: 3.3V 、 5.0V
 - 可変オプション: $1.2\text{V} \sim 39\text{V}$
- 出力電流: 最大 150mA
- V_{OUT} 精度:
 - $\pm 1\%$ (ライン、負荷、温度の全範囲)
- 静止電流 (I_Q): $45\mu\text{A}$ (標準値)
- 低いドロップアウト: 350mV (標準値)
- オープンドレインのパワーグッド出力
- 出力電流制限とサーマルシャットダウン
- 幅広いセラミック出力コンデンサの値全体で安定:
 - C_{OUT} 範囲: $1\mu\text{F} \sim 100\mu\text{F}$
 - ESR 範囲: $0\Omega \sim 2\Omega$
- パッケージオプション:
 - D (8ピン SOIC)
 - DRB (8ピン VSON)

2 アプリケーション

- トラクション インバータ
- 車体制御モジュール (BCM)
- オンボードチャージャ
- テレマティクス制御



ドロップアウト電圧 vs 温度

3 概要

TPS7C84-Q1 は入力範囲の広い低ドロップアウトのレギュレータ (LDO) で、 $2.1\text{V} \sim 40\text{V}$ の入力電圧範囲と、最大 150mA の負荷電流に対応しています。TPS7C84-Q1 には、固定と可変の出力タイプがあります。固定出力オプションには、 3.3V と 5V があります。可変デバイスを使用し、出力を $1.2\text{V} \sim 39\text{V}$ の範囲で設定できます。

このデバイスは、フィードバック ピンの電圧を監視して出力電圧のステータスを表示するパワーグッド (PG) 出力を備えています。EN 入力および PG 出力を使用して、システムの複数の電源をシーケンシングできます。

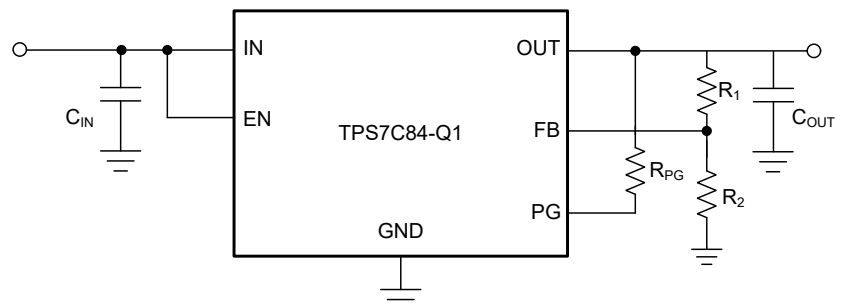
TPS7C84-Q1 は、最大 40V の V_{IN} バッテリー接続アプリケーション向けに設計されています。出力電圧範囲が広いため、MCU やプロセッサに電力を供給するだけでなく、シリコン カーバイド (SiC) ゲートドライバやマイクのバイアス電圧を生成することもできます。

このデバイスは、SOIC パッケージとコンパクトな PCB (プリント基板) 設計に適したウェットプル フランク付き小型 VSON パッケージで供給されます。熱抵抗が低いいため、デバイス全体で大きな発熱があっても持続して動作できます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ (2)
TPS7C84-Q1	D (SOIC, 8)	4.9mm × 6mm
	DRB (VSON, 8)	3mm × 3mm

- 詳細については、「[メカニカル、パッケージ、および注文情報](#)」を参照してください。
- パッケージ サイズ (長さ × 幅) は公称値で、該当する場合はピンも含まれます。



代表的なアプリケーション回路



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4 Pin Configuration and Functions

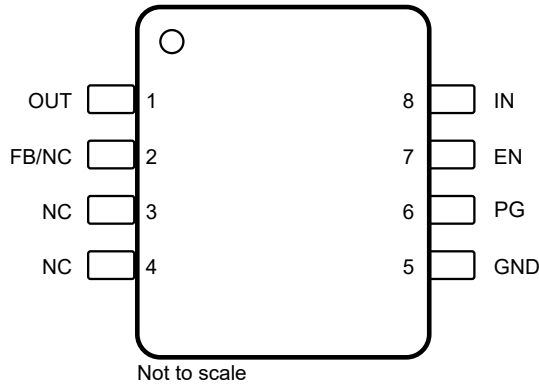


図 4-1. D Package, 8-Pin SOIC (Top View)

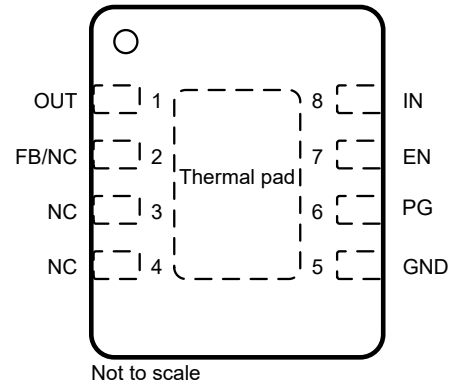


図 4-2. DRB Package, 8-Pin VSON (Top View)

表 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
EN	7	I	Enable pin. The device is disabled when the enable pin becomes lower than the enable logic input low level (V_{IL}). To make sure the device is enabled, drive the EN pin above the logic high level (V_{IH}). Do not leave this pin floating because this pin is high impedance. If this pin is left floating, the pin state becomes undefined and the device potentially enables or disables.
FB/NC	2	I	This pin is a feedback pin when using an external resistor divider or an NC pin when using the device with a fixed output voltage. When using the adjustable device, connect this pin through a resistor divider to the output for the device to function. See the Feedback Resistor Selection section for more information. If using a fixed output, leave this pin floating or connected to GND.
GND	5	—	Ground
IN	8	I	Input power-supply voltage pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground. See the Recommended Operating Conditions table and the Input and Output Capacitor Requirements section. Place the input capacitor as close to the input of the device as possible.
NC	3, 4	—	No internal connection. Leave this pin floating or tied to GND for best thermal performance.
OUT	1	O	Regulated output voltage pin. A capacitor is required from OUT to GND for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from OUT to GND. Place the output capacitor as close to the device output as possible. See the Input and Output Capacitor Requirements section for more details.
PG	6	O	Active-high, open-drain power-good output. This pin goes low when V_{OUT} drops by 6% of the nominal value.

(1) I = input; O = output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
IN	Continuous input voltage	-0.3	42	V
OUT	Output voltage	-0.3	VIN+0.3 ⁽³⁾	
EN	EN input voltage	-0.3	42	
PG	PG comparator output voltage ⁽²⁾	-0.3	42	
FB	FEEDBACK input voltage	-0.3	5	
T _{stg}	Storage temperature	-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime
- (2) Can exceed input supply voltage.
- (3) The absolute maximum rating is VIN + 0.3V or 42V, whichever is smaller.

5.2 ESD Ratings

			VALUE	UNIT	
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾	±2500	V	
		Charged-device model (CDM), per AEC V Q100-011	All pins		±1000
			Corner pins		±1000

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{IN}	Input voltage	2.1		40	V
V _{EN}	Enable voltage	0		40	V
V _{OUT}	Output voltage	1.2		39	V
I _{OUT}	Output current	0		150	mA
C _{OUT}	Output capacitor ⁽¹⁾	1	2.2	100	μF
C _{OUT ESR}	Output capacitor ESR	0		2	Ω
C _{IN}	Input capacitor		1		μF
C _{FF}	Feed-forward capacitor (optional ⁽²⁾ , for adjustable device only)		10		pF
I _{FB_DIVIDER}	Feedback divider current ⁽²⁾ (adjustable device only)	12			μA
T _J	Junction temperature	-40		150	°C

- (1) Effective output capacitance of 0.5μF minimum required for stability.
 (2) C_{FF} required for stability if the feedback divider current < 12μA. Feedback divider current = V_{OUT} / (R₁ + R₂). See the *Feed-Forward Capacitor (C_{FF})* section for details.

5.4 Thermal Information

THERMAL METRIC ^{(1) (2)}		D	UNIT
		8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	123	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	67.8	°C/W
R _{θJB}	Junction-to-board thermal resistance	70.7	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	18.0	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	69.8	°C/W

- (1) The thermal data is based on the JEDEC standard high K profile, JESD 51-7. Two-signal, two-plane, four-layer board with 2-oz. copper. The copper pad is soldered to the thermal land pattern. Also, correct attachment procedure must be incorporated.
 (2) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.5 Electrical Characteristics

specified at T_J = -40°C to +150°C, at V_{IN} = V_{OUT} (nominal) + 1V, I_{OUT} = 100 μA, C_{OUT} = 2.2μF, V_{EN} ≥ 2V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V _{OUT}	Output voltage accuracy	V _{IN} = [V _{OUT(NOM)} + 1V] to 40V, I _{OUT} = 100μA to 150mA	T _J = 25°C	-0.5		0.5	%
			T _J = -40°C to 150°C	-1		1	
ΔV _{OUT(ΔV_{IN})}	Line regulation	V _{IN} = [V _{OUT(NOM)} + 1V] to 40V	T _J = -40°C to 150°C	0.000	4	0.01	%/V
ΔV _{OUT(ΔI_{OUT})}	Load regulation	I _{OUT} = 100 μA to 150mA	T _J = -40°C to 150°C	0.02		0.2	%
V _{FB}	Feedback voltage	Reference voltage for FB	T _J = -40°C to 150°C	-1		1	%
I _{FB}	FEEDBACK bias current		T _J = 25°C		2	10	nA
			T _J = -40°C to 150°C			15	
V _{DO}	Dropout voltage adjustable output	V _{IN} = 3.5V, I _{OUT} = 150mA	T _J = -40°C to 150°C		350	660	mV
	Dropout voltage fixed 3.3V output	V _{IN} = V _{OUT} (nominal) = 3.3V, I _{OUT} = 150mA				670	
	Dropout voltage fixed 5V output	V _{IN} = V _{OUT} (nominal) = 5V, I _{OUT} = 150mA				580	

5.5 Electrical Characteristics (続き)

specified at $T_J = -40^\circ\text{C}$ to $+150^\circ\text{C}$, at $V_{IN} = V_{OUT}$ (nominal) + 1V, $I_{OUT} = 100\ \mu\text{A}$, $C_{OUT} = 2.2\ \mu\text{F}$, $V_{EN} \geq 2\text{V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_Q	Quiescent current	$I_{OUT} = 0$	$T_J = -40^\circ\text{C}$ to 150°C			56	μA
		$I_{OUT} = 100\ \mu\text{A}$			45	68	
		$I_{OUT} = 150\text{mA}$				1.15	mA
UVLO	UVLO V_{IN} rising	$I_{OUT} = 100\ \mu\text{A}$	$T_J = -40^\circ\text{C}$ to 150°C	1.8	1.9	2.0	V
	UVLO V_{IN} falling			1.7	1.8	1.9	
	Hysteresis					100	mV
V_{IL}	Enable logic input low level	Low (regulator OFF)				0.7	V
V_{IH}	Enable logic input high level	High (regulator ON)	$T_J = -40^\circ\text{C}$ to 150°C	1.9			
I_{EN}	EN pin current	$V_{EN} = 40\text{V}$	$T_J = -40^\circ\text{C}$ to 150°C			0.8	μA
I_{CL}	Current limit	$V_{IN} \geq 3\text{V}$, $V_{OUT} = 0\text{V}$	$T_J = -40^\circ\text{C}$ to 150°C	165	235	280	mA
V_n	Output noise (RMS), 10Hz to 100KHz	$C_{OUT} = 1\ \mu\text{F}$	$T_J = 25^\circ\text{C}$		265		μV_{rms}
PSRR	Power supply ripple rejection	$V_{IN} - V_{OUT} = 1\text{V}$, frequency = 100Hz, $I_{OUT} = 5\text{mA}$	$T_J = 25^\circ\text{C}$		80		dB
$V_{PG(OL)}$	PG pin low level output voltage	$V_{IN} \geq 2\text{V}$, $I_{OL} = 400\ \mu\text{A}$	$T_J = 25^\circ\text{C}$		180	230	mV
			$T_J = -40^\circ\text{C}$ to 150°C			280	
$V_{PG(TH,RISING)}$	V_{OUT} rising		$T_J = -40^\circ\text{C}$ to 150°C			97	% V_{OUT}
$V_{PG(TH,FALLING)}$	V_{OUT} falling			92			
$V_{PG(HYST)}$	Hysteresis		$T_J = 25^\circ\text{C}$		2		
$I_{SHUTDOWN}$	Shutdown supply current (I_{GND})	$V_{EN} \leq 0.7\text{V}$, $V_{IN} \leq 40\text{V}$, $V_{OUT} = 0\text{V}$	$T_J = 25^\circ\text{C}$		3	4.5	μA
			$T_J = -40^\circ\text{C}$ to 150°C			6	
$T_{SD(SHUTDOWN)}$	Junction shutdown temperature				177		$^\circ\text{C}$
$T_{SD(HYST)}$	Hysteresis of thermal shutdown				15		$^\circ\text{C}$

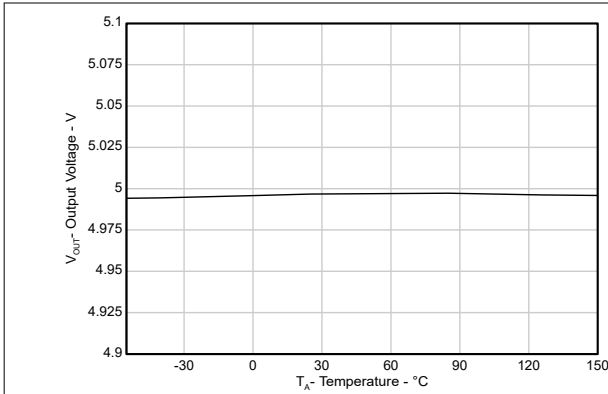
5.6 Timing Requirements

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PGDH}	PG delay time rising, time from 92% V_{OUT} to 20% of PG ⁽¹⁾	25	50	65	μs
t_{PGDL}	PG delay time falling, time from 90% V_{OUT} to 80% of PG ⁽¹⁾	6	13	18	μs

(1) Output Overdrive = 10%

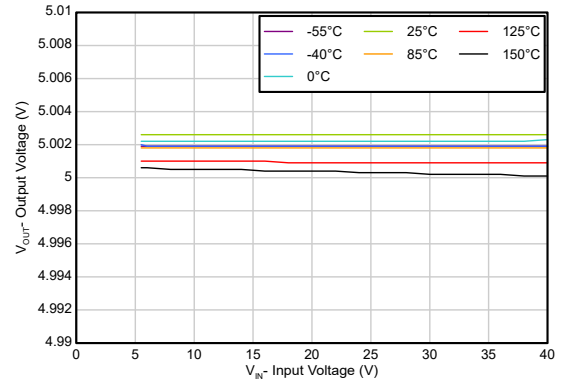
5.7 Typical Characteristics

at $V_{IN} = V_{OUT} (\text{nominal}) + 1V$, $I_{OUT} = 100\mu A$, $C_{OUT} = 2.2\mu F$, and $V_{EN} \geq 2V$ (unless otherwise noted)



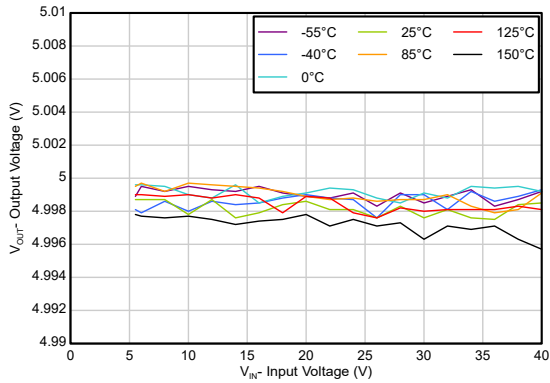
$V_{IN} = 6V$, $V_{OUT} = 5V$, $I_{OUT} = 150mA$

5-1. Output Voltage vs Temperature



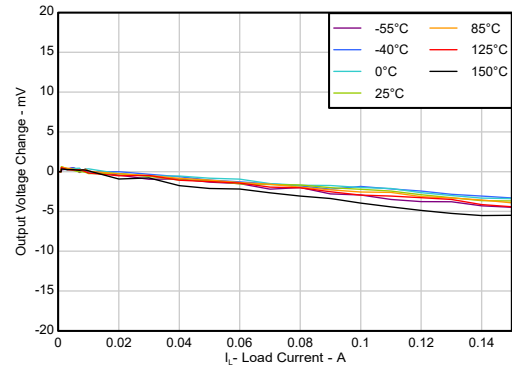
$V_{OUT} = 5V$, $I_{OUT} = 100\mu A$

5-2. Line Regulation vs Input Voltage



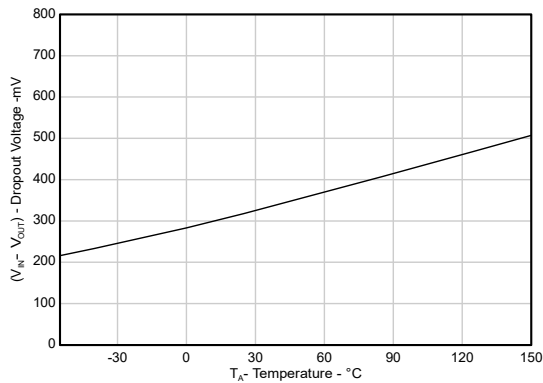
$V_{OUT} = 5V$, $I_{OUT} = 150mA$

5-3. Line Regulation vs Input Voltage



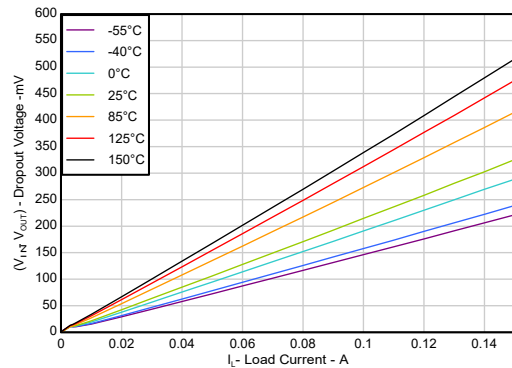
$V_{IN} = 6V$, $V_{OUT} = 5V$

5-4. Load Regulation vs Load Current



$V_{IN} = 4.9V$, $I_{OUT} = 150mA$

5-5. Dropout Voltage vs Temperature

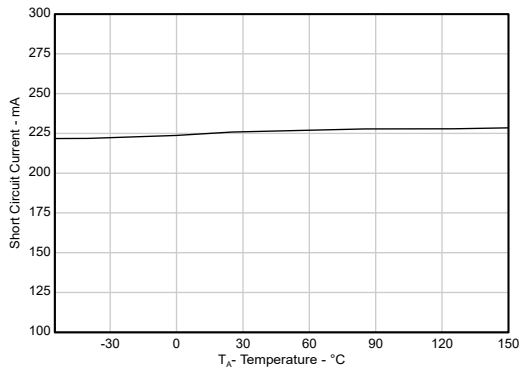


$V_{IN} = 4.9V$

5-6. Dropout Voltage vs Output Current

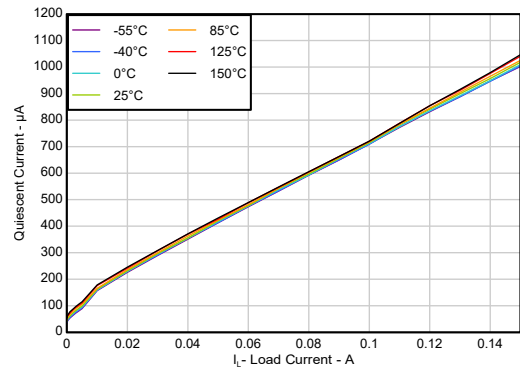
5.7 Typical Characteristics (continued)

at $V_{IN} = V_{OUT} (\text{nominal}) + 1V$, $I_{OUT} = 100\mu A$, $C_{OUT} = 2.2\mu F$, and $V_{EN} \geq 2V$ (unless otherwise noted)



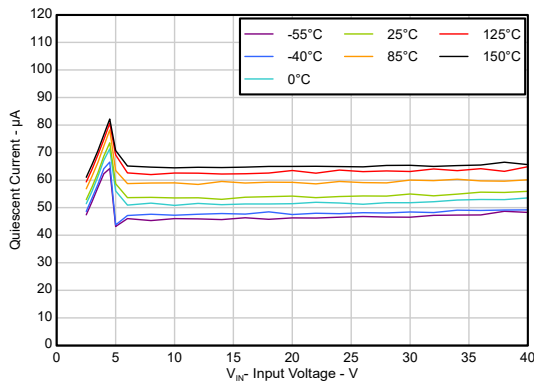
$V_{IN} = 6V, V_{OUT} = 0V$

5-7. Short-Circuit Current vs Temperature



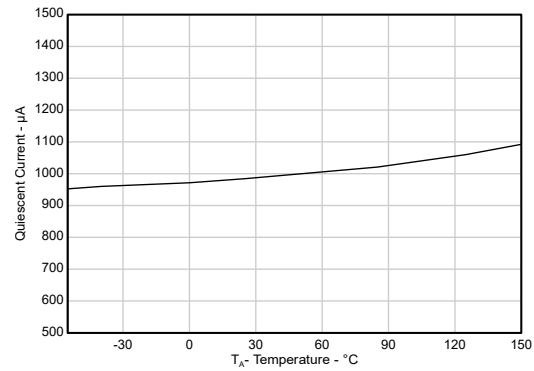
$V_{IN} = 6V, V_{OUT} = 5V$

5-8. Quiescent Current vs Load Current



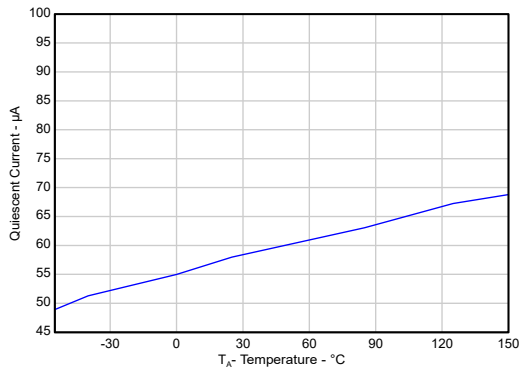
$V_{OUT} = 5V$

5-9. Quiescent Current vs Input Voltage ($I_{OUT} = 0mA$)



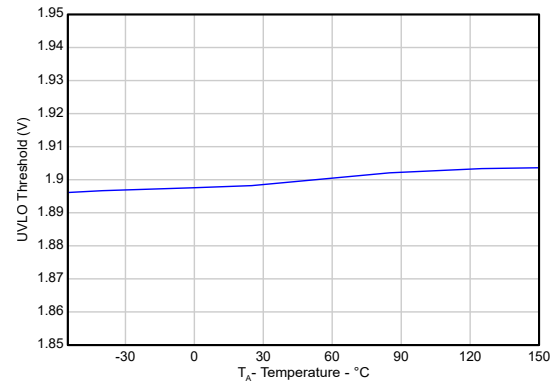
$V_{IN} = 6V, V_{OUT} = 5V$

5-10. Quiescent Current vs Temperature ($I_{OUT} = 150mA$)



$V_{IN} = 6V, V_{OUT} = 5V$

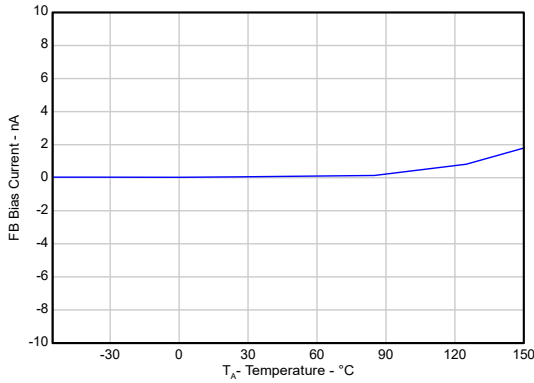
5-11. Quiescent Current vs Temperature ($I_{OUT} = 100\mu A$)



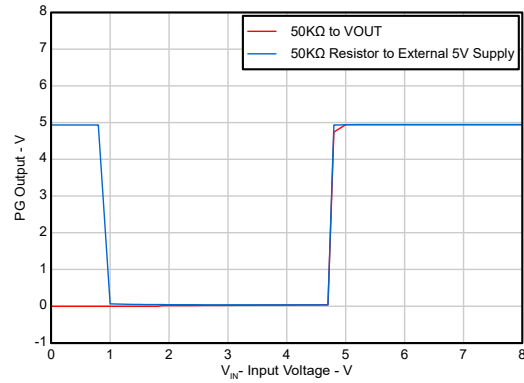
5-12. Undervoltage Lockout (UVLO) Threshold vs Temperature

5.7 Typical Characteristics (continued)

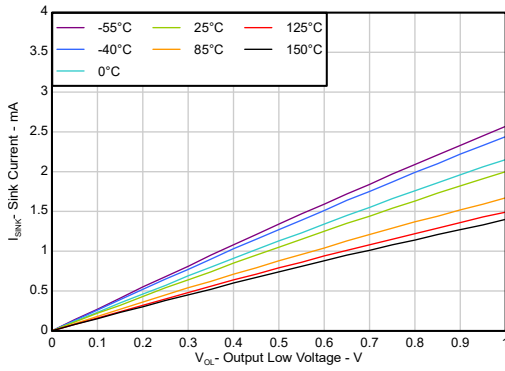
at $V_{IN} = V_{OUT} (\text{nominal}) + 1V$, $I_{OUT} = 100\mu A$, $C_{OUT} = 2.2\mu F$, and $V_{EN} \geq 2V$ (unless otherwise noted)



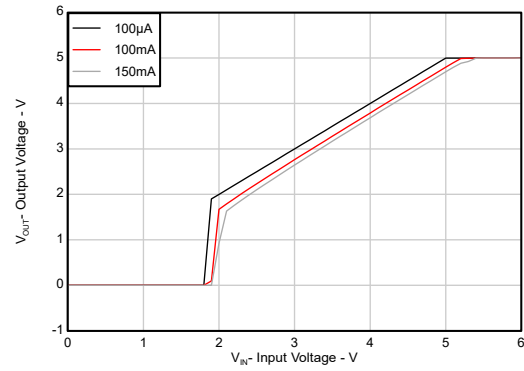
5-13. FB Bias Current vs Temperature



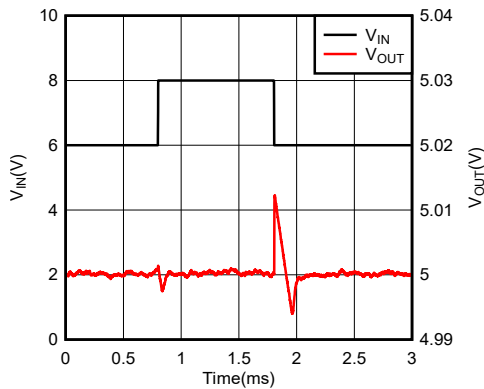
5-14. PG Comparator Output vs Input Voltage



5-15. PG Comparator Sink Current vs Output Low Voltage

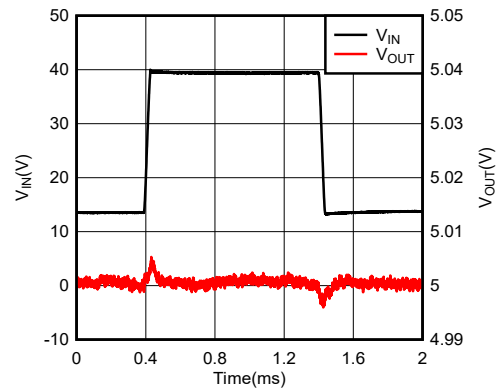


5-16. Output Voltage vs Input Voltage



$V_{IN} = 6V \text{ to } 8V$, slew rate = $1V/\mu s$, $V_{OUT} = 5V$, $C_{OUT} = 1\mu F$, $I_{OUT} = 100\mu A$

5-17. Line Transient Response vs Time



$V_{IN} = 13.5V \text{ to } 40V$, slew rate = $1V/\mu s$, $V_{OUT} = 5V$, $C_{OUT} = 1\mu F$, $I_{OUT} = 1mA$

5-18. Line Transient Response vs Time

5.7 Typical Characteristics (continued)

at $V_{IN} = V_{OUT} (\text{nominal}) + 1V$, $I_{OUT} = 100\mu A$, $C_{OUT} = 2.2\mu F$, and $V_{EN} \geq 2V$ (unless otherwise noted)

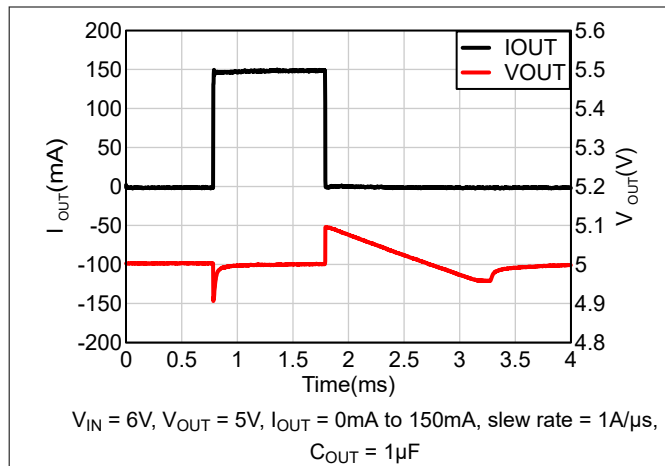


Figure 5-19. Load Transient Response vs Time

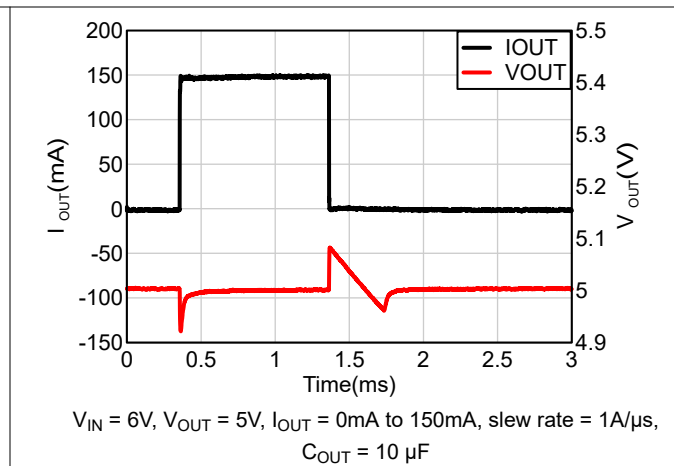


Figure 5-20. Load Transient Response vs Time

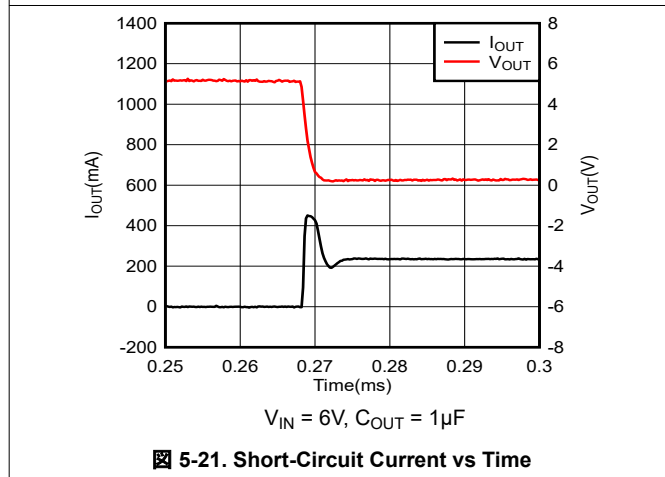


Figure 5-21. Short-Circuit Current vs Time

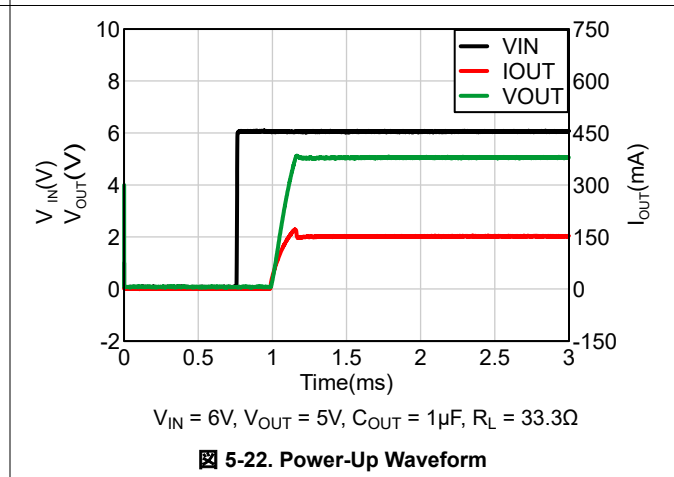


Figure 5-22. Power-Up Waveform

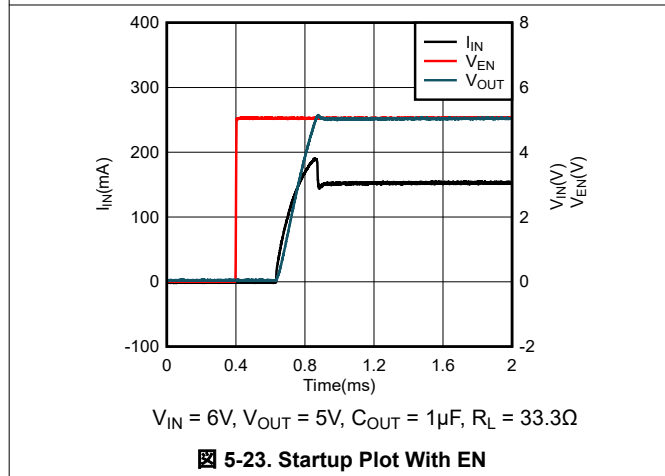


Figure 5-23. Startup Plot With EN

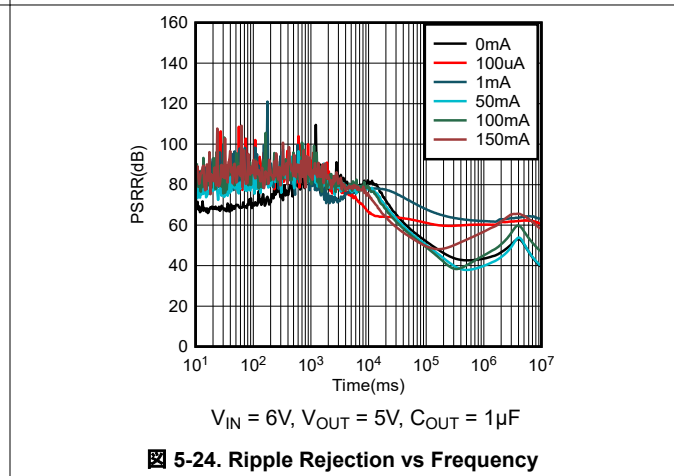
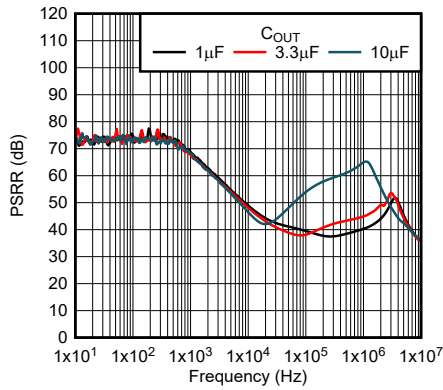


Figure 5-24. Ripple Rejection vs Frequency

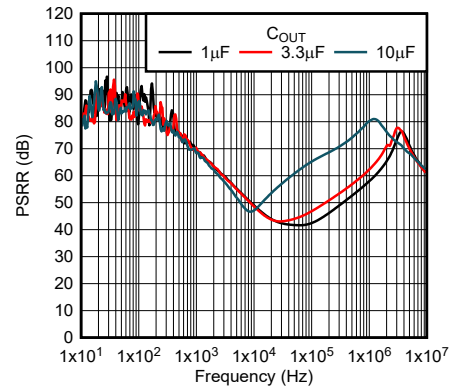
5.7 Typical Characteristics (continued)

at $V_{IN} = V_{OUT} (\text{nominal}) + 1V$, $I_{OUT} = 100\mu A$, $C_{OUT} = 2.2\mu F$, and $V_{EN} \geq 2V$ (unless otherwise noted)



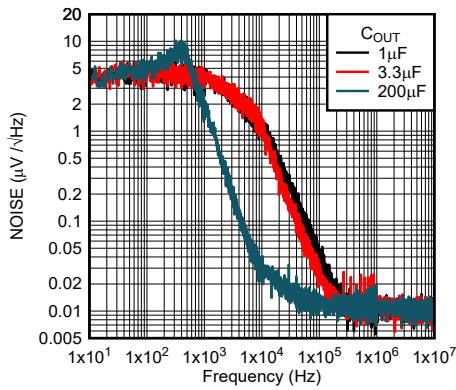
$V_{IN} = 6V, V_{OUT} = 5V, I_{OUT} = 100mA$

5-25. Ripple Rejection vs Frequency



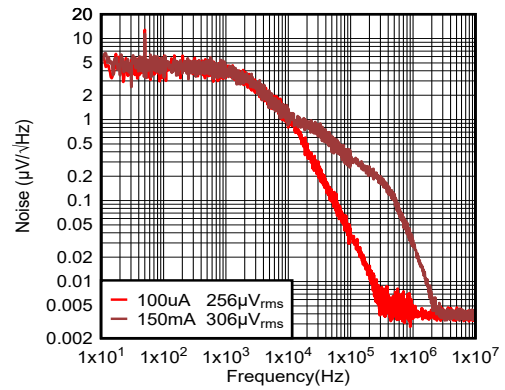
$V_{IN} = 6V, V_{OUT} = 5V, I_{OUT} = 1mA$

5-26. Ripple Rejection vs Frequency



$V_{IN} = 6V, V_{OUT} = 5V, I_{OUT} = 100\mu A$

5-27. Output Noise vs Frequency



$V_{IN} = 6V, V_{OUT} = 5V, C_{OUT} = 1\mu F$

5-28. Output Noise vs Frequency

6 Detailed Description

6.1 Overview

The TPS7C84-Q1 is a low-dropout linear regulator (LDO) designed to connect to the battery in automotive applications. The device accommodates a wide input supply voltage range up to 40V. The TPS7C84-Q1 is available in 3.3V and 5V fixed output voltages. Alternatively, by connecting the FB pin to an external resistor divider, the output is able to be set to any value between 1.2V to 39V.

The TPS7C84-Q1 has a power-good output (PG) that monitors the voltage at the feedback pin to indicate the status of the output voltage. The EN input and PG output are used for sequencing multiple power supplies in the system. The TPS7C84-Q1 is stable with small ceramic output capacitors, allowing for a small overall solution size. This device has an output tolerance of 1% across line, load, and temperature variation and is capable of delivering 150mA of continuous load current. This device includes integrated thermal shutdown, current limit, and undervoltage lockout (UVLO) features. This device delivers excellent line and load transient performance. The operating junction temperature range of the device is from -40°C to $+150^{\circ}\text{C}$.

6.2 Functional Block Diagrams

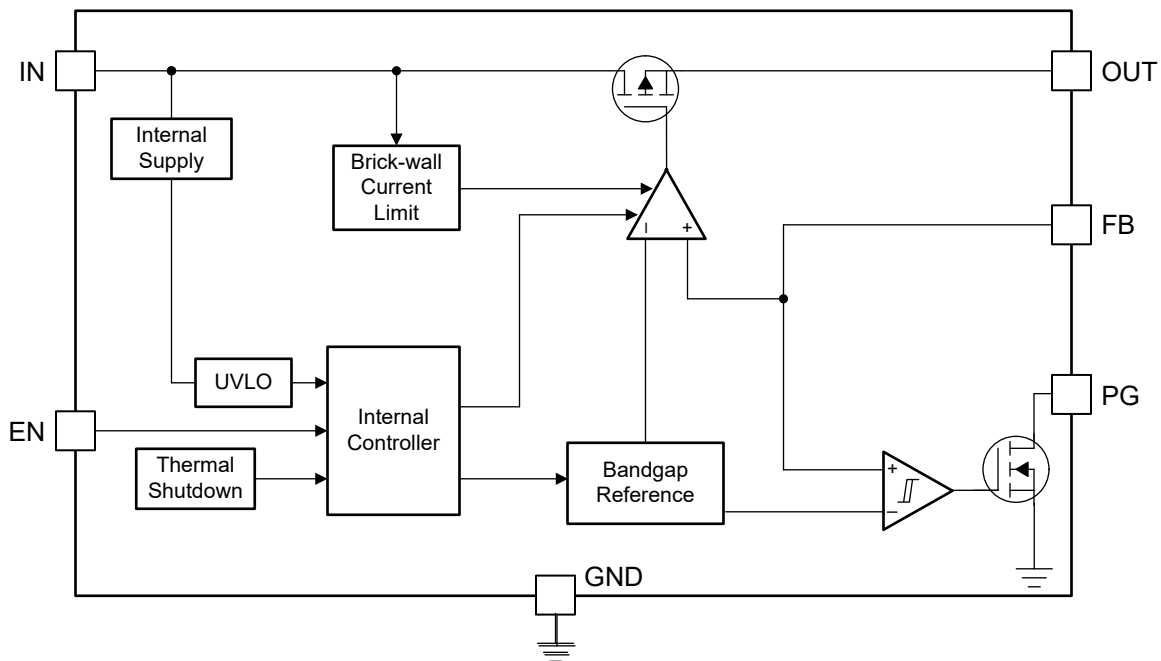


图 6-1. Adjustable Output Block Diagram

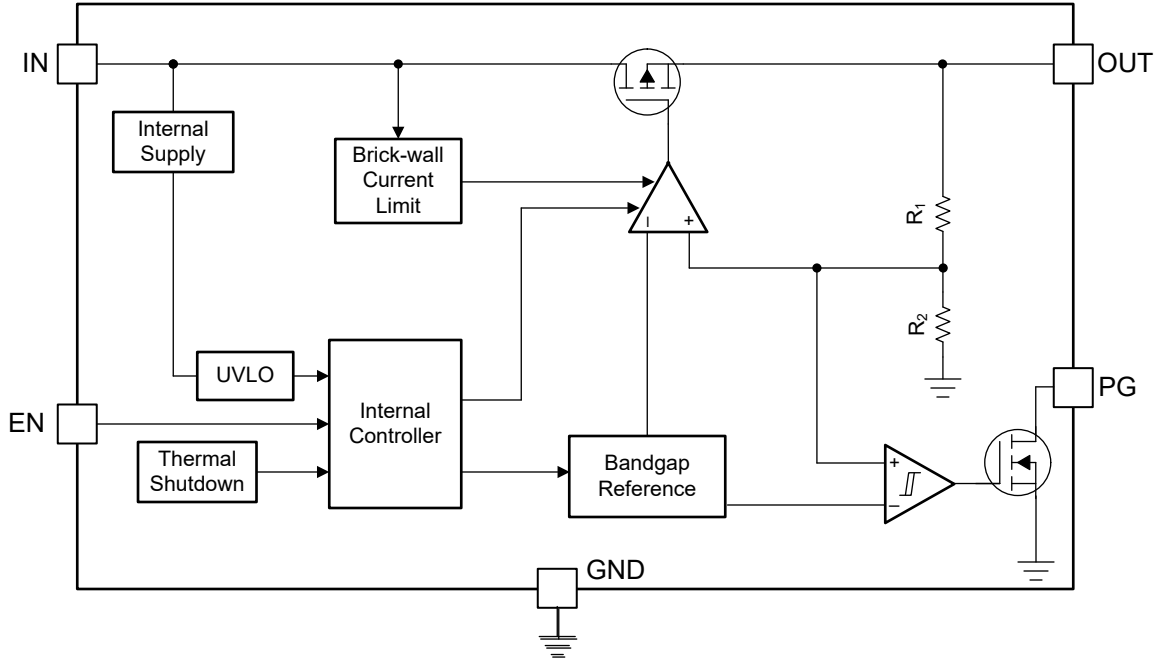


図 6-2. Fixed Output Block Diagram

6.3 Feature Description

6.3.1 Output Enable

The EN pin for the device is an active-high pin. The output voltage is enabled when the EN pin voltage is greater than the high-level input voltage of the EN pin. Conversely, the output voltage is disabled when the EN pin voltage is less than the low-level input voltage of the EN pin. If independent control of the output voltage is not needed, connect the EN pin to the device input voltage.

6.3.2 Dropout Voltage

Dropout voltage (V_{DO}) is defined as $V_{IN} - V_{OUT}$ at the rated output current (I_{RATED}), where the pass transistor is fully on. V_{IN} is the input voltage, V_{OUT} is the output voltage, and I_{RATED} is the maximum I_{OUT} listed in the [Recommended Operating Conditions](#) table. At this operating point, the pass transistor is driven fully on. Dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage where the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source, on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

6.3.3 Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a brick-wall scheme. In a high-load current fault, the brick-wall scheme limits the output current to the current limit (I_{CL}). I_{CL} is listed in the [Electrical Characteristics](#) table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power $[(V_{IN} - V_{OUT}) \times I_{CL}]$. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the [Know Your Limits application note](#).

Figure 6-3 shows a diagram of the current limit.

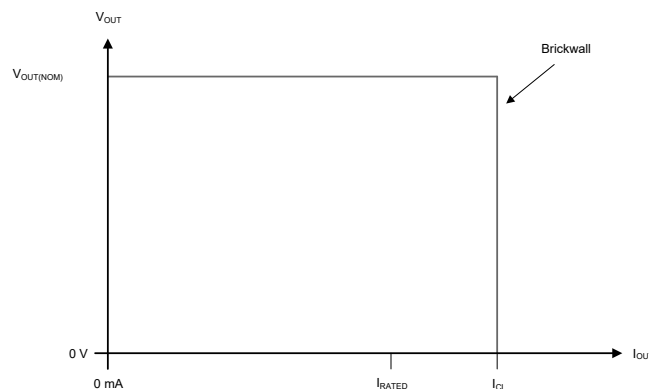


Figure 6-3. Current Limit

6.3.4 Undervoltage Lockout (UVLO)

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage. This circuit allows for a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the [Electrical Characteristics](#) table.

6.3.5 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(\text{shutdown})}$ (typical). Thermal shutdown hysteresis makes sure that the device resets (turns on) when the temperature falls to $T_{SD(\text{reset})}$ (typical).

The thermal time-constant of the semiconductor die is fairly short. Thus the device cycles on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start-up is high from large $V_{IN} - V_{OUT}$ voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start-up completes.

For reliable operation, limit the junction temperature to the maximum listed in the [Recommended Operating Conditions](#) table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the device internal protection circuitry is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

6.4 Device Functional Modes

6.4.1 Shutdown Mode

Place this device in shutdown mode with a logic low at the EN pin. Return the logic level high to restore operation or tie EN to V_{IN} if this mode is not used.

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Reverse Current

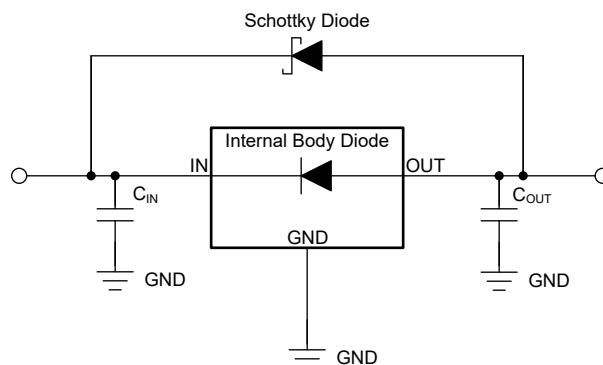
Excessive reverse current potentially damages this device. Reverse current flows through the intrinsic body diode of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current occur are outlined in this section, all of which potentially exceed the absolute maximum rating of $V_{OUT} \leq V_{IN} + 0.3V$.

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, use external protection to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated.

☒ 7-1 shows one approach for protecting the device.



☒ 7-1. Example Circuit for Reverse Current Protection Using a Schottky Diode

7.1.2 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source impedance is more than 0.5Ω . Use a higher value capacitor if large, fast rise-time load or line transients are anticipated. Additionally, use a higher-value capacitor if the device is located several inches from the input power source.

Dynamic performance of the device is improved by using an output capacitor. Use an output capacitor within the range specified in the [Recommended Operating Conditions](#) table for stability.

7.1.3 Estimating Junction Temperature

The JEDEC standard now recommends using psi (Ψ) thermal metrics to estimate the linear regulator junction temperatures when in-circuit on a typical PCB board application. These metrics are not thermal resistance

parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The [Thermal Information](#) table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the printed circuit board (PCB) surface temperature 1mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \quad (2)$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \quad (3)$$

where:

- T_B is the PCB surface temperature measured 1mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use the metrics, see the [Semiconductor and IC Package Thermal Metrics application note](#).

7.1.4 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the PCB, and correct sizing of the thermal plane. Make sure the PCB area around the regulator has few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (4)$$

注

Power dissipation is minimized, and therefore greater efficiency achieved, by correct selection of the system voltage rails. For the lowest power dissipation, use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. Make sure this pad area contains an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. Power dissipation and junction temperature are most often related by the $R_{\theta JA}$ of the combined PCB and device package and the T_A . $R_{\theta JA}$ is the junction-to-ambient thermal resistance and T_A is the temperature of the ambient air. The following equation describes this relationship.

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (5)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design. This resistance therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the [Thermal Information](#) table is determined by the

JEDEC standard PCB and copper-spreading area. $R_{\theta JA}$ is used as a relative measure of package thermal performance.

7.2 Typical Application

Figure 7-2 shows a typical application circuit for the TPS7C84-Q1. Use different values of external components, depending on the end application. If needed, use a larger output capacitor during fast load steps to prevent a reset from occurring. Use a low-ESR ceramic capacitor with an X5R or X7R dielectric.

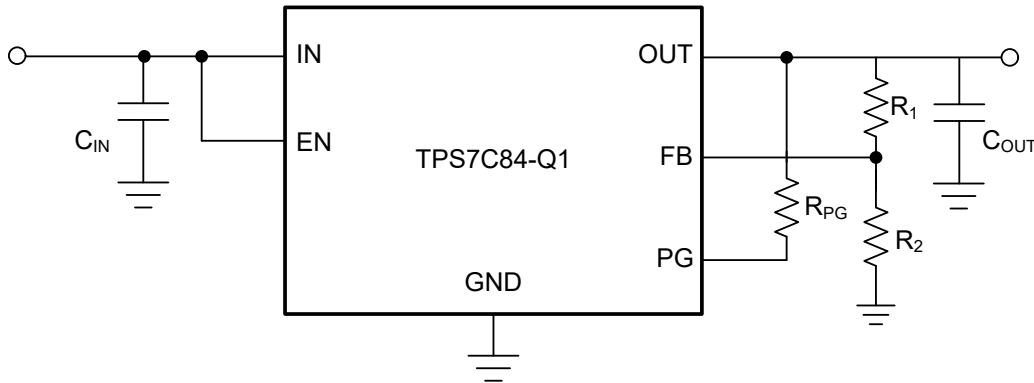


Figure 7-2. Typical Application Schematic for the TPS7C84-Q1

7.2.1 Design Requirements

Table 7-1 summarizes the design requirements for Figure 7-2.

Table 7-1. Design Parameters

PARAMETER	VALUE
Input voltage range	6V to 40V
Output voltage	5V
Output current	150mA
Output capacitor	1 μ F

7.2.1.1 Recommended Capacitor Types

7.2.1.1.1 Recommended Capacitors

The TPS7C84-Q1 requires an output capacitor of at least 1 μ F for stability and an equivalent series resistance (ESR) between 0 Ω and 2 Ω . Without the output capacitor, the regulator oscillates. For best transient performance, use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and ESR over temperature. When choosing a capacitor for a specific application, be mindful of the DC bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. For best performance, the maximum recommended output capacitor is 100 μ F. An input capacitor is not required for stability. However, good analog practice is to connect a capacitor (500nF or higher) between the GND and IN pins. Some input supplies have a high impedance, thus placing the input capacitor on the input supply helps reduce input impedance. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. If the input supply has high impedance over a large range of frequencies, use several input capacitors in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast rise-time load transients are anticipated, or if the device is located several inches from the input power source.

7.2.2 Detailed Design Procedure

7.2.2.1 Feedback Resistor Selection

V_{OUT} is set by the external feedback resistors R_1 and R_2 , according to the following equation:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) \quad (6)$$

In this equation, V_{FB} is the FB pin current error term. To ignore V_{FB} in this equation, set the feedback divider current to 100 times the FB pin current listed in the [Electrical Characteristics](#) table. This setting provides the maximum feedback divider series resistance, as shown in the following equation:

$$R_1 + R_2 \leq \frac{V_{OUT}}{(I_{FB} \times 100)} \quad (7)$$

7.2.2.2 Feedforward Capacitor

Connect a feedforward capacitor (C_{FF}) between the OUT pin and the FB pin. C_{FF} improves transient, noise, and PSRR performance. If a higher capacitance C_{FF} is used, the start-up time increases. For a detailed description of the C_{FF} tradeoffs, see the [Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator application note](#).

As shown in [Figure 7-3](#), poor layout practices and using long traces at the FB pin results in the formation of a parasitic capacitor (C_{FB}).

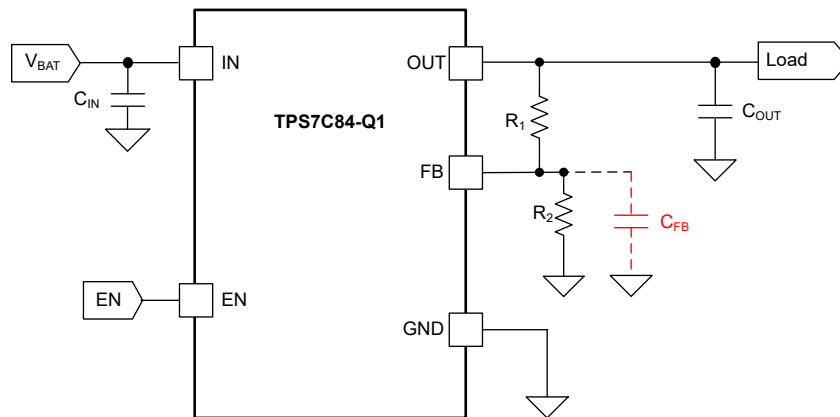


図 7-3. Formation of a Parasitic Capacitor at the FB Pin

C_{FB} , along with the feedback resistors R_1 and R_2 potentially results in the formation of an uncompensated pole in the transfer function of the loop gain. A C_{FB} value as small as 6pF potentially causes the parasitic pole frequency, given by [Equation 8](#), to fall within the LDO bandwidth and result in instability.

$$f_P = \frac{1}{(2 \times \pi \times C_{FB} \times (R_1 \parallel R_2))} \quad (8)$$

Adding a feedforward capacitor (C_{FF}) creates a zero in the loop gain transfer function that compensates for the parasitic pole created by C_{FB} . [Figure 7-4](#) shows this compensation. [Equation 9](#) and [Equation 10](#) calculate the pole and zero frequencies.

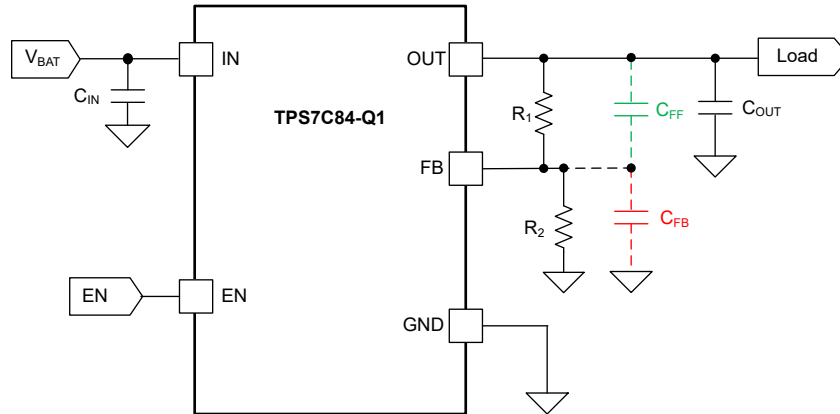


図 7-4. A Feedforward Capacitor Compensates the Effects of the Parasitic Capacitor

$$f_p = \frac{1}{(2 \times \pi \times (R_1 \parallel R_2) \times (C_{FF} + C_{FB}))} \tag{9}$$

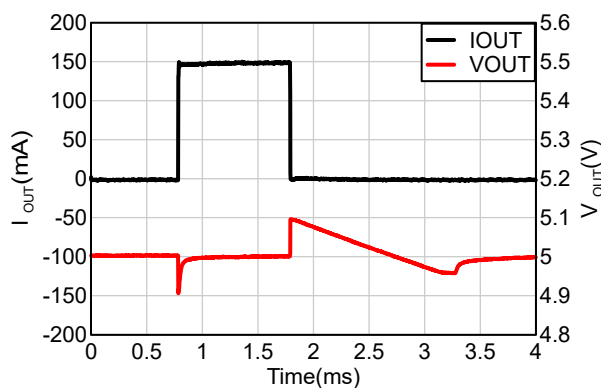
$$f_z = \frac{1}{(2 \times \pi \times C_{FF} \times R_1)} \tag{10}$$

The C_{FF} value that makes f_p equal to f_z depends on the values of C_{FB} and the feedback resistors used in the application. This C_{FF} value also results in a pole-zero cancellation. Alternatively, if the feedforward capacitor is selected so that $C_{FF} \gg C_{FB}$, then the pole and zero frequencies from 式 9 and 式 10 are related as:

$$\frac{f_p}{f_z} \cong \left(1 + \frac{R_1}{R_2}\right) = \frac{V_{OUT}}{V_{FB}} \tag{11}$$

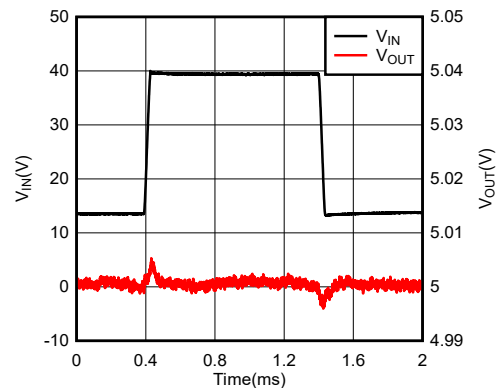
In most applications, particularly where a 3.3V or 5V V_{OUT} is generated, this ratio is not very large. Thus implying that the frequencies are located close to each other and therefore the parasitic pole is compensated. A C_{FF} value of approximately $100\text{pF} \leq C_{FF} \leq 10\text{nF}$ typically helps prevent instability caused by the parasitic capacitance on the feedback node. This C_{FF} range helps even for large V_{OUT} values, where this ratio is potentially as large as 20.

7.2.3 Application Curve



$V_{IN} = 6\text{V}$, $V_{OUT} = 5\text{V}$, $I_{OUT} = 0\text{mA}$ to 150mA , slew rate = $1\text{A}/\mu\text{s}$, $C_{OUT} = 1\mu\text{F}$

図 7-5. Load Transient Response vs Time



$V_{IN} = 13.5\text{V}$ to 40V , slew rate = $1\text{V}/\mu\text{s}$, $V_{OUT} = 5\text{V}$, $C_{OUT} = 1\mu\text{F}$, $I_{OUT} = 1\text{mA}$

図 7-6. Line Transient Response vs Time

7.3 Power Supply Recommendations

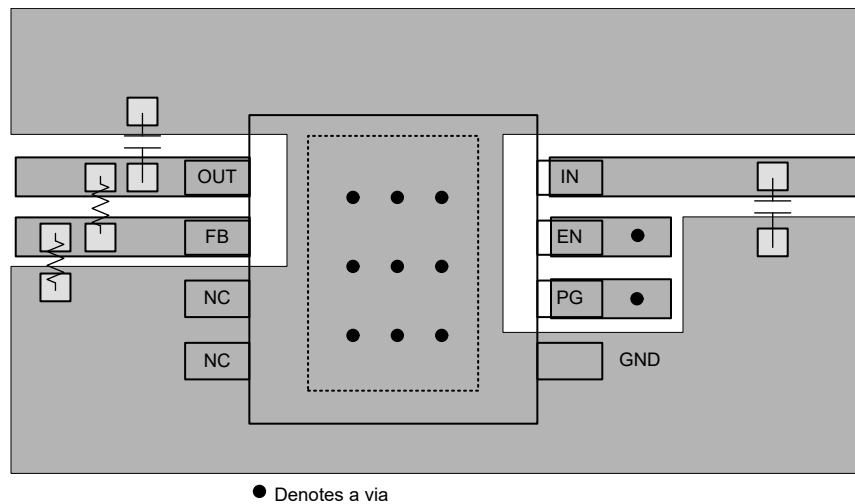
Limit maximum input voltage to 40V for proper operation. Place input and output capacitors as close to the device as possible to take advantage of the high-frequency, noise-filtering properties.

7.4 Layout

7.4.1 Layout Guidelines

- Verify that the traces on the input and outputs of the device are wide enough to handle the desired currents. For this device, use a larger output trace to accommodate the larger available current.
- Place input and output capacitors as close to the device as possible to take advantage of the high-frequency, noise-filtering properties.

7.4.2 Layout Example



☒ 7-7. SOIC (D) Package Adjustable Output

8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

表 8-1. Device Nomenclature

PRODUCT ⁽¹⁾	V _{OUT}
TPS7C84xxQ yyyzQ1	<p>xx is the nominal output voltage (for example, 50 = 5.0V, 33 = 3.3V). Q indicates that this device is a grade-1 device in accordance with the AEC-Q100 standard. yyy is the package designator. z is the reel quantity. Q1 indicates that this device is an automotive grade (AEC-Q100) device.</p>
TPS7C8401Q yyyzQ1	<p>01 indicates that this device is the adjustable option. Q indicates that this device is a grade-1 device in accordance with the AEC-Q100 standard yyy is the package designator. z is the reel quantity. Q1 indicates that this device is an automotive grade (AEC-Q100) device.</p>

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

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8.6 用語集

[テキサス・インスツルメンツ用語集](#)

この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (September 2024) to Revision A (December 2024)

Page

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新..... 1
- デバイスのステータスを「事前情報」から「量産」に変更 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS7C8401QDRQ1	ACTIVE	SOIC	D	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples
TPS7C8401QDRQ1	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C8401D	Samples
TPS7C8433QDRQ1	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C8433D	Samples
TPS7C8450QDRQ1	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C8450D	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7C8401QDRQ1	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS7C8433QDRQ1	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS7C8450QDRQ1	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7C8401QDRQ1	SOIC	D	8	3000	340.5	338.1	20.6
TPS7C8433QDRQ1	SOIC	D	8	3000	340.5	338.1	20.6
TPS7C8450QDRQ1	SOIC	D	8	3000	340.5	338.1	20.6



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



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NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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