TPS7H1101A-SP 1.5V～7V入力、3A、放射線強化型LDOレギュレータ

1 特長

- 5962R13202:
  - 放射線強度保証(RHA): 最大TID 100krad (Si)
  - 総照射線量耐性: 100krad (Si)
  - ELDRSフリー: 100krad (Si)
  - 線量率: 10mrad (Si)/s
  - 単一イベント・ラッチアップ(SEL)耐性:
    LET = 85 MeV-cm^2/mg
  - SEBおよびSEGR耐性:
    LET = 85 MeV-cm^2/mg
  - SET/SEFI開始スレッショルド > 40 MeV-cm^2/mg、詳細については「*放射線レポート*」(SNAA257)を参照
    - 下流の重要なコンポーネントの損傷を防止するため、常にLOWにアップセットするよう設計
  - SET/SEFIクロスセクション・プロット、詳細については「*放射線レポート*」(SNAA257)を参照
- **非常に低いV_{IN}範囲**: 1.5V～7V
- **最大出力電流** 3A
- **電流共有/並列動作により、最大6Aの出力電流を供給可能**
- **セラミック出力コンデンサで安定動作**
- **ライン、負荷、温度の範囲全体にわたって±2%の精度**
- **外付けのコンデンサによりソフトスタートをプログラム可能**
- **すべての入力電圧にわたる入力イネーブルとパワー・グッド出力によるパワー・シーケンス**
- **非常に低いドロップアウトLDO電圧**:
  1A (25℃)、V_{OUT} = 1.8Vにおいて62mV
- **低ノイズ**:
  V_{IN} = 2V、V_{OUT} = 1.8V、3A時に20.33μVRMS
- PSRR: 1kHzにおいて45dB超
- **非常に優れた負荷/ライン過渡応答**
- **フォールドバック電流制限**
- 「ツールとソフトウェア」タブを参照
- **熱的に強化されたCFPパッケージ(0.6℃/W $R_{\theta JC}$)**

2 アプリケーション

- **人工衛星のポイント・オブ・ロード電源**: FPGA、マイクロコントローラ、ASIC、データ・コンバータ用
- **人工衛星のペイロード**
- **RF、VCO、受信機、アンプ用の、放射線強化された低ノイズのリニア・レギュレータ電源**
- **クリーンなアナログ電源要件**
- **軍用温度範囲(-55℃～125℃)で利用可能**
- **エンジニアリング評価(/EM)サンプルを利用可能**(1)

3 概要

TPS7H1101A-SPはTPS7H1101-SPの改良版で、入力電圧範囲の全体にわたってイネーブル機能を使用できます。放射線強化されたLDOリニア・レギュレータであり、PMOSパス素子構成を使用します。1.5V～7Vの広い入力電圧範囲で動作し、非常に優れたPSRRを実現しています。TPS7H1101A-SPには、正確でプログラム可能、かつ非常に広い範囲で調整可能な、フォールドバック電流制限が実装されています。FPGA、DSP、マイクロコントローラの複雑な電力要件に対応するため、TPS7H1101A-SPにはイネーブル・オンおよびオフ機能、ソフトスタートのプログラム機能、電流共有機能、パワー・グッドのオープン・ドレイン出力が搭載されています。

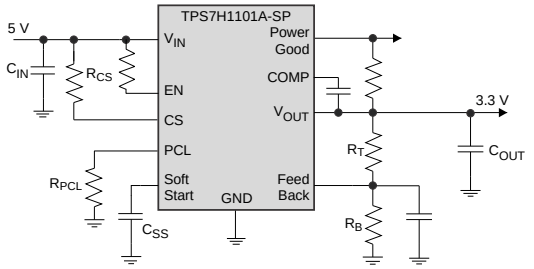
製品情報(2)

型番	パッケージ	本体サイズ(公称)
TPS7H1101A-SP	CFP (16)	11.00mm×9.60mm
	KGD	—

(1) これらのユニットは、技術的な評価のみを目的としています。標準とは異なるフロー(バーンインがないなど)に従って処理されており、25℃の温度定格のみがテストされれています。これらのユニットは、認定、量産、放射線テスト、航空での使用には適していません。これらの部品は、MILに規定されている温度範囲-55℃～125℃、または動作寿命全体にわたる性能を保証されていません。

(2) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

代表的なアプリケーション回路



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4 改訂履歴

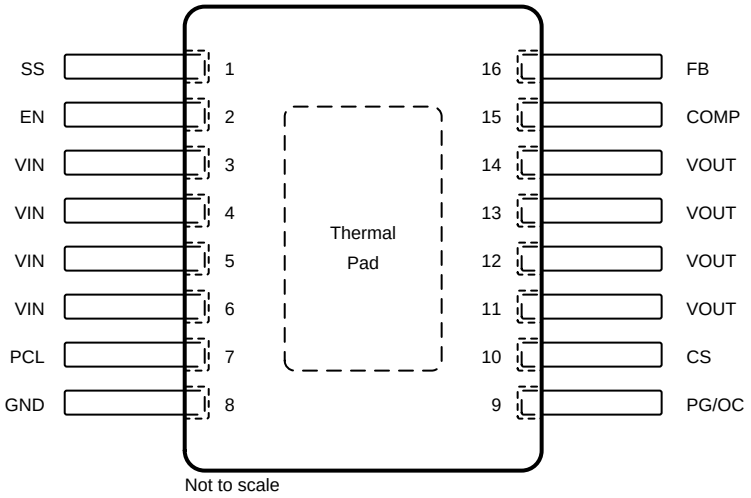
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2017年4月発行のものから更新 **Page**

- Added Bare Die Information table ... 4
- Added Bond Pad Coordinates in Microns table ... 5

5 Pin Configuration and Functions

HKR Package
16-Pin CFP
Bottom View



Not to scale

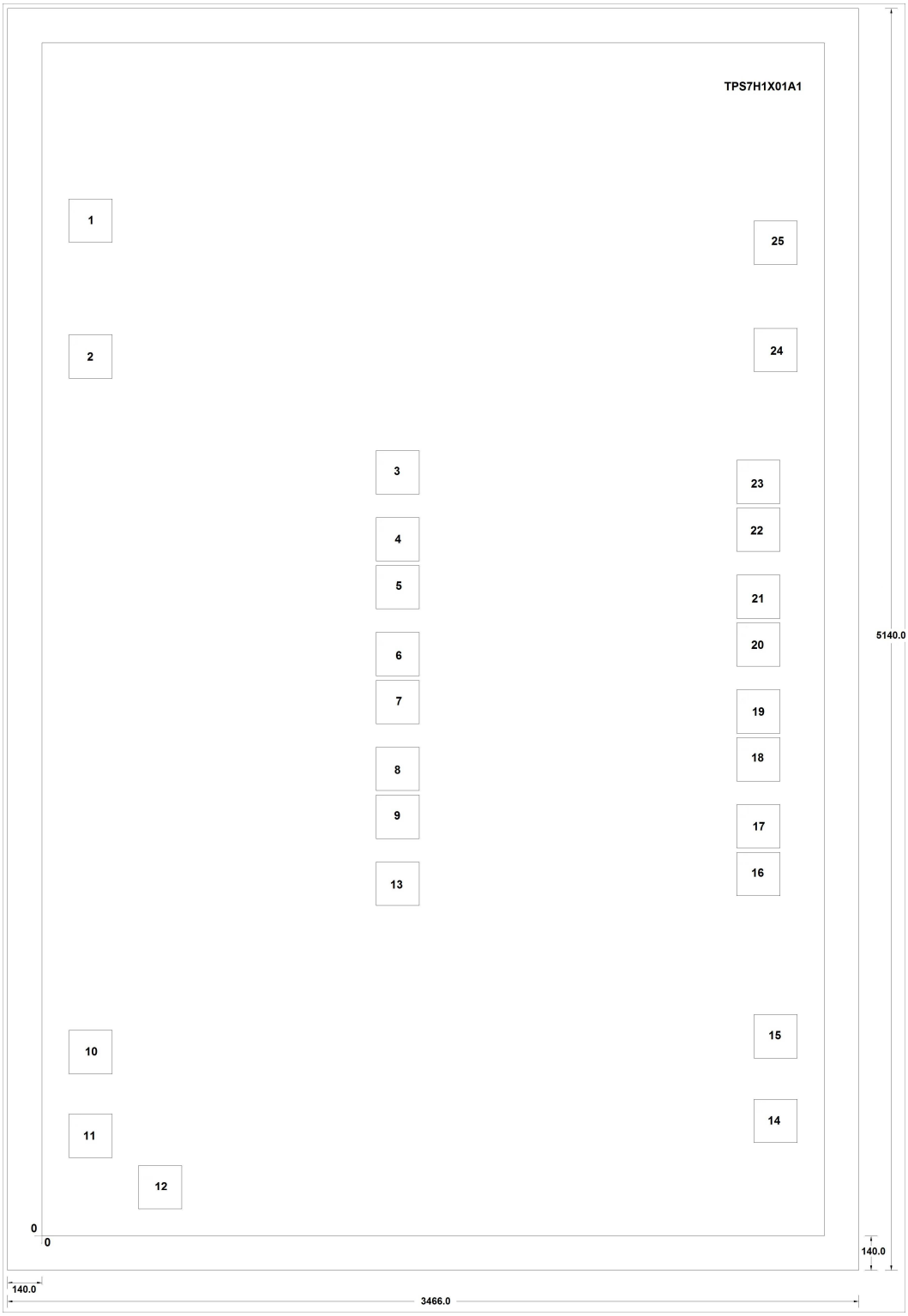
Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
SS	1	I/O	Soft-start terminal. Connecting an external capacitor slows down the output voltage ramp rate after enable event.
EN	2	I	Enable terminal. Driving this terminal to logic high enables the device; driving the terminal to logic low disables the device.
V_{IN}	3	I	Unregulated supply voltage. TI recommends to connect an input capacitor as a good analog circuit practice.
	4		
	5		
	6		
PCL	7	I/O	Programmable current limit. A resistor to GND sets the overcurrent limit activation point. The range of resistor that can be used on the PCL terminal to GND is 8.2 kΩ to 160 kΩ.
GND	8	—	Ground/thermal pad.(1)
PG/OC	9	O	Power Good terminal. PG is an open-drain output to indicate the output voltage reaches 90% of target. PG terminal is also used as indicator when an overcurrent condition is activated. PG pin should have a pull-up resistor to the V_{OUT} pin.
CS	10	I/O	Current sense terminal. Resistor connected from CS to V_{IN}. CS terminal indicates voltage proportional to output current. CS terminal low: Foldback current limit disabled. CS terminal high: Foldback current limit enabled.
V_{OUT}	11	O	Regulated output.
	12		
	13		
	14		
COMP	15	I/O	Internal compensation point for error amplifier.
FB	16	I	The output voltage feedback input through voltage dividers. See the *Adjustable Output Voltage (Feedback Circuit)* section.

(1) Thermal pad must be connected to GND.

Bare Die Information

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
15 mils	Silicon with backgrind	Ground	AlCu	30 kA



NOTE: All dimensions are in microns.

Bond Pad Coordinates in Microns

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
SS	1	109.89	4046.805	287.19	4224.105
EN	2	109.89	3493.35	287.19	3670.65
VIN	3	1359.99	3021.345	1537.29	3198.645
VIN	4	1359.99	2749.005	1537.29	2926.305
VIN	5	1359.99	2553.705	1537.29	2731.005
VIN	6	1359.99	2281.365	1537.29	2458.665
VIN	7	1359.99	2086.065	1537.29	2263.365
VIN	8	1359.99	1813.725	1537.29	1991.025
VIN	9	1359.99	1618.425	1537.29	1795.725
PCL	10	109.89	660.285	287.19	837.585
GND	11	109.89	319.455	287.19	496.755
GND	12	392.58	109.935	569.88	287.235
VIN	13	1359.99	1346.085	1537.29	1523.385
PG/OC	14	2898.945	379.62	3076.245	556.92
CS	15	2898.945	724.32	3076.245	901.62
VOUT	16	2829.105	1384.695	3006.405	1561.995
VOUT	17	2829.105	1579.815	3006.405	1757.115
VOUT	18	2829.105	1852.335	3006.405	2029.635
VOUT	19	2829.105	2047.455	3006.405	2224.755
VOUT	20	2829.105	2319.975	3006.405	2497.275
VOUT	21	2829.105	2515.095	3006.405	2692.395
VOUT	22	2829.105	2787.615	3006.405	2964.915
VOUT	23	2829.105	2982.735	3006.405	3160.035
COMP	24	2898.945	3519.72	3076.245	3697.02
FB	25	2898.945	3956.535	3076.245	4133.835

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	V_{IN}, PG	–0.3	7.5	V
	FB, COMP, PCL, CS, EN	–0.3	V_{IN} + 0.3	
Output voltage	V_{OUT}, SS	–0.3	7.5	V
PG terminal sink current		0.001	5	mA
Maximum operating junction temperature, T_J		–55	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_J	Operating junction temperature	–55		125	°C

6.4 Thermal Information

THERMAL METRIC(1)(2)		TPS7H1101A-SP HKR (CFP) 16 PINS	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.6	°C/W

(1) Do not allow package body temperature to exceed 265°C at any time or permanent damage may result.
(2) Maximum power dissipation may be limited by overcurrent protection.

6.5 Electrical Characteristics

1.5 V ≤ V_{IN} ≤ 7 V, $V_{OUT(target)}$ = V_{IN} – 0.35 V, I_{OUT} = 10 mA, V_{EN} = 1.1 V, C_{OUT} = 22 µF, PG terminal pulled up to V_{IN} with 50 kΩ, over operating temperature range (T_J = –55°C to 125°C), unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		1.5		7	V
V_{FB}	Feedback terminal voltage(1)	0 A ≤ I_{OUT} ≤ 3 A, 1.5 V ≤ V_{IN} ≤ 7 V	0.594	0.605	0.616	V
V_{OUT}	Output voltage range		0.8		V_{IN}	V
	Output voltage accuracy(1)	0 A ≤ I_{OUT} ≤ 3 A, 1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 0.8 V, 1.2 V, 1.8 V, 6.65 V	–2%		2%	
ΔV_{OUT}%/ ΔV_{IN}	Line regulation	1.5 V ≤ V_{IN} ≤ 7 V	–0.07	0.01	0.07	%/V
ΔV_{OUT}%/ ΔI_{OUT}	Load regulation	0.8 V ≤ V_{OUT} ≤ 6.65 V, 0 ≤ I_{Load} ≤ 3 A		0.08		%/A
ΔV_{OUT}	DC input line regulation	1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 0.8 V, 1.2 V, 1.8 V, I_{OUT} = 10 mA, T_J = –55°C(2)		0.5	3	mV
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 0.8 V, 1.2 V, 1.8 V, I_{OUT} = 10 mA, T_J = 25°C(2)		0.2	0.6	
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 0.8 V, 1.2 V, 1.8 V, I_{OUT} = 10 mA, T_J = 125°C(2)		0.2	1	

(1) The output voltage accuracy of condition at I_{OUT} = 2 A and I_{OUT} = 3 A is specified by characterization, but not production tested.
(2) Line and load regulations done under pulse condition for t < 10 ms.

Electrical Characteristics (continued)

1.5 V ≤ V_{IN} ≤ 7 V, $V_{OUT(target)}$ = V_{IN} – 0.35 V, I_{OUT} = 10 mA, V_{EN} = 1.1 V, C_{OUT} = 22 µF, PG terminal pulled up to V_{IN} with 50 kΩ, over operating temperature range (T_J = –55°C to 125°C), unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔV_O	DC output load regulation(3)	V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 1 A, T_J = –55°C(2)		0.4	1	mV
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 1 A, T_J = 25°C(2)		0.6	1.1	
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 1 A, T_J = 125°C(2)		0.8	1.3	
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 2 A, T_J = –55°C(2)		0.8	1.8	
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 2 A, T_J = 25°C(2)		1.3	1.8	
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 2 A, T_J = 125°C(2)		1.6	2.4	
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 3 A, T_J = –55°C(2)		1.1	1.9	
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 3 A, T_J = 25°C(2)		1.9	2.6	
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 3 A, T_J = 125°C(2)		2.5	3.4	
		V_{OUT} = 1.2 V, 0 ≤ I_{Load} ≤ 1 A, T_J = –55°C(2)		0.3	1.2	
		V_{OUT} = 1.2 V, 0 ≤ I_{Load} ≤ 1 A, T_J = 25°C(2)		0.5	1.3	
		V_{OUT} = 1.2 V, 0 ≤ I_{Load} ≤ 1 A, T_J = 125°C(2)		0.6	1.3	
		V_{OUT} = 1.2 V, 0 ≤ I_{Load} ≤ 2 A, T_J = –55°C(2)		0.8	1.6	
		V_{OUT} = 1.2 V, 0 ≤ I_{Load} ≤ 2 A, T_J = 25°C(2)		1.1	2.1	
		V_{OUT} = 1.2 V, 0 ≤ I_{Load} ≤ 2 A, T_J = 125°C(2)		1.5	2.1	
		V_{OUT} = 1.2 V, 0 ≤ I_{Load} ≤ 3 A, T_J = –55°C(2)		1	1.7	
		V_{OUT} = 1.2 V, 0 ≤ I_{Load} ≤ 3 A, T_J = 25°C(2)		1.1	2.4	
		V_{OUT} = 1.2 V, 0 ≤ I_{Load} ≤ 3 A, T_J = 125°C(2)		2.2	3.5	
		V_{OUT} = 1.8 V, 0 ≤ I_{Load} ≤ 1 A, T_J = –55°C(2)		0.1	0.9	
		V_{OUT} = 1.8 V, 0 ≤ I_{Load} ≤ 1 A, T_J = 25°C(2)		0.3	0.9	
		V_{OUT} = 1.8 V, 0 ≤ I_{Load} ≤ 1 A, T_J = 125°C(2)		0.4	1.2	
		V_{OUT} = 1.8 V, 0 ≤ I_{Load} ≤ 2 A, T_J = –55°C(2)		1.4	2.4	
		V_{OUT} = 1.8 V, 0 ≤ I_{Load} ≤ 2 A, T_J = 25°C(2)		0.7	1.4	
		V_{OUT} = 1.8 V, 0 ≤ I_{Load} ≤ 2 A, T_J = 125°C(2)		0.6	1.9	
		V_{OUT} = 1.8 V, 0 ≤ I_{Load} ≤ 3 A, T_J = –55°C(2)		2.5	3.9	
		V_{OUT} = 1.8 V, 0 ≤ I_{Load} ≤ 3 A, T_J = 25°C(2)		1.2	2.1	
		V_{OUT} = 1.8 V, 0 ≤ I_{Load} ≤ 3 A, T_J = 125°C(2)		1.2	2.5	
		V_{OUT} = 6.65 V, 0 ≤ I_{Load} ≤ 1 A, T_J = –55°C(2)		1.5	2.9	
		V_{OUT} = 6.65 V, 0 ≤ I_{Load} ≤ 1 A, T_J = 25°C(2)		0.4	2.6	
		V_{OUT} = 6.65 V, 0 ≤ I_{Load} ≤ 1 A, T_J = 125°C(2)		2.8	3.5	
		V_{OUT} = 6.65 V, 0 ≤ I_{Load} ≤ 2 A, T_J = –55°C(2)		3.5	5.9	
		V_{OUT} = 6.65 V, 0 ≤ I_{Load} ≤ 2 A, T_J = 25°C(2)		1.1	4.7	
		V_{OUT} = 6.65 V, 0 ≤ I_{Load} ≤ 2 A, T_J = 125°C(2)		5.8	8	
		V_{OUT} = 6.65 V, 0 ≤ I_{Load} ≤ 3 A, T_J = –55°C(2)		5.6	9.3	
		V_{OUT} = 6.65 V, 0 ≤ I_{Load} ≤ 3 A, T_J = 25°C(2)		3.7	8	
		V_{OUT} = 6.65 V, 0 ≤ I_{Load} ≤ 3 A, T_J = 125°C(2)		13	25	
V_{DO}	Dropout voltage(3)	I_{OUT} = 3 A, V_{OUT} = 1.3 V, V_{IN} = V_{OUT} + V_{DO}		210	335	mV
I_{CL}	Programmable output current limit range	V_{IN} = 1.5 V, V_{OUT} = 1.2 V, PCL resistance = 47 kΩ	500		750	mA
		V_{IN} = 1.5 V, V_{OUT} = 1.2 V, PCL resistance varies	200		3500(4)	
V_{CS}	Operating voltage range at CS		0.3		V_{IN}	V
CSR	Current sense ratio	I_{LOAD} / I_{CS}, V_{IN} = 2.3 V, V_{OUT} = 1.9 V	47394	47500	56000	A/A

(3) The parameter is specified to the limit in characterization, but not production tested.
(4) The maximum limit of the I_{CL}parameter is specified to the limit in characterization, but not production tested.

Electrical Characteristics (continued)

1.5 V ≤ V_{IN} ≤ 7 V, $V_{OUT(target)}$ = V_{IN} – 0.35 V, I_{OUT} = 10 mA, V_{EN} = 1.1 V, C_{OUT} = 22 µF, PG terminal pulled up to V_{IN} with 50 kΩ, over operating temperature range (T_J = –55°C to 125°C), unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{GND}	GND terminal current	V_{IN} = 1.5 V, V_{OUT} = 1.2 V, I_{OUT} = 2 A			10	16	mA
I_Q	Quiescent current (no load)	V_{IN} = V_{OUT} + 0.5 V, I_{OUT} = 0 A			7	10	mA
I_{SHDN}	Shutdown current	1.5 V ≤ V_{IN} ≤ 7 V, pre and post 100 krads (Si), T_J = 25°C(5)			26	230	µA
I_{SNS}, I_{FB}	FB/SNS terminal current	V_{IN} = 7 V, V_{OUT} = 6.65 V			1	5	nA
I_{EN}	EN terminal input current	V_{IN} = 7 V, V_{EN} = 7 V, V_{OUT} = 6.65 V			20	150	nA
V_{ILEN}	EN terminal input low (disable)	1.5 V < V_{IN} < 7 V				0.55	V
V_{IHEN}	EN terminal input high (enable)	1.5 V < V_{IN} < 7 V		V_{IN} – 0.7			V
Eprop Dly	Enable terminal propagation delay	V_{IN} = 2.2 V, EN rise to I_{OUT}rise			650	1000	µs
T_{EN}	Enable terminal turn-on delay	V_{IN} = 2.2 V, V_{OUT} = 1.8 V, I_{LOAD} = 1 A, C_{OUT} = 220 µF, C_{SS} = 2 nF			1.4	1.6	ms
V_{THPG}	PG threshold	No load, 0.8 V ≤ V_{OUT} ≤ 6.65 V		86%	90%		
$V_{THPGHYS}$	PG hysteresis	1.5 V ≤ V_{IN} ≤ 7 V			2%		
V_{OLPG}	PG terminal output low	I_{PG} = 0 mA to –1 mA			120	300	mV
I_{LKGPG}	PG terminal leakage current	V_{OUT} > V_{THPG}, V_{PG} = 1.2 V			0.2	1.5	µA
		V_{OUT} > V_{THPG}, V_{PG} = 7 V			0.5	2.5	
I_{SS}	SS terminal charge current	V_{IN} = 1.5 V to 7 V			2.5	3.5	µA
I_{SSdisb}	SS terminal disable current	V_{IN} = 1.5 V to 7 V			5	10	µA
V_{SS}	SS terminal voltage (device enabled)(6)	V_{IN} = 1.5 V to 7 V				1.232	V
V_{SSdisb}	SS terminal low-level input voltage to disable device	V_{IN} = 1.5 V to 7 V				0.4	V
PSRR	Power-supply rejection ratio	V_{IN} = 2.5 V, V_{OUT} = 1.8 V, C_{OUT} = 220 µF	1 kHz		48		dB
			100 kHz		25		
V_N	Output noise voltage	BW = 10 Hz to 100 kHz, I_{OUT} = 3 A, V_{IN} = 2 V, V_{OUT} = 1.8 V			20.33		$µV_{RMS}$
TSD	Thermal shutdown temperature				185		°C

(5) This maximum limit applies to SMD 5962R13202 post 100-krads (Si) test at 25°C.
(6) Any external pullup voltage should not exceed 1.188 V.

6.6 Typical Characteristics

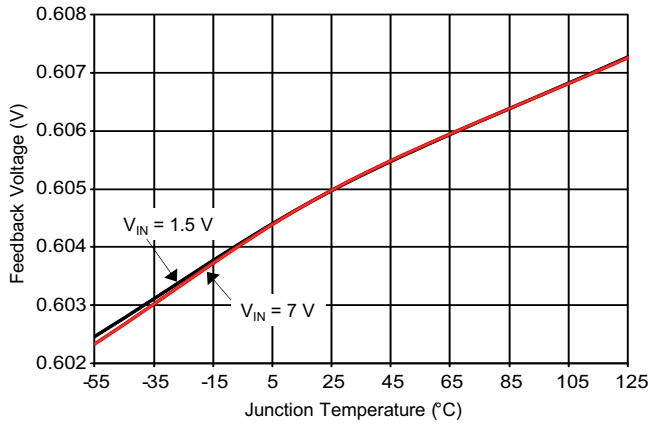


図 1. Feedback Voltage vs Temperature

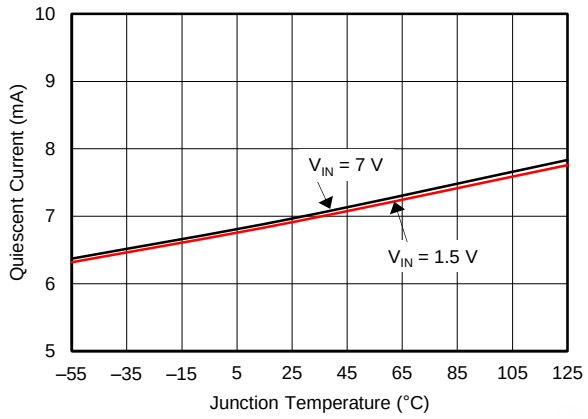


図 2. Quiescent Current vs Temperature

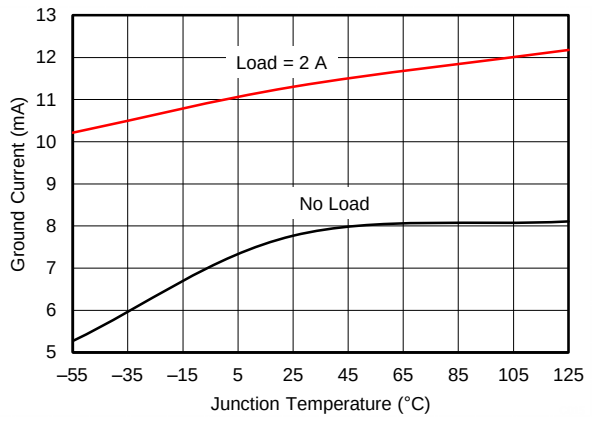


図 3. Ground Current vs Temperature

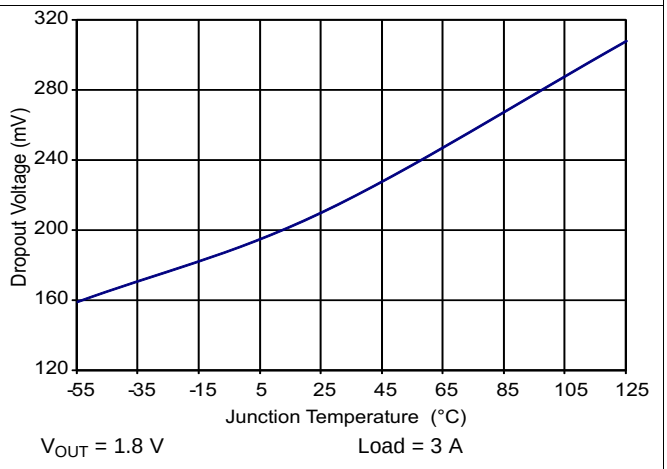


図 4. Dropout Voltage vs Temperature

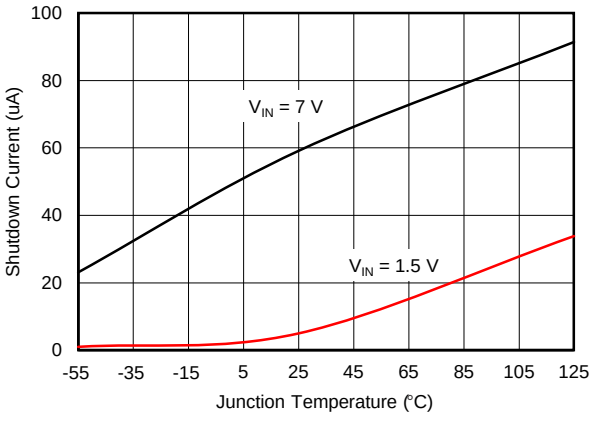


図 5. Shutdown Current vs Temperature

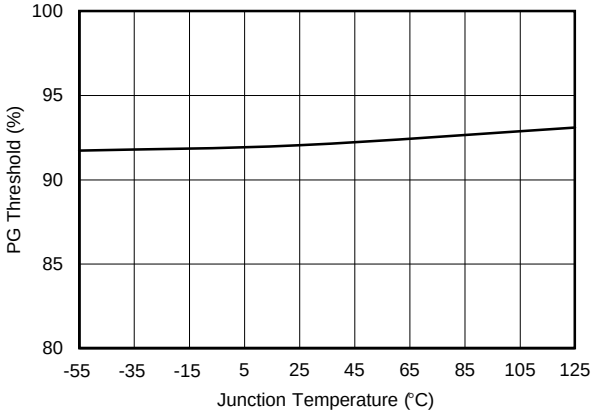
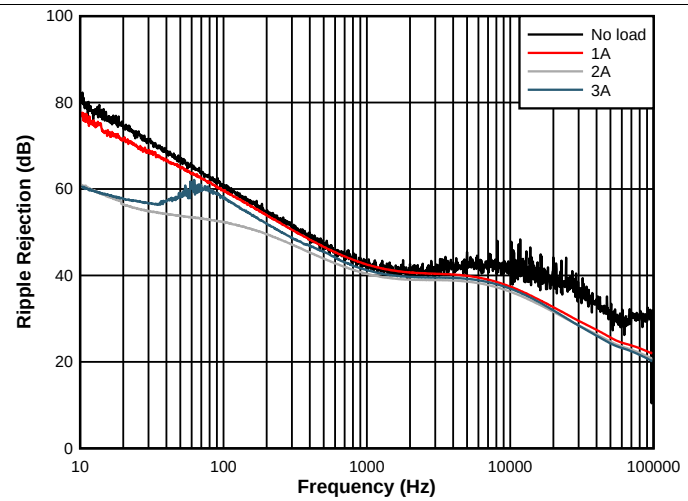


図 6. PG Threshold vs Temperature

Typical Characteristics (continued)



V_{IN} = 2.5 V V_{OUT} = 1.8 V

図 7. Power Supply Ripple Rejection vs Frequency

7 Detailed Description

7.1 Overview

The TPS7H1101A-SP is 3-A, 1.5-V to 7-V LDO linear regulator that uses PMOS pass element configuration.

It uses TI's proprietary process to achieve low noise, high PSRR combined with high-thermal performance in a 16-pin ceramic flatpack package (HKR).

A number of features are incorporated in the design to provide high reliability and system flexibility. Current foldback, current limit, and thermal protection are incorporated in the design to make it viable for harsh environments.

The device also has a current sense monitoring feature. A resistor connected from the current sense (CS) terminal to VIN indicates voltage proportional to the output current. When CS is held high, foldback current limit is enabled. Shorting CS low disables the foldback current limit.

A resistor connected from the programmable current limit (PCL) terminal to ground sets the overcurrent limit activation point. When overcurrent limit activation point is reached, it results in LDO going into current foldback mode. Output current is reduced to approximately 50% of the current limit set point. The *PCL* section provides a detailed description of this feature.

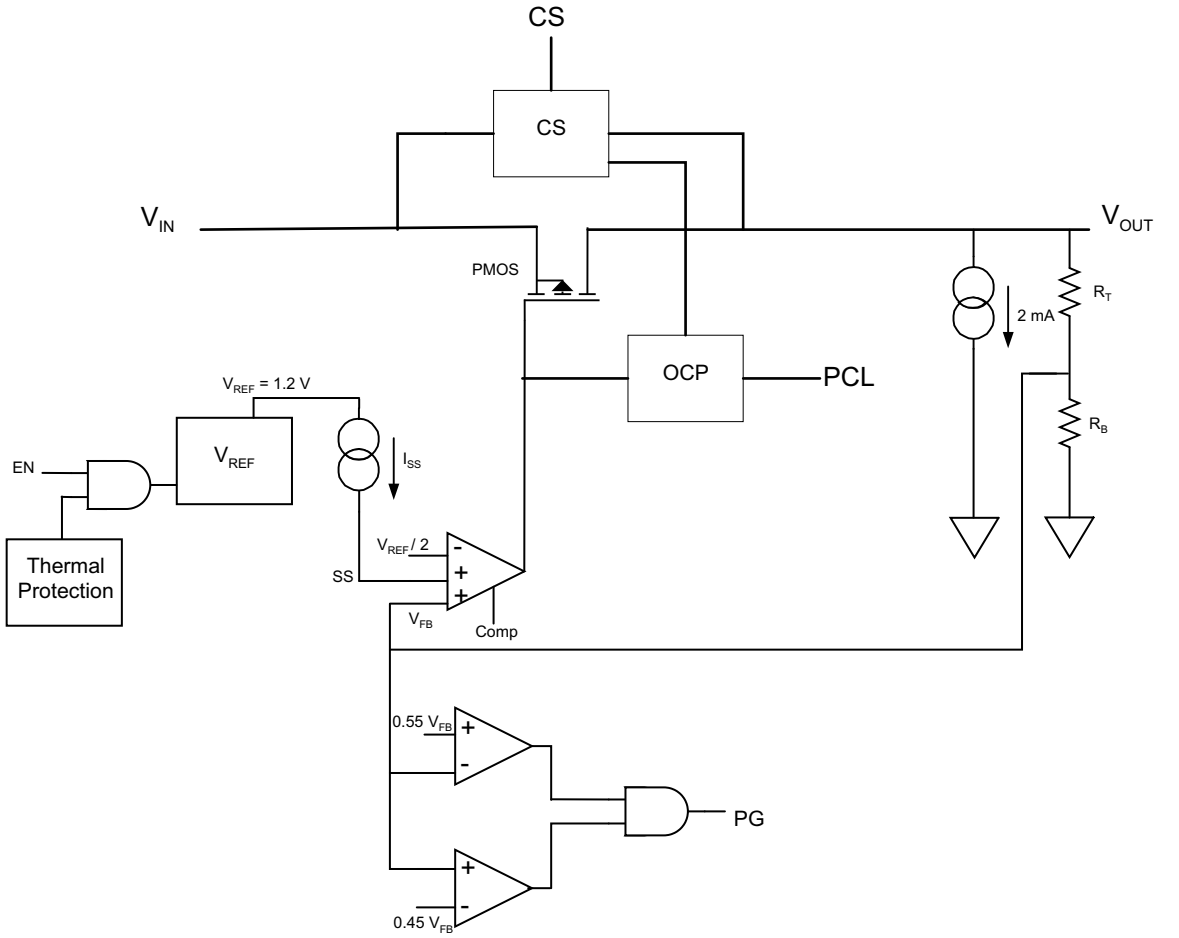
TPS7H1101A-SP incorporates thermal protection, which disables the output when the junction temperature rises approximately 185°C, allowing the device to cool. Cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

A resistor connected from the CS terminal to VIN indicates voltage proportional to the output load current.

To provide system flexibility for demanding current needs, the LDO can be configured in parallel operation as indicated in 図 20. The *Current Sharing* section provides detailed parallel operation information.

An enable feature is incorporated in the design allowing the user to enable or disable the LDO. Power Good, an open-drain connection, indicates the status of the output voltage. These provide the customers system flexibility in monitoring and controlling the LDO operation.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Soft Start

Connecting a capacitor from the SS terminal to GND (C_{SS}) slows down the output voltage ramp rate. The soft-start capacitor charges up to 1.2 V.

$$C_{SS} = \frac{t_{SS} \bullet I_{SS}}{V_{FB}}$$

where

- t_{SS} = soft-start time
- I_{SS} = 2.5 µA
- $V_{FB} = V_{REF} / 2 = 0.605$ V (1)

7.3.2 Power Good (PG)

Power Good terminal (9) is an open-drain connection and can be used to sequence multiple LDOs. 図 8 shows typical connection. The PG terminal will be pulled low until the output voltage reaches 90% of its maximum level. At that point, the PG pin will be pulled up. Since the PG pin is open drain, it can be pulled up to any voltage as long as it does not exceed the absolute max of 7.5 V listed in the *Electrical Characteristics* table.

Feature Description (continued)

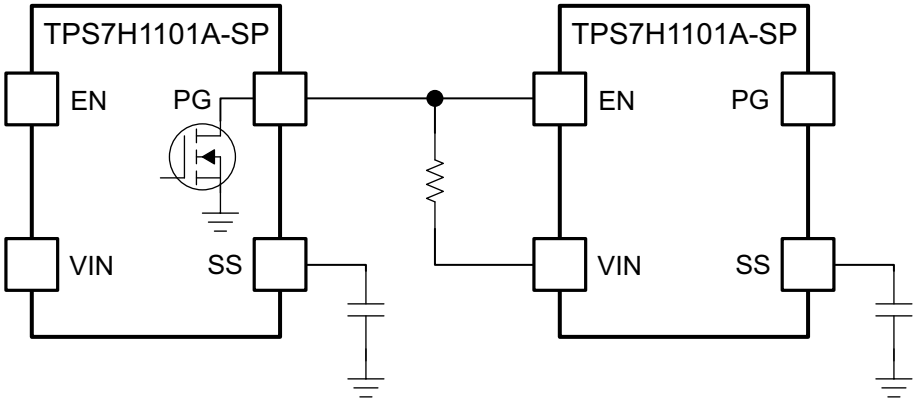


図 8. Sequencing LDOs with Power Good

注

For PSpice models, WEBENCH, and mini-POL reference design, see the *Tools & Software* tab.

1. PSpice average model (stability – Bode plot)
2. PSpice transient model (switching waveforms)
3. WEBENCH design tool, www.ti.com/product/TPS7H1101A-SP/toolssoftware

7.4 Device Functional Modes

7.4.1 Enable/Disable

For V_{IN} from 1.5 V to 7 V, TPS7H1101A-SP can be disabled by pulling the enable terminal to logic low at a minimum of 0.7 V. In all cases, the enable terminal should be connected to V_{IN}.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7H1101A-SP LDO linear regulator is targeted to harsh environment applications. This regulator has various features such as low dropout, soft start, output current foldback, high-side current sensing (where sensing voltage at CS pin provides voltage proportional to output current), and current sharing.

8.1.1 Stability

Conventional Bode plots are a standard approach in assessing stability as shown in 図 9. This approach requires that we have a single feedback path where an AC signal is injected across a resistor (typically 50 Ω) and measurements are taken on either side of the resistor. From this, loop gain and phase plots can be generated. Crossover frequency, f_C, is defined as the frequency where the magnitude of the loop gain is unity and phase margin is evaluated at the crossover frequency f_C.

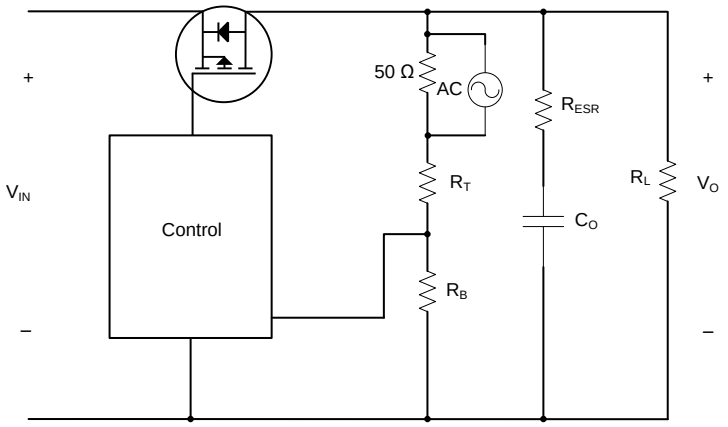


図 9. Conventional Bode Plot

However, there are conditions where the feedback loop is not accessible or there may be multiple feedback paths, as with the TPS7H1101A-SP. When there are multiple feedback loops the conventional Bode plot approach will not be representative of the device's true response. The TPS7H1101A-SP uses a conventional feedback loop in addition to an inner fast loop that injects current into the error amplifier, which in turn greatly improves the transient response of the device. The Bode plot method can still be used to understand the behavior of the main loop, but this will show a lower crossover frequency and thus imply a slower transient response than the actual performance of the device. Fortunately, accurate and quantitative stability metrics can still be assessed from output impedance measurements and simulations.

There are multiple ways output impedance can be measured. One approach is to inject a small current at the output of the regulator and compare it to the resulting voltage response. The variation in the phase of the output impedance across frequency can be related to the phase margin through the group delay.

Group delay, T_g, is the rate of change of phase with respect to frequency as shown in 式 2. Most SPICE simulation packages can plot this parameter and certain frequency analyzers boast software that supports a direct measurement. Using this software, phase margin can be extracted from the group delay plot. The phase margin and crossover frequency reported from these measurements will include the effects of both feedback loops.

$$T_g = \frac{d\phi}{d\omega} \quad (2)$$

Application Information (continued)

The stability of the device can be qualitatively validated by applying a step load to the output and observing the response. The SPICE models for the device can be found in *Tools & Software* on the product page. To simulate impedance measurements, the transient model should be used. For a more detailed explanation of this approach and how to use the model to simulate the output impedance and group delay, please see reference (1) in the *関連資料* section.

8.2 Typical Application

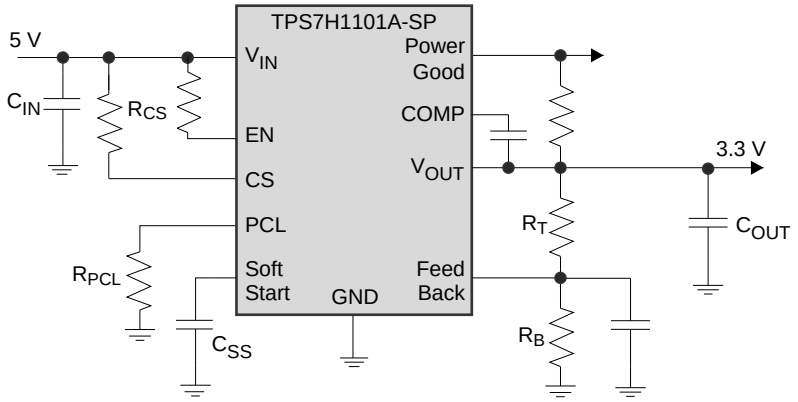


図 10. Typical Application Circuit

Typical Application (continued)

8.2.1 Detailed Design Procedure

8.2.1.1 Adjustable Output Voltage (Feedback Circuit)

The output voltage of the TPS7H1101A-SP can be set to a user-programmable level between 0.8 V and 6.65 V. Achieve this by using a resistor divider connected between V_{OUT}, FB, and GND terminals. R_{TOP} connected between V_{OUT} and V_{FB}, and R_{BOTTOM} connected between V_{FB} and GND.

Use 式 3 to determine V_{OUT}.

$$V_{OUT} = \frac{(R_{TOP} + R_{BOTTOM}) \bullet V_{FB}}{R_{BOTTOM}} \quad (3)$$

where

- V_{FB} = 0.605 V

表 1. Resistor Values for Typical Voltages

V_{OUT}	Standard 1% Resistors		Standard 0.1% Resistors	
	R_{TOP}	R_{BOTTOM}	R_{TOP}	R_{BOTTOM}
0.8 V	10.7 kΩ	33.2 kΩ	10.7 kΩ	33.2 kΩ
1 V	13.7 kΩ	21 kΩ	12.6 kΩ	19.3 kΩ
1.2 V	11.3 kΩ	11.5 kΩ	11.8 kΩ	12 kΩ
1.5 V	15.8 kΩ	10.7 kΩ	18.2 kΩ	12.3 kΩ
1.8 V	23.2 kΩ	11.8 kΩ	32 kΩ	16.2 kΩ
2.5 V	10.7 kΩ	3.4 kΩ	37.9 kΩ	12.1 kΩ
3.3 V	51.1 kΩ	11.5 kΩ	10.2 kΩ	2.29 kΩ
4 V	13.3 kΩ	2.37 kΩ	31.2 kΩ	5.56 kΩ
5 V	11.5 kΩ	1.58 kΩ	16.2 kΩ	2.23 kΩ
5.5 V	17.4 kΩ	2.15 kΩ	89.8 kΩ	11.1 kΩ
6 V	90.9 kΩ	10.2 kΩ	10.7 kΩ	1.2 kΩ
6.5 V	26.7 kΩ	2.74 kΩ	15.2 kΩ	1.56 kΩ
6.6 V	11.3 kΩ	1.15 kΩ	22.1 kΩ	2.23 kΩ
6.7 V	39.2 kΩ	3.92 kΩ	13.8 kΩ	1.37 kΩ

8.2.1.2 PCL

PCL resistor, R_{PCL}, sets the overcurrent limit activation point and can be calculated per 式 4.

$$R_{PCL} = (CSR \times V_{REF}) / (I_{CL} - 0.0403) \quad (4)$$

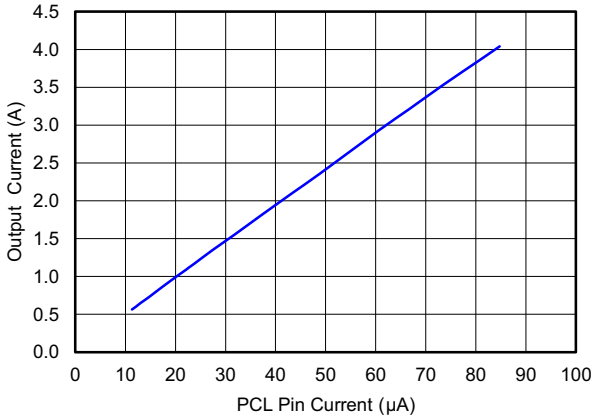
where

- V_{REF} = 0.605 V
- I_{CL} = Programmable current limit (A)
- Current sense ratio (CSR) is the ratio of output load current to I_{CS}. The typical value of the CSR is 47394.

図 11 shows the output load current (I_{OUT}) versus PCL terminal current (I_{CL}).

A suitable resistor R_{PCL} must be chosen to ensure the CS terminal is within its operating range of 0.3 V to V_{IN}.

The maximum PCL is 3.5 A. The range of resistor that can be used on the PCL terminal to GND is 8.2 kΩ to 160 kΩ.



V_{IN} = 2.3 V V_{OUT} = 1.8 V y = 47394x + 0.0403

図 11. I_{OUT} (A) vs I_{PCL} (µA)

8.2.1.3 High-Side Current Sense

図 12 shows the cascode NMOS current mirror. V_{cs} must be in the range as specified in the *Electrical Characteristics* table. The following example shows the typical calculation of R_{cs}.

$$I_{CS} = \frac{I_{LOAD} + I_{offset}}{CSR} \quad (5)$$

$$R_{CS} = \frac{V_{IN} - V_{CS}}{I_{CS}} \quad (6)$$

where

- I_{LOAD} is the output load current.
- CSR is the current sense ratio.

When V_{IN} = 2.3 V, select V_{CS} = 2.05 V, I_{LOAD} = 3 A, CSR = 47394, and I_{offset} = 0.1899 A, then I_{CS} = 67.306 µA and R_{CS} = 3.714 kΩ.

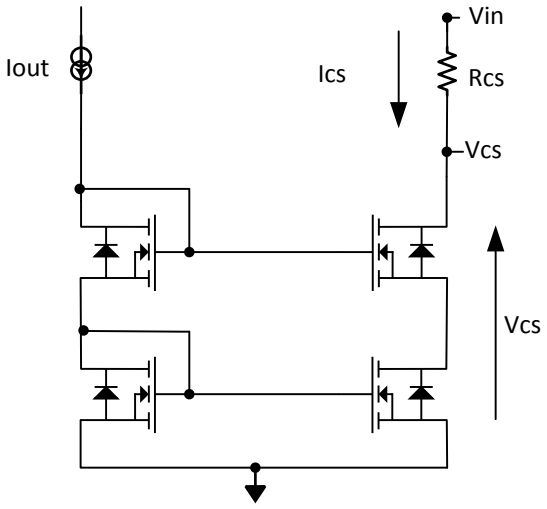
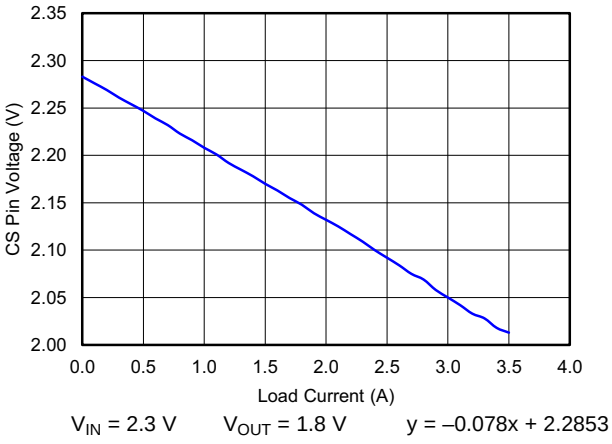


図 12. Cascode NMOS Current Mirror

For TPS7H1101A-SP, 図 13 shows the typical curve V_{CS} vs I_{OUT} for V_{IN} = 2.28 V and R_{CS} = 3.65 kΩ. A resistor connected from the CS terminal to V_{IN} indicates voltage proportional to the output current.

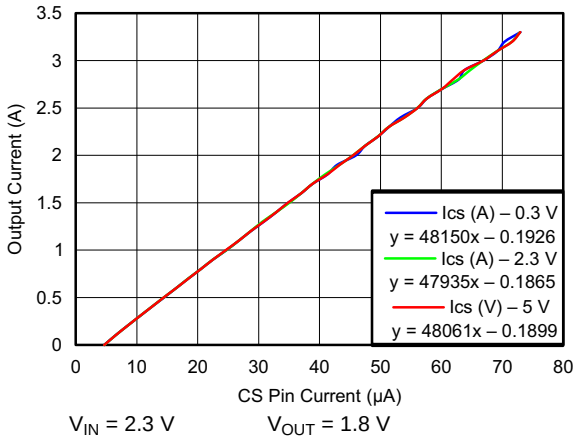
Monitoring current in the CS terminal (I_{CS} vs I_{OUT}) indicates the current sense ratio between the main PMOSFET and the current sense MOSFET as shown in 図 14.

図 15 shows I_{OUT} vs I_{CS} when the voltage on CS terminal is varied from 0.3 V to 7 V.



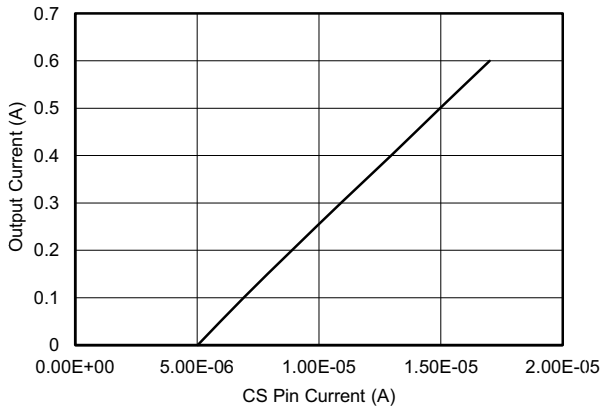
V_{IN} = 2.3 V V_{OUT} = 1.8 V y = –0.078x + 2.2853

図 13. V_{CS} (V) vs I_{OUT} (A)



V_{IN} = 2.3 V V_{OUT} = 1.8 V

図 14. I_{OUT} (A) vs I_{CS} (A)



y = 49917x – 0.2466

図 15. I_{OUT} (A) vs I_{CS} (A)

8.2.1.4 Current Foldback

1. The TPS7H1101A-SP has a current foldback feature which can be enabled when the CS terminal is held high. Shorting CS low disables the foldback current limit. If the foldback current limit is disabled, then the LDO will begin regulating again as soon as the current falls below the clamp threshold.
2. With foldback current limit enabled, when current limit trip point is activated,
   (a) Output voltage drops low, and
   (b) Output current folds back to approximately 50% of the current limit trip point.
   This results in minimizing the power loss under fault conditions. Monitoring the voltage at the CS terminal indicates voltage proportional to the output current.

8.2.1.5 Transient Response

図 16, 図 17, and 図 18 indicate the transient response behavior of the LDO for 50% step load change.

Channel 1: Input voltage

Channel 2: Output voltage overshoot/undershoot

Channel 3: Step load in current

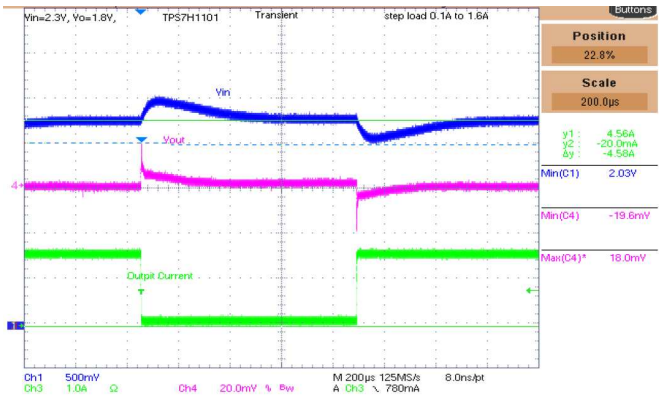


図 16. Load Transient Response: Step Load 0.1 to 1.6 A, V_{IN} = 2.3 V, V_{OUT} = 1.8 V

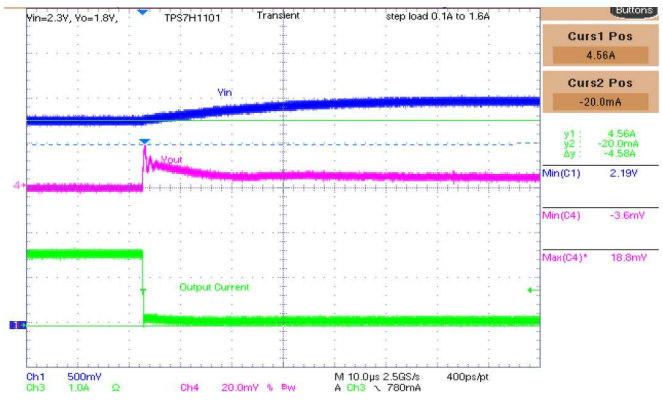


図 17. Expanded View Overshoot

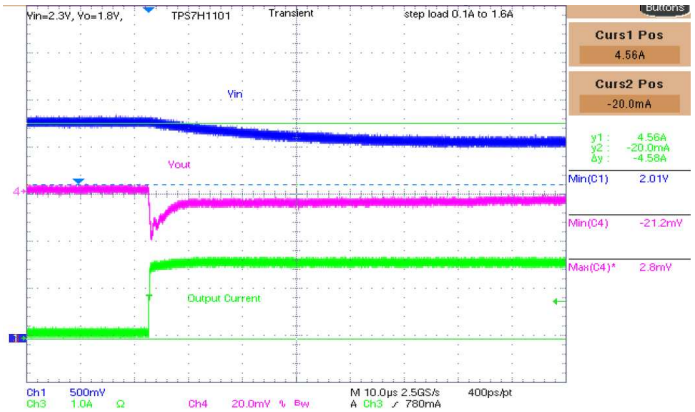


図 18. Expanded View Undershoot

8.2.1.6 Current Sharing

For demanding load requirements, multiple LDOs can be paralleled as indicated in 図 20. In parallel mode, the CS terminal of LDO1 must be connected to the PCL terminal of LDO2 via a series resistor, R_{CL}, and CS terminal of LDO2 must be connected to PCL terminal of LDO1 via series resistor, R_{CL}. The typical value of R_{CL} in parallel operation is 3.75 kΩ for current limit > 6 A. In parallel configuration, R_{CL} (resistor from PCL to GND) and R_{CS} (resistor from CS terminal to V_{IN}) must be left open (unpopulated). The R_{CL} value must be selected so that the operating condition of the CS terminal is maintained, as specified in the *Electrical Characteristics* table. The current from PCL through RCL of LDO1 is determined by the output load current of LDO2 divided by the CSR. Hence, the voltage at CS terminal of the LDO1 is 0.605 V – ((output load current of LDO2 + 0.2458) / CSR × R_{CL}).

Alternately, it can also provide twice the output current to meet system needs. When using two LDOs in parallel operation for higher output load current, use POL TPS50601-SP as an input source.

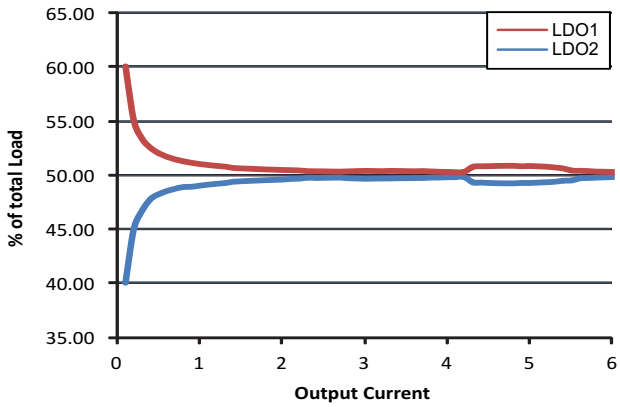


図 19. LDO Current Share

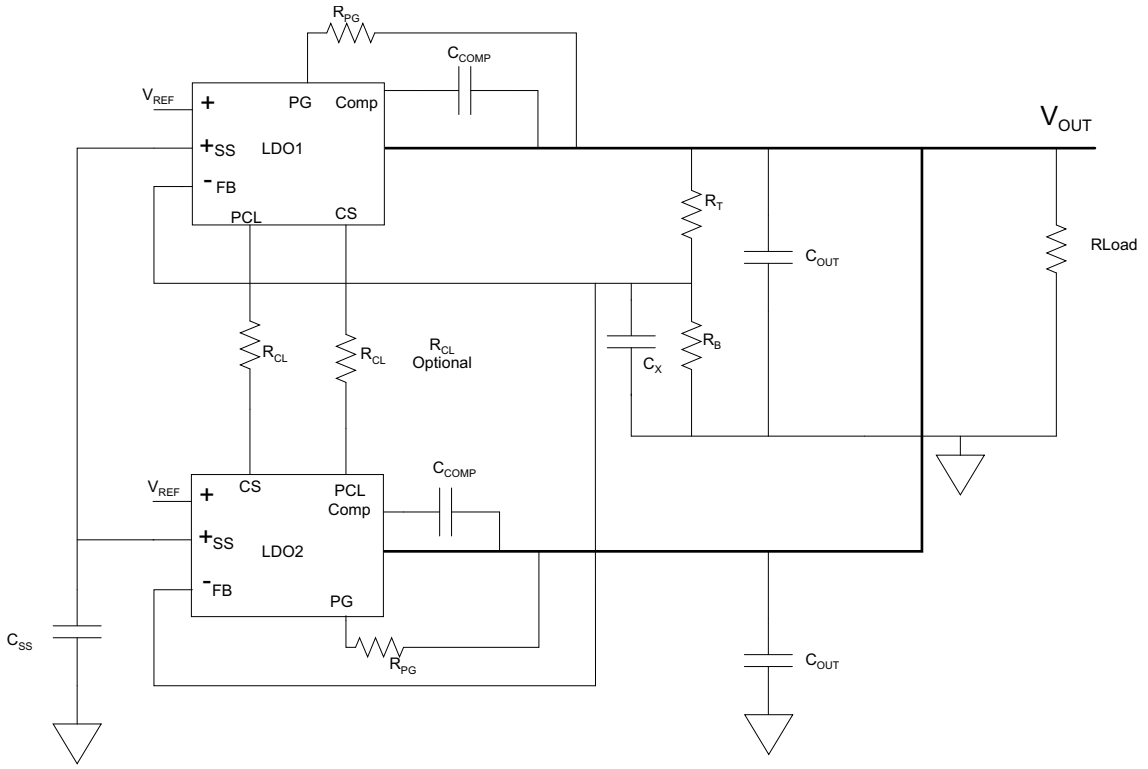


図 20. Block Diagram (Parallel Operation)

8.2.1.7 Compensation

図 21 shows a generic block diagram for TPS7H1101A-SP LDO with external compensation components. LDO incorporates nested loops, thus providing the high gain necessary to meet design performance.

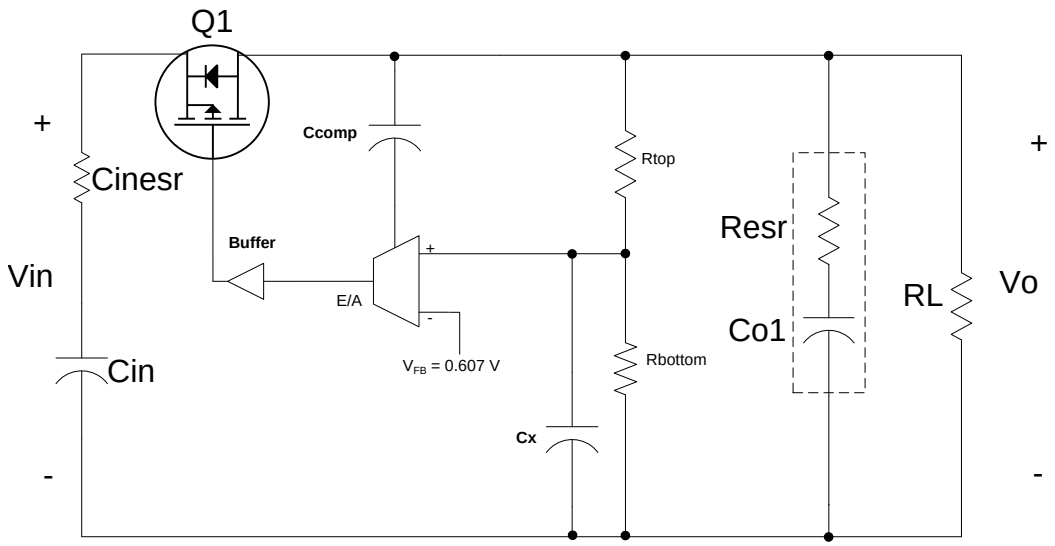


図 21. TPS7H1101A-SP Compensation

Resistor divider composed of R_{top} and R_{bottom} determine the output voltage set points as indicated by 式 3.

Output capacitor C_{OUT} introduces a pole and a zero as shown in the following.

$$F_{p\_co} = \frac{1}{2 \bullet \pi \bullet C_o \bullet R_L} \quad (7)$$

$$F_{z\_co} = \frac{1}{2 \bullet \pi \bullet C_o \bullet C_{esr}} \quad (8)$$

The TPS7H1101A-SP was designed so that the ESR of the output capacitor will not have a strong influence on the response of the LDO. However, an optional capacitor, C_x, can be added in parallel with the bottom feedback resistor to introduce a pole to cancel F_{z_co}. 式 9 shows how to calculate the location of the pole introduced by C_x. To cancel the zero directly, F_p should be equal to F_{z_co}.

$$F_p = \frac{1}{2 \bullet \pi \bullet C_x \bullet R_{bottom}} \quad (9)$$

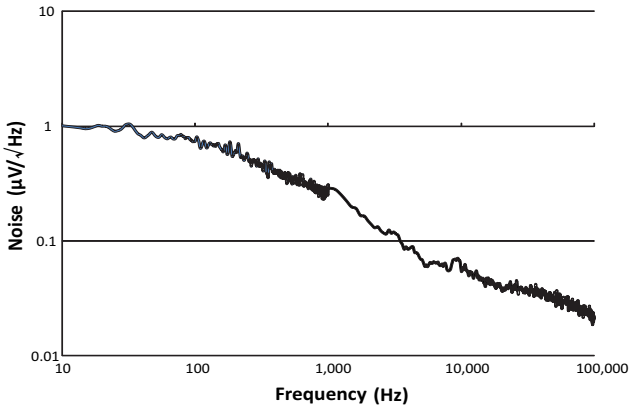
C_x is calculated to be 1000 pF for C_o = 220 µF, C_{esr} = 45 mΩ, and R_{bottom} = 10 kΩ.

Internal compensation in the LDO cancels the output capacitor pole introduced by C_{OUT} and R_L.

C_{comp} introduces a dominant pole at low frequency. TI recommends that a C_{comp} value of 10 nF.

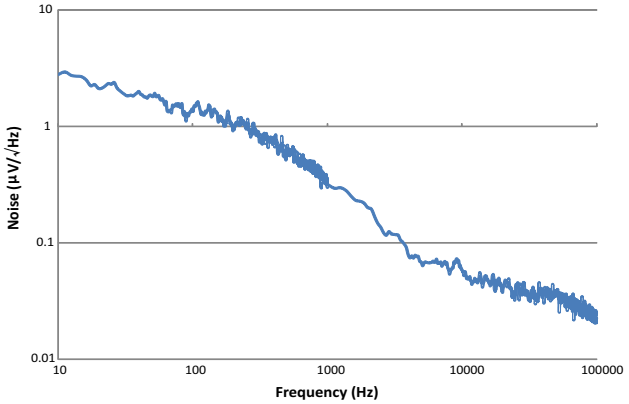
8.2.1.8 Output Noise

Output noise is measured using an HP3495A. 図 22 and 図 23 show noise of the TPS7H1101A-SP in µV/√Hz vs frequency.



V_{IN} = 2 V V_{OUT} = 1.8 V at 3 A
C_{IN} = 220 µF C_{LOAD} = 220 µF

図 22. RMS Noise (10 Hz to 100 kHz) = 20.33 µVrms



V_{IN} = 7 V V_{OUT} = 6.7 V at I_{LOAD} = 3 A
C_{IN} = 220 µF C_{LOAD} = 220 µF

図 23. RMS Noise (10 Hz to 100 kHz) = 31.68 µVrms

8.2.1.9 Capacitors

TPS7H1101A-SP requires the use of a combination of tantalum and ceramic capacitors to achieve good volume to capacitance ratio. 表 2 highlights some of the capacitors used in the device. TI recommends to follow proper derating guidelines as recommended by the capacitor manufacturer based upon output voltage and operating temperature.

Note that polymer-based tantalum capacitors must be derated to at least 60% of rated voltage, whereas manganese oxide (MnO_2) based tantalum capacitors should be derated to 33% of rated voltage depending upon the operating temperature.

TI recommends to use a tantalum capacitor along with a 0.1-µF ceramic capacitor. The device is stable for input and output tantalum capacitor values of 10 µF to 220 µF with the ESR range of 10 mΩ to 2 Ω. However, the dynamic performance of the device varies based on load conditions and the capacitor values used.

TI recommends a minimum output capacitor of 22 µF with ESR of 1 Ω or less to prevent oscillations. X7R dielectrics are preferred. See 表 2 for various capacitor recommendations.

表 2. TPS7H1101A-SP Capacitors

CAPACITOR PART NUMBER	CAPACITOR DETAILS (CAPACITOR, VOLTAGE, ESR)	TYPE	VENDOR
T493X107K016CH612A(1)	100 µF, 16 V, 100 mΩ	Tantalum - MnO2	Kemet
T493X226M025AH6x20(1)	22 µF, 25 V, 35 mΩ	Tantalum - MnO2	Kemet
T525D476M016ATE035(1)	47 µF, 10 V, 35 mΩ	Tantalum - Polymer	Kemet
T540D476M016AH6520(1)	47 µF, 16 V, 20 mΩ	Tantalum - Polymer	Kemet
T525D107M010ATE025(1)	100 µF, 10 V, 25 mΩ	Tantalum - Polymer	Kemet
T541X337M010AH6720(1)	330 µF, 10 V, 6 mΩ	Tantalum - Polymer	Kemet
T525D227M010ATE025(1)	220 µF, 10 V, 25 mΩ	Tantalum - Polymer	Kemet
T495X107K016ATE100(1)	100 µF, 16 V, 100 mΩ	Tantalum - MnO2	Kemet
CWR29FK227JTHC(1)	220 µF, 10 V, 180 mΩ	Tantalum - MnO2	AVX
THJE107K016AJH	100 µF, 16 V, 58 mΩ	Tantalum	AVX
THJE227K010AJH	220 µF, 10 V, 40 mΩ	Tantalum	AVX
SMX33C336KAN360	33 µF, 25 V	Stacked ceramic	AVX
SR2225X7R335K1P5#M123	3.3 µF, 25 V, 10 mΩ	Ceramic	Presidio Components Inc

(1) Operating temperature is –55°C to 125°C.

8.2.2 Application Curves

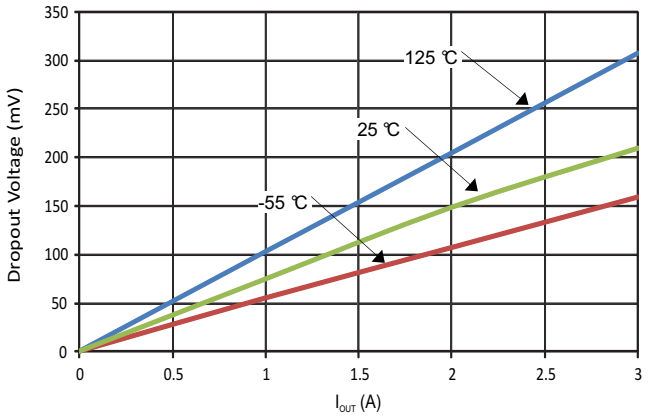


図 24. VDO vs I_{OUT}

9 Power Supply Recommendations

This device is designed to operate with an input voltage supply up to 7 V. The minimum input voltage should provide adequate headroom greater than the dropout voltage for the device to have a regulated output. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

- For best performance, all traces should be as short as possible, and no longer than 5 cm.
- Use wide traces for IN, OUT and GND to minimize the parasitic electrical effects.
- Place the output capacitors (COUT) as close as possible to the OUT pin of the device.

10.2 Layout Example

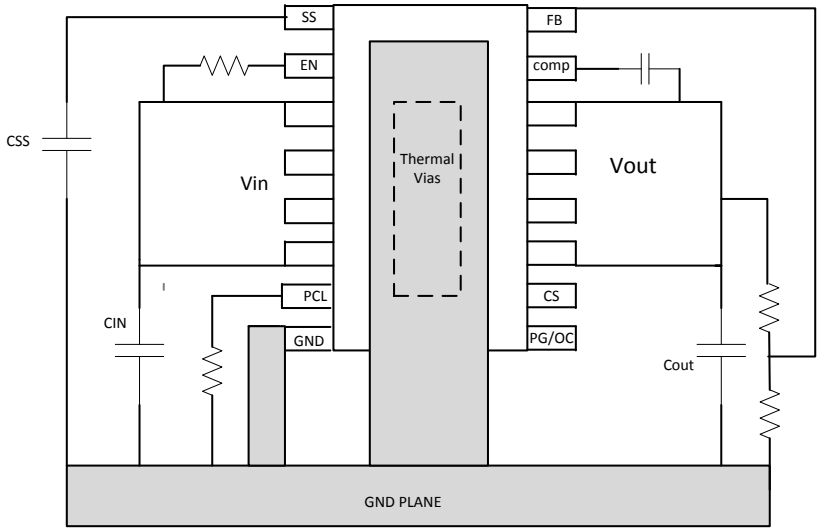


図 25. PCB Layout Example

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 デベロッパー・ネットワークの製品に関する免責事項

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11.1.2 デバイスの項目表記

KGD 品質保証のベア・ダイ

RHA 宇宙用システム向けの放射線強度保証

5962R13202 TPS50601-SPと同じデバイスで、標準のマイクロ回路図面(SMD)とともに示されています。

TPS7H1101A-SP 5962R10221と同じデバイスで、TIのパッケージ図とともに示されています。

11.2 ドキュメントのサポート

11.2.1 関連資料

(1) *『固定レギュレータの安定性評価』*、Tom Boehler、Paul Ho、AEi Systems

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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11.5 商標

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11.6 静電気放電に関する注意事項

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11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962R1320202V9A	ACTIVE	XCEPT	KGD	0	70	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 125		Samples
5962R1320202VXC	ACTIVE	CFP	HKR	16	25	RoHS-Exempt & Green	NIAU	N / A for Pkg Type	-55 to 125	5962R1320202VXC TPS7H1101-RHA	Samples
TPS7H1101AHKR/EM	ACTIVE	CFP	HKR	16	25	RoHS-Exempt & Green	NIAU	N / A for Pkg Type	25 to 25	TPS7H1101AHKR/EM EVAL ONLY	Samples
TPS7H1101AY/EM	ACTIVE	XCEPT	KGD	0	5	RoHS & Green	Call TI	N / A for Pkg Type	25 to 25		Samples
TPS7H1101HKR/EM	ACTIVE	CFP	HKR	16	25	RoHS-Exempt & Green	NIAU	N / A for Pkg Type	25 to 25	TPS7H1101HKREM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

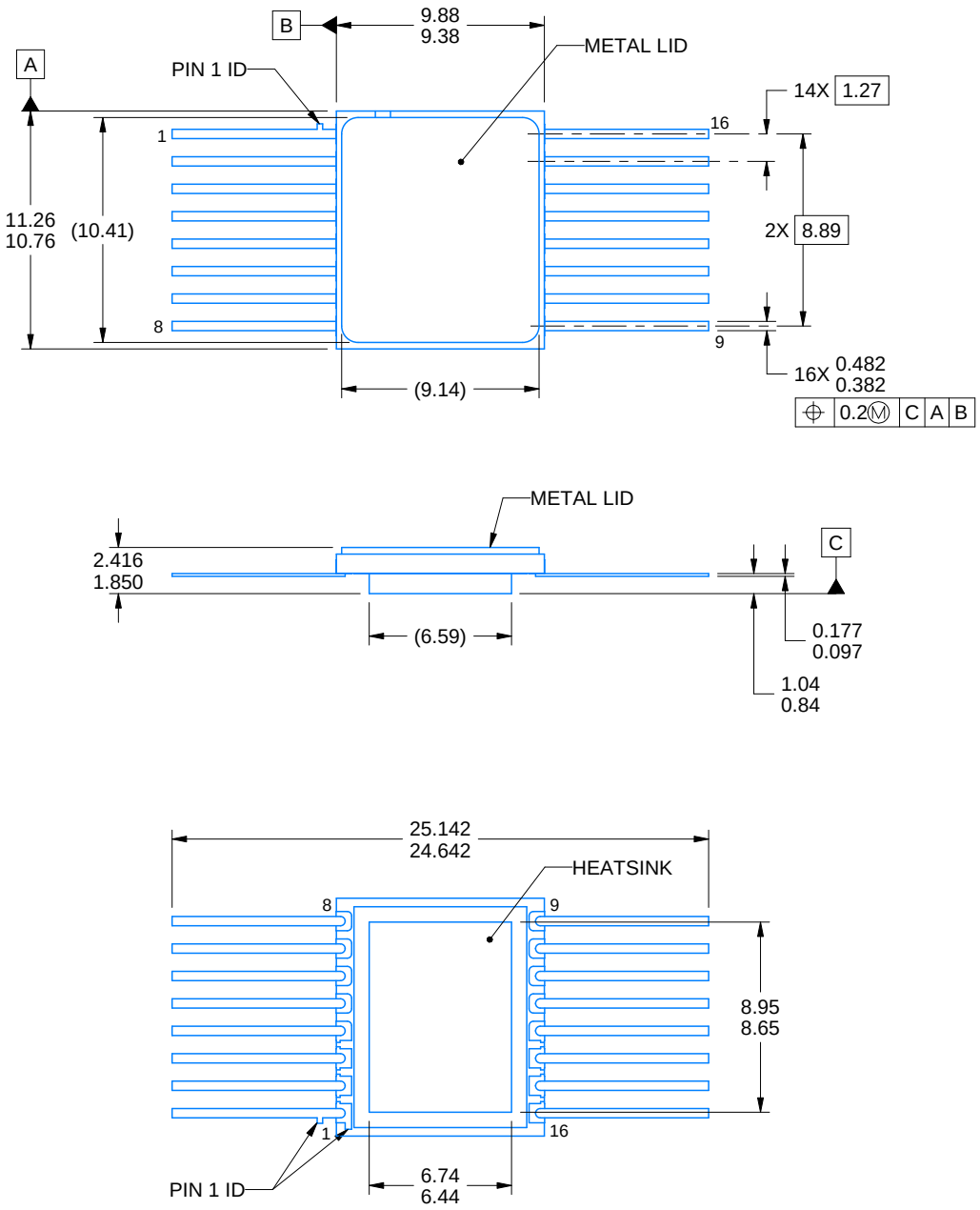
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

HKR0016A

CFP - 2.416 mm max height

CERAMIC DUAL FLATPACK



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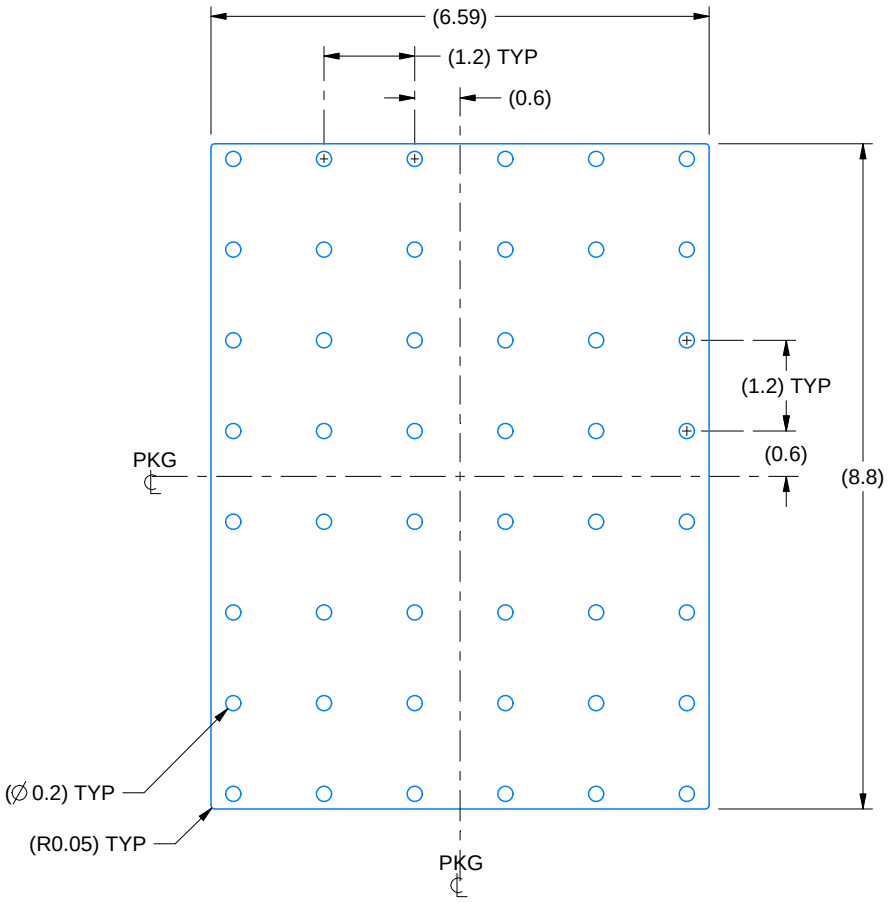
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid. Lid is connected to Heatsink.
4. The terminals are gold plated.
5. Falls within MIL-STD-1835 CDFP-F11A.



HEATSINK LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X

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