TEXAS INSTRUMENTS
TPSM82902
JAJSPB3 – NOVEMBER 2022

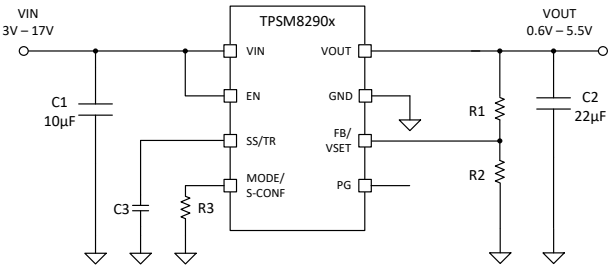
TPSM82902、2-A、3V～17V、高効率の低 I_Q 降圧コンバータ・モジュール、MicroSiP™ パッケージで供給、インダクタ内蔵

1 特長

- 高効率で、広いデューティ・サイクルと広い負荷範囲に対応
  - I_Q：4µA (標準値)
  - 62mΩ ハイサイドおよび 22mΩ ローサイド $R_{DS(ON)}$
- 3mm × 2.8mm × 1.6mm の MicroSiP™ パッケージ
- 最大 2A の連続出力電流
- -40℃～125℃の範囲で ±0.9% の帰還電圧精度
- 構成可能な出力電圧：
  - V_{FB} 外部分圧器：0.6V～5.5V
  - V_{SET} 内部分圧器：0.4V～5.5V の 16 通りの選択肢
- 100% モードを備えた DCS-Control トポロジ
- MODE/S-CONF ピンによる優れた柔軟性
  - 2.5MHz または 1.0MHz のスイッチング周波数
  - 強制 PWM または自動 PFM パワー・セーブ・モード (動的モード変更機能付き)
  - 自動効率向上 (AEE)
  - 出力放電のオン / オフ
- きわめてフレキシブルで優れた使いやすさ
  - 単層ルーティング用に最適化されたピン配置
  - 高精度イネーブル入力
  - パワー・グッド出力
  - 可変ソフトスタートおよびトラッキング
- 外部ブートストラップ・コンデンサ不要
- WEBENCH® Power Designer により、TPSM82902 を使用するカスタム設計を作成

2 アプリケーション

- データ・センターおよびエンタープライズ・コンピューティング
- 有線ネットワーク
- ワイヤレス・インフラ
- ファクトリ・オートメーション / 制御
- 試験 / 測定機器



概略回路図

3 概要

TPSM82902 は、使いやすく、高効率、小型、フレキシブルな同期整流降圧 DC/DC コンバータ MicroSiP パッケージ・モジュールです。スイッチング周波数は 2.5MHz または 1.0MHz を選択可能で、小型の部品を使用でき、高速な過渡応答を実現します。このデバイスは、DCS-Control トポロジにより ±1% の高い V_{OUT} 精度をサポートしています。3V～17V の広い入力電圧レンジで動作するため、12V 電源レール、シングル・セルまたはマルチ・セルのリチウムイオン、5V または 3.3V レールなど、各種の公称入力に対応します。

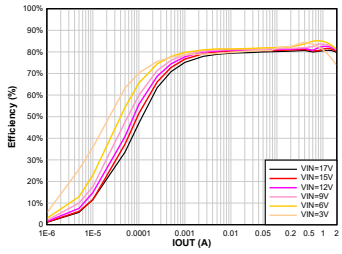
TPSM82902 は、軽負荷時には自動的にパワー・セーブ・モードに移行し (自動 PFM/PWM 選択時)、高効率を維持します。また、非常に小さな負荷でも高い効率を実現するため、標準的な静止電流は 4µA と低くなっています。AEE がイネーブルの場合、V_{IN}、V_{OUT}、負荷電流の全体にわたる高効率を実現します。このデバイスは、内部 / 外部分圧器、スイッチング周波数、出力電圧放電、自動パワー・セーブ・モードまたは強制 PWM 動作を設定する MODE/Smart-CONF 入力を備えています。

このデバイスは、3.0mm × 2.8mm × 1.6mm の小型 11 ピン MicroSiP パッケージで供給され、1µH インダクタが内蔵されています。

パッケージ情報

部品番号	パッケージ (1)	本体サイズ (公称)
TPSM82902	SIS (uSiP、11)	3.00mm × 2.80mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



効率と出力電流との関係 (V_O = 1.2V、2.5MHz の自動 PFM/PWM 時)

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
November 2022	*	Initial Release

5 Pin Configuration and Functions

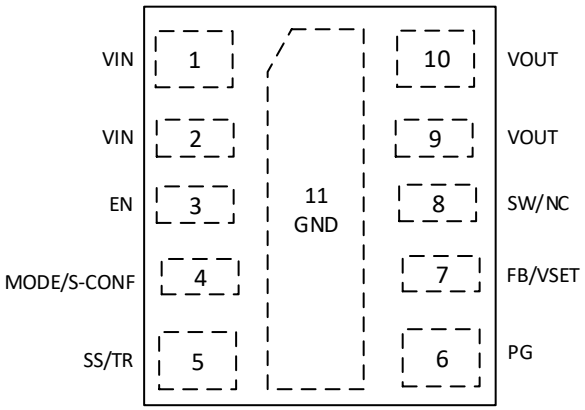


図 5-1. 11-Pin SIS MicroSiP™ Package (Top View, Device Pins Face Down)

表 5-1. Pin Functions

Pin		I/O	Description
Name	Number		
VIN	1, 2	I	Power supply input pin. Ensure the input capacitor is connected as close as possible between the VIN and GND pins.
EN	3	I	Enable input pin. Connect to logic low to disable the device. Pull high to enable the device. Do not leave this pin unconnected.
MODE/ S-CONF	4	I	Device mode selection (auto PFM/PWM or forced PWM operation) and SmartConfig™ application. Connect high, low, or to a resistor to configure the device according to 表 7-2. Do not leave this pin unconnected.
SS/TR	5	I	Soft start/tracking pin. An external capacitor connected from this pin to GND defines the rise time for the internal reference voltage. The pin can also be used as an input for tracking and sequencing. The pin can be left floating for the fastest ramp-up time.
PG	6	O	Open-drain power-good output. High = V_{OUT} is ready. Low = V_{OUT} is below nominal regulation. This pin requires a pullup resistor.
FB/VSET	7	I	Depends on device configuration (see セクション 7.3.1) • FB: Voltage feedback input. Connect a resistive output voltage divider to this pin. • VSET: Output voltage setting pin. Connect a resistor to GND to choose the output voltage according to 表 7-3.
SW/NC	8	NC	Switch pin of the converter. Do not connect, leave floating.
VOUT	9, 10	O	Output voltage pin. Connect directly to the positive pin of the output capacitor.
GND	11	—	Ground pin. It must be connected directly to the common ground plane. It must be soldered to achieve appropriate power dissipation and mechanical reliability.

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	VIN	–0.3	18	V
	EN, PG	–0.3	18	
	MODE/S-CONF	–0.3	18	
	FB/VSET, SS/TR, VOUT	–0.3	6	
T_J	Junction temperature	–55	125	°C
	Peak reflow case temperature		260	°C
	Maximum number of reflows allowed		3	
Mechanical shock	Mil-STD-883D, Method 2002.3, 1 msec, 1/2 sine, mounted		1500	G
Mechanical vibration	Mil-STD-883D, Method 2007.2, 20 to 2000 Hz		20	G
T_{stg}	Storage temperature	–55	125	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_I	Input voltage range	3.0		17	V
V_O	Output voltage range	0.4		5.5	V
C_I	Effective input capacitance	3	10		µF
C_O	Effective output capacitance (2.5MHz selection)	10	22	100 (1)	µF
C_O	Effective output capacitance (1.0MHz selection)	6	22	50 (1)	µF
I_{OUT}	Output current	0		2	A
I_{SINK_PG}	Sink current at PG-Pin			1	mA
T_J	Junction temperature (2)	-40		125	°C

(1) This is for capacitors directly at the output of the device. More capacitance is allowed if there is a series resistance associated to the capacitor.
(2) Operating lifetime is derated at junction temperatures greater than 125°C.

6.4 Thermal Information

THERMAL METRIC(1)		TPSM8290x uSIP11-Pin		UNIT
		JEDEC PCB	TPSM8290xEVM-188	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	58.2	48.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34.5		°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	26.9		°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	0.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	26.6	27.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	26.0		°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

V_I = 3 V to 17 V, T_J = -40°C to +125°C, Typical values at V_I = 12.0 V and T_A = 25°C,unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_{Q_PSM}	Operating Quiescent Current (Power Save Mode)	Iout = 0 mA, device not switching		4		µA
I_{Q_PWM}	Operating Quiescent Current (PWM Mode)	VIN=12 V, VOUT=1.2 V; Iout = 0 mA, device switching		8		mA
I_{SD}	Shutdown current into VIN pin	EN = 0 V		0.27	3.5	µA
V_{UVLO}	Under Voltage Lock-Out	V_{IN} rising	2.85	2.925	3.0	V
	Under Voltage Lock-Out	V_{IN} falling	2.7	2.775	2.85	V
V_{UVLO_HYS}	Under Voltage Lock-Out Hysteresis	Hysteresis		150		mV
CONTROL & INTERFACE						
I_{LKG}	EN Input leakage current	EN = 12 V		10	300	nA
V_{IH_MODE}	High-Level Input Voltage at MODE/S-CONF-Pin		1.0			V
T_{SD}	Thermal Shutdown Threshold	T_J rising		170		°C
	Thermal Shutdown Hysteresis	Hysteresis		20		
V_{IH}	High-level input voltage at EN-Pin		0.97	1.0	1.03	V
V_{IL}	Low-level input voltage at EN-Pin		0.87	0.9	0.93	V
R_{EN_PD}	Smart-Enable Internal Pulldown Resistor	EN = LOW		0.5		MΩ
V_{PG}	Power good threshold	V_{FB} rising, referenced to V_{FB} nominal	93.5%	96%	99%	
		V_{FB} falling, referenced to V_{FB} nominal	88.5%	93%	96%	
		Hysteresis	1.5%	3.5%	6%	
V_{PG_OL}	Low-level output voltage at PG pin	I_{SINK} = 1 mA			0.4	V
I_{PG_LKG}	Input leakage current into PG pin	V_{PG} = 5 V		15	550	nA
t_{PG_DLY}	Power good delay time	V_{FB} falling		32		µs
R_{SET}	S-CONF/VSET Resistor Tolerance		–4		+4	%
C_{SET}	Maximum Capacitance connected to S-CONF/VSET Pins				30	pF
POWER SWITCHES						
I_{LKG_SW}	Leakage current into SW-Pin	V_{SW} = V_{OS} = 5.5 V		2	7	µA
R_{DS_ON}	High-side FET on resistance	V_{IN} > 4 V, I_{SW} = 500 mA		62	111	mΩ
	Low-side FET on resistance	V_{IN} > 4 V, I_{SW} = 500 mA		22	40	

6.5 Electrical Characteristics (continued)

V_I = 3 V to 17 V, T_J = -40°C to +125°C, Typical values at V_I = 12.0 V and T_A = 25°C,unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LIM}	High-side FET current limit	TPSM82902	3.6	4.4	5.3	A
	Low-side FET current limit	TPSM82902	3.4	3.8	4.2	A
I_{LIM_SINK}	Low-side FET sink current limit		1.3	1.7	2.5	A
f_{SW}	Switching frequency	2.5-MHz selection		2.5		MHz
$T_{ON(MIN)}$	Minimum On-time			50		ns
f_{SW}	Switching frequency	1.0-MHz selection		1.0		MHz
D	Dutycycle				1	
R_{PD}	Dropout resistance	100% mode, V_{IN} > 4 V		100		mΩ
OUTPUT						
V_{O_Reg1}	Output Voltage Regulation	VSET Configuration selected. T_J = 25°C.	–0.9%		+0.9%	
V_{O_Reg2}	Output Voltage Regulation	VSET Configuration selected. 0 °C< T_J < 85°C	–1.1%		+1.1%	
V_{O_Reg3}	Output Voltage Regulation	VSET Configuration selected. –40°C < T_J < 125°C	–1.25%		+1.25%	
V_{FB}	Feedback Regulation Voltage	Adjustable Configuration selected		0.6		V
V_{FB_Reg1}	Feedback Voltage Regulation	FB-Option selected. T_J = 25°C.	–0.6%		+0.6%	
V_{FB_Reg2}	Feedback Voltage Regulation	FB-Option selected. 0°C < T_J < 85°C.	–0.65%		+0.65%	
V_{FB_Reg3}	Feedback Voltage Regulation	FB-Option selected. –40°C < T_J < 125°C	–0.9%		+0.9%	
I_{FB}	Input leakage current into FB pin	Adjustable configuration, VFB = 0.6 V		1	70	nA
T_{delay}	Start-up delay time	I_O = 0 mA, time from EN=HIGH until start switching, Adjustable Configuration selected		600	1400	µs
	Start-up delay time	I_O = 0 mA, time from EN=HIGH until start switching, VSET Configuration selected. The typical value is based on the first option of VSET configuration.		650	1850	µs
T_{SS}	Soft-Start time	I_O = 0 mA after T_{delay}, from 1st switching pulse until target V_O; TR/SS-Pin = OPEN		150	200	µs
I_{SS}	SS/TR source current		2.3	2.5	2.7	µA
$V_{FB}/V_{SS/TR}$	Tracking Gain, Adjustable Configuration			0.75		
$V_{FB}/V_{SS/TR}$	Tracking Gain tolerance			±8		mV
R_{DISCH}	Active Discharge Resistance	Discharge = ON - Option Selected, EN = LOW,		7.5	20	Ω

6.6 Typical Characteristics

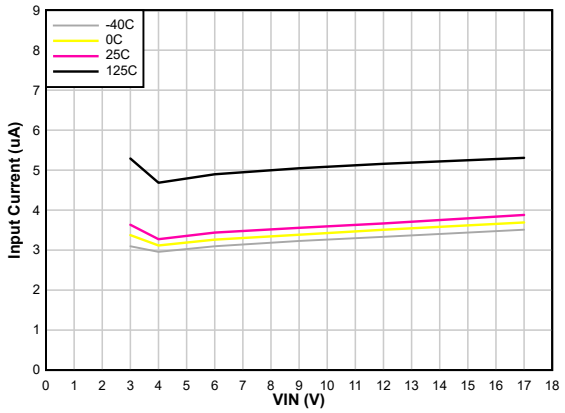


図 6-1. Typical Quiescent Current vs V_{IN}

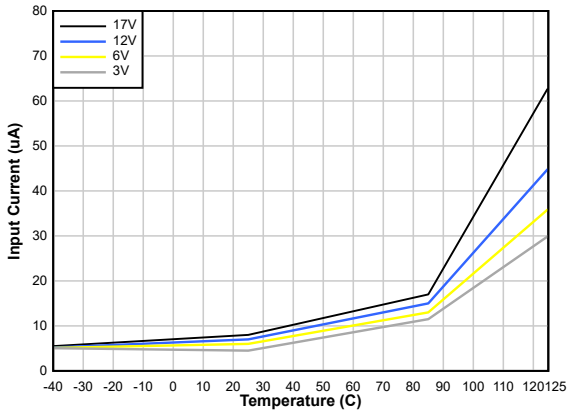


図 6-2. Maximum Quiescent Current vs Temperature

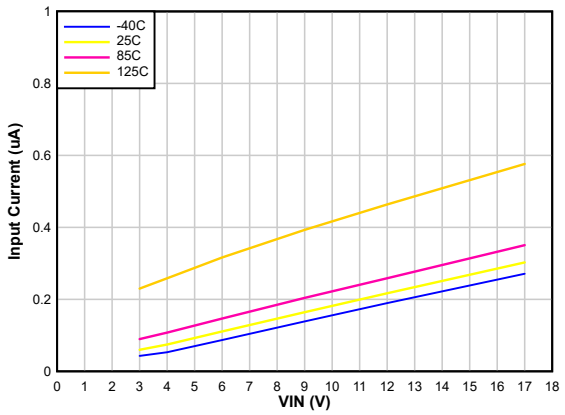


図 6-3. Typical Shutdown Current

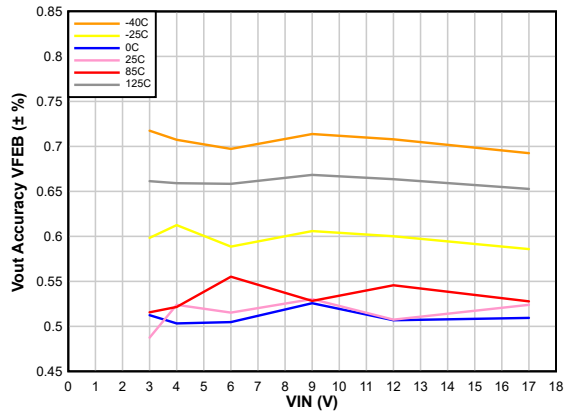


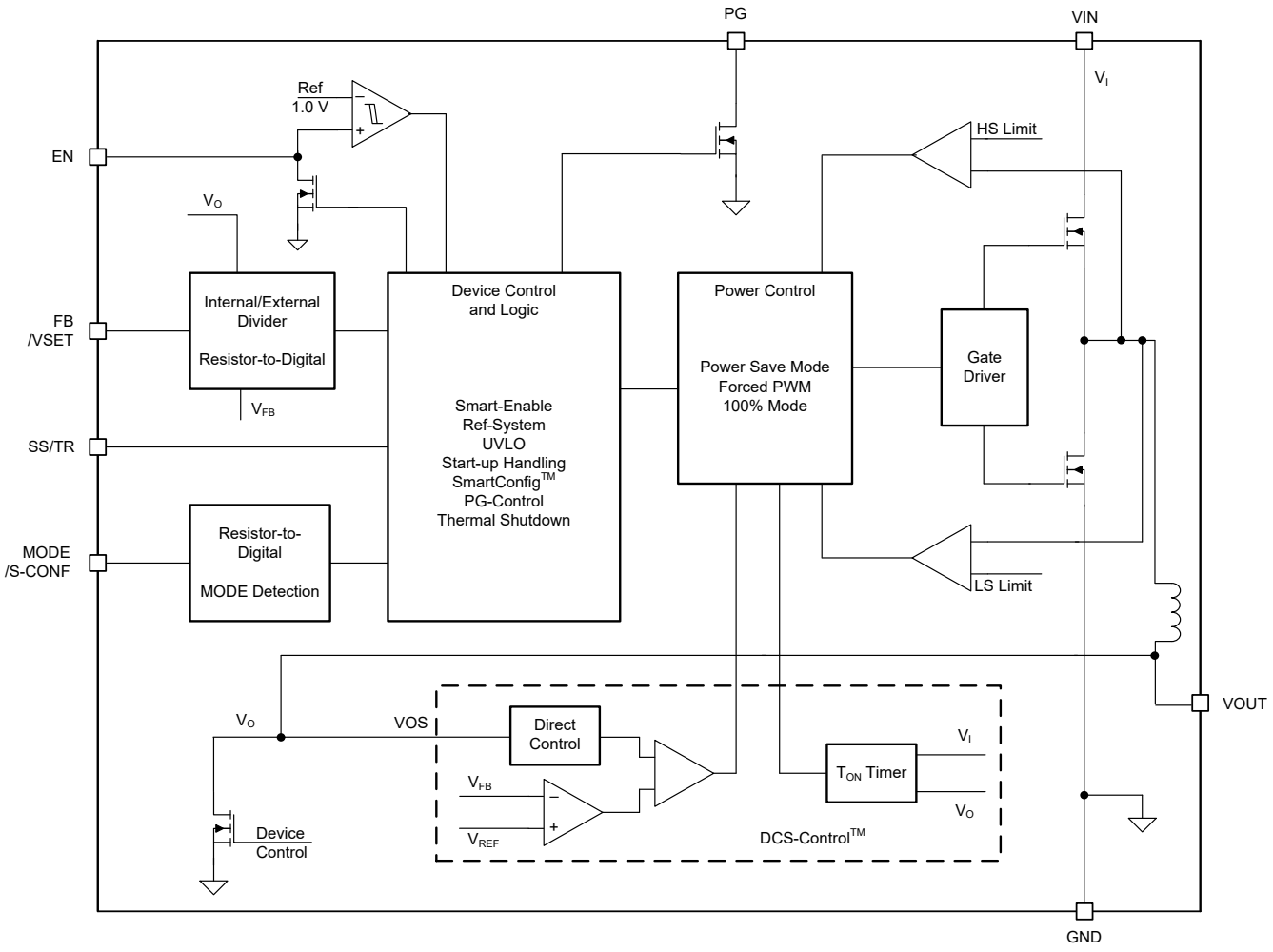
図 6-4. Output Voltage Accuracy – VFEB Selected

7 Detailed Description

7.1 Overview

The TPSM82902 synchronous step-down converter MicroSiP package module is based on DCS-Control (Direct Control with Seamless Transition into power save mode). DCS-Control is an advanced regulation topology that combines the advantages of hysteretic, voltage mode, and current mode control. This control loop takes information about output voltage changes and feeds it directly to a fast comparator stage. The control loop sets the switching frequency, which is constant for steady-state operating conditions, and provides immediate response to dynamic load changes. To get accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low-ESR capacitors.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Mode Selection and Device Configuration (MODE/S-CONF)

With MODE/S-CONF (SmartConfig application), this device features an input with two functions. It can be used to customize the device behavior in two ways:

- Select the device mode (FPWM or auto PFM/PWM with AEE operation) traditionally with a HIGH- or LOW-level.
- Select the device configuration (switching frequency, internal/external feedback, output discharge, and PFM/PWM mode) by connecting a single resistor to the MODE/S-CONF pin.

The device interprets this pin during the start-up sequence after the internal OTP readout and before it starts switching in soft start. If the device reads a HIGH- or LOW-level, the dynamic mode change is active and PFM/PWM mode can be changed during operation. If the device reads a resistor value, there is no further interpretation during operation and device mode or other configurations cannot be changed afterward.

注

The MODE/S-CONF pin must not be left floating. Connect the pin high, low, or to a resistor to configure the device according to 表 7-2.

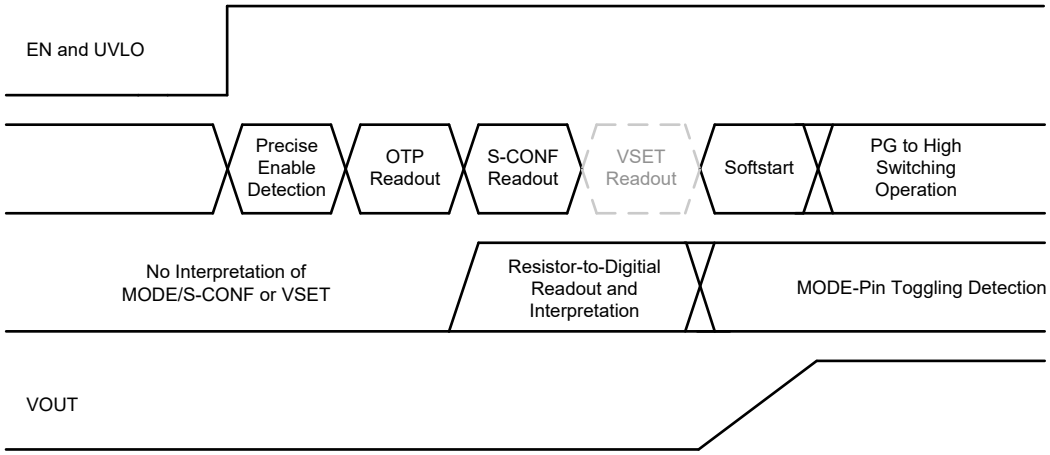


図 7-1. Interpretation of S-CONF and VSET Flow

注意

For each operating mode and switching frequency, the following V_{OUT} range is recommended:

表 7-1. Recommended V_{OUT} Ranges with Respect to MODE and F_{SW}

Mode	F_{SW} (MHz)	V_{OUT}
Auto PFM/PWM	1 MHz	0.4 V < V_{OUT} < 2.0 V
Forced PWM	1 MHz	0.4 V < V_{OUT} < 2.0 V
Auto PFM/PWM with AEE	2.5 MHz	0.4 V < V_{OUT}< 5.5 V
Forced PWM	2.5 MHz	2.0 V < V_{OUT} < 5.5 V

Failure to follow the recommended V_{OUT} ranges causes the device to malfunction.

表 7-2. SmartConfig™ Application Setting Table

#	Level Or Resistor Value [Ω] (1)	FB/VSET-Pin	F_{SW} (MHz)	Output Discharge	Mode (Auto or Forced PWM)	Dynamic Mode Change
	Setting Options by Level					
1	GND	external FB	2.5	yes	Auto PFM/PWM with AEE	active
2	HIGH (>V_{IH_MODE})	external FB	2.5	yes	Forced PWM	
	Setting Options by Resistor					
3	7.15 k	external FB	2.5	no	Auto PFM/PWM with AEE	not active
4	8.87 k	external FB	2.5	no	Forced PWM	
5	11.0 k	external FB	1	yes	Auto PFM/PWM	
6	13.7 k	external FB	1	yes	Forced PWM	
7	16.9 k	external FB	1	no	Auto PFM/PWM	
8	21.0 k	external FB	1	no	Forced PWM	
9	26.1 k	VSET	2.5	yes	Auto PFM/PWM with AEE	
10	32.4 k	VSET	2.5	yes	Forced PWM	
11	40.2 k	VSET	2.5	no	Auto PFM/PWM with AEE	
12	49.9 k	VSET	2.5	no	Forced PWM	
13	61.9 k	VSET	1	yes	Auto PFM/PWM	
14	76.8 k	VSET	1	yes	Forced PWM	
15	95.3 k	VSET	1	no	Auto PFM/PWM	
16	118 k	VSET	1	no	Forced PWM	

(1) E96 Resistor Series, 1% Accuracy, Temperature Coefficient better or equal than ±200 ppm/°C

7.3.2 Adjustable V_O Operation (External Voltage Divider)

The TPSM82902 can be programmed by the MODE/S-CONF pin to either classical configuration where the FB/VSET pin is used as the feedback pin, sensing V_O through an external resistive divider. The TPSM82902 can also be programmed to 16 different fixed output voltages. These are set through an external resistor between the FB/VSET pin and GND. In this configuration, V_O is directly sensed at the VOS internal terminal connection of the device.

If the device is configured to operate in classical adjustable V_O operation, the FB/VSET pin is used as the feedback pin and needs to sense V_O through an external divider network. 図 7-2 shows the typical schematic for this configuration.

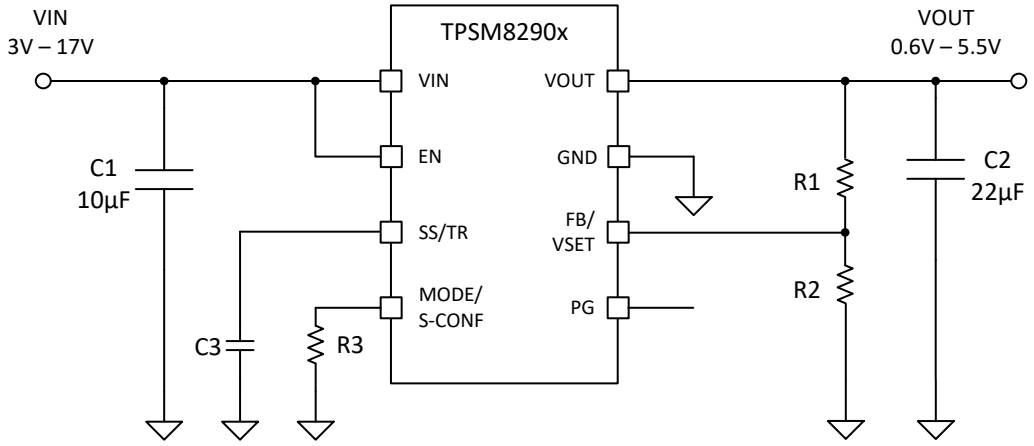


図 7-2. Adjustable V_O Operation Schematic

7.3.3 Setable V_O Operation (VSET and Internal Voltage Divider)

If the device is configured to VSET operation, V_O is sensed only through the internal VOS connection by an internal resistor divider. The target V_O is programmed by an external resistor connected between the VSET pin and GND. 図 7-3 shows the typical schematic for this configuration.

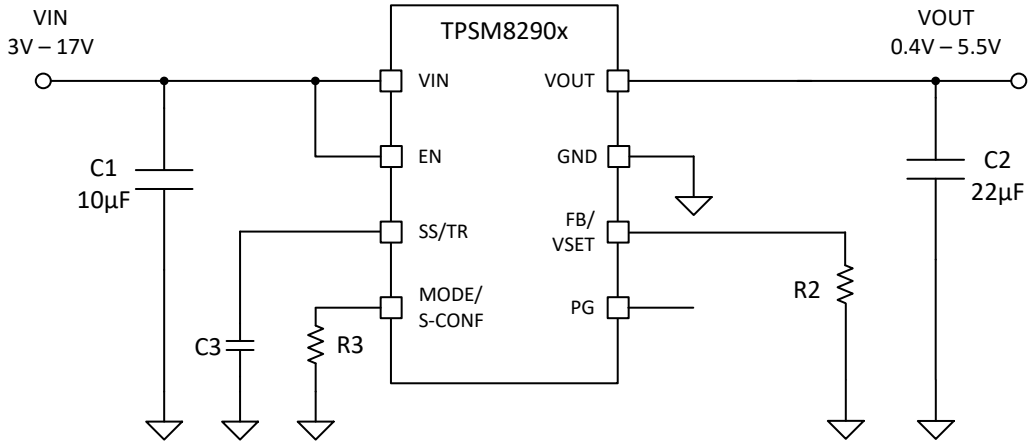


図 7-3. Setable V_O Operation Schematic

表 7-3. VSET Selection Table

#	Resistor Value [Ω]	Target V_O [V]
1	GND	1.2
2	4.64 k	0.4
3	5.76 k	0.6
4	7.15 k	0.8
5	8.87 k	1.0
6	11.0 k	1.1
7	13.7 k	1.3
8	16.9 k	1.35
9	21.0 k	1.8
10	26.1 k	1.9
11	40.2 k	2.5
12	61.9 k	3.8
13	76.8 k	5.0
14	95.3 k	5.1
15	118.0 k	5.5
16	249.00 k or larger/Open	3.3

7.3.4 Soft Start/Tracking (SS/TR)

With the SS/TR pin, it is possible to adjust the soft-start behavior and track an external voltage. See セクション 8.2.2.4 for operation details.

The internal soft-start circuitry controls the output voltage slope during start-up. This avoids excessive inrush current and makes sure there is a controlled output voltage rise time. It also prevents unwanted voltage drops from high impedance power sources or batteries. When EN is set high to start operation, the device starts switching after a delay, then the internal reference, and hence V_O, rises with a slope controlled by an external capacitor connected to the SS/TR pin.

Leaving the SS/TR pin unconnected provides the fastest start-up, limited internally (the pin must not be pulled LOW externally).

If the device is set to shut down (EN = GND), undervoltage lockout, or thermal shutdown, an internal resistor pulls the SS/TR pin down to ensure a proper low level. Returning from those states causes a new start-up sequence as set by the SS/TR connection.

A voltage supplied to SS/TR can be used to track a primary voltage. The output voltage follows this voltage up and down in forced PWM mode. In PFM mode, the output voltage decreases based on the load current.

7.3.5 Smart Enable with Precise Threshold

The voltage applied at the enable pin of the TPSM82902 is compared to a fixed threshold rising voltage, allowing the user to drive the pin by a slowly changing voltage and enables the use of an external RC network to achieve a power-up delay.

The precise enable input allows the user to program the undervoltage lockout by adding a resistor divider to the input of the enable pin.

The enable input threshold for a falling edge is lower than the rising edge threshold. The TPSM82902 starts operation when the rising threshold is exceeded. For proper operation, the EN pin must be terminated and must not be left floating. Pulling the EN pin low forces the device into shutdown. In this mode, the internal high-side and low-side MOSFETs are turned off and the entire internal control circuitry is switched off.

An internal resistor pulls the EN pin to GND when the device is disabled and avoids floating the pin after the device is enabled, the pulldown is removed. This prevents an uncontrolled start-up of the device in case the EN pin cannot be driven to a low level safely. With EN low, the device is in shutdown mode. The device is turned on with EN set to a high level. The pulldown control circuit disconnects the pulldown resistor on the EN pin after the internal control logic and the reference have been powered up. With EN set to a low level, the device enters shutdown mode and the pulldown resistor is activated again.

7.3.6 Power Good (PG)

The TPSM82902 has a built-in power-good (PG) feature to indicate whether the output voltage has reached its target and the device is ready. The PG signal can be used for start-up sequencing of multiple rails. The PG pin is an open-drain output that requires a pullup resistor to any voltage up to the recommended input voltage level. PG is low when the device is turned off due to EN, UVLO (undervoltage lockout), or thermal shutdown. V_{IN} must remain present for the PG pin to stay low.

If the power-good output is not used, it is recommended to tie to GND or leave it open.

表 7-4. Power Good Indicator Functional Table

Logic Signals				PG Status
V_I	EN Pin	Thermal Shutdown	V_O	
V_I > UVLO	HIGH	No	V_O on target	**High Impedance**
			V_O < target	**LOW**
		Yes	x	**LOW**
	LOW	x	x	**LOW**
1.8 V< V_I < UVLO	x	x	x	**LOW**
V_I < 1.8 V	x	x	x	**Undefined**

7.3.7 Undervoltage Lockout (UVLO)

If the input voltage drops, the undervoltage lockout prevents mis-operation of the device by switching off both the power FETs. The device is fully operational for voltages above the rising UVLO threshold and turns off if the input voltage trips below the threshold for a falling supply voltage.

7.3.8 Current Limit And Short Circuit Protection

The TPSM82902 is protected against overload and short circuit events. If the inductor current exceeds the high-side FET current limit (I_{LIMH}), the high-side switch is turned off and the low-side switch is turned on to ramp down the inductor current. The high-side FET turns on again only if the current in the low-side FET has decreased below the low-side FET current limit threshold.

Due to internal propagation delay, the actual current can exceed the static current limit during that time. The dynamic current limit is given as 式 1:

$$I_{peak(typ)} = I_{LIMH} + \frac{V_L}{L} \times t_{PD} \quad (1)$$

where

- I_{LIMH} is the static high-side FET current limit as specified in the *Electrical Characteristics*.
- L is the effective inductance at the peak current (approximately 0.9 µH).
- V_L is the voltage across the inductor ($V_{IN} – V_{OUT}$).
- t_{PD} is the internal propagation delay of typically 50 ns.

The current limit can exceed static values, especially if the input voltage is high and very small inductances are used. The dynamic high-side switch peak current can be calculated as follows:

$$I_{peak(typ)} = I_{LIMH} + \frac{VIN - VOUT}{L} \times 50ns \quad (2)$$

7.3.9 Thermal Shutdown

The junction temperature, T_J, of the device is monitored by an internal temperature sensor. If T_J rises and exceeds the thermal shutdown threshold, T_{SD}, the device shuts down. Both the high-side and low-side power FETs are turned off and PG goes low. When T_J decreases below the hysteresis, the converter resumes normal operation, beginning with soft start. During a PFM skip pause, the thermal shutdown feature is not active. A shutdown or re-start is only triggered during a switching cycle. See セクション 7.4.3.

7.4 Device Functional Modes

7.4.1 Pulse Width Modulation (PWM) Operation

The TPSM82902 has two operating modes: forced PWM mode discussed in this section and PWM/PFM as discussed in セクション 7.4.3.

With the MODE/S-CONF pin configured for PWM mode, the TPSM82902 operates with pulse width modulation in continuous conduction mode (CCM) with a nominal switching frequency of 2.5 MHz/1.0 MHz. The frequency variation in PWM is controlled and depends on V_{IN}, V_{OUT}, and the inductance. The on time in forced PWM mode is given by 式 3:

$$TON = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{sw}} \tag{3}$$

7.4.2 AEE (Automatic Efficiency Enhancement)

When the MODE/S-CONF pin is configured for AEE mode, the TPSM82902 provides the highest efficiency over the entire input voltage and output voltage range by automatically adjusting the switching frequency of the converter. This is achieved by setting the predictive off time of the converter. The efficiency of a switched mode converter is determined by the power losses during the conversion. The efficiency decreases if V_{OUT} decreases, V_{IN} increases as shown in 式 4, or both. In order to keep the efficiency high over the entire duty cycle range (V_{OUT}/V_{IN} ratio), the switching frequency is adjusted while maintaining the ripple current.

$$F_{sw}(MHz) = 10 \times V_{OUT} \times \frac{V_{IN} - V_{OUT}}{V_{IN}^{\ 2}} \tag{4}$$

The AEE function in the TPSM82902 adjusts the on time (TON) in power save mode, depending on the input voltage and the output voltage to maintain highest efficiency. The on time in steady-state operation can be estimated as using 式 5:

$$TON = 100 \times \frac{VIN}{VIN - VOUT}[ns] \tag{5}$$

式 6 shows the relationship among the inductor ripple current, switching frequency, and duty cycle.

$$\Delta I_L = V_{OUT} \times \left(\frac{1-D}{L \times f_{SW}}\right) = V_{OUT} \times \left(\frac{1-\left(\frac{V_{OUT}}{V_{IN}}\right)}{L \times f_{SW}}\right) \tag{6}$$

Efficiency increases by decreasing switching losses and preserving high efficiency for varying duty cycles, while the ripple current amplitude remains low enough to deliver the full output current without reaching current limit. The AEE feature provides an efficiency enhancement for various duty cycles, especially for lower V_{OUT} values where fixed frequency converters suffer from a significant efficiency drop. Furthermore, this feature compensates for the very small duty cycles of high V_{IN} to low V_{OUT} conversion, which limits the control range in other topologies.

7.4.3 Power Save Mode Operation (Auto PFM/PWM)

When the MODE/S-CONF pin is configured for power save mode (auto PFM/PWM), the device operates in PWM mode as long the output current is higher than half of the ripple current of the inductor. To maintain high efficiency at light loads, the device enters power save mode at the boundary to discontinuous conduction mode (DCM). This happens if the output current becomes smaller than half of the ripple current of the inductor. The power save mode is entered seamlessly when the load current decreases. This makes sure there is a high efficiency in light load operation. The device remains in power save mode as long as the inductor current is discontinuous.

In power save mode, the switching frequency decreases linearly with the load current maintaining high efficiency. The transition in and out of power save mode is seamless in both directions.

In addition to adjusting the switching, the TPSM82902 adjusts the on time (TON) in power save mode, depending on the input voltage and the output voltage to maintain the highest efficiency using the AEE function when 2.5 MHz is selected as described in セクション 7.4.2.

In power save mode, the TON time can be estimated using 式 3 for 1 MHz and 式 5 for 2.5 MHz (given the AEE is enabled for 2.5 MHz).

For very small output voltages, an absolute minimum on time of about 50 ns is kept to limit switching losses. The operating frequency is thereby reduced from its nominal value, which keeps efficiency high. Using TON, the typical peak inductor current in power save mode is approximated by 式 7:

$$ILPSM_{(peak)} = \frac{(VIN - VOUT)}{L} \times TON \tag{7}$$

There is a minimum off time that limits the duty cycle of the TPSM82902. When V_{IN} decreases to typically 15% above V_{OUT}, the TPSM82902 does not enter power save mode, regardless of the load current. The device maintains output regulation in PWM mode.

The output voltage ripple in power save mode is given by 式 8:

$$\Delta V = \frac{L \times VIN^2}{200 \times C}\left(\frac{1}{VIN - VOUT} + \frac{1}{VOUT}\right) \tag{8}$$

where

- L is the effective inductance (approximately 0.9 µF).
- C is the output effective capacitance.

7.4.4 100% Duty-Cycle Operation

The duty cycle of the buck converter operating in PWM mode is given as D = V_{OUT}/V_{IN}. The duty cycle increases as the input voltage comes close to the output voltage and the off time gets smaller. When the minimum off time of typically 80 ns is reached, the TPSM82902 scales down its switching frequency while it approaches 100% mode. In 100% mode, the device keeps the high-side switch on continuously. The high-side switch stays turned on as long as the output voltage is below the internal set point. This allows the conversion of small input to output voltage differences (for example, getting longest operation time of battery-powered applications). In 100% duty cycle mode, the low-side FET is switched off.

The minimum input voltage to maintain output voltage regulation, depending on the load current and the output voltage level, can be calculated as:

$$VIN_{(min)} = VOUT + IOUT\left(R_{DS(on)} + R_L\right) \tag{9}$$

where

- I_{OUT} is the output current.
- $R_{DS(on)}$ is the on-state resistance of the high-side FET.
- R_L is the DC resistance of the inductor used (approximately 40 mΩ).

7.4.5 Output Discharge Function

The purpose of the discharge function is to ensure a defined down-ramp of the output voltage when the device is being disabled but also to keep the output voltage close to 0 V when the device is off. The output discharge feature is only active after the TPSM82902 has been enabled at least once since the supply voltage was applied. The internal discharge resistor is connected to the VOS pin. The discharge function is enabled as soon

as the device is disabled, in thermal shutdown, or in undervoltage lockout. The minimum supply voltage required for the discharge function to remain active typically is 2 V.

7.4.6 Starting into a Pre-Biased Load

The TPSM82902 is capable of starting into a pre-biased output. The device only starts switching when the internal soft-start ramp is equal or higher than the feedback voltage. If the voltage at the feedback pin is biased to a higher voltage than the nominal value, the TPSM82902 does not start switching unless the voltage at the feedback pin drops to the target.

8 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPSM82902 device is highly efficient, small, and flexible synchronous step-down DC-DC converter MicroSiP package module that is easy to use. A wide input voltage range of 3 V to 17 V supports a wide variety of inputs like 12-V supply rails, single-cell or multi-cell Li-Ion, and 5-V or 3.3-V rails.

8.2 Typical Application with Adjustable Output Voltage

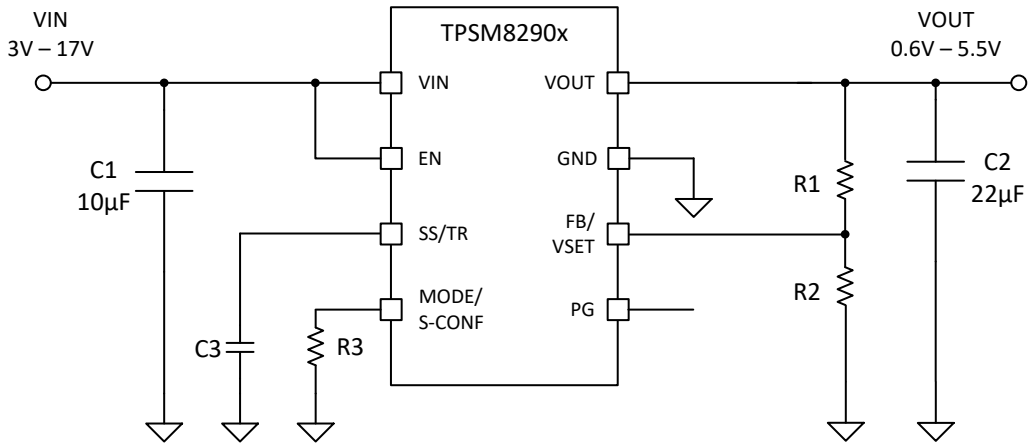

図 8-1. Typical Application Circuit

8.2.1 Design Requirements

表 8-1. List of Components

Reference	Description	Manufacturer
IC	17 V, 3-A Step-Down Converter	TPSM8290x series; Texas Instruments
CIN	10 µF, 25 V, Ceramic, 0805	C3216X7R1E106M160AE, TDK
COUT	22 µF, 16 V, Ceramic, 0805	C2012X7S1A226M125AC, TDK
CSS	Depends on soft start time; see セクション 8.2.2.3.3.	16 V, Ceramic, X7R
R1	Depending on V_{OUT}; see セクション 8.2.2.2.	Standard 1% metal film
R2	Depending on V_{OUT}; see セクション 8.2.2.2.	Standard 1% metal film
R3	Depending on device setting, see セクション 7.3.1.	Standard 1% metal film

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM82902 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Programming the Output Voltage

The output voltage of the TPSM82902 is adjustable. It can be programmed for output voltages from 0.6 V to 5.5 V using a resistor divider from V_{OUT} to GND. The voltage at the FB pin is regulated to 600 mV. The value of the output voltage is set by the selection of the resistor divider from 式 10. It is recommended to choose resistor values that allow a current of at least 2 µA, meaning the value of R2 must not exceed 400 kΩ. Lower resistor values are recommended for highest accuracy and most robust design.

$$R_1 = R_2 \times \left(\frac{VOUT}{VFB} - 1 \right) \tag{10}$$

With typical VFB = 0.6 V, 1-MHz switching frequency is not recommended for V_{OUT} > 1.8 V.

表 8-2. Setting the Output Voltage

Nominal Output Voltage	R1	R2	Exact Output Voltage
0.75 V	24.9 kΩ	100 kΩ	0.749 V
1.2 V	100 kΩ	100 kΩ	1.2 V
1.5 V	150 kΩ	100 kΩ	1.5 V
1.8 V	200 kΩ	100 kΩ	1.8 V
2.0 V	49.9 kΩ	21.5 kΩ	1.992 V
2.5 V	100 kΩ	31.6 kΩ	2.498 V
3.0 V	100 kΩ	24.9 kΩ	3.009 V
3.3 V	113 kΩ	24.9 kΩ	3.322 V
5.0 V	182 kΩ	24.9 kΩ	4.985 V

8.2.2.3 Capacitor Selection

8.2.2.3.1 Output Capacitor

The recommended value for the output capacitor is 22 µF. Output capacitance above 100 µF needs to have a ESR of ≥ 10 mΩ for stable operation. The architecture of the TPSM82902 allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, use X7R or X5R dielectric. Using a higher value has advantages like smaller voltage ripple and a tighter DC output accuracy in power save mode (see the *Optimizing the TPS62130/40/50/60 Output Filter* application report).

In power save mode, the output voltage ripple depends on the output capacitance, its ESR, ESL, and the peak inductor current. Using ceramic capacitors provides small ESR, ESL, and low ripple. The output capacitor needs to be as close as possible to the device.

For large output voltages, the DC bias effect of ceramic capacitors is large and the effective capacitance must be observed.

8.2.2.3.2 Input Capacitor

For most applications, 10 µF nominal is sufficient and is recommended, though a larger value reduces input current ripple further. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. A low-ESR multilayer ceramic capacitor (MLCC) is recommended for best filtering and must be placed between VIN and GND as close as possible to those pins.

表 8-3. List of Capacitors

Type (1)	Nominal Capacitance [µF]	Voltage Rating [V]	Size	Manufacturer
C3216X7R1E106K160AB	10	25	0805	TDK
C2012X7S1A226M125AC	22	10	0805	TDK

(1) Lower of I_{RMS} at 40°C rise or I_{SAT} at 30% drop

8.2.2.3.3 Soft-Start Capacitor

A capacitor connected between SS/TR pin and GND allows a user-programmable start-up slope of the output voltage.

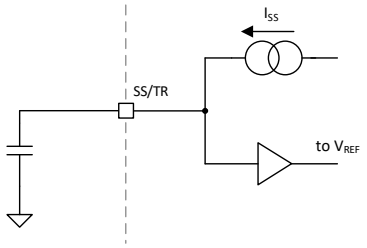

図 8-2. Soft-Start Operation Simplified Schematic

An internal constant current source is provided to charge the external capacitance. The capacitor required for a given soft-start ramp time is given by:

$$C_{SS} = T_{SS} \times \frac{I_{SS}}{V_{REF}} \tag{11}$$

where

- C_{SS} is the capacitance required at the SS/TR pin.
- T_{SS} is the desired soft-start ramp time.
- I_{SS} is the SS/TR source current, see the *Electrical Characteristics*.
- V_{REF} is the feedback regulation voltage divided by tracking gain (V_{FB}/0.75), see the *Electrical Characteristics*.

The fastest achievable typical ramp time is 150 µs even if the external C_{ss} capacitance is lower than 680 pF or the pin is open.

8.2.2.4 Tracking Function

If a tracking function is desired, the SS/TR pin can be used for this purpose by connecting it to an external tracking voltage. The output voltage tracks that voltage with the typical gain and offset as specified in the *Electrical Characteristics*.

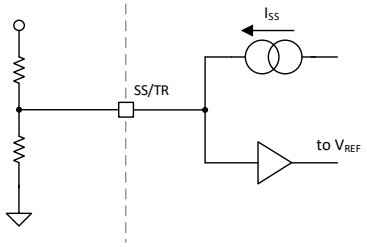

図 8-3. Tracking Operation Simplified Schematic

$$V_{FB} = 0.75 \times V_{SS/TR} \tag{12}$$

When the SS/TR pin voltage is above 0.8 V, the internal voltage is clamped and the device goes to normal regulation. This works for rising and falling tracking voltages with the same behavior, as long as the input voltage is inside the recommended operating conditions. For decreasing SS/TR pin voltage in PFM mode, the device does not sink current from the output. The resulting decrease of the output voltage can therefore be slower than the SS/TR pin voltage if the load is light. When driving the SS/TR pin with an external voltage, do not exceed the voltage rating of the SS/TR pin, which is 6 V. The SS/TR pin is internally connected with a resistor to GND when EN = 0.

If the input voltage drops below undervoltage lockout, the output voltage goes to zero, independent of the tracking voltage. 図 8-4 shows how to connect devices to get ratiometric and simultaneous sequencing by using the tracking function.

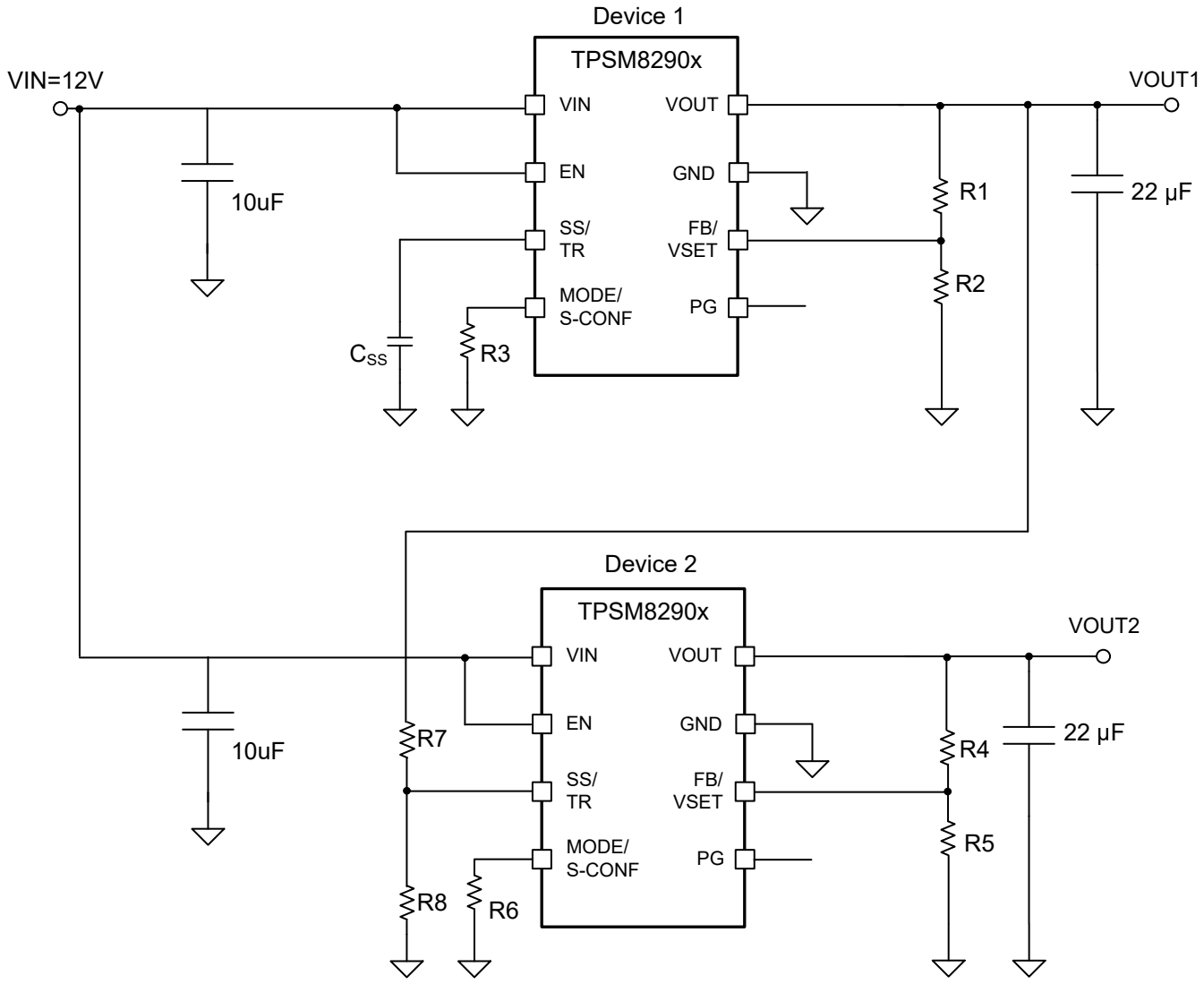

図 8-4. Schematic for Ratiometric and Simultaneous Start-Up

The resistive divider of R7 and R8 can be used to change the ramp rate of VOUT2 to be faster, slower, or the same as VOUT1.

A sequential start-up is achieved by connecting the PG pin of VOUT of device 1 to the EN pin of device 2. PG requires a pullup resistor. Ratiometric start-up sequence happens if both supplies are sharing the same soft-start capacitor. 式 11 gives the soft-start time, though the SS/TR current has to be doubled. Details about these and other tracking and sequencing circuits are found in *Sequencing and Tracking With the TPS621-Family and TPS821-Family* application report.

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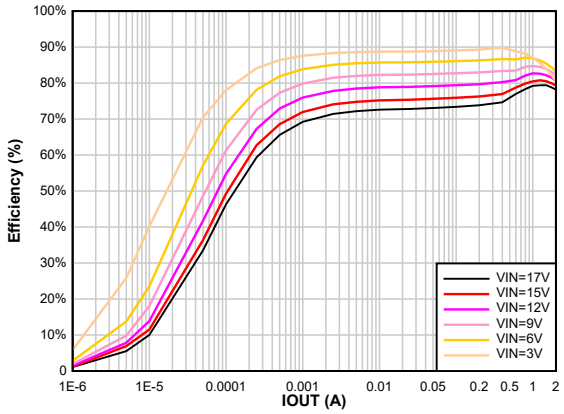
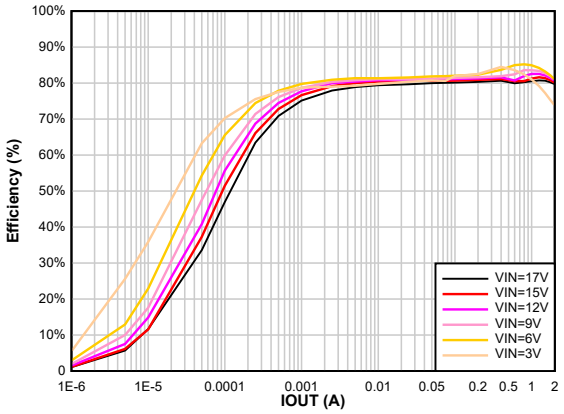
If the voltage at the FB pin is below its typical value of 0.6 V, the output voltage accuracy can have a wider tolerance than specified. The current of 2.5 µA out of the SS/TR pin also has an influence on the tracking function, especially for high resistive external voltage dividers on the SS/TR pin.

8.2.3 Application Curves



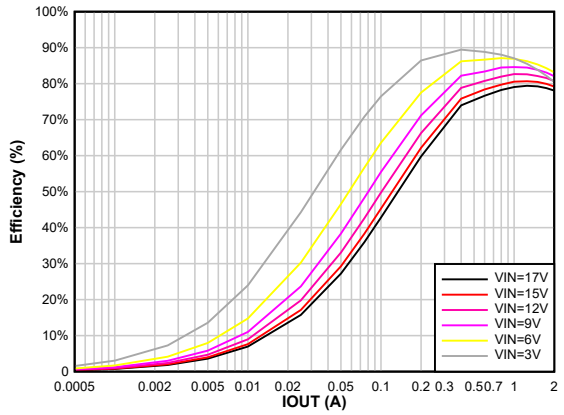
Auto PFM/PWM F_{sw} = 1 MHz

図 8-5. Efficiency vs Output Current V_{OUT} = 1.2 V



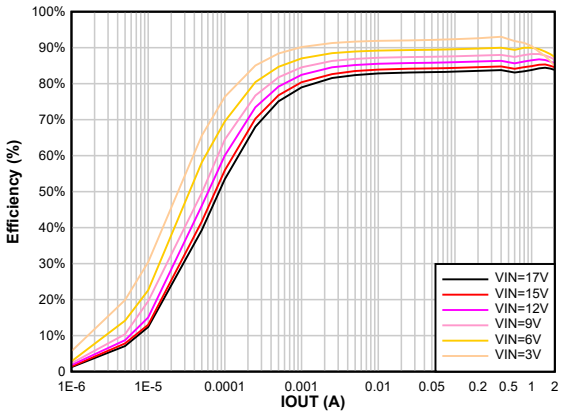
Auto PFM/PWM F_{sw} = 2.5 MHz

図 8-6. Efficiency vs Output Current V_{OUT} = 1.2 V



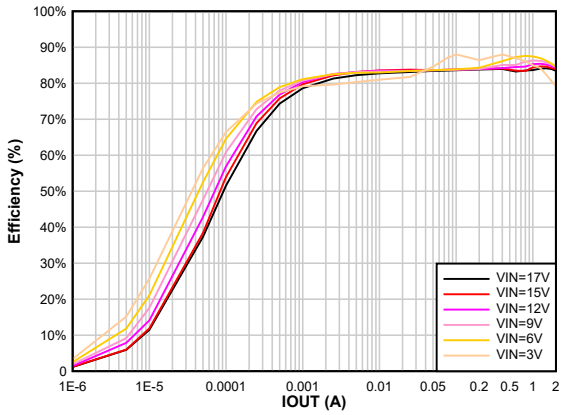
FPWM F_{sw} = 1 MHz

図 8-7. Efficiency vs Output Current V_{OUT} = 1.2 V



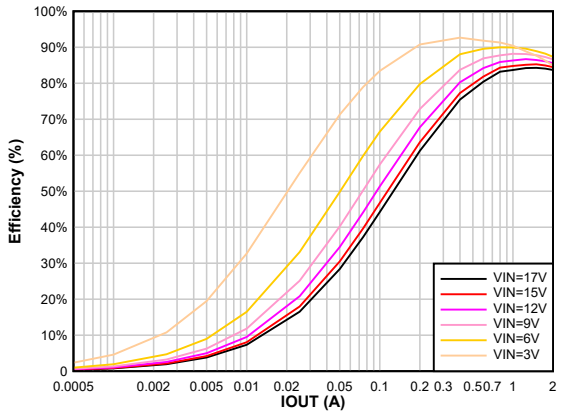
Auto PFM/PWM F_{sw} = 1 MHz

図 8-8. Efficiency vs Output Current V_{OUT} = 1.8 V



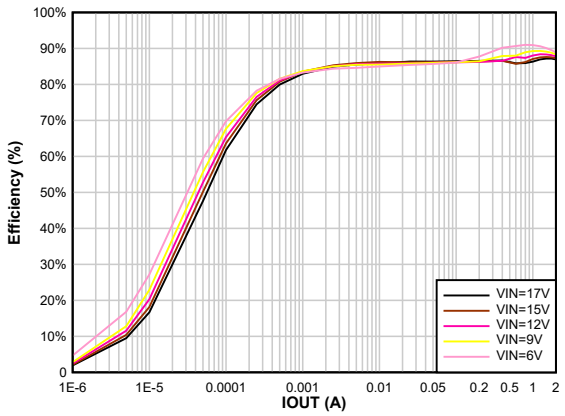
Auto PFM/PWM F_{sw} = 2.5 MHz

図 8-9. Efficiency vs Output Current V_{OUT} = 1.8 V



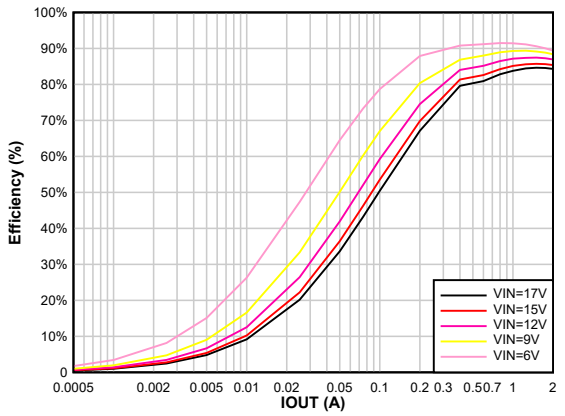
FPWM F_{sw} = 1 MHz

図 8-10. Efficiency vs Output Current V_{OUT} = 1.8 V



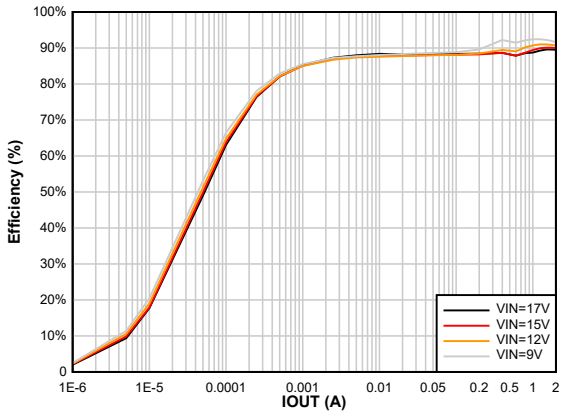
Auto PFM/PWM F_{sw} = 2.5 MHz

図 8-11. Efficiency vs Output Current V_{OUT} = 3.3 V



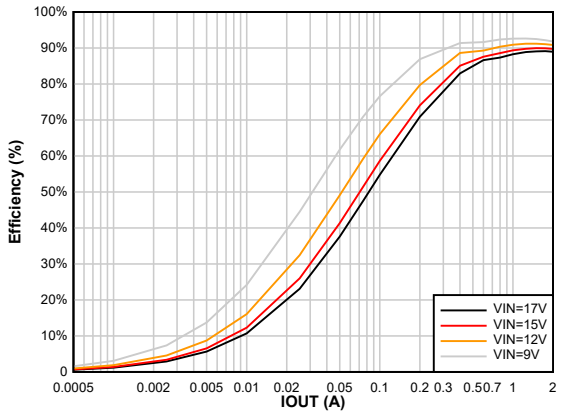
FPWM F_{sw} = 2.5 MHz

図 8-12. Efficiency vs Output Current V_{OUT} = 3.3 V



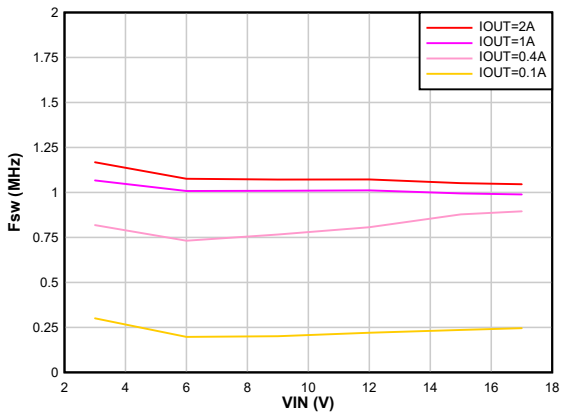
Auto PFM/PWM F_{sw} = 2.5 MHz

図 8-13. Efficiency vs Output Current V_{OUT} = 5.5 V



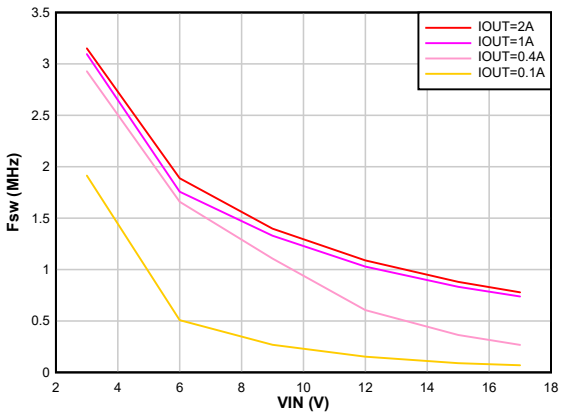
FPWM F_{sw} = 2.5 MHz

図 8-14. Efficiency vs Output Current V_{OUT} = 5.5 V



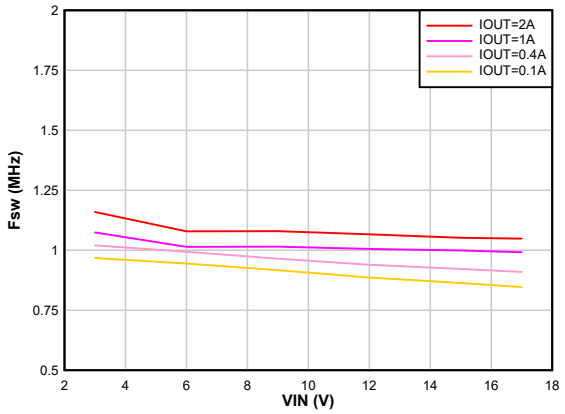
Auto PFM/PWM F_{sw} = 1 MHz

図 8-15. Switching Frequency vs Input Voltage V_{OUT} = 1.2 V



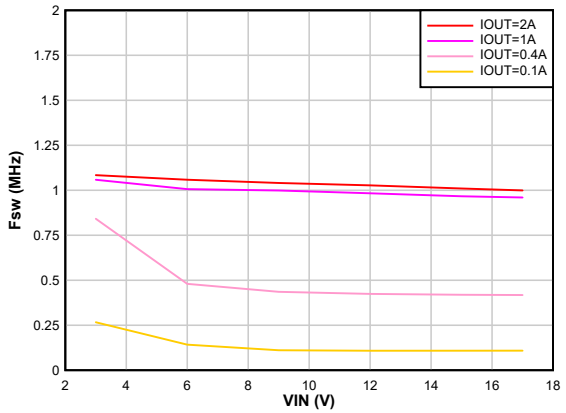
Auto PFM/PWM F_{sw} = 2.5 MHz

図 8-16. Switching Frequency vs Input Voltage V_{OUT} = 1.2 V



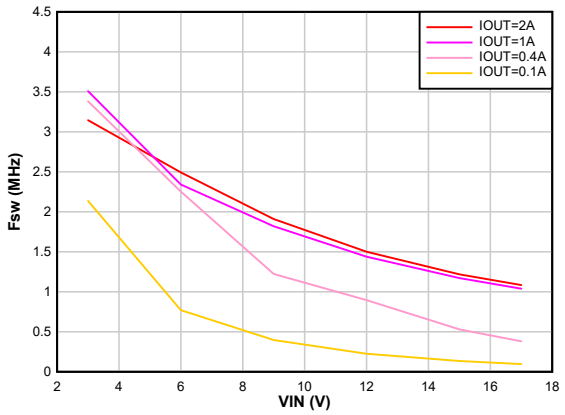
FPWM F_{sw} = 1 MHz

図 8-17. Switching Frequency vs Input Voltage V_{OUT} = 1.2 V



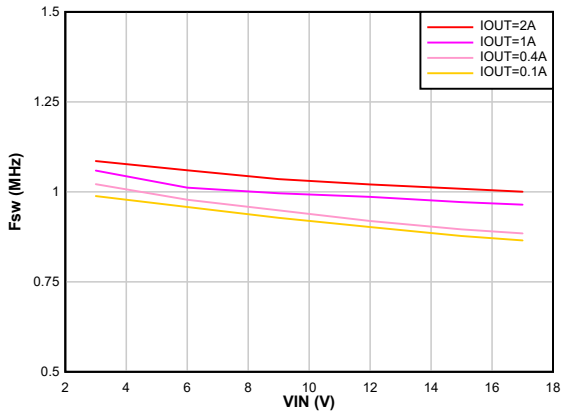
Auto PFM/PWM F_{sw} = 1 MHz

図 8-18. Switching Frequency vs Input Voltage V_{OUT} = 1.8 V



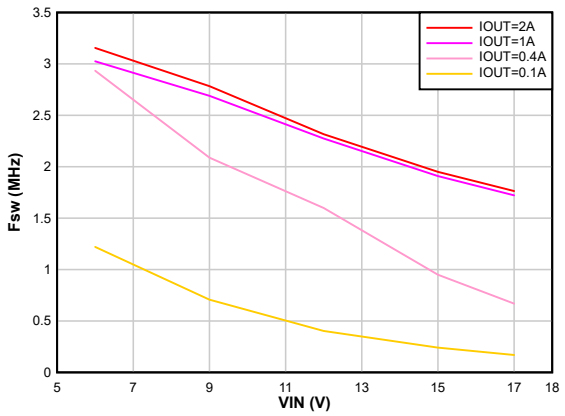
Auto PFM/PWM F_{sw} = 2.5 MHz

図 8-19. Switching Frequency vs Input Voltage V_{OUT} = 1.8 V



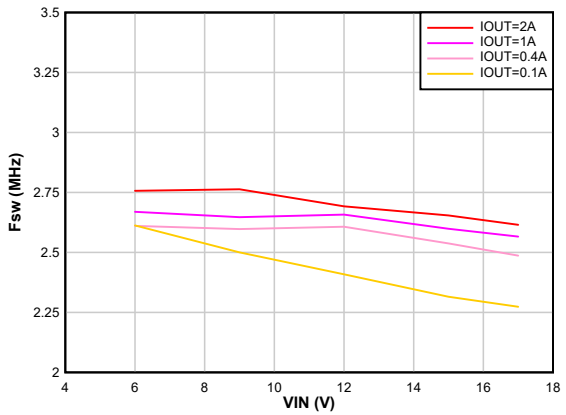
FPWM F_{sw} = 1 MHz

図 8-20. Switching Frequency vs Input Voltage V_{OUT} = 1.2 V



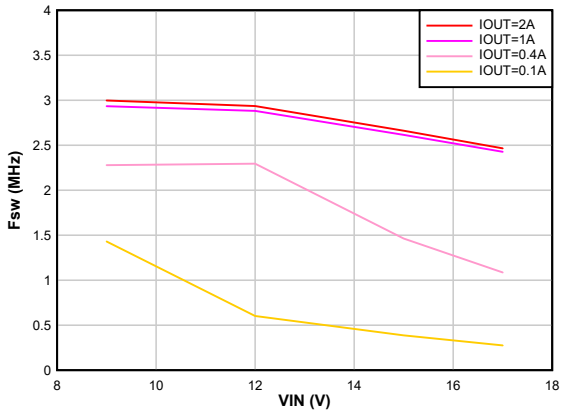
Auto PFM/PWM F_{sw} = 2.5 MHz

図 8-21. Switching Frequency vs Input Voltage V_{OUT} = 3.3 V



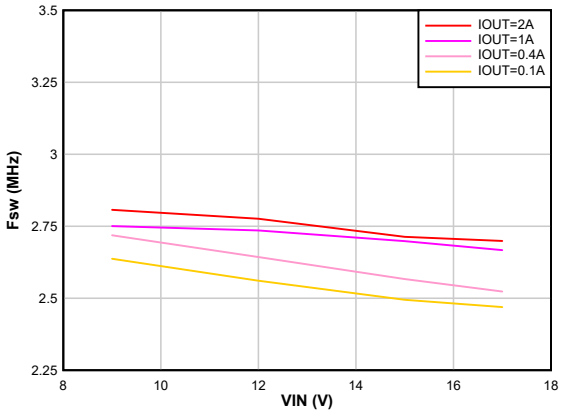
FPWM F_{sw} = 2.5 MHz

図 8-22. Switching Frequency vs Input Voltage V_{OUT} = 3.3 V



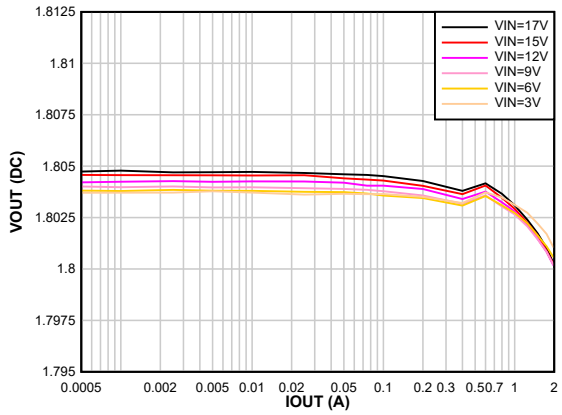
Auto PFM/PWM F_{sw} = 2.5 MHz

図 8-23. Switching Frequency vs Input Voltage V_{OUT} = 5.5 V



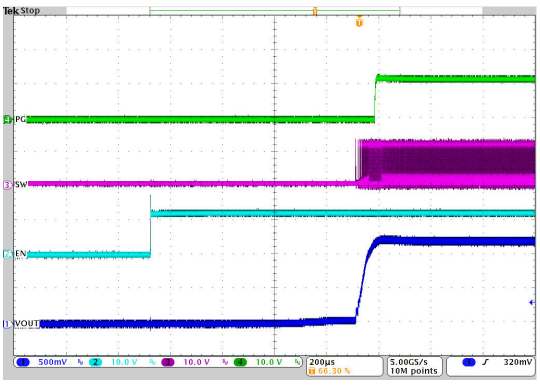
FPWM F_{sw} = 2.5 MHz

図 8-24. Switching Frequency vs Input Voltage V_{OUT} = 5.5 V



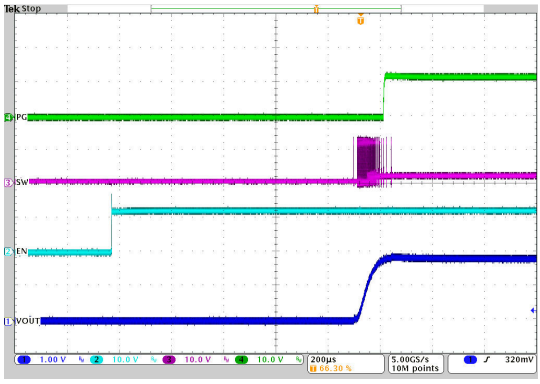
FPWM F_{sw} = 1 MHz

図 8-25. Output Voltage vs Output Current V_{OUT} = 1.8 V



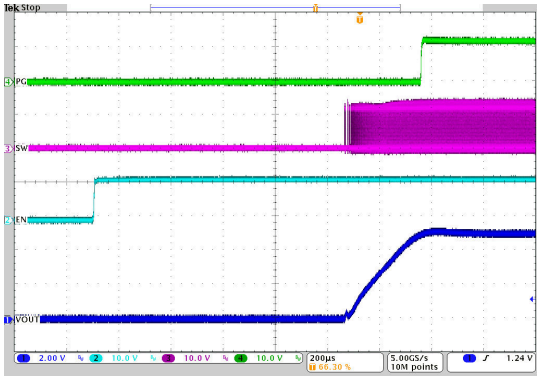
V_{IN} = 12 V 1-MHz FPWM I_O = 0 mA
V_{OUT} = 1.2 V T_A = 25°C

図 8-26. Start-Up Timing



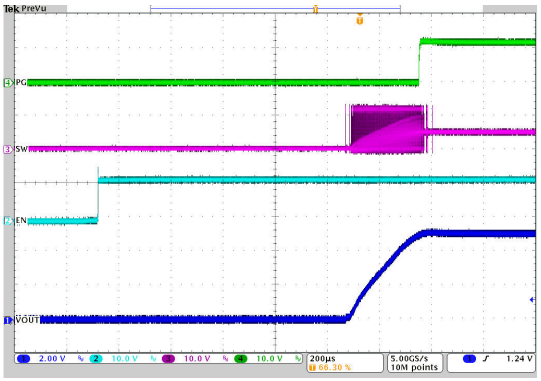
V_{IN} = 12 V 1-MHz Auto PFM/PWM I_O = 1 A
V_{OUT} = 1.8 V T_A = 25°C

図 8-27. Start-Up Timing



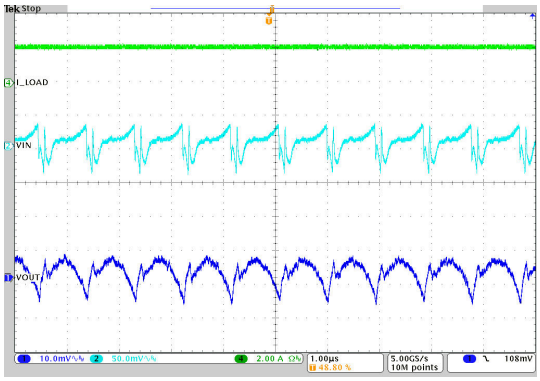
V_{IN} = 12 V 2.5-MHz FPWM I_O = 1 A
V_{OUT} = 5 V T_A = 25°C

図 8-28. Start-Up Timing



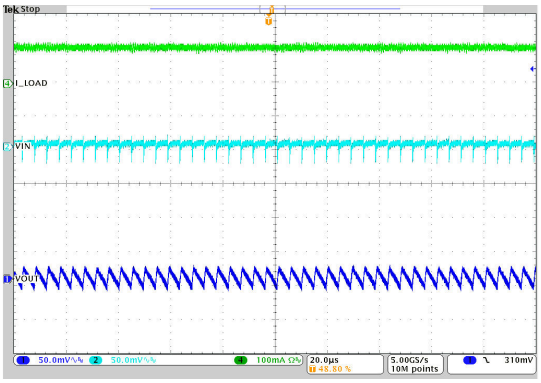
V_{IN} = 12 V　2.5-MHz PFM/PWM　I_O = 1 A
V_{OUT} = 5 V　T_A = 25°C

図 8-29. Start-Up Timing



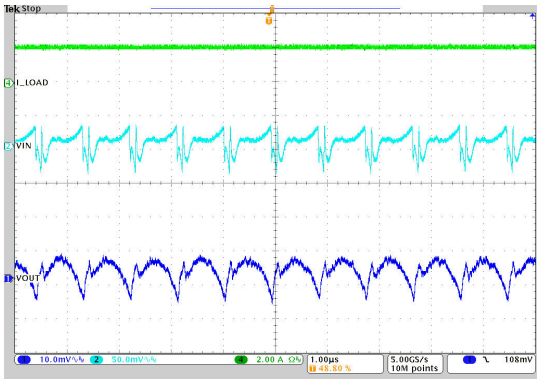
V_{IN} = 12 V　1-MHz Auto PFM/PWM　I_O = 2 A
V_{OUT} = 1.2 V　T_A = 25°C

図 8-30. Output Voltage Ripple



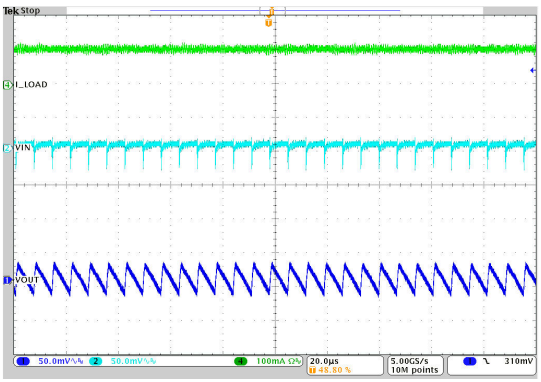
V_{IN} = 12 V　1-MHz Auto PFM/PWM　I_O = 0.1 A
V_{OUT} = 1.2 V　T_A = 25°C

図 8-31. Output Voltage Ripple



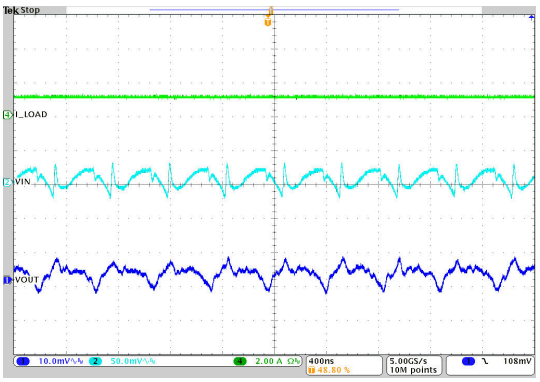
V_{IN} = 12 V　2.5-MHz Auto PFM/PWM　I_O = 2 A
V_{OUT} = 1.2 V　T_A = 25°C

図 8-32. Output Voltage Ripple



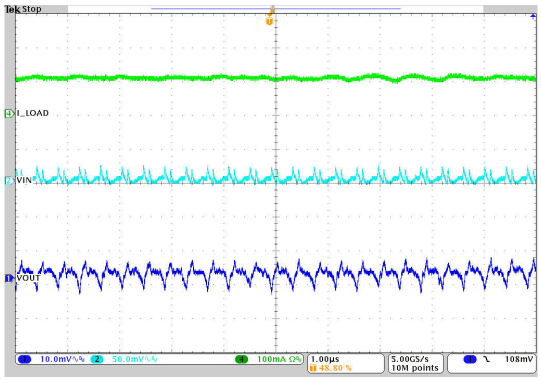
V_{IN} = 12 V　2.5-MHz Auto PFM/PWM　I_O = 0.1 A
V_{OUT} = 1.2 V　T_A = 25°C

図 8-33. Output Voltage Ripple



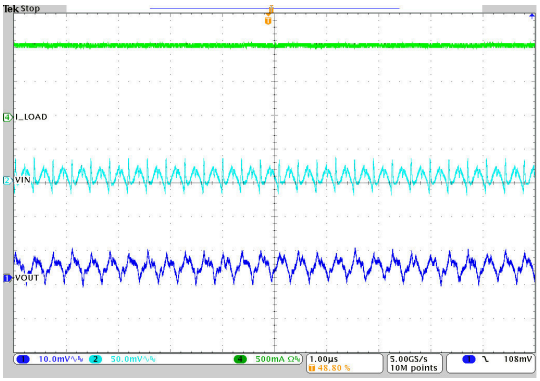
V_{IN} = 12 V　2.5-MHz Auto PFM/PWM　I_O = 1 A
V_{OUT} = 3.3 V　T_A = 25°C

図 8-34. Output Voltage Ripple



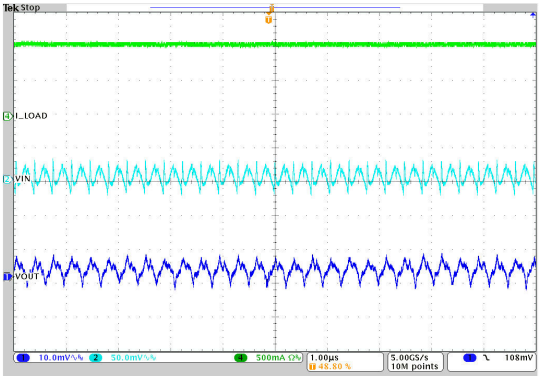
V_{IN} = 12 V　2.5-MHz FPWM　I_O = 0.1 A
V_{OUT} = 3.3 V　T_A = 25°C

図 8-35. Output Voltage Ripple



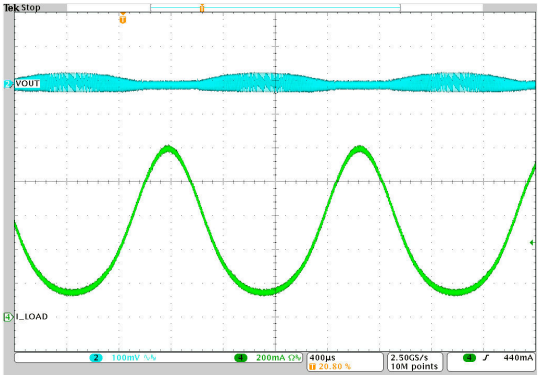
V_{IN} = 12 V　2.5-MHz FPWM　I_O = 1 A
V_{OUT} = 5.0 V　T_A = 25°C

図 8-36. Output Voltage Ripple



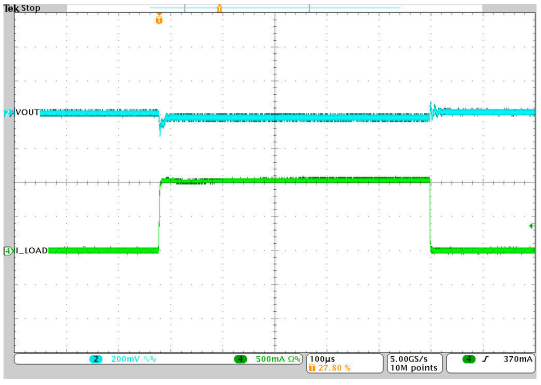
V_{IN} = 12 V　2.5-MHz Auto PFM/PWM
V_{OUT} = 5.0 V　I_O = 1 A　T_A = 25°C

図 8-37. Output Voltage Ripple



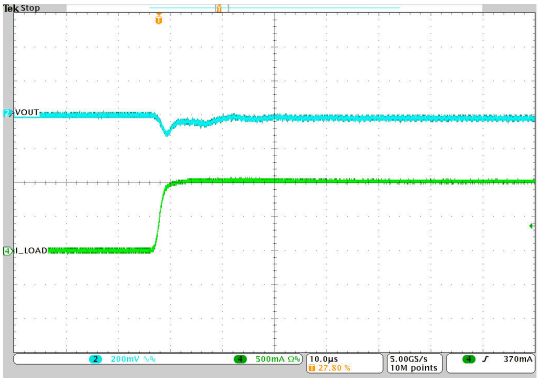
V_{IN} = 12 V　1-MHz Auto PFM/PWM　I_O = 0.1 A to 1 A
V_{OUT} = 1.2 V　T_A = 25°C

図 8-38. PSM-to-PWM Transition



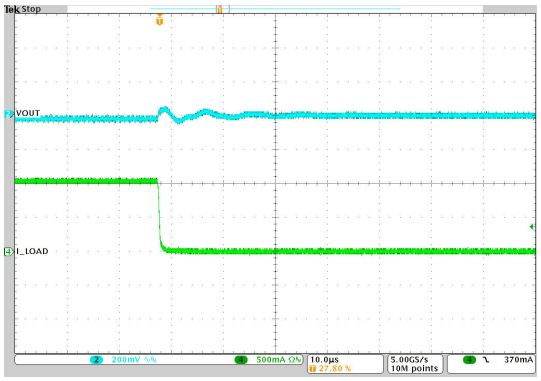
V_{IN} = 12 V　1-MHz Auto PFM/PWM　I_O = 5 mA to 1 A to 5 mA
V_{OUT} = 1.2 V　T_A = 25°C

図 8-39. Load Transient Response



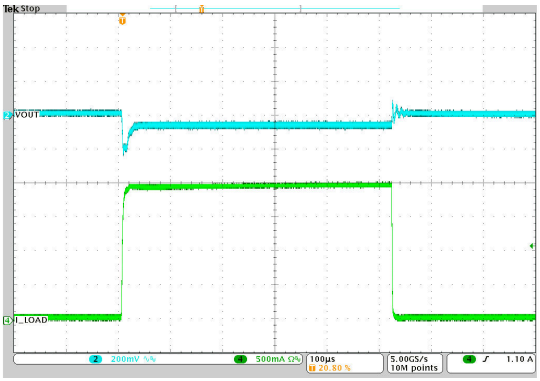
V_{IN} = 12 V　1-MHz Auto PFM/PWM　I_O = 5 mA to 1 A
V_{OUT} = 1.2 V　T_A = 25°C

図 8-40. Load Transient Response – Rising Edge



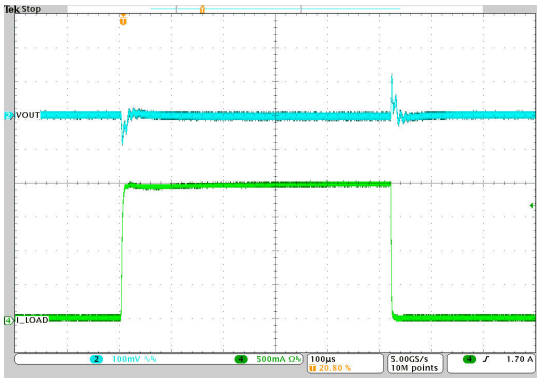
V_{IN} = 12 V　1-MHz Auto PFM/PWM　I_O = 1 A to 5 mA
V_{OUT} = 1.2 V　T_A = 25°C

図 8-41. Load Transient Response – Falling Edge



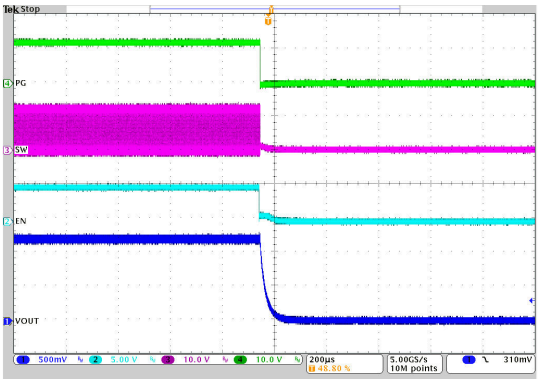
V_{IN} = 12 V　I_O = 5 mA to 2 A to 5 mA
V_{OUT} = 3.3 V　2.5-MHz Auto PFM/PWM　T_A = 25°C

図 8-42. Load Transient Response



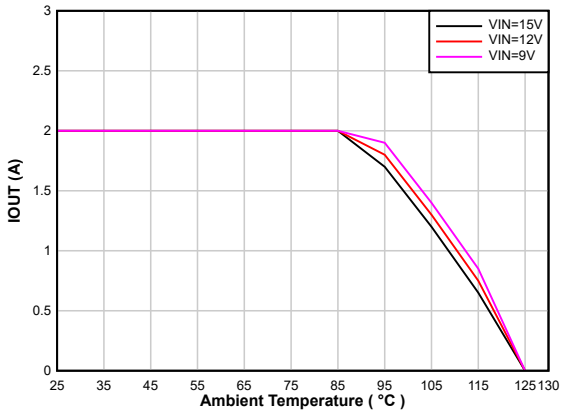
V_{IN} = 12 V　2.5-MHz FPWM　I_O = 5 mA to 2 A to 5 mA
V_{OUT} = 3.3 V　T_A = 25°C

図 8-43. Load Transient Response



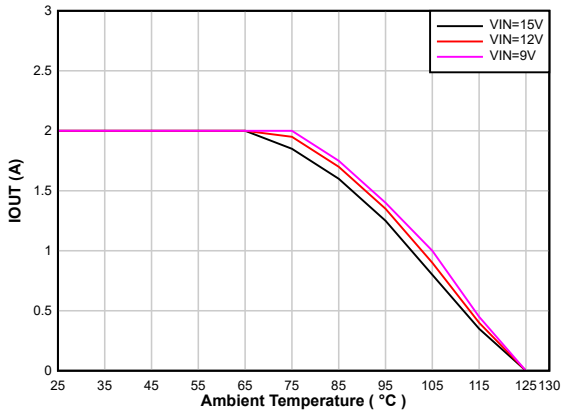
V_{IN} = 12 V　Output Discharge = Yes
V_{OUT} = 1.2 V　T_A = 25°C

図 8-44. Output Discharge Function – Enabled



Auto PFM/PWM　F_{sw} = 2.5 MHz

図 8-45. Thermal Derating V_{OUT} = 1.2 V



Auto PFM/PWM　F_{sw} = 2.5 MHz

図 8-46. Thermal Derating V_{OUT} = 3.3 V

8.3 Typical Application with Setable V_O Using VSET

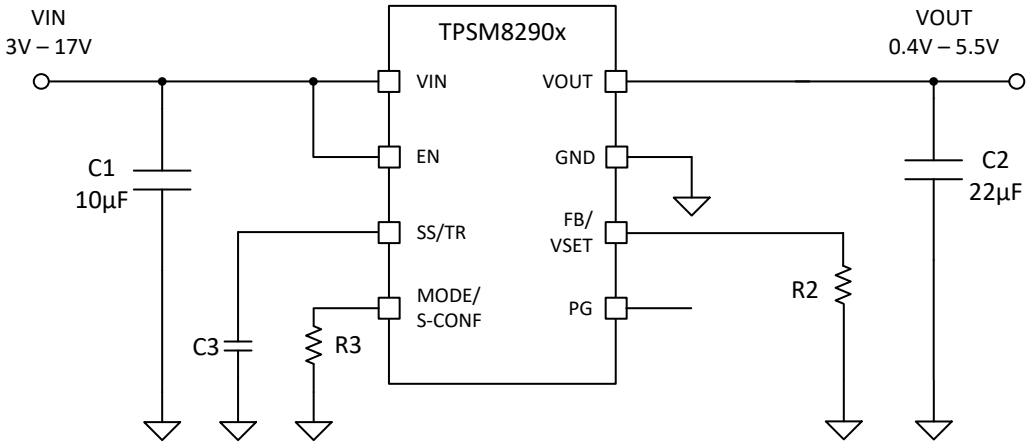


図 8-47. Typical Application Circuit (VSET)

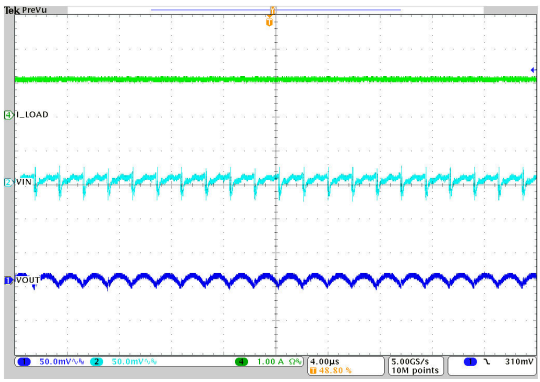
8.3.1 Design Requirements

VSET allows the user to set the output voltage using only one resistor to ground on the FB/VSET pin. 表 7-3 shows the 16 available options.

8.3.2 Detailed Design Procedure

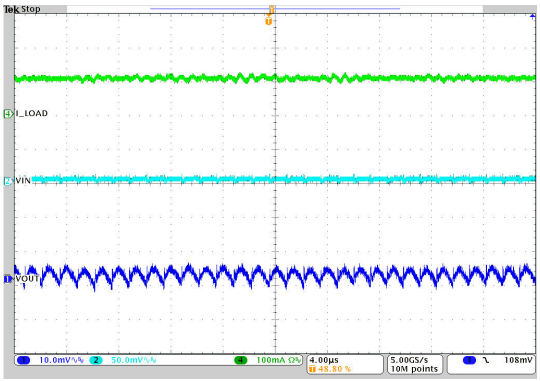
The VSET option needs to be selected using the MODE/S-CONF pin. After the device is configured to VSET operation, V_O is sensed only through the VOS pin by an internal resistor divider. The target V_O is programmed by an external resistor R2 connected between FB/VSET and GND.

8.3.3 Application Curves



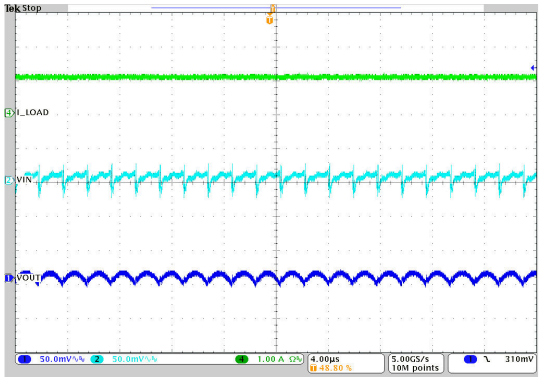
V_{IN} = 12 V　1-MHz Auto　I_O = 1 A
V_{OUT} = 0.4 V　PFM/PWM　T_A = 25°C

図 8-48. Output Voltage Ripple



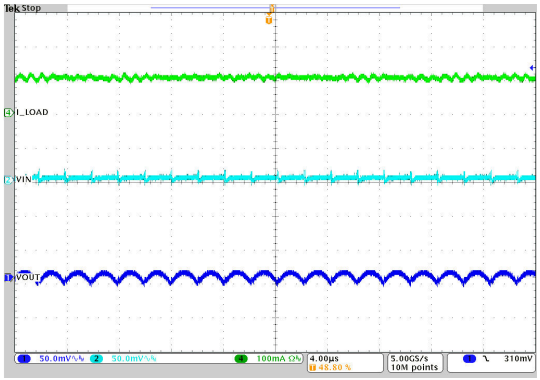
V_{IN} = 12 V　1-MHz Auto　I_O = 100 mA
V_{OUT} = 0.4 V　PFM/PWM　T_A = 25°C

図 8-49. Output Voltage Ripple



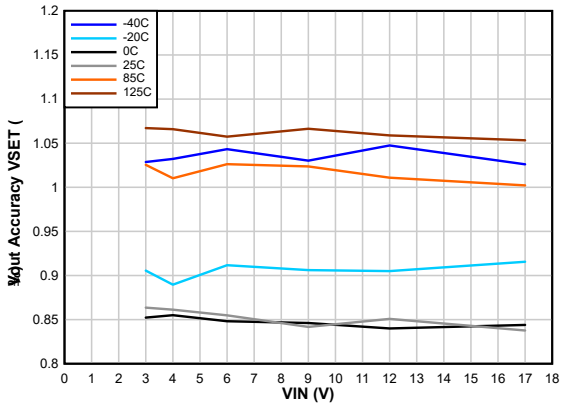
V_{IN} = 12 V　1-MHz FPWM　I_O = 1 A
V_{OUT} = 0.4 V　T_A = 25°C

図 8-50. Output Voltage Ripple



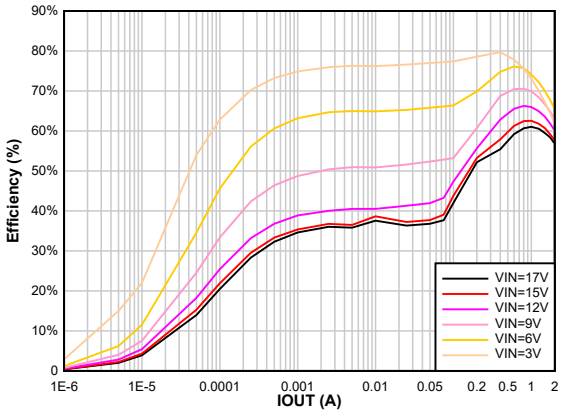
V_{IN} = 12 V　1-MHz FPWM　I_O = 100 mA
V_{OUT} = 0.4 V　T_A = 25°C

図 8-51. Output Voltage Ripple



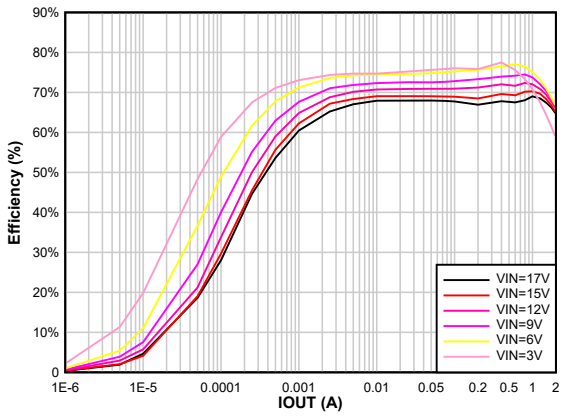
V_{IN} = 3 V–17 V　Temp = –40°C to 150°C

図 8-52. Output Voltage Accuracy – VSET Selected



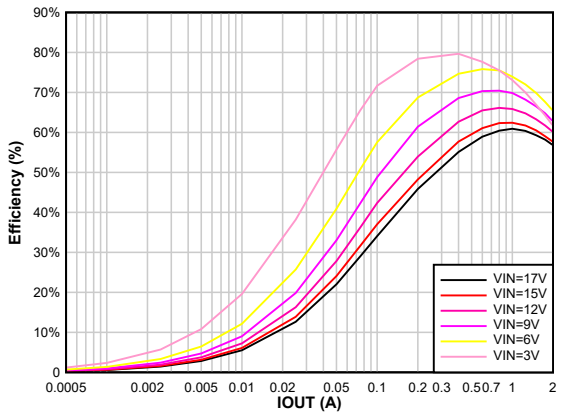
Auto PFM/PWM　F_{sw} = 1 MHz

図 8-53. Efficiency vs Output Current V_{OUT} = 0.4 V



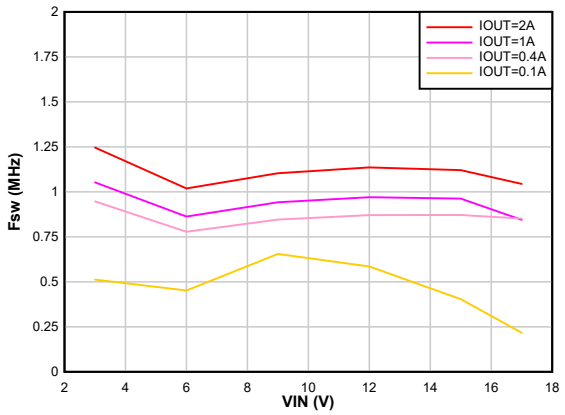
Auto PFM/PWM F_{sw} = 2.5 MHz

図 8-54. Efficiency vs Output Current V_{OUT} = 0.4 V



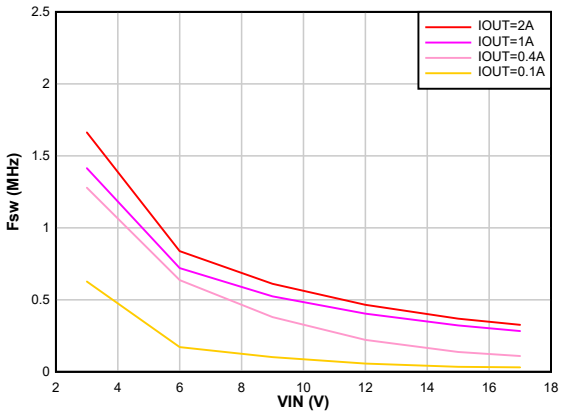
FPWM F_{sw} = 1 MHz

図 8-55. Efficiency vs Output Current V_{OUT} = 0.4 V



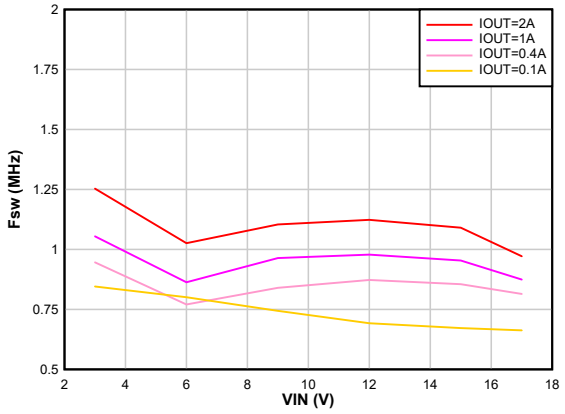
Auto PFM/PWM F_{sw} = 1 MHz

図 8-56. Switching Frequency vs Input Voltage V_{OUT} = 0.4 V



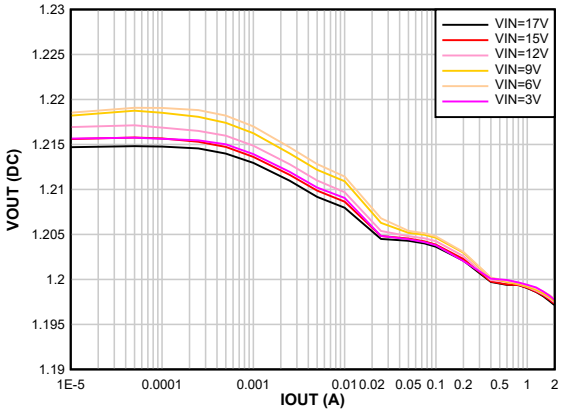
Auto PFM/PWM F_{sw} = 2.5 MHz

図 8-57. Switching Frequency vs Input Voltage V_{OUT} = 0.4 V



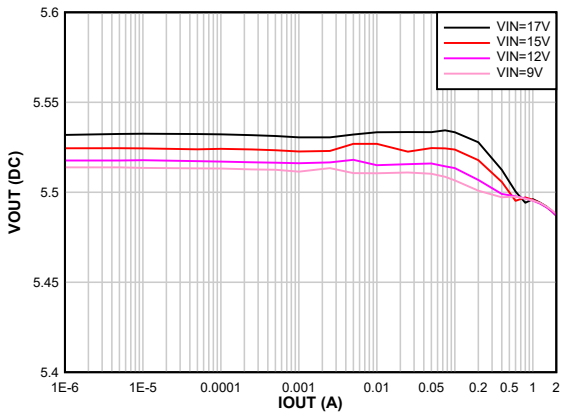
FPWM F_{sw} = 1 MHz

図 8-58. Switching Frequency vs Input Voltage V_{OUT} = 0.4 V



Auto PFM/PWM F_{sw} = 1 MHz

図 8-59. Output Voltage vs Output Current V_{OUT} = 1.2 V



Auto PFM/PWM F_{sw} = 2.5 MHz

図 8-60. Output Voltage vs Output Current
V_{OUT} = 5.5 V

8.4 Power Supply Recommendations

The power supply to the TPSM82902 must have a current rating according to the supply voltage, output voltage, and output current of the TPSM82902.

8.5 Layout

8.5.1 Layout Guidelines

A proper layout is critical for the operation of a switched mode power supply, even more at high switching frequencies. Therefore, the PCB layout of the TPSM82902 demands careful attention to ensure operation and to get the performance specified. A poor layout can lead to issues like poor regulation (both line and load), stability and accuracy weaknesses, increased EMI radiation, bad thermal performance, and noise sensitivity.

- See 図 8-61 for the recommended layout of the TPSM82902, which is designed for common external ground connections. TI recommends placing all components as close as possible to the package pins. The input and output capacitors placement specifically, must be closest to the VIN, VOUT, and GND pins of the TPSM82902.
- Provide low capacitive paths (with respect to all other nodes) for traces with high dv/dt. Therefore, the input and output capacitance must be placed as close as possible to the IC pins and parallel wiring over long distances as well as narrow traces must be avoided. Loops which conduct an alternating current must outline an area as small as possible, as this area is proportional to the energy radiated.
- Sensitive nodes like FB needs to be connected with short wires and not nearby high dv/dt signals. As it carries information about the output voltage, it must be connected as close as possible to the actual output voltage (at the output capacitor). The capacitor on the SS/TR pin as well as the FB resistors, R1 and R2, must be kept close to the module and connect directly to those pins and the system ground plane. The same applies to VSET resistor if VSET is used to scale the output voltage.
- The package uses the pins for power dissipation. Thermal vias on the VIN, VOUT, and GND pins help to spread the heat through the PCB.
- In case of the EN, and MODE/S-CONF need to be tied to the input supply voltage at V_{IN}, the connection must be made directly at the input capacitor as indicated in the schematics.
- The SW/NC pin must not be connected to any other traces. For best practice, this pin must be left floating. If the pin is soldered to PCB copper, the pour needs to be: as small as possible, no inner layer connections, no vias, electrically floating, and limited to the pin area as possible.
- Refer to 図 8-61 for an example of component placement, routing and thermal design. The recommended layout is implemented on the EVM and shown in its user's guide.

8.5.2 Layout Example

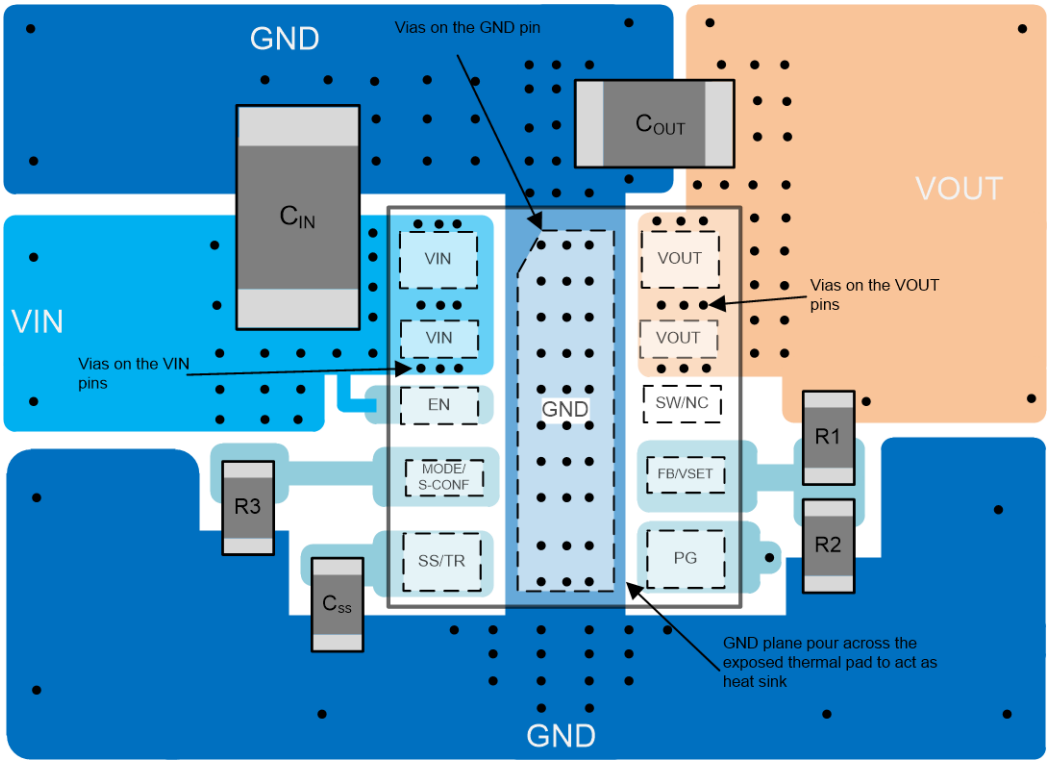


図 8-61. Layout

8.5.2.1 Thermal Considerations

Implementation of power converter modules with low-profile and fine-pitch such as MircoSiP packages typically requires special attention to power dissipation and thermal rise. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

The TPSM82902 is designed for a maximum operating junction temperature (T_J) of 125°C. Therefore, the maximum output power is limited by the power losses that can be dissipated over the actual thermal resistance, given by the package and the surrounding PCB structures. If the thermal resistance of the package is given, the size of the surrounding copper area and a proper thermal connection of the module can reduce the thermal resistance. To get an improved thermal behavior, TI recommends to follow the following guidelines:

- Use a multi-layer PCB boards (at least four layers, with 1-oz or more copper).
- Use thermal vias on the GND pin to connect the GND top layer with the GND inner and bottom layers. This helps dissipate the heat across layers.
- Generate as large a GND plane as allowable on the top and bottom layers, especially right near the package. The exposed thermal pad of the device sits right at the middle of the package. This is ideal for thermal dissipation. To take advantage of that, TI recommends the ground plan to cross through the package to allow maximum ground plan connection with the exposed pad. See 図 8-61 how the north ground pour is connecting with the south ground pour as it crosses through the exposed pad of the package.
- Use thermal vias on the VIN and VOUT pins (as close as possible to the pin) and around input and output capacitors to connect the VIN and VOUT top layer with the inner and bottom layers. This helps dissipate the heat across layers as well as decreases the resistance drop on these traces.
- Use wide and short traces for the main current paths to reduce the parasitic inductance and resistance and helps on thermal dissipation.
- Introduce airflow in the system if possible.
- Refer to 図 8-61 for an example of component placement, routing and thermal design.

For more details on how to use the thermal parameters, see the *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* and *Semiconductor and IC Package Thermal Metrics* application reports.

If short circuit or overload conditions are present, the device is protected by limiting internal power dissipation.

The device is qualified for long term qualification with a 125°C junction temperature.

9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

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9.1.2 Development Support

9.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM82902 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 サポート・リソース

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPSM82902SISR	Active	Production	uSiP (SIS) | 11	3000 | LARGE T&R	Yes	NIAU	Level-2-260C-1 YEAR	-40 to 125	TM2902
TPSM82902SISR.A	Active	Production	uSiP (SIS) | 11	3000 | LARGE T&R	Yes	NIAU	Level-2-260C-1 YEAR	-40 to 125	TM2902

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

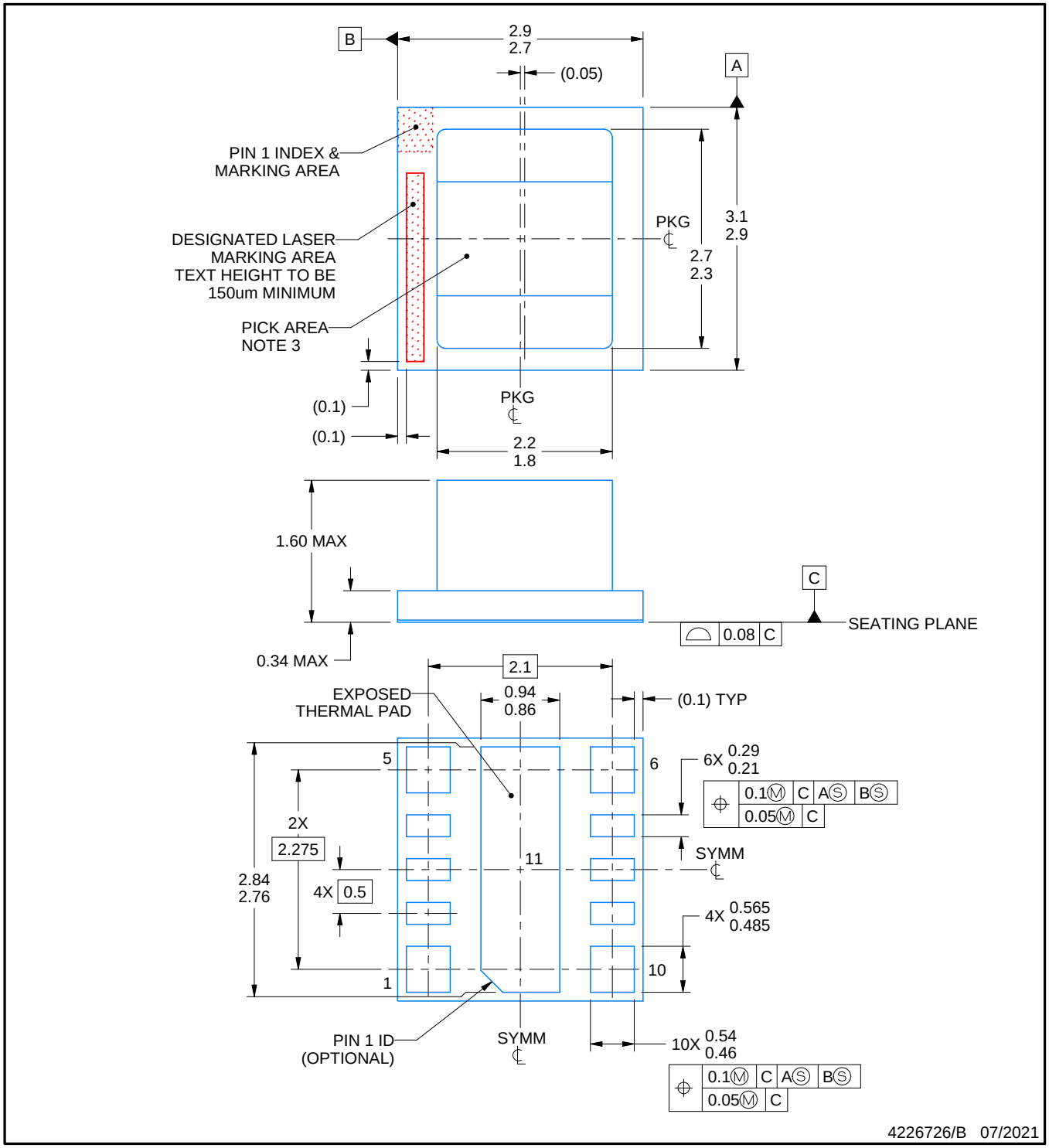
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

SIS0011A

PACKAGE OUTLINE

MicroSiP™ - 1.6 mm max height

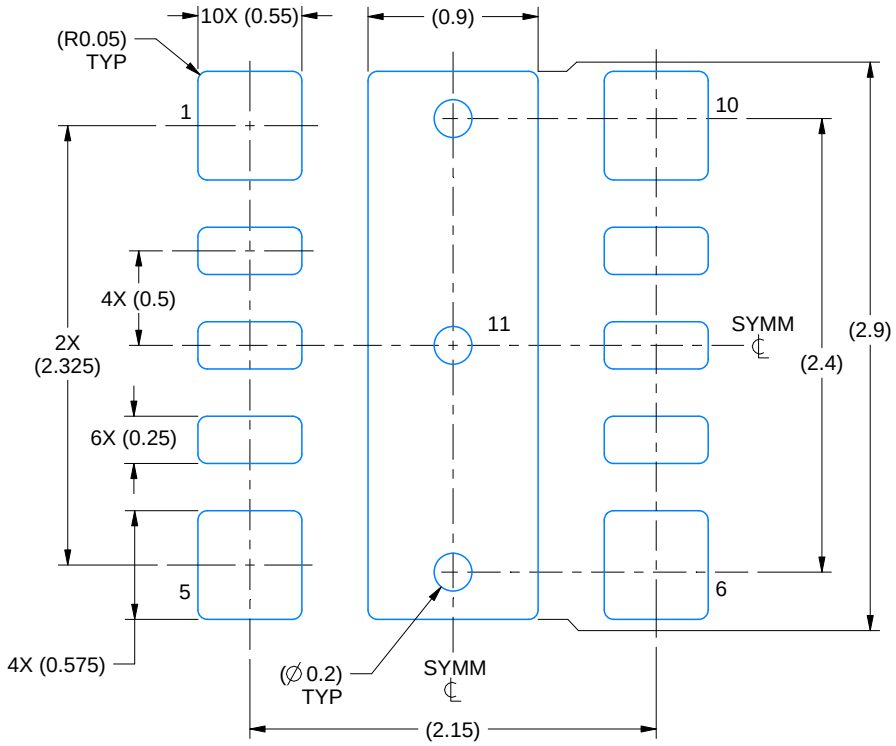
MICRO SYSTEM IN PACKAGE



MicroSiP is a trademark of Texas Instruments

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pick and place nozzle ∅ 1.3 mm or smaller recommended.
4. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:25X

SOLDER MASK DETAIL

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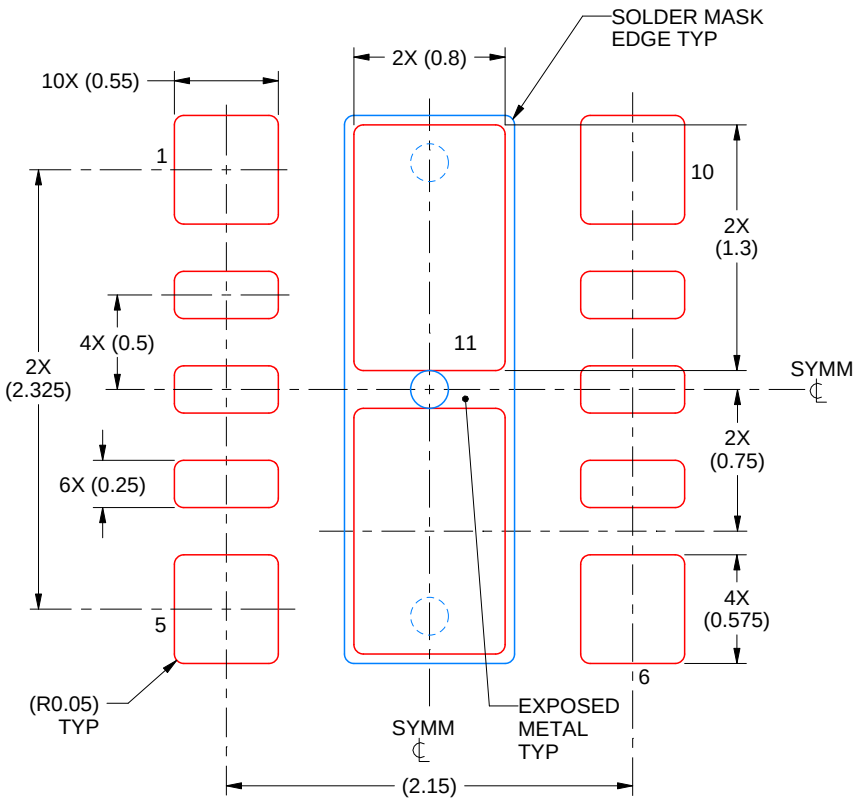
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月