Direct Downconversion Receiver

Check for Samples: TRF371109

FEATURES

- **Frequency Range: 300 MHz to 1700 MHz**
- **Integrated Baseband Programmable Gain Amplifier**
- **On-Chip Programmable Baseband Filter**
- **High Cascaded IP3: 27 dBm at 900 MHz**
- **High IP2: 68 dBm at 900 MHz**
- **Hardware and Software Power Down**
- **Three-Wire Serial Interface**
- **Single Supply: 4.5-V to 5.5-V Operation**
- **Silicon Germanium Technology**

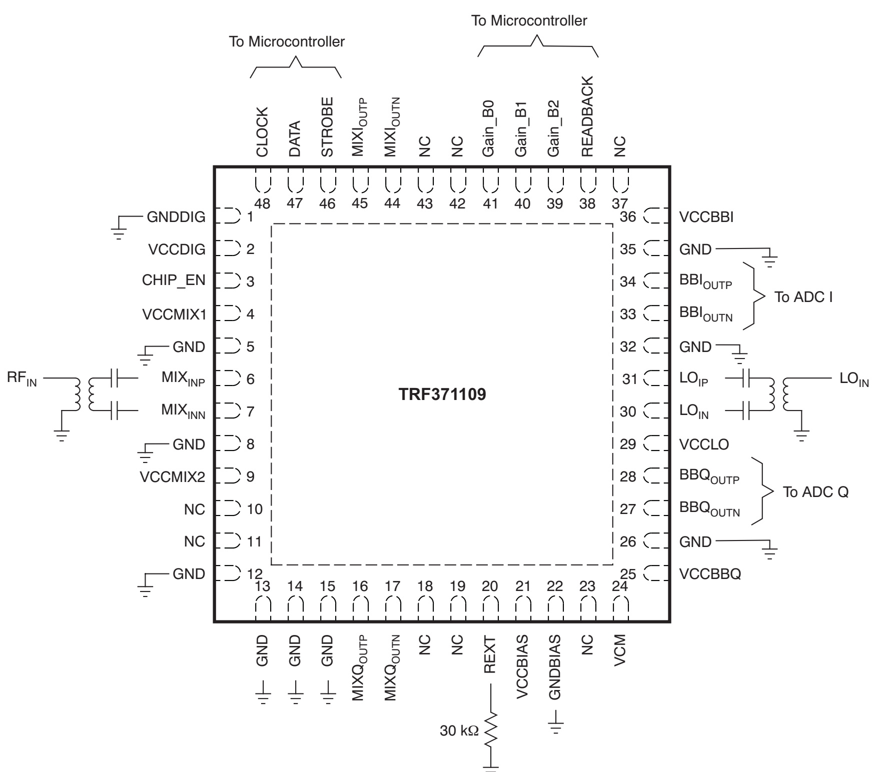
APPLICATIONS

- **Multicarrier Wireless Infrastructure**
- **WiMAX**
- **High-Linearity Direct-Downconversion Receiver**
- **LTE (Long Term Evolution)**

DESCRIPTION

The TRF371109 is a highly linear direct-conversion quadrature receiver. The TRF371109 integrates balanced I and Q mixers, LO buffers, and phase splitters to convert an RF signal directly to I and Q baseband. The on-chip programmable gain amplifiers allow adjustment of the output signal level without the need for external variable gain (attenuator) devices. The TRF371109 integrates programmable baseband low-pass filters that attenuate nearby interference, eliminating the need for an external baseband filter.

Housed in a 7-mm × 7-mm VQFN package, the TRF371109 provides the smallest and most integrated receiver solution available for high-performance equipment.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

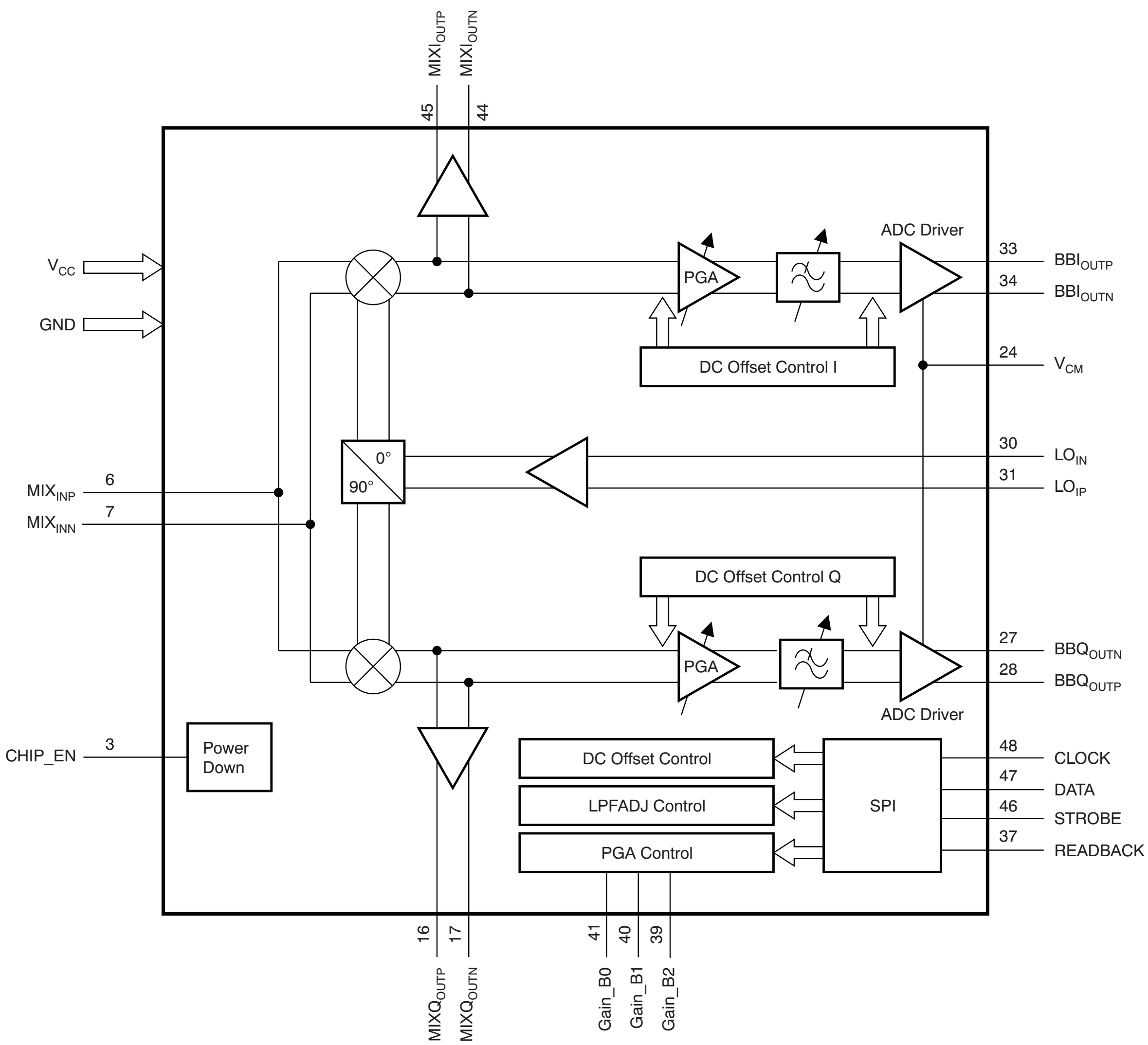
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE DEVICE OPTIONS(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TRF371109	VQFN-48	RGZ	–40°C to +85°C	TRF371109IRGZ	TRF371109IRGZR	Tape and Reel, 2500
					TRF371109IRGZT	Tape and Reel, 250

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted).[1]

	VALUE	UNIT
Supply voltage range[2]	–0.3 to 5.5	V
Digital I/O voltage range	–0.3 to V_{CC} +0.5	V
Operating virtual junction temperature range, T_J	–40 to +150	°C
Operating ambient temperature range, T_A	–40 to +85	°C
Storage temperature range, T_{stg}	–65 to +150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V_{CC}	Power-supply voltage	4.5	5.0	5.5	V
	Power-supply voltage ripple			940	μV_{PP}
T_A	Operating free-air temperature range	–40		+85	°C
T_J	Operating virtual junction temperature range	–40		+150	°C

THERMAL CHARACTERISTICS

Over recommended operating free-air temperature range (unless otherwise noted).

PARAMETER[1]		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Thermal resistance, junction-to-ambient	Soldered slug, no airflow		26		°C/W
		Soldered slug, 200-LFM airflow		20.1		
		Soldered slug, 400-LFM airflow		17.4		
$R_{\theta JA}$[2]		7-mm × 7-mm, 48-pin PDFP		25		
$R_{\theta JB}$	Thermal resistance, junction-to-board	7-mm × 7-mm 48-pin PDFP		12		°C/W

(1) Determined using JEDEC standard JESD-51 with high-K board

(2) 16 layers, high-K board

THERMAL INFORMATION

THERMAL METRIC[1]		TRF371109 RGZ 48 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	26.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	11.2	
θ_{JB}	Junction-to-board thermal resistance	3.4	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	3.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	0.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

At V_{CC} = 5 V, LO power = 0 dBm, and T_A = +25°C,unless otherwise noted.

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC PARAMETERS						
I_{CC}	Total supply current			360		mA
	Power-down current			2		mA
IQ DEMODULATOR AND BASEBAND SECTION						
f_{RF}	Frequency range		300		1700	MHz
	Gain range		22	24		dB
	Gain step	See[(1)]		1		dB
Pin_{Max}	Maximum RF power input	Before damage		25		dBm
OIP3		Gain setting = 24[(2)]		30		dBV_{RMS}
$P1dB_{Min}$		One tone[(3)]		3		dBV_{RMS}
f_{Min}	Minimum baseband low-pass filter (LPF) cutoff frequency	1-dB point[(4)]		700		kHz
f_{Max}	Maximum baseband LPF cutoff frequency	3-dB point[(4)]	15			MHz
f_{Bypass}	Baseband LPF cutoff frequency in bypass mode	3-dB point[(5)]		30		MHz
F_{sel}	Baseband relative attenuation at LPF cutoff frequency (f_C)[(6)]	1 × f_C		1		dB
		1.5 × f_C		8		dB
		2 × f_C		32		dB
		3 × f_C		54		dB
		4 × f_C		75		dB
		5 × f_C		90		dB
	Image suppression			–40		dB
	Output BB attenuator			3		dB
	Output load impedance[(7)]	Parallel resistance		1		kΩ
		Parallel capacitance		20		pF
V_{CM}	Output, common-mode	Measured at I- and Q-channel baseband outputs		1.5		V
	Baseband harmonic level	Second harmonic[(8)]		–100		dBc
		Third harmonic[(8)]		–93		dBc
LOCAL OSCILLATOR PARAMETERS						
	Local oscillator frequency		300		1700	MHz
	LO input level	See [(9)]	–3	0	6	dBm
	LO leakage	At MIX_{INN}/MIX_{INP} at 0-dBm LO drive level		–58		dBm
DIGITAL INTERFACE						
V_{IH}	High-level input voltage		0.6 × V_{CC}	5	V_{CC}	V
V_{IL}	Low-level input voltage		0		0.8	V
V_{OH}	High-level output voltage		0.8 × V_{CC}			V
V_{OL}	Low-level output voltage				0.2 × V_{CC}	V

(1) Two consecutive gain settings.
(2) Two CW tones at an offset from LO frequency smaller than the baseband-filter cutoff frequency. Performance is set by baseband circuitry regardless of LO frequency.
(3) Single CW tone at an offset from LO frequency smaller than the baseband-filter cutoff frequency. Performance is set by baseband circuitry regardless of LO frequency.
(4) Baseband low-pass filter cutoff frequency is programmable through SPI register LPFADJ. LPFADJ = 0 corresponds to max bandwidth; LPFADJ = 255 corresponds to minimum BW.
(5) Filter Ctrl setting equal to 0.
(6) Attenuation relative to passband gain.
(7) The typical value for this parameter is the load impedance that the device is able to drive.
(8) LO frequency set to 900 MHz. Power-in set to –40 dBm. Gain setting at 24. DC offset calibration engaged. Input signal set at 2.5-MHz offset.
(9) LO power outside of this range is possible but may introduce degraded performance.

ELECTRICAL CHARACTERISTICS (continued)

At V_{CC} = 5 V, LO power = 0 dBm, and T_A = +25°C,unless otherwise noted.

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{LO} = 300 MHz(10)						
G_{Max}	Maximum gain(11)	Gain setting = 24		48.7		dB
NF	Noise figure	Gain setting = 24		8.7		dB
IIP3	Third-order input intercept point	Gain setting = 24(12)(13)		13.9		dBm
IIP2	Second-order input intercept point	Gain setting = 24(13)(14)		45		dBm
f_{LO} = 700 MHz(10)						
G_{Max}	Maximum gain(11)	Gain setting = 24		43		dB
NF	Noise figure	Gain setting = 24		10.7		dB
IIP3	Third-order input intercept point	Gain setting = 24(12)(13)		25		dBm
IIP2	Second-order input intercept point	Gain setting = 24(13)(14)		70		dBm
f_{LO} = 900 MHz(10)						
G_{Max}	Maximum gain(11)	Gain setting = 24		41		dB
NF	Noise figure	Gain setting = 24		12.4		dB
		Gain setting = 16		14.8		dB
IIP3	Third-order input intercept point	Gain setting = 24(12)(13)		27		dBm
IIP2	Second-order input intercept point	Gain setting = 24(13)(14)		68		dBm
f_{LO} = 1425 MHz(10)						
G_{Max}	Maximum gain(11)	Gain setting = 24		36.9		dB
NF	Noise figure	Gain setting = 24		15.5		dB
IIP3	Third-order input intercept point	Gain setting = 24(12)(13)		27		dBm
IIP2	Second-order input intercept point	Gain setting = 24(13)(14)		65		dBm
f_{LO} = 1700 MHz(10)						
G_{Max}	Maximum gain(11)	Gain setting = 24		35.9		dB
NF	Noise figure	Gain setting = 24		17.5		dB
IIP3	Third-order input intercept point	Gain setting = 24(12)(13)		25.5		dBm
IIP2	Second-order input intercept point	Gain setting = 24(13)(14)		60		dBm

(10) For broadband frequency sweeps, the Picosecond balun (model #5310A) is used at the RF and LO input. For frequency bands between 600 MHz and 1250 MHz, the Murata balun LDB21897M005C-001 is used. Performance parameters adjusted for balun insertion loss. Recommended baluns for respective frequency band are listed:
700 MHz and 900 MHz: Murata LDB21897M005C-001 (or equivalent)
1740 MHz: Murata LDB211G8005C-001 (or equivalent)
1950 MHz: Murata LDB211G9005C-001 (or equivalent)
2025 MHz: Murata LDB211G9005C-001 (or equivalent)
2500 MHz: Murata LDB212G4005C-001 (or equivalent)
3500 MHz: Johanson 3600BL14M050E (or equivalent)
(11) Gain defined as voltage gain from MIX_{IN} (V_{RMS}) to either baseband output: BBI/Q_{OUT} (V_{RMS})
(12) Two CW tones of –30 dBm at $f_{RF1} = f_{LO} \pm (2 \bullet f_c)$ and $f_{RF2} = f_{LO} \pm [(4 \bullet f_c) + 100\ kHz]$; f_c = Baseband filter 1-dB cutoff frequency.
(13) Because the two-tone interference sources are outside of the baseband filter bandwidth, the results are inherently independent of the gain setting. Intermodulation parameters are recorded at maximum gain setting, where measurement accuracy is best.
(14) Two CW tones at –30 dBm at $f_{RF1} = f_{LO} \pm (2 \bullet f_c)$ and $f_{RF2} = f_{LO} \pm [(2 \bullet f_c) + 100\ kHz]$; IM2 product measured at 100-kHz output frequency. f_C = Baseband filter 1-dB cutoff frequency.

TIMING REQUIREMENTS

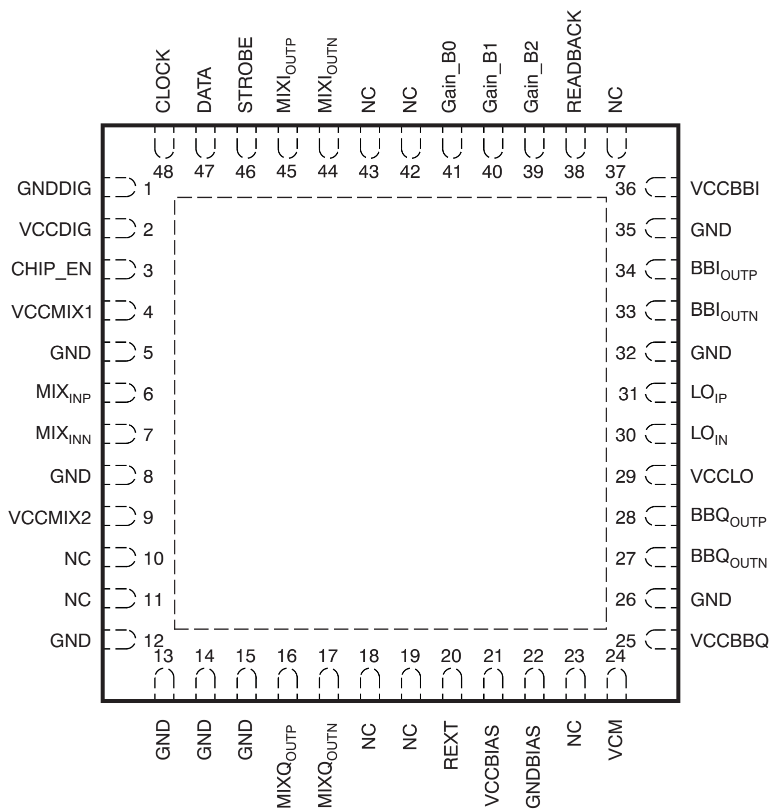
At V_{CC} = 5 V, LO power = 0 dBm, and T_A = +25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(CLK)}$	Clock period		50			ns
t_{SU1}	Setup time, data		10			ns
t_H	Hold time, data		10			ns
t_W	Pulse width, STROBE		20			ns
t_{SU2}	Setup time, STROBE		10			ns

DEVICE INFORMATION

PIN ASSIGNMENTS

RGZ PACKAGE
VQFN-48
(TOP VIEW)



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NO.	NAME		
1	GNDDIG		Digital ground
2	VCCDIG		Digital power supply
3	CHIP_EN	I	Chip enable
4	VCCMIX1		Mixer power supply
5	GND		Ground
6	MIX_{INP}	I	Mixer input: positive terminal
7	MIX_{INN}	I	Mixer input: negative terminal
8	GND		Ground
9	VCCMIX2		Mixer power supply
10	NC		No connect
11	NC		No connect
12	GND		Ground
13	GND		Ground
14	GND		Ground
15	GND		Ground
16	$MIXQ_{OUTP}$	O	Mixer Q output: positive terminal (test pin)
17	$MIXQ_{OUTN}$	O	Mixer Q output: negative terminal (test pin)
18	NC		No connect
19	NC		No connect
20	REXT	O	Reference bias external resistor
21	VCCBIAS		Bias block power supply
22	GNDBIAS		Bias block ground
23	NC		No connect
24	VCM	I	Baseband input common-mode voltage
25	VCCBBQ		Baseband Q chain power supply
26	GND		Ground
27	BBQ_{OUTN}	O	Baseband Q (in quadrature) output: negative terminal
28	BBQ_{OUTP}	O	Baseband Q (in quadrature) output: positive terminal
29	VCCLO		Local oscillator power supply
30	LO_{IN}	I	Local oscillator input: negative terminal
31	LO_{IP}	I	Local oscillator input: positive terminal
32	GND		Ground
33	BBI_{OUTN}	O	Baseband I (in-phase) output: positive terminal
34	BBI_{OUTP}	O	Baseband I (in-phase) output: negative terminal
35	GND		Ground
36	VCCBBI		Baseband I (in phase) power supply
37	NC		No connect
38	READBACK	O	SPI readback data
39	Gain_B2	I	PGA fast gain control bit 2
40	Gain_B1	I	PGA fast gain control bit 1
41	Gain_B0	I	PGA fast gain control bit 0
42	NC		No connect
43	NC		No connect
44	MIX_{IOUTN}	O	Mixer I output: negative terminal
45	MIX_{IOUTP}	O	Mixer I output: positive terminal
46	STROBE	I	SPI enable
47	DATA	I	SPI data input
48	CLOCK	I	SPI clock input

TYPICAL CHARACTERISTICS

At V_{CC} = 5 V, LO power = 0 dBm, and T_A = +25°C, using balun Murata LDB21897M005C-001 (unless otherwise noted).

Table of Graphs

Gain	vs LO frequency(1)(2)(3)	Figure 1, Figure 2, Figure 3
Noise figure	vs LO frequency(1)(2)(3)	Figure 4, Figure 5, Figure 6
IIP3	vs LO frequency(4)(5)(6)	Figure 7, Figure 9, Figure 8
IIP2	vs LO frequency(4)(5)(6)	Figure 10, Figure 12, Figure 11
Gain	vs LO frequency	Figure 13, Figure 14, Figure 15
IIP3	vs LO frequency(5)(6)	Figure 16, Figure 17, Figure 18, Figure 19
IIP2	vs LO frequency(5)(6)	Figure 20, Figure 21, Figure 22, Figure 23
Noise figure	vs LO frequency(3)	Figure 24, Figure 25, Figure 26
OIP3	vs Frequency offset(7)(3)	Figure 27, Figure 28, Figure 29, Figure 30
Noise figure	vs BB gain setting(8)	Figure 31
Gain	vs BB gain setting(8)	Figure 32
Gain	vs Frequency offset(9)	Figure 33, Figure 34
Gain	vs Frequency offset (bypass mode)(9)	Figure 35, Figure 36
1-dB LPF corner frequency	vs LPFADJ setting	Figure 37
Relative LPF group delay	vs Frequency offset(10)	Figure 38
Image rejection	vs BB frequency offset	Figure 39
DC offset limit	vs Temperature(11)	Figure 40
Out-of-band P1dB	vs Relative offset multiplier to corner frequency(12)	Figure 41

(1) Measured with broadband Picosecond 5310A balun on the LO input and single ended connection on the RF input. Performance gain adjusted for the 3-dB differential to single-ended insertion loss.
(2) Performance ripple because of impedance mismatch on the RF input.
(3) Measured with the maximum baseband gain (BB gain) setting, unless otherwise noted.
(4) Measured with broadband Picosecond 5310A balun on the LO input and RF input. Balun insertion loss is compensated for in the measurement.
(5) Out-of-band intercept point is defined with tones that are at least two times farther out than the programmed LPF corner frequency that generate an intermodulation tone that falls inside the LPF passband.
(6) Out-of-band intercept point depends on the demodulator performance and not the baseband circuitry; the measurement is taken at max gain but is valid across all PGA settings.
(7) Measured with filter in bypass mode to characterize the passband circuitry across baseband frequencies.
(8) Data taken with LO frequency = 900 MHz.
(9) Normalized gain.
(10) Relative to the low frequency offset group delay in bypass mode.
(11) Idet set to 50 µA; RF signal is off; LO at 2.4 GHz at 0 dBm; Det filter set to 1 kHz; Clk Div set to 1024.
(12) In-band tone set to 1 MHz; out-of-band jammer tone set to specified relative offset ratio from the programmed corner frequency. Jammer tone is increased until in-band tone compresses 1 dB.

TYPICAL CHARACTERISTICS

At V_{CC} = 5 V, LO power = 0 dBm, and T_A = +25°C, using balun Murata LDB21897M005C-001 (unless otherwise noted).

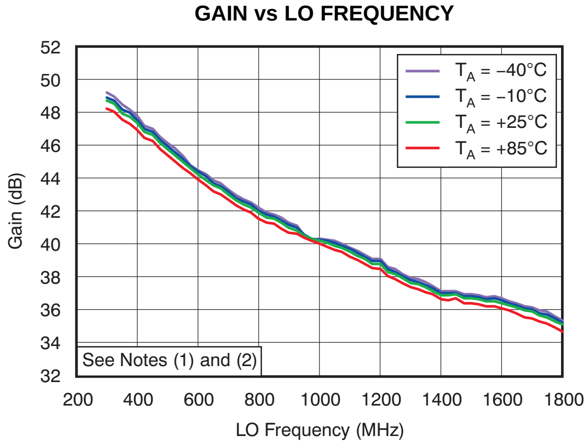


Figure 1.

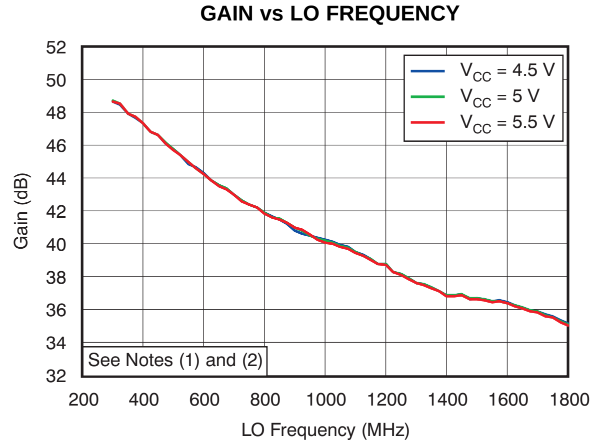


Figure 2.

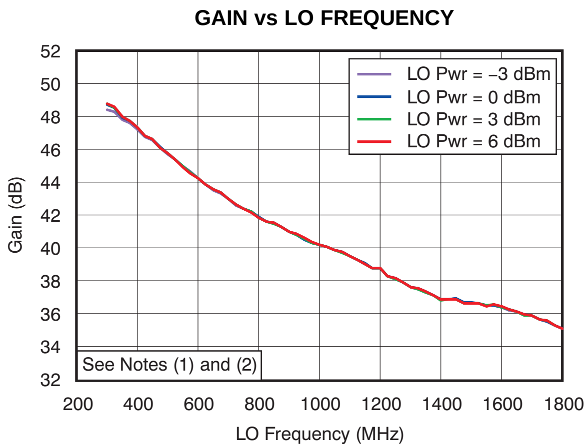


Figure 3.

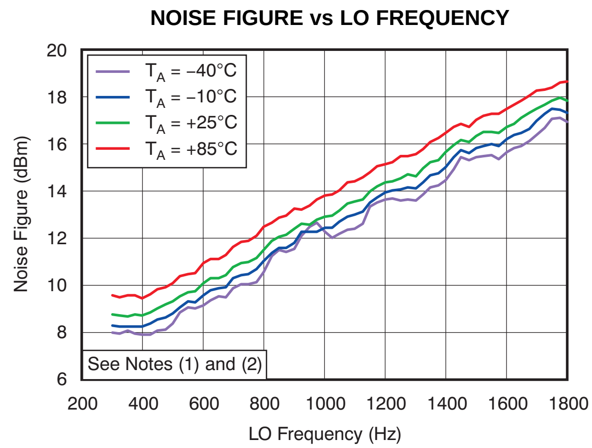


Figure 4.

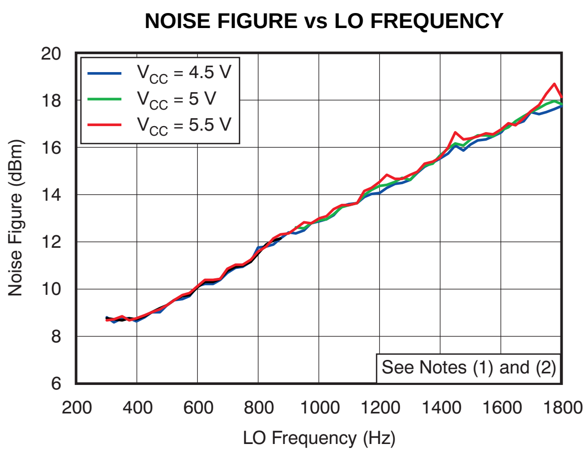


Figure 5.

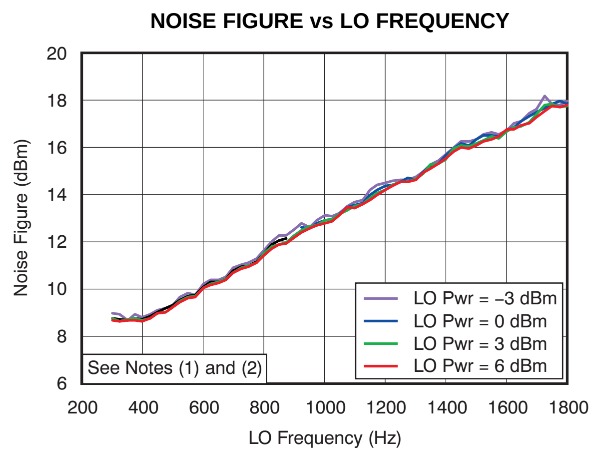
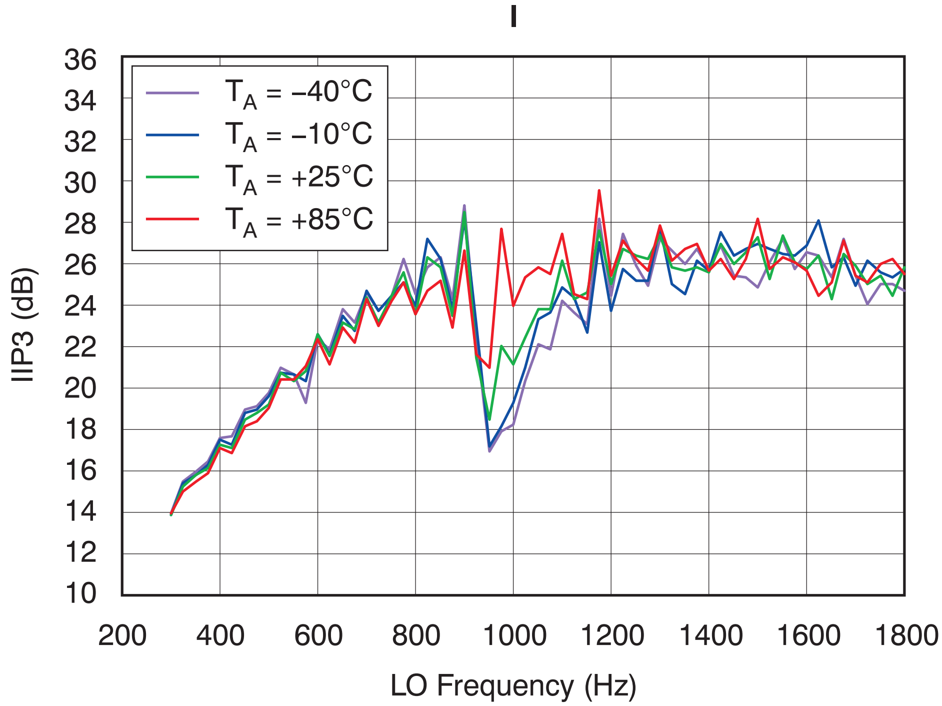


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At V_{CC} = 5 V, LO power = 0 dBm, and T_A = +25°C, using balun Murata LDB21897M005C-001 (unless otherwise noted).

IIP3 vs LO FREQUENCY



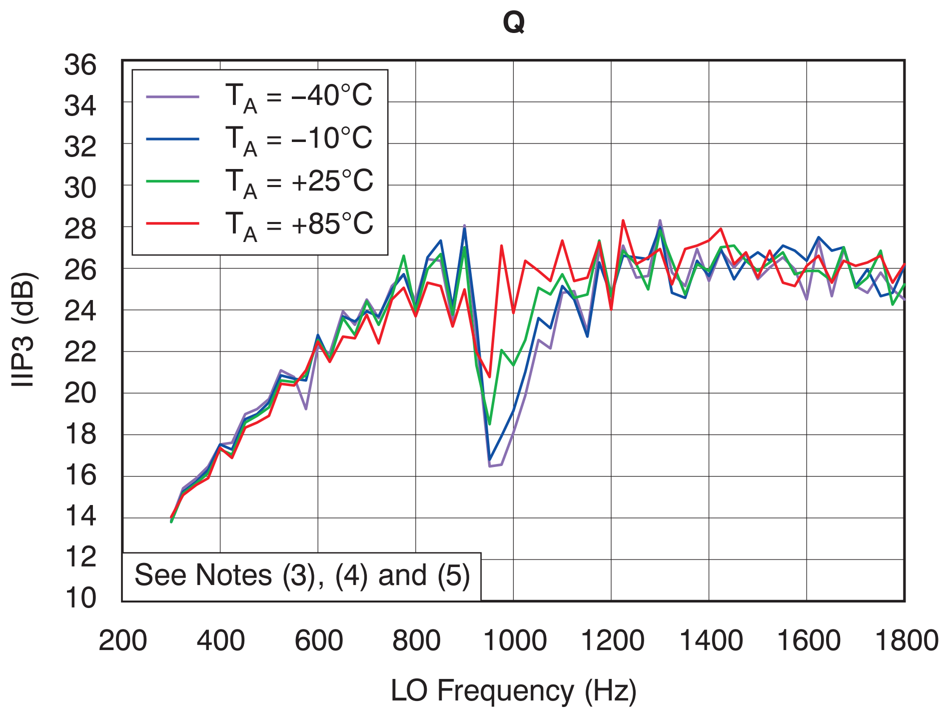


Figure 7.

TYPICAL CHARACTERISTICS (continued)

At V_{CC} = 5 V, LO power = 0 dBm, and T_A = +25°C, using balun Murata LDB21897M005C-001 (unless otherwise noted).

IIP3 vs LO FREQUENCY

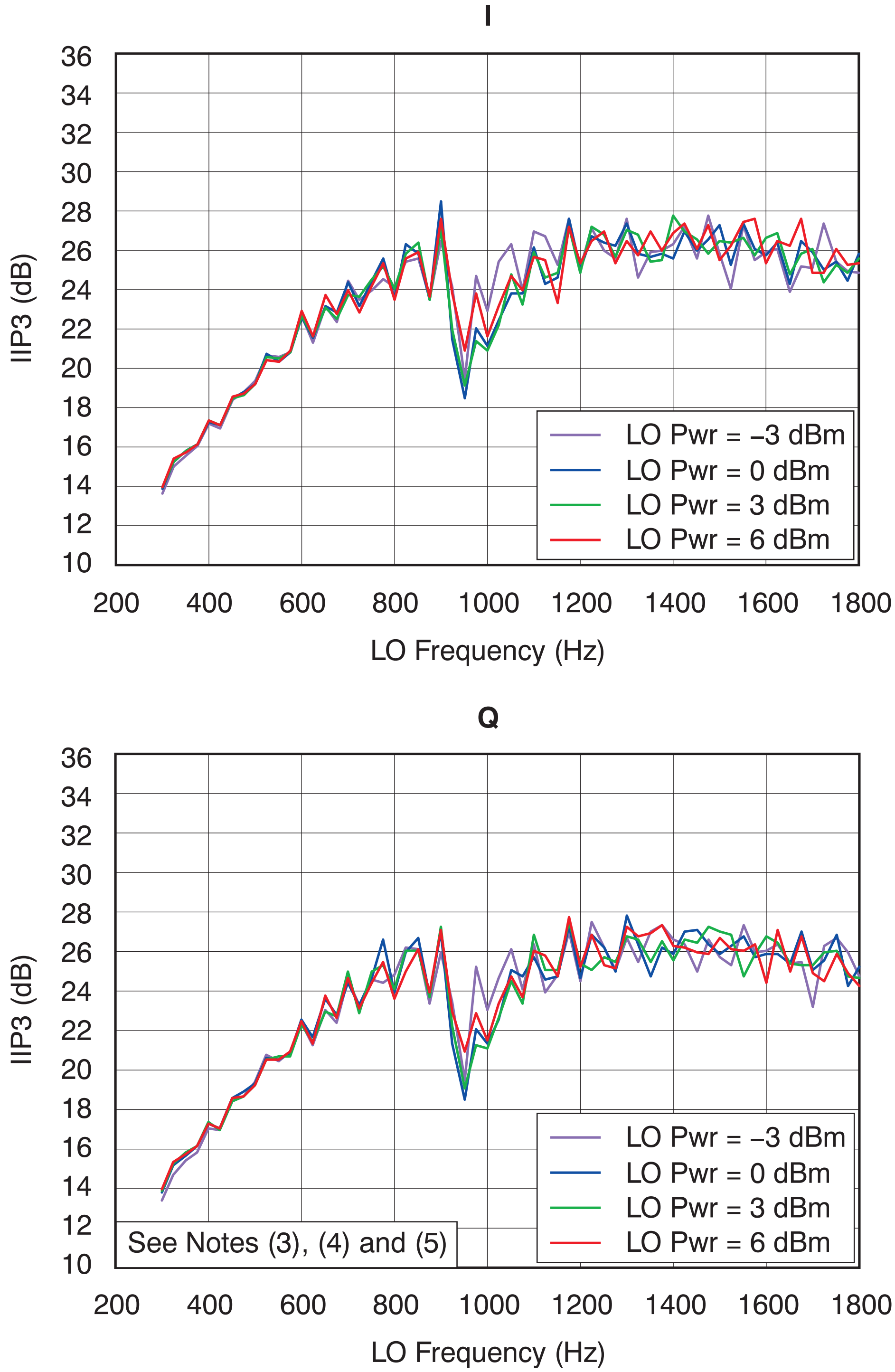
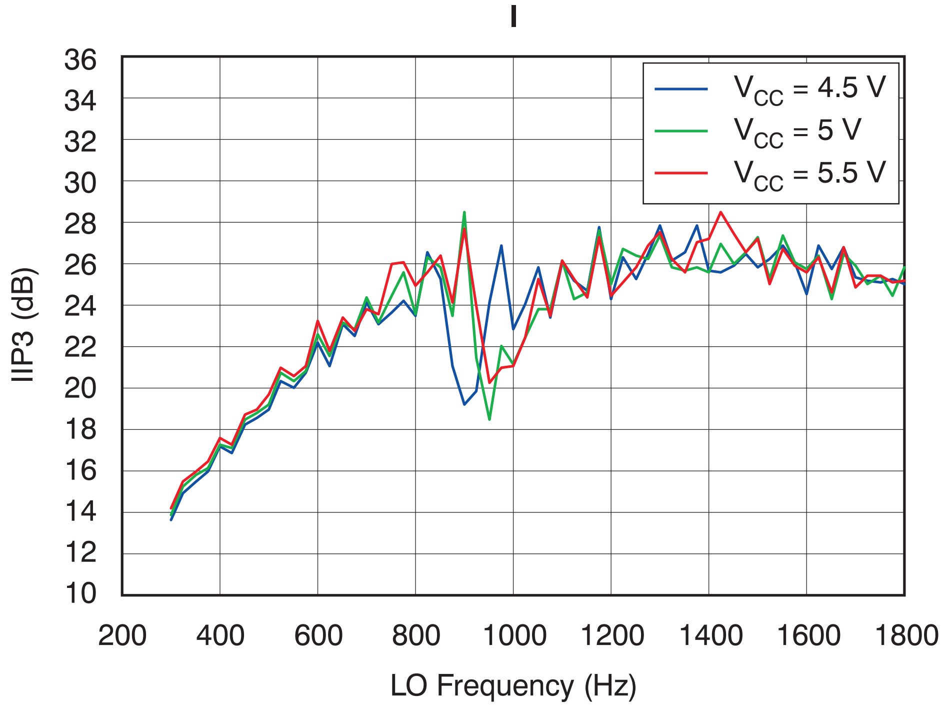


Figure 8.

TYPICAL CHARACTERISTICS (continued)

At V_{CC} = 5 V, LO power = 0 dBm, and T_A = +25°C, using balun Murata LDB21897M005C-001 (unless otherwise noted).

IIP3 vs LO FREQUENCY



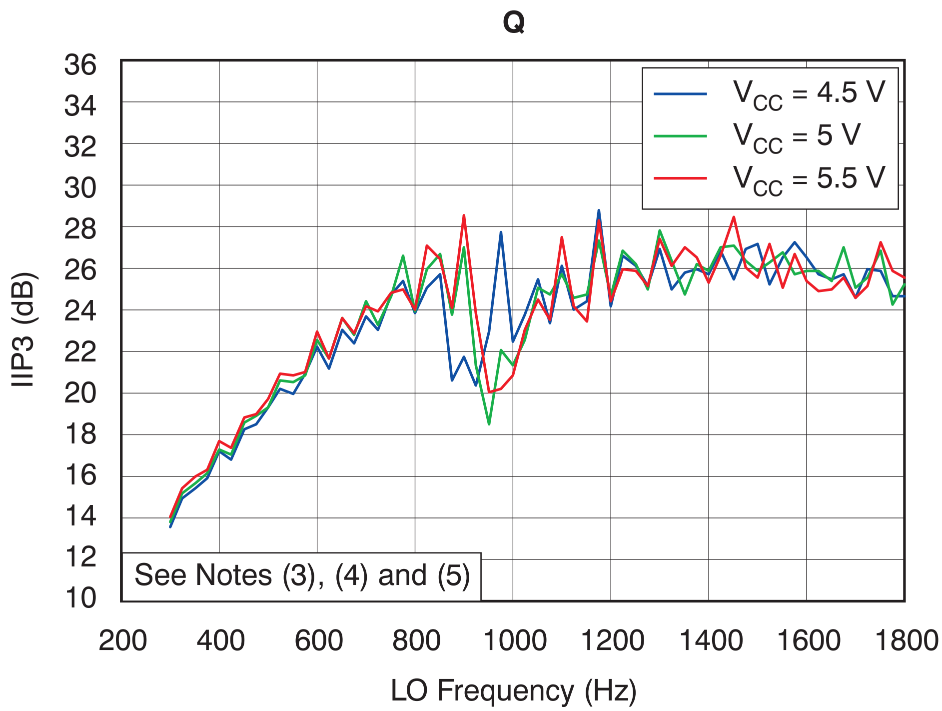


Figure 9.

TYPICAL CHARACTERISTICS (continued)

At V_{CC} = 5 V, LO power = 0 dBm, and T_A = +25°C, using balun Murata LDB21897M005C-001 (unless otherwise noted).

IIP2 vs LO FREQUENCY

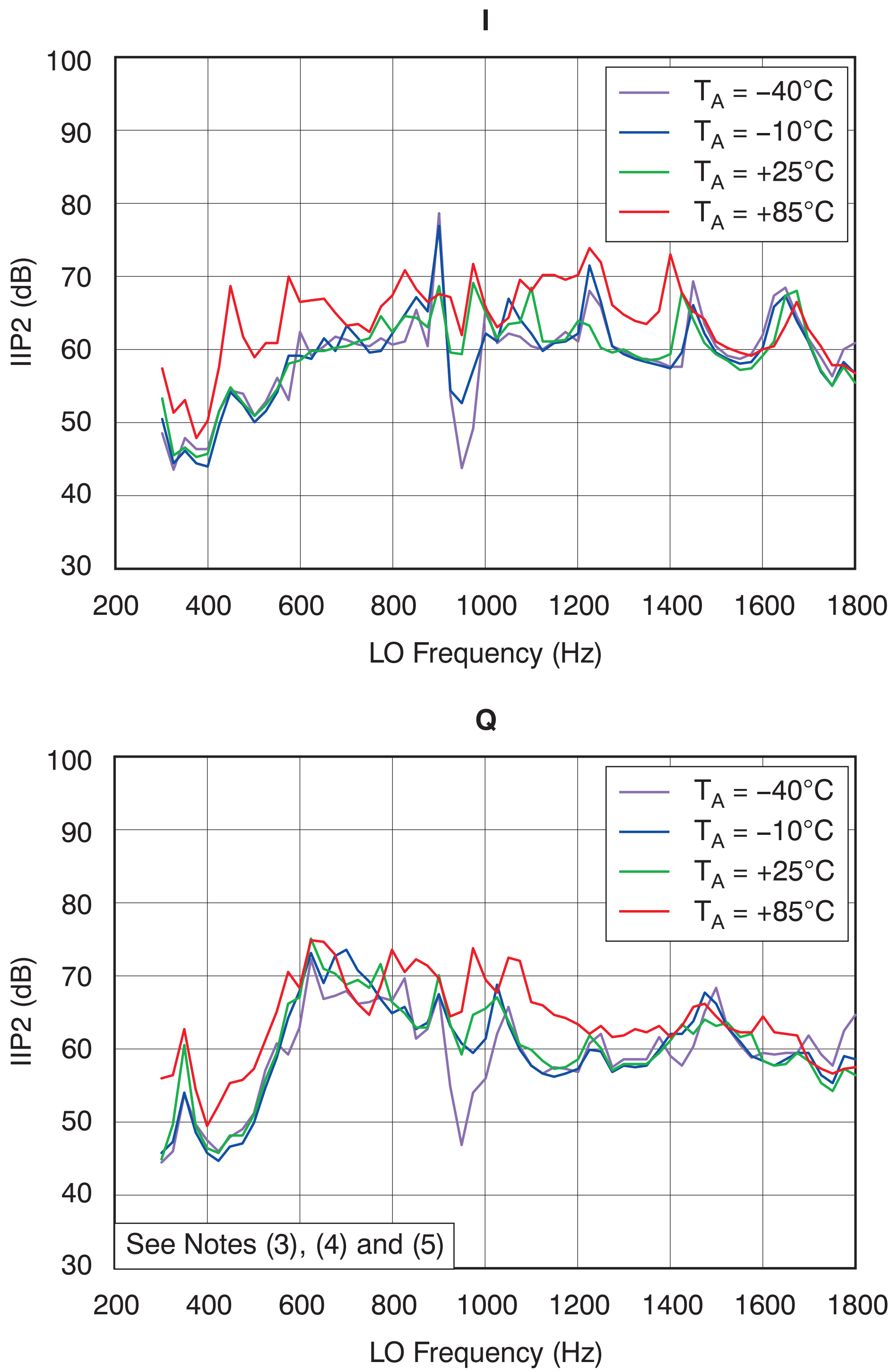
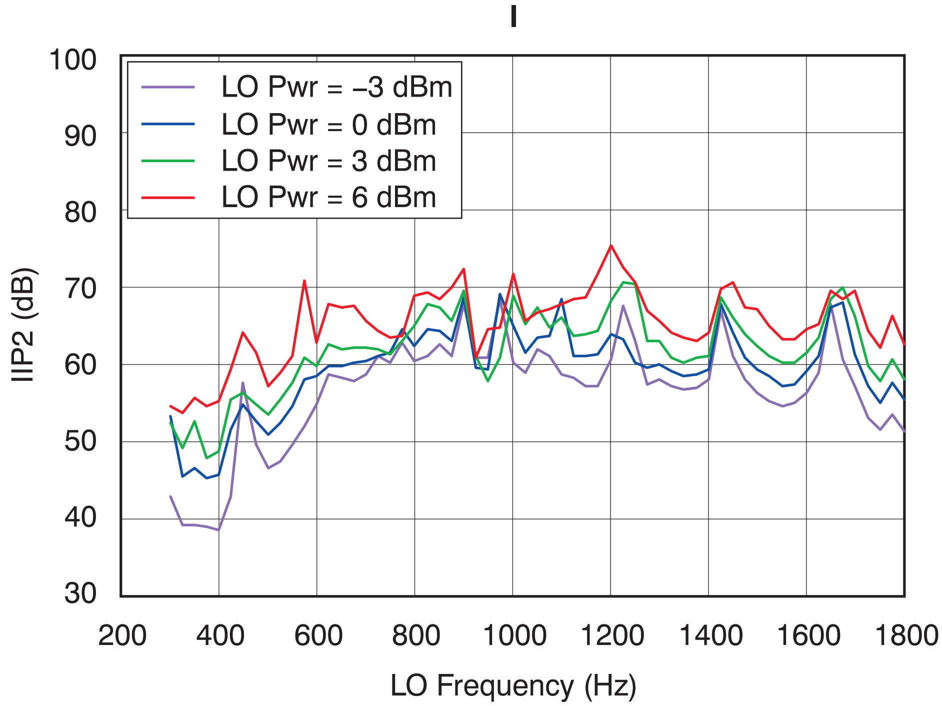


Figure 10.

TYPICAL CHARACTERISTICS (continued)

At V_{CC} = 5 V, LO power = 0 dBm, and T_A = +25°C, using balun Murata LDB21897M005C-001 (unless otherwise noted).

IIP2 vs LO FREQUENCY



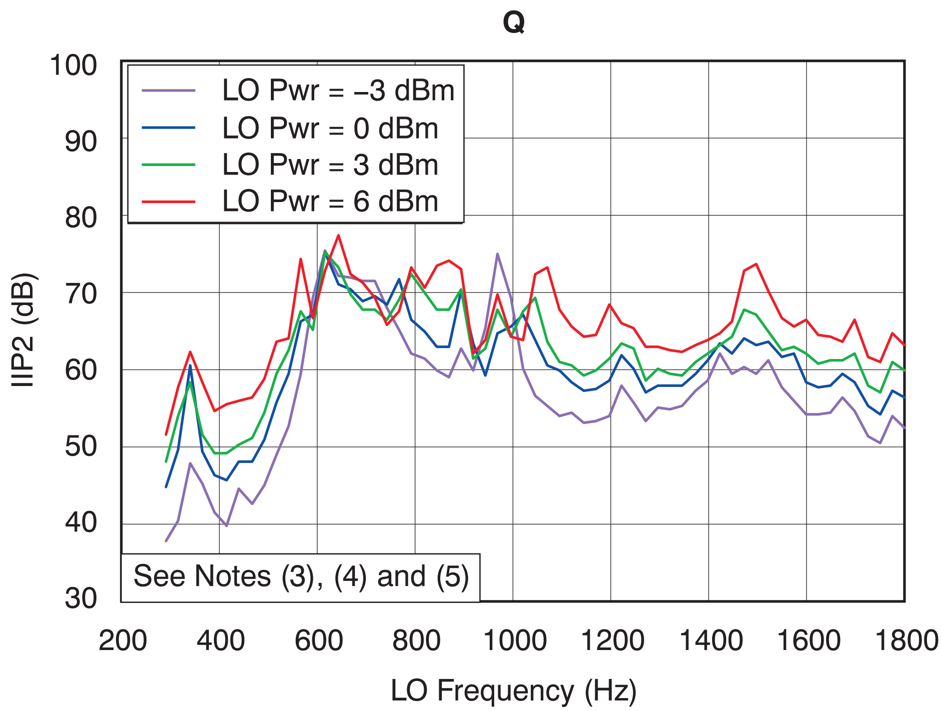


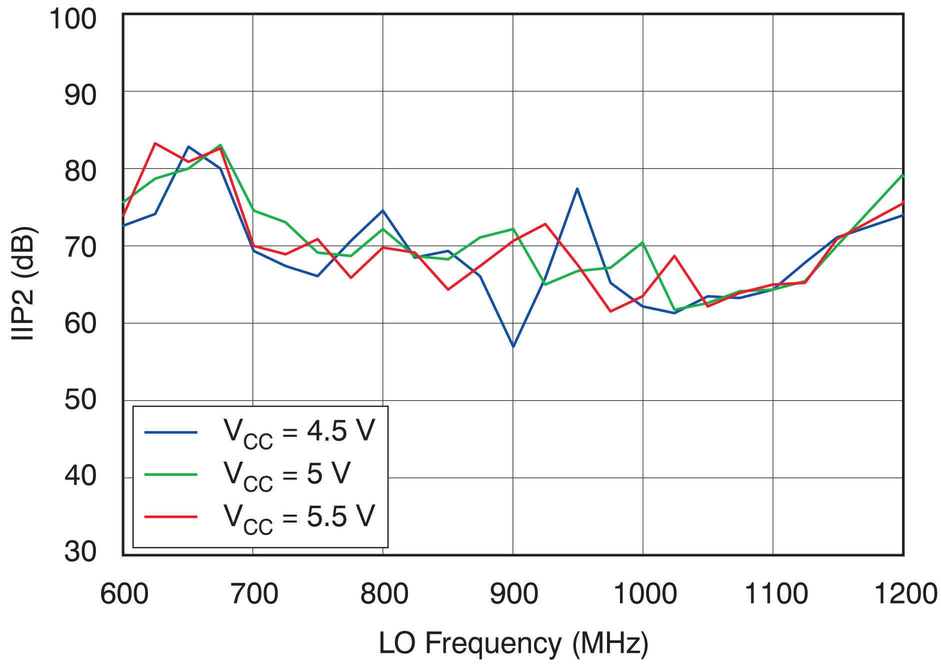
Figure 11.

TYPICAL CHARACTERISTICS (continued)

At V_{CC} = 5 V, LO power = 0 dBm, and T_A = +25°C, using balun Murata LDB21897M005C-001 (unless otherwise noted).

IIP2 vs LO FREQUENCY

I



Q

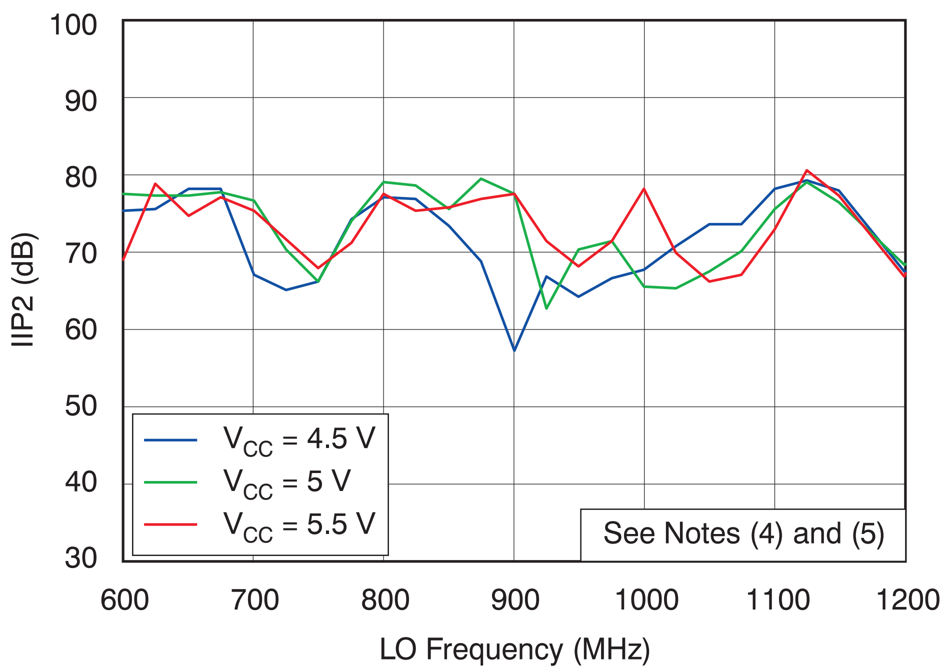


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At V_{CC} = 5 V, LO power = 0 dBm, and T_A = +25°C, using balun Murata LDB21897M005C-001 (unless otherwise noted).

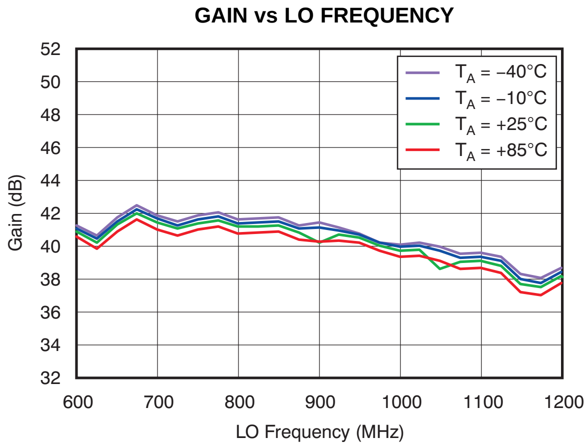


Figure 13.

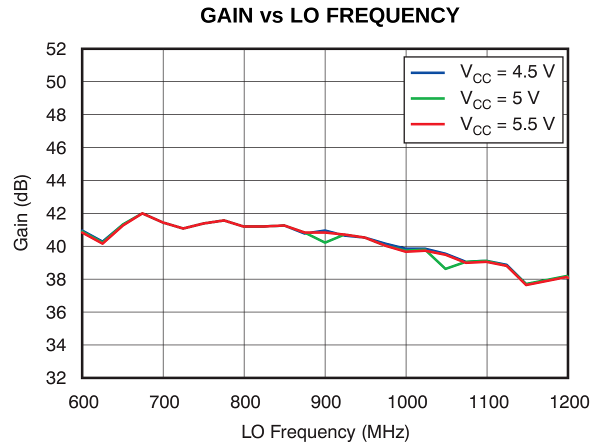


Figure 14.

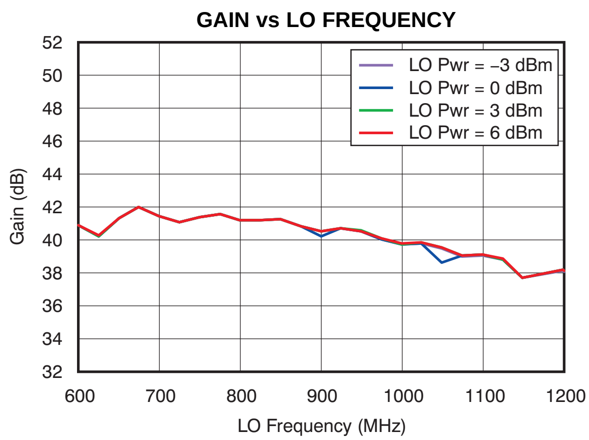
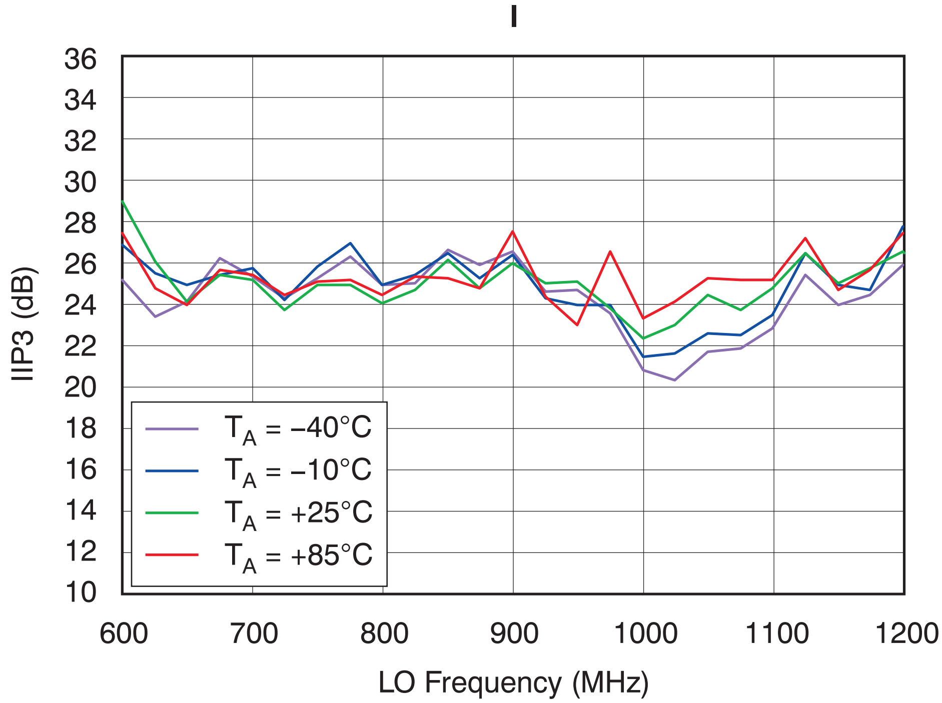


Figure 15.

TYPICAL CHARACTERISTICS (continued)

At V_{CC} = 5 V, LO power = 0 dBm, and T_A = +25°C, using balun Murata LDB21897M005C-001 (unless otherwise noted).

IIP3 vs LO FREQUENCY



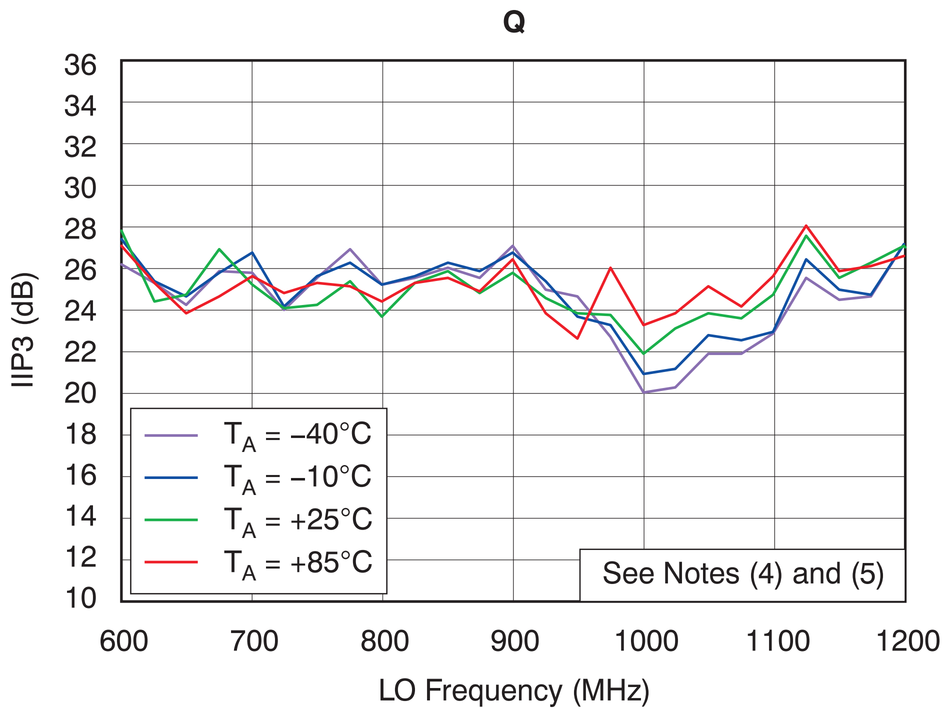
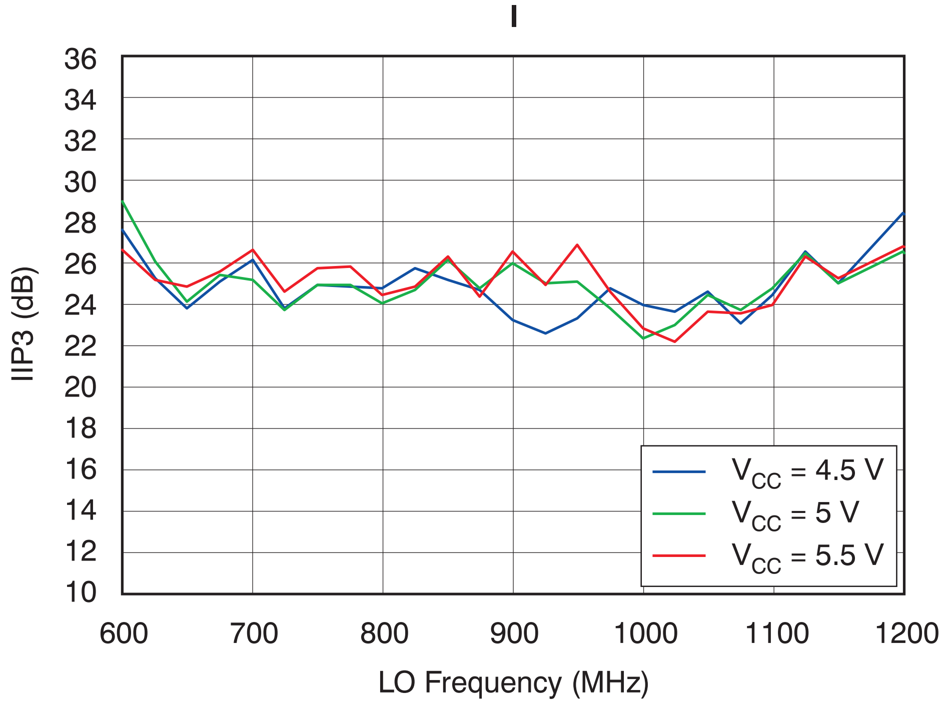


Figure 16.

TYPICAL CHARACTERISTICS (continued)

At V_{CC} = 5 V, LO power = 0 dBm, and T_A = +25°C, using balun Murata LDB21897M005C-001 (unless otherwise noted).

IIP3 vs LO FREQUENCY



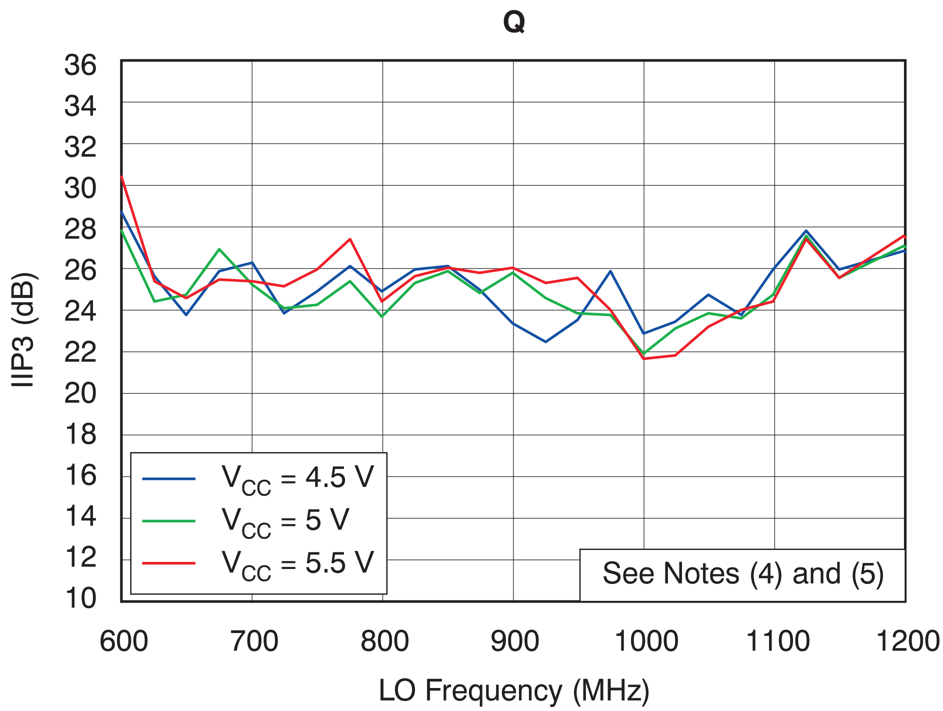
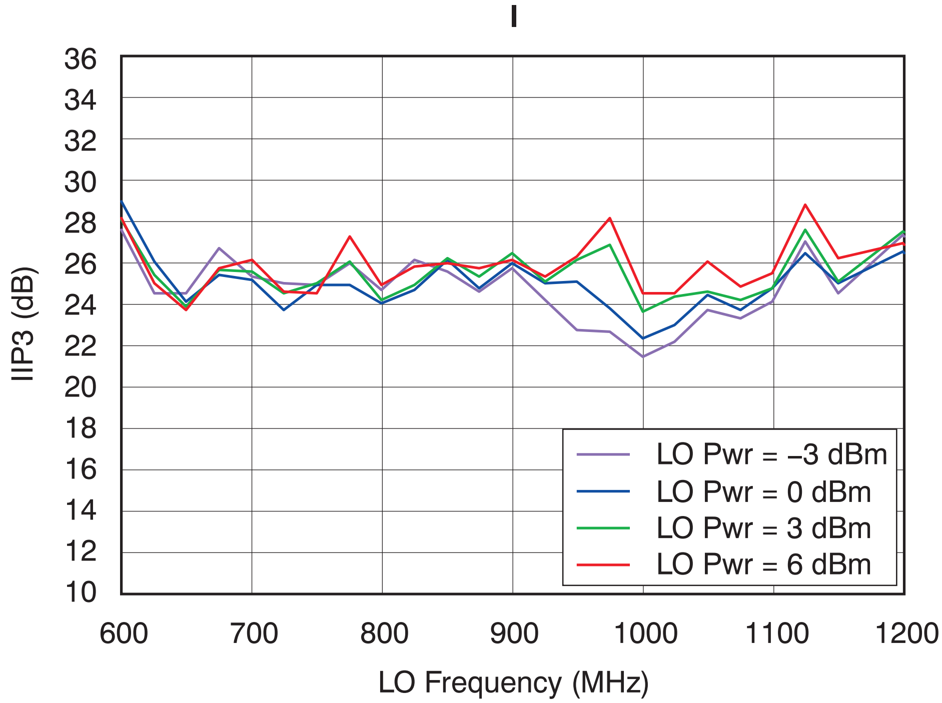


Figure 17.

TYPICAL CHARACTERISTICS (continued)

At V_{CC} = 5 V, LO power = 0 dBm, and T_A = +25°C, using balun Murata LDB21897M005C-001 (unless otherwise noted).

IIP3 vs LO FREQUENCY



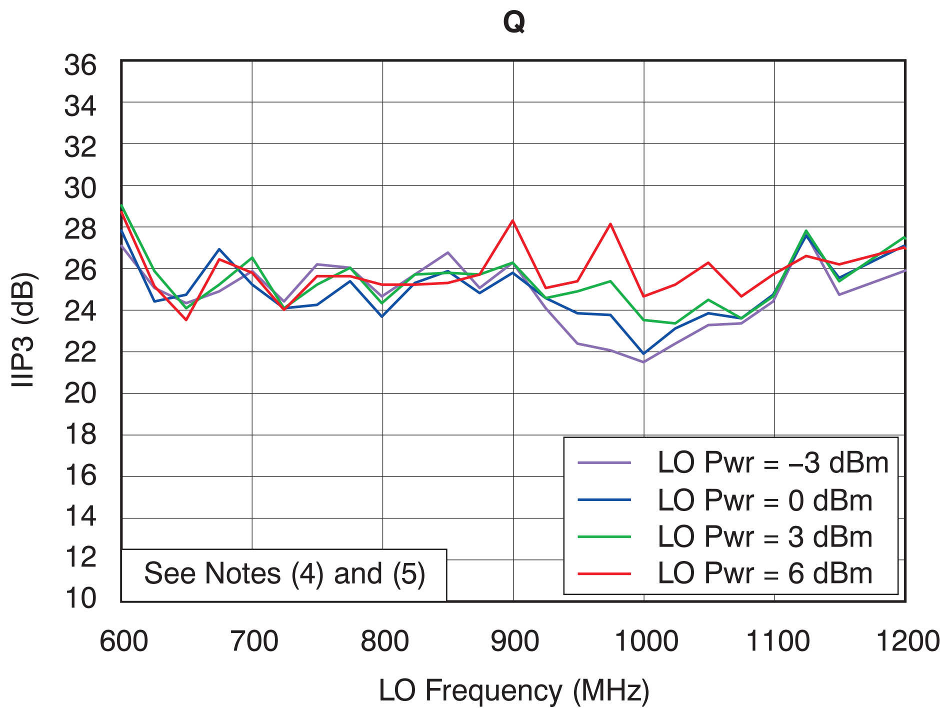
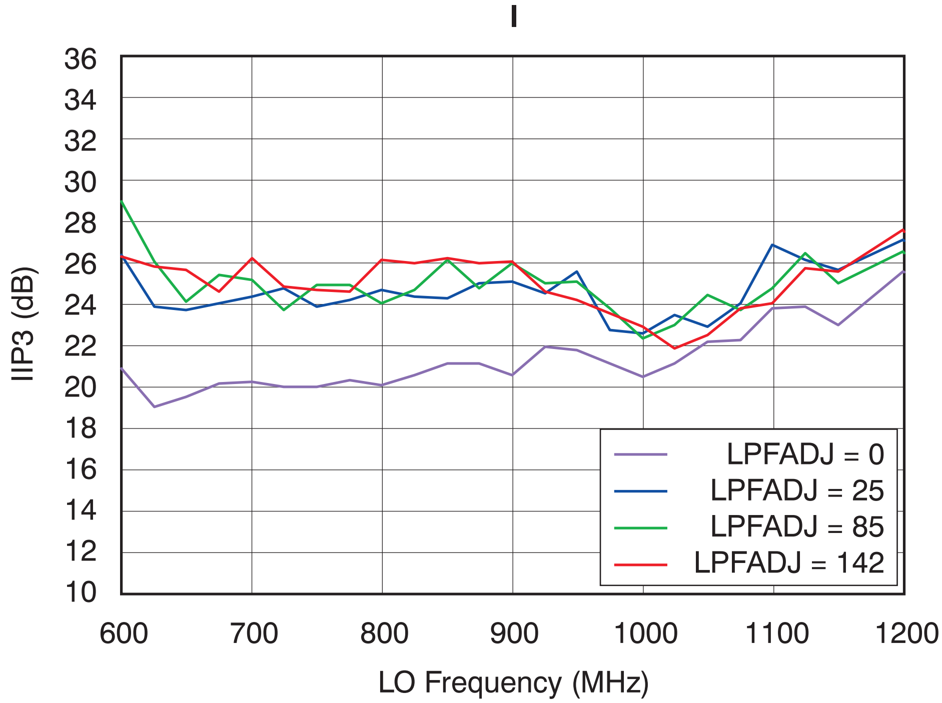


Figure 18.

TYPICAL CHARACTERISTICS (continued)

At V_{CC} = 5 V, LO power = 0 dBm, and T_A = +25°C, using balun Murata LDB21897M005C-001 (unless otherwise noted).

IIP3 vs LO FREQUENCY



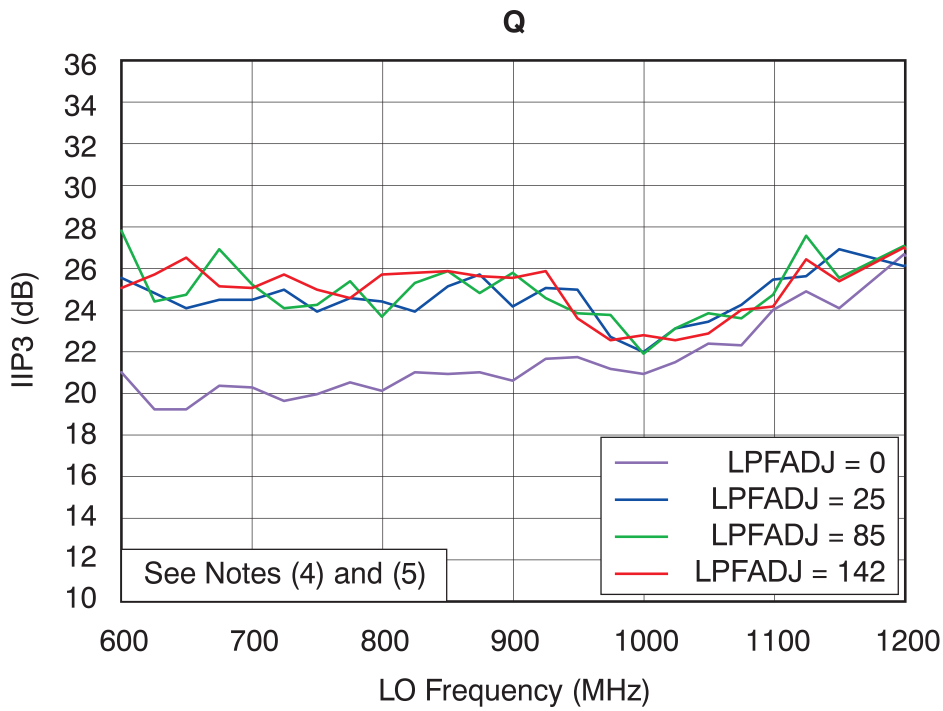


Figure 19.

TYPICAL CHARACTERISTICS (continued)

At V_{CC} = 5 V, LO power = 0 dBm, and T_A = +25°C, using balun Murata LDB21897M005C-001 (unless otherwise noted).

IIP2 vs IO FREQUENCY

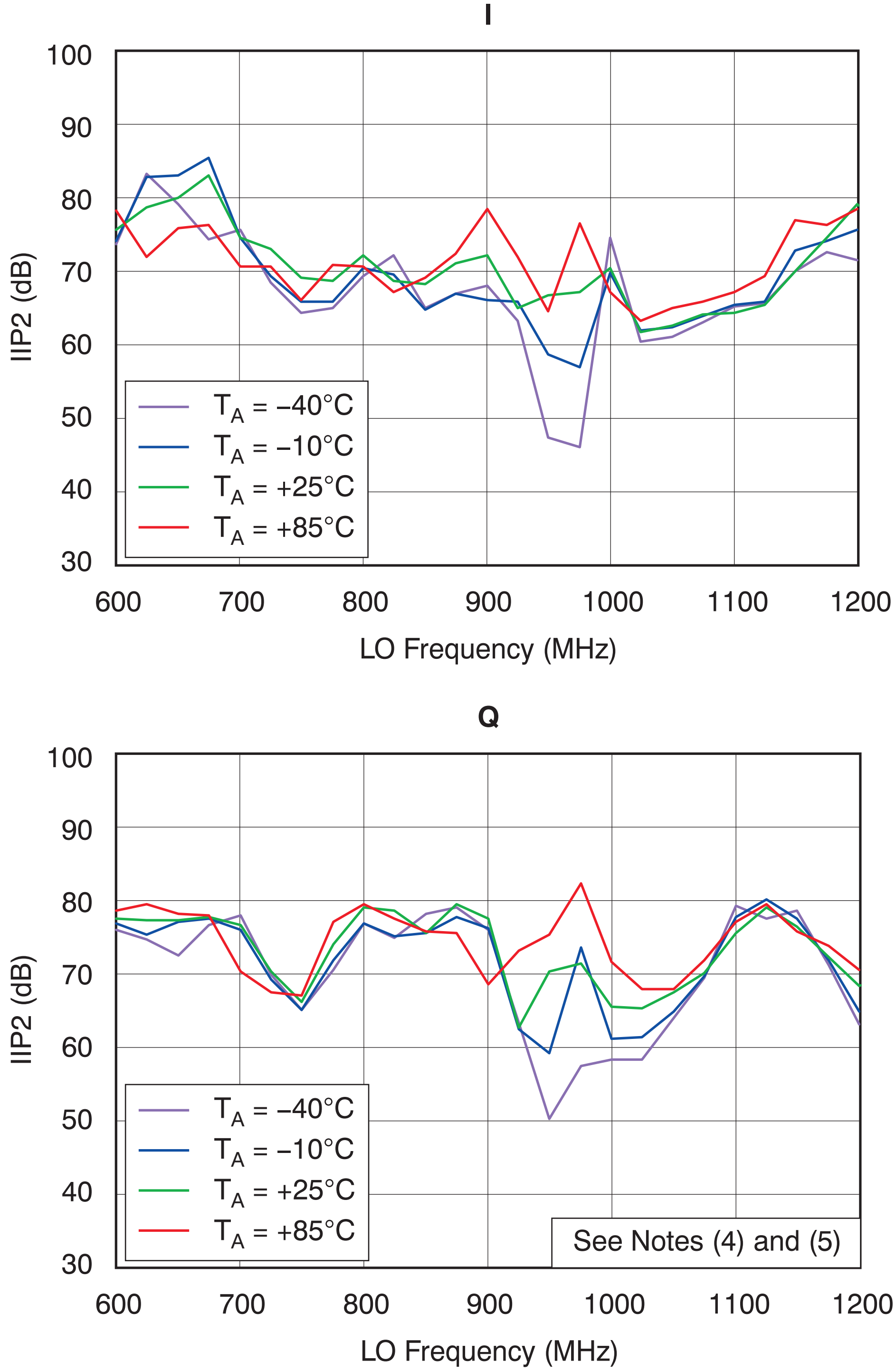
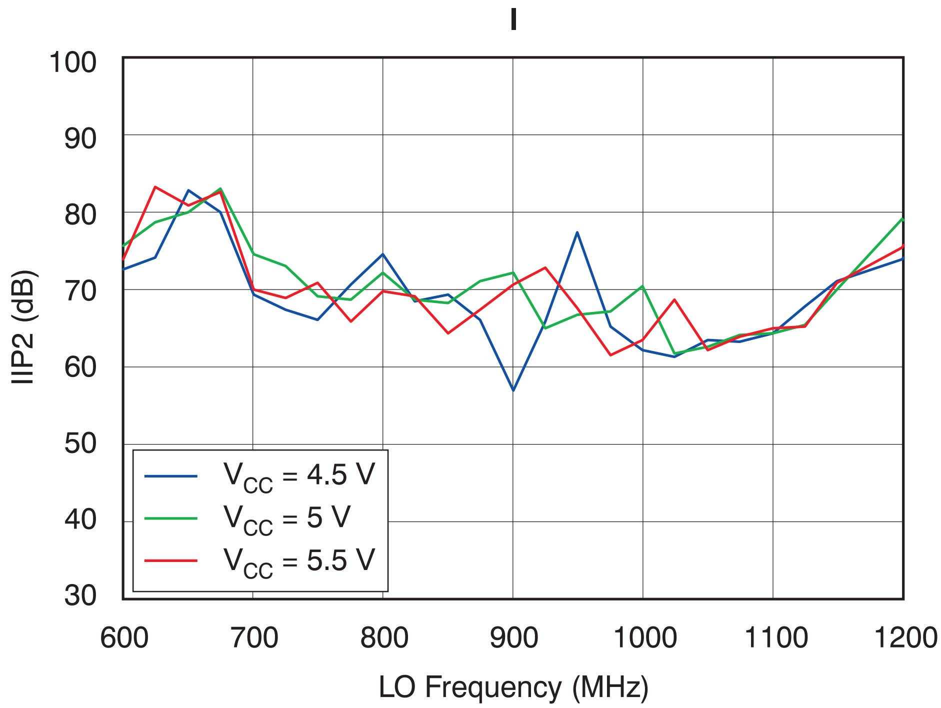


Figure 20.

TYPICAL CHARACTERISTICS (continued)

At V_{CC} = 5 V, LO power = 0 dBm, and T_A = +25°C, using balun Murata LDB21897M005C-001 (unless otherwise noted).

IIP2 vs LO FREQUENCY



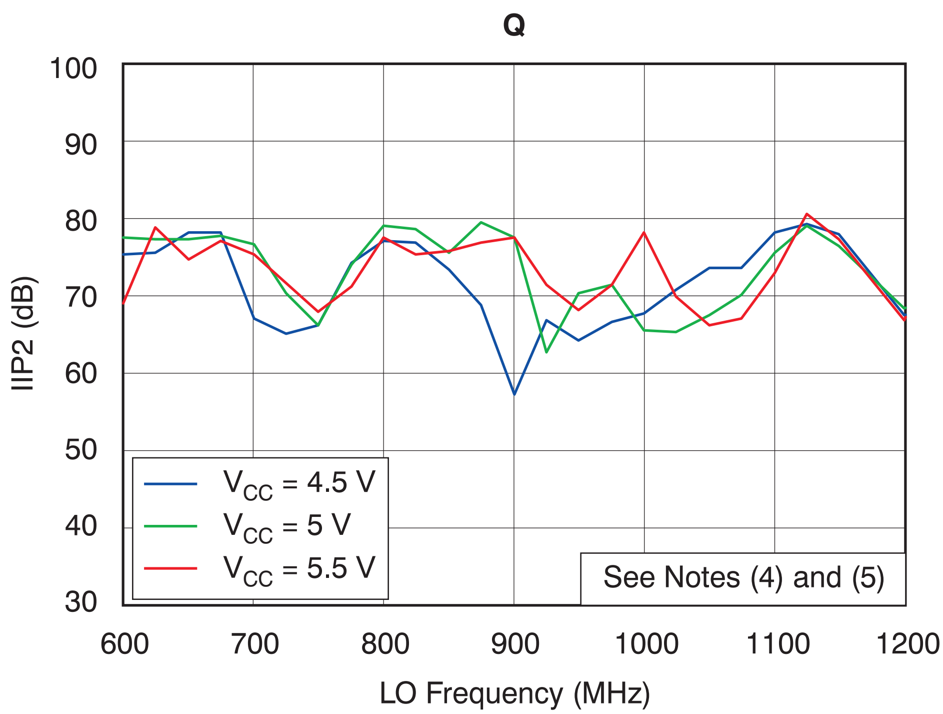
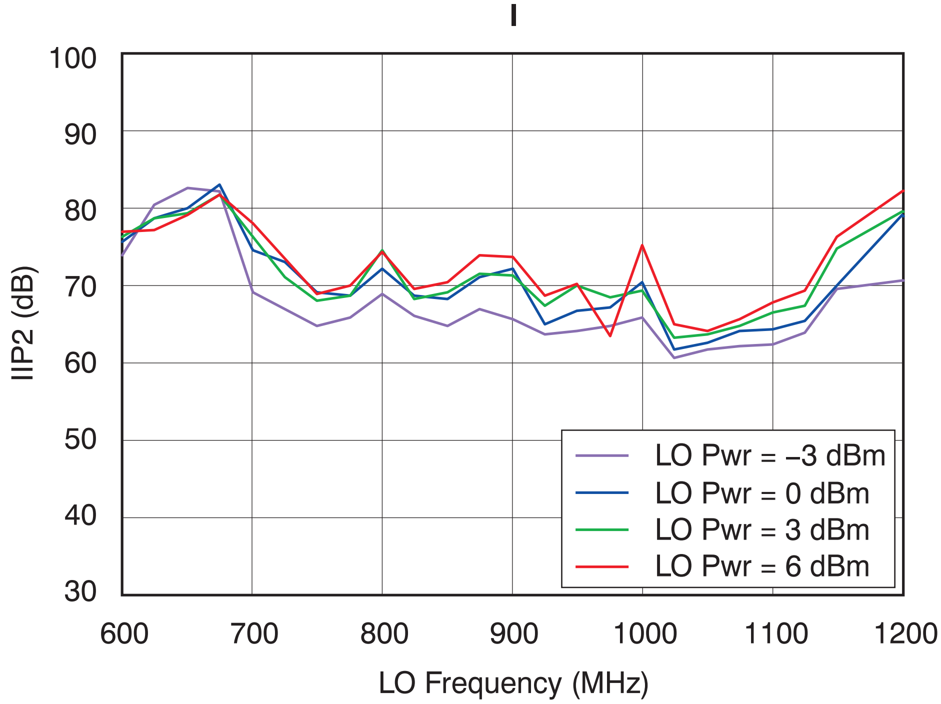


Figure 21.

TYPICAL CHARACTERISTICS (continued)

At V_{CC} = 5 V, LO power = 0 dBm, and T_A = +25°C, using balun Murata LDB21897M005C-001 (unless otherwise noted).

IIP2 vs LO FREQUENCY



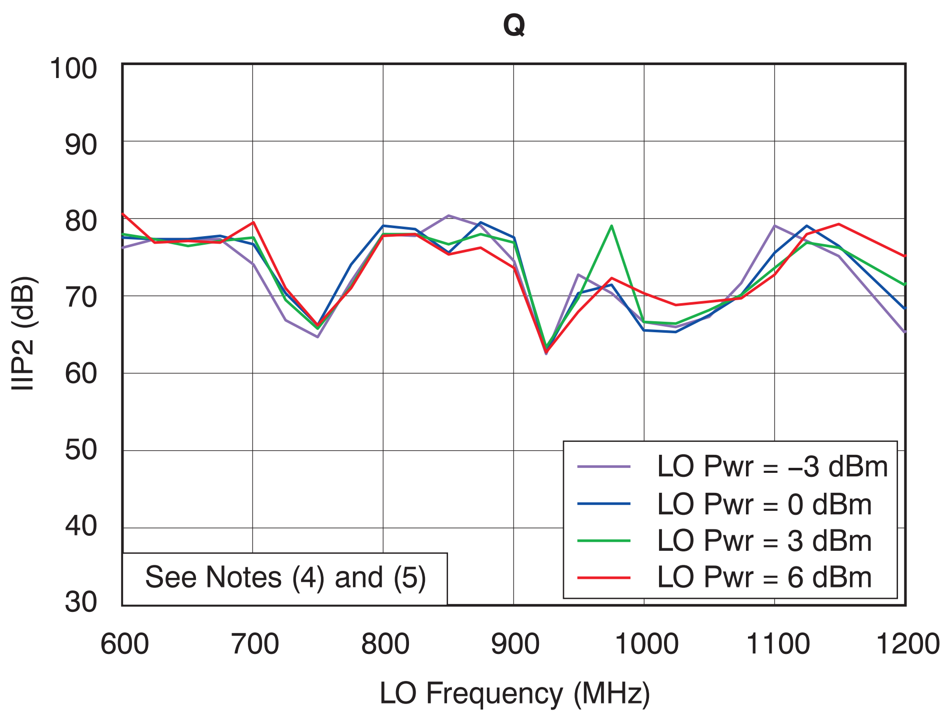
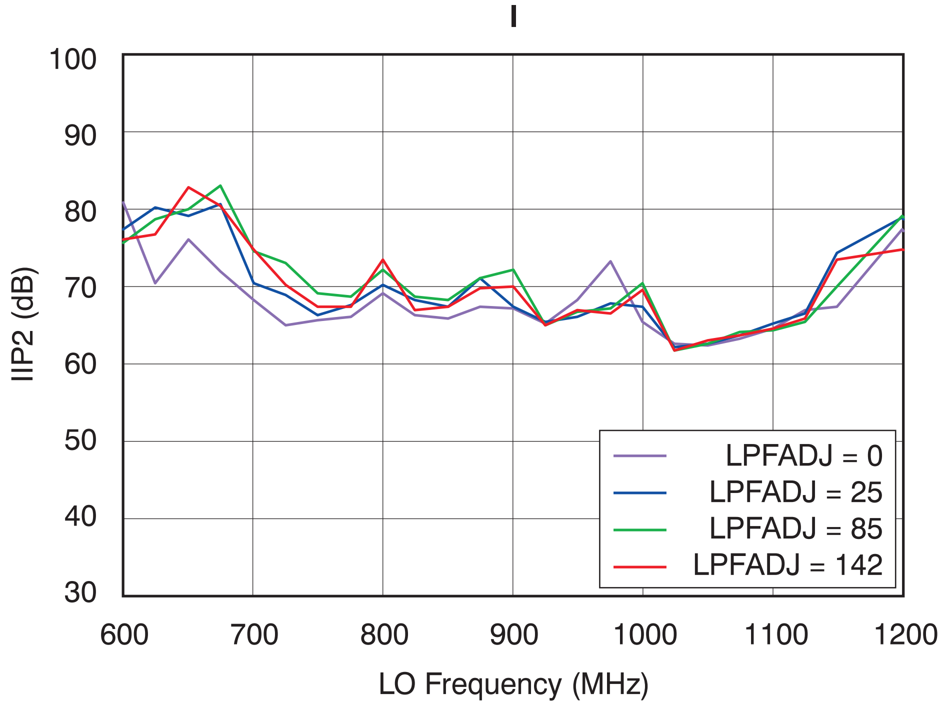


Figure 22.

TYPICAL CHARACTERISTICS (continued)

At V_{CC} = 5 V, LO power = 0 dBm, and T_A = +25°C, using balun Murata LDB21897M005C-001 (unless otherwise noted).

IIP2 vs LO FREQUENCY



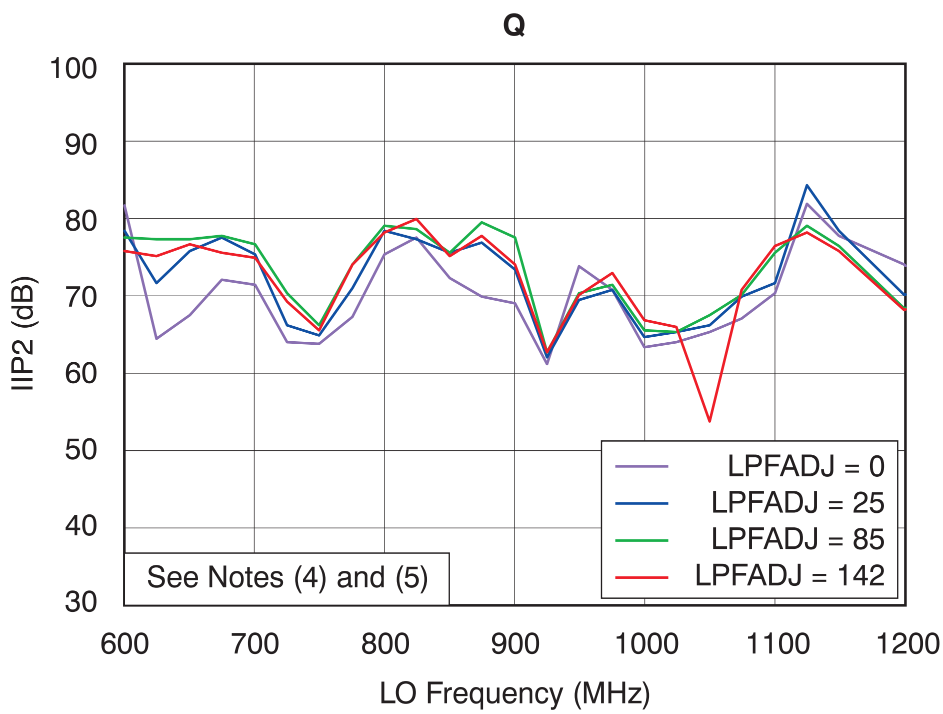


Figure 23.

TYPICAL CHARACTERISTICS (continued)

At V_{CC} = 5 V, LO power = 0 dBm, and T_A = +25°C, using balun Murata LDB21897M005C-001 (unless otherwise noted).

NOISE FIGURE vs LO FREQUENCY

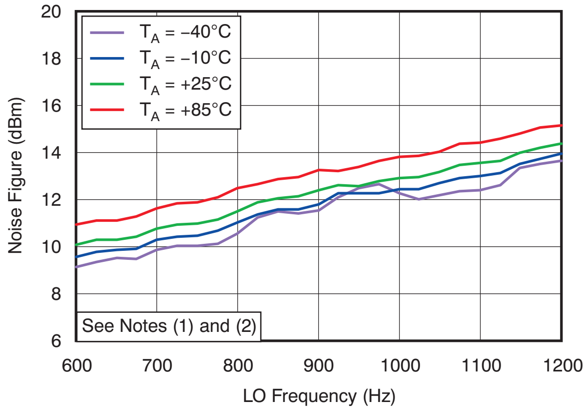


Figure 24.

NOISE FIGURE vs LO FREQUENCY

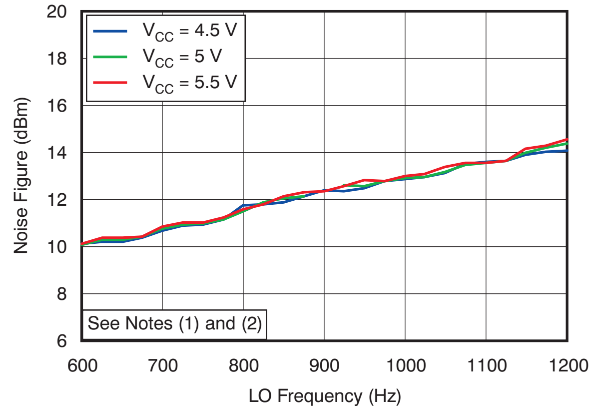


Figure 25.

NOISE FIGURE vs LO FREQUENCY

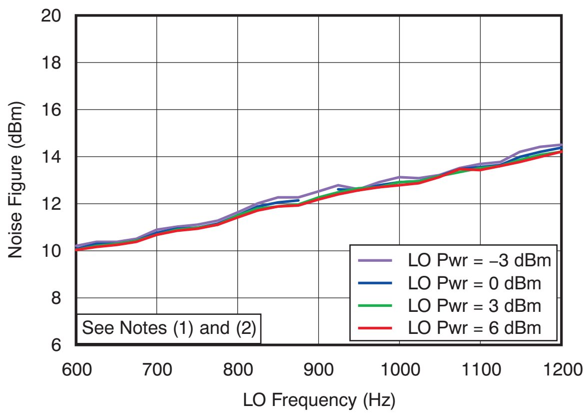


Figure 26.

OIP3 vs FREQUENCY OFFSET

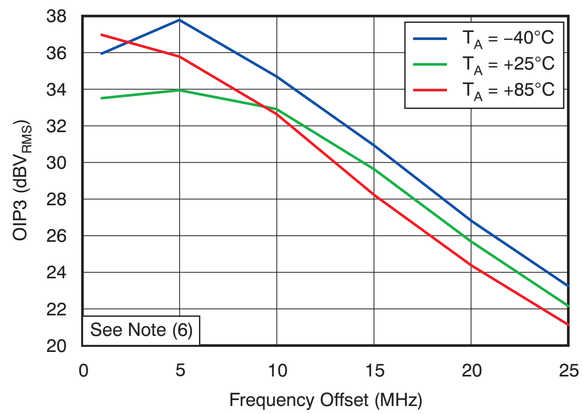


Figure 27.

OIP3 vs FREQUENCY OFFSET

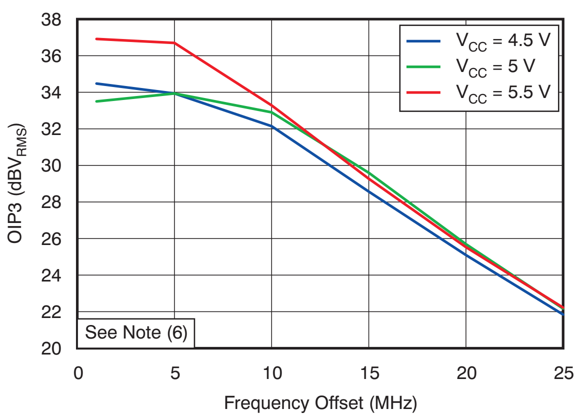


Figure 28.

OIP3 vs FREQUENCY OFFSET

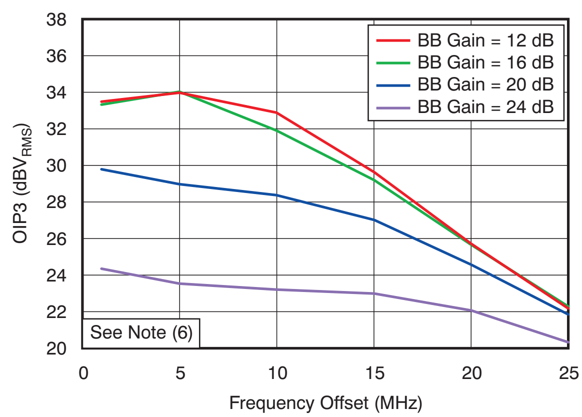


Figure 29.

TYPICAL CHARACTERISTICS (continued)

At V_{CC} = 5 V, LO power = 0 dBm, and T_A = +25°C, using balun Murata LDB21897M005C-001 (unless otherwise noted).

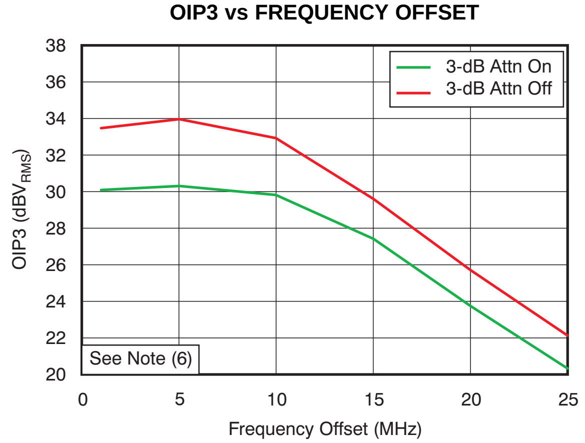


Figure 30.

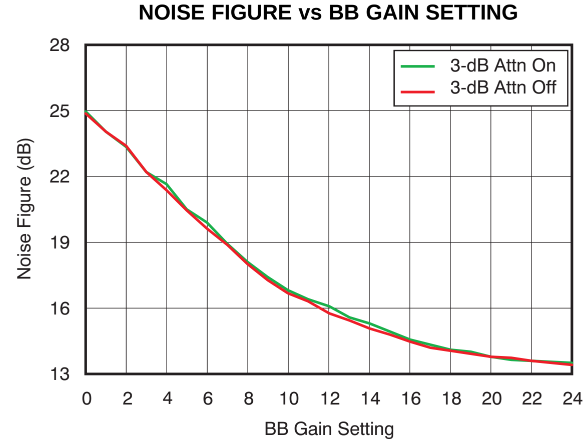


Figure 31.

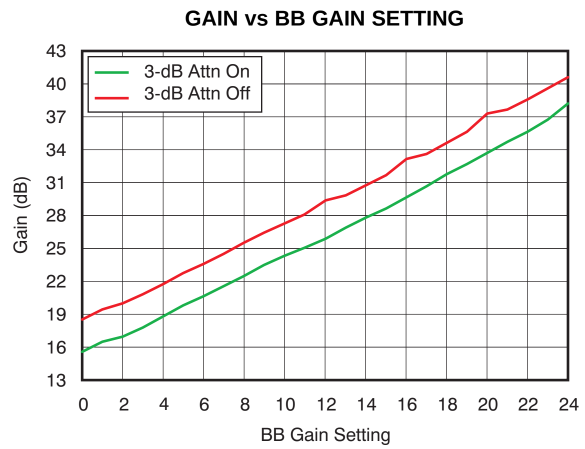


Figure 32.

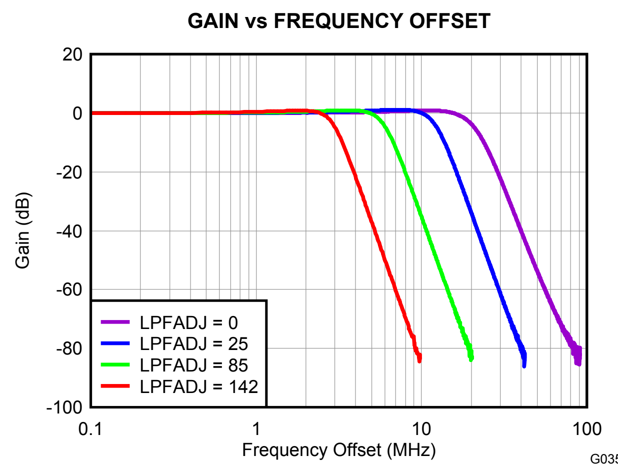


Figure 33.

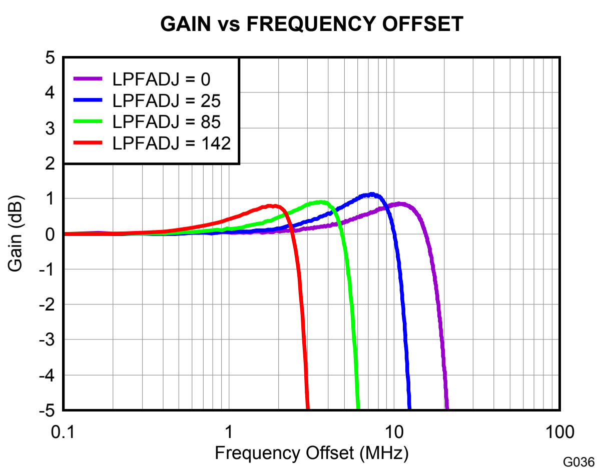


Figure 34.

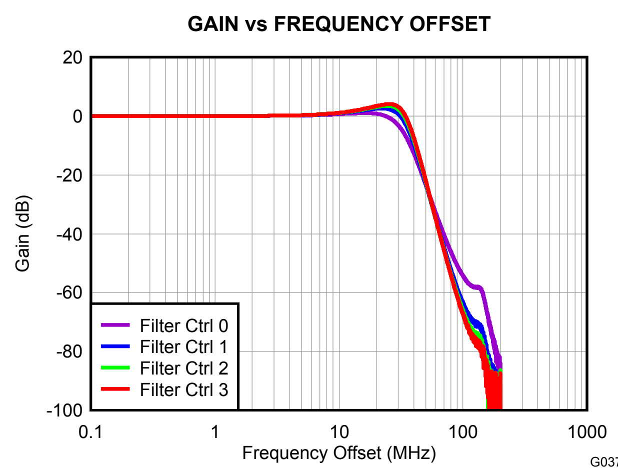


Figure 35.

TYPICAL CHARACTERISTICS (continued)

At V_{CC} = 5 V, LO power = 0 dBm, and T_A = +25°C, using balun Murata LDB21897M005C-001 (unless otherwise noted).

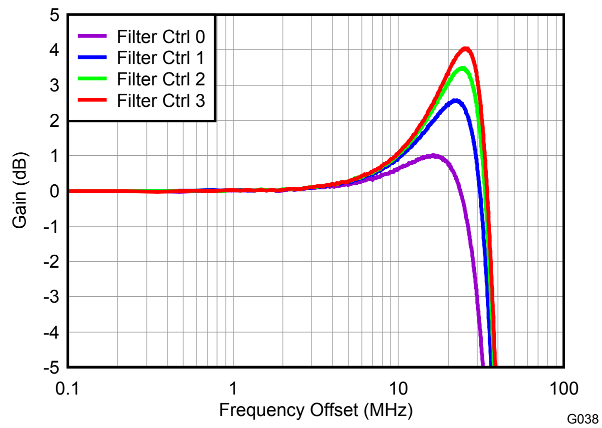


Figure 36.

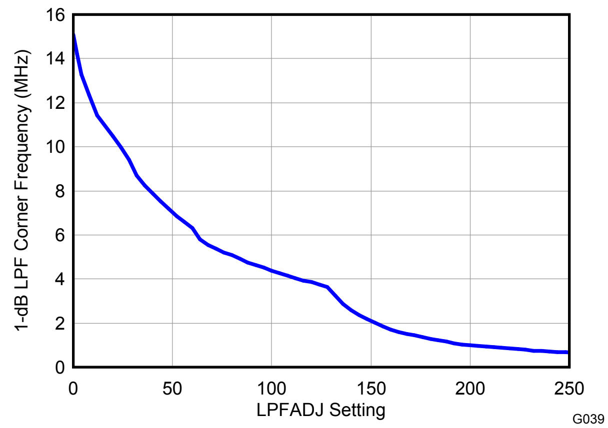


Figure 37.

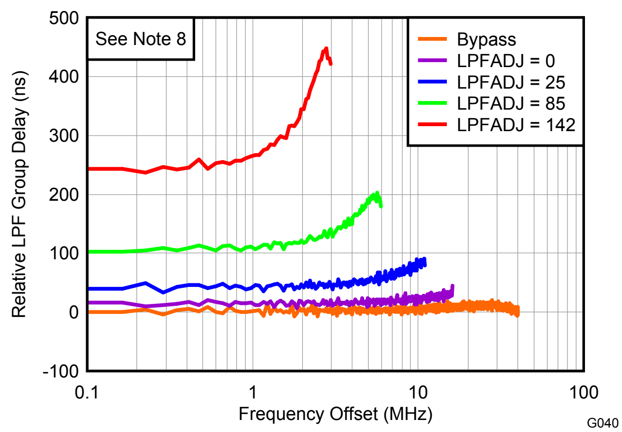


Figure 38.

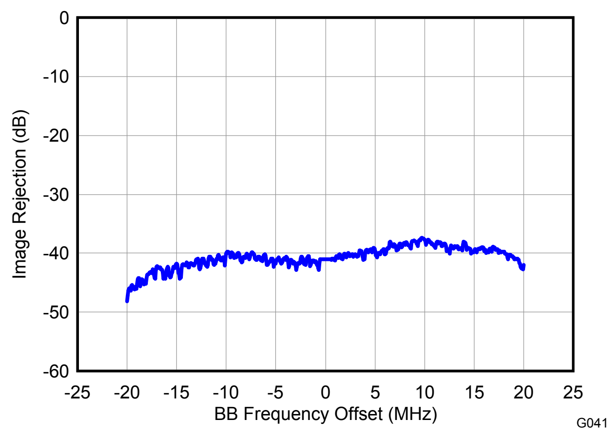


Figure 39.

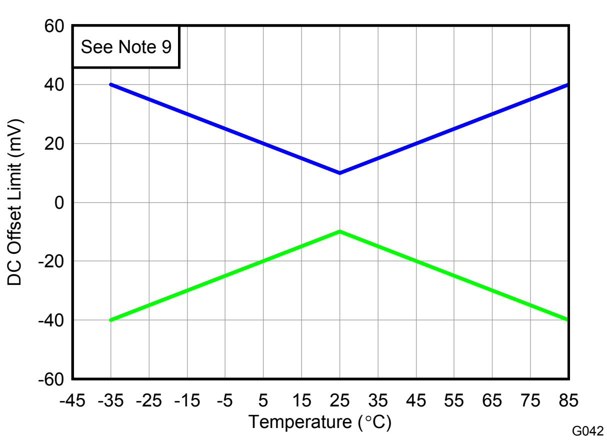


Figure 40.

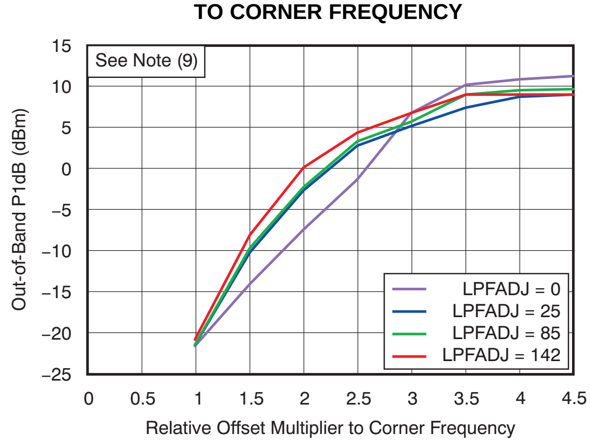


Figure 41.

REGISTER INFORMATION

SERIAL INTERFACE PROGRAMMING REGISTERS DEFINITION

The TRF371109 features a three-wire serial programming interface (SPI) that controls an internal 32-bit shift register. There are three signals that must be applied: CLOCK (pin 48), serial DATA (pin 47), and STROBE (pin 46). DATA (DB0–DB31) is loaded LSB-first and is read on the rising edge of CLOCK. STROBE is asynchronous to CLOCK, and at its rising edge the data in the shift register is loaded into the selected internal register. The first two bits (DB0–DB1) are the address to select the available internal registers.

READBACK Mode

The TRF371109 implements the capability to read back the content of the serial programming interface registers. In addition, it is possible to read back the status of the internal DAC registers that are automatically set after an auto dc-offset calibration. Each readback is composed by two phases: writing followed by the actual reading of the internal data (refer to Figure 42).

During the writing phase, a command is sent to the TRF371109 to set it in readback mode and to specify which register is to be read. In the proper reading phase, at each rising clock edge, the internal data is transferred into the READBACK pin and can be read at the following falling edge (LSB first). The first clock after LE goes high (end of writing cycle) is idle, and the following 32 clock pulses transfer the internal register content to the READBACK pin.

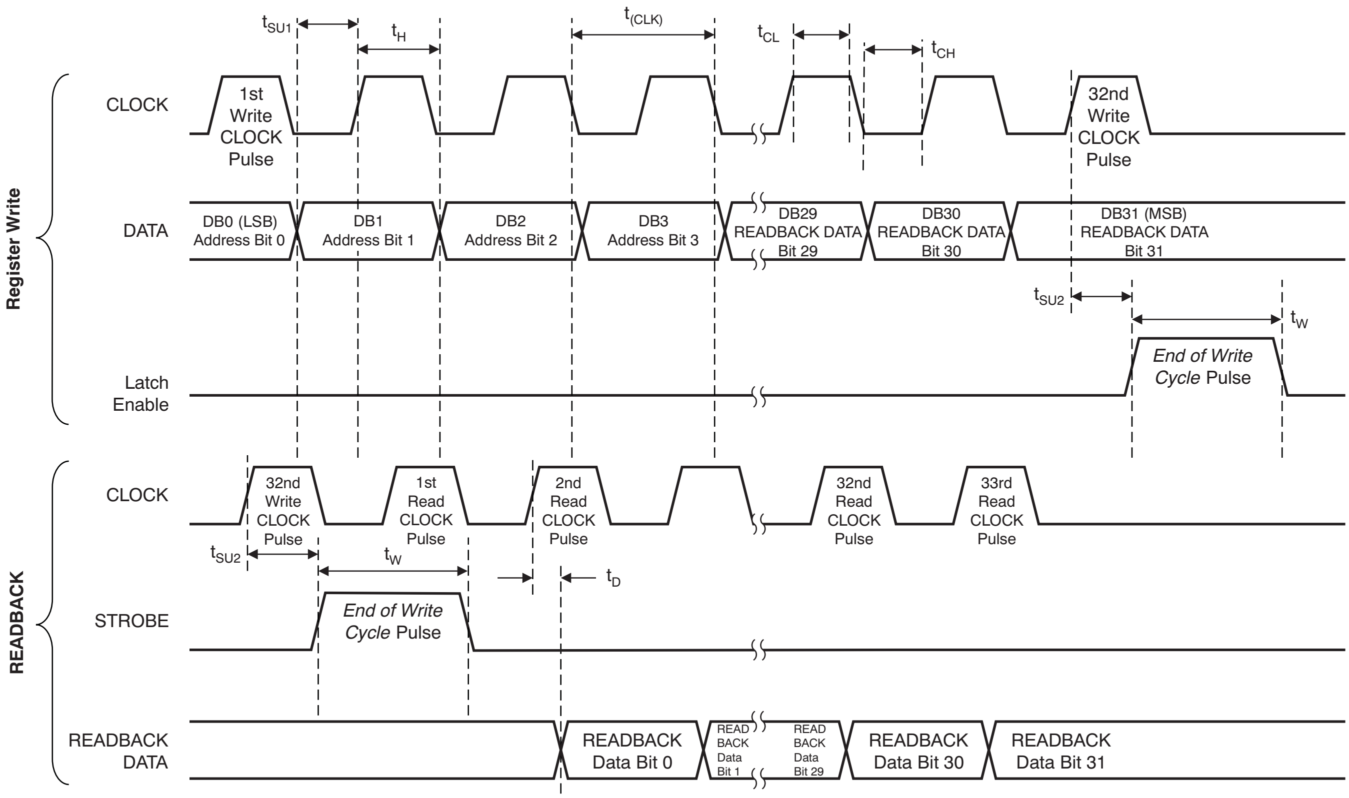


Figure 42. Serial Programming Timing Diagram

Table 1 shows the register summary. Table 2 through Table 6 list the device setup information for Register 1 to Register 5, respectively. Table 7 lists the device setup for Register 0.

Table 1. Register Summary(1)

Bit #	Reg 1	Reg 2	Bit #	Reg 3	Reg 5	Bit #	Reg 0
Bit0	Register address	Register address	Bit0	Register address	Register address	Bit0	Register address
Bit1			Bit1			Bit1	
Bit2			Bit2			Bit2	
Bit3	SPI bank addr	SPI bank addr	Bit3	SPI bank addr	SPI bank addr	Bit3	SPI bank addr
Bit4			Bit4			Bit4	
Bit5	PWD RF	En auto-cal	Bit5	ILoadA	Mix GM trim	Bit5	ID
Bit6	NU	IDAC for dc offset	Bit6			Bit6	
Bit7	PWD buf		Bit7		Mix LO trim	Bit7	NU
Bit8	P		Bit8			Bit8	
Bit9	NU		Bit9		LO trim	Bit9	
Bit10	PWD DC OFF DIG		Bit10			Bit10	
Bit11	NU		Bit11	ILoadB	Mix buf trim	Bit11	
Bit12	BB gain		Bit12			Bit12	
Bit13			Bit13		Fltr trim	Bit13	
Bit14		QDAC for dc offset	Bit14			Bit14	
Bit15			Bit15		Out buf trim	Bit15	
Bit16			Bit16			Bit16	DC offset Q DAC
Bit17	LPFADJ		Bit17	QLoadA	NU	Bit17	
Bit18			Bit18			Bit18	
Bit19			Bit19			Bit19	
Bit20			Bit20			Bit20	
Bit21			Bit21			Bit21	
Bit22		IDet	Bit22			Bit22	
Bit23			Bit23	QLoadB		Bit23	
Bit24		Cal sel	Bit24			Bit24	DC offset I DAC
Bit25	DC detector bandwidth	CLK div ratio	Bit25			Bit25	
Bit26			Bit26			Bit26	
Bit27	Fast gain		Bit27			Bit27	
Bit28	Gain sel	Cal clk sel	Bit28			Bit28	
Bit29	Osc test	Osc trim	Bit29	Bypass		Bit29	
Bit30	NU		Bit30	Fltr ctrl		Bit30	
Bit31	En 3dB attn		Bit31			Bit31	

(1) Register 4 is not used.

Table 2. Register 1 Device Setup

REGISTER 1	NAME	RESET VALUE	WORKING DESCRIPTION
Bit0	ADDR<0>	1	Register address
Bit1	ADDR<1>	0	
Bit2	ADDR<2>	0	
Bit3	ADDR<3>	1	SPI bank address
Bit4	ADDR<4>	0	
Bit5	PWD_MIX	0	Mixer power down (Off = '1')
Bit6	NU	0	Not used
Bit7	PWD_BUF	1	Mixer out test buffer power down (Off = '1')
Bit8	PWD_FILT	0	Baseband filter power down (Off = '1')
Bit9	NU	0	Not used
Bit10	PWD_DC_OFF_DIG	1	DC offset calibration power down (Off = '1')

Table 2. Register 1 Device Setup (continued)

REGISTER 1	NAME	RESET VALUE	WORKING DESCRIPTION
Bit11	NU	1	Not used
Bit12	BBGAIN_0	1	Baseband gain setting. Default = 15. Range is from 0 (minimum gain setting) to 24 (maximum gain setting). See the *Application Information* section for more information on gain setting and fast gain control options.
Bit13	BBGAIN_1	1	
Bit14	BBGAIN_2	1	
Bit15	BBGAIN_3	1	
Bit16	BBGAIN_4	0	
Bit17	LPFADJ_0	0	Sets programmable low-pass filter corner frequency. Range = 255 (lowest corner frequency) to 0 (highest corner frequency). Default value is 128.
Bit18	LPFADJ_1	0	
Bit19	LPFADJ_2	0	
Bit20	LPFADJ_3	0	
Bit21	LPFADJ_4	0	
Bit22	LPFADJ_5	0	
Bit23	LPFADJ_6	0	
Bit24	LPFADJ_7	1	
Bit25	EN_FLT_B0	0	Selects dc offset detector filter bandwidth. Setting {00, 01, 11} = {10 MHz, 10 kHz, 1 kHz}
Bit26	EN_FLT_B1	0	
Bit27	EN_FASTGAIN	0	Enable external fast-gain control
Bit28	GAIN_SEL	0	Fast-gain control multiplier bit (×2 = 1)
Bit29	OSC_TEST	0	Enables Osc out on readback pin if = 1
Bit30	NU	0	Not used
Bit31	EN 3dB Attn	0	Enables output 3-dB attenuator

EN_FLT_B0/1: These bits control the bandwidth of the detector used to measure the dc offset during the automatic calibration. There is an RC filter in front of the detector that can be fully bypassed. EN_FLT_B0 controls the resistor (bypass = 1), while EN_FLT_B1 controls the capacitor (bypass = 1). The typical 3-dB cutoff frequencies of the detector bandwidth are summarized in Table 3 (see the *Application Information* section for more detail on the dc offset calibration and the detector bandwidth).

Table 3. Detector Bandwidth Settings

EN_FLT_B1	EN_FLT_B0	TYPICAL 3-dB CUTOFF FREQ	NOTES
x	0	10 MHz	Maximum bandwidth, bypass R, C
0	1	10 kHz	Enable R
1	1	1 kHz	Minimum bandwidth, enable R, C

Table 4. Register 2 Device Setup

REGISTER 2	NAME	RESET VALUE	WORKING DESCRIPTION
Bit0	ADDR<0>	0	Register address
Bit1	ADDR<1>	1	
Bit2	ADDR<2>	0	
Bit3	ADDR<3>	1	SPI bank address
Bit4	ADDR<4>	0	
Bit5	EN_AUTOCAL	0	Enable autocal when = '1'; reset to '0' when done.

Table 4. Register 2 Device Setup (continued)

REGISTER 2	NAME	RESET VALUE	WORKING DESCRIPTION
Bit6	IDAC_BIT0	0	I-DAC bits to be set during manual dc offset cal
Bit7	IDAC_BIT1	0	
Bit8	IDAC_BIT2	0	
Bit9	IDAC_BIT3	0	
Bit10	IDAC_BIT4	0	
Bit11	IDAC_BIT5	0	
Bit12	IDAC_BIT6	0	
Bit13	IDAC_BIT7	1	
Bit14	QDAC_BIT0	0	Q-DAC bits to be set during manual dc offset cal
Bit15	QDAC_BIT1	0	
Bit16	QDAC_BIT2	0	
Bit17	QDAC_BIT3	0	
Bit18	QDAC_BIT4	0	
Bit19	QDAC_BIT5	0	
Bit20	QDAC_BIT6	0	
Bit21	QDAC_BIT7	1	
Bit22	IDET_B0	1	Set reference current for digital calibration; Settings {00 to 11} = {50 μA to 200 μA}. Setting '00' = highest resolution.
Bit23	IDET_B1	1	
Bit24	CAL_SEL	1	DC offset calibration select. '0' = manual cal; '1' = autocal.
Bit25	Clk_div_ratio<0>	0	Clk divider ratio. Setting {000 to 111} = {1, 8, 16, 128, 256, 1024, 2048, 16684}. A higher div ratio (slower clk) improves cal accuracy and reduces speed.
Bit26	Clk_div_ratio<1>	0	
Bit27	Clk_div_ratio<2>	0	
Bit28	Cal_clk_sel	1	Select internal oscillator when 1, SPI clk when '0'
Bit29	Osc_trim<0>	1	Internal oscillator frequency trimming; Setting {000} = ~300 kHz; Setting {111} = ~1.8 MHz. Nominal setting {110} = ~900 kHz.
Bit30	Osc_trim<1>	1	
Bit31	Osc_trim<2>	0	

Table 5. Register 3 Device Setup

REGISTER 3	NAME	RESET VALUE	WORKING DESCRIPTION
Bit0	ADDR<0>	1	Register address
Bit1	ADDR<1>	1	
Bit2	ADDR<2>	0	
Bit3	ADDR<3>	1	SPI bank address
Bit4	ADDR<4>	0	
Bit5	ILOAD_a<0>	0	I mixer offset side A
Bit6	ILOAD_a<1>	0	
Bit7	ILOAD_a<2>	0	
Bit8	ILOAD_a<3>	0	
Bit9	ILOAD_a<4>	0	
Bit10	ILOAD_a<5>	0	
Bit11	ILOAD_b<0>	0	I mixer offset side B
Bit12	ILOAD_b<1>	0	
Bit13	ILOAD_b<2>	0	
Bit14	ILOAD_b<3>	0	
Bit15	ILOAD_b<4>	0	
Bit16	ILOAD_b<5>	0	

Table 5. Register 3 Device Setup (continued)

REGISTER 3	NAME	RESET VALUE	WORKING DESCRIPTION
Bit17	QLOAD_a<0>	0	Q mixer offset side A
Bit18	QLOAD_a<1>	0	
Bit19	QLOAD_a<2>	0	
Bit20	QLOAD_a<3>	0	
Bit21	QLOAD_a<4>	0	
Bit22	QLOAD_a<5>	0	
Bit23	QLOAD_b<0>	0	Q mixer offset side B
Bit24	QLOAD_b<1>	0	
Bit25	QLOAD_b<2>	0	
Bit26	QLOAD_b<3>	0	
Bit27	QLOAD_b<4>	0	
Bit28	QLOAD_b<5>	0	
Bit29	Bypass	0	Engage filter bypass
Bit30	Fltr Ctrl_b<0>	1	Used to adjust for filter peaking response; set to 0 in bypass mode, 1 otherwise
Bit31	Fltr Ctrl_b<1>	0	

I/Q Mixer Load A/B: these bits adjust the load on the mixer output. All values should be 0. No modification is necessary.

Register 4: No programming required for Register 4.

Table 6. Register 5 Device Setup

REGISTER 5	NAME	RESET VALUE	WORKING DESCRIPTION
Bit0	ADDR<0>	1	Register address
Bit1	ADDR<1>	0	
Bit2	ADDR<2>	1	
Bit3	ADDR<3>	1	SPI bank address
Bit4	ADDR<4>	0	
Bit5	MIX_GM_TRIM<0>	1	Mixer gm current trim
Bit6	MIX_GM_TRIM<1>	0	
Bit7	MIX_LO_TRIM<0>	1	Mixer switch core VCM trim
Bit8	MIX_LO_TRIM<1>	0	
Bit9	LO_TRIM<0>	1	LO buffers current trim
Bit10	LO_TRIM<1>	0	
Bit11	MIX_BUFF_TRIM<0>	1	Mixer output buffer current trim
Bit12	MIX_BUFF_TRIM<1>	0	
Bit13	FLTR_TRIM<0>	1	Filter current trim
Bit14	FLTR_TRIM<1>	0	
Bit15	OUT_BUFF_TRIM<0>	1	Filter output buffer current trim
Bit16	OUT_BUFF_TRIM<1>	0	

Table 6. Register 5 Device Setup (continued)

REGISTER 5	NAME	RESET VALUE	WORKING DESCRIPTION
Bit17		0	
Bit18		0	
Bit19		0	
Bit20		0	
Bit21		0	
Bit22		0	
Bit23		0	
Bit24	NU	0	Not used
Bit25		0	
Bit26		0	
Bit27		0	
Bit28		0	
Bit29		0	
Bit30		0	
Bit31		0	

Readback (Write Command)

0	0	0	1	0	Zero Fill										
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15
Zero fill												Register address			1
Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31

Reg 0:DAC/Device ID Readback

Register Address			SPI Bank Addr		ID		NU								
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15
DC offset Q DAC								DC offset I DAC							
Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31

Table 7. Register 0 Device Setup (Read-Only)

READBACK REGISTER	NAME	RESET VALUE	WORKING DESCRIPTION
Bit0	ADDR<0>	0	Select SPI register 1 to 5
Bit1	ADDR<1>	0	
Bit2	ADDR<2>	0	
Bit3	ADDR<3>	1	Select SPI bank 1 to 3
Bit4	ADDR<4>	0	
Bit5	ID<0>	1	Version ID: 01 = –25
Bit6	ID<1>	0	
Bit7	NU	0	Not used
Bit8		0	
Bit9		0	
Bit10		0	
Bit11		0	
Bit12		0	
Bit13		0	
Bit14		0	
Bit15		0	

Table 7. Register 0 Device Setup (Read-Only) (continued)

<table>
<tr><th>READBACK REGISTER</th><th>NAME</th><th>RESET VALUE</th><th>WORKING DESCRIPTION</th></tr>
<tr><td>Bit16</td><td>DC_OFFSET_Q<0></td><td>0</td><td rowspan="8">DC offset DAC Q register</td></tr>
<tr><td>Bit17</td><td>DC_OFFSET_Q<1></td><td>0</td></tr>
<tr><td>Bit18</td><td>DC_OFFSET_Q<2></td><td>0</td></tr>
<tr><td>Bit19</td><td>DC_OFFSET_Q<3></td><td>0</td></tr>
<tr><td>Bit20</td><td>DC_OFFSET_Q<4></td><td>0</td></tr>
<tr><td>Bit21</td><td>DC_OFFSET_Q<5></td><td>0</td></tr>
<tr><td>Bit22</td><td>DC_OFFSET_Q<6></td><td>0</td></tr>
<tr><td>Bit23</td><td>DC_OFFSET_Q<7></td><td>1</td></tr>
<tr><td>Bit24</td><td>DC_OFFSET_I<0></td><td>0</td><td rowspan="8">DC offset DAC I register</td></tr>
<tr><td>Bit25</td><td>DC_OFFSET_I<1></td><td>0</td></tr>
<tr><td>Bit26</td><td>DC_OFFSET_I<2></td><td>0</td></tr>
<tr><td>Bit27</td><td>DC_OFFSET_I<3></td><td>0</td></tr>
<tr><td>Bit28</td><td>DC_OFFSET_I<4></td><td>0</td></tr>
<tr><td>Bit29</td><td>DC_OFFSET_I<5></td><td>0</td></tr>
<tr><td>Bit30</td><td>DC_OFFSET_I<6></td><td>0</td></tr>
<tr><td>Bit31</td><td>DC_OFFSET_I<7></td><td>1</td></tr>
</table>

APPLICATION INFORMATION

Gain Control

The TRF371109 integrates a baseband programmable gain amplifier (PGA) that provides 24 dB of gain range with 1-dB steps. The PGA gain is controlled through SPI by a 5-bit word (register 1 bits<12,16>). Alternatively, the PGA can be programmed by a combination of five bits programmed through the SPI and three parallel external bits (pins Gain_B2, Gain_B1, Gain_B0). The external bits are used to reduce the PGA setting quickly without having to reprogram the SPI registers. The fast gain control multiplier bit (register 1, bit 28) sets the step size of each bit to either 1 dB or 2 dB. This configuration allows a fast gain reduction of 0 dB to 7 dB in 1-dB steps or 0 dB to 14 dB in 2-dB steps.

The PGA gain control word (BBgain<0,4>) can be programmed to a setting between 0 and 24. This word is the SPI programmed gain (register 1 bits<12,16>) minus the parallel external three bits, as shown in Figure 43. Note that the PGA gain setting rails at 0 and does not go any lower. Typical applications set the nominal PGA gain setting to 17 and use the fast gain control bits to protect the analog-to-digital converter (ADC) in the event of a strong input jammer signal.

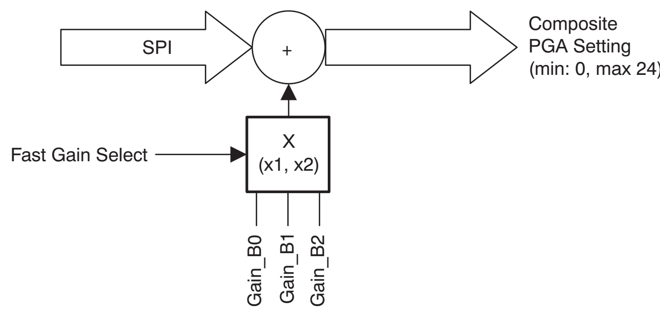


Figure 43. PGA Gain Control Word

For example, if a PGA gain setting of 19 is desired, then the SPI can be programmed directly to a value of 19. Alternatively, the SPI gain register can be programmed to 24 and the parallel external bits set to '101' (binary), corresponding to 5-dB reduction.

Automated DC Offset Calibration

The TRF371109 provides an automatic calibration procedure for adjusting the dc offset in the baseband I/Q paths. The internal calibration requires a clock in order to function. The TRF371109 can use the internal relaxation oscillator or the external SPI clock. Using the internal oscillator is the preferred method, which is selected by setting the Cal_Sel_Clk (register 2, bit 28) to '1'. The internal oscillator frequency is set through the Osc_Trim bits (register 2, bits <29,31>). The oscillator frequency is detailed in Table 8.

Table 8. Internal Oscillator Frequency Control

OSC_TRIM<2>	OSC_TRIM<1>	OSC_TRIM<0>	FREQUENCY
0	0	0	300 kHz
0	0	1	500 kHz
0	1	0	700 kHz
0	1	1	900 kHz
1	0	0	1.1 MHz
1	0	1	1.3 MHz
1	1	0	1.5 MHz
1	1	1	1.8 MHz

The default settings of these registers correspond to a 900-kHz oscillator frequency. This frequency is sufficient for auto calibration and does not need to be modified.

The output full-scale range of the internal dc offset correction digital-to-analog converters (DACs) is programmable (IDET_B<0,1, register 2 bit<22,23>). The range is shown in Table 9.

Table 9. DC Offset Correction DAC Programmable Range

I(Q) Det_B0	I(Q) Det_B1	FULL-SCALE
0	0	50 µA
0	1	100 µA
1	0	150 µA
1	1	200 µA

The I- and Q-channel output maximum dc offset correction range can be calculated by multiplying the values in Table 9 by the baseband PGA gain. The LSB of the digital correction depends on the programmed maximum correction range. For optimum resolution and best correction. the dc offset DAC range should be set to 10 mV for both the I- and Q-channels with the PGA gain set for the nominal condition. The dc offset correction DAC output is affected by changes in the PGA gain; if the initial calibration yields optimum results, however, then PGA gain adjustment during normal operation does not significantly impair the dc offset balance. For example, if the optimized calibration yields a dc offset balance of 2 mV at a gain setting of 17, then the dc offset maintains a balance of less than 10 mV as the gain is adjusted ±7 dB.

The dc offset correction DACs are programmed from the internal registers when the AUTO_CAL bit (register 2, bit 24) is set to '1'. At start-up, the internal registers are loaded at half-scale, corresponding to a decimal value of 128. The auto calibration is initiated by toggling the EN_AUTOCAL bit (register 2, bit 5) to '1'. When the calibration is complete, this bit automatically resets to '0'. During calibration, the RF Local Oscillator (LO) must be applied.

The dc offset DAC state is stored in the internal registers and maintained as long as the power supply remains on, or until a new calibration begins.

The required clock speed for the optimum calibration is determined by the internal detector behavior (integration bandwidth, gain, and sensitivity). The input bandwidth of the detector can be adjusted by changing the cutoff frequency of the RC low-pass filter (LPF) in front of the detector (register 1, bits 25-26). EN_FLT_B0 controls the resistor (bypass = '1') and EN_FLT_B1 controls the capacitor (bypass = '1'). The typical 3-dB cutoff frequencies of the detector bandwidth are summarized in Table 3. The clock speed can be slowed down by selecting a clock divider ratio (register 2, bits 25-27).

The detector has more averaging time the slower the clock; therefore, it can be desirable to slow down the clock speed for a given condition to achieve optimum results. For example, if there is no RF present on the RF input port, the detection filter can be left wide (10 MHz) and the clock divider can be left at *divide-by-1*. The auto calibration yields a dc offset balance between the differential baseband output ports (I and Q) that is less than 15 mV. Some minor improvement may be obtained by increasing the averaging of the detector through increasing the clock divider up to 256.

On the other hand, if there is a modulated RF signal present at the input port, it is desirable to reduce the detector bandwidth to filter out most of the modulated signal. The detector bandwidth can be set to a 1-kHz corner frequency. With the modulated signal present and with the detection bandwidth reduced, additional averaging is required to get the optimum results. A clock divider setting of 1024 yields optimum results.

Of course, an increase in the averaging is possible by increasing the clock divider at the expense of a longer converging time. The convergence time can be calculated by the following:

$$\tau_C = \frac{(\text{Auto\_Cal\_Clk\_Cycles}) \times (\text{Clk\_Divider})}{\text{Osc\_Freq}} \tag{1}$$

For the case with a clock divider of 1024 and with the nominal oscillator frequency of 900 kHz, the convergence time is:

$$\tau_C = \frac{(9) \times (1024)}{900\ \text{kHz}} = 10.24\ \text{ms} \tag{2}$$

Alternate Method for Adjusting DC Offset

The internal registers that control the internal dc current DAC are accessible through the SPI and provide a user-programmable method for implementing the dc offset calibration. To employ this option, the CAL_SEL bit must be set to '0'. During this calibration, an external instrument monitors the output dc offset between the I/Q differential outputs and programs the internal registers (IDAC_BIT<0,7> and QDAC_BIT<0,7> bits) to cancel the dc offset.

PCB Layout Guidelines

The TRF371109 device is fitted with a ground slug on the back of the package that must be soldered to the printed circuit board (PCB) ground with adequate ground vias to ensure good thermal and electrical connections. The recommended via pattern and ground pad dimensions are shown in Figure 44. The recommended via diameter is 8 mils (0.2 mm). The ground pins of the device can be directly tied to the ground slug pad for a low-inductance path to ground. Additional ground vias may be added if space allows. The no-connect (NC) pins can also be tied to the ground plane.

Decoupling capacitors at each of the supply pins are recommended. The high-frequency decoupling capacitors for the RF mixers (VCCMIX) should be placed close to the respective pins. The value of the capacitor should be chosen to provide a low-impedance RF path to ground at the frequency of operation. Typically, this value is approximately 10 pF or lower. The other decoupling capacitors at the other supply pins should be kept as close as possible to the respective pins.

The device exhibits symmetry with respect to the quadrature output paths. It is recommended that the PCB layout maintain that symmetry in order to ensure that the quadrature balance of the device is not impaired. The I/Q output traces should be routed as differential pairs and the respective lengths all kept equal to each other. Decoupling capacitors for the supply pins should be kept symmetrical where possible. The RF differential input lines related to the RF input and the LO input should also be routed as differential lines with the respective lengths kept equal. If an RF balun is used to convert a single-ended input to a differential input, then the RF balun should be placed close to the device. Implement the RF balun layout according to the manufacturer guidelines to provide best gain and phase balance to the differential outputs. On the RF traces, maintain proper trace widths to keep the characteristic impedance of the RF traces at a nominal 50 Ω.

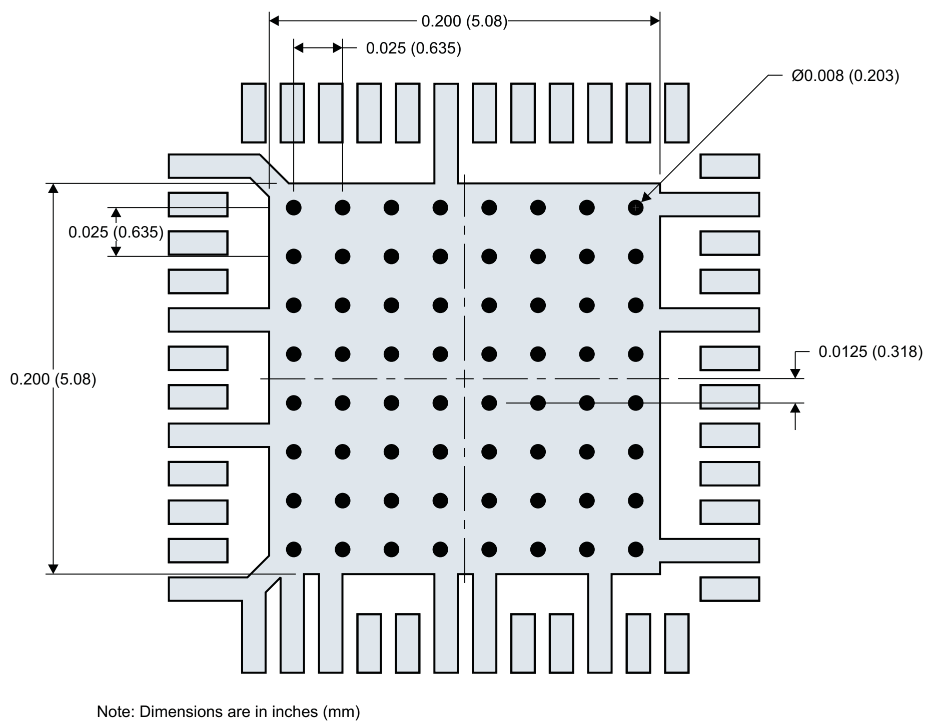


Figure 44. PCB Layout Guidelines

Application Schematic

Figure 45 shows the typical application schematic. The RF bypass capacitors and coupling capacitors on the supply pins should be adjusted to provide the best high-frequency bypass based on the frequency of operation.

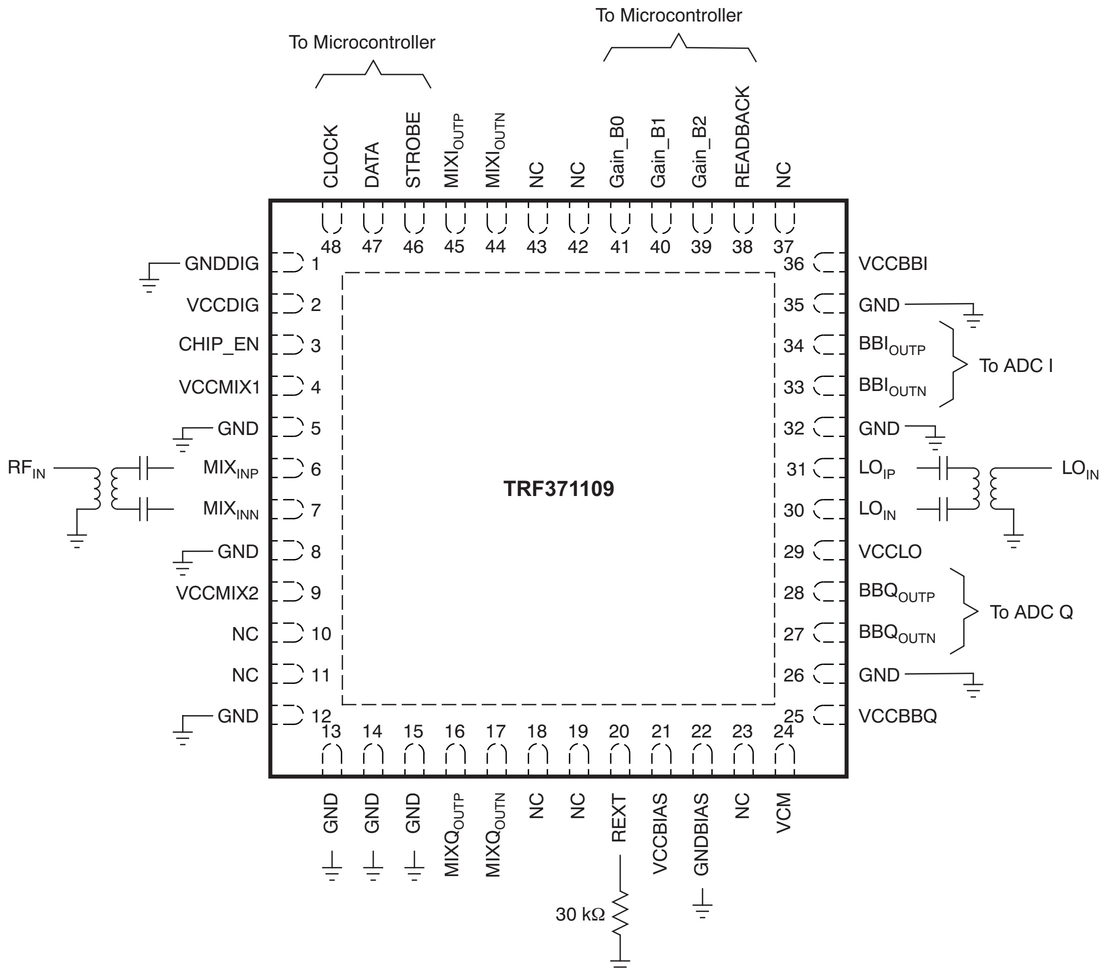


Figure 45. TRF371109 Application Schematic

The RF input port and the RF LO port require differential input paths. Single-ended RF inputs to these ports can be converted with an RF balun that is centered at the band of interest. Linearity performance of the TRF371109 depends on the amplitude and phase balance of the RF balun; therefore, care should be taken with the selection of the balun device and with the RF layout of the device. The recommended RF balun devices are listed in Table 10.

Table 10. RF Balun Devices

MANUFACTURER	PART NUMBER	FREQUENCY RANGE	UNBALANCE IMPEDANCE	BALANCE IMPEDANCE
Murata	LDB21897M005C-001	897 MHz ±100 MHz	50 Ω	50 Ω
Murata	LDB211G8005C-001	1800 MHz ±100 MHz	50 Ω	50 Ω
Murata	LDB211G9005C-001	1900 MHz ±100 MHz	50 Ω	50 Ω
Murata	LDB212G4005C-001	2.3 GHz to 2.7 GHz	50 Ω	50 Ω
Johanson	3600BL14M050E	3.3 GHz to 3.8 GHz	50 Ω	50 Ω

ADC Interface

The TRF3711 has an integrated ADC driver buffer that allows direct connection to an ADC without additional active circuitry. The common-mode voltage generated by the ADC can be directly supplied to the TRF3711 through the VCM pin (pin 24). Otherwise, a nominal common-mode voltage of 1.5 V should be applied to that pin. The TRF3711 device can operate with a common-mode voltage from 1.5 V to 2.8 V without any negative imact on the output performance. Figure 46 illustrates the degradation of the output compression point as the common-mode voltage exceeds those values.

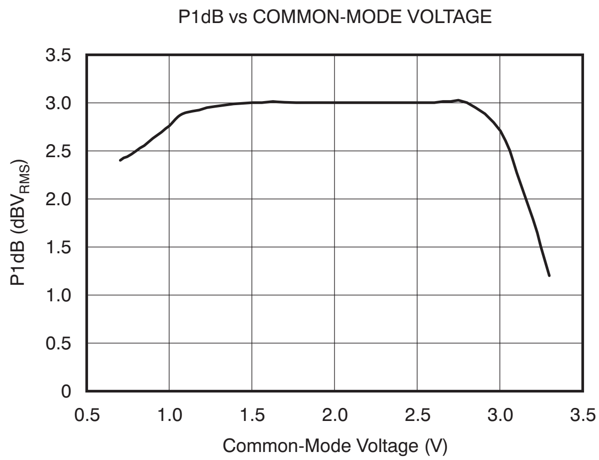


Figure 46. P1dB Performance vs. Common Mode Voltage

Application for a High-Performance RF Receiver Signal Chain

The TRF371109 is the centerpiece component of a high-performance, direct-downconversion receiver. This device is a highly-integrated, direct-downconversion demodulator that requires minimal additional devices to complete the signal chain. A signal chain block diagram example is shown in Figure 47.

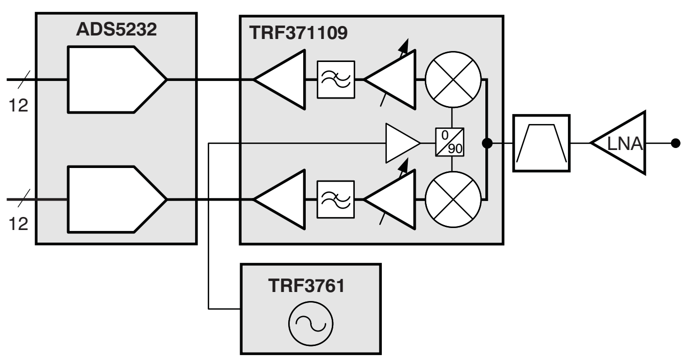


Figure 47. Block Diagram of Direct Downconvert Receiver

The lineup requires a low-noise amplifier (LNA) that operates at the frequency of interest with typical 1- to 2-dB noise figure (NF) performance. An RF bandpass filter (BPF) is selected at the frequency band of interest to prevent unwanted signals and images outside the band from reaching the demodulator. The TRF371109 incorporates the direct downconvert demodulation, baseband filtering, and baseband gain-control functions. An external synthesizer, such as the TRF3761, provides the LO source to the TRF371109. The differential outputs of the TRF3761 directly match with the LO input of the TRF371109. The quadrature outputs (I/Q) of the TRF371109 directly drive the input to the ADC. A dual ADC such as the ADS5232 12-bit, 65-MSPS ADC matches perfectly with the differential I/Q output of the TRF371109. In addition, the common-mode output voltage generated by the ADS5232 is fed directly into the common-mode ports (pin 24) to ensure that the optimum dynamic range of the ADC is maintained.

EVALUATION TOOLS

An evaluation module is available to test the TRF371109 performance. The TRF371109EVM can be configured with different baluns to enable operation in various frequency bands. The TRF371109EVM is available for purchase through the Texas Instruments web site at www.ti.com.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March, 2011) to Revision B	Page
• Updated *Automated DC Offset Calibration* section with correct information about the dc Offset Correction DACs	35

Changes from Original (December, 2010) to Revision A	Page
• Revised the *Register Information* section	28

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRF371109IRGZR	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	TRF 371109IRGZ	Samples
TRF371109IRGZT	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	TRF 371109IRGZ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

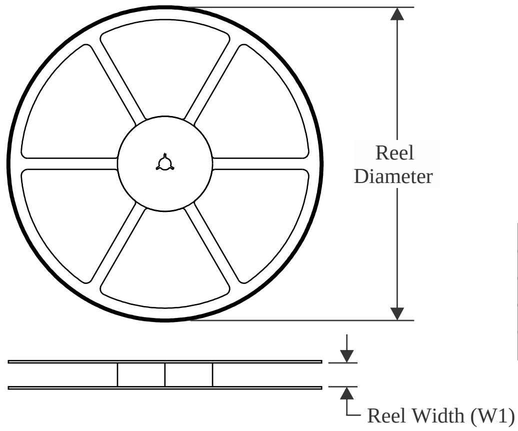
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

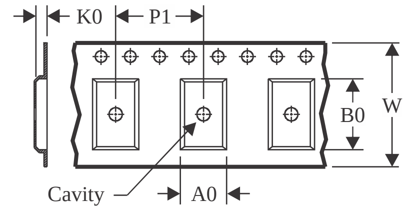
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

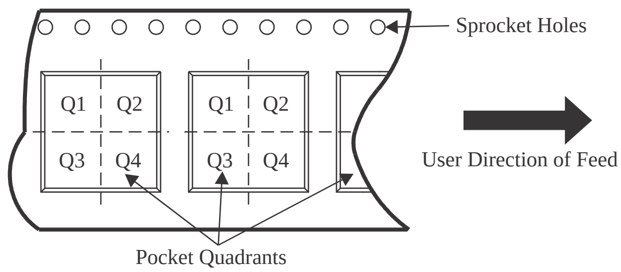


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

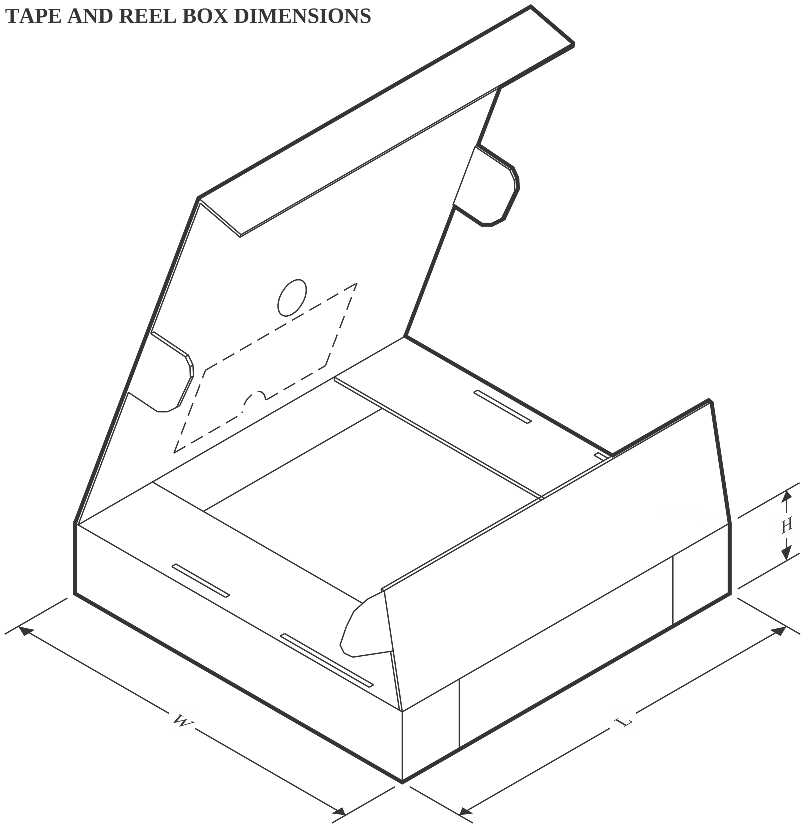
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRF371109IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

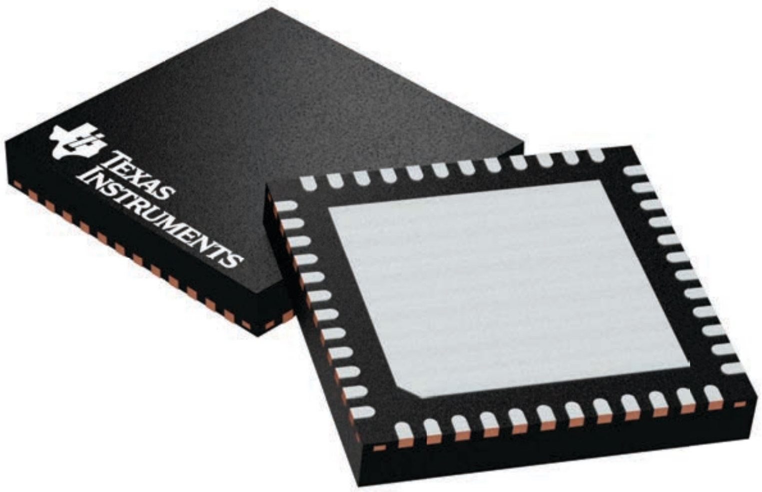
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRF371109IRGZR	VQFN	RGZ	48	2500	350.0	350.0	43.0

RGZ 48

VQFN - 1 mm max height

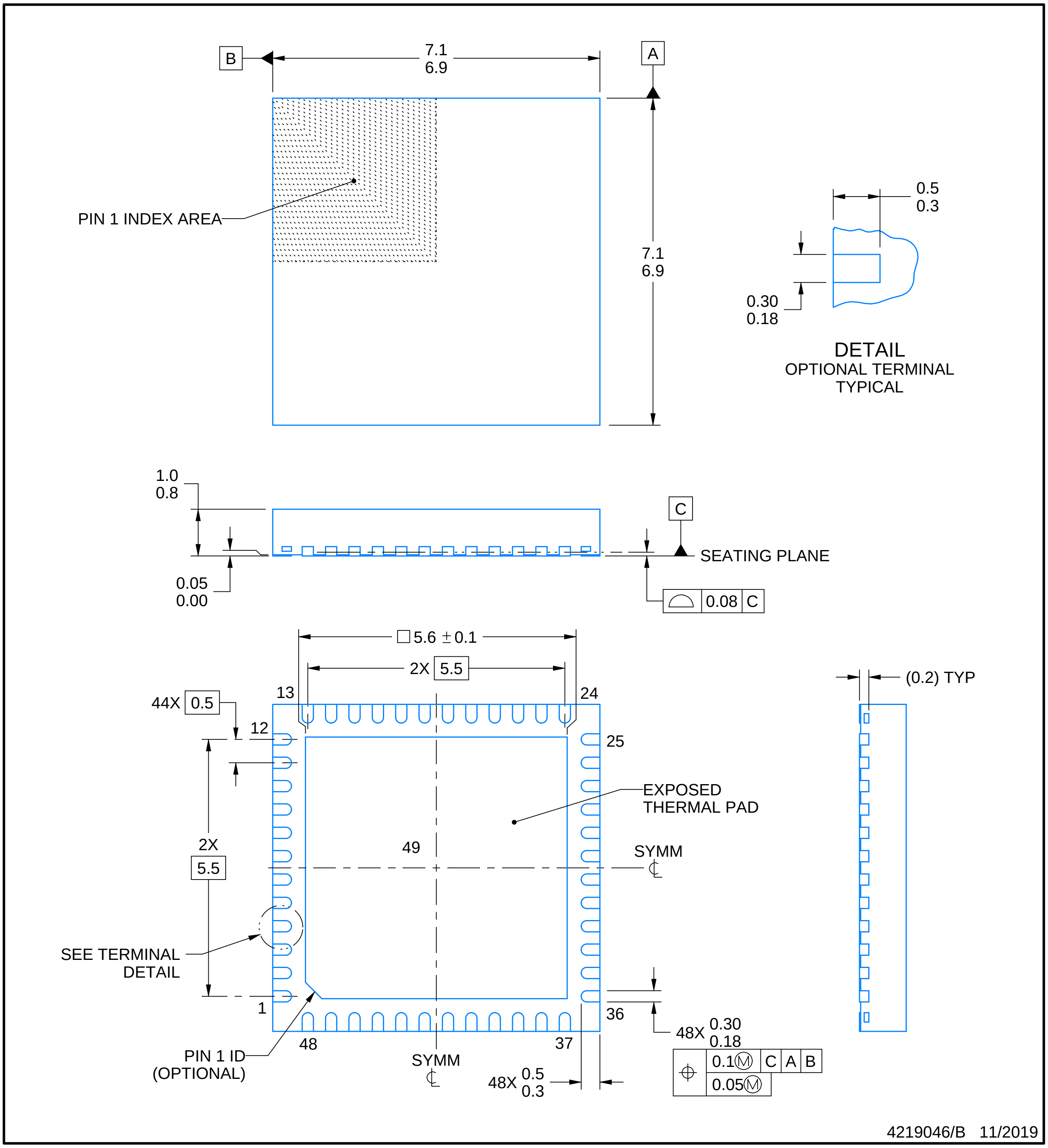
7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



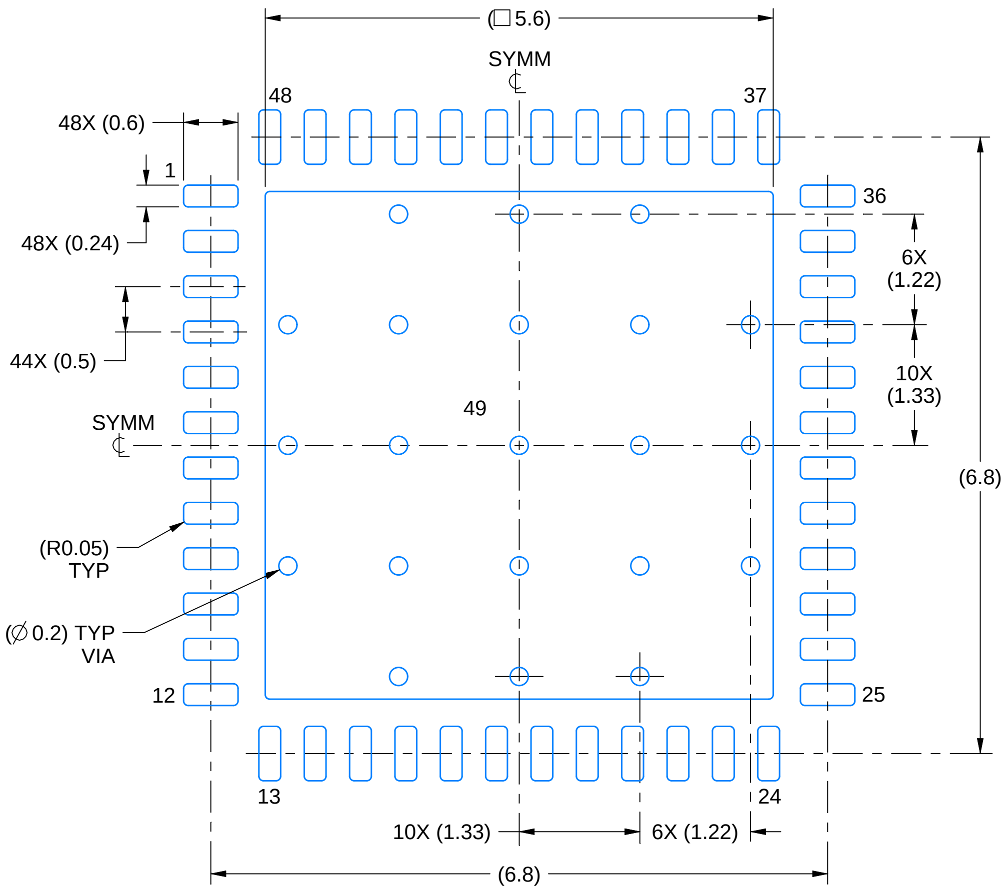
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224671/A

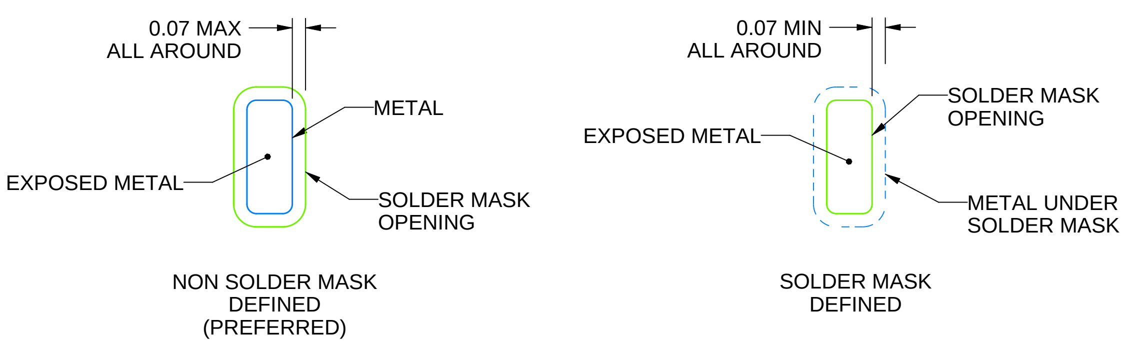


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

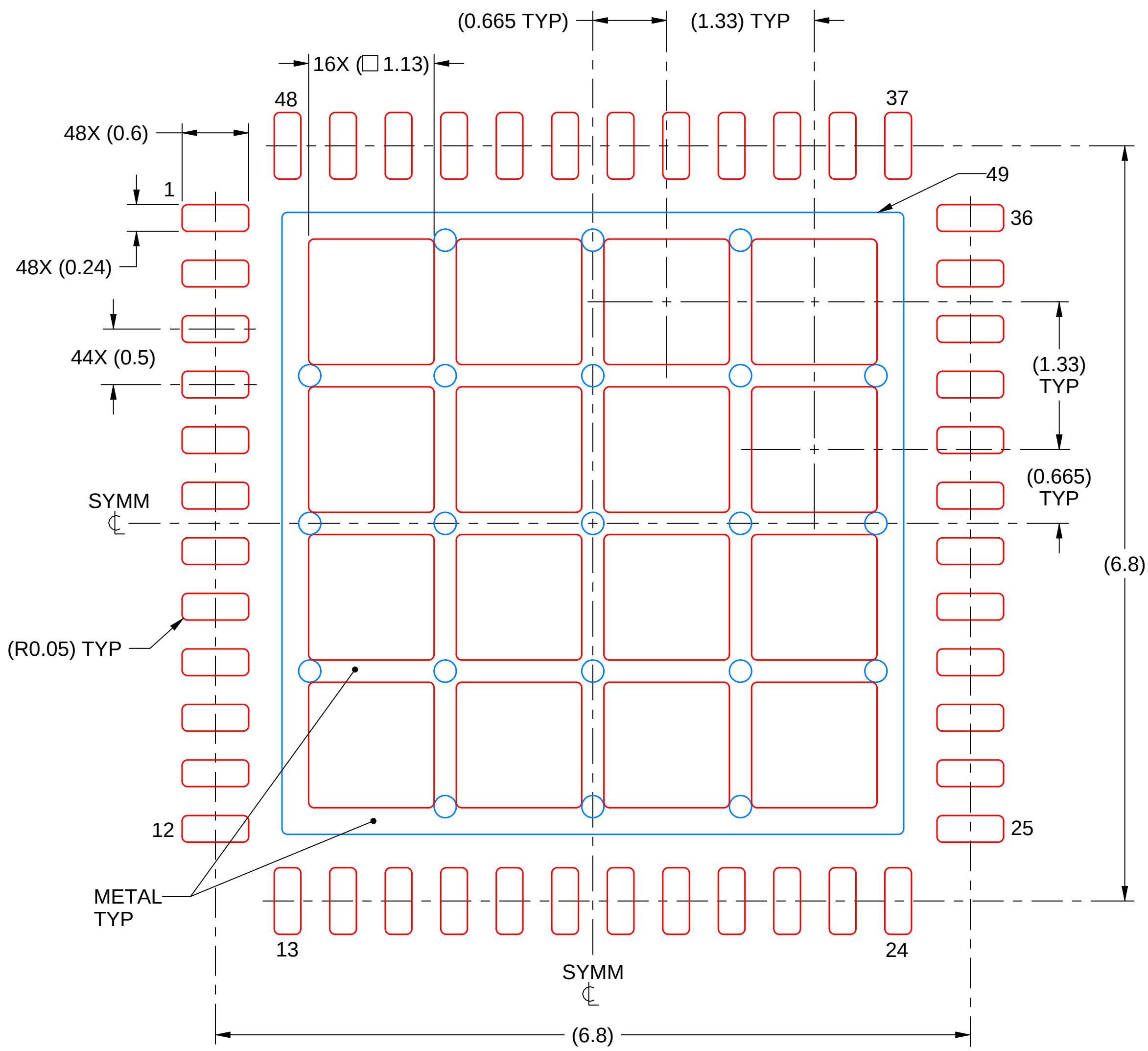


SOLDER MASK DETAILS

4219046/B 11/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
66% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

4219046/B 11/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.