

# TRS202E 5V デュアル RS-232 ラインドライバ/レシーバ、±15kV IEC ESD 保護機能搭載

## 1 特長

- RS-232 バスピンに対する IEC61000-4-2 (Level 4) ESD 保護機能:
  - ±8kV 接触放電
  - ±15kV 気中放電
  - ±15kV 人体モデル
- TIA/EIA-232-F および ITU v.28 規格の要件に適合またはそれを上回る性能
- 5V V<sub>CC</sub> 電源で動作
- 最大 120kbit/s で動作
- 外付けコンデンサ: 4 × 0.1μF または 4 × 1μF
- JESD 78, Class II 準拠で 100mA を超えるラッチアップ性能

## 2 アプリケーション

- バッテリー駆動システム
- ノート PC
- ノート PC
- セットトップ ボックス
- ハンドヘルド機器

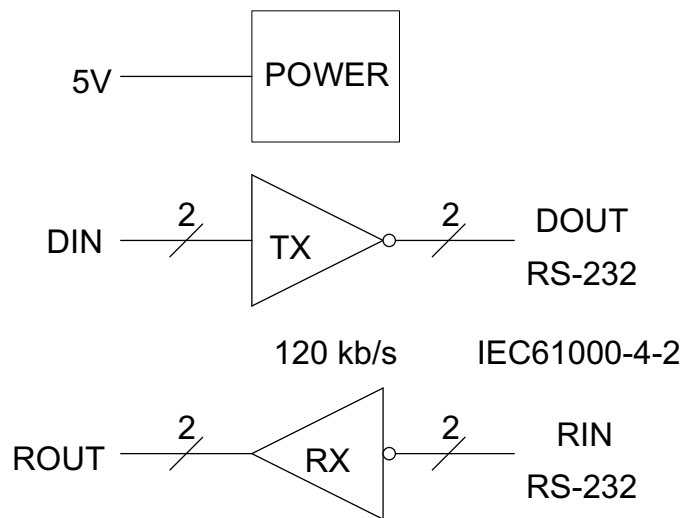
## 3 概要

TRS202E は、2 つのラインドライバ、2 つのラインレシーバ、1 つのデュアルチャージポンプ回路で構成されています。TRS202E は、ピン間 (シリアルポート接続ピン、GND を含む) で IEC61000-4-2 (レベル 4) の ESD 保護機能を備えています。このデバイスは、TIA/EIA-232-F の要件を満たし、非同期通信コントローラとシリアルポートコネクタの間の電気的インターフェイスとして機能します。チャージポンプと 4 つの小さな外付けコンデンサにより、5V の単一電源で動作できます。本デバイスは最大 120kbit/s のデータ信号速度、最大 30V/μs のドライバ出力スlewレートで動作します。

### パッケージ情報

部品番号	パッケージ (1)	パッケージサイズ (2)
TRS202E	SOIC (D) (16)	9.9mm × 6mm
	SOIC (DW) (16)	10.4mm × 10.3mm
	PDIP (N) (16)	19.3mm × 9.4mm
	TSSOP (PW) (16)	5mm × 6.4mm

- 詳細については、[セクション 10](#) を参照してください。
- パッケージサイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



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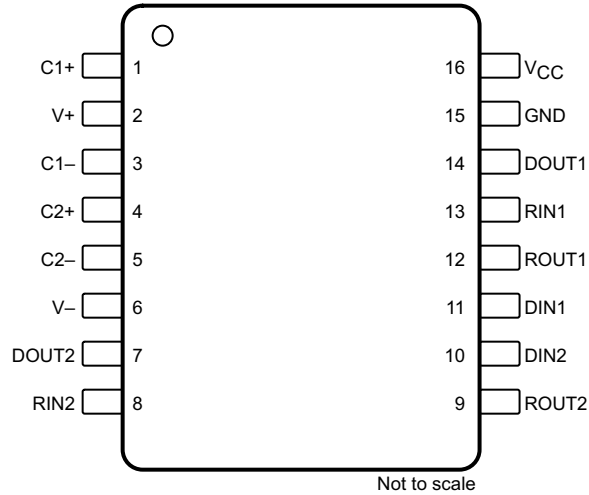
### 論理図 (正論理)



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## 4 Pin Configuration and Functions




**4-1. D, DW, N or PW Package, 16-Pin SOIC or TSSOP (Top View)**

**表 4-1. Pin Functions**

PIN		I/O	DESCRIPTION
NO.	NAME		
1	C1+	—	Positive lead of C1 capacitor
2	V+	O	Positive charge pump output for storage capacitor only
3	C1–	—	Negative lead of C1 capacitor
4	C2+	—	Positive lead of C2 capacitor
5	C2–	—	Negative lead of C2 capacitor
6	V–	O	Negative charge pump output for storage capacitor only
7	DOUT2	O	RS-232 line data output (to remote RS-232 system)
8	RIN2	I	RS-232 line data input (from remote RS-232 system)
9	ROUT2	O	Logic data output (to UART)
10	DIN2	I	Logic data input (from UART)
11	DIN1	I	Logic data input (from UART)
12	ROUT1	O	Logic data output (to UART)
13	RIN1	I	RS-232 line data input (from remote RS-232 system)
14	DOUT1	O	RS-232 line data output (to remote RS-232 system)
15	GND	—	Ground
16	V <sub>CC</sub>	—	Supply voltage, connect to external 5-V power supply

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup> <sup>(2)</sup>

		MIN	MAX	UNIT
Supply voltage, $V_{CC}$ <sup>(2)</sup>		-0.3	6	V
Positive charge pump voltage, $V+$ <sup>(2)</sup>		$V_{CC} - 0.3$	14	V
Negative charge pump voltage, $V-$		-14	0.3	V
Input voltage, $V_I$	Drivers	-0.3	$V+ + 0.3$	V
	Receivers		$\pm 30$	
Output voltage, $V_O$	Drivers	$V- - 0.3$	$V+ + 0.3$	V
	Receivers	-0.3	$V_{CC} + 0.3$	
Short-circuit duration, $D_{OUT}$		Continuous		
Operating virtual junction temperature, $T_J$			150	°C
Storage temperature, $T_{stg}$		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.

### 5.2 ESD Ratings

			VALUE	UNIT	
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	Pins 7, 8, 13, 14, 15	$\pm 15000$	V	
		All other pins	$\pm 2000$		
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>		All pins		$\pm 1500$
	IEC 61000-4-2 contact discharge		Pins 7, 8, 13, 14, 15		$\pm 8000$
	IEC 61000-4-2 air-gap discharge		Pins 7, 8, 13, 14, 15		$\pm 15000$

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

see [Figure 7-1](#) <sup>(1)</sup>

		MIN	NOM	MAX	UNIT
Supply voltage		4.5	5	5.5	V
$V_{IH}$	Driver high-level input voltage ( $D_{IN}$ )	2			V
$V_{IL}$	Driver low-level input voltage ( $D_{IN}$ )			0.8	V
$V_I$	Driver input voltage ( $D_{IN}$ )	0		5.5	V
	Receiver input voltage	-30		30	
$T_A$	Operating free-air temperature	TRS202EC		70	°C
		TRS202EI	-40	85	

- (1) Test conditions are  $C1$  to  $C4 = 0.1\mu F$  at  $V_{CC} = 5V \pm 0.5V$ .

## 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		D (SOIC)	DW (SOIC)	N (PDIP)	PW (TSSOP)	UNIT
		16 PINS	16 PINS	16 PINS	16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	84.6	77.1	44.1	107.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	43.5	39.9	30.8	38.4	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	43.2	41.8	24.2	53.7	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	10.4	12.9	15.2	3.2	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	42.8	41.3	24	53.1	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted; see [Figure 7-1](#))<sup>(1)</sup>

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
I <sub>CC</sub>	Supply current	No load, V <sub>CC</sub> = 5V			
			8	15	mA

(1) Test conditions are C1 to C4 = 0.1μF at V<sub>CC</sub> = 5V + 0.5V.

(2) All typical values are at V<sub>CC</sub> = 5V and T<sub>A</sub> = 25°C.

## 5.6 Electrical Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 7-1](#))<sup>(1)</sup>

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	D <sub>OUT</sub> at R <sub>L</sub> = 3kΩ to GND, D <sub>IN</sub> = GND			V
V <sub>OL</sub>	Low-level output voltage	D <sub>OUT</sub> at R <sub>L</sub> = 3kΩ to GND, D <sub>IN</sub> = V <sub>CC</sub>			V
I <sub>IH</sub>	High-level input current	V <sub>I</sub> = V <sub>CC</sub>			μA
I <sub>IL</sub>	Low-level input current	V <sub>I</sub> at 0V			μA
I <sub>OS</sub> <sup>(3)</sup>	Short-circuit output current	V <sub>CC</sub> = 5.5V and V <sub>O</sub> = 0V			mA
r <sub>o</sub>	Output resistance	V <sub>CC</sub> , V <sub>+</sub> , V <sub>-</sub> = 0V, and V <sub>O</sub> = ±2V			Ω

(1) Test conditions are C1 to C4 = 0.1μF at V<sub>CC</sub> = 5V + 0.5V.

(2) All typical values are at V<sub>CC</sub> = 5V and T<sub>A</sub> = 25°C.

(3) Short-circuit durations must be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output must be shorted at a time.

## 5.7 Electrical Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted; see [Figure 7-1](#))<sup>(1)</sup>

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -1mA			V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 1.6mA			V
V <sub>IT+</sub>	Positive-going input threshold voltage	V <sub>CC</sub> = 5V and T <sub>A</sub> = 25°C			V
V <sub>IT-</sub>	Negative-going input threshold voltage	V <sub>CC</sub> = 5V and T <sub>A</sub> = 25°C			V
V <sub>hys</sub>	Input hysteresis (V <sub>IT+</sub> - V <sub>IT-</sub> )				V
r <sub>i</sub>	Input resistance	V <sub>I</sub> = ±3V to ±25V			kΩ

(1) Test conditions are C1 to C4 = 0.1μF at V<sub>CC</sub> = 5V + 0.5V.

(2) All typical values are at V<sub>CC</sub> = 5V and T<sub>A</sub> = 25°C.

## 5.8 Switching Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted; see [7-1](#))<sup>(1)</sup>

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
	Maximum data rate	$C_L = 50$ to $1000\text{pF}$ , one $D_{OUT}$ switching, and $R_L = 3\text{k}\Omega$ to $7\text{k}\Omega$ (see <a href="#">6-1</a> )	120			kbit/s
$t_{PLH(D)}$	Propagation delay time, low- to high-level output	$C_L = 2500\text{pF}$ , all drivers loaded, and $R_L = 3\text{k}\Omega$ (see <a href="#">6-1</a> )		2		$\mu\text{s}$
$t_{PHL(D)}$	Propagation delay time, high- to low-level output	$C_L = 2500\text{pF}$ , all drivers loaded, and $R_L = 3\text{k}\Omega$ (see <a href="#">6-1</a> )		2		$\mu\text{s}$
$t_{sk(p)}$	Pulse skew <sup>(3)</sup>	$C_L = 150$ to $2500\text{pF}$ and $R_L = 3\text{k}\Omega$ to $7\text{k}\Omega$ (see <a href="#">6-2</a> )		300		ns
SR(tr)	Slew rate, transition region	$C_L = 50$ to $1000\text{pF}$ , $V_{CC} = 5\text{V}$ , and $R_L = 3\text{k}\Omega$ to $7\text{k}\Omega$ (see <a href="#">6-1</a> )	3	6	30	$\text{V}/\mu\text{s}$

(1) Test conditions are  $C_1$  to  $C_4 = 0.1\mu\text{F}$  at  $V_{CC} = 5\text{V} + 0.5\text{V}$ .

(2) All typical values are at  $V_{CC} = 5\text{V}$  and  $T_A = 25^\circ\text{C}$ .

(3) Pulse skew is defined as  $|t_{PLH} - t_{PHL}|$  of each channel of the same device.

## 5.9 Switching Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted; see [6-3](#))<sup>(1)</sup>

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
$t_{PLH(R)}$	Propagation delay time, low- to high-level output	$C_L = 150\text{pF}$		0.5	10	$\mu\text{s}$
$t_{PHL(R)}$	Propagation delay time, high- to low-level output	$C_L = 150\text{pF}$		0.5	10	$\mu\text{s}$
$t_{sk(p)}$	Pulse skew <sup>(3)</sup>			300		ns

(1) Test conditions are  $C_1$  to  $C_4 = 0.1\mu\text{F}$  at  $V_{CC} = 5\text{V} + 0.5\text{V}$ .

(2) All typical values are at  $V_{CC} = 5\text{V}$  and  $T_A = 25^\circ\text{C}$ .

(3) Pulse skew is defined as  $|t_{PLH} - t_{PHL}|$  of each channel of the same device.

## 5.10 Typical Characteristics

$T_A = 25^\circ\text{C}$  (unless otherwise noted)

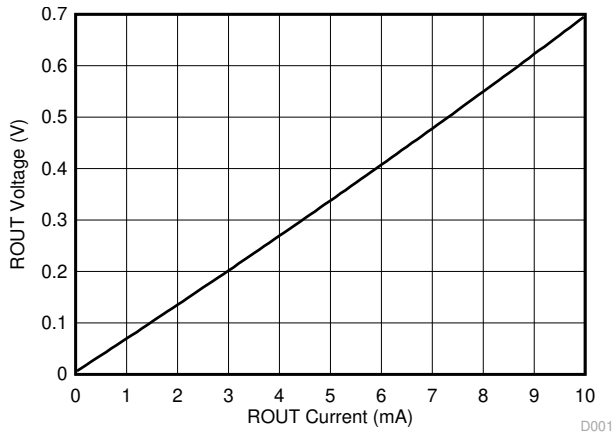


图 5-1. Receiver  $V_{OL}$  vs Output Current

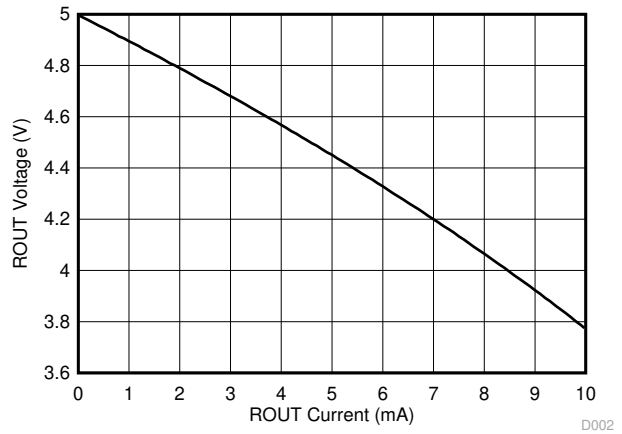


图 5-2. Receiver  $V_{OH}$  vs Output Current

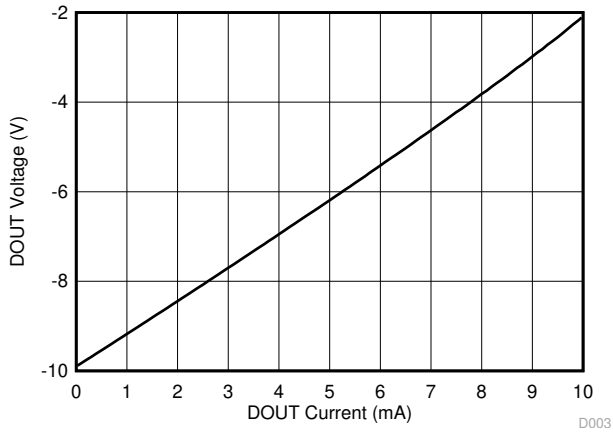


图 5-3. Driver  $V_{OL}$  vs Output Current

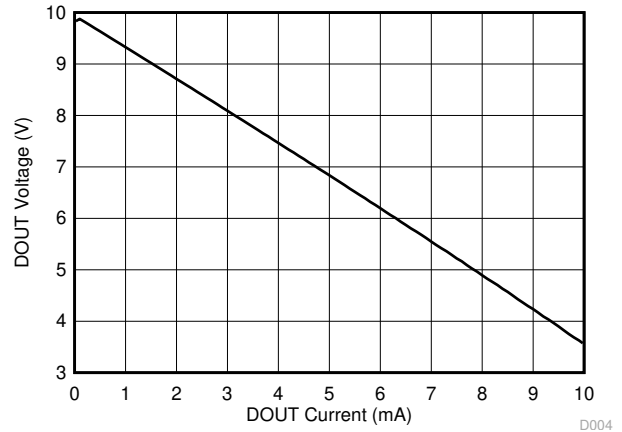


图 5-4. Driver  $V_{OH}$  vs Output Current

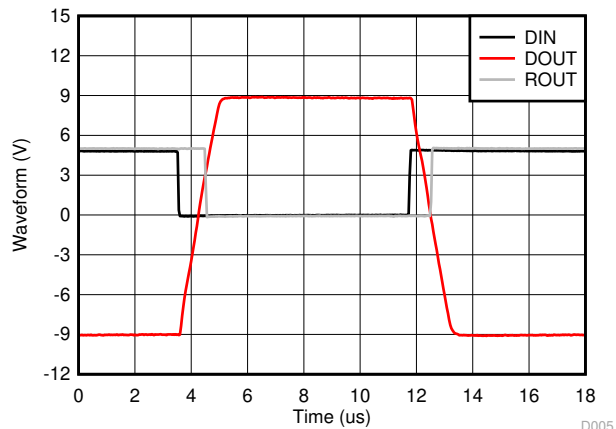
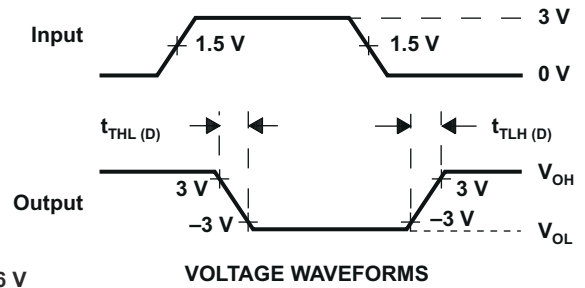
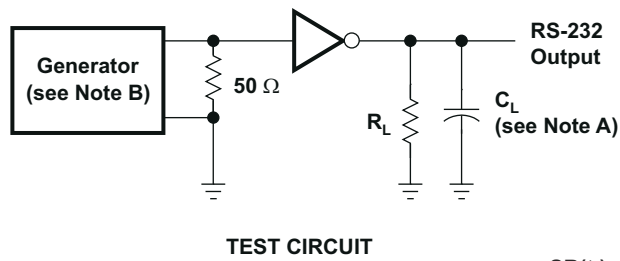


图 5-5. Driver and Receiver Loopback Waveforms

## Parameter Measurement Information

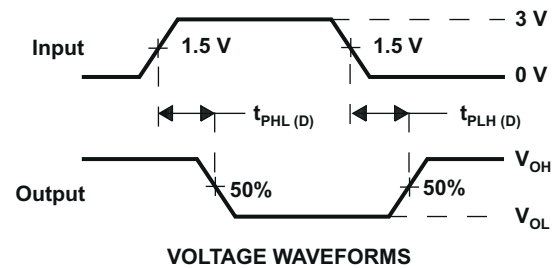
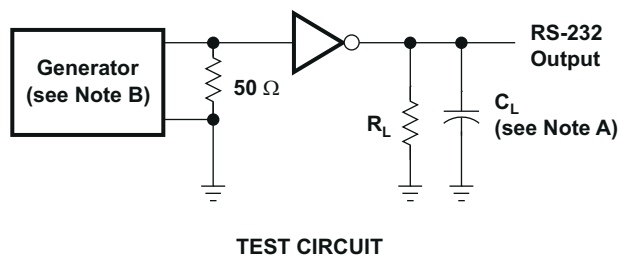


$$SR(t_f) = \frac{6 \text{ V}}{t_{\text{THL(D)}} \text{ or } t_{\text{TLH(D)}}$$

NOTES: A.  $C_L$  includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 120 kbit/s,  $Z_0 = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ .

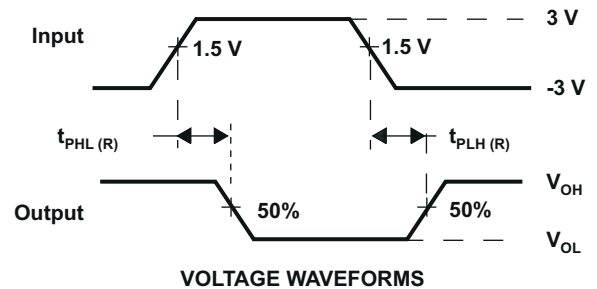
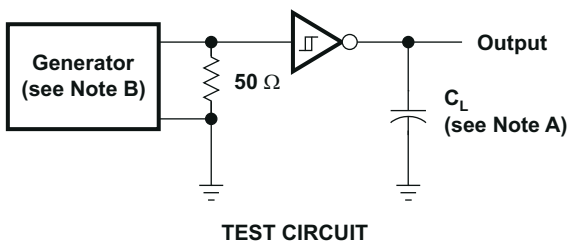
### 6-1. Driver Slew Rate



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 120 kbit/s,  $Z_0 = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ .

### 6-2. Driver Pulse Skew



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. The pulse generator has the following characteristics:  $Z_0 = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ .

### 6-3. Receiver Propagation Delay Times

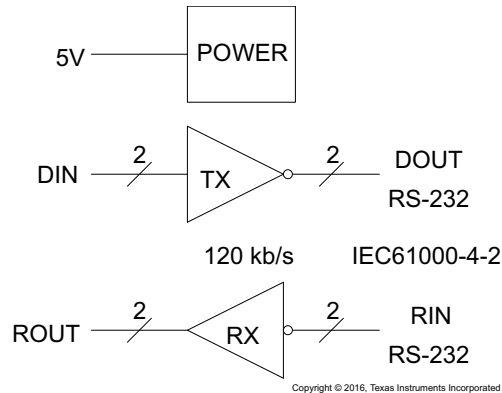


## 6 Detailed Description

### 6.1 Overview

The TRS202E device is a dual driver and receiver that includes a capacitive voltage generator using four capacitors to supply TIA/EIA-232-F voltage levels from a single 5V supply. All RS-232 pins have 15kV HBM and IEC61000-4-2 Air-Gap discharge protection. RS-232 pins also have 8-kV IEC61000-4-2 contact discharge protection. Each receiver converts TIA/EIA-232-F inputs to 5V TTL/CMOS levels. These receivers have shorted and open fail safe. The receiver can accept up to  $\pm 30\text{V}$  inputs and decode inputs as low as  $\pm 3\text{V}$ . Each driver converts TTL/CMOS input levels into TIA/EIA-232-F levels. Outputs are protected against shorts to ground.

### 6.2 Functional Block Diagram



### 6.3 Feature Description

#### 6.3.1 Power

The power block increases and inverts the 5V supply for the RS-232 driver using a charge pump that requires four  $0.1\mu\text{F}$  or  $1\mu\text{F}$  external capacitors.

#### 6.3.2 RS-232 Driver

Two drivers interface standard logic levels to RS-232 levels. The driver inputs do not have internal pullup resistors. Do not float the driver inputs.

#### 6.3.3 RS-232 Receiver

Two Schmitt trigger receivers interface RS-232 levels to standard logic levels. Each receiver has an internal  $5\text{-k}\Omega$  load to ground. An open input results in a high output on  $R_{OUT}$ .

### 6.4 Device Functional Modes

#### 6.4.1 $V_{CC}$ Powered by 5V

The device is in normal operation when powered by 5V.

#### 6.4.2 $V_{CC}$ Unpowered

When TRS202E is unpowered, it can be safely connected to an active remote RS-232 device.

### 6.4.3 Truth Tables

表 6-1 and 表 6-2 list the function for each driver and receiver (respectively).

**表 6-1. Function Table for Each Driver**

INPUT DIN <sup>(1)</sup>	OUTPUT DOUT
L	H
H	L

(1) H = high level, L = low level

**表 6-2. Function Table for Each Receiver**

INPUT RIN <sup>(1)</sup>	OUTPUT ROUT
L	H
H	L
Open	H

(1) H = high level, L = low level,  
Open = input disconnected or connected driver off

## 7 Application and Implementation

### 注

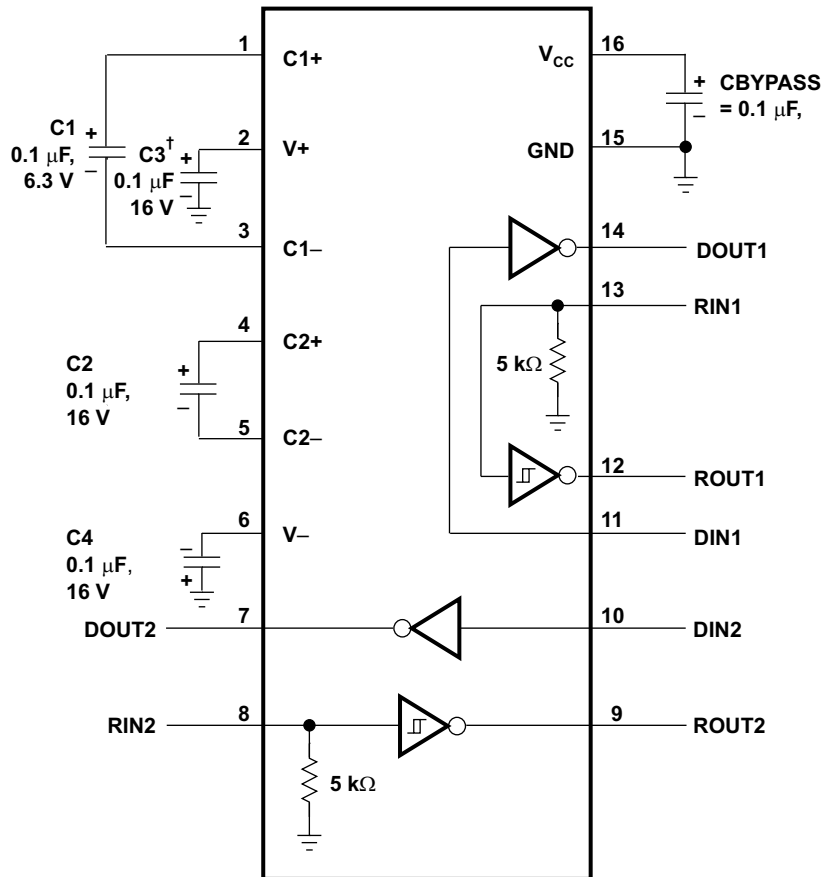
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### 7.1 Application Information

For proper operation, add capacitors as shown in 図 7-1. Pins 9 through 12 connect to UART or general purpose logic lines. RS-232 lines on pins 7, 8, 13, and 14 connect to a connector or cable.

### 7.2 Typical Application

Two driver and two receiver channels are supported for full duplex transmission with hardware flow control. The two 5kΩ-resistors are internal to the TRS202E.



† C3 can be connected to  $V_{CC}$  or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

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図 7-1. Typical Operating Circuit and Capacitor Values

### 7.2.1 Design Requirements

- $V_{CC}$  minimum is 4.5V and maximum is 5.5V.
- Maximum recommended bit rate is 120kbps.

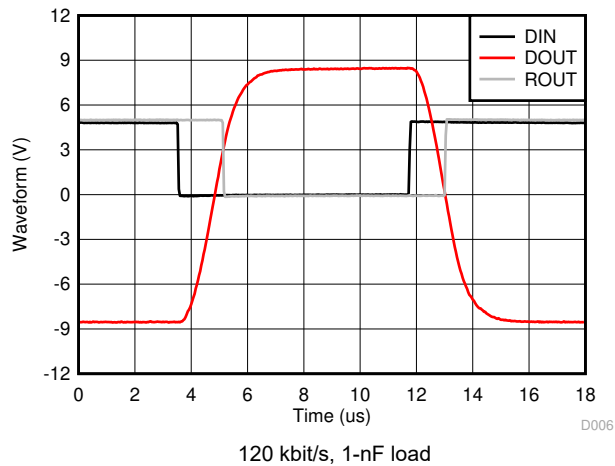
### 7.2.2 Detailed Design Procedure

#### 7.2.2.1 Capacitor Selection

The capacitor type used for C1 through C4 is not critical for proper operation. The TRIS202E requires 0.1 $\mu$ F capacitors. 1- $\mu$ F capacitors are also acceptable. TI recommends ceramic dielectrics. When using the minimum recommended capacitor values, ensure the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (for example, 2 $\times$ ) nominal value. The capacitors' effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V-.

Bypass  $V_{CC}$  to ground with at least 0.1 $\mu$ F. In applications sensitive to power-supply noise generated by the charge pumps, decouple  $V_{CC}$  to ground with a capacitor the same size as (or larger than) the charge-pump capacitors (C1 to C4).

### 7.2.3 Application Curves



**7-2. Driver and Receiver Loopback Signal**

### 7.3 Power Supply Recommendations

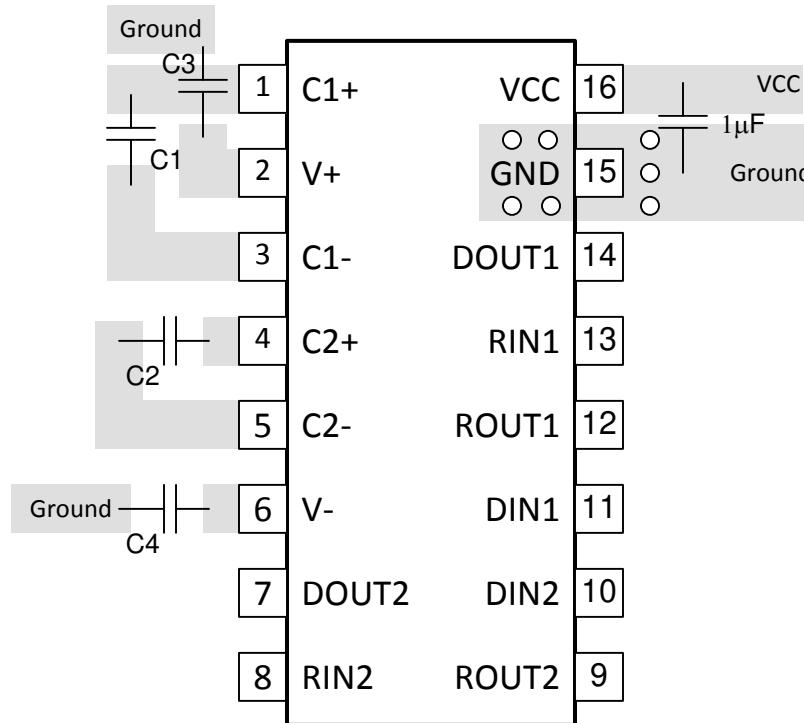
The  $V_{CC}$  voltage must be connected to the same power source used for logic device connected to DIN and ROUT pins.  $V_{CC}$  must be between 4.5V and 5.5V.

## 7.4 Layout

### 7.4.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes that have the fastest rise and fall times. Make the impedance from TRS202E ground pin and circuit boards ground plane as low as possible for best ESD performance. Use wide metal and multiple vias on both sides of ground pin.

### 7.4.2 Layout Example



☒ 7-3. TRS202E Layout

## 8 Device and Documentation Support

### 8.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com) のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 8.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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### 8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

### 8.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 8.5 用語集

TI 用語集 この用語集には、用語や略語の一覧および定義が記載されています。

## 9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

### Changes from Revision E (November 2016) to Revision F (February 2024) Page

- 「パッケージ情報」表を変更..... 1
- Changed the *Thermal Information* table..... 5

### Changes from Revision D (November 2012) to Revision E (November 2016) Page

- 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加。..... 1
- 「注文情報」表を削除 (このデータシートの末尾にある「パッケージ オプションについての付録」を参照) ..... 1
- Changed Package thermal impedance,  $R_{\theta JA}$ , values in Thermal Information table From: 73°C/W To: 76.7°C/W (D), From: 57°C/W To: 77.1°C/W (DW), From: 67°C/W To: 44.1°C/W (N), and From: 108°C/W To: 101.7°C/W (PW)..... 5

### Changes from Revision C (May 2010) to Revision D (November 2012) Page

- Fixed  $I_{OS}$  values in *Electrical Characteristics* table, changed – to  $\pm$ ..... 5

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRS202ECD	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70	TRS202EC	
TRS202ECDR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70	TRS202EC	
TRS202ECDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS202EC	Samples
TRS202ECN	ACTIVE	PDIP	N	16	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	TRS202ECN	Samples
TRS202ECPWR	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	0 to 70	RU02EC	
TRS202EID	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85	TRS202EI	
TRS202EIDR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS202EI	Samples
TRS202EIDW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS202EI	Samples
TRS202EIDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS202EI	Samples
TRS202EIN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TRS202EIN	Samples
TRS202EIPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RU02EI	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.



<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS202ECDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TRS202EIDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TRS202EIDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TRS202EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRS202EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS202ECDWR	SOIC	DW	16	2000	350.0	350.0	43.0
TRS202EIDR	SOIC	D	16	2500	340.5	336.1	32.0
TRS202EIDWR	SOIC	DW	16	2000	350.0	350.0	43.0
TRS202EIPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
TRS202EIPWR	TSSOP	PW	16	2000	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TRS202ECN	N	PDIP	16	25	506	13.97	11230	4.32
TRS202EIDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
TRS202EIN	N	PDIP	16	25	506	13.97	11230	4.32

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



## GENERIC PACKAGE VIEW

**DW 16**

**SOIC - 2.65 mm max height**

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



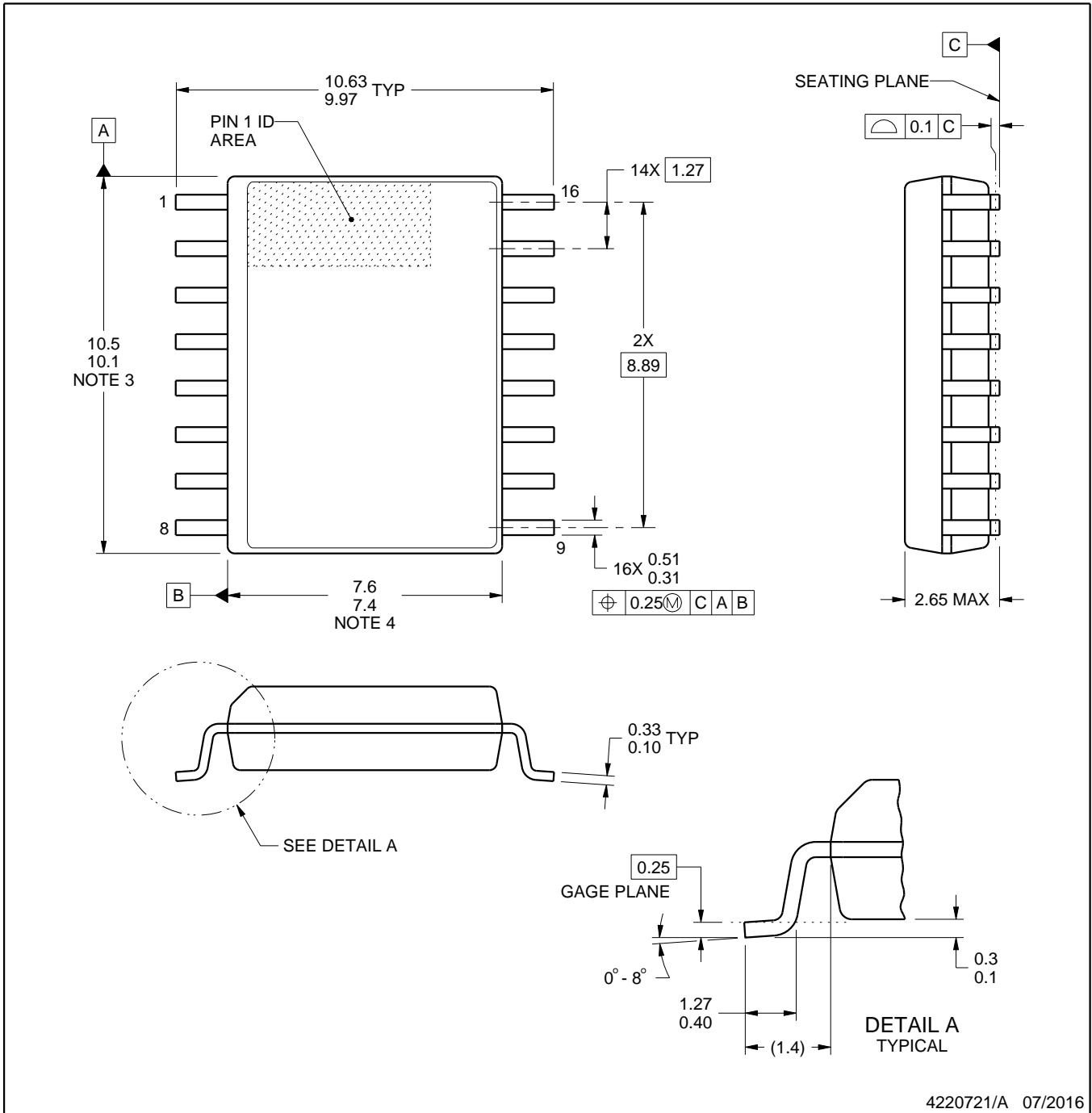
4224780/A



# DW0016A

# PACKAGE OUTLINE SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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