TRSF3221E ±15kV IEC ESD 保護機能搭載、小型パッケージの 3V～5.5V シングル チャネル RS-232 1Mbit ライン ドライバ / レシーバ

1 特長

- RS-232 ピンの ESD 保護
  - ±15kV 人体モデル (HBM)
  - ±8kV IEC 61000-4-2 接触放電
  - ±15kV IEC 61000-4-2 エアギャップ放電
- 3V～5.5V の V_{CC} 電源で動作
- 最大 1Mbit/s で動作
  - 低速のピン互換デバイス (250kbit/s) – TRS3221E
- ニア チップスケール パッケージ、16 ピン VQFN (RGT、TSSOP パッケージより 82% 小型) で供給
- 小さいスタンバイ電流:1µA (標準値)
- 外付けコンデンサ:4 × 0.1µF
- 3.3V 電源で 5V ロジック入力を許容
- 自動パワー ダウン機能により、ドライバを自動的にディセーブルすることで電力を節約

2 アプリケーション

- 産業用 PC
- 有線ネットワーク
- データ・センターおよびエンタープライズ・コンピューティング
- バッテリ駆動システム
- PDA
- ノートブック PC
- ノート PC
- パームトップ PC
- ハンドヘルド機器

3 概要

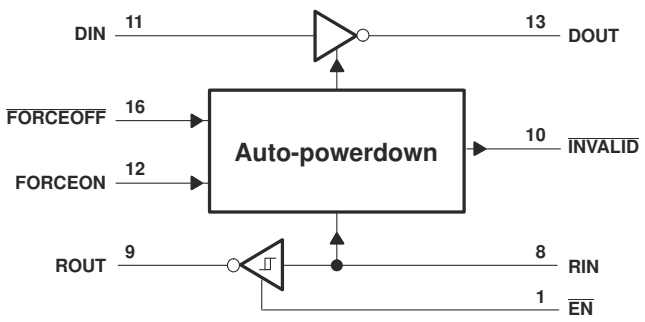
TRSF3221E デバイスは 1 つのライン ドライバ、1 つのライン レシーバ、1 つのデュアル チャージ ポンプ回路で構成されており、±15kV のピン間 (シリアル ポート接続ピン、GND を含む) IEC ESD 保護機能を備えています。TRSF3221E は、非同期通信コントローラとシリアルポート コネクタの間の電気的インターフェイスとして機能します。チャージ ポンプと 4 つの小さな外付けコンデンサにより、3V～5.5V の単一電源で動作できます。TRSF3221E は最大 1Mbit/s のデータ信号速度、24V/µs～150V/µs のドライバ出力スルーレートで動作します。

シリアル ポートが使われていない際のパワー マネージメントを柔軟に制御できます。FORCEON が LOW かつ $\overline{\text{FORCEOFF}}$ が HIGH の場合、自動パワー ダウン機能が動作します。この動作モード中、TRSF3221E がレシーバ入力で有効な RS-232 信号を検出しない場合、ドライバ出力はディスエーブルになります。$\overline{\text{FORCEOFF}}$ を Low に設定しかつイネーブル ($\overline{\text{EN}}$) 入力を High に設定すると、ドライバとレシーバはどちらもシャットダウンされ、消費電流は 1µA に減少します。シリアル ポートを切り離した場合、またはペリフェラル ドライバをオフにした場合、自動パワー ダウン状態になります。FORCEON と $\overline{\text{FORCEOFF}}$ を HIGH にすると、自動パワー ダウンを無効にできます。自動パワー ダウンが有効な場合、レシーバの入力に有効な信号が印加されると、デバイスは自動的にアクティブになります。$\overline{\text{INVALID}}$ 出力は、レシーバの入力に RS-232 信号が存在するかどうかをユーザーに通知します。$\overline{\text{INVALID}}$ は、レシーバの入力電圧が 2.7V を上回っている、または −2.7V を下回っている、あるいは −0.3V と 0.3V の間にあった期間が 30µs 未満である場合、HIGH (有効データ) になります。$\overline{\text{INVALID}}$ は、レシーバの入力電圧が 30µs を超えて -0.3V と 0.3V の間にある場合、Low (無効データ) になります。
レシーバの入力レベルについては、図 6-5 を参照してください。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TRSF3221E	DB (SSOP)	6.2 mm × 5.3mm
	PW (TSSOP)	5 mm × 4.4mm
	RGT (VQFN)	3 mm × 3mm
	SOT-23-THN (DYY) (16)	4.2mm × 2mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



論理図 (正論理)

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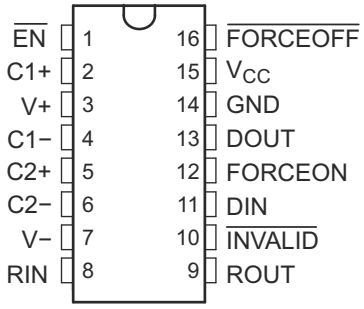
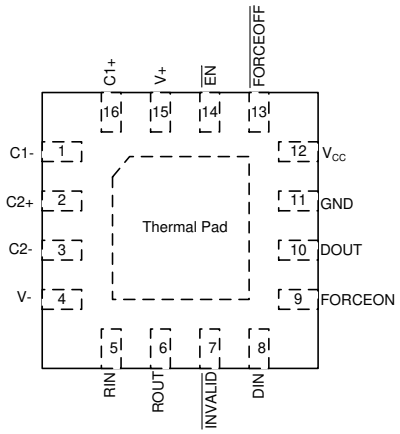
4 Pin Configuration and Functions



DB or PW Package. 16 Pins (Top View)



RGT, VSON Package, 16 Pins (Top View)

表 4-1. Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	DB or PW	RGT		
$\overline{EN}$	1	14	--	Low input enables receiver ROUT output. High input sets ROUT to high impedance.
C1+	2	16	-	Positive lead of C1 capacitor
V+	3	15	O	Positive charge pump output for storage capacitor only
C1-	4	1	-	Negative lead of C1 capacitor
C2+	5	2	-	Positive lead of C2 capacitor
C2-	6	3	-	Negative lead of C2 capacitor
V-	7	4	O	Negative charge pump output for storage capacitor only
RIN	8	5	I	RS232 line data input (from remote RS232 system)
ROUT	9	6	O	Logic data output (to UART)
$\overline{INVALID}$	10	7		Invalid output pin. Output low when RIN input is unpowered.
DIN	11	8	I	Logic data input (from UART)
FORCEON	12	9		Automatic power-down control input
DOUT	13	10	O	RS232 line data output (to remote RS232 system)
GRD	14	11	-	Ground
V_{CC}	15	12	-	Supply Voltage, Connect to external 3V to 5.5V power supply
$\overline{FORCEOFF}$	16	13		Automatic power-down control input
Thermal Pad	-	Yes	-	Exposed thermal pad. Can be connected to GND or left floating.

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

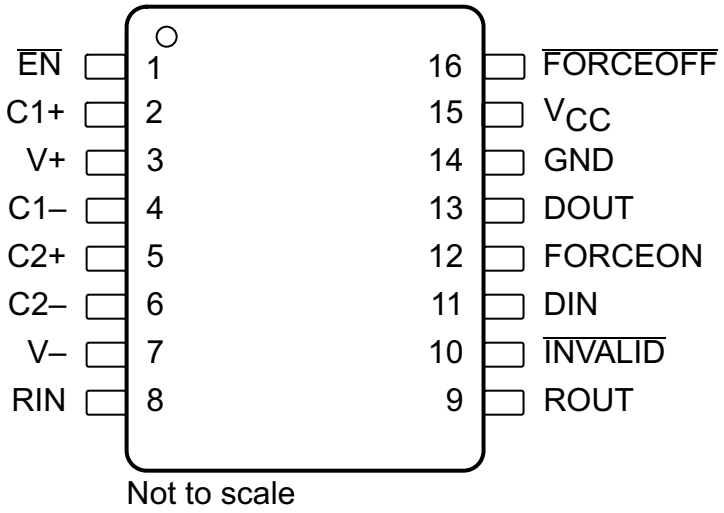


図 4-1. DYY Package
16-Pin SOT-23-THN
(Top View)

表 4-2. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
$\overline{EN}$	1	I	Low input enables receiver ROUT output. High input sets ROUT to high impedance.
C1+	2	—	Positive terminals of the voltage-doubler charge pump capacitors
V+	3	O	5.5V supply generated by the charge pump
C1–	4	—	Negative terminals of the voltage-doubler charge pump capacitors
C2+	5		Positive terminals of the voltage-doubler charge pump capacitors
C2–	6		Negative terminals of the voltage-doubler charge pump capacitors
V–	7	O	–5.5V supply generated by the charge pump
RIN	8	I	RS-232 receiver input
ROUT	9	O	Receiver output
$\overline{INVALID}$	10	O	Invalid output pin. Output low when RIN input is unpowered.
DIN	11	I	Driver input
FORCEON	12	I	Automatic power-down control input
DOUT	13	O	RS-232 driver output
GND	14	—	Ground
V_{CC}	15	—	3V to 5.5V supply voltage
$\overline{FORCEOFF}$	16	I	Automatic power-down control input

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)See (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range(2)		–0.3	6	V
V+	Positive output supply voltage range(2)		–0.3	7	V
V–	Negative output supply voltage range(2)		0.3	–7	V
V+ – V–	Supply voltage difference(2)			13	V
V_I	Input voltage range	Driver ($\overline{FORCEOFF}$, FORCEON, $\overline{EN}$)	–0.3	6	V
		Receiver	–25	25	
V_O	Output voltage range	Driver	–13.2	13.2	V
		Receiver ($\overline{INVALID}$)	–0.3	V_{CC} + 0.3	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings, IEC Specifications

PIN NAME	TEST CONDITIONS	VALUE	UNIT
RIN, DOUT(2)	HBM	±15,000	V
	IEC 61000-4-2 Contact Discharge(1) (2)	±8,000	
	IEC 61000-4-2 Air-Gap Discharge(1) (2)	±15,000	

(1) For the RGT and PW package only, a minimum of 1µF capacitor is required between VCC and GND to meet the specified IEC-ESD level.
(2) For optimized IEC ESD performance for DYY package, the recommendation is to have series resistor (≥ 50Ω), on all logic inputs directly connected to power or ground, to minimize the transient currents going into or out of the logic pins.

5.4 Recommended Operating Conditions

See 図 8-1 and (1)

				MIN	NOM	MAX	UNIT
	Supply voltage		V_{CC} = 3.3 V	3	3.3	3.6	V
			V_{CC} = 5 V	4.5	5	5.5	
V_{IH}	Driver and control high-level input voltage	DIN, $\overline{FORCEOFF}$, FORCEON, $\overline{EN}$	V_{CC} = 3.3 V	2			V
			V_{CC} = 5 V	2.4			
V_{IL}	Driver and control low-level input voltage	DIN, $\overline{FORCEOFF}$, FORCEON, $\overline{EN}$				0.8	V
V_I	Driver and control input voltage	DIN, $\overline{FORCEOFF}$, FORCEON		0		5.5	V
V_I	Receiver input voltage			–25		25	V
T_A	Operating free-air temperature		TRSF3221EI	–40		85	°C
			TRSF3221EC	0		70	

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

5.5 Thermal Resistance Characteristics

THERMAL METRIC(1)		TRSF3221E				UNIT
		DB (SSOP)	PW (TSSOP)	RGT (VQFN)	DYY (SOT-23-THN)	
		16 Pins	16 Pins	16 Pins	16 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	82	110.9	58.8	119.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.7	41.7	55.8	56.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.4	57.2	23.8	51.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	11.0	4.2	1.7	2.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	43.8	56.6	23.7	51.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	9	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.6 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 図 8-1)

PARAMETER			TEST CONDITIONS(1)	MIN	TYP(2)	MAX	UNIT
I_I	Input leakage current	$\overline{FORCEOFF}$, FORCEON, $\overline{EN}$			±0.01	±1	µA
I_{CC}	Supply current (T_A = 25°C)	Auto-powerdown disabled	No load, $\overline{FORCEOFF}$ and FORCEON at V_{CC}		0.3	1	mA
		Powered off	No load, $\overline{FORCEOFF}$ at GND		1	10	µA
		Auto-powerdown enabled	No load, $\overline{FORCEOFF}$ at V_{CC}, FORCEON at GND, All RIN are open or grounded		1	10	

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

5.7 Electrical Characteristics, Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see 図 8-1)

PARAMETER		TEST CONDITIONS(1)			MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	DOUT at R_L = 3 kΩ to GND,	DIN = GND		5	5.4		V
V_{OL}	Low-level output voltage	DOUT at R_L = 3 kΩ to GND,	DIN = V_{CC}		–5	–5.4		V
I_{IH}	High-level input current	V_I = V_{CC}				±0.01	±1	µA
I_{IL}	Low-level input current	V_I at GND				±0.01	±1	µA
I_{OS}	Short-circuit output current(3)	V_{CC} = 3.6 V,	V_O = 0 V			±35	±60	mA
		V_{CC} = 5.5 V,	V_O = 0 V			±35	±90	
r_o	Output resistance	V_{CC}, V+, and V– = 0 V,	V_O = ±2 V		300	10M		Ω
I_{off}	Output leakage current	$\overline{FORCEOFF}$ = GND	V_O = ±12 V,	V_{CC} = 3 V to 3.6 V			±25	µA
			V_O = ±10 V,	V_{CC} = 4.5 V to 5.5 V			±25	

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Short-circuit durations must be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output can be shorted at a time.

5.8 Switching Characteristics, Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see 図 8-1)

PARAMETER		TEST CONDITIONS(1)			MIN	TYP(2)	MAX	UNIT
Maximum data rate (see 図 6-1)		R_L = 3 kΩ	C_L = 1000 pF		250			kbit/s
			C_L = 250 pF,	V_{CC} = 3 V to 4.5 V	1000			
			C_L = 1000 pF,	V_{CC} = 4.5 V to 5.5 V	1000			
$t_{sk(p)}$	Pulse skew(3)	C_L = 250 pF	R_L = 3 kΩ 図 6-2	RGT Package		25		ns
		C_L = 150 pF to 2500 pF,	R_L = 3 kΩ to 7 kΩ, See 図 6-2	DB or PW package		100		
SR(tr)	Slew rate, transition region (see 図 6-1)	V_{CC} = 3.3 V,	R_L = 3 kΩ to 7 kΩ,	C_L = 150 pF to 1000 pF	18		150	V/µs

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} – t_{PHL}|$ of each channel of the same device.

5.9 Electrical Characteristics, Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see 図 8-1)

PARAMETER		TEST CONDITIONS(1)	MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA	V_{CC} – 0.6 V	V_{CC} – 0.1 V		V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 3.3 V		1.6	2.4	V
		V_{CC} = 5 V		1.9	2.4	
$V_{IT–}$	Negative-going input threshold voltage	V_{CC} = 3.3 V	0.6	1.1		V
		V_{CC} = 5 V	0.8	1.4		
V_{hys}	Input hysteresis ($V_{IT+} – V_{IT–}$)			0.5		V
I_{off}	Output leakage current	$\overline{FORCEOFF}$ = 0 V		±0.05	±10	µA
r_i	Input resistance	V_I = ±3 V to ±25 V	3	5	7	kΩ

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

5.10 Switching Characteristics, Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see 図 8-1)

PARAMETER		TEST CONDITIONS(1)		TYP(2)	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 150 pF, See 図 6-3	RGT package	100	ns
			DB or PW package	150	
t_{PHL}	Propagation delay time, high- to low-level output	C_L = 150 pF, See 図 6-3	RGT package	125	ns
			DB or PW package	150	
t_{en}	Output enable time	C_L = 150 pF, R_L = 3 kΩ, See 図 6-4		200	ns
t_{dis}	Output disable time	C_L = 150 pF, R_L = 3 kΩ, See 図 6-4		200	ns
$t_{sk(p)}$	Pulse skew(3)	See 図 6-3	RGT package	25	ns
			DB or PW package	50	

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} – t_{PHL}|$ of each channel of the same device.

5.11 Electrical Characteristics, Auto-Powerdown

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 図 6-5)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{T+(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}		2.7	V
$V_{T–(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}	–2.7		V
$V_{T(invalid)}$	Receiver input threshold for $\overline{INVALID}$ low-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}	–0.3	0.3	V
V_{OH}	$\overline{INVALID}$ high-level output voltage	I_{OH} = –1 mA, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}	V_{CC} – 0.6		V
V_{OL}	$\overline{INVALID}$ low-level output voltage	I_{OL} = 1.6 mA, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}		0.4	V

5.12 Switching Characteristics, Auto-Powerdown

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 図 6-5)

PARAMETER		TYP(1)	UNIT
t_{valid}	Propagation delay time, low- to high-level output	1	µs
$t_{invalid}$	Propagation delay time, high- to low-level output	30	µs
t_{en}	Supply enable time	100	µs

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

5.13 Typical Characteristics

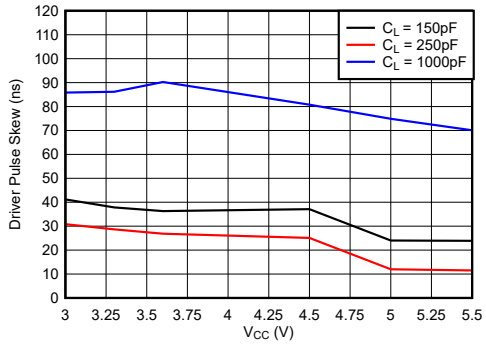


図 5-1. Driver Pulse Skew vs Load Capacitance and Supply Voltage at T_A = 25°C (RGT Package)

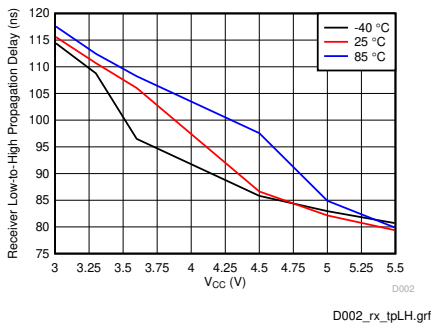


図 5-2. Receiver Path Low-to-High Propagation Delay vs T_A and Supply Voltage (RGT Package)

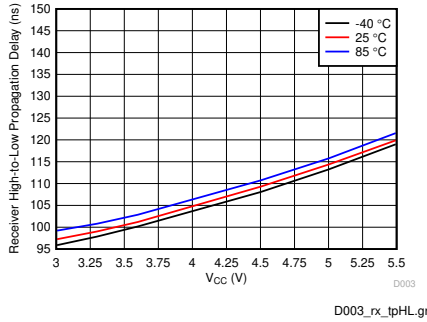


図 5-3. . Receiver Path High-to-Low Propagation Delay vs TA and Supply Voltage (RGT Package)

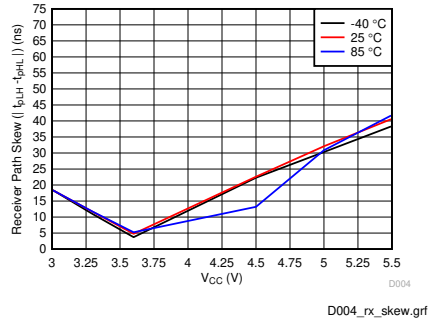
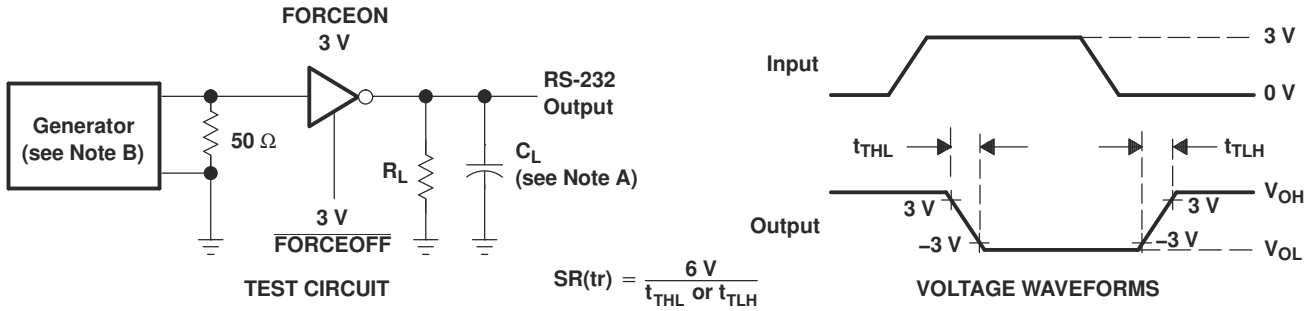


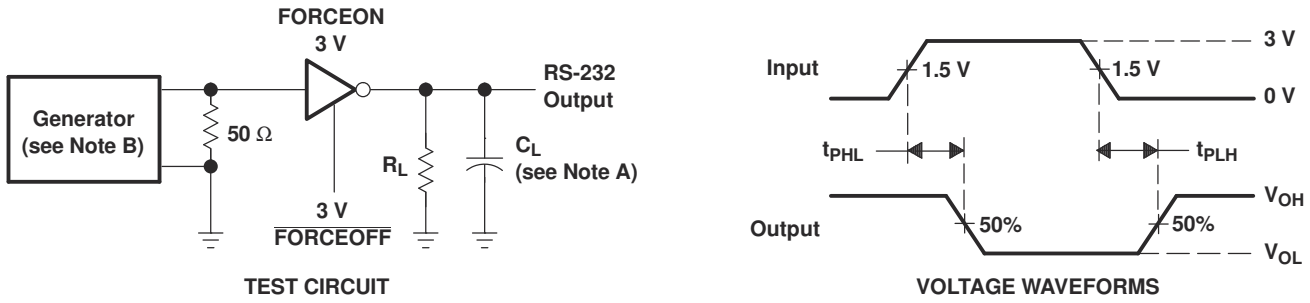
図 5-4. Receiver Pulse Skew ($|t_{pLH} - t_{pHL}|$) vs T_A and Supply Voltage (RGT Package)

6 Parameter Measurement Information



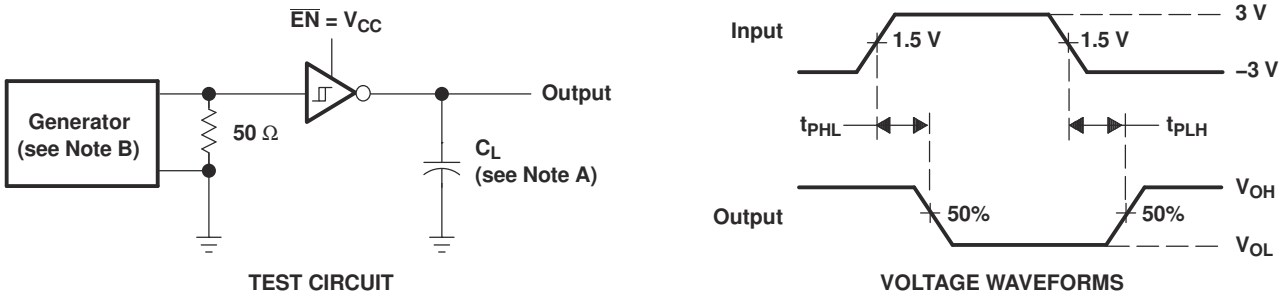
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

図 6-1. Driver Slew Rate



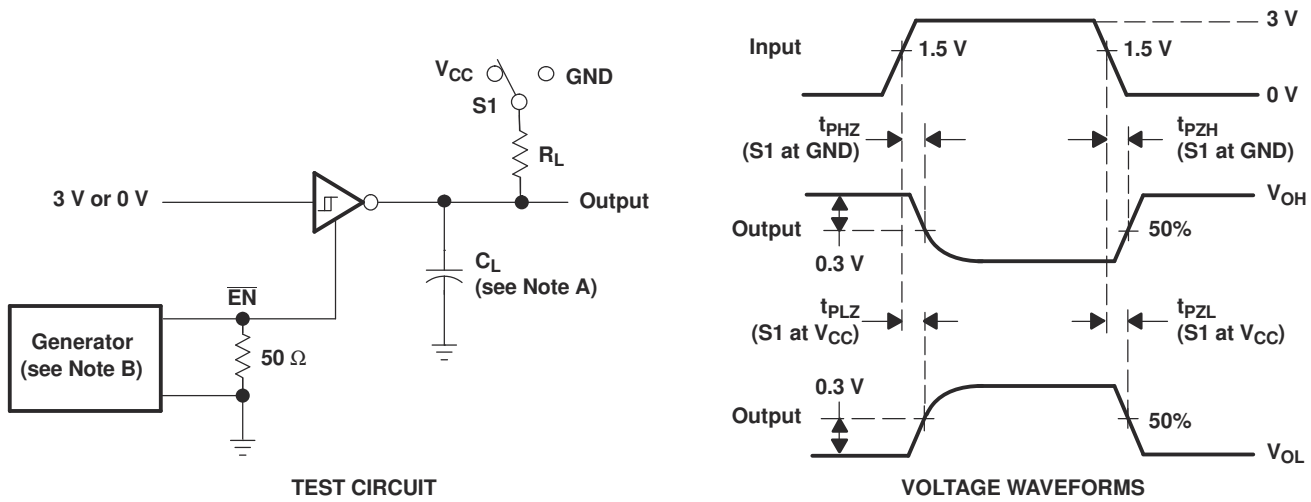
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

図 6-2. Driver Pulse Skew



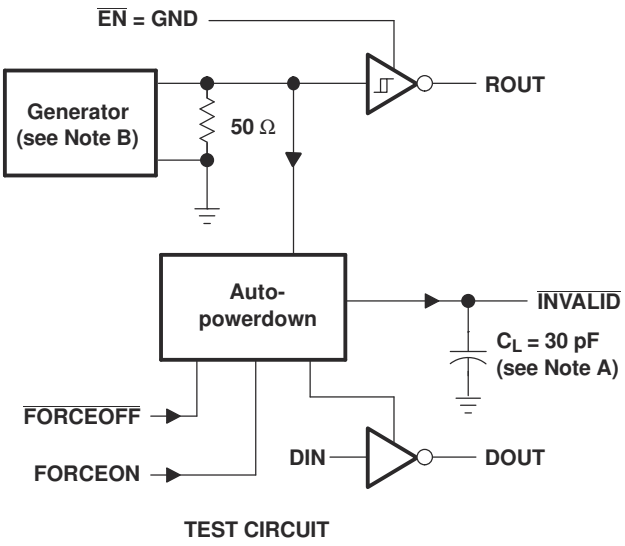
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

図 6-3. Receiver Propagation Delay Times

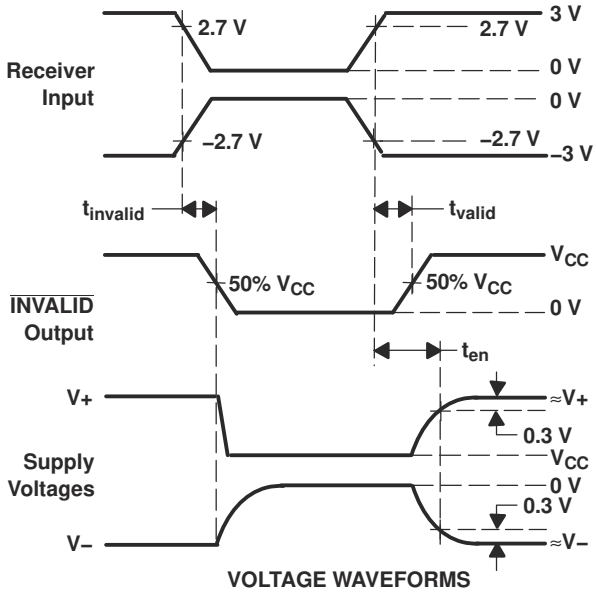


NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.
C. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
D. t_{PZL} and t_{PZH} are the same as t_{en}.

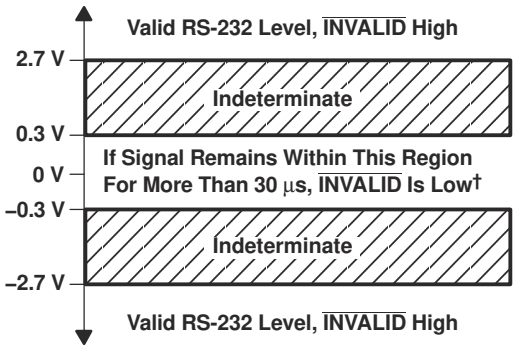
図 6-4. Receiver Enable and Disable Times



TEST CIRCUIT



VOLTAGE WAVEFORMS



† Auto-powerdown disables drivers and reduces supply current to 1 µA.

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 5 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

図 6-5. $\overline{\text{INVALID}}$ Propagation Delay Times and Driver Enabling Time

7 Detailed Description

7.1 Overview

The TRSF3221E consists of one line driver, one line receiver, and a dual charge-pump circuit with ±15kV IEC ESD protection pin to pin (serial-port connection pins, including GND). The TRSF3221E provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3V to 5.5V supply. The TRSF3221E operates at data signaling rates up to 1Mbit/s and a driver output slew rate of 24V/µs to 150V/µs.

Flexible control options for power management are available when the serial port is inactive. The auto-powerdown feature functions when FORCEON is low and $\overline{\text{FORCEOFF}}$ is high. During this mode of operation, if the TRSF3221E does not sense a valid RS-232 signal on the receiver input, the driver output is disabled. If $\overline{\text{FORCEOFF}}$ is set low and the enable ($\overline{\text{EN}}$) input is high, both the driver and receiver are shut off, and the supply current is reduced to 1µA. Disconnecting the serial port or turning off the peripheral drivers causes the auto-powerdown condition to occur. Auto-powerdown can be disabled when FORCEON and $\overline{\text{FORCEOFF}}$ are high. With auto-powerdown enabled, the device is activated automatically when a valid signal is applied to the receiver input. The $\overline{\text{INVALID}}$ output notifies the user if an RS-232 signal is present at the receiver input. $\overline{\text{INVALID}}$ is high (valid data) if the receiver input voltage is greater than 2.7V or less than –2.7V, or has been between –0.3V and 0.3V for less than 30µs. $\overline{\text{INVALID}}$ is low (invalid data) if the receiver input voltage is between –0.3V and 0.3V for more than 30µs. Outputs are protected against shorts to ground.

7.2 Functional Block Diagram

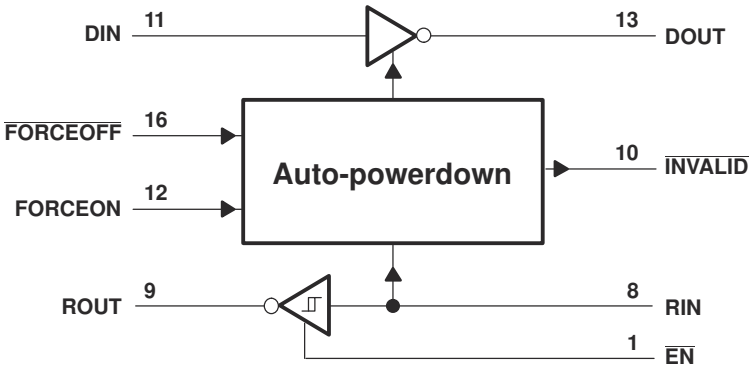


図 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

The power block increases, inverts, and regulates voltage at V+ and V– pins using a charge pump that requires four external capacitors. Auto-power-down feature for driver is controlled by FORCEON and $\overline{\text{FORCEOFF}}$ inputs. Receiver is controlled by $\overline{\text{EN}}$ input. When MAX3221E is unpowered, it can be safely connected to an active remote RS-232 device.

The driver interfaces the standard logic level to RS232 voltage levels. The DIN input must be valid high or low.

The receiver interfaces RS-232 levels to standard logic levels. An open input results in a high output on ROUT. RIN input includes an internal standard RS-232 load. A logic high input on the $\overline{\text{EN}}$ pin shuts down the receiver output.

7.4 Device Functional Modes

Functional Tables, Each Driver

INPUTS[1]				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	$\overline{\text{FORCEOFF}}$	VALID RIN RS-232 LEVEL		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	
L	L	H	No	Z	Powered off by auto-powerdown feature
H	L	H	No	Z	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

Each Receiver

INPUTS[1]			OUTPUT ROUT
RIN	$\overline{\text{EN}}$	VALID RIN RS-232 LEVEL	
L	L	X	H
H	L	X	L
X	H	X	Z
Open	L	No	H

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = disconnected input or connected driver off

8 Application and Implementation

注

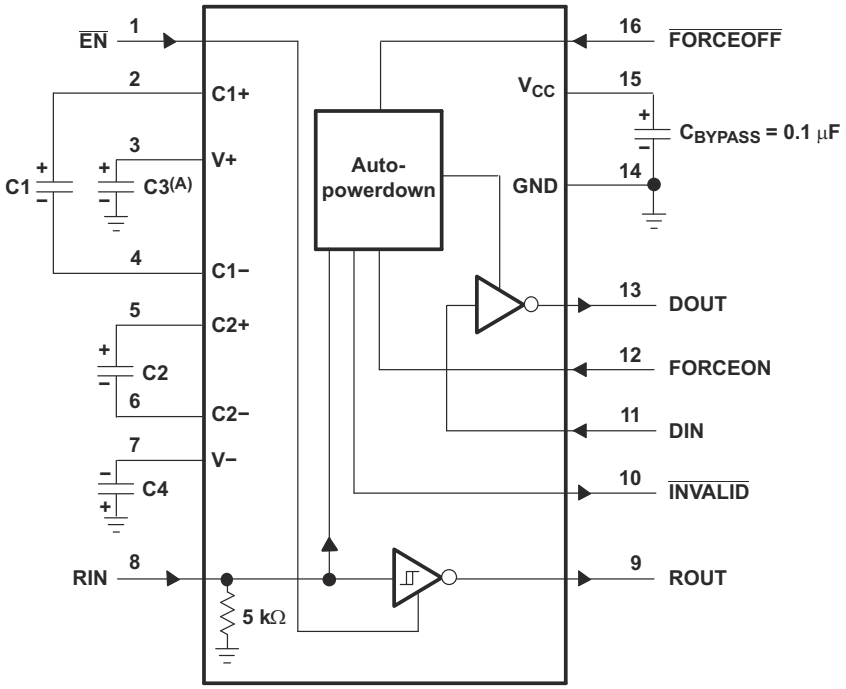
以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The TRSF3221E line driver and receiver is a specialized device for 3V to 5.5V RS-232 communication applications. This application is a generic implementation of this device with all required external components. For proper operation, add capacitors as shown in 表 8-1.

8.1.1 Typical Application

ROUT and DIN connect to UART or general purpose logic lines. FORCEON and $\overline{\text{FORCEOFF}}$may be connected general purpose logic lines or tied to ground or VCC. $\overline{\text{INVALID}}$ may be connected to a general purpose logic line or left unconnected. RIN and DOUT lines connect to a RS-232 connector or cable. DIN, FORCEON, and $\overline{\text{FORCEOFF}}$ inputs must not be left unconnected.



A. C3 can be connected to V_{CC} or GND.
B. Resistor values shown are nominal.
C. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they must be connected as shown.

図 8-1. Typical Operating Circuit and Capacitor Values

表 8-1. V_{CC} vs Capacitor Values

V_{CC}	C1	C2, C3, C4
3.3V ± 0.3V	0.1µF	0.1µF
5V ± 0.5V	0.047µF	0.33µF
3V to 5.5V	0.1µF	0.47µF

8.1.1.1 Design Requirements

- Recommended VCC is 3.3V or 5V – 3V to 5.5V is also possible
- Maximum recommended bit rate is 1Mbps
- Use capacitors as shown in 図 8-1 and 表 8-1

8.1.1.2 Detailed Design Procedure

For proper operation:

- DIN, $\overline{\text{FORCEOFF}}$ and FORCEON inputs must be connected to valid low or high logic levels
- Select capacitor values based on VCC level for best performance

ROUT and DIN connect to UART or general purpose logic lines. FORCEON and $\overline{\text{FORCEOFF}}$ may be connected general purpose logic lines or tied to ground or VCC. $\overline{\text{INVALID}}$ may be connected to a general purpose logic line or left unconnected. RIN and DOUT lines connect to a RS232 connector or cable. DIN, FORCEON, and $\overline{\text{FORCEOFF}}$ inputs must not be left unconnected.

8.1.2 Application Performance Plot

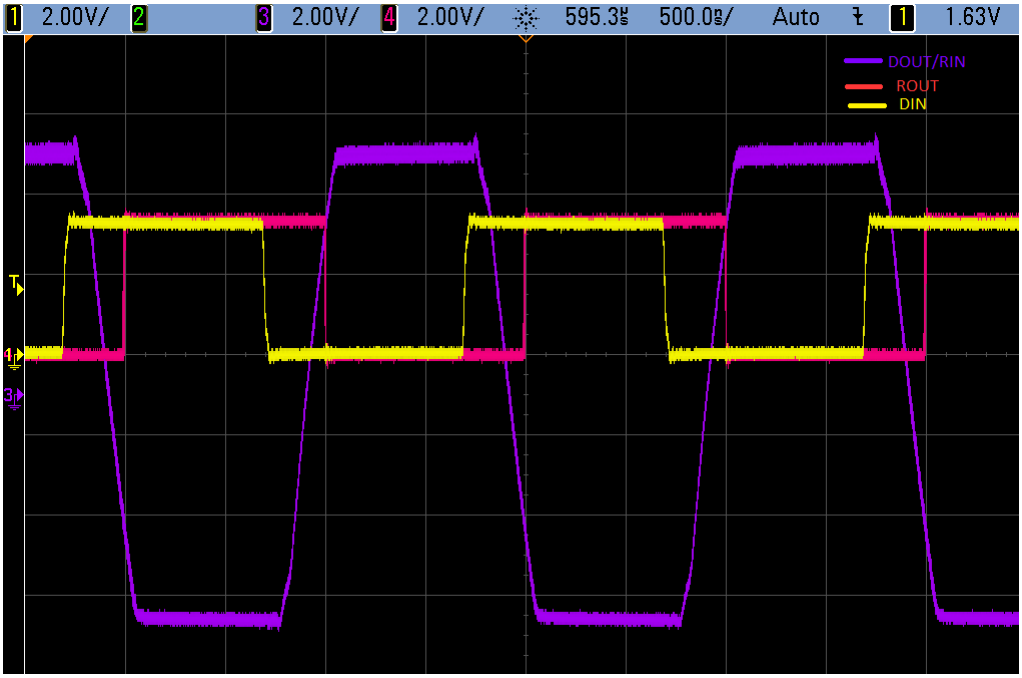


図 8-2. 1 Mbps Driver to Receiver Loopback Timing Waveform, V_{CC} = 3.3 V

8.2 Power Supply Recommendations

V_{CC} must be between 3V and 5.5V. Charge pump capacitors must be chosen using V_{CC} vs Capacitor Values.

8.3 Layout

8.3.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes, which have the fastest rise and fall times.

8.3.2 Layout Example

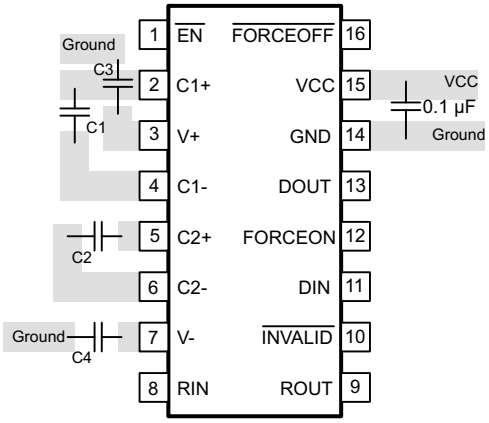


図 8-3. Layout Diagram

9 Device and Documentation Support

9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.2 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

9.3 商標

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

9.4 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (July 2021) to Revision C (December 2024)	Page
• 「製品情報」表を「パッケージ情報」表に変更	1
• データシートに SOT-23-THN (DYY) パッケージを追加	1
• Added Note 2 to the *ESD Ratings, IEC Specifications*	5

Changes from Revision A (May 2021) to Revision B (July 2021)	Page
• *「アプリケーション」*の一覧を変更	1
• Changed the table note for the *ESD Ratings, IEC Specifications* table to make it also applicable to PW package	5
• Changed the thermal information for PW package	6

Changes from Revision * (August 2007) to Revision A (May 2021)	Page
• 「製品情報」表、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRSF3221ECDB	OBSOLETE	SSOP	DB	16		TBD	Call TI	Call TI	0 to 70	RT21EC	
TRSF3221ECDBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	RT21EC	Samples
TRSF3221ECPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	RT21EC	Samples
TRSF3221EIDBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT21EI	Samples
TRSF3221EIDYYR	ACTIVE	SOT-23-THIN	DYY	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT21EI	Samples
TRSF3221EIPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	RT21EI	Samples
TRSF3221EIRGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	F3221	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

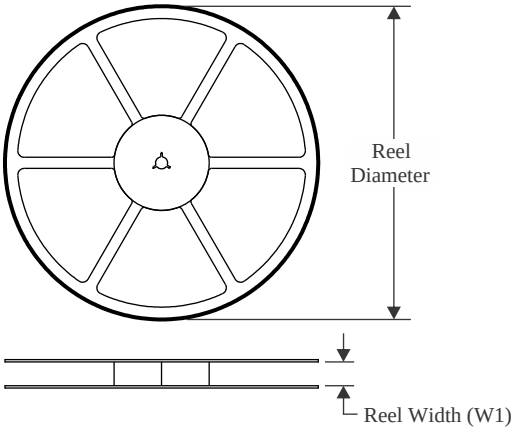
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

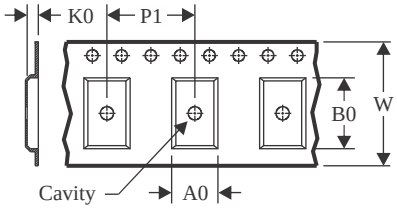
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

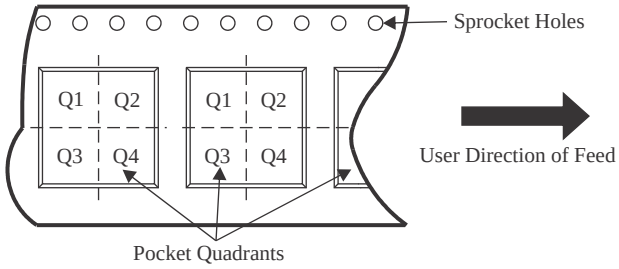


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

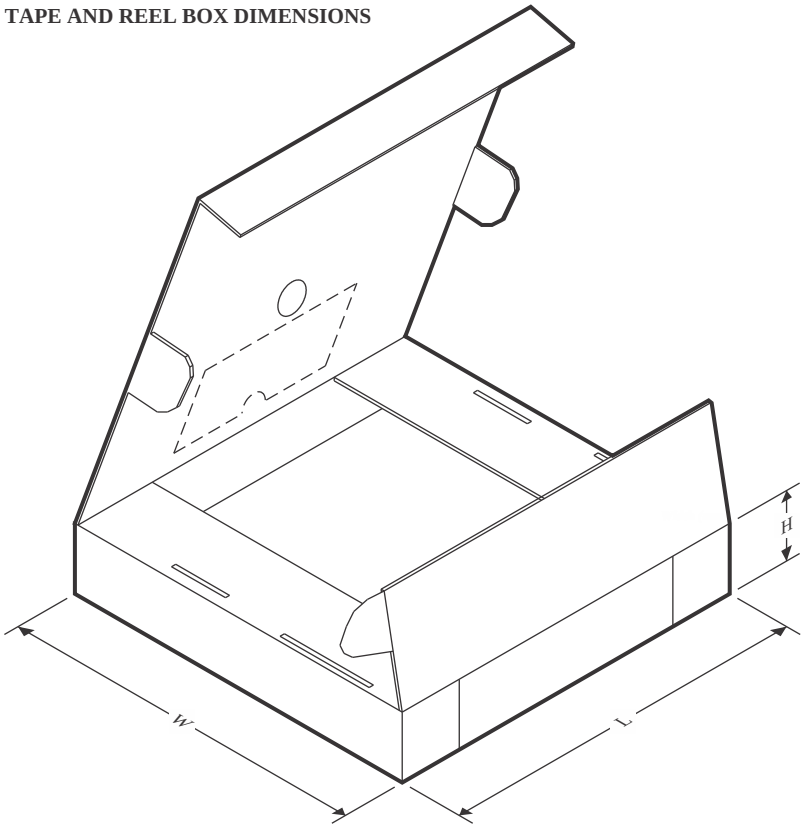
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRSF3221ECDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TRSF3221ECPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRSF3221EIDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TRSF3221EIDYYR	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TRSF3221EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRSF3221EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRSF3221EIRGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

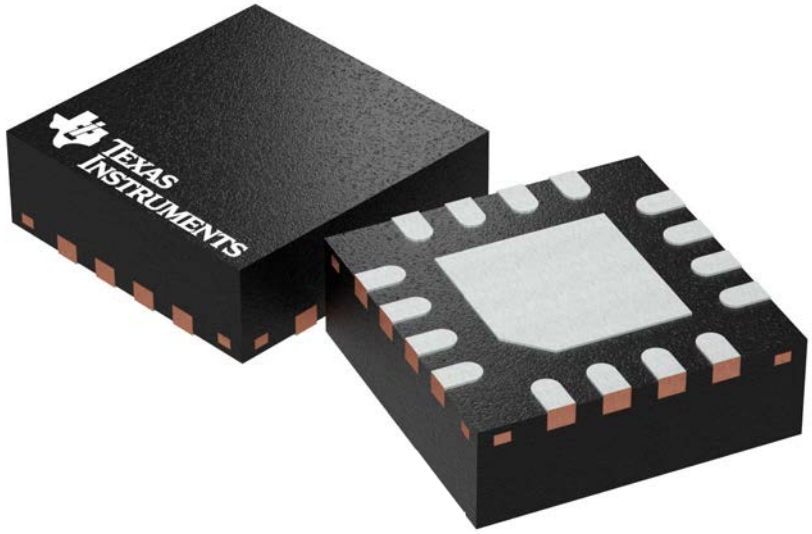


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRSF3221ECDBR	SSOP	DB	16	2000	356.0	356.0	35.0
TRSF3221ECPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TRSF3221EIDBR	SSOP	DB	16	2000	356.0	356.0	35.0
TRSF3221EIDYYR	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
TRSF3221EIPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TRSF3221EIPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TRSF3221EIRGTR	VQFN	RGT	16	3000	367.0	367.0	35.0

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



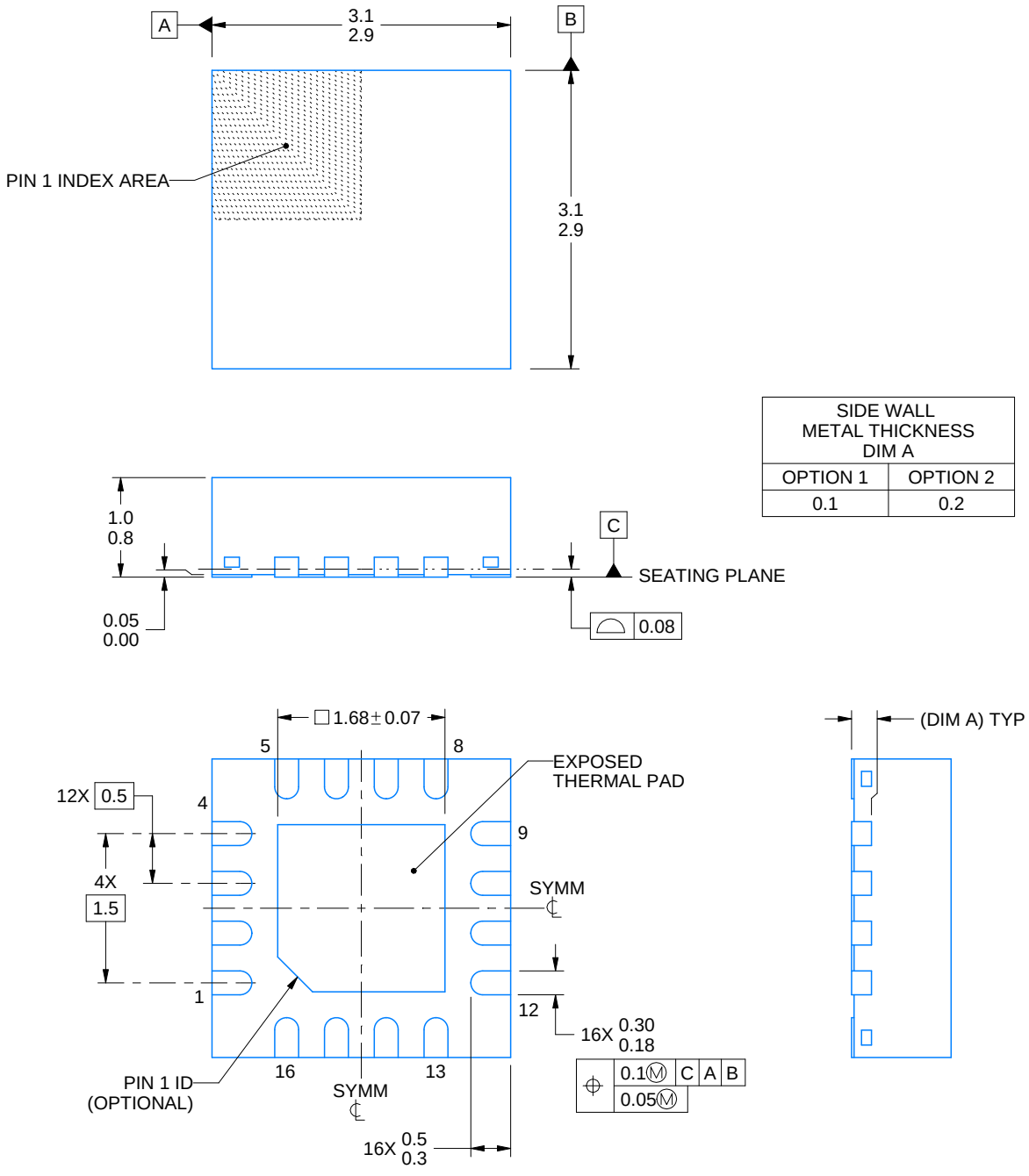
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGT0016C

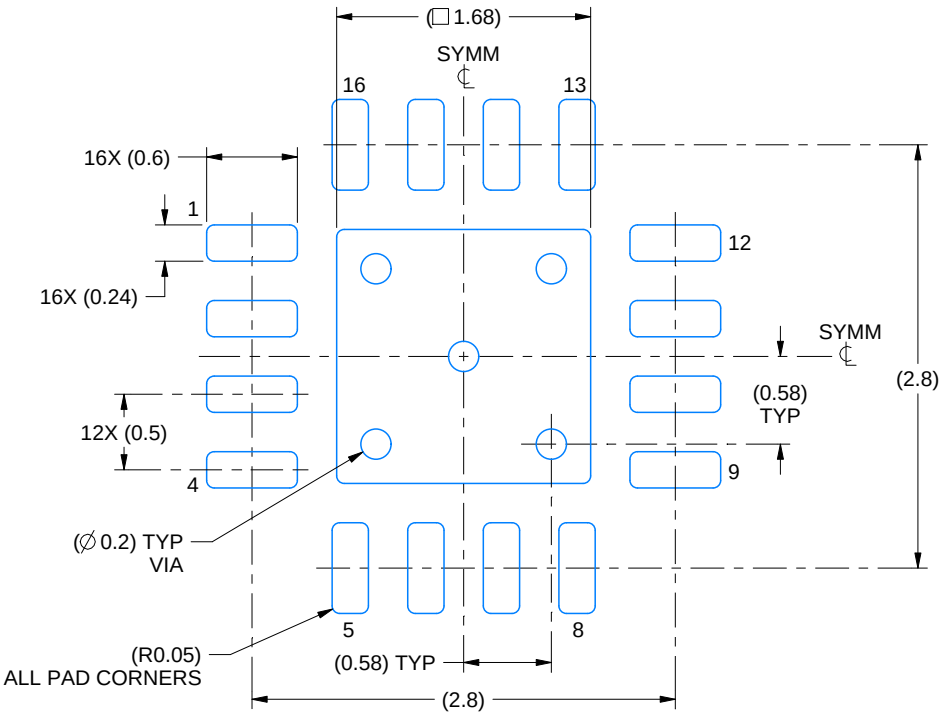
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

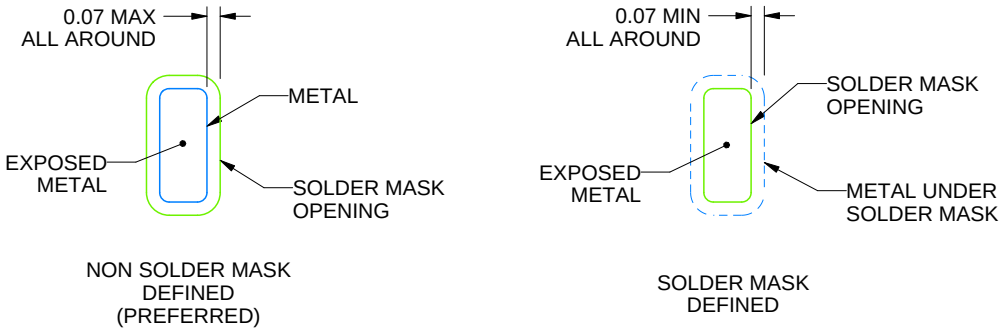


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

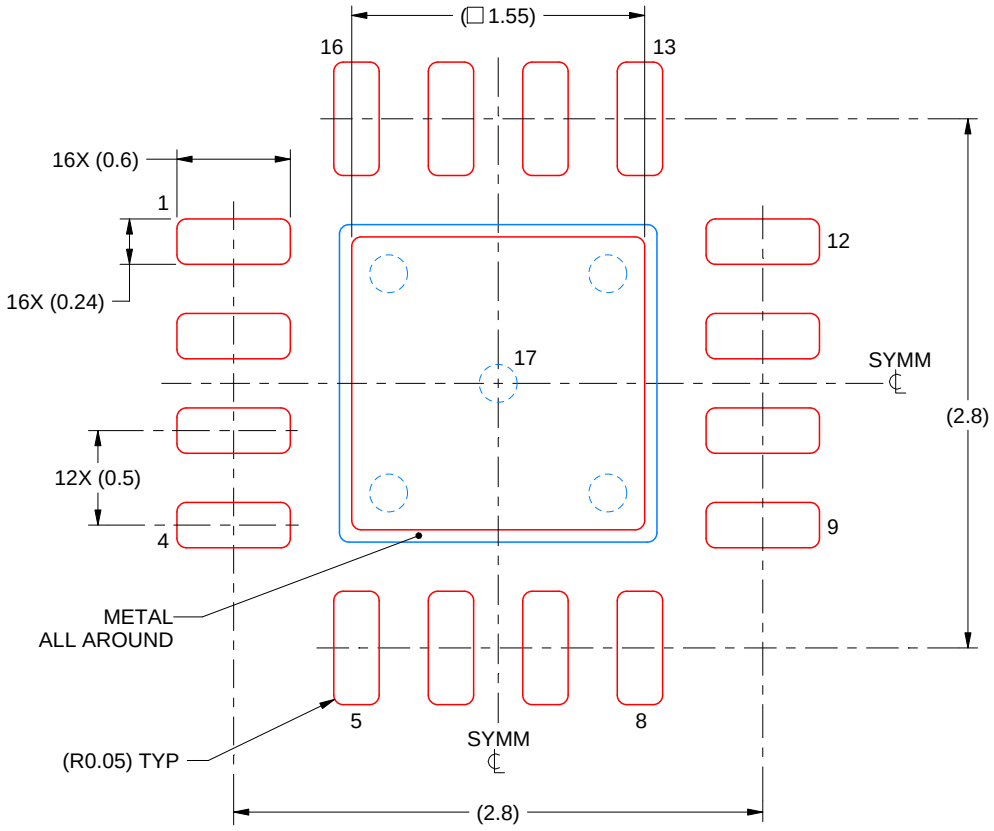


SOLDER MASK DETAILS

4222419/D 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222419/D 04/2022

NOTES: (continued)

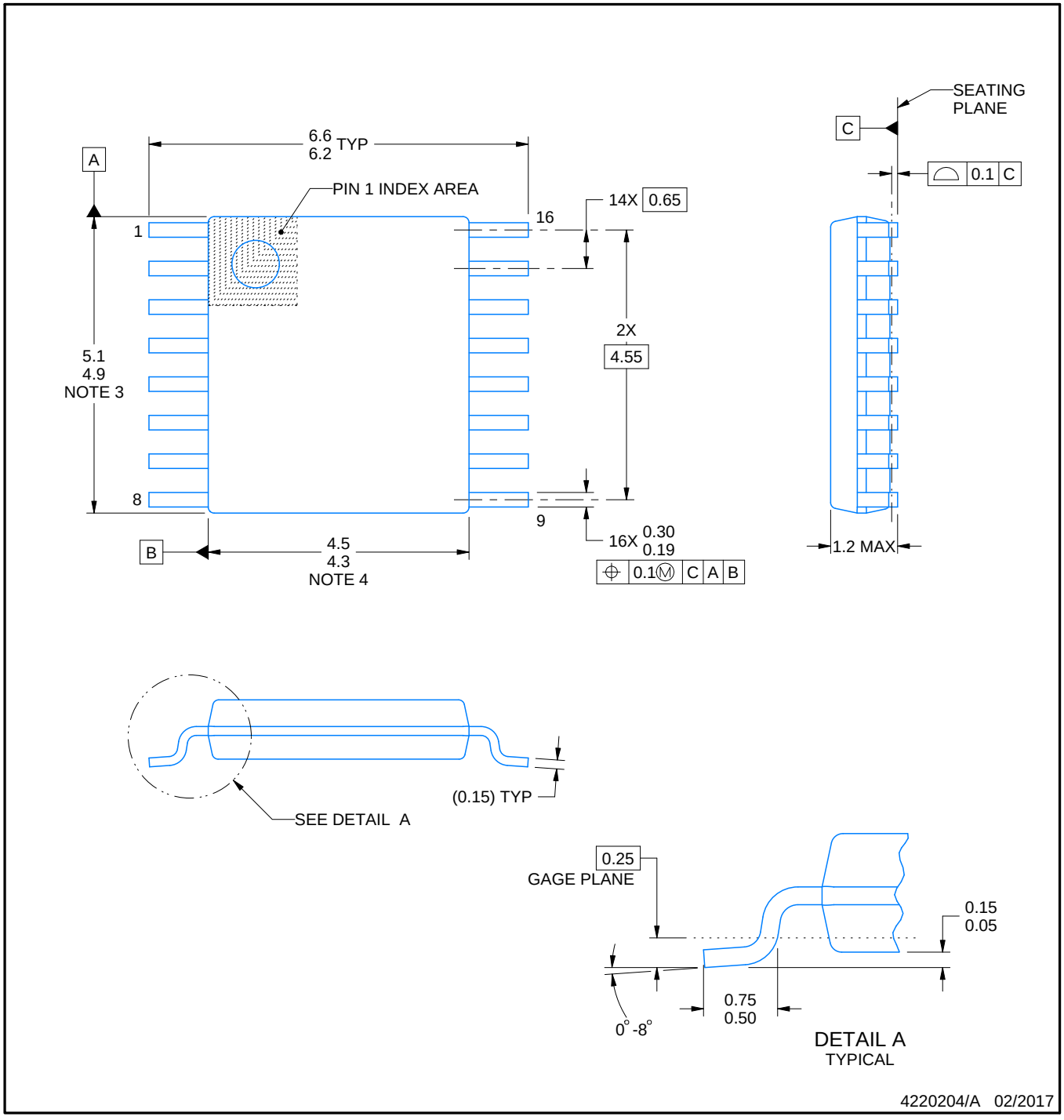
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0016A

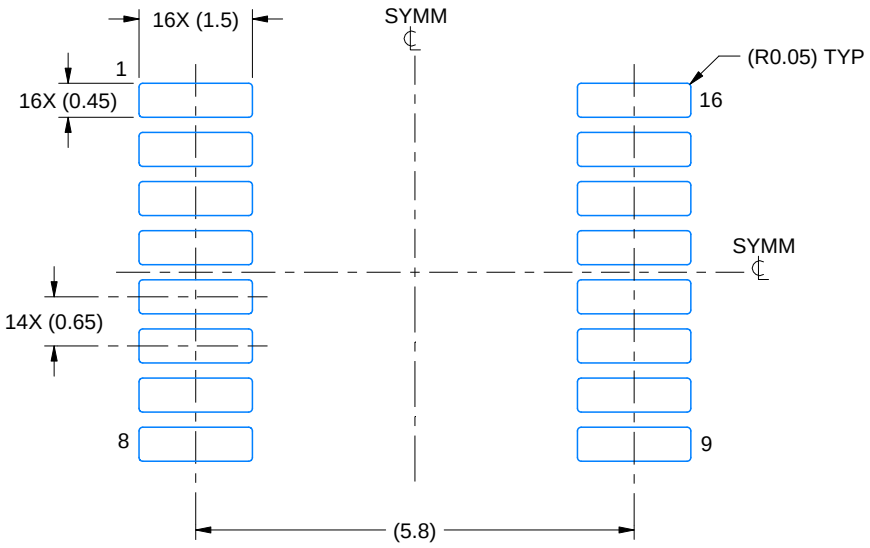
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

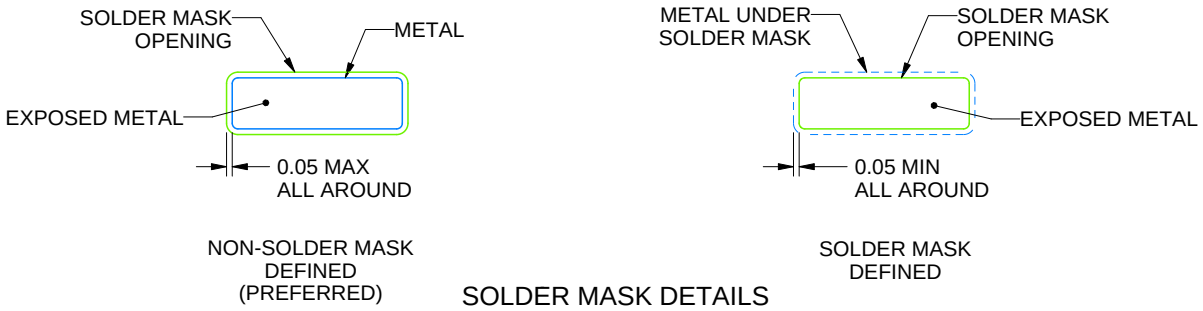


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

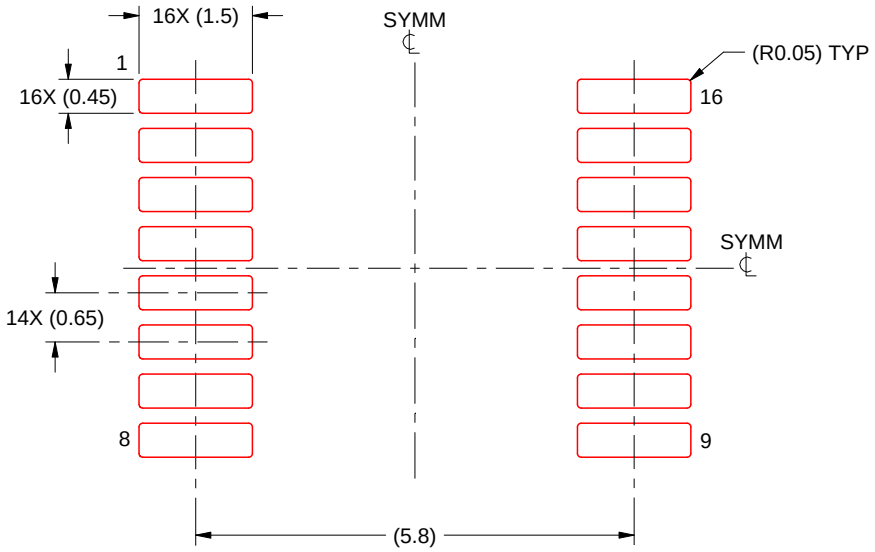


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

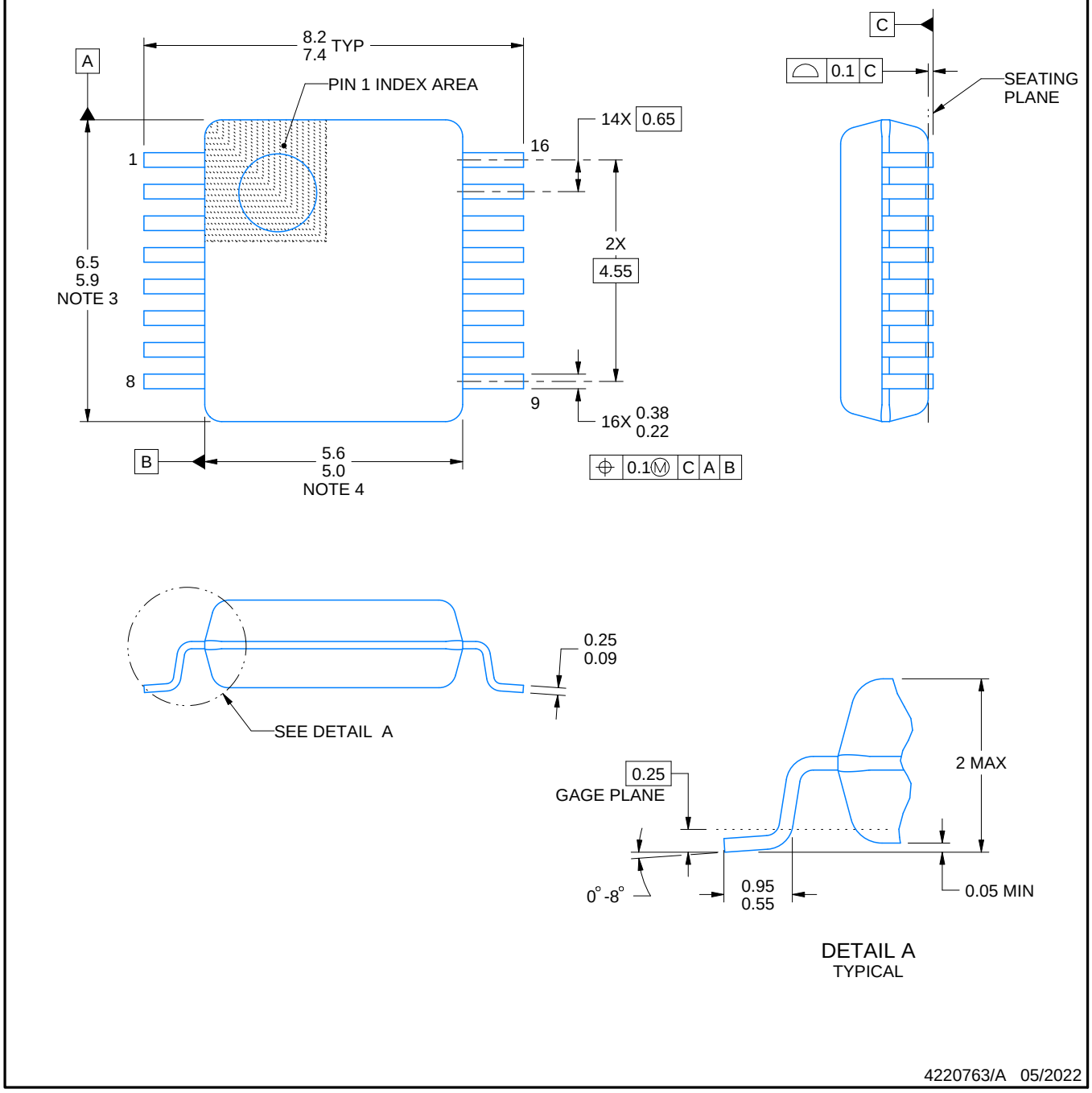
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DB0016A

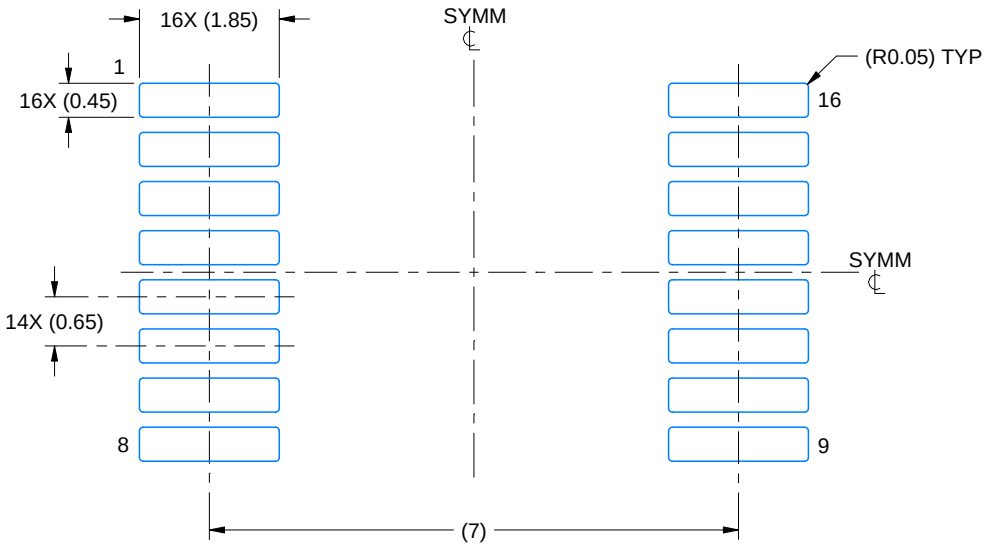
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

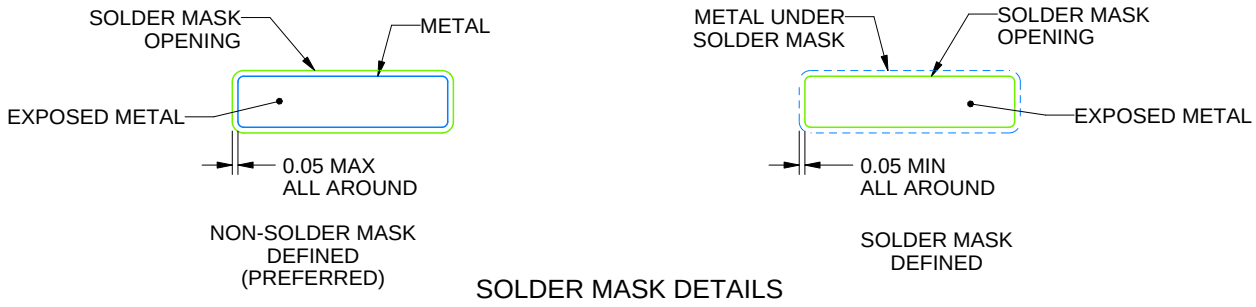


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

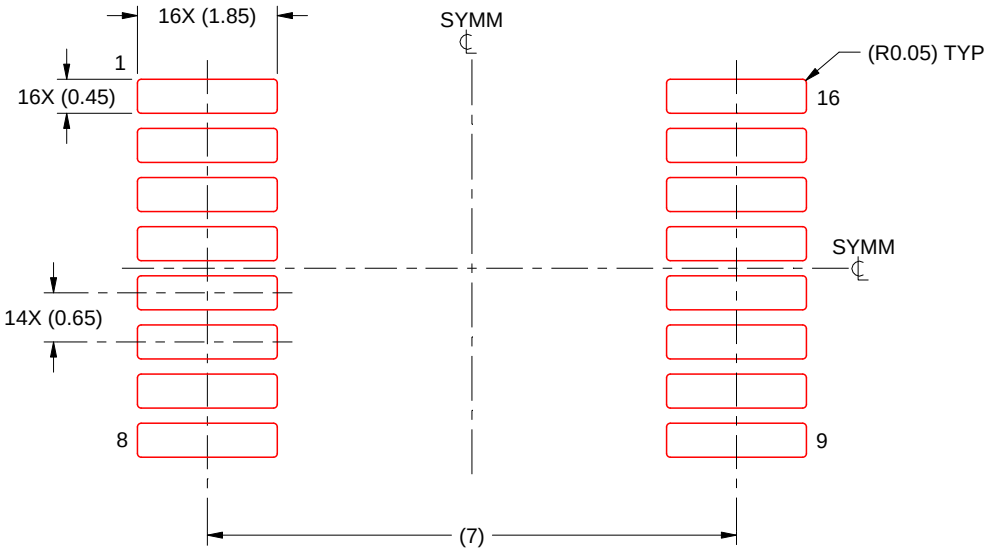


SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

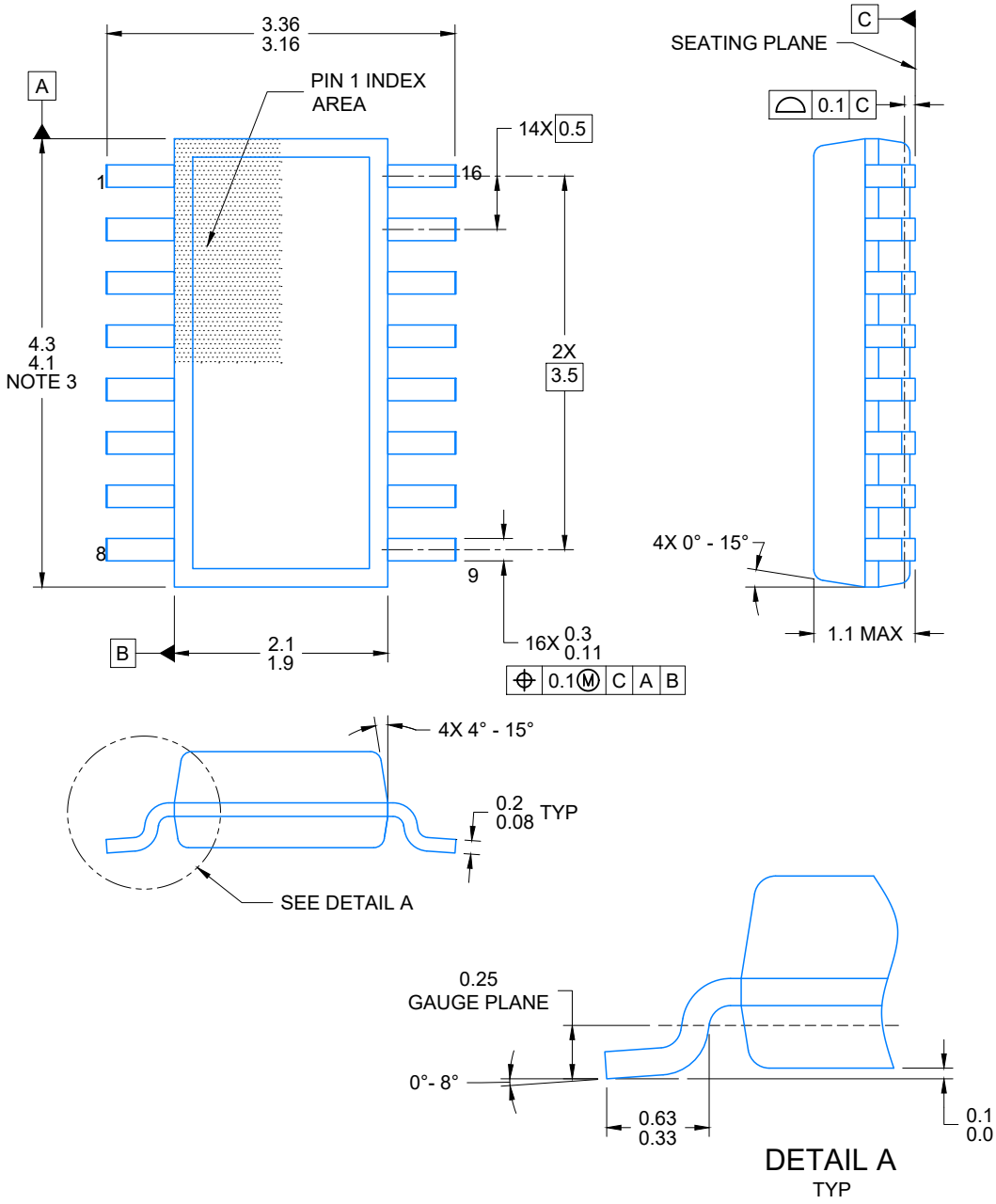
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DYY0016A

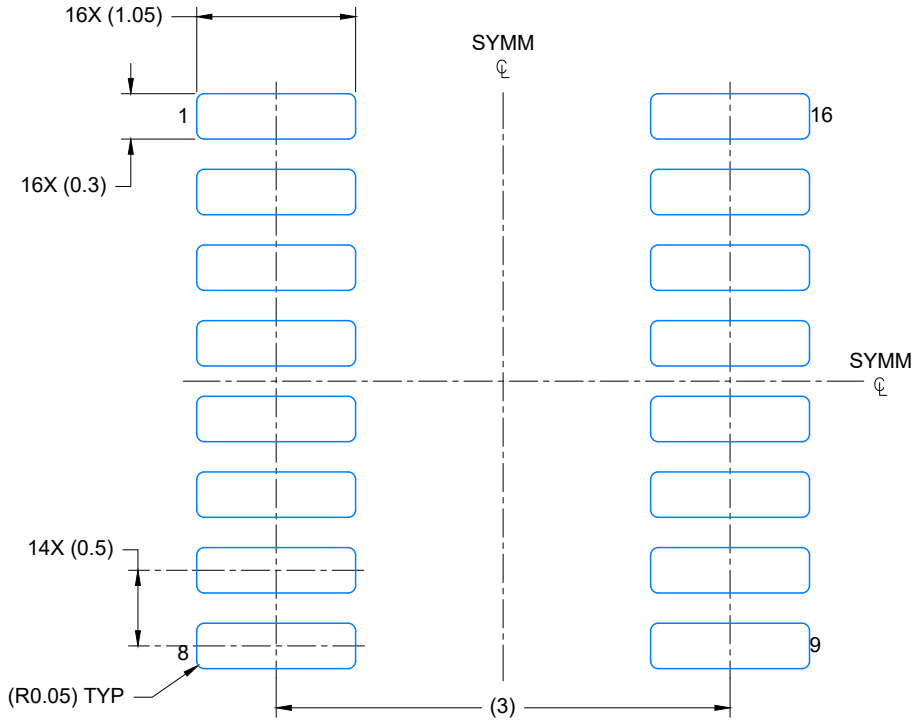
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

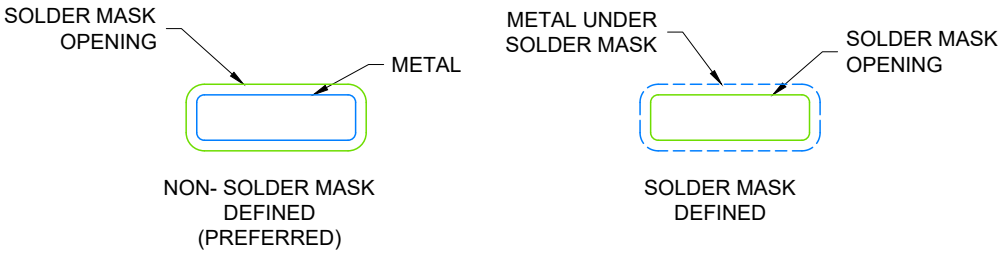


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4224642/D 07/2024

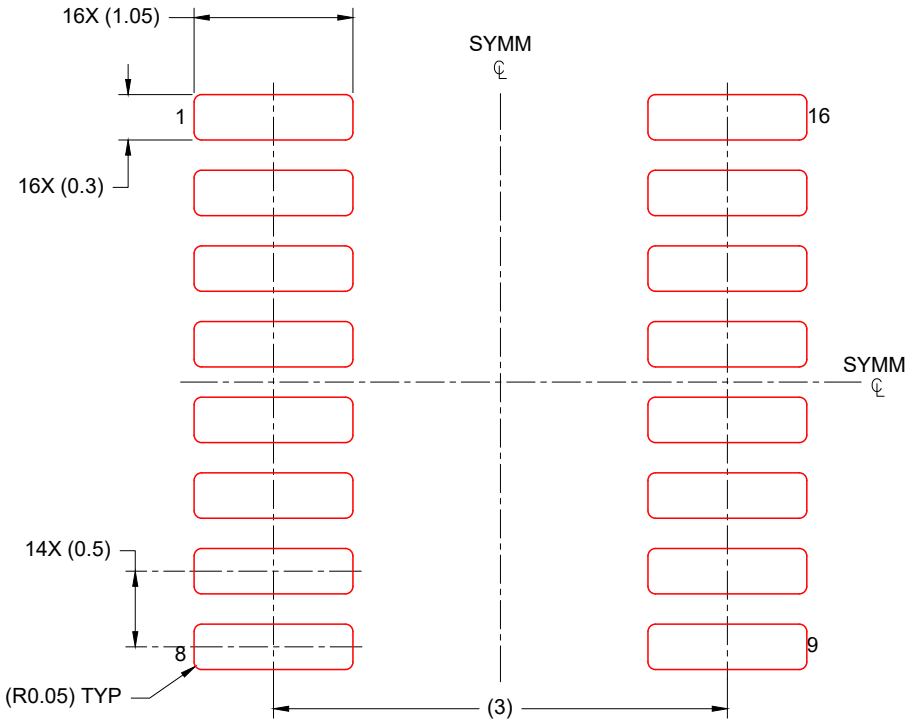
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224642/D 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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