TS5A23157 デュアル10Ω SPDTアナログ・スイッチ

1 特長

- 低いオン抵抗(125℃で15Ω)
- 125℃で動作
- 制御入力は5V許容
- Break-Before-Makeスイッチングを規定
- 低い電荷注入
- 優れたオン抵抗マッチング
- 低い全高調波歪み
- 1.8V～5.5Vの単電源で動作
- JESD 78, Class II準拠で100mA超のラッチアップ性能
- ESD性能はJESD 22に準拠しテスト済み
  - 人体モデルで2000V (A114-B、クラスII)
  - 荷電デバイス・モデルで1000V (C101)

2 アプリケーション

- サンプル・アンド・ホールド回路
- バッテリ駆動の機器
- オーディオおよびビデオ信号のルーティング
- 通信用回路

3 概要

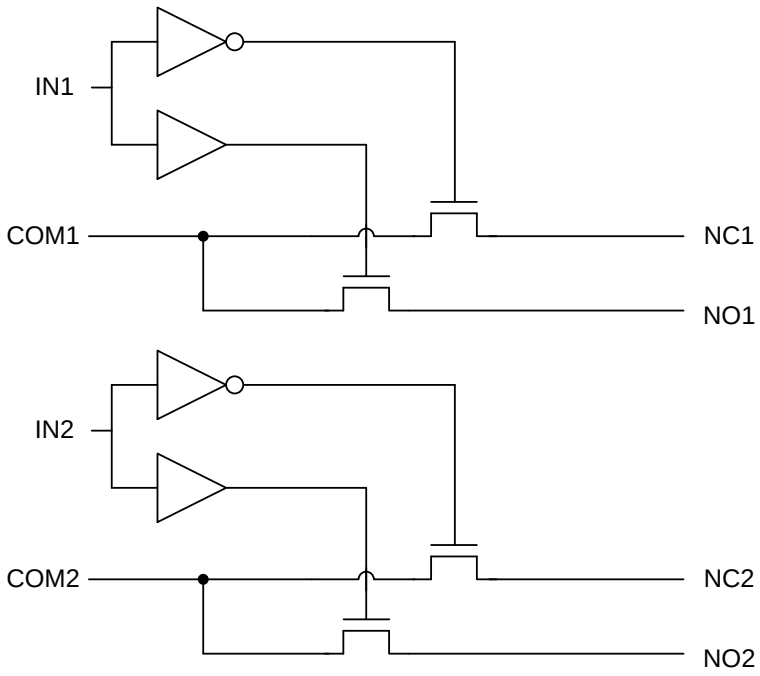
TS5A23157はデュアル単極双投(SPDT)アナログ・スイッチで、1.65V～5.5Vで動作するように設計されています。このデバイスはデジタルとアナログの両方の信号を処理でき、最大5.5V(ピーク)の信号をどちらの方向にも転送できます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TS5A23157DGS	VSSOP (10)	3.00mm×3.00mm
TS5A23157RSE	UQFN (10)	2.00mm×1.50mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

ブロック図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

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- Changed the Operating temperature MAX value From: 85°C To: 125°C in the *Recommended Operating Conditions* table ... 4
- Changed the *Thermal Information* table ... 4
- Changed r_{on} in the *Electrical Characteristics for 5-V Supply* table ... 5
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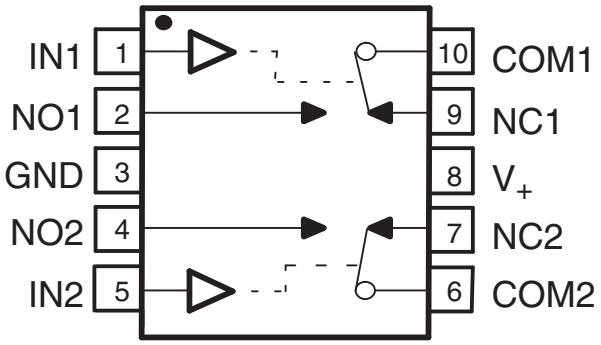
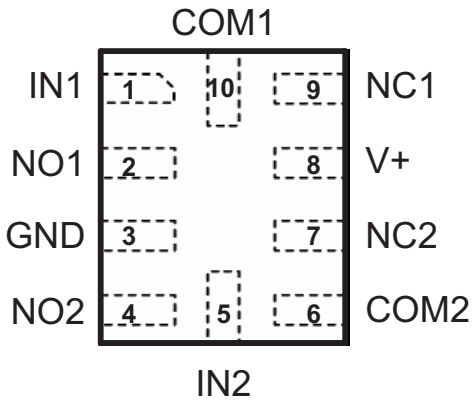
5 Pin Configuration and Functions

DGS Package
10-Pin VSSOP
Top View



RSE Package
10-Pin UQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IN1	I	Select pin for switch 1
2	NO1	I/O	Normally open I/O for switch 1
3	GND	—	Ground
4	NO2	I/O	Normally open I/O for switch 2
5	IN2	I	Select pin for switch 2
6	COM2	I/O	Common I/O for switch 2
7	NC2	I/O	Normally closed I/O for switch 2
8	V+	—	Power supply pin
9	NC1	I/O	Normally closed I/O for switch 1
10	COM1	I/O	Common I/O for switch 1

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_+	Supply voltage(2)		–0.5	6.5	V
V_{NC} V_{NO} V_{COM}	Analog voltage(2)(3)(4)		–0.5	V_+ + 0.5	V
$I_{I/OK}$	Analog port diode current	V_{NC}, V_{NO}, V_{COM} < 0 or V_{NC}, V_{NO}, V_{COM} > V_+		±50	mA
I_{NC} I_{NO} I_{COM}	On-state switch current	V_{NC}, V_{NO}, V_{COM} = 0 to V_+		±50	mA
V_{IN}	Digital input voltage(2)(3)		–0.5	6.5	V
I_{IK}	Digital input clamp current	V_{IN} < 0		–50	mA
	Continuous current through V_+ or GND			±100	mA
T_J	Junction Temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) This value is limited to 5.5 V maximum.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{I/O}$	Switch input/output voltage	0	V_+	V
V+	Supply voltage	1.65	5.5	V
V_I	Control input voltage	0	5.5	V
T_A	Operating temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TS5A23157		UNIT
		DGS (VSSOP)	RSE (UQFN)	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	210.5	215.4	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	99.1	140.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	132.4	137.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	29.1	13.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	130.5	137.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics for 5-V Supply

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_+	V
r_{on}	ON-state resistance	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = –30 mA,	Switch ON, see Figure 9	Full	4.5 V			10	Ω
				-40 to 125°C				15	
Δr_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 3.15 V, I_{COM} = –30 mA,	Switch ON, see Figure 9	25°C	4.5 V		0.15		Ω
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = –30 mA,	Switch ON, see Figure 9	25°C	4.5 V		4		Ω
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO OFF leakage current	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = 0 to V_+,	Switch OFF, see Figure 10	25°C	5.5 V	–1	0.05	1	μA
				Full		–1		1	
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO ON leakage current	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = Open,	Switch ON, see Figure 10	25°C	5.5 V	–0.1		0.1	μA
				Full		–1		1	
$I_{COM(ON)}$	COM ON leakage current	V_{NC} or V_{NO} = Open, V_{COM} = 0 to V_+,	Switch ON, see Figure 10	25°C	5.5 V	–0.1		0.1	μA
				Full		–1		1	
DIGITAL INPUTS (IN12, IN2)(2)									
V_{IH}	Input logic high			Full		V_+ × 0.7			V
				-40 to 125°C	4.75 V to 5.25 V	3.1			
V_{IL}	Input logic low			Full				V_+ × 0.3	V
I_{IH}, I_{IL}	Input leakage current	V_{IN} = 5.5 V or 0		25°C	5.5 V	–1	0.05	1	μA
				Full		–1		1	
DYNAMIC									
t_{ON}	Turnon time	V_{NC} = GND and V_{NO} = V_+ or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, see Figure 12	Full	4.5 V to 5.5 V	1.7		5.7	ns
				-40 to 125°C	4.75 V to 5.25 V	1.2		8.7	ns
t_{OFF}	Turnoff time	V_{NC} = GND and V_{NO} = V_+ or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, see Figure 12	Full	4.5 V to 5.5 V	0.8		3.8	ns
				-40 to 125°C	4.75 V to 5.25 V	0.5		6.8	ns
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 35 pF, see Figure 13	Full	4.5 V to 5.5 V	0.5			ns
Q_C	Charge injection	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	See Figure 17	25°C	5 V		7		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or V_{NO} = V_+ or GND,	Switch OFF, see Figure 11	25°C	5 V		5.5		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance	V_{NC} or V_{NO} = V_+ or GND,	Switch ON, see Figure 11	25°C	5 V		17.5		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND,	Switch ON, see Figure 11	25°C	5 V		17.5		pF
C_{IN}	Digital input capacitance	V_{IN} = V_+ or GND,	See Figure 11	25°C	5 V		2.8		pF
BW	Bandwidth	R_L = 50 Ω,	Switch ON, see Figure 14	25°C	4.5 V		220		MHz

(1) T_A = 25°C.
(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

Electrical Characteristics for 5-V Supply (continued)

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP[1]	MAX	UNIT
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 10 MHz,	Switch OFF, see Figure 15	25°C	4.5 V		–65		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 10 MHz,	Switch ON, see Figure 16	25°C	4.5 V		–66		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 600 Hz to 20 kHz, see Figure 18	25°C	4.5 V		0.01%		
SUPPLY									
I_+	Positive supply current	V_{IN} = V_+ or GND,	Switch ON or OFF	25°C	5.5 V			1	µA
				Full				10	
ΔI_+	Change in supply current	V_{IN} = V_+ – 0.6 V		Full	5.5 V			500	µA

6.6 Electrical Characteristics for 3.3-V Supply

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_+	V
r_{on}	ON-state resistance	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = –24 mA,	Switch ON, see Figure 9	Full	3 V			18	Ω
				-40 to 125°C				23	
Δr_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 2.1 V, I_{COM} = –24 mA,	Switch ON, see Figure 9	25°C	3 V		0.2		Ω
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = –24 mA,	Switch ON, see Figure 11	25°C	3 V		9		Ω
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO OFF leakage current	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = 0 to V_+,	Switch OFF, see Figure 10	25°C	3.6 V	–1	0.05	1	µA
				Full		–1		1	
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO ON leakage current	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = Open,	Switch ON, see Figure 10	25°C	3.6 V	–0.1		0.1	µA
				Full		–1		1	
$I_{COM(ON)}$	COM ON leakage current	V_{NC} or V_{NO} = Open, V_{COM} = 0 to V_+,	Switch ON, see Figure 10	25°C	3.6 V	–0.1		0.1	µA
				Full		–1		1	
DIGITAL INPUTS (IN12, IN2)(2)									
V_{IH}	Input logic high			Full		V_+ × 0.7			V
V_{IL}	Input logic low			Full				V_+ × 0.3	V
I_{IH}, I_{IL}	Input leakage current	V_{IN} = 5.5 V or 0		25°C	3.6 V	–1	0.05	1	µA
				Full		–1		1	
DYNAMIC									
t_{ON}	Turn-on time	V_{NC} = GND and V_{NO} = V_+ or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, see Figure 12	Full	3 V to 3.6 V	2.5		7.6	ns
				-40 to 125°C		2.0		10.6	ns
t_{OFF}	Turnoff time	V_{NC} = GND and V_{NO} = V_+ or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, see Figure 12	Full	3 V to 3.6 V	1.5		5.3	ns
				-40 to 125°C		1.0		8.3	ns
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 35 pF, see Figure 13	Full	3 V to 3.6 V	0.5			ns
Q_C	Charge injection	R_L = 50 Ω, C_L = 0.1 nF,	see Figure 17	25°C	3.3 V		3		pC
BW	Bandwidth	R_L = 50 Ω, Switch ON,	see Figure 14	25°C	3 V		220		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 10 MHz,	Switch OFF, see Figure 15	25°C	3 V		–65		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 10 MHz,	Switch ON, see Figure 16	25°C	3 V		–66		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 600 Hz to 20 kHz, see Figure 18	25°C	3 V		0.015%		
SUPPLY									
I_+	Positive supply current	V_{IN} = V_+ or GND,	Switch ON or OFF	25°C	3.6 V			1	µA
				Full				10	
ΔI_+	Change in supply current	V_{IN} = V_+ – 0.6 V		Full	3.6 V			500	µA

(1) T_A = 25°C.
(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.7 Electrical Characteristics for 2.5-V Supply

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_+	V
r_{on}	ON-state resistance	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = –8 mA,	Switch ON, see Figure 9	Full	2.3 V			45	Ω
				-40 to 125°C				50	
Δr_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 1.6 V, I_{COM} = –8 mA,	Switch ON, see Figure 9	25°C	2.3 V		0.5		Ω
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = –8 mA,	Switch ON, see Figure 9	25°C	2.3 V		27		Ω
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO OFF leakage current	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = 0 to V_+,	Switch OFF, see Figure 10	25°C	2.7 V	–1	0.05	1	µA
				Full		–1		1	
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO ON leakage current	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = Open,	Switch ON, see Figure 10	25°C	2.7 V	–0.1		0.1	µA
				Full		–1		1	
$I_{COM(ON)}$	COM ON leakage current	V_{NC} or V_{NO} = Open, V_{COM} = 0 to V_+,	Switch ON, see Figure 10	25°C	2.7 V	–0.1		0.1	µA
				Full		–1		1	
DIGITAL INPUTS (IN12, IN2)(2)									
V_{IH}	Input logic high			Full		V_+ × 0.7			V
V_{IL}	Input logic low			Full				V_+ × 0.3	V
I_{IH}, I_{IL}	Input leakage current	V_{IN} = 5.5 V or 0		25°C	2.7 V	–1	0.05	1	µA
				Full		–1		1	
DYNAMIC									
t_{ON}	Turnon time	V_{NC} = GND and V_{NO} = V_+ or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, see Figure 12	Full	2.3 V to 2.7 V	3.5		14	ns
				-40 to 125°C		2.5		17	
t_{OFF}	Turnoff time	V_{NC} = GND and V_{NO} = V_+ or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, see Figure 12	Full	2.3 V to 2.7 V	2		7.5	ns
				-40 to 125°C		1.5		10.5	ns
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 35 pF, see Figure 13	Full	2.3 V to 2.7 V	0.5			ns
BW	Bandwidth	R_L = 50 Ω,	Switch ON, see Figure 14	25°C	2.3 V		220		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 10 MHz,	Switch OFF, see Figure 15	25°C	2.3 V		–65		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 10 MHz,	Switch ON, see Figure 16	25°C	2.3 V		–66		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 600 Hz to 20 kHz, see Figure 18	25°C	2.3 V		0.025%		
SUPPLY									
I_+	Positive supply current	V_{IN} = V_+ or GND,	Switch ON or OFF	25°C	2.7 V			1	µA
				Full				10	
ΔI_+	Change in supply current	V_{IN} = V_+ – 0.6 V		Full	2.7 V			500	µA

(1) T_A = 25°C.
(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.8 Electrical Characteristics for 1.8-V Supply

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_+	V
r_{on}	ON-state resistance	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = –4 mA,	Switch ON, see Figure 9	Full	1.65 V			140	Ω
				-40 to 125°C				180	
Δr_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 1.15 V, I_{COM} = –4 mA,	Switch ON, see Figure 9	25°C	1.65 V		1		Ω
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = –4 mA,	Switch ON, see Figure 9	25°C	1.65 V		110		Ω
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO OFF leakage current	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = 0 to V_+,	Switch OFF, see Figure 10	25°C	1.95 V	–1	0.05	1	µA
				Full		–1		1	
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO ON leakage current	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = Open,	Switch ON, see Figure 10	25°C	1.95 V	–0.1		0.1	µA
				Full		–1		1	
$I_{COM(ON)}$	COM ON leakage current	V_{NC} or V_{NO} = Open, V_{COM} = 0 to V_+,	Switch ON, see Figure 10	25°C	1.95 V	–0.1		0.1	µA
				Full		–1		1	
DIGITAL INPUTS (IN12, IN2)(2)									
V_{IH}	Input logic high			Full		V_+ × 0.75			V
V_{IL}	Input logic low			Full				V_+ × 0.25	V
I_{IH}, I_{IL}	Input leakage current	V_{IN} = 5.5 V or 0		25°C	1.95 V	–1	0.05	1	µA
				Full		–1		1	
DYNAMIC									
t_{ON}	Turnon time	V_{NC} = GND and V_{NO} = V_+ or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, see Figure 12	Full	1.65 V to 1.95 V	7		24	ns
				-40 to 125°C		5.5		27	ns
t_{OFF}	Turnoff time	V_{NC} = GND and V_{NO} = V_+ or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, see Figure 12	Full	1.65 V to 1.95 V	3		13	ns
				-40 to 125°C		2		16	
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 35 pF, see Figure 13	Full	1.65 V to 1.95 V	0.5			ns
BW	Bandwidth	R_L = 50 Ω,	Switch ON, see Figure 14	25°C	1.8 V		220		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 10 MHz,	Switch OFF, see Figure 15	25°C	1.8 V		–60		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 10 MHz,	Switch ON, see Figure 16	25°C	1.8 V		–66		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 600 Hz to 20 kHz, see Figure 18	25°C	1.8 V		0.015%		
SUPPLY									
I_+	Positive supply current	V_{IN} = V_+ or GND,	Switch ON or OFF	25°C	1.95 V			1	µA
				Full				10	
ΔI_+	Change in supply current	V_{IN} = V_+ – 0.6 V		Full	1.95 V			500	µA

(1) T_A = 25°C.
(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.9 Typical Characteristics

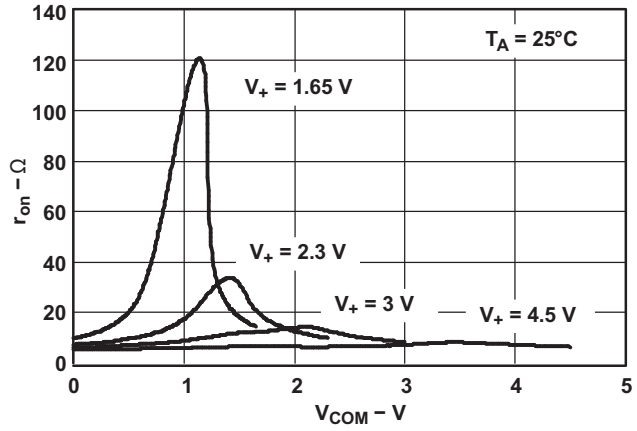


Figure 1. r_{on} vs V_{COM}

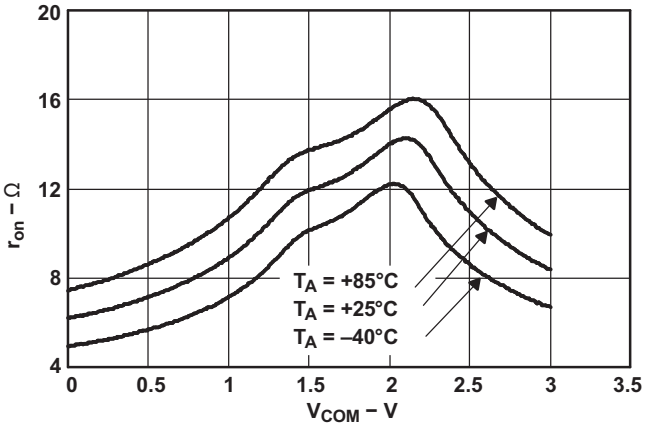


Figure 2. r_{on} vs V_{COM} (V_+ = 3 V)

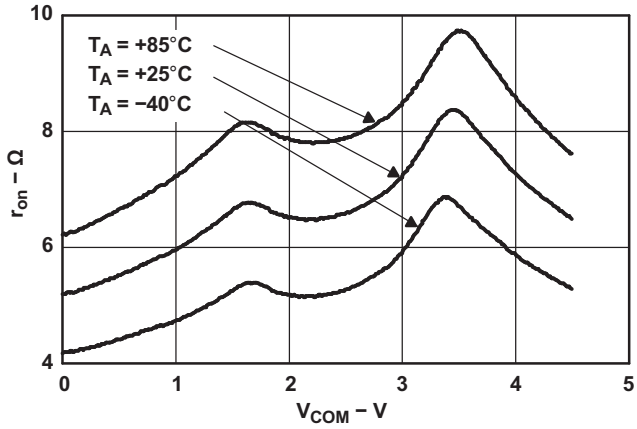


Figure 3. r_{on} vs V_{COM} (V_+ = 5 V)

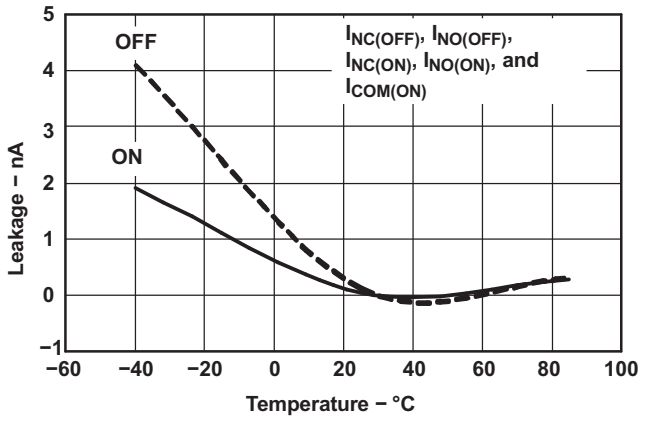


Figure 4. Leakage Current vs Temperature (V_+ = 5.5 V)

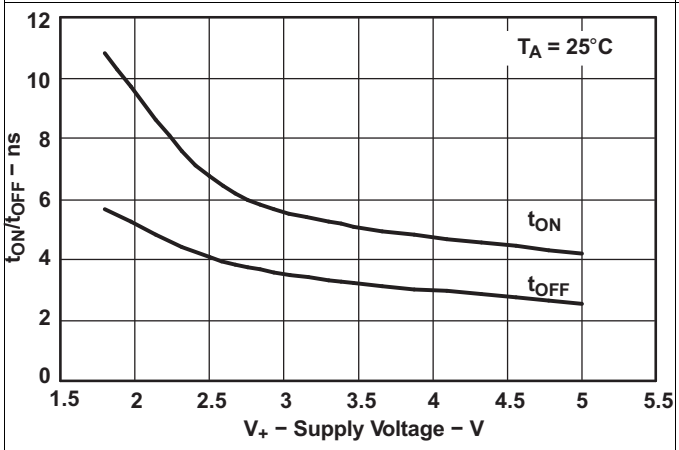


Figure 5. t_{ON} and t_{OFF} vs V_+

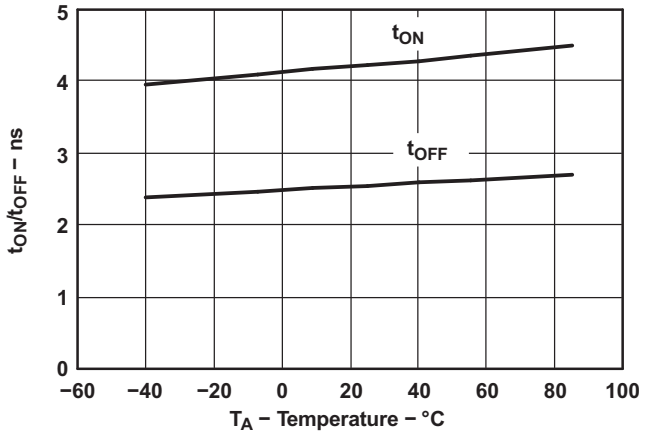


Figure 6. t_{ON} and t_{OFF} vs Temperature (V_+ = 5 V)

Typical Characteristics (continued)

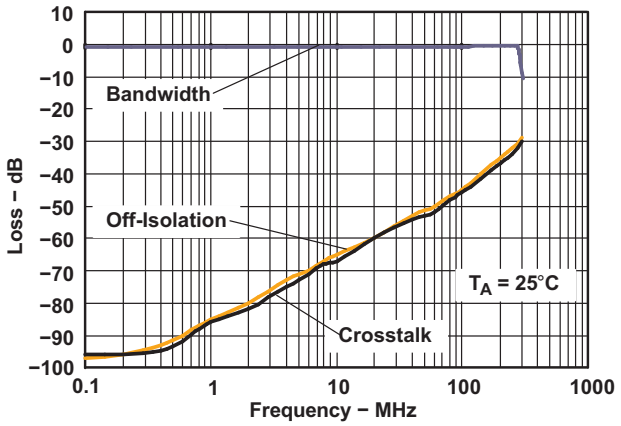


Figure 7. Frequency Response (V_+ = 3 V)

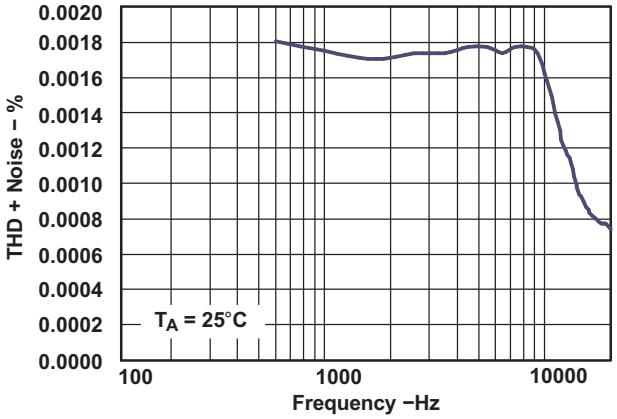


Figure 8. Total Harmonic Distortion (THD) vs Frequency (V_+ = 3 V)

7 Parameter Measurement Information

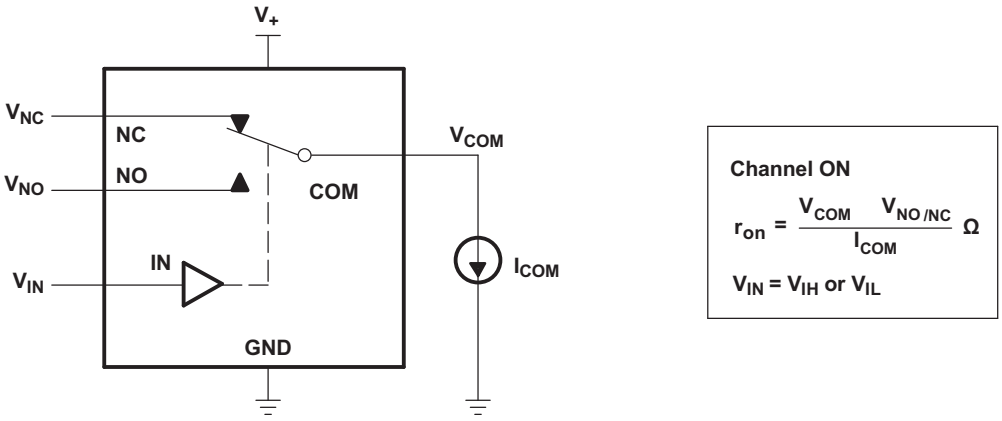


Figure 9. ON-State Resistance (r_{on})

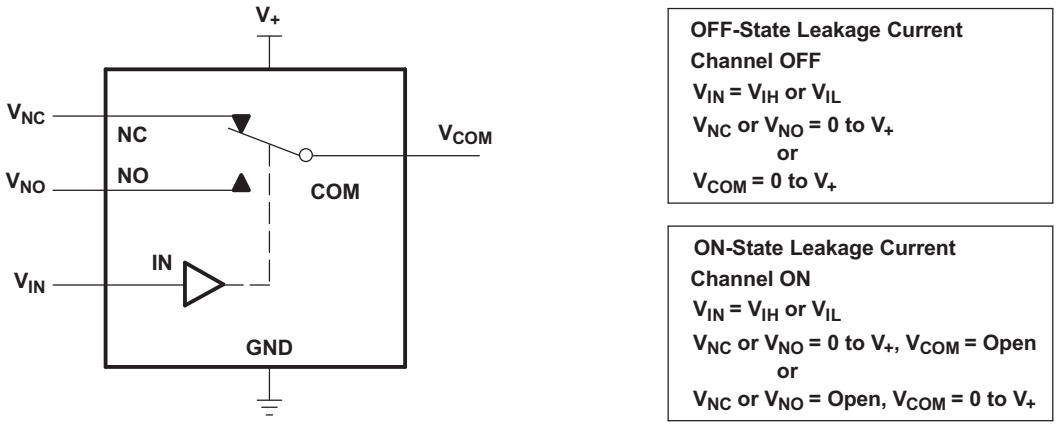


Figure 10. ON- and OFF-State Leakage Current ($I_{COM(ON)}$, $I_{NC(OFF)}$, $I_{NO(OFF)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)

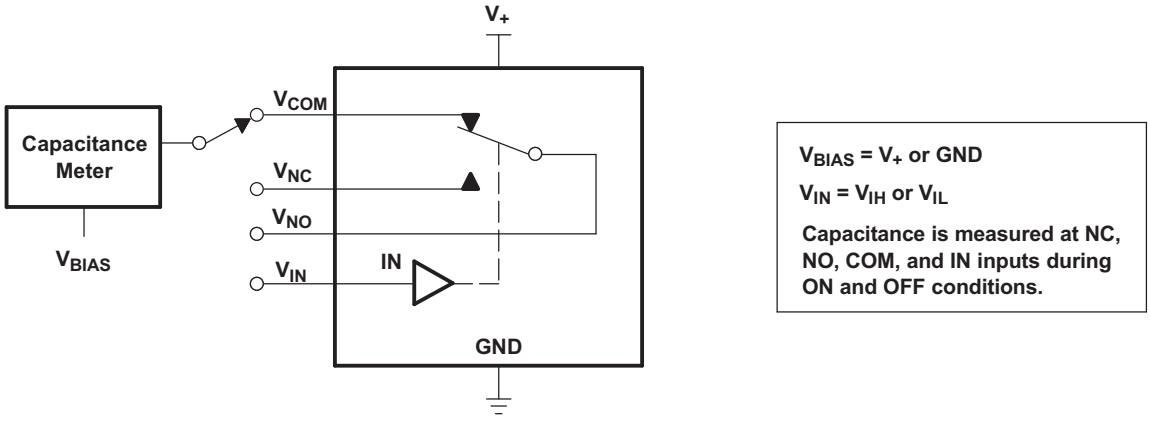
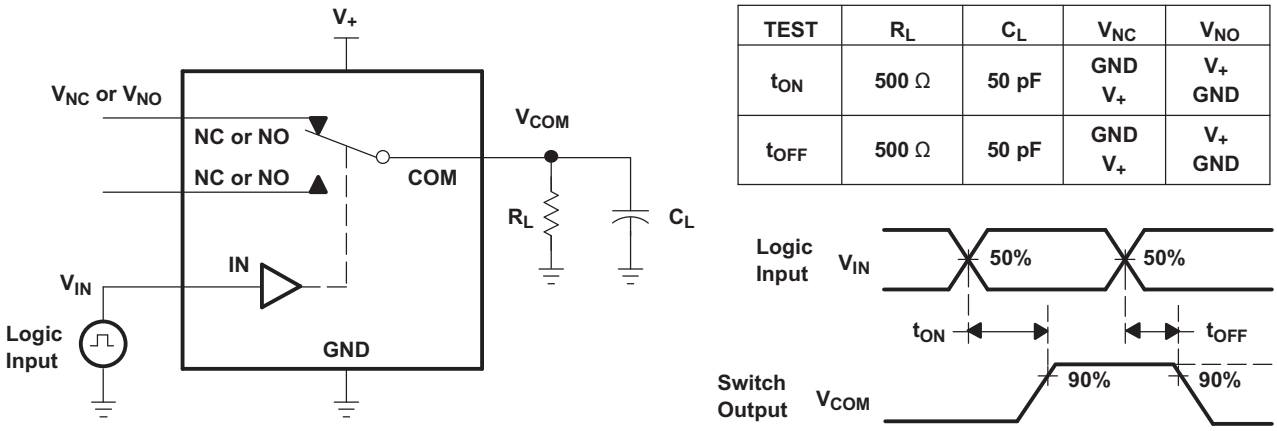


Figure 11. Capacitance (C_{IN}, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)

Parameter Measurement Information (continued)



TEST	R_L	C_L	V_{NC}	V_{NO}
t_{ON}	500 Ω	50 pF	GND V_+	V_+ GND
t_{OFF}	500 Ω	50 pF	GND V_+	V_+ GND

Figure 12. Turnon (t_{ON}) and Turnoff (t_{OFF}) Time

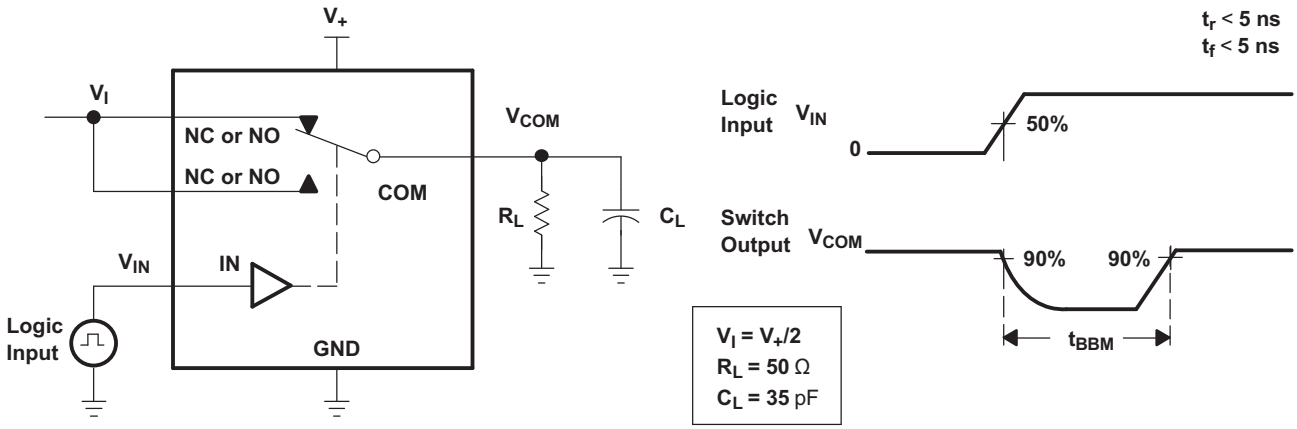


Figure 13. Break-Before-Make (t_{BBM}) Time

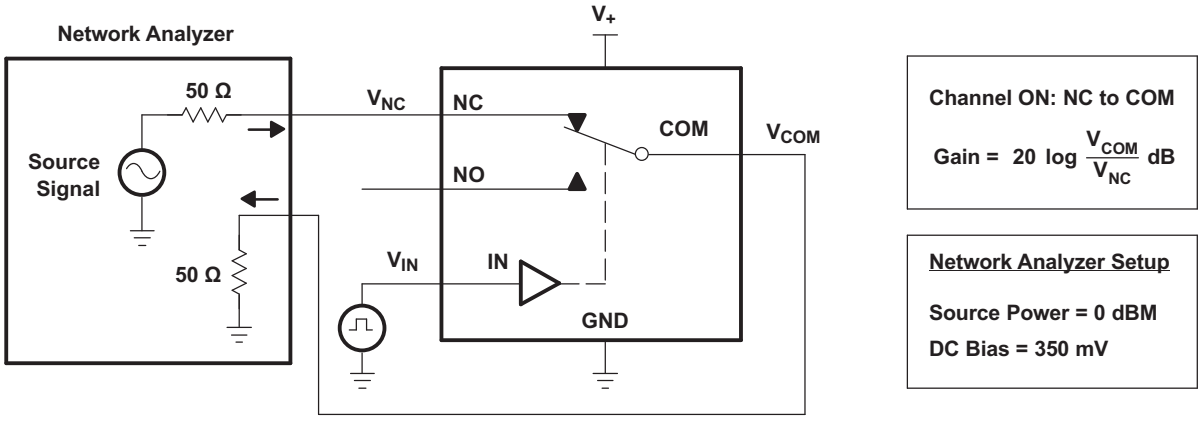


Figure 14. Frequency Response (BW)

Parameter Measurement Information (continued)

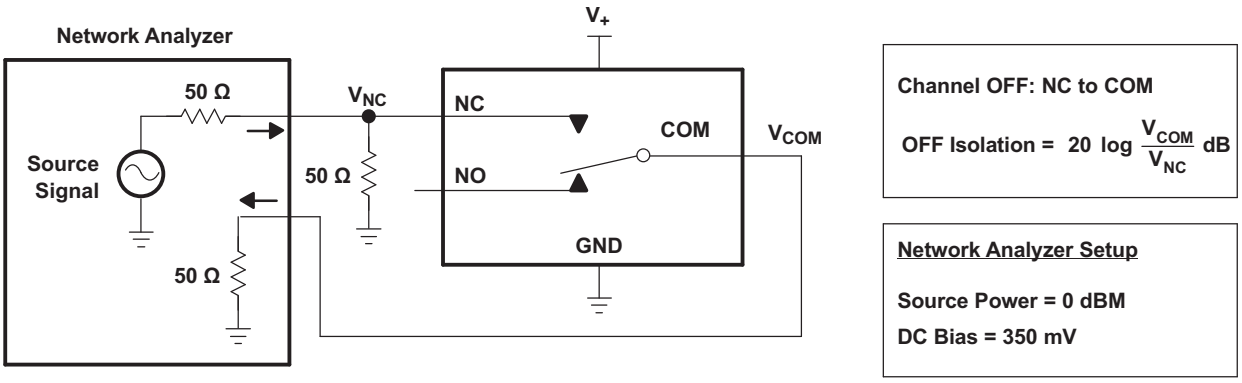


Figure 15. OFF Isolation (O_{ISO})

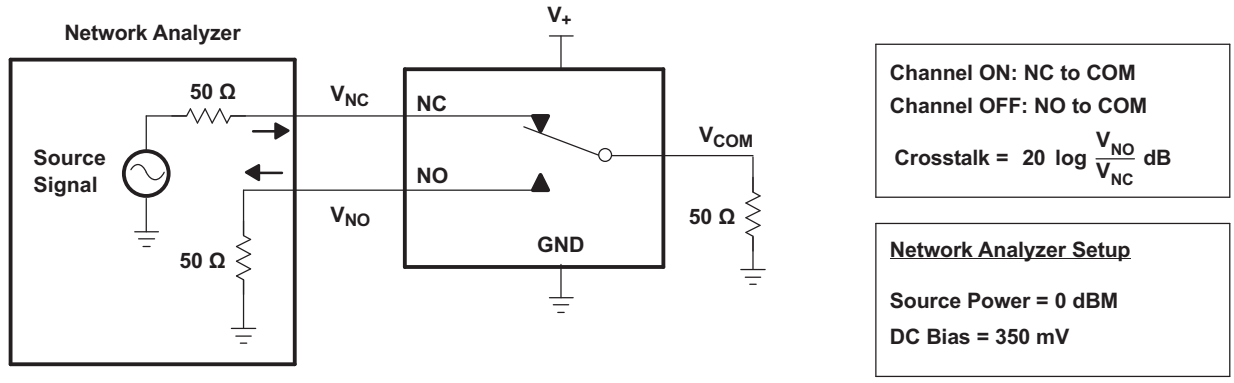


Figure 16. Crosstalk (X_{TALK})

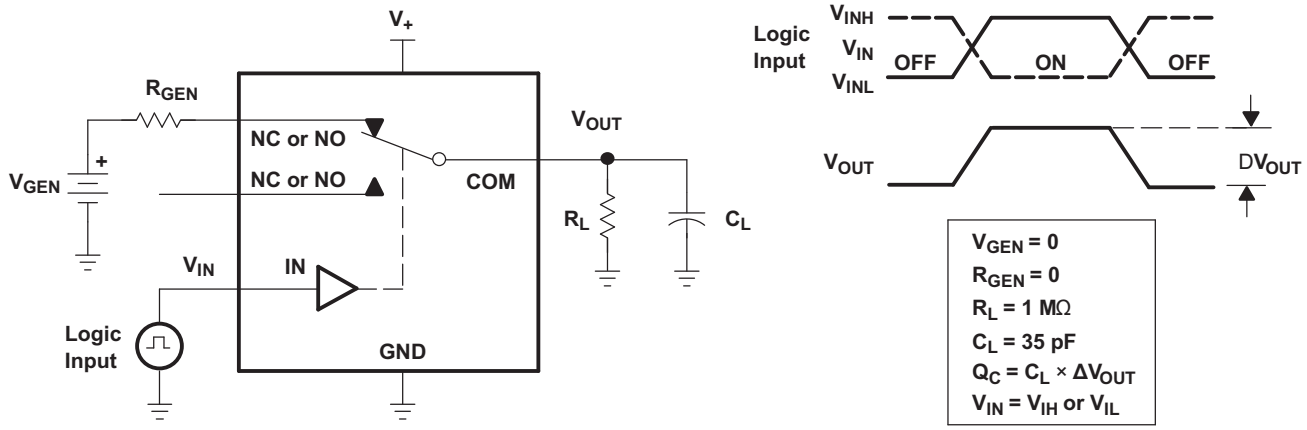


Figure 17. Charge Injection (Q_C)

Parameter Measurement Information (continued)

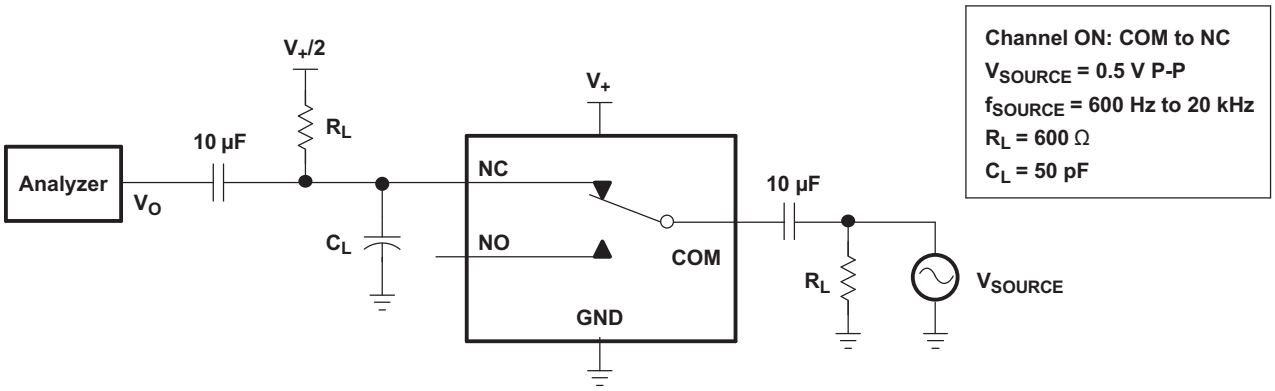


Figure 18. Total Harmonic Distortion (THD)

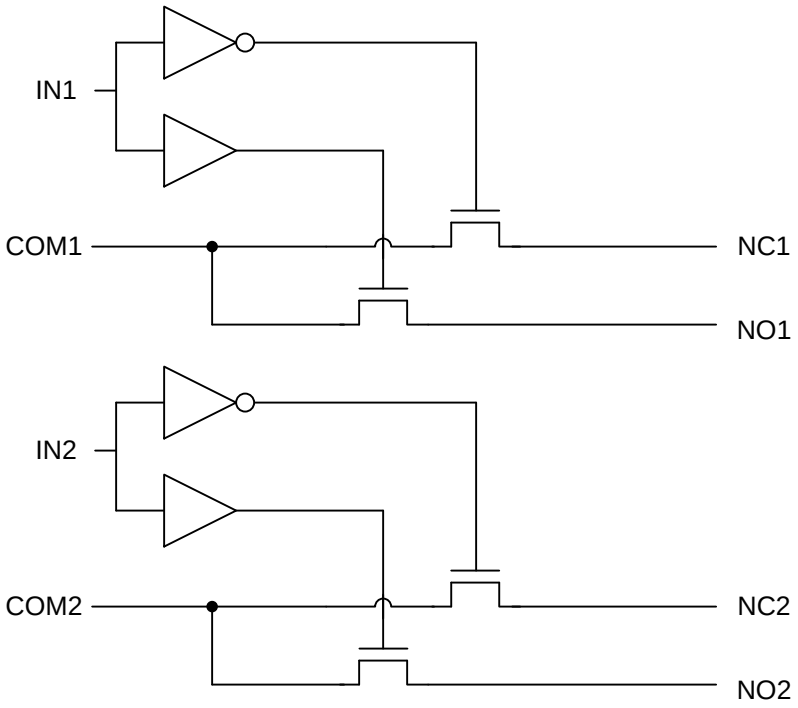
8 Detailed Description

8.1 Overview

The TS5A23157 is a dual single-pole-double-throw (SPDT) solid-state analog switch. The TS5A23157, like all analog switches, is bidirectional. When powered on, each COM pin is connected to its respective NC pin when the IN pin is low. For this device, NC stands for *normally closed* and NO stands for *normally open*. If IN is low, COM is connected to NC. If IN is high, COM is connected to NO.

The TS5A23157 is a break-before-make switch. This means that during switching, a connection is broken before a new connection is established. The NC and NO pins are never connected to each other.

8.2 Functional Block Diagram



8.3 Feature Description

The low ON-state resistance, ON-state resistance matching, and charge injection in the TS5A23157 make this switch an excellent choice for analog signals that require minimal distortion. In addition, the low THD allows audio signals to be preserved more clearly as they pass through the device.

The 1.65-V to 5.5-V operation allows compatibility with more logic levels, and the bidirectional I/Os can pass analog signals from 0 V to V_+ with low distortion. The control inputs are 5-V tolerant, allowing control signals to be present without V_{CC}.

8.4 Device Functional Modes

Table 1 lists the functional modes for TS5A23157.

Table 1. Function Table

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TS5A3157 can be used in a variety of customer systems. The TS5A3157 can be used anywhere multiple analog or digital signals must be selected to pass across a single line.

9.2 Typical Application

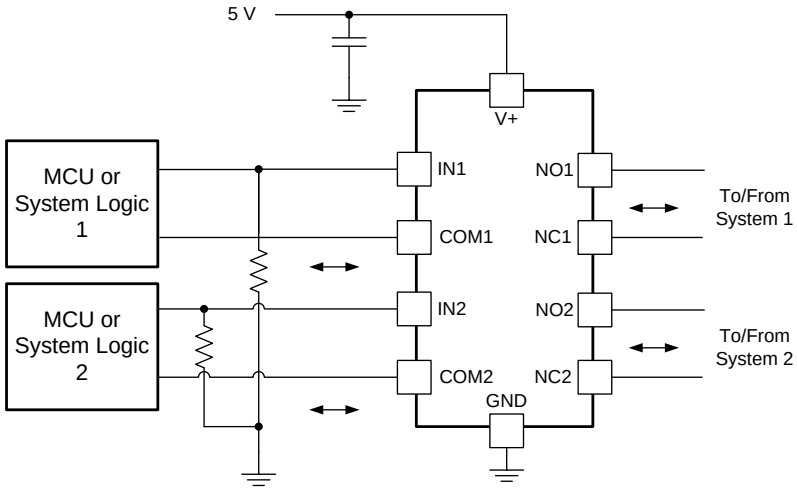


Figure 19. System Schematic for TS5A23157

9.2.1 Design Requirements

In this particular application, V_+ was 5 V, although V_+ is allowed to be any voltage specified in *Recommended Operating Conditions*. A decoupling capacitor is recommended on the V+ pin. See *Power Supply Recommendations* for more details.

9.2.2 Detailed Design Procedure

In this application, IN is, by default, pulled low to GND. Choose the resistor size based on the current driving strength of the GPIO, the desired power consumption, and the switching frequency (if applicable). If the GPIO is open-drain, use pullup resistors instead.

Typical Application (continued)

9.2.3 Application Curve

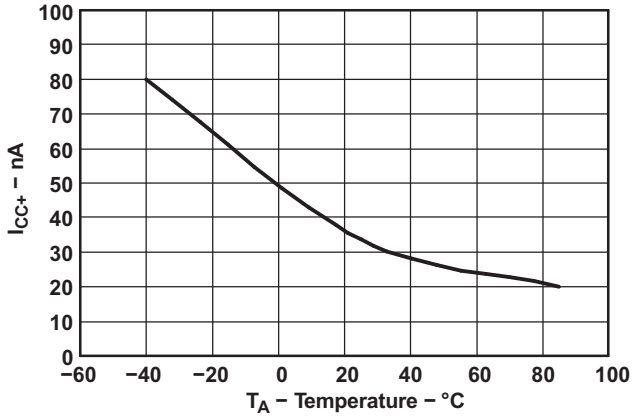


Figure 20. Power-Supply Current vs Temperature (V_+ = 5 V)

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF bypass capacitor is recommended. If there are multiple pins labeled V_{CC}, then a 0.01-µF or 0.022-µF capacitor is recommended for each V_{CC} because the V_{CC} pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-µF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self–inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. Below figure shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

Unused switch I/Os, such as NO, NC, and COM, can be left floating or tied to GND. However, the IN pin must be driven high or low. Due to partial transistor turnon when control inputs are at threshold levels, floating control inputs can cause increased I_{CC} or unknown switch selection states.

11.2 Layout Example

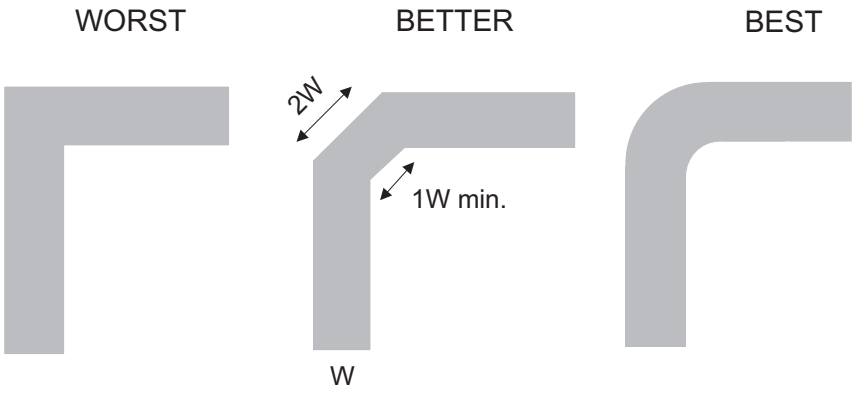


Figure 21. Trace Example

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 デバイスの項目表記

表 2. パラメータの説明

記号	説明
V_{COM}	COM電圧
V_{NC}	NC電圧
V_{NO}	NO電圧
r_{on}	チャネルがオンのときの、COMポートとNCポートの間、またはCOMポートとNOポートの間の抵抗
Δr_{on}	チャネル間のr_{on}の差
$r_{on(flat)}$	規定の条件の範囲における、チャネルのr_{on}の最大値と最小値との差
$I_{NC(OFF)}$	ワーストケースの入力および出力条件で、対応チャネル(NCからCOM)がオフ状態のとき、NCポートで測定されるリーク電流
$I_{NO(OFF)}$	ワーストケースの入力および出力条件で、対応チャネル(NOからCOM)がオフ状態のとき、NOポートで測定されるリーク電流
$I_{NC(ON)}$	対応チャネル(NCからCOM)がオン状態、出力(COM)がオープンのとき、NCポートで測定されるリーク電流
$I_{NO(ON)}$	対応チャネル(NOからCOM)がオン状態、出力(COM)がオープンのとき、NOポートで測定されるリーク電流
$I_{COM(ON)}$	対応チャネル（NOからCOM、またはNCからCOM）がオン状態、出力（NCまたはNO）がオープンのとき、COMポートで測定されるリーク電流
V_{IH}	制御入力(IN)の論理HIGHの最小入力電圧
V_{IL}	制御入力(IN)の論理LOWの最大入力電圧
V_{IN}	INの電圧
I_{IH}、I_{IL}	INで測定されるリーク電流
t_{ON}	スイッチのターンオン時間。このパラメータは、規定された条件の範囲で、スイッチがオンになるときのデジタル制御(IN)信号とアナログ出力(COM/NC/NO)信号との間の伝搬遅延により測定されます。
t_{OFF}	スイッチのターンオフ時間。このパラメータは、規定された条件の範囲で、スイッチがオフになるときのデジタル制御(IN)信号とアナログ出力(COM/NC/NO)信号との間の伝搬遅延により測定されます。
t_{BBM}	Break-Before-Make時間。このパラメータは、規定された条件の範囲で、制御信号の状態が変化するときの2つの隣接するアナログ・チャネル(NCおよびNO)の出力間の伝播遅延により測定されます。
Q_C	電荷注入は、制御(IN)入力からアナログ(NC、NO、COM)出力への、望ましくない信号のカップリングの測定値です。この値はクーロン(C)単位で、制御入力のスイッチングによって誘導される合計電荷により測定されます。電荷注入$Q_C = C_L \times \Delta V_O$。ここで、$C_L$は負荷容量、$\Delta V_O$はアナログ出力電圧の変化です。
$C_{NC(OFF)}$	対応チャネル(NCからCOM)がオフのときのNCポートの容量
$C_{NO(OFF)}$	対応チャネル(NCからCOM)がオフのときのNOポートの容量
$C_{NC(ON)}$	対応チャネル(NCからCOM)がオンのときのNCポートの容量
$C_{NO(ON)}$	対応チャネル(NCからCOM)がオンのときのNOポートの容量
$C_{COM(ON)}$	対応チャネル(COMからNC、またはCOMからNO)がオンのときのCOMポートの容量
C_{IN}	INの容量
O_{ISO}	スイッチのオフ絶縁は、オフ状態のスイッチのインピーダンス測定値です。これは、対応チャネル(NCからCOM、またはNOからCOM)がオフ状態のとき、特定の周波数についてdB単位で測定されます。オフ絶縁$O_{ISO} = 20LOG\ (V_{NC}/V_{COM})$ dB。ここで、V_{COM}は入力、V_{NC}は出力です。
X_{TALK}	クロストークは、オンのチャネルからオフのチャネル(NCからNO、またはNOからNC)への、望ましくない信号カップリングの測定値です。この値は特定の周波数において、dB単位で測定されます。クロストーク$X_{TALK} = 20log\ (V_{NC1}/V_{NO1})$。ここで$V_{NO1}$は入力、$V_{NC1}$は出力です。
BW	スイッチの帯域幅。オン状態のチャネルのゲインがdcゲインより-3dB低くなる周波数です。ゲインは次の式で計測されます。$20log\ (V_{NC}/V_{COM})$ dB。ここで、V_{NC}は出力、V_{COM}は入力です。
I_+	制御(IN)ピンがV_+またはGNDであるときの静的消費電流
ΔI_+	これは、各制御(IN)入力が規定の電圧であるとき（V_+またはGNDではなく）のI_+の増分です。

表 3. 特性の概要

構成	**2:1**マルチプレクサ/デマルチプレクサ **(2 × SPDT)**
チャネル数	2
オン抵抗(r_{on})	10Ω
チャネル間オン抵抗ばらつき(Δr_{on})	0.15Ω
オン抵抗平坦性($r_{on(flat)}$)	4Ω
ターンオン/ターンオフ時間(t_{ON}/t_{OFF})	5.7ns/3.8ns
Break-Before-Make時間(t_{BBM})	0.5ns
電荷注入(Q_C)	7pC
帯域幅(BW)	220MHz
オフ絶縁(O_{ISO})	10MHz時に–65dB
クロストーク(XTALK)	10MHz時に–66dB
全高調波歪み(THD)	0.01%
リーク電流($I_{COM(OFF)}$/$I_{NC(OFF)}$)	±1μA
パッケージ・オプション	10ピンDGSおよびRSE

12.2 ドキュメントのサポート

12.2.1 関連資料

関連資料については、以下を参照してください。

- *『低速またはフローティングCMOS入力の影響』*、SCBA004

12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

12.4 商標

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12.5 静電気放電に関する注意事項

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12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS5A23157DGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(3BR, JBR)
TS5A23157DGSR.B	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(3BR, JBR)
TS5A23157DGSRG4	Active	Production	VSSOP (DGS) | 10	2500 | null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JBR
TS5A23157DGSRG4.B	Active	Production	VSSOP (DGS) | 10	2500 | null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JBR
TS5A23157RSER	Active	Production	UQFN (RSE) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JBO
TS5A23157RSER.B	Active	Production	UQFN (RSE) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JBO
TS5A23157RSERG4.B	Active	Production	UQFN (RSE) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JBO

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TS5A23157 :

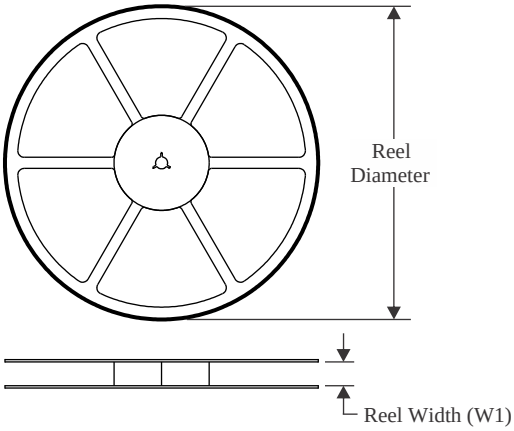
- Automotive : TS5A23157-Q1

NOTE: Qualified Version Definitions:

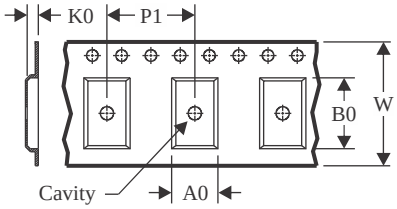
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

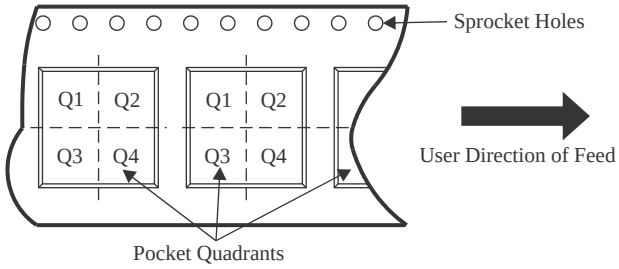


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

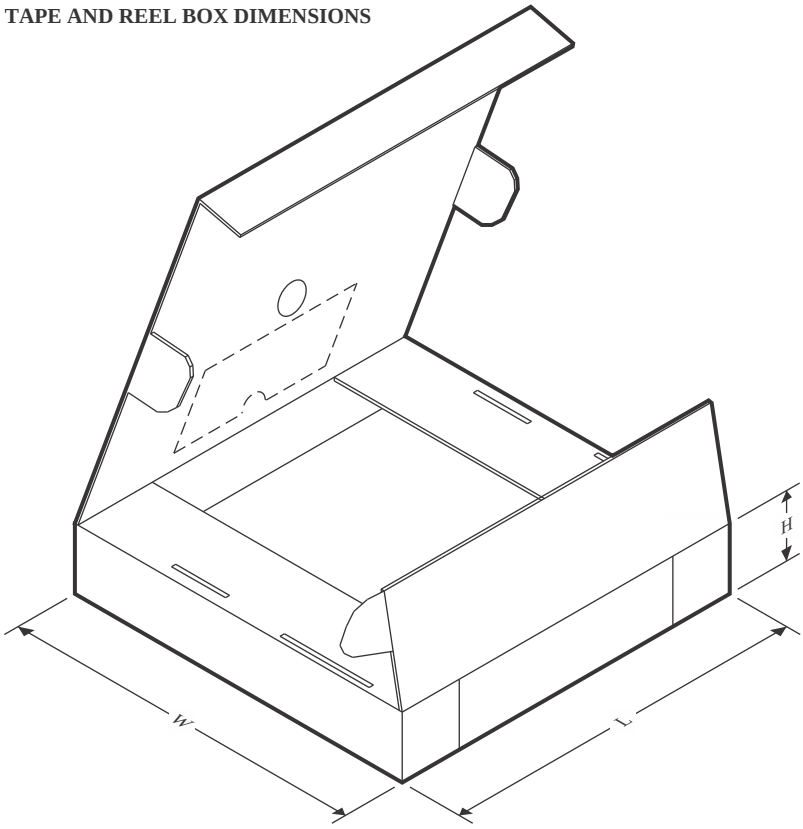
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A23157DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
TS5A23157RSER	UQFN	RSE	10	3000	180.0	9.5	1.7	2.2	0.75	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

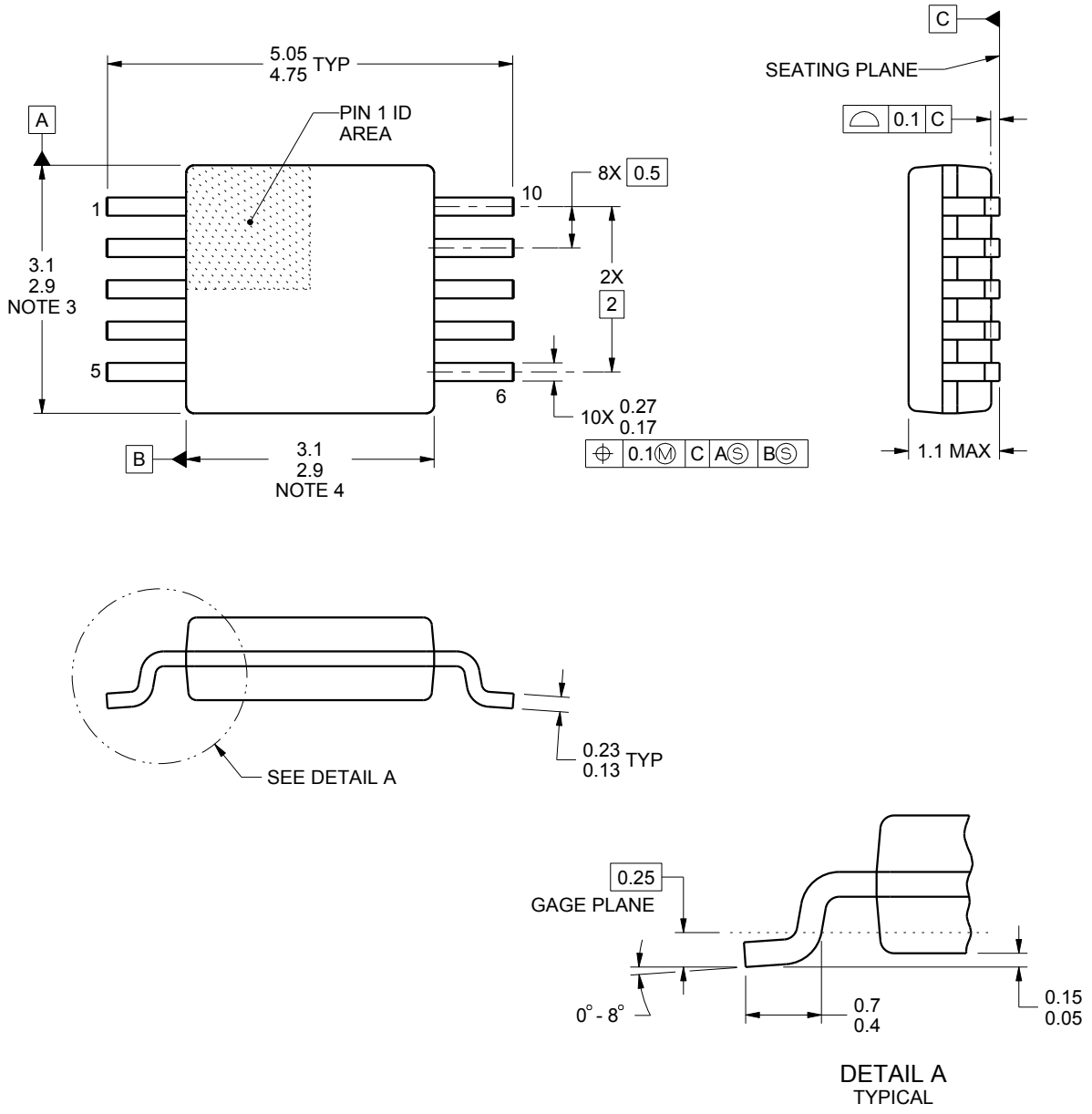
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A23157DGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
TS5A23157RSER	UQFN	RSE	10	3000	189.0	185.0	36.0

PACKAGE OUTLINE

DGS0010A

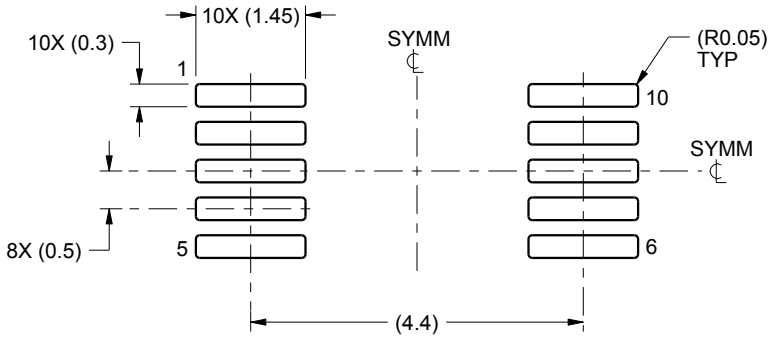
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

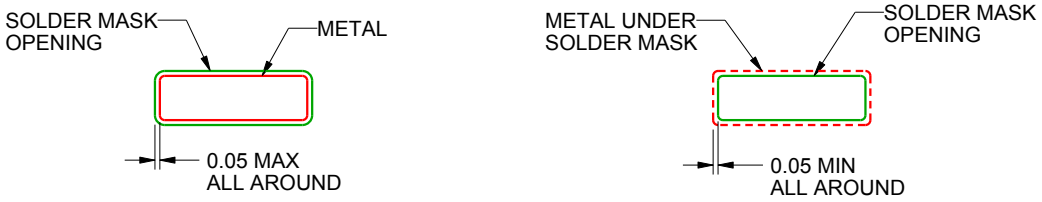


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

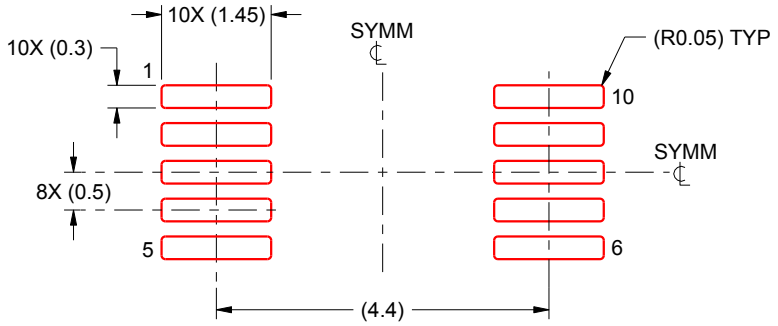


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

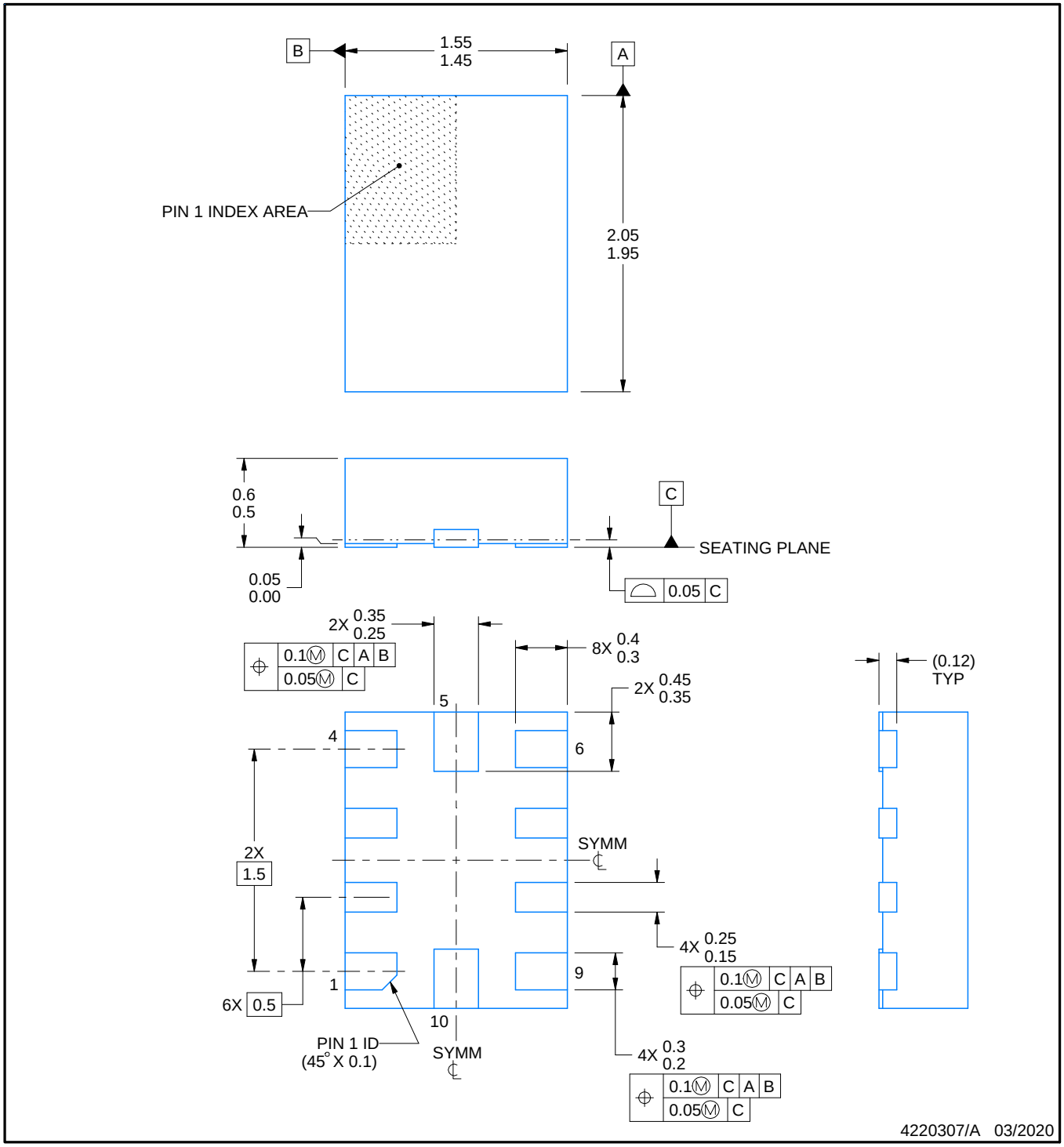
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RSE0010A

PACKAGE OUTLINE

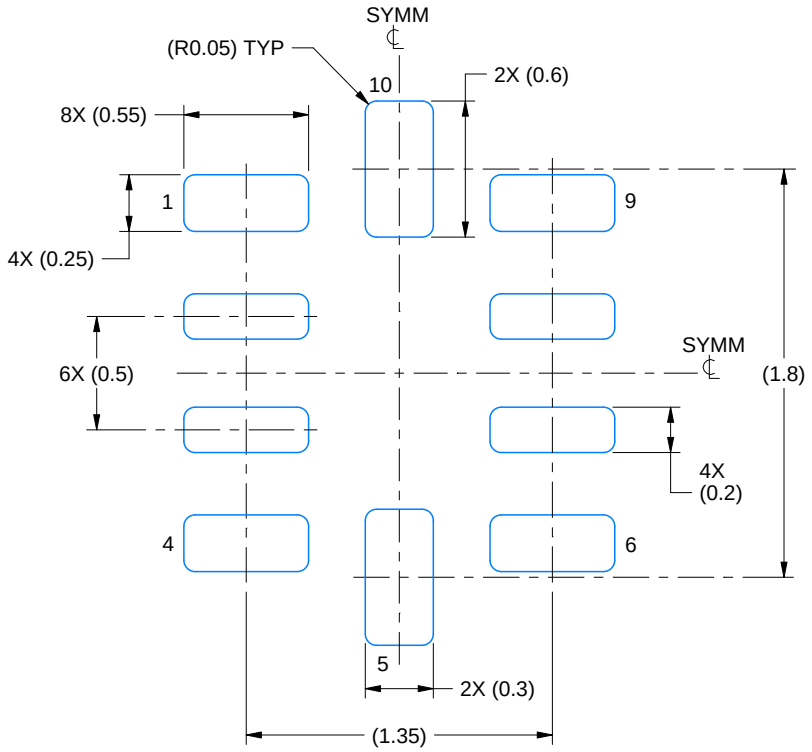
UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

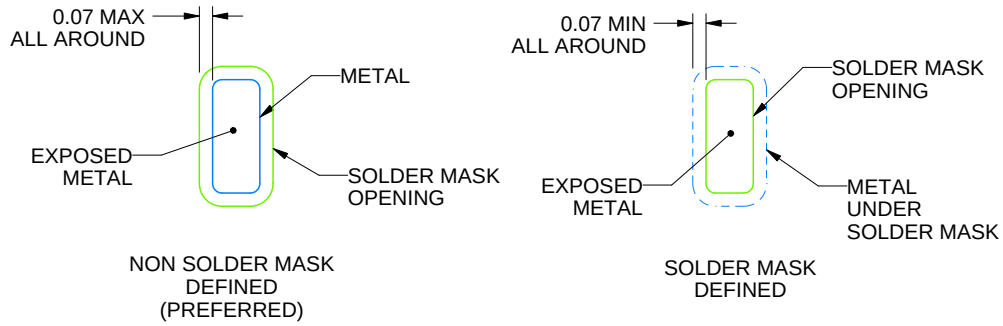


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X

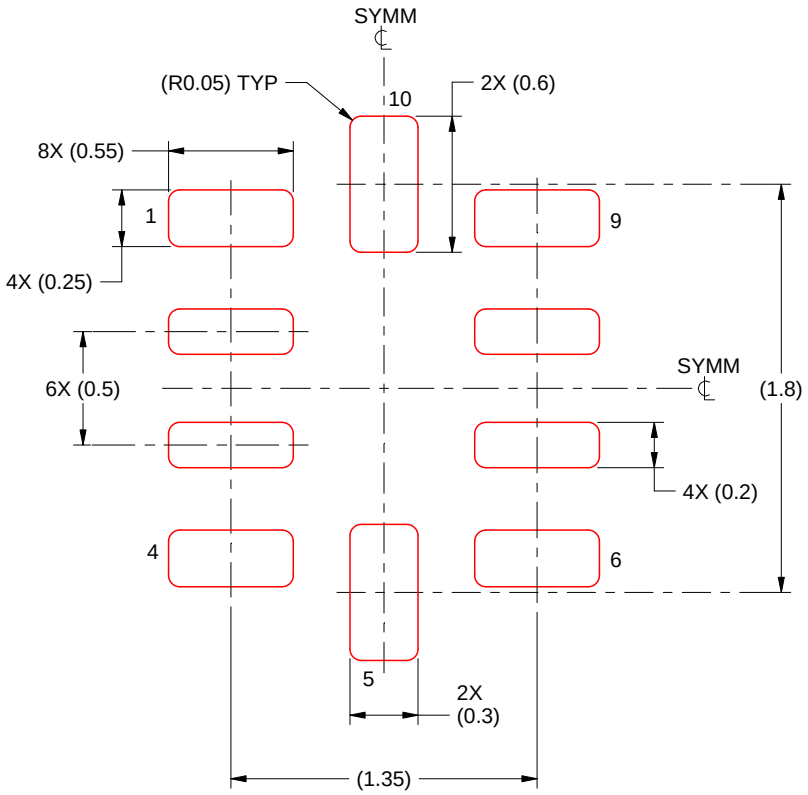


SOLDER MASK DETAILS
NOT TO SCALE

4220307/A 03/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE: 30X

4220307/A 03/2020

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月