

FEATURES

- Overshoot and Undershoot Voltage Protection
- Specified Break-Before-Make Switching
- Low ON-State Resistance (10 Ω)
- Control Inputs Are 5-V Tolerant
- Low Charge Injection
- Excellent ON-Resistance Matching
- Low Total Harmonic Distortion (THD)
- 1.8-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
 - 300-V Machine Model (A115-A)

APPLICATIONS

- Sample-and-Hold Circuit
- Battery-Powered Equipments
- Audio and Video Signal Routing
- Communication Circuits

DESCRIPTION/ORDERING INFORMATION

The TS5A623157 is a dual single-pole, double-throw (SPDT) analog switch designed to operate from 1.65 V to 5.5 V. This device can handle both digital and analog signals. Signals up to V+ (peak) can be transmitted in either direction.

The TS5A623157 senses overshoot and undershoot events at the I/Os and responds by preventing voltage differentials from developing and turning the switch on.

ORDERING INFORMATION

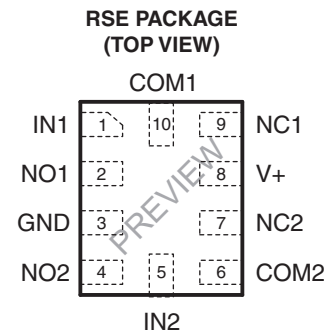
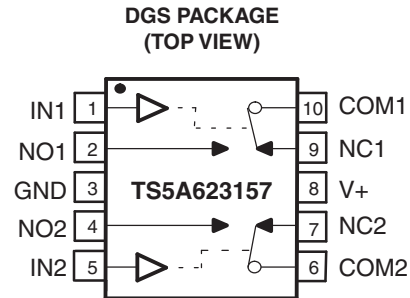
T _A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	VSSOP (MSOP-10) – DGS	Tape and reel	TS5A623157DGSR	35R
	QFN – RSE	Tape and reel	TS5A623157RSER	PREVIEW

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

FUNCTION TABLE

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TS5A623157
DUAL 10-Ω SPDT ANALOG SWITCH
WITH UNDERSHOOT/OVERSHOOT VOLTAGE PROTECTION

SCDS253–SEPTEMBER 2007

SUMMARY OF CHARACTERISTICS
 $V_+ = 5\text{ V}$, $T_A = 25^\circ\text{C}$

Configuration	2:1 multiplexer/demultiplexer (1 × SPDT)
Number of channels	2
ON-state resistance (r_{on})	10 Ω
ON-state resistance match (Δr_{on})	0.15 Ω
ON-state resistance flatness ($r_{on(flat)}$)	2 Ω
Turn-on/turn-off time (t_{ON}/t_{OFF})	5 ns / 3.4 ns
Break-before-make time (t_{BBM})	0.5 ns
Charge injection (Q_C)	5 pC
Bandwidth (BW)	371 MHz
OFF isolation (O_{ISO})	-61 dB at 10 MHz
Crosstalk (X_{TALK})	-61 dB at 10 MHz
Total harmonic distortion (THD)	0.06%
Leakage current ($I_{NO(OFF)}/I_{NC(OFF)}$)	±1 μA
Power-supply current (I_+)	1.2 μA
Undershoot protection	-2 V
Overshoot protection	$V_+ + 2\text{ V}$
Package options	10-pin VSSOP (DGS), 10-pin QFN (RSE)

Absolute Minimum and Maximum Ratings⁽¹⁾⁽²⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_+	Supply voltage range ⁽³⁾	-0.5	6.5	V
V_{NC} V_{NO} V_{COM}	Analog voltage range ⁽³⁾⁽⁴⁾⁽⁵⁾	-0.5	$V_+ + 0.5$	V
$I_{I/OK}$	Analog port diode current	$V_+ < V_{NC}, V_{NO}, V_{COM} < 0$		±50 mA
I_{NC} I_{NO} I_{COM}	On-state switch current	$V_{NC}, V_{NO}, V_{COM} = 0 \text{ to } V_+$		±50 mA
V_{IN}	Digital input voltage range ⁽³⁾⁽⁴⁾	-0.5	6.5	V
I_{IK}	Digital input clamp current	$V_I < 0$		-50 mA
I_+ I_{GND}	Continuous current through V_+ or GND			±100 mA
T_{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (5) This value is limited to 5.5 V maximum.

Package Thermal Impedance

			UNIT
θ_{JA}	Package thermal impedance ⁽¹⁾	DGS package	165
		RSE package	243

- (1) The package thermal impedance is calculated in accordance with JESD 51-7.

PRODUCT PREVIEW

Electrical Characteristics for 5-V Supply
 $V_+ = 4.5 \text{ V to } 5.5 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT		
Analog Switch										
Analog signal range	V_{COM}, V_{NO}, V_{NC}				0		V_+	V		
Voltage undershoot	V_{IKU}	$0 \geq (I_{NC}, I_{NO}, \text{ or } I_{COM}) \geq -50 \text{ mA}$		5.5 V			-2	V		
Peak ON-state resistance	r_{peak}	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$, $I_{COM} = -30 \text{ mA}$, Switch ON, See Figure 14	25°C	4.5 V		4.6	11	Ω		
			Full						13	
ON-state resistance	r_{on}	$V_{NO} \text{ or } V_{NC} = 0$, $I_{COM} = 30 \text{ mA}$	25°C	4.5 V		4	6.5	Ω		
			Full						8	
			25°C						4	8
			Full							
			25°C						5.5	10
			Full							
ON-state resistance match between channels	Δr_{on}	$V_{NO} \text{ or } V_{NC} = 3.15 \text{ V}$, $I_{COM} = -30 \text{ mA}$, Switch ON, See Figure 14	25°C	4.5 V		0.1	0.14	Ω		
			Full						0.15	
ON-state resistance flatness	$r_{on(Flat)}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$, $I_{COM} = -30 \text{ mA}$, Switch ON, See Figure 14	25°C	4.5 V		1.5	2	Ω		
			Full						4	
NC, NO OFF leakage current	$I_{NC(OFF)}, I_{NO(OFF)}$	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } V_+$, $V_{COM} = V_+ \text{ to } 0$, Switch OFF, See Figure 15	25°C	5.5 V		1	20	nA		
			Full						150	
NC, NO ON leakage current	$I_{NC(ON)}, I_{NO(ON)}$	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } V_+$, $V_{COM} = \text{Open}$, Switch ON, See Figure 16	25°C	5.5 V		1	20	nA		
			Full						150	
COM ON leakage current	$I_{COM(ON)}$	$V_{NC} \text{ or } V_{NO} = \text{Open}$, $V_{COM} = 0 \text{ to } V_+$, Switch ON, See Figure 16	25°C	5.5 V		1	20	nA		
			Full						150	
Digital Control Input (IN)										
Input logic high	V_{IH}		Full		$V_+ \times 0.7$		5.5	V		
Input logic low	V_{IL}		Full		0		$V_+ \times 0.3$	V		
Input leakage current	I_{IH}, I_{IL}	$V_I = 5.5 \text{ V or } 0$	25°C	5.5 V		0.1	10	nA		
			Full						30	

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Electrical Characteristics for 5-V Supply (continued)

$V_+ = 4.5\text{ V to }5.5\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT	
Dynamic									
Turn-on time	t_{ON}	$V_{COM} = V_+$ or GND, $R_L = 500\ \Omega$,	$C_L = 50\text{ pF}$, See Figure 17	25°C	5 V	1	3.5	5	ns
				Full	4.5 V to 5.5 V	1		6	
Turn-off time	t_{OFF}	$V_{COM} = V_+$ or GND, $R_L = 500\ \Omega$,	$C_L = 50\text{ pF}$, See Figure 17	25°C	5 V	1	2.8	3.4	ns
				Full	4.5 V to 5.5 V	1		3.8	
Output voltage during undershoot	V_{OUTU}	See Figure 24			2.5	$V_{OH} - 0.3$		V	
Output voltage during overshoot	V_{OUTO}	See Figure 24				$V_{OL} + 0.3$	2	V	
Break-before-make time	t_{BBM}	$V_{NC} = V_{NO} = V_+/2$, $R_L = 50\ \Omega$,	$C_L = 50\text{ pF}$, See Figure 18	25°C	5 V	0.5	5	12	ns
				Full	4.5 V to 5.5 V	0.5		14	
Charge injection	Q_C	$V_{GEN} = 0$, $R_{GEN} = 0$,	$C_L = 0.1\text{ nF}$, See Figure 22	25°C	5 V		110	pC	
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	5 V		5	pF	
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch ON,	See Figure 16	25°C	5 V		14.5	pF	
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 16	25°C	5 V		14.5	pF	
Digital input capacitance	C_I	$V_I = V_+$ or GND,	See Figure 16	25°C	5 V		3.5	pF	
Bandwidth	BW	$R_L = 50\ \Omega$, Switch ON,	See Figure 19	25°C	5 V		371	MHz	
OFF isolation	O_{ISO}	$R_L = 50\ \Omega$, $f = 10\text{ MHz}$,	Switch OFF, See Figure 20	25°C	5 V		-61	dB	
Crosstalk	X_{TALK}	$R_L = 50\ \Omega$, $f = 10\text{ MHz}$,	Switch ON, See Figure 21	25°C	5 V		-61	dB	
Total harmonic distortion	THD	$R_L = 600\ \Omega$, $C_L = 50\text{ pF}$,	$f = 20\text{ Hz to }20\text{ kHz}$, See Figure 23	25°C	5 V		0.06	%	
Supply									
Positive supply current	I_+	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	5.5 V	0.01	0.15	μA	
				Full			1.2		

PRODUCT PREVIEW

Electrical Characteristics for 3.3-V Supply

$V_+ = 3\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT	
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}				0		V_+	V	
Voltage undershoot	V_{IKU}	$0 \geq (I_{NC}, I_{NO}, \text{ or } I_{COM}) \geq -50\text{ mA}$		3.6 V				V	
Peak ON-state resistance	r_{peak}	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$, $I_{COM} = -24\text{ mA}$, Switch ON, See Figure 14	25°C	3 V		8.9	14	Ω	
			Full				18		
ON-state resistance	r_{on}	$V_{NO} \text{ or } V_{NC} = 0$, $I_{COM} = 24\text{ mA}$ Switch ON, See Figure 14	25°C	3 V		5.4	8	Ω	
			Full				10		
			25°C				7.4		12
			Full				15		
ON-state resistance match between channels	Δr_{on}	$V_{NO} \text{ or } V_{NC} = 2.1\text{ V}$, $I_{COM} = -24\text{ mA}$, Switch ON, See Figure 14	25°C	3 V		0.1	0.2	Ω	
			Full				0.2		
ON-state resistance flatness	$r_{on(Flat)}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$, $I_{COM} = -24\text{ mA}$, Switch ON, See Figure 14	25°C	3 V		2.8	4	Ω	
			Full				7		
NC, NO OFF leakage current	$I_{NC(OFF)}, I_{NO(OFF)}$	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } V_+$, $V_{COM} = V_+ \text{ to } 0$, Switch OFF, See Figure 15	25°C	3.6 V		0.5	10	nA	
			Full				100		
NC, NO ON leakage current	$I_{NC(ON)}, I_{NO(ON)}$	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } V_+$, $V_{COM} = \text{Open}$, Switch ON, See Figure 16	25°C	3.6 V		0.5	10	nA	
			Full				100		
COM ON leakage current	$I_{COM(ON)}$	$V_{NC} \text{ or } V_{NO} = \text{Open}$, $V_{COM} = 0 \text{ to } V_+$, Switch ON, See Figure 16	25°C	3.6 V		0.5	10	nA	
			Full				100		
Digital Control Input (IN)									
Input logic high	V_{IH}		Full		$V_+ \times 0.7$		5.5	V	
Input logic low	V_{IL}		Full		0		$V_+ \times 0.3$	V	
Input leakage current	I_{IH}, I_{IL}	$V_I = 5.5\text{ V or }0$	25°C	3.6 V		0.1	10	nA	
			Full				20		

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Electrical Characteristics for 3.3-V Supply (continued)

$V_+ = 3\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT	
Dynamic									
Turn-on time	t_{ON}	$V_{COM} = V_+$ or GND, $R_L = 500\ \Omega$,	$C_L = 50\text{ pF}$, See Figure 17	25°C	3.3 V	1	4.7	9.0	ns
				Full	3 V to 3.6 V	1		10.0	
Turn-off time	t_{OFF}	$V_{COM} = V_+$ or GND, $R_L = 500\ \Omega$,	$C_L = 50\text{ pF}$, See Figure 17	25°C	3.3 V	1	3.2	6.3	ns
				Full	3 V to 3.6 V	1		7.0	
Output voltage during undershoot	V_{OUTU}	See Figure 24			2.5	$V_{OH} - 0.3$		V	
Output voltage during overshoot	V_{OUTO}	See Figure 24				$V_{OL} + 0.3$	2	V	
Break-before-make time	t_{BBM}	$V_{NC} = V_{NO} = V_+/2$, $R_L = 50\ \Omega$,	$C_L = 50\text{ pF}$, See Figure 18	25°C	3.3 V	0.5	7	17	ns
				Full	3 V to 3.6 V	0.5		19.5	
Charge injection	Q_C	$V_{GEN} = 0$, $R_{GEN} = 0$,	$C_L = 0.1\text{ nF}$, See Figure 22	25°C	3.3 V		75	pC	
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	3.3 V		5	pF	
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch ON,	See Figure 16	25°C	3.3 V		14.5	pF	
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 16	25°C	3.3 V		14.5	pF	
Digital input capacitance	C_I	$V_I = V_+$ or GND,	See Figure 16	25°C	3.3 V		3.5	pF	
Bandwidth	BW	$R_L = 50\ \Omega$, Switch ON,	See Figure 19	25°C	3.3 V		370	MHz	
OFF isolation	O_{ISO}	$R_L = 50\ \Omega$, $f = 10\text{ MHz}$,	Switch OFF, See Figure 20	25°C	3.3 V		-60	dB	
Crosstalk	X_{TALK}	$R_L = 50\ \Omega$, $f = 10\text{ MHz}$,	Switch ON, See Figure 21	25°C	3.3 V		-60	dB	
Total harmonic distortion	THD	$R_L = 600\ \Omega$, $C_L = 50\text{ pF}$,	$f = 20\text{ Hz to }20\text{ kHz}$, See Figure 23	25°C	3.3 V		0.1	%	
Supply									
Positive supply current	I_+	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	3.6 V		0.05	0.5	μA
				Full				0.75	

PRODUCT PREVIEW

Electrical Characteristics for 2.5-V Supply
 $V_+ = 2.3 \text{ V to } 2.7 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT	
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}				0		V_+	V	
Voltage undershoot	V_{IKU}	$0 \text{ mA} \geq (I_{NC}, I_{NO}, \text{ or } I_{COM}) \geq -50 \text{ mA}$		2.7 V				V	
Peak ON-state resistance	r_{peak}	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$, $I_{COM} = -8 \text{ mA}$, Switch ON, See Figure 14	25°C	2.3 V		13.9	30	Ω	
			Full						35
ON-state resistance	r_{on}	$V_{NO} \text{ or } V_{NC} = 0$, $I_{COM} = 8 \text{ mA}$ Switch ON, See Figure 14	25°C	2.3 V		6.6	8.5	Ω	
			Full						12
			25°C						8.9
			Full						25
ON-state resistance match between channels	Δr_{on}	$V_{NO} \text{ or } V_{NC} = 1.6 \text{ V}$, $I_{COM} = -8 \text{ mA}$, Switch ON, See Figure 14	25°C	2.3 V		0.05	0.3	Ω	
			Full						0.5
ON-state resistance flatness	$r_{on(Flat)}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$, $I_{COM} = -8 \text{ mA}$, Switch ON, See Figure 14	25°C	2.3 V		5	15	Ω	
			Full						20
NC, NO OFF leakage current	$I_{NC(OFF)}, I_{NO(OFF)}$	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } V_+$, $V_{COM} = V_+ \text{ to } 0$, Switch OFF, See Figure 15	25°C	2.7 V		0.1	10	nA	
			Full						100
NC, NO ON leakage current	$I_{NC(ON)}, I_{NO(ON)}$	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } V_+$, $V_{COM} = \text{Open}$, Switch ON, See Figure 16	25°C	2.7 V		0.1	10	nA	
			Full						10
COM ON leakage current	$I_{COM(ON)}$	$V_{NC} \text{ or } V_{NO} = \text{Open}$, $V_{COM} = 0 \text{ to } V_+$, Switch ON, See Figure 16	25°C	2.7 V		0.1	10	nA	
			Full						100
Digital Control Input (IN)									
Input logic high	V_{IH}		Full		$V_+ \times 0.75$		5.5	V	
Input logic low	V_{IL}		Full		0		$V_+ \times 0.25$	V	
Input leakage current	I_{IH}, I_{IL}	$V_I = 5.5 \text{ V or } 0$	25°C	2.7 V		5	10	nA	
			Full						20

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Electrical Characteristics for 2.5-V Supply (continued)

$V_+ = 2.3 \text{ V to } 2.7 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic								
Turn-on time	t_{ON}	$V_{COM} = V_+$ or GND, $R_L = 500 \Omega$, $C_L = 50 \text{ pF}$, See Figure 17	25°C	2.5 V	2	6.2	9.6	ns
			Full	2.3 V to 2.7 V	2		12	
Turn-off time	t_{OFF}	$V_{COM} = V_+$ or GND, $R_L = 500 \Omega$, $C_L = 50 \text{ pF}$, See Figure 17	25°C	2.5 V	1.5	4.5	7.0	ns
			Full	2.3 V to 2.7 V	1.5		7.5	
Output voltage during undershoot	V_{OUTU}	See Figure 24			$V_{OH} - 0.3$			V
Output voltage during overshoot	V_{OUTO}	See Figure 24			$V_{OL} + 0.3$			2 V
Break-before-make time	t_{BBM}	$V_{NC} = V_{NO} = V_+/2$, $R_L = 50 \Omega$, $C_L = 50 \text{ pF}$, See Figure 18	25°C	2.5 V	0.5	10	25	ns
			Full	2.3 V to 2.7 V	0.5		28.5	
Charge injection	Q_C	$V_{GEN} = 0$, $R_{GEN} = 0$, $C_L = 0.1 \text{ nF}$, See Figure 22	25°C	2.5 V	58			pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch OFF, See Figure 16	25°C	2.5 V	5			pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch ON, See Figure 16	25°C	2.5 V	14.5			pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON, See Figure 16	25°C	2.5 V	14.5			pF
Digital input capacitance	C_I	$V_I = V_+$ or GND, See Figure 16	25°C	2.5 V	3.5			pF
Bandwidth	BW	$R_L = 50 \Omega$, Switch ON, See Figure 19	25°C	2.5 V	367			MHz
OFF isolation	O_{ISO}	$R_L = 50 \Omega$, $f = 10 \text{ MHz}$, Switch OFF, See Figure 20	25°C	2.5 V	-60			dB
Crosstalk	X_{TALK}	$R_L = 50 \Omega$, $f = 10 \text{ MHz}$, Switch ON, See Figure 21	25°C	2.5 V	-60			dB
Total harmonic distortion	THD	$R_L = 600 \Omega$, $C_L = 50 \text{ pF}$, $f = 20 \text{ Hz to } 20 \text{ kHz}$, See Figure 23	25°C	2.5 V	0.15			%
Supply								
Positive supply current	I_+	$V_I = V_+$ or GND, Switch ON or OFF	25°C	2.7 V	50			nA
			Full		100 550			

PRODUCT PREVIEW

Electrical Characteristics for 1.8-V Supply

$V_+ = 1.65\text{ V to }1.95\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT	
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}				0		V_+	V	
Voltage undershoot	V_{IKU}	$0 \geq (I_{NC}, I_{NO}, \text{ or } I_{COM}) \geq -50\text{ mA}$		1.95 V				V	
Peak ON-state resistance	r_{peak}	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$, $I_{COM} = -4\text{ mA}$, Switch ON, See Figure 14	25°C	1.65 V		41.1	60	Ω	
			Full				120		
ON-state resistance	r_{on}	$V_{NO} \text{ or } V_{NC} = 0$, $I_{COM} = 4\text{ mA}$, Switch ON, See Figure 14	25°C	1.65 V		9.2	15	Ω	
			Full				15		
			25°C				1.8		40
			Full				45		
ON-state resistance match between channels	Δr_{on}	$V_{NO} \text{ or } V_{NC} = 1.15\text{ V}$, $I_{COM} = -4\text{ mA}$, Switch ON, See Figure 14	25°C	1.65 V		0.1	0.6	Ω	
			Full				0.8		
ON-state resistance flatness	$r_{on(Flat)}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$, $I_{COM} = -4\text{ mA}$, Switch ON, See Figure 14	25°C	1.65 V		26.5	80	Ω	
			Full				100		
NC, NO OFF leakage current	$I_{NC(OFF)}, I_{NO(OFF)}$	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } V_+$, $V_{COM} = V_+ \text{ to } 0$, Switch OFF, See Figure 15	25°C	1.95 V		0.05	10	nA	
			Full				100		
NC, NO ON leakage current	$I_{NC(ON)}, I_{NO(ON)}$	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } V_+$, $V_{COM} = \text{Open}$, Switch ON, See Figure 16	25°C	1.95 V		0.1	10	μA	
			Full				100		
COM ON leakage current	$I_{COM(ON)}$	$V_{NC} \text{ or } V_{NO} = \text{Open}$, $V_{COM} = 0 \text{ to } V_+$, Switch ON, See Figure 16	25°C	1.95 V		0.1	10	nA	
			Full				100		
Digital Control Input (IN)									
Input logic high	V_{IH}		Full		$V_+ \times 0.75$		5.5	V	
Input logic low	V_{IL}		Full		0		$V_+ \times 0.25$	V	
Input leakage current	I_{IH}, I_{IL}	$V_I = 5.5\text{ V or }0$	25°C	1.95 V		0.05	1	nA	
			Full				20		

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Electrical Characteristics for 1.8-V Supply (continued)

$V_+ = 1.65\text{ V to }1.95\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic								
Turn-on time	t_{ON}	$V_{COM} = V_+$ or GND, $R_L = 500\ \Omega$, $C_L = 50\text{ pF}$, See Figure 17	25°C	1.8 V	9.6	23	ns	
			Full	1.65 V to 1.95 V		24		
Turn-off time	t_{OFF}	$V_{COM} = V_+$ or GND, $R_L = 500\ \Omega$, $C_L = 50\text{ pF}$, See Figure 17	25°C	1.8 V	6.3	10	ns	
			Full	1.65 V to 1.95 V		12		
Output voltage during undershoot	V_{OUTU}	See Figure 24			$V_{OH} - 0.3$		V	
Output voltage during overshoot	V_{OUTO}	See Figure 24			$V_{OL} + 0.3$		V	
Break-before-make time	t_{BBM}	$V_{NC} = V_{NO} = V_+/2$, $R_L = 50\ \Omega$, $C_L = 50\text{ pF}$, See Figure 18	25°C	1.8 V	0.5	18	50	ns
			Full	1.65 V to 1.95 V	0.5	55		
Charge injection	Q_C	$V_{GEN} = 0$, $R_{GEN} = 0$, $C_L = 0.1\text{ nF}$, See Figure 22	25°C	1.8 V	40		pC	
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch OFF, See Figure 16	25°C	1.8 V	5.0		pF	
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch ON, See Figure 16	25°C	1.8 V	14.5		pF	
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON, See Figure 16	25°C	1.8 V	14.5		pF	
Digital input capacitance	C_I	$V_I = V_+$ or GND, See Figure 16	25°C	1.8 V	3.5		pF	
Bandwidth	BW	$R_L = 50\ \Omega$, Switch ON, See Figure 19	25°C	1.8 V	369		MHz	
OFF isolation	O_{ISO}	$R_L = 50\ \Omega$, $f = 10\text{ MHz}$, Switch OFF, See Figure 20	25°C	1.8 V	-60		dB	
Crosstalk	X_{TALK}	$R_L = 50\ \Omega$, $f = 10\text{ MHz}$, Switch ON, See Figure 21	25°C	1.8 V	-60		dB	
Total harmonic distortion	THD	$R_L = 600\ \Omega$, $C_L = 50\text{ pF}$, $f = 20\text{ Hz to }20\text{ kHz}$, See Figure 23	25°C	1.8 V	0.4		%	
Supply								
Positive supply current	I_+	$V_I = V_+$ or GND, Switch ON or OFF	25°C	1.95 V	0.1	50	nA	
			Full		400			

PRODUCT PREVIEW

PIN DESCRIPTION

PIN NO.	NAME	DESCRIPTION
1	IN1	Digital control to connect COM to NO or NC
2	NO1	Normally open
3	GND	Digital ground
4	NO2	Normally open
5	IN2	Digital control to connect COM to NO or NC
6	COM2	Common
7	NC2	Normally closed
8	V+	Power supply
9	NC1	Normally closed
10	COM1	Common

PARAMETER DESCRIPTION

SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NC}	Voltage at NC
V_{NO}	Voltage at NO
r_{on}	Resistance between COM and NC or COM and NO ports when the channel is ON
Δr_{on}	Difference of r_{on} between channels
$r_{on(flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NC(OFF)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state under worst-case input and output conditions
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state under worst-case input and output conditions
$I_{NC(ON)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) being open
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) being open
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (NO to COM or NC to COM) in the ON state and the output (NC or NO) being open
V_{IH}	Minimum input voltage for logic high for the control input (IN)
V_{IL}	Minimum input voltage for logic low for the control input (IN)
V_{IN}	Voltage at control input (IN)
I_{IH}, I_{IL}	Leakage current measured at control input (IN)
t_{ON}	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog outputs (COM/NC/NO) signal when the switch is turning ON.
t_{OFF}	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog outputs (COM/NC/NO) signal when the switch is turning OFF.
t_{BBM}	Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC, NO, or COM) output. This is measured in coulombs (=) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_O$, C_L is the load capacitance and ΔV_O is the change in analog output voltage.
$C_{NC(OFF)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NC to COM) is OFF
$C_{NC(ON)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NC to COM) is ON
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON
C_1	Capacitance of control input (IN)
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state.

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PARAMETER DESCRIPTION (continued)

SYMBOL	DESCRIPTION
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured at a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency where the gain of an ON channel is –3 dB below the dc gain.
THD	Total harmonic distortion is defined as the ratio of the root mean square (RMS) value of the second, third, and higher harmonics to the magnitude of fundamental harmonic.
I+	Static power-supply current with the control (IN) pin at V+ or GND
V_{OUTU}	Output voltage during an undershoot event. This is measured by turning off a specific channel and applying an undershoot voltage at the input of the switch.
V_{OUTO}	Output voltage during an overshoot event. This is measured by turning off a specific channel and applying an overshoot voltage at the input of the switch.

TYPICAL CHARACTERISTICS

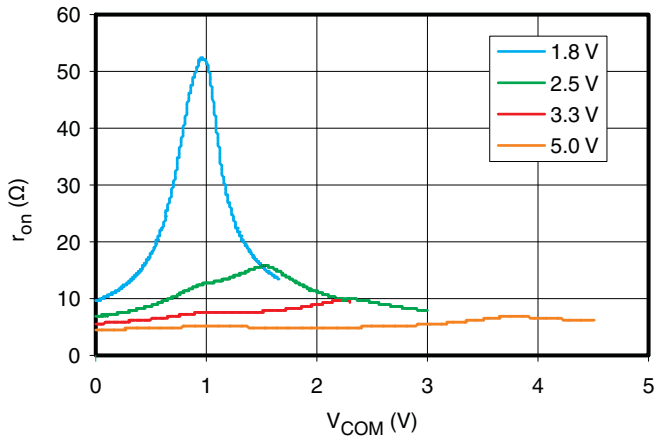


Figure 1. r_{ON} vs V_{COM}

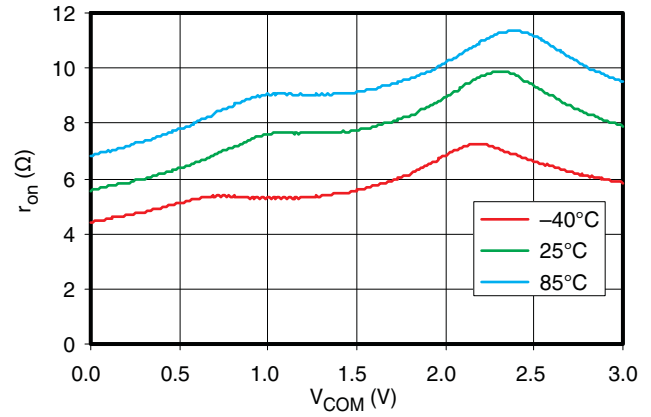


Figure 2. r_{ON} vs V_{COM} ($V_+ = 3.3$ V)

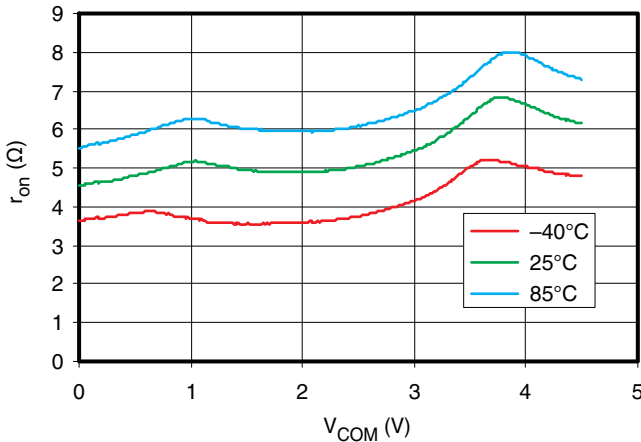


Figure 3. r_{ON} vs V_{COM} ($V_+ = 5$ V)

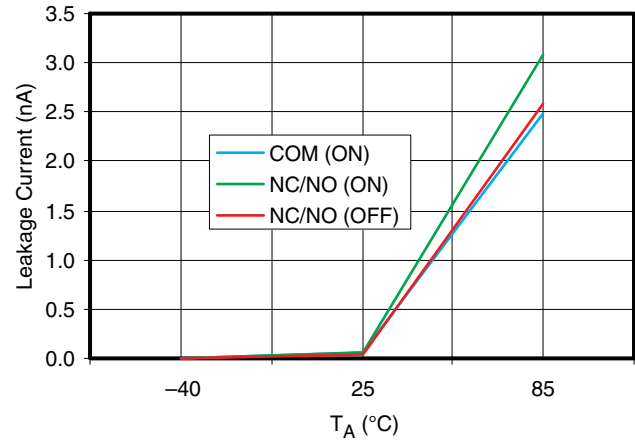


Figure 4. Leakage Current vs Temperature

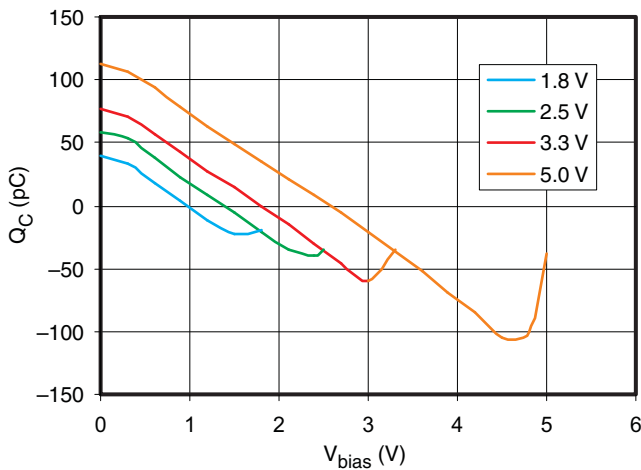


Figure 5. Charge Injection vs V_{COM}

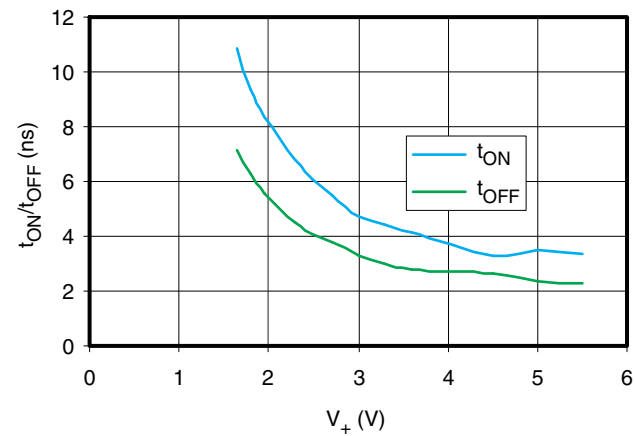


Figure 6. t_{ON} and t_{OFF} vs Supply Voltage

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS (continued)

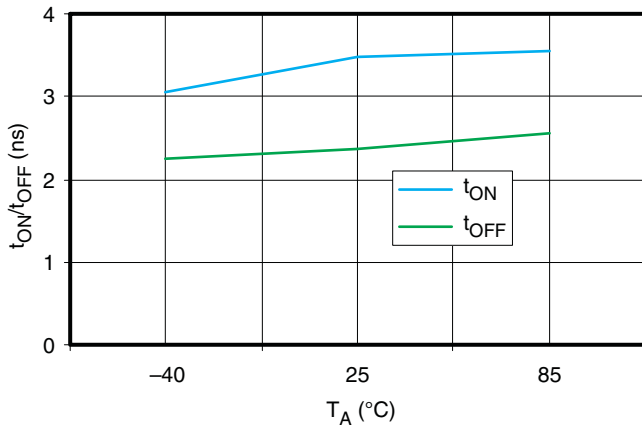


Figure 7. t_{ON} and t_{OFF} vs Temperature

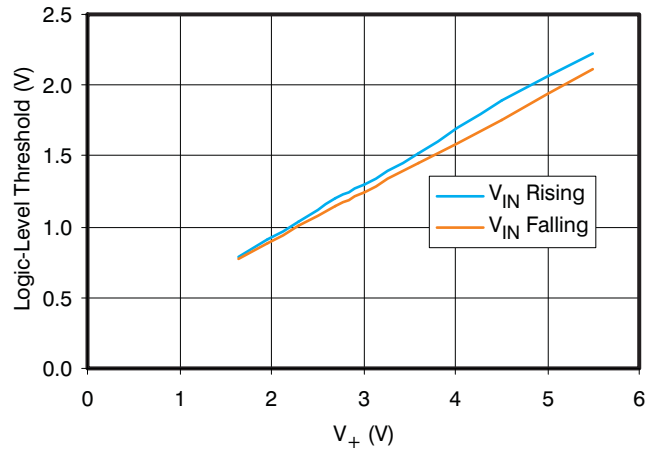


Figure 8. Logic-Level Threshold

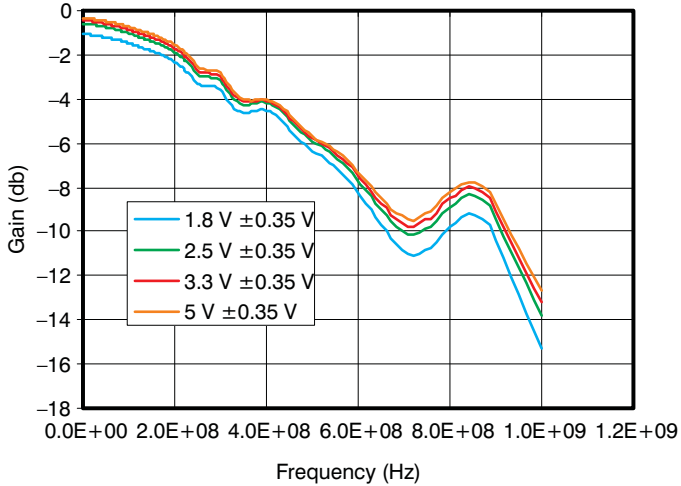


Figure 9. Bandwidth (BW)

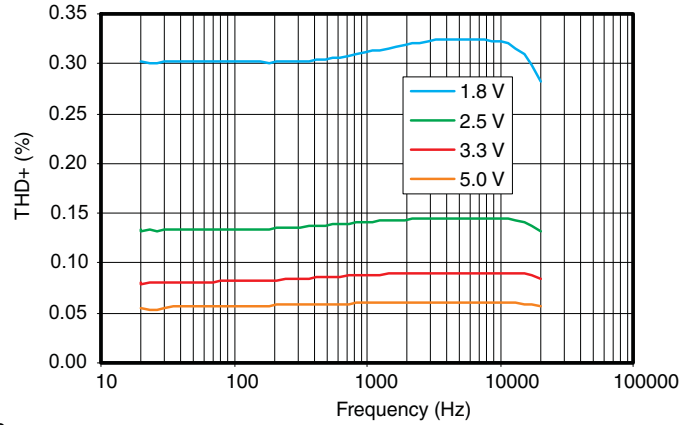


Figure 10. Total Harmonic Distortion (THD) vs Frequency

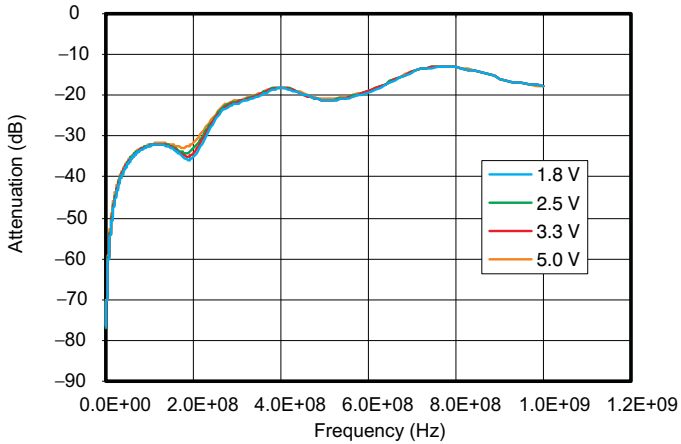


Figure 11. Off Isolation

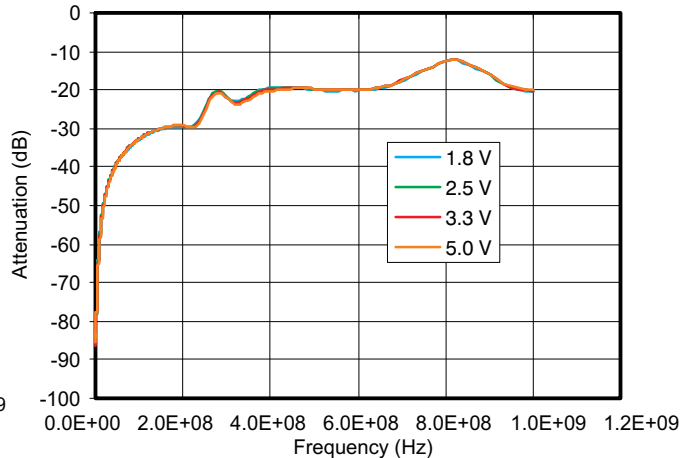


Figure 12. Crosstalk

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS (continued)

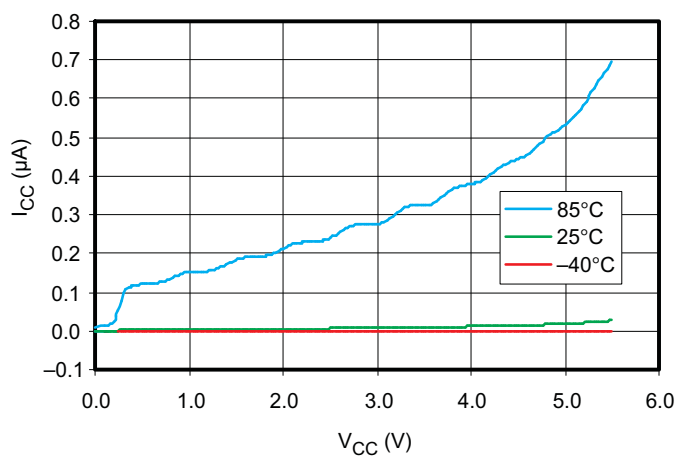


Figure 13. Supply Current vs Supply Voltage

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

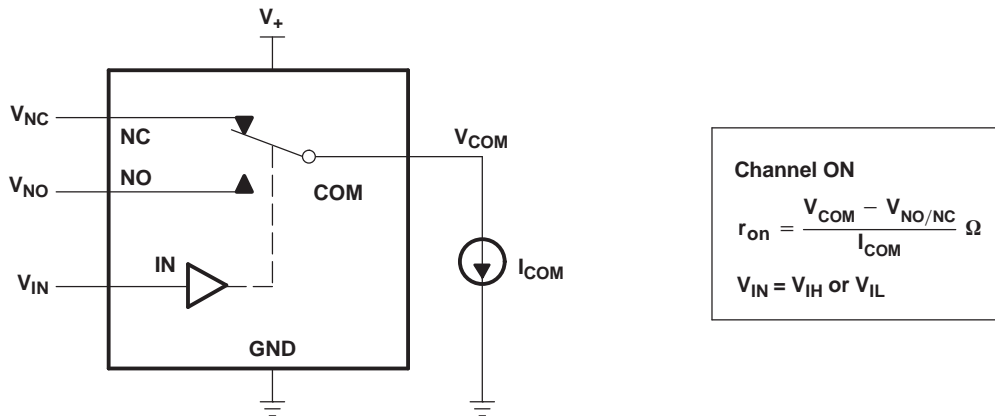


Figure 14. ON-State Resistance (r_{on})

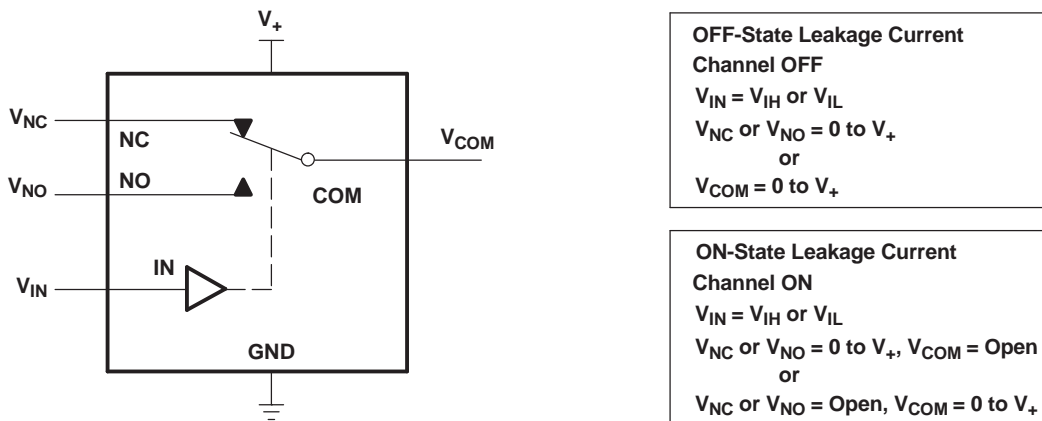


Figure 15. ON- and OFF-State Leakage Current ($I_{COM(ON)}$, $I_{NC(OFF)}$, $I_{NO(OFF)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)

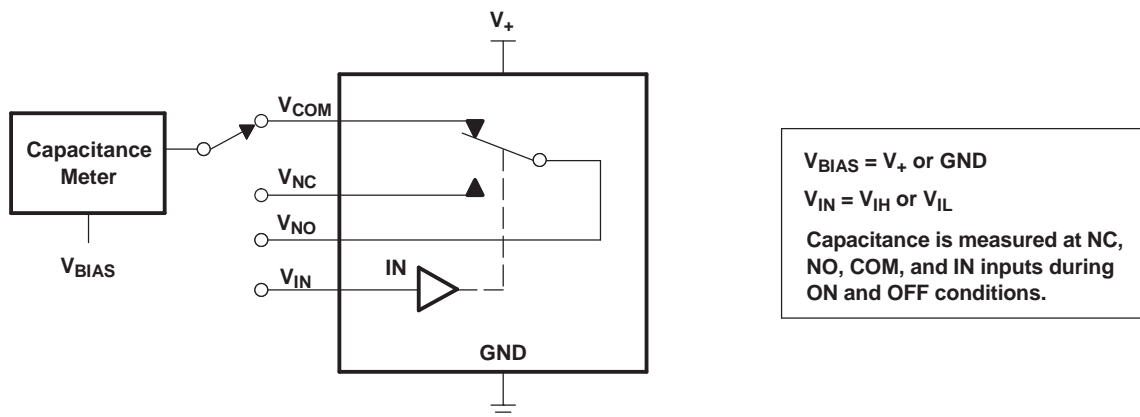
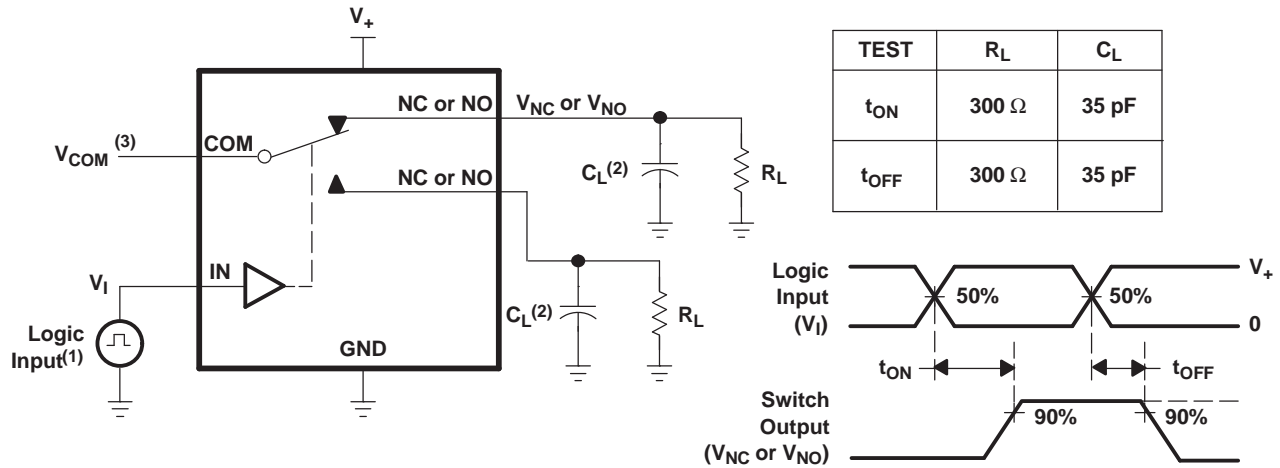


Figure 16. Capacitance (C_{IN} , $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)

PARAMETER MEASUREMENT INFORMATION (continued)



- (1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
- (2) C_L includes probe and jig capacitance.
- (3) See Electrical Characteristic for V_{COM}.

Figure 17. Turn-On (t_{ON}) and Turn-Off (t_{OFF}) Time

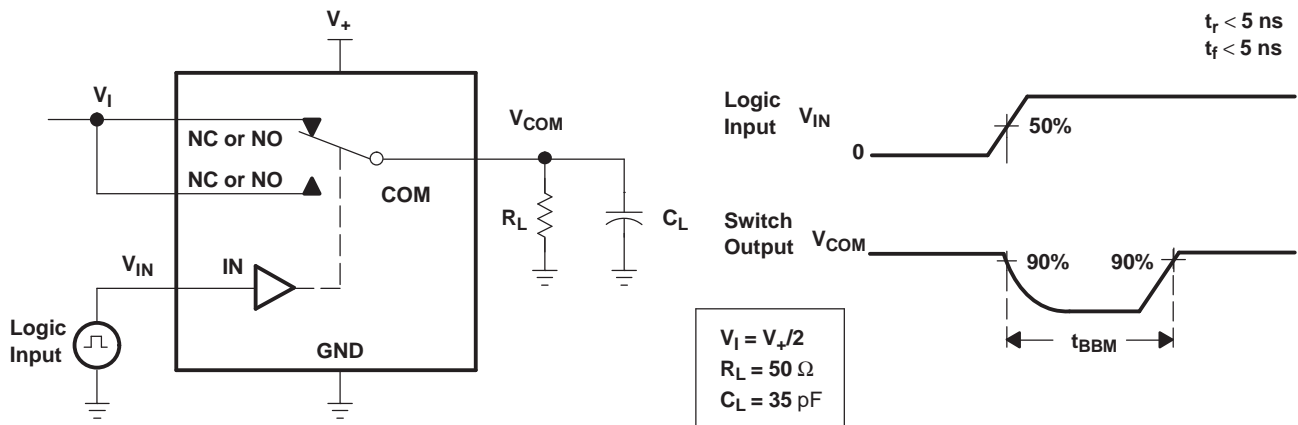


Figure 18. Break-Before-Make (t_{BBM}) Time

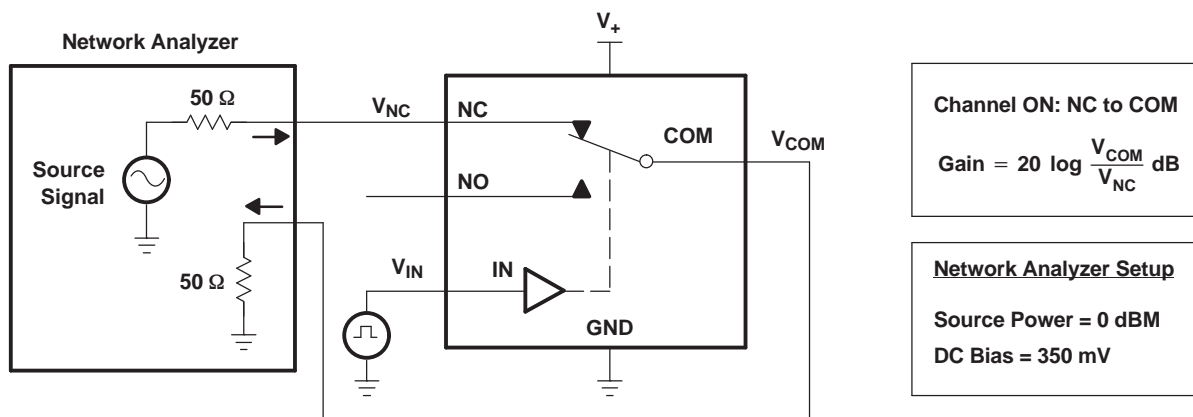


Figure 19. Frequency Response (BW)

PARAMETER MEASUREMENT INFORMATION (continued)

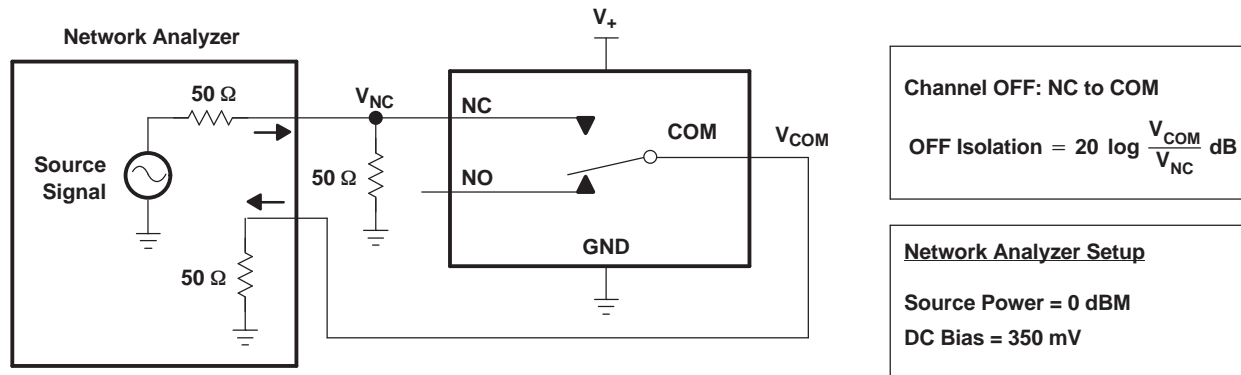


Figure 20. OFF Isolation (O_{ISO})

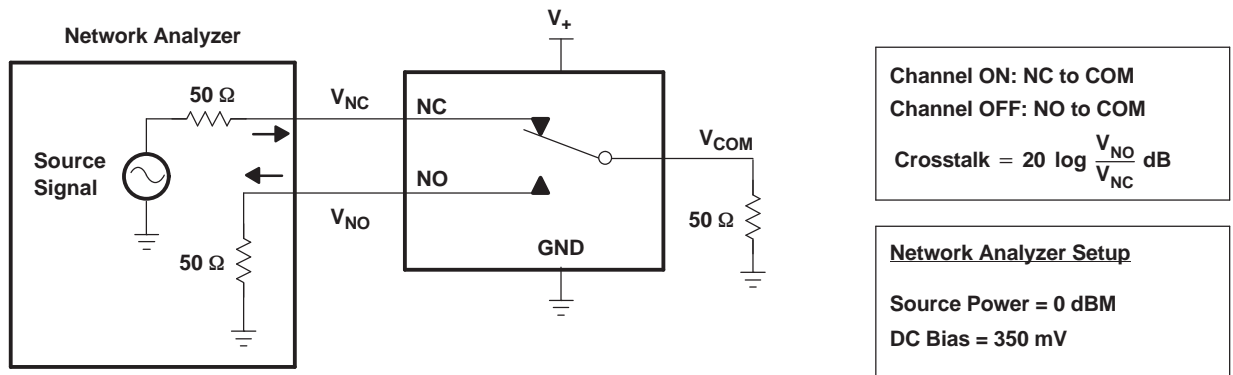


Figure 21. Crosstalk (X_{TALK})

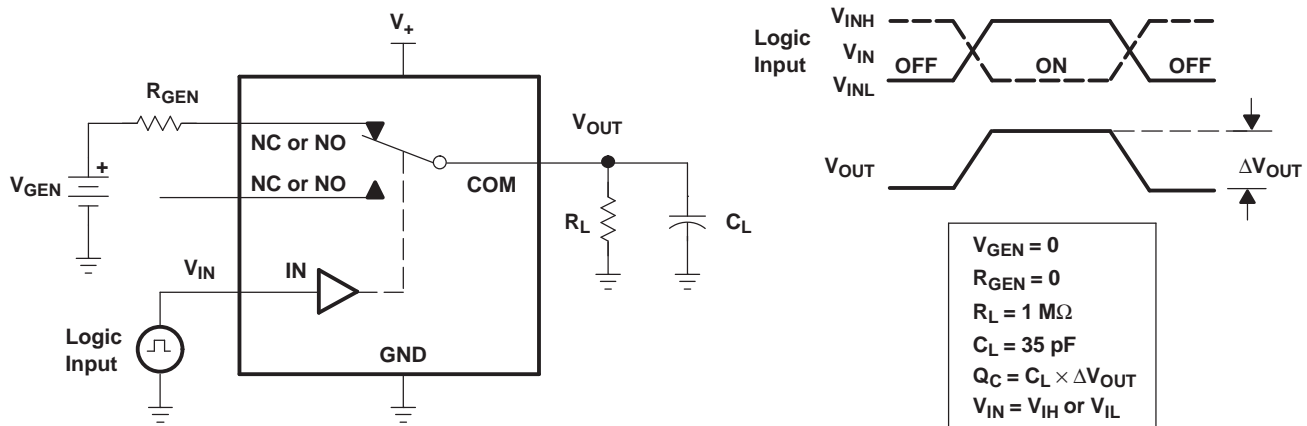


Figure 22. Charge Injection (Q_C)

PARAMETER MEASUREMENT INFORMATION (continued)

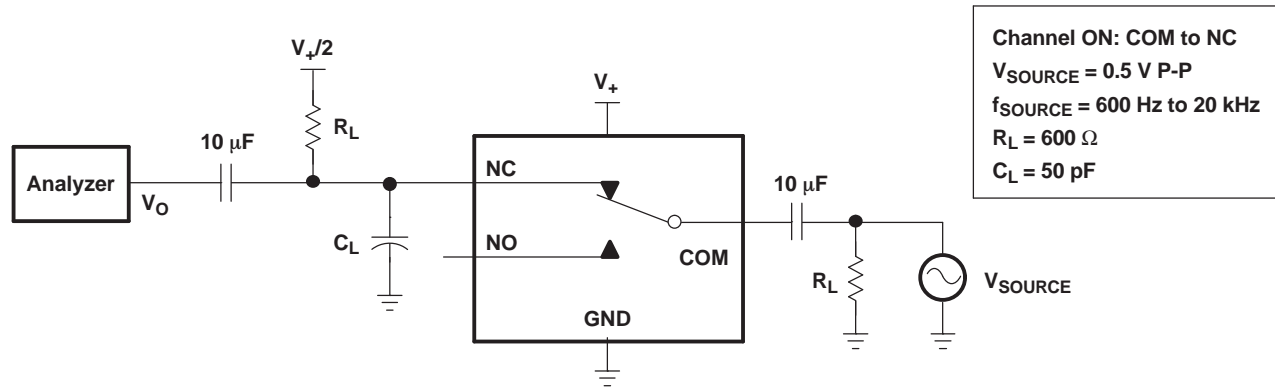
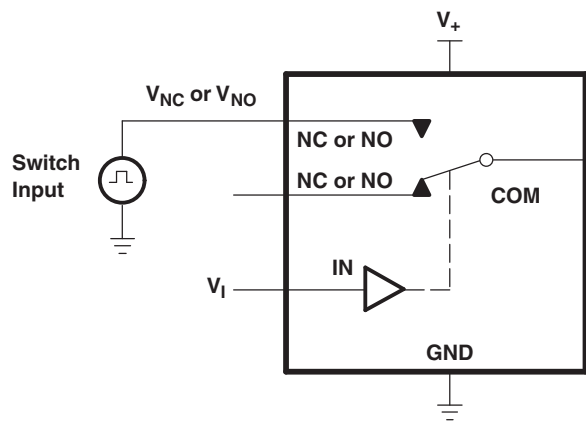


Figure 23. Total Harmonic Distortion (THD)



TEST	R_L	C_L	V_{TR}	V_I
V_{OUTU}	100 kΩ	10 pF	7 V	V_+ or GND Switch OFF
V_{OUTO}	100 kΩ	10 pF	GND	V_+ or GND Switch OFF

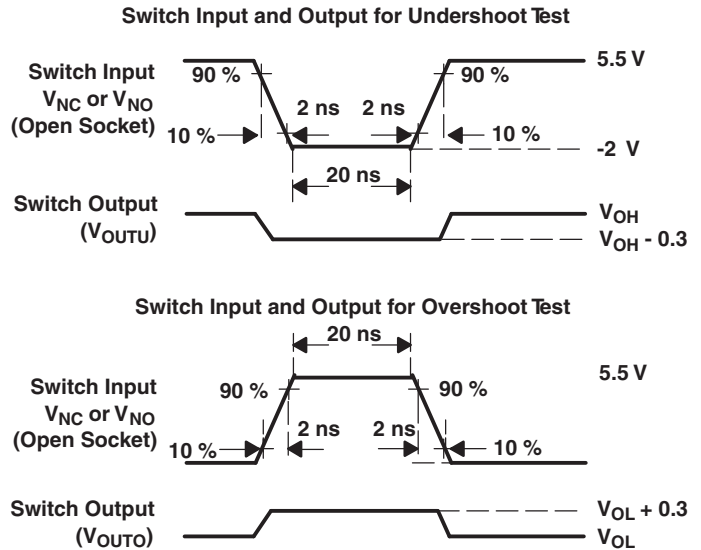


Figure 24. Undershoot and Overshoot Test

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A623157DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	35R	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A623157DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
TS5A623157DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A623157DGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
TS5A623157DGSR	VSSOP	DGS	10	2500	358.0	335.0	35.0

DGS0010A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

EXAMPLE BOARD LAYOUT

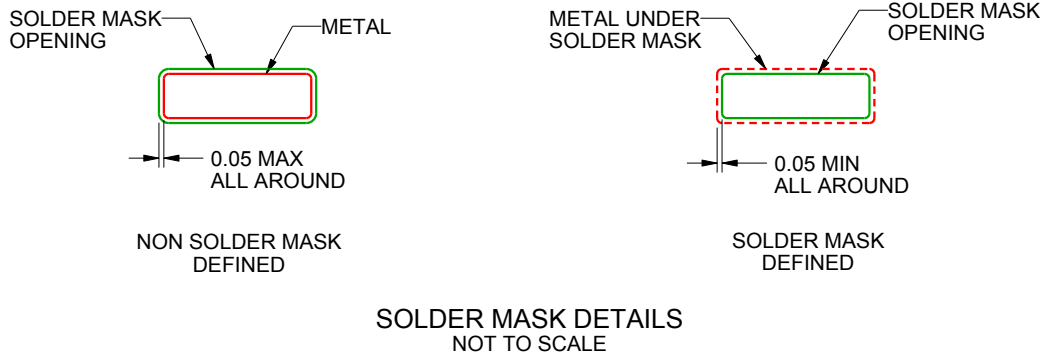
DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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