TS5MP645 4データ・レーン、2:1 MIPIスイッチ(10チャネル、2:1アナログ・スイッチ)

1 特長

- 電源電圧範囲: 1.65V～5.5V
- 10チャネルの2:1スイッチ
- 電源オフ保護
  V_{DD} = 0VのときI/OはHi-Z
- 低いR_{ON}: 標準値2.45Ω
- 低いC_{ON}: 1.5pF
- 最小帯域幅1.5GHz
- 非常に低いクロストーク: -40dB
- 低消費電力のディセーブル・モード
- 1.8V互換のロジック入力
- JESD 22を超えるESD保護
  – 人体モデル(HBM) 2000V

2 アプリケーション

- 携帯電話
- タブレット
- PC/ノートPC
- 仮想現実
- 拡張現実

3 概要

TS5MP645は、4データ・レーンのMIPIスイッチです。このデバイスは最適化された10チャネル(5差動)の単極双投スイッチで、高速アプリケーションで使用されます。TS5MP645は、複数のMIPI準拠デバイスを単一のCSI/DSI、C-PHY/D-PHYモジュールに接続しやすくするよう設計されています。

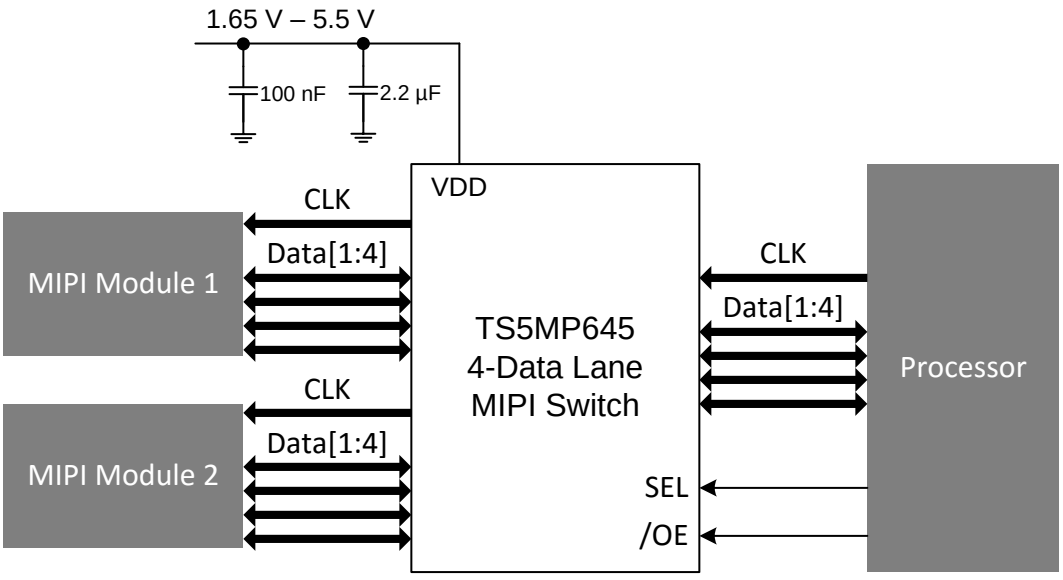
このデバイスは帯域幅が非常に優れており、チャネル間のスキューが低く、信号の劣化が小さく、レイアウト損失を補償するため広いマージンがあります。消費電流が小さいため、低消費電力アプリケーションの要求を満たすことができます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TS5MP645	DSBGA(YFP)	2.42mm×2.42mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

概略回路図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (March 2018) から **Revision B** に変更 **Page**

- Changed the I_{OFF} Test conditions From: V_{DD} = 1.65 V to 5.5 V To: V_{DD} = 0 V, 1.65 V to 5.5 V in the *Electrical Characteristics* table ... 6

2018年1月発行のものから更新 **Page**

- 「製品情報」で本体サイズ(公称)を2.459×2.459から2.42×2.42に変更 ... 1

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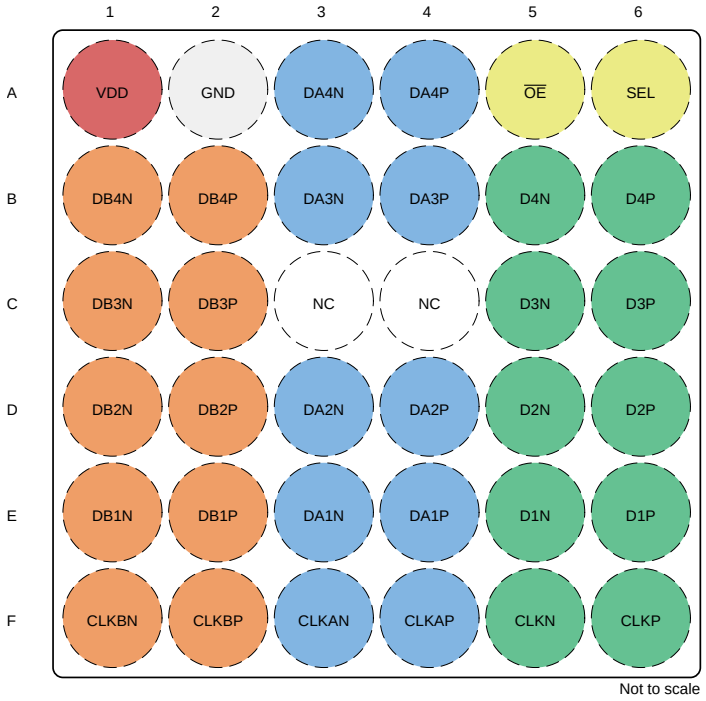
5 Pin Configuration and Functions

DSBGA Package
36 Pin (YFP)
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VDD	A1	PWR	Power supply input
GND	A2	GND	Device Ground
DA4N	A3	I/O	Differential I/O
DA4P	A4	I/O	Differential I/O
$\overline{OE}$	A5	I	Output enable (Active Low)
SEL	A6	I	Channel Select
DB4N	B1	I/O	Differential I/O
DB4P	B2	I/O	Differential I/O
DA3N	B3	I/O	Differential I/O
DA3P	B4	I/O	Differential I/O
D4N	B5	I/O	Differential I/O
D4P	B6	I/O	Differential I/O
DB3N	C1	I/O	Differential I/O
DB3P	C2	I/O	Differential I/O
NC	C3	-	No connect
NC	C4	-	No connect
D3N	C5	I/O	Differential I/O
D3P	C6	I/O	Differential I/O
DB2N	D1	I/O	Differential I/O
DB2P	D2	I/O	Differential I/O
DA2N	D3	I/O	Differential I/O

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Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
DA2P	D4	I/O	Differential I/O
D2N	D5	I/O	Differential I/O
D2P	D6	I/O	Differential I/O
DB1N	E1	I/O	Differential I/O
DB1P	E2	I/O	Differential I/O
DA1N	E3	I/O	Differential I/O
DA1P	E4	I/O	Differential I/O
D1N	E5	I/O	Differential I/O
D1P	E6	I/O	Differential I/O
CLKBN	F1	I/O	Differential I/O
CLKBP	F2	I/O	Differential I/O
CLKAN	F3	I/O	Differential I/O
CLKAP	F4	I/O	Differential I/O
CLKN	F5	I/O	Differential I/O
CLKP	F6	I/O	Differential I/O

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{DD}	Supply Voltage	-0.5	6	V
$V_{I/O}$	Analog voltage range (DxN, CLKN, DxP, CLKP, DAxN, CLKAN, DAxP, CLKAP, DBxN, CLKBN, DBxP, CLKBP)	-0.5	4	V
V_{SEL} , $V_{\overline{OE}}$	Digital Input Voltage (SEL, $\overline{OE}$)	-0.5	6	V
T_J	Junction temperature	-65	150	°C
T_{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage are with respect to ground, unless otherwise specified

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply Voltage	1.65		5.5	V
$V_{I/O}$	Analog voltage range (DxN, CLKN, DxP, CLKP, DAxN, CLKAN, DAxP, CLKAP, DBxN, CLKBN, DBxP, CLKBP)	0		3.6	V
V_{SEL}, $V_{\overline{OE}}$	Digital Input Voltage (SEL, $\overline{OE}$)	0		5.5	V
$I_{I/O}$	Continuous I/O current	-35		35	mA
T_A	Operating ambient temperature	-40		85	°C
T_J	Junction temperature	-65		150	°C

6.4 Thermal Information

THERMAL METRIC(1)		TS5MP645	UNIT
		YFP	
		36	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	57.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	12.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_{DD}	Active Supply Current	V_{DD} = 1.65 V to 5.5 V $\overline{OE}$ = 0 V SEL = 0 V to 5.5 V Dn, CLKn = 0 V	0	30	60	µA
I_{DD_PD}	Power-down Supply current	V_{DD} = 1.65 V to 5.5 V $\overline{OE}$ = V_{DD} SEL = 0 V to 5.5 V Dn, CLKn = 0 V	0	0.1	1	µA
$I_{DD_PD_1.8}$	Power-down Supply current	VDD = 1.65 V to 5.5 V $\overline{OE}$ = 1.8 V SEL = 0 V to 5.5 V Dn, CLKn = 0 V	0	0.1	10	µA
DC CHARACTERISTICS						
R_{ON_HS}	On-state resistance	V_{DD} = 1.65 V to 5.5 V $\overline{OE}$ = 0 V Dn,CLKn = -8 mA, 0.2V DAn, DBn, CLKAn, CLKBn = 0.2 V, -8 mA		2.45	5.5	Ω
R_{ON_LP}	On-state resistance	V_{DD} = 1.65 V to 5.5 V $\overline{OE}$ = 0 V Dn, CLKn = -8 mA, 1.2V DAn, DBn, CLKAn, CLKBn = 1.2 V, -8 mA		2.65	6.5	Ω
$R_{ON_flat_HS}$	On-state resistance flatness	V_{DD} = 1.65 V to 5.5 V $\overline{OE}$ = 0 V Dn, CLKn = -8 mA, 0 V to 0.3 V DAn, DBn, CLKAn, CLKBn = 0 V to 0.3 V,-8 mA		0.1		Ω
$R_{ON_flat_LP}$	On-state resistance flatness	V_{DD} = 1.65 V to 5.5 V $\overline{OE}$ = 0 V Dn, CLKn = -8 mA, 0 V to 1.3 V DAn, DBn, CLKAn, CLKBn = 0 V to 1.3 V, -8 mA		0.9		Ω
Δ_{RON_HS}	On-state resistance match between+and - paths	V_{DD} = 1.65 V to 5.5 V $\overline{OE}$ = 0 V Dn, CLKn = -8 mA, 0.2 V DAn, DBn, CLKAn, CLKBn = 0.2 V, -8 mA		0.1		Ω
Δ_{RON_LP}	On-state resistance match between+and - paths	V_{DD} = 1.65 V to 5.5 V $\overline{OE}$ = 0 V Dn, CLKn = -8 mA, 1.2 V DAn, DBn, CLKAn, CLKBn = 1.2 V, -8 mA		0.1		Ω
I_{OFF}	Switch off leakage current	V_{DD} = 0 V, 1.65 V to 5.5 V $\overline{OE}$ = 0 V to 5.5 V SEL= 0 V to 5.5 V Dn, CLKn = 0 V to 1.3 V DAn, DBn, CLKAn, CLKBn = 0 V to 1.3 V	-0.5		0.5	µA
I_{ON}	Switch on leakage current	V_{DD} = 1.65 V to 5.5 V $\overline{OE}$ = 0 V SEL= 0 V to 5.5 V Dn, CLKn = 0 V to 1.3 V DAn, DBn, CLKAn, CLKBn = 0 V to 1.3 V	-0.5		0.5	µA
DYNAMIC CHARACTERISTICS						
t_{SWITCH}	Switching time between channels	V_{DD} = 1.65 V to 5.5 V $\overline{OE}$ = 0 V Dn, CLKn = 0.6 V DAn, DBn, CLKAn, CLKBn: R_L=50 Ω, C_L = 5 pF			1.5	µs
f_{SEL_MAX}	Maximum toggling frequency for the SEL line	V_{DD} = 1.65 V to 5.5 V Dn, CLKn = 0.6 V DAn, DBn, CLKAn, CLKBn: R_L= 50 Ω, C_L=1 pF			100	kHz
$t_{ON_\overline{OE}}$	Device enable time $\overline{OE}$ to switch on	V_{DD} = 1.65 V to 5.5 V Dn, CLKn = 0.6 V DAn, DBn, CLKAn, CLKBn: R_L= 50 Ω, C_L= 1 pF		50	300	µs
t_{ON_VDD}	Device enable time V_{DD} to switch on	V_{DD} = 0 V to 1.65 V Dn, CLKn = 0.6 V DAn, DBn, CLKAn, CLKBn: R_L= 50 Ω, C_L= 1 pF		50	300	µs

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Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{OFF_\overline{OE}}$	Device disable time $\overline{OE}$ to switch off	V_{DD} = 1.65 V to 5.5 V Dn, CLKn = 0.6 V DAn, DBn, CLKAn, CLKBn: R_L= 50 Ω, C_L= 1 pF		0.5	1	µs
t_{OFF_VDD}	Device disable time V_{DD} to switch off	V_{DD} = 5 V to 0 V VDD ramp rate = 250 µs Dn, CLKn = 0.6 V DAn, DBn, CLKAn, CLKBn: R_L = 50 Ω, C_L = 1pF		0.5	1	ms
$t_{MIN_\overline{OE}}$	Minimum pulse width for $\overline{OE}$	V_{DD} = 1.65 V to 5.5 V Dn, CLKn = 0.6 V DAn, DBn, CLKAn, CLKBn: R_L = 50 Ω, C_L = 1 pF	500			ns
t_{BBM}	Break before make time	V_{DD} = 1.65 V to 5.5 V $\overline{OE}$ = 0 V Dn, CLKn = R_L = 50 Ω, C_L = 1 pF DAn, DBn, CLKAn, CLKBn: 0.6 V	50			ns
t_{SKEW}	Intrapair skew	V_{DD} = 1.65 V to 5.5 V $\overline{OE}$ = 0 V Dn, CLKn = 0.3 V DAn, DBn, CLKAn, CLKBn: R_L = 50 Ω, C_L = 1 pF		1		ps
t_{SKEW}	Interpair Skew	V_{DD} = 1.65 V to 5.5 V $\overline{OE}$ = 0 V Dn, CLKn = 0.3 V DAn, DBn, CLKAn, CLKBn: R_L = 50 Ω, C_L = 1 pF		4		ps
t_{PD}	Propagation delay with 100 ps rise time	V_{DD} = 1.65 V to 5.5 V $\overline{OE}$ = 0 V Dn, CLKn = 0.6 V DAn, DBn, CLKAn, CLKBn: R_L = 50 Ω, C_L = 1 pF t_{RISE} = 100 ps		40		ps
O_{ISO}	Differential off isolation	V_{DD} = 1.65 V $\overline{OE}$ = 0 V, V_{DD} SEL = 0 V, V_{DD} Dn, CLKn, DAn, DBn, CLKAn, CLKBn: R_S = 50 Ω, R_L = 50 Ω, C_L = 1 pF $V_{I/O}$ = 200 mV + 200 mV_{PP} (differential) f = 1250 MHz		-20		dB
X_{TALK}	Differential channel to channel crosstalk	V_{DD} = 1.65 V to 5.5 V $\overline{OE}$ = 0 V, V_{DD} SEL = 0 V, V_{DD} Dn, CLKn, DAn, DBn, CLKAn, CLKBn: R_S = 50 Ω, R_L = 50 Ω, C_L = 1 pF $V_{I/O}$ = 200 mV + 200 mV_{PP} (differential) f = 1250 MHz		-40		dB
BW	Differential Bandwidth	V_{DD} = 1.65 V to 5.5 V $\overline{OE}$ = 0 V SEL = 0 V, V_{DD} Dn, CLKn, DAn, DBn, CLKAn, CLKBn: R_S = 50 Ω, R_L = 50 Ω, C_L = 1 pF $V_{I/O}$ = 200 mV + 200 mV_{PP} (differential)	1.5	2		GHz
I_{LOSS}	Insertion Loss	V_{DD} = 1.65 V to 5.5 V $\overline{OE}$ = 0 V SEL = 0 V, V_{DD} Dn, CLKn, DAn, DBn, CLKAn, CLKBn: R_S = 50 Ω, R_L = 50 Ω, C_L = 1 pF $V_{I/O}$ = 200 mV + 200 mV_{PP} (differential) f = 100 kHz	-0.4			dB
C_{OFF}	Off capacitance	V_{DD} = 1.65 V to 5.5 V $\overline{OE}$ = 0 V, V_{DD} SEL = 0 V, V_{DD} Dn, CLKn, DAn, DBn, CLKAn, CLKBn = 0 V , 0.2 V f = 1250 MHz		1.5		pF
C_{ON}	On capacitance	V_{DD} = 1.65 V to 5.5 V $\overline{OE}$ = V_{DD} SEL = 0 V, V_{DD} Dn, CLKn, DAn, DBn, CLKAn, CLKBn = 0 V , 0.2 V f = 1250 MHz		1.5		pF

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Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL CHARACTERISTICS						
V_{IH}	Input logic high (SEL, $\overline{OE}$)	$V_{I/O}$ = 0.6 V, R_L = 50 Ω, C_L = 5 pF	1.425		5.5	V
V_{IL}	Input logic low (SEL, $\overline{OE}$)	$V_{I/O}$ = 0.6 V, R_L = 50 Ω, C_L = 5 pF	0		0.5	V
I_{IH}	Input high leakage current (SEL, $\overline{OE}$)	$V_{I/O}$ = 0.6 V, R_L = 50 Ω, C_L = 5 pF	-5		5	µA
I_{IL}	Input low leakage current (SEL, $\overline{OE}$)	$V_{I/O}$ = 0.6 V, R_L = 50 Ω,C_L = 5 pF	-5		5	µA
R_{PD}	Internal pull-down resistance on digital input pins	$V_{I/O}$ = 0.6 V, R_L = 50 Ω, C_L = 5 pF		6		MΩ
C_{SEL}, $C_{\overline{OE}}$	Digital Input capacitance (SEL, $\overline{OE}$)	f = 1 MHz		5		pF

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6.6 Typical Characteristics

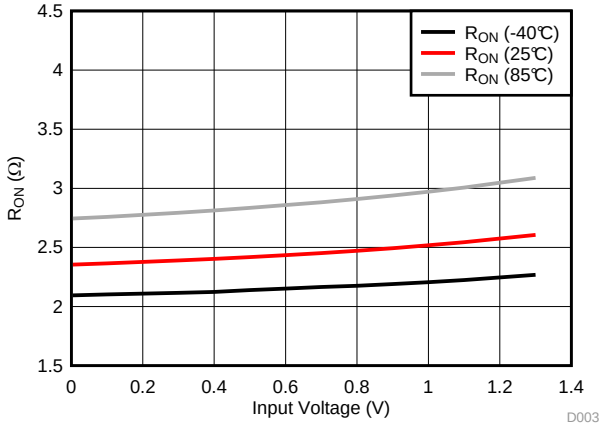

図 1. R_{ON} vs Input Voltage. V_{DD} = 1.65 V

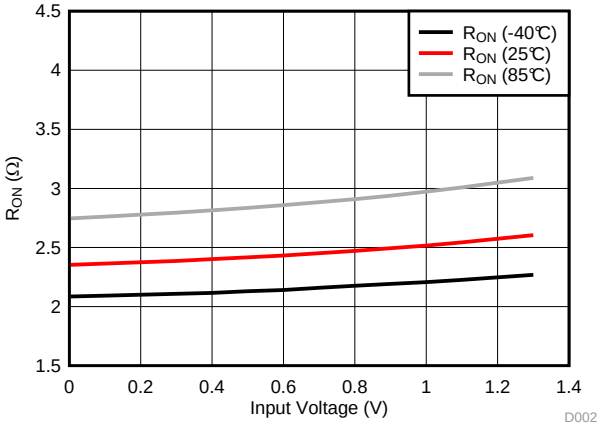

図 2. R_{ON} vs Input Voltage. V_{DD} = 3.3 V

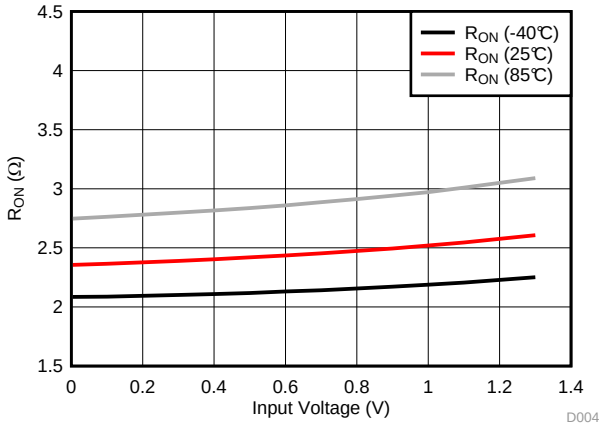

図 3. R_{ON} vs Input Voltage. V_{DD} = 5.5 V

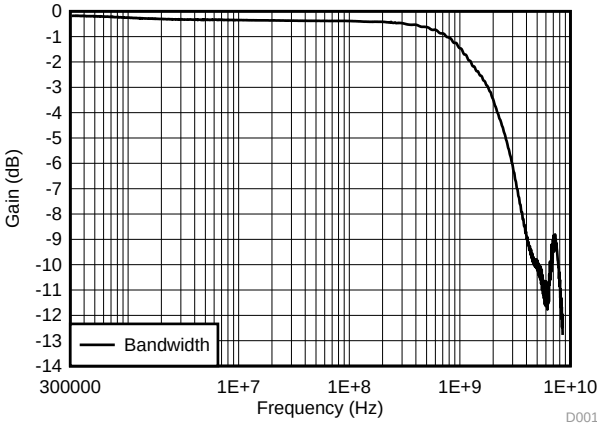

図 4. Differential Bandwidth

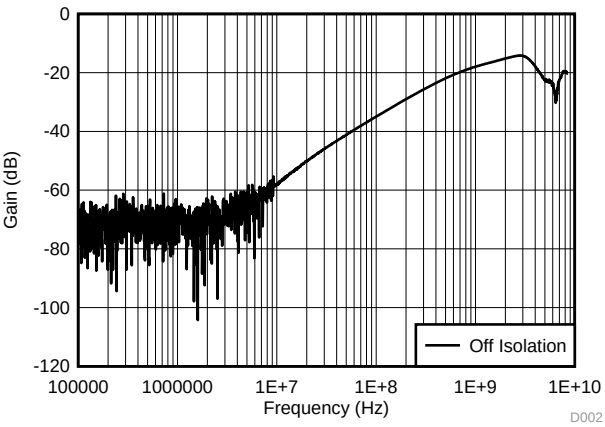

図 5. Off Isolation

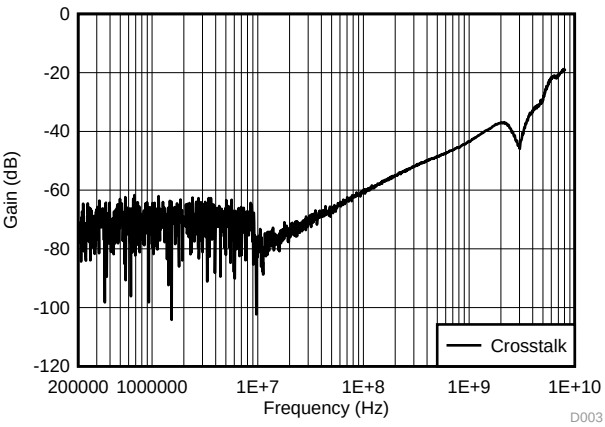

図 6. Differential Crosstalk

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7 Parameter Measurement Information

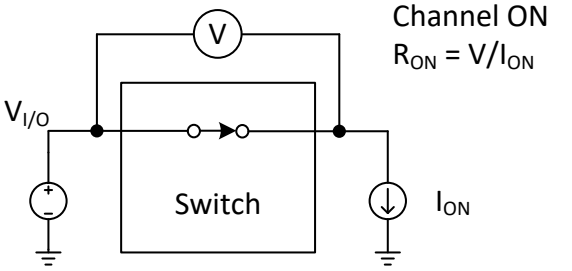

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図 7. On Resistance

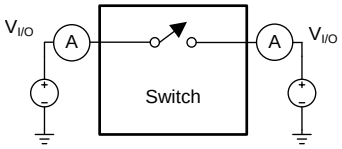


図 8. Off Leakage

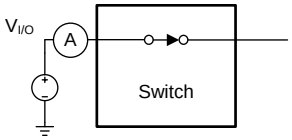
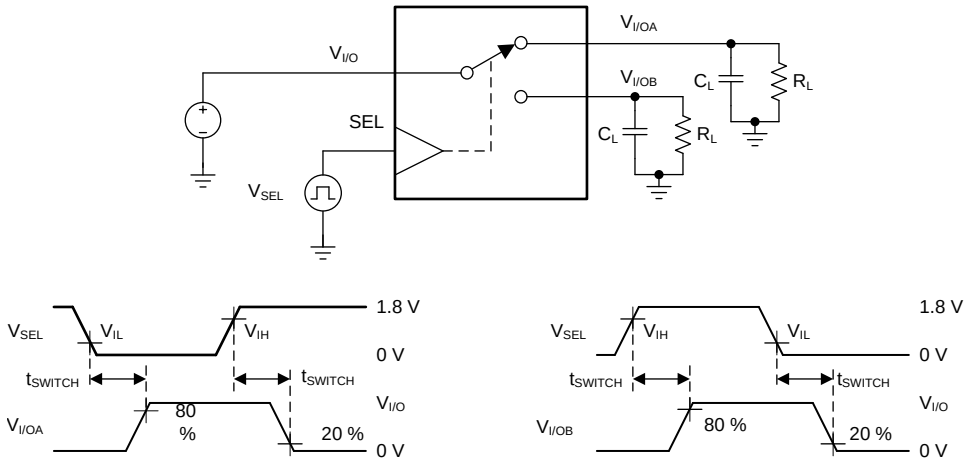


図 9. On Leakage



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(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω , t_r = 3 ns, t_f = 3 ns.

(2) C_L includes probe and jig capacitance.

図 10. t_{SWITCH} timing

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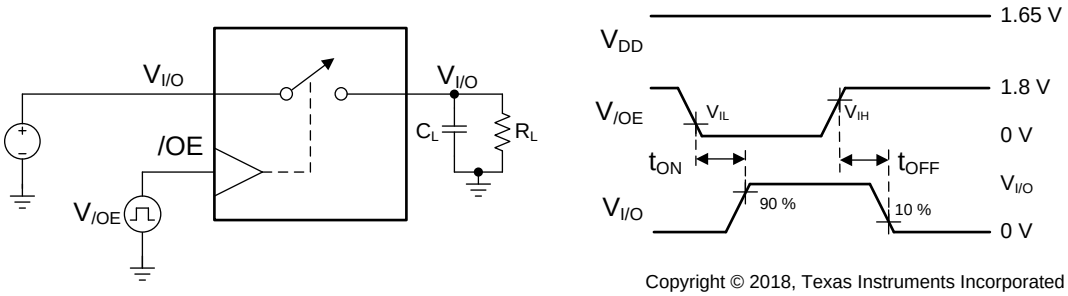
Parameter Measurement Information (continued)



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(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω , t_r = 3 ns, t_f = 3 ns.

(2) C_L includes probe and jig capacitance.

図 11. t_{ON} and t_{OFF} Timing for $\overline{OE}$

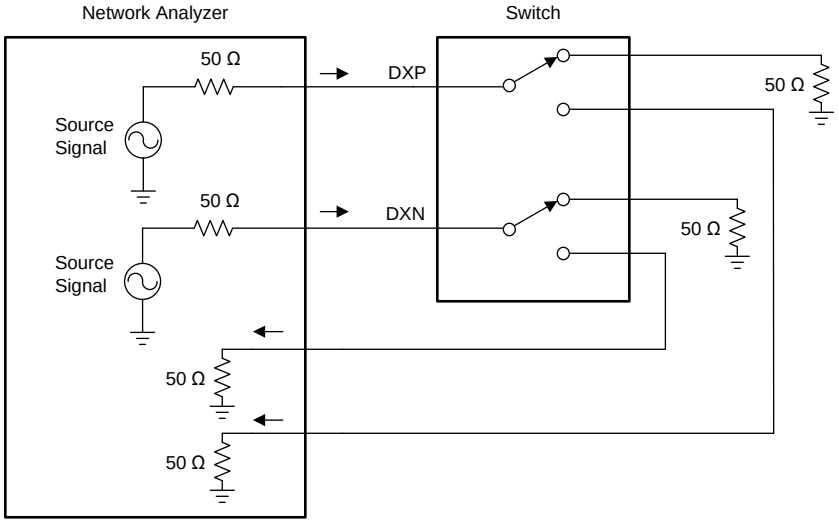

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図 12. Off Isolation

Parameter Measurement Information (continued)

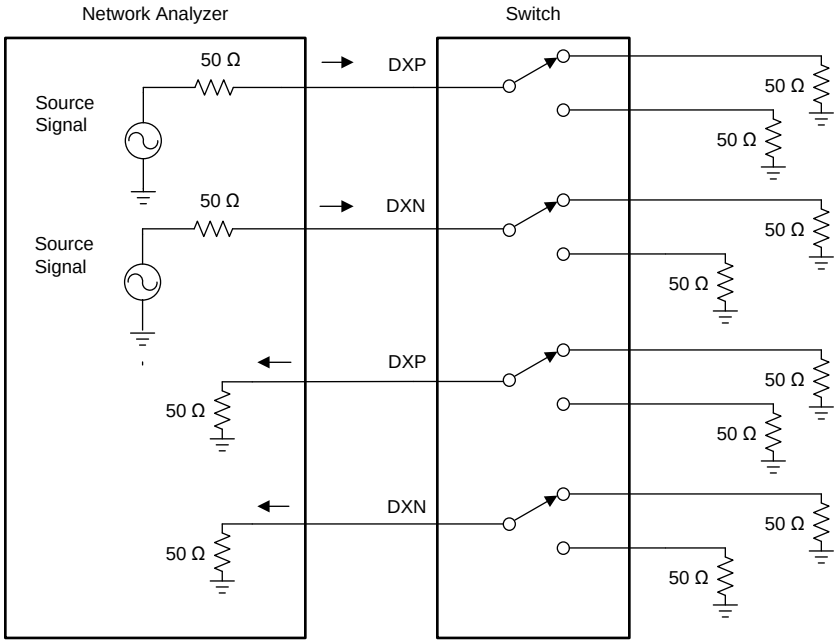

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図 13. Crosstalk

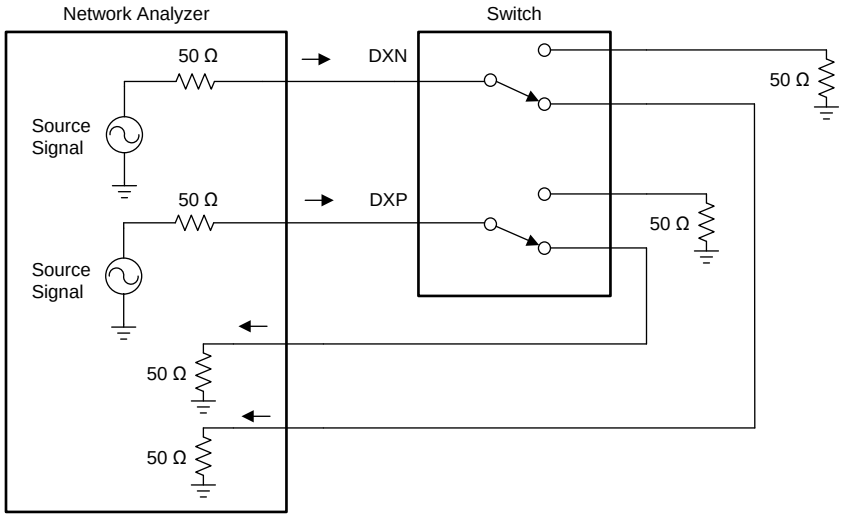

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図 14. BW and Insertion Loss

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Parameter Measurement Information (continued)

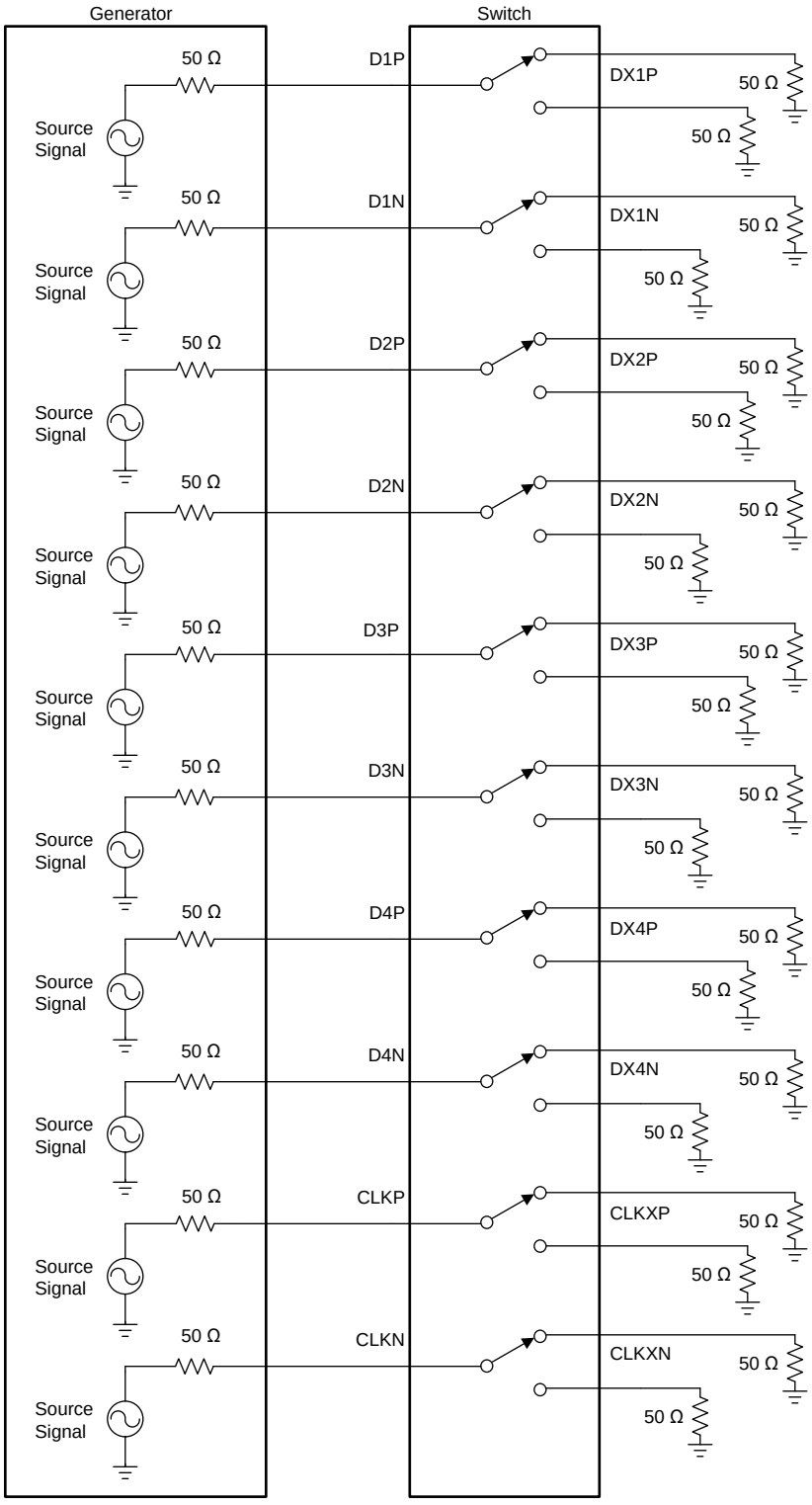

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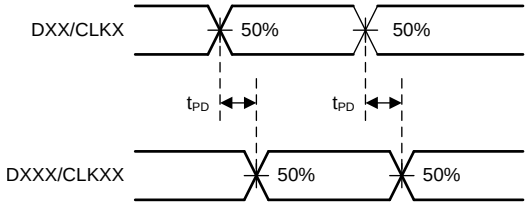
図 15. t_{PD}, $t_{SKEW(INTRA)}$ and t_{SKEW} Setup

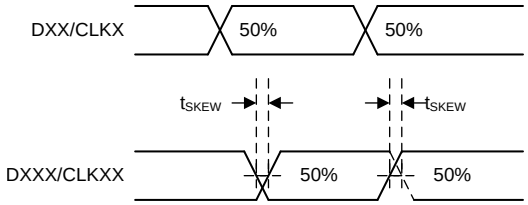
Parameter Measurement Information (continued)



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω , t_r = 100 ps, t_f = 100 ps.

(2) C_L includes probe and jig capacitance.

図 16. t_{PD}



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω , t_r = 100 ps, t_f = 100 ps.

(2) C_L includes probe and jig capacitance.

図 17. t_{SKEW}

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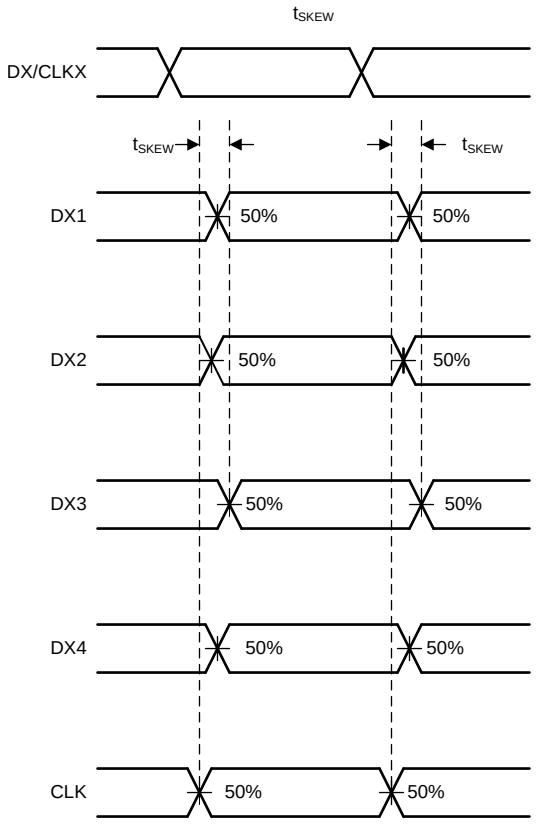
Parameter Measurement Information (continued)

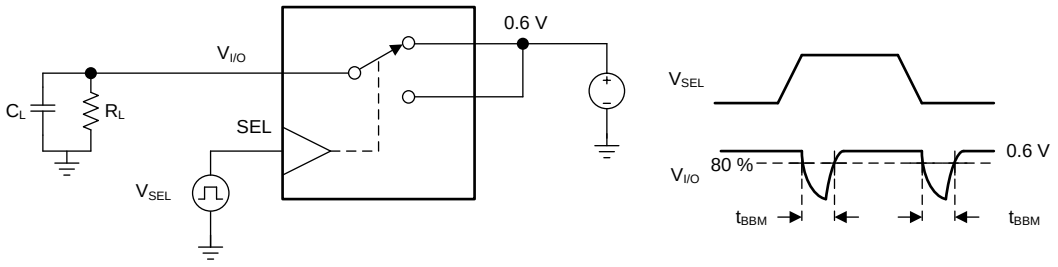


(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω , t_r = 100 ps, t_f = 100 ps.

(2) C_L includes probe and jig capacitance.

(3) $t_{SK(INTER)}$ is the max skew between all channels. Diagram exaggerates $t_{SK(INTER)}$ to show measurement technique

図 18. t_{SKEW}



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(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω , t_r = 3 ns, t_f = 3 ns.

(2) C_L includes probe and jig capacitance.

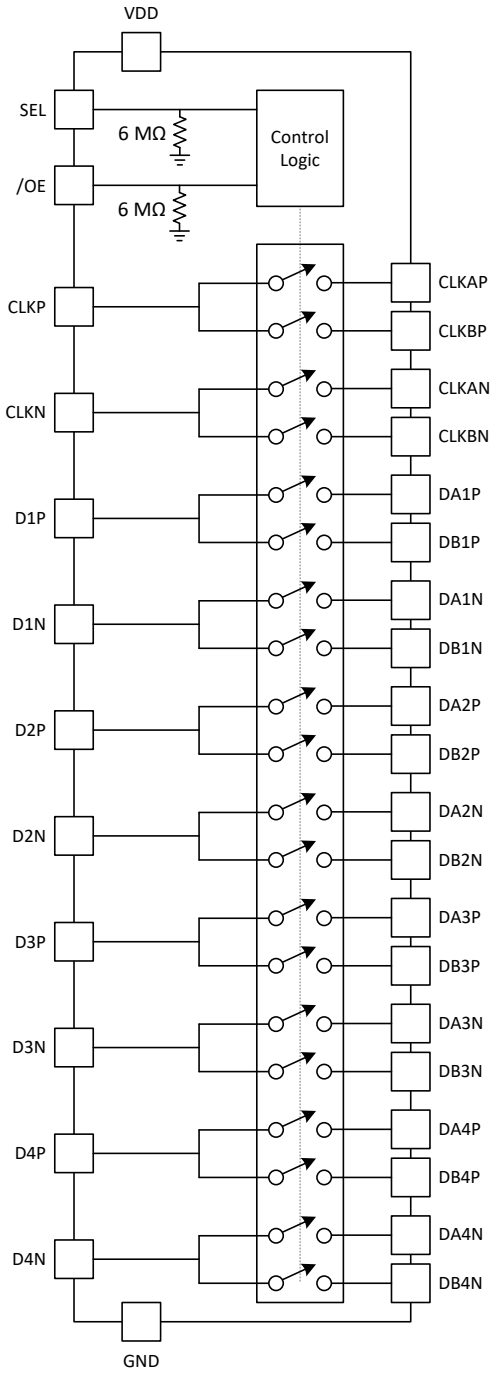
図 19. t_{BBM}

8 Detailed Description

8.1 Overview

The TS5MP645 is a high-speed 4 Data lane 2:1 MIPI Switch. The device includes 10 channels (5 differential) with 4 differential data lanes and 1 differential clock lane for D-PHY, CSI or DSI. The switch allows a single MIPI port to interface between two MIPI modules, expanding the number of potential MIPI devices that can be used within a system that is MIPI port limited.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Powered-Off Protection

When the TS5MP645 is powered off (VDD = 0 V) the I/Os and digital logic pins of the device will remain in a high impedance state. The crosstalk, off-isolation, and leakage remains within the electrical specifications. This prevents errant voltages from reaching the rest of the system and maintains isolation when the system is powering up.

図 20 shows an example system containing a switch without powered-off protection with the following system level scenario

1. Subsystem A powers up and starts sending information to Subsystem B that remains unpowered.
2. The I/O voltage back powers the supply rail in Subsystem B.
3. The digital logic is back powered and turns on the switch. The signal is transmitted to Subsystem B before it is powered and damages it.

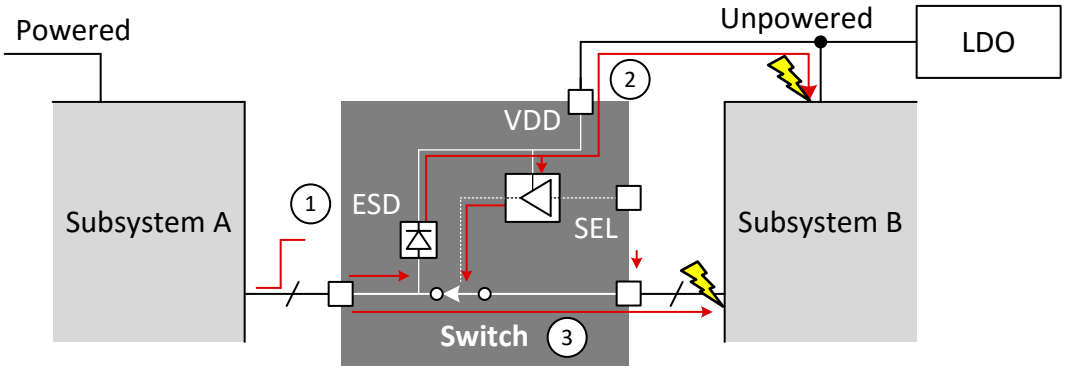

図 20. System Without Powered-Off Protection

With powered-off protection, the switch prevents back powering the supply and the switch remains high-impedance. Subsystem B remains protected.

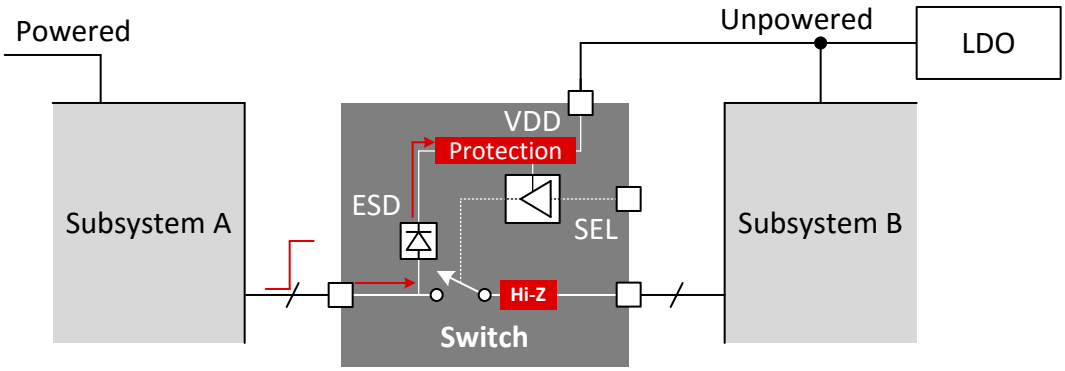

図 21. System With Powered-Off Protection

This features has the following system level benefits.

- Protects the system from damage.
- Prevents data from being transmitted unintentionally
- Eliminates the need for power sequencing solutions reducing BOM count and cost, simplifying system design and improving reliability.

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Feature Description (continued)

8.3.2 1.8 V Logic Compatible Inputs

The TS5MP645 has 1.8 V logic compatible digital inputs for switch control. Regardless of the V_{DD} voltage the digital input thresholds remained fixed, allowing a 1.8 V processor GPIO to control the TS5MP645 without the need for an external translator. This saves both space and BOM cost.

An example setup for a system without a 1.8 V logic compatible input is shown in 図 22. Here the supply mismatch between the process and its GPIO output and the supply to the switch require a translator.

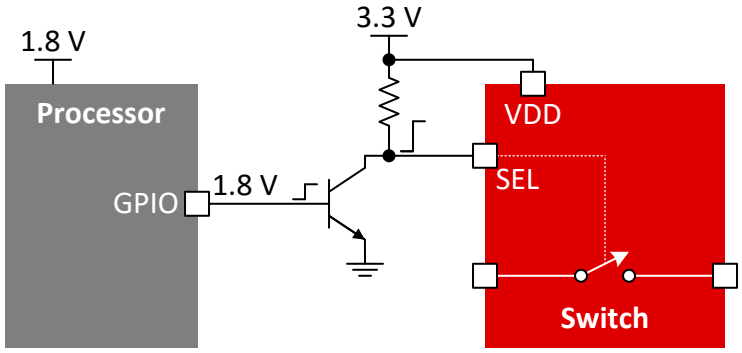

図 22. System Without 1.8 V Logic Compatible Inputs

With the 1.8 V logic compatibility in the TS5MP645, the translator is built in to the device so that the external components are no longer needed, simplifying the system design and overall cost.

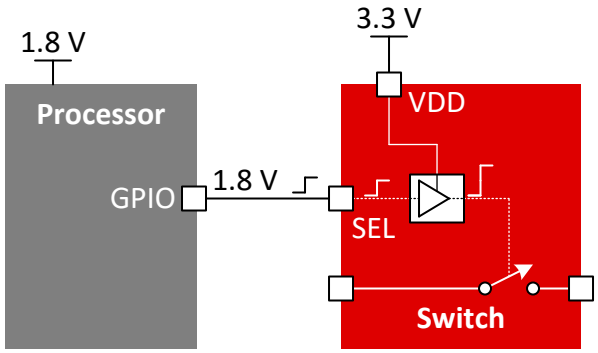

図 23. System With 1.8 V Logic Compatible Inputs

8.3.3 Low Power Disable Mode

The TS5MP645 has a low power mode that places all the signal paths in a high impedance state and lowers the current consumption while the device is not in use. To put the device in low power mode and disable the switch, the output enable pin $\overline{OE}$ must be supplied with a logic high signal.

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8.4 Device Functional Modes

8.4.1 Pin Functions

SEL and $\overline{OE}$ have weak 6-MΩ pulldown resistors to prevent floating input logic.

表 1. Function Table

$\overline{OE}$	SEL	Function
H	X	I/O pins High-Impedance
L	L	CLK(P/N) = CLKA(P/N)
		Dn(P/N) = DAn(P/N)
L	H	CLK(P/N) = CLKB(P/N)
		Dn(P/N) = DBn(P/N)

8.4.2 Low Power Mode

While the output enable pin $\overline{OE}$ is supplied with a logic high the device remains in low power state. This reduces the current consumption substantially and the switches are be high impedance. The SEL pin is ignored while the $\overline{OE}$ remains high. Upon exiting low power mode, the switch status reflects the SEL pin as seen in 表 1.

8.4.3 Switch Enabled Mode

While the output enable pin $\overline{OE}$ is supplied with a logic low the device will remain in switch enabled mode.

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9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.2 Typical Application

図 24 represents a typical application of the TS5MP645 MIPI switch. The TS5MP645 is used to switch signals between multiple MIPI modules and a single MIPI port on a processor. This expands the capabilities of a single port to handle multiple MIPI modules.

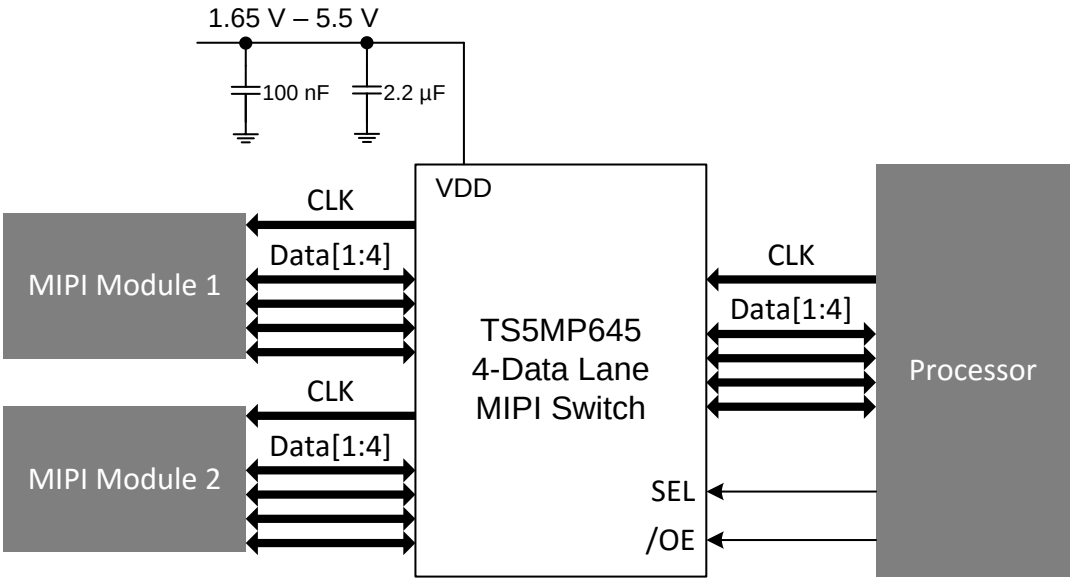

図 24. Typical TS5MP645 Application

9.2.1 Design Requirements

Design requirements of the MIPI standard being used must be followed. Supply pin decoupling capacitors of 2.2 µF and 100 nF are recommended for best performance. The TS5MP645 has internal 6-MΩ pulldown resistors on SEL and $\overline{OE}$. The pulldown on these pins ensure that the digital remains in a non-floating state during system power-up to prevent shoot through current spikes and an unknown switch status. By default the switch will power up enabled and with the A path selected until driven externally by the processor.

9.2.2 Detailed Design Procedure

The TS5MP645 can be properly operated without any external components. However, TI recommends that unused I/O signal pins be connected to ground through a 50 Ω resistor to prevent signal reflections and maintain device performance. The NC pins of the device do not require any external connections or terminations and have no connection to the rest of the device internally.

The clock and data lanes can be interchanged as necessary to facilitate the best layout possible for the application. For example the clock can be placed on the D1 channel and a data lane can be used on the CLK channel if this improves the layout. In addition the signal lines of the TS5MP645 are routed single ended on the chip die. This makes the device suitable for both differential and single-ended high-speed systems.

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Typical Application (continued)

9.2.3 Application Curves

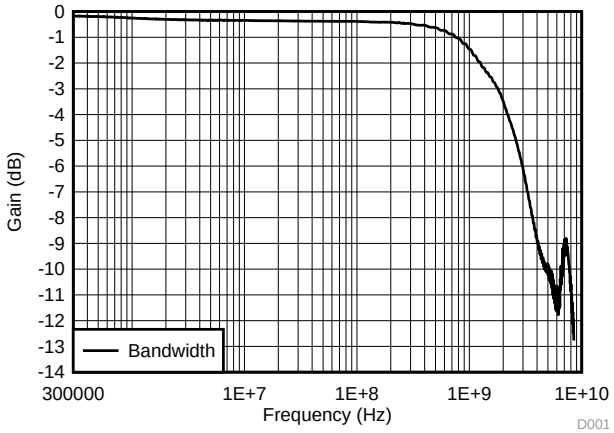

図 25. Differential Bandwidth

10 Power Supply Recommendations

When the TS5MP645 is powered off (V_{DD} = 0 V), the I/Os of the device remains in a high-Z state. The crosstalk, off-isolation, and leakage remain within the electrical *Specifications*. Power to the device is supplied through the VDD pin. Decoupling capacitors of 100 nF and 2.2 µF are recommended on the supply.

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11 Layout

11.1 Layout Guidelines

Place the supply de-coupling capacitors as close to the VDD and GND pin as possible. The spacing between the power traces, supply and ground, and the signal I/O lines, clock and data, should be a minimum of three times the race width of the signal I/O lines to maintain signal integrity.

The characteristic impedance of the trace(s) must match that of the receiver and transmitter to maintain signal integrity. Route the high-speed traces using a minimum amount of vias and corners. This will reduce the amount of impedance changes.

When it becomes necessary to make the traces turn 90°, use two 45° turns or an arc instead of making a single 90° turn.

Do not route high-speed traces near crystals, oscillators, external clock signals, switching regulators, mounting holes or magnetic devices.

Avoid stubs on the signal lines.

All I/O signal traces should be routed over a continuous ground plane with no interruptions. The minimum width from the edge of the trace to any break in the ground plane must be 3 times the trace width. When routing on PCB inner signal layers, the high speed traces should be between two ground planes and maintain characteristic impedance.

High speed signal traces must be length matched as much as possible to minimize skew between data and clock lines.

11.2 Layout Example

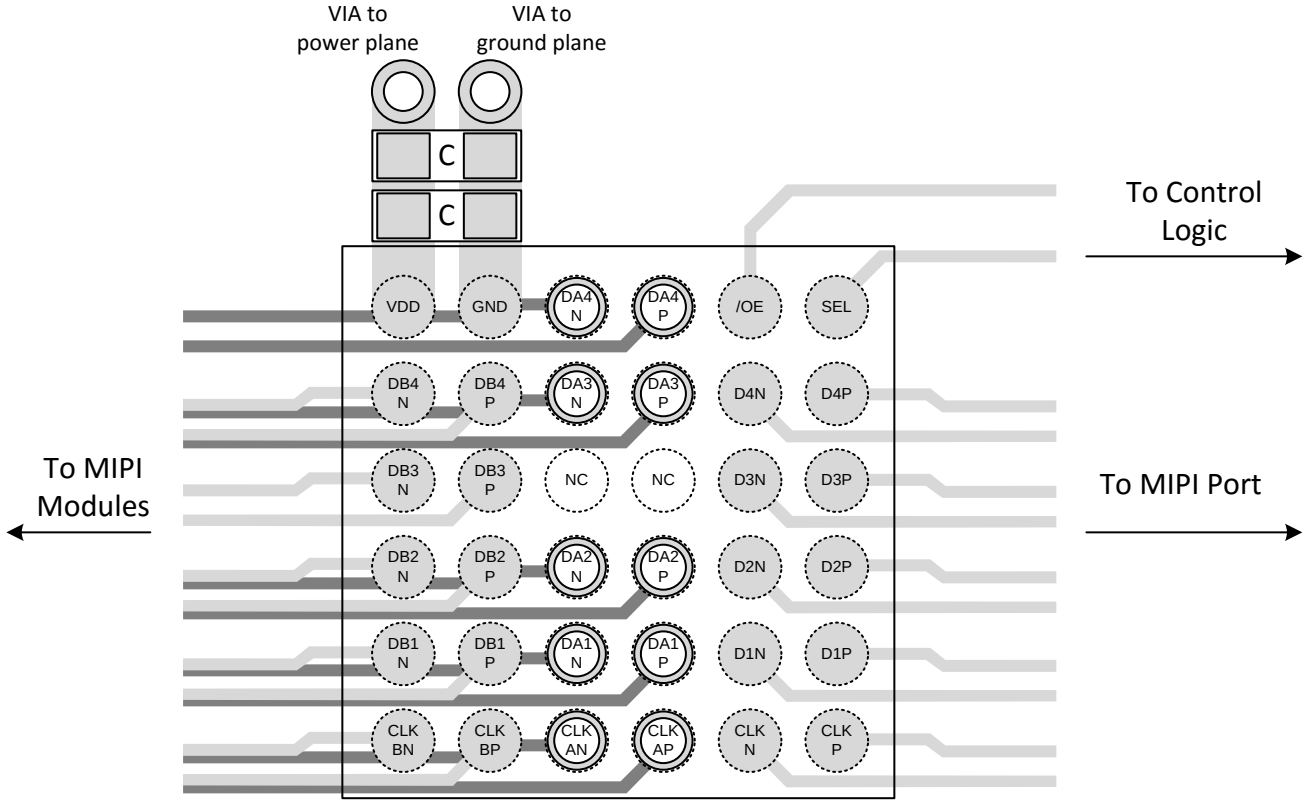

図 26. Layout Example

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12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.2 ドキュメントの更新通知を受け取る方法

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12.3 コミュニティ・リソース

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静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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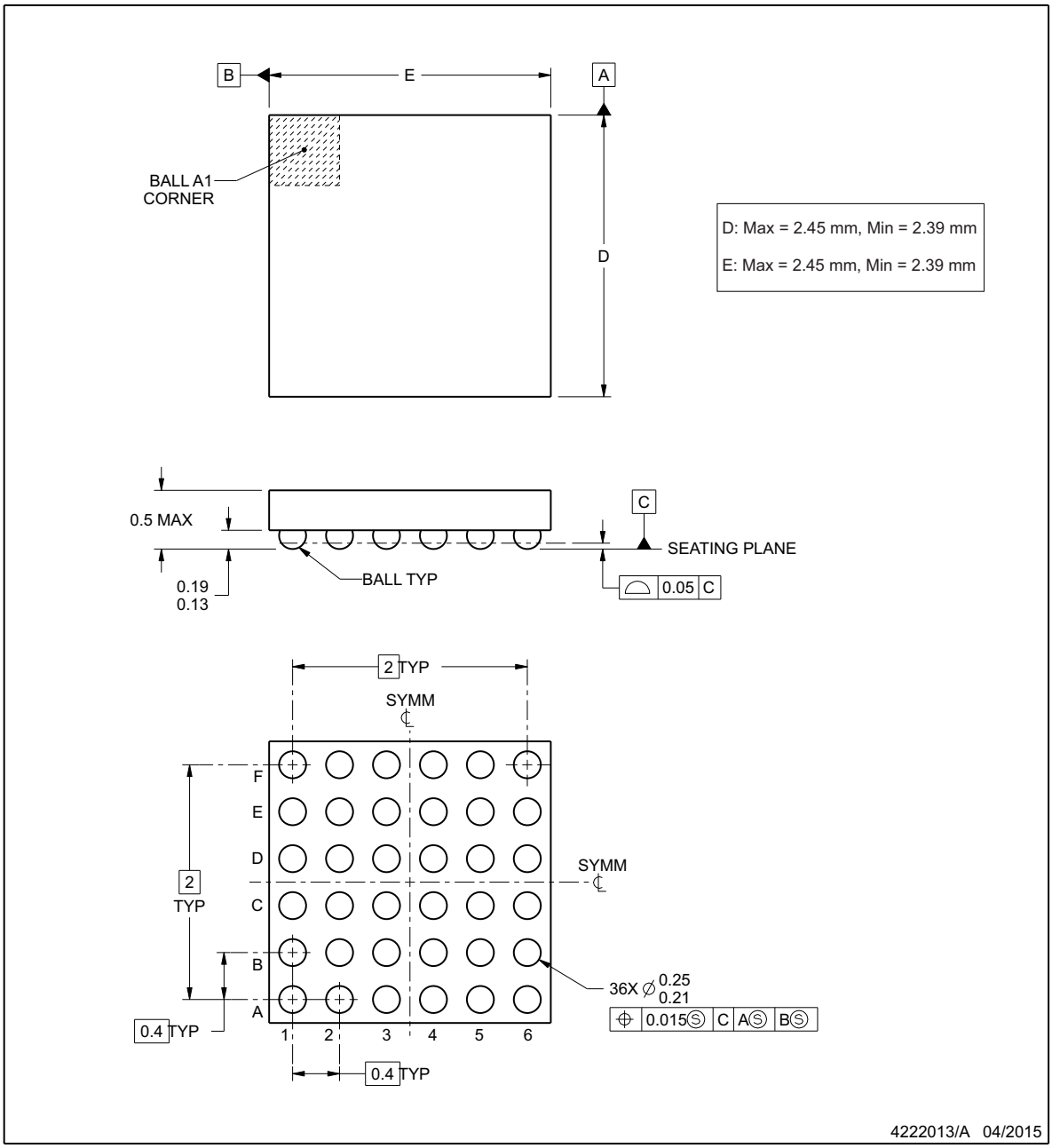
PACKAGE OUTLINE

YFP0036

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

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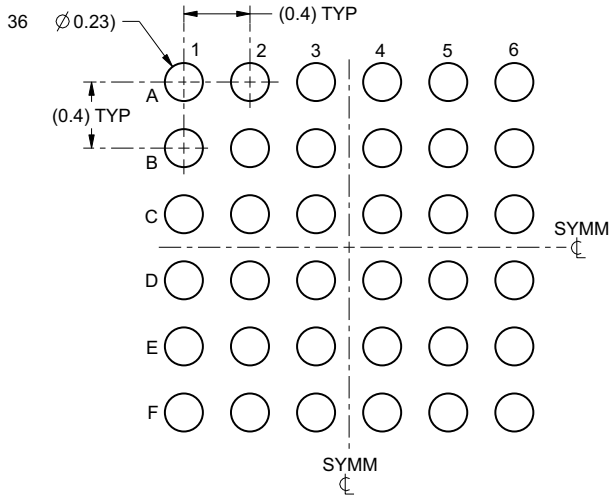
EXAMPLE BOARD LAYOUT

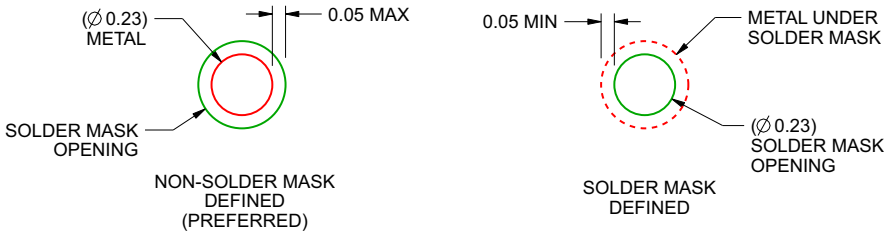
YFP0036

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS
NOT TO SCALE

4222013/A 04/2015

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

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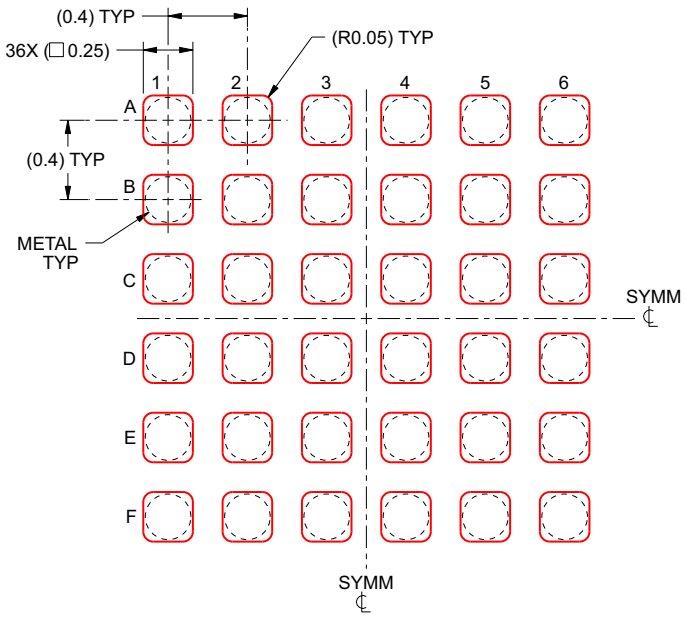
EXAMPLE STENCIL DESIGN

YFP0036 **DSBGA - 0.5 mm max height**

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4222013/A 04/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS5MP645NYFPR	NRND	Production	DSBGA (YFP) | 36	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TS5MP645
TS5MP645NYFPR.A	NRND	Production	DSBGA (YFP) | 36	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TS5MP645
TS5MP645YFPR	NRND	Production	DSBGA (YFP) | 36	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TS5MP645
TS5MP645YFPR.A	NRND	Production	DSBGA (YFP) | 36	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TS5MP645

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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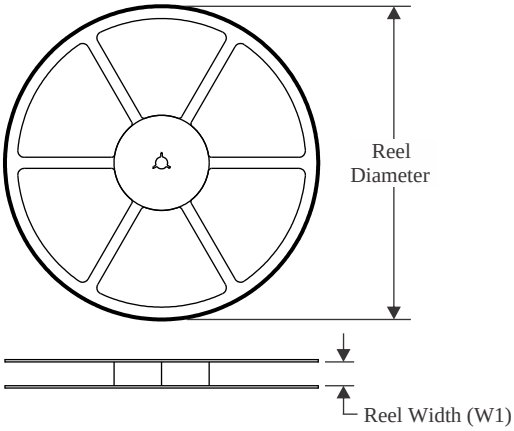
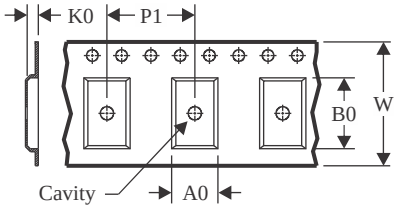
TAPE AND REEL INFORMATION

REEL DIMENSIONS

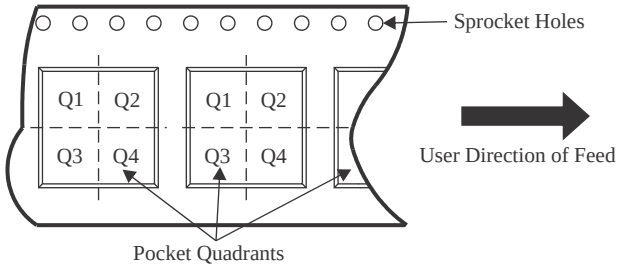


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

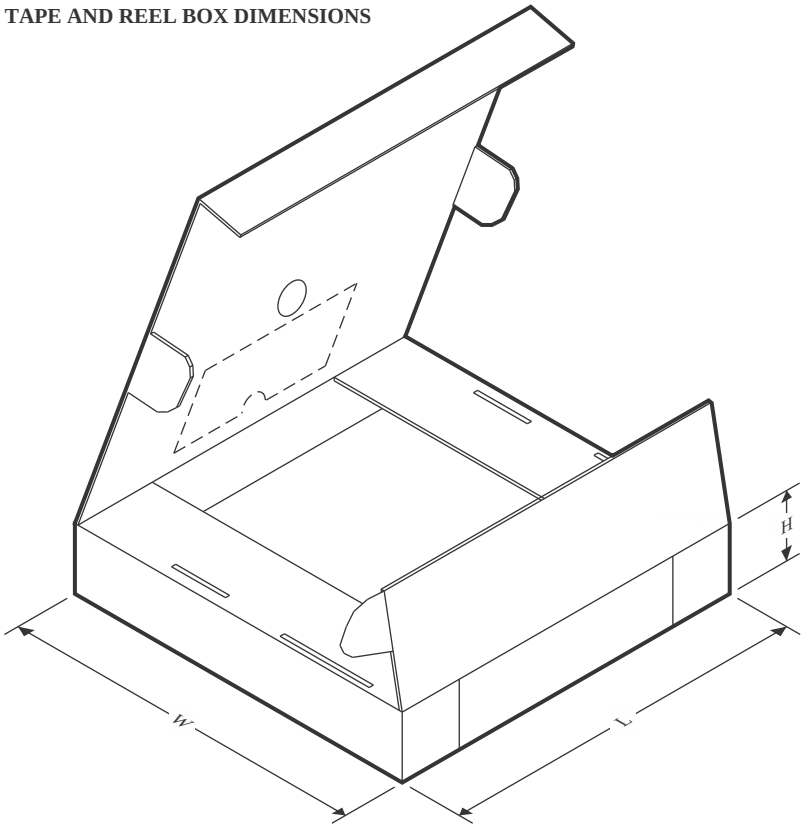
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5MP645NYFPR	DSBGA	YFP	36	3000	180.0	8.4	2.58	2.58	0.62	4.0	8.0	Q1
TS5MP645YFPR	DSBGA	YFP	36	3000	330.0	12.4	2.58	2.58	0.62	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

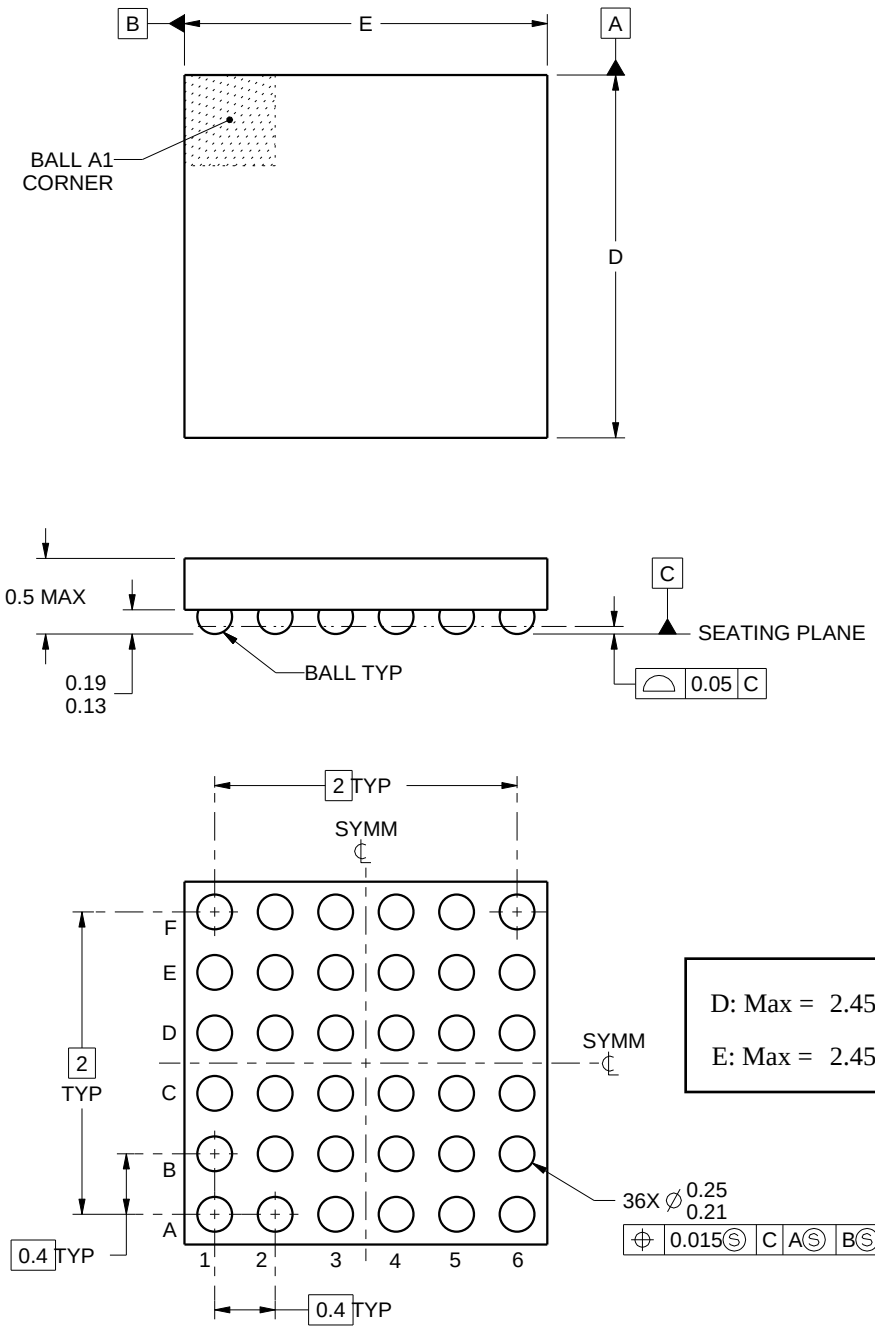
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5MP645NYFPR	DSBGA	YFP	36	3000	182.0	182.0	20.0
TS5MP645YFPR	DSBGA	YFP	36	3000	335.0	335.0	25.0

PACKAGE OUTLINE

YFP0036

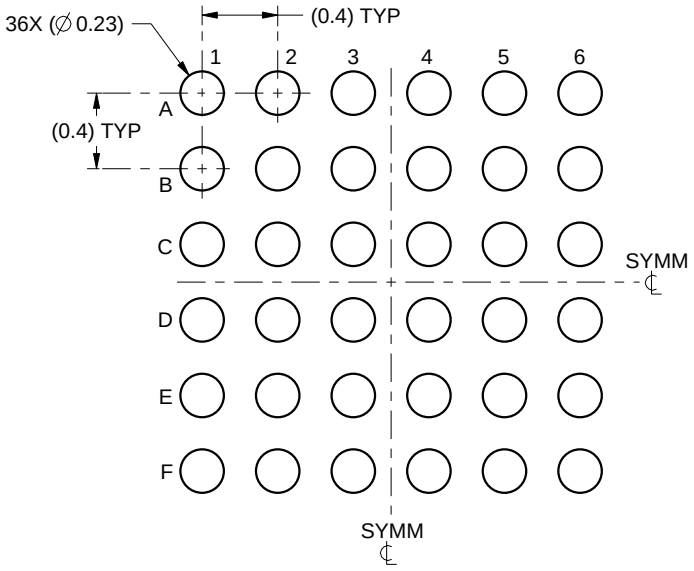
DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY

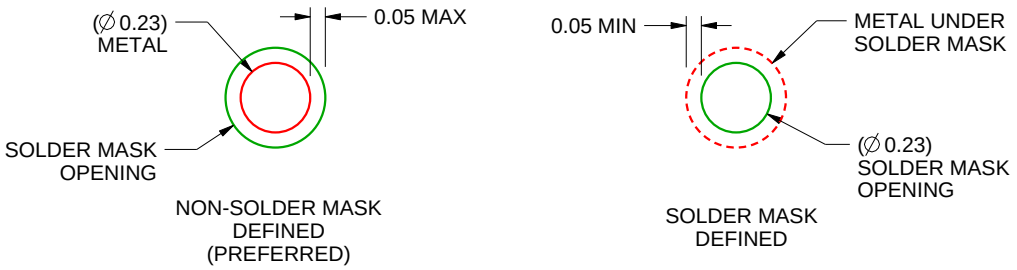


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS
NOT TO SCALE

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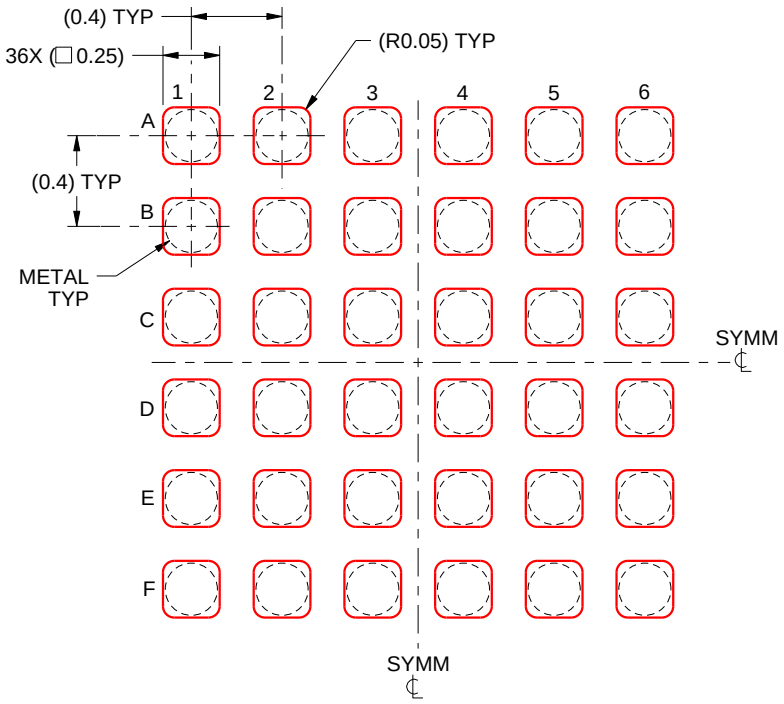
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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