

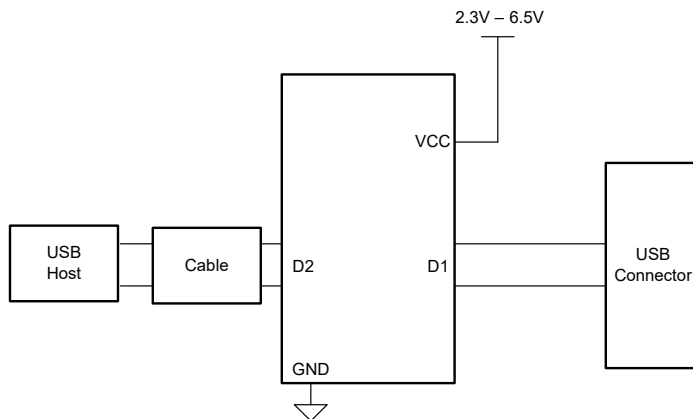
TUSB211A-Q1 車載向け、USB 2.0 480Mbps 高速シグナルコンディショナ

1 特長

- 車載アプリケーション向けに AEC-Q100 認定済み
 - デバイス温度グレード 2 : -40°C ~ 105°C
- 広い電源電圧範囲 : 2.3 ~ 6.5V
- USB 切断時およびシャットダウン時の非常に低い消費電力
- USB 2.0 High-Speed 信号のコンディショニングを提供
- USB 2.0、OTG 2.0、BC 1.2 に対応
- Low-Speed、Full-Speed、High-Speed 信号処理のサポート
- 特定のホストやデバイスに非依存
- 最大 5m のケーブル長をサポート
 - 外付けのプルダウン抵抗により 4 つの信号 EQ (エッジブーストと DC ブースト) 設定を選択可能
- 2 つの TUSB211A-Q1 デバイスを使って最大 10m のケーブル長に対応
- スケーラブルなソリューション - 損失が大きいアプリケーションに対応するため、デバイスをダイジーチェーン接続可能
- TUSB211、212、214、216、217A (3.3V) とピン互換

2 アプリケーション

- 車載用インフォテインメントおよびクラスタ
- 車載ヘッドユニット
- アクティブケーブル、延長ケーブル、バックプレーン



概略回路図

3 概要

TUSB211A-Q1 は第 3 世代 USB™ 2.0 High Speed シグナルコンディショナで、伝送チャネルでの AC 損失 (容量性負荷による) および DC 損失 (抵抗損失による) を補償するように設計されています。

TUSB211A-Q1 には、エッジブースタにより USB 2.0 High Speed 信号の遷移エッジを高速化し、DC ブースト機能により静的電圧レベルを上げる特許取得済みの設計が採用されています。

また、TUSB211A-Q1 はプリイコライゼーション機能を備えているため、長いケーブルを使用するアプリケーションで ISI (符号間干渉) ジッタを補償できます。USB Low Speed および Full Speed 信号特性は、TUSB211A-Q1 による影響を受けません。

TUSB211A-Q1 は、パケットタイミングの変更も伝搬遅延またはレイテンシの追加もせずに信号品質を向上させることができます。

TUSB211A-Q1 により、最長 5 メートルのケーブルを使用したシステムで、USB 2.0 High Speed 近端アイコンプライアンスに合格することが可能になります。

TUSB211A-Q1 は、USB On-The-Go (OTG) および Battery Charging (BC) プロトコルにも対応しています。

デバイスの比較

| 部品番号 | パッケージ (1) | 動作温度 (T _A) °C |
|-------------|-----------------|---------------------------|
| TUSB211A | RWB (X2QFN, 12) | 0 ~ 70 |
| TUSB211AI | | -40 ~ 85 |
| TUSB211A-Q1 | | -40 ~ 105 |

パッケージ情報

| 部品番号 | パッケージ (1) | パッケージサイズ (2) |
|-------------|-----------------|---------------|
| TUSB211A-Q1 | RWB (X2QFN, 12) | 1.6mm × 1.6mm |

(1) 詳細については、[セクション 10](#) を参照してください。

(2) パッケージサイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



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4 Pin Configuration and Functions

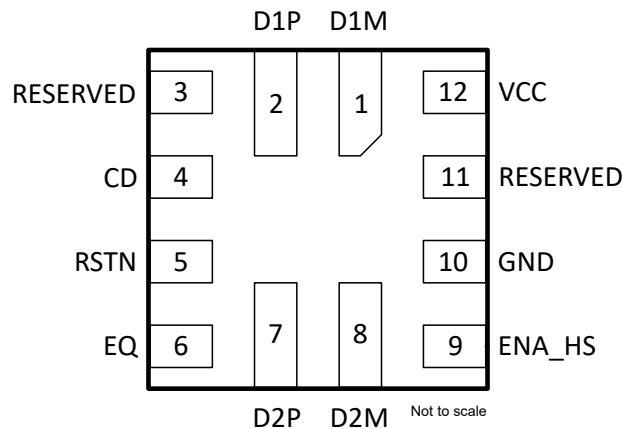


図 4-1. TUSB211A-Q1 RWB 12-Pin X2QFN (Top View)

表 4-1. Pin Functions

| PIN | | TYPE ⁽¹⁾ | INTERNAL PULLUP/PULLDOWN | DESCRIPTION |
|----------|-----|---------------------|--|--|
| NAME | NO. | | | |
| EQ | 6 | I | N/A | USB High-speed EQ select via external pull down resistor. Both edge boost and DC boost are controlled by a single pin. Sampled upon power up. Does not recognize real time adjustments. Auto selects EQ LEVEL = 3 when left floating. |
| RESERVED | 11 | I | 500kΩ PU | Reserved pin for TI test purposes. Leave floating or connect external capacitor to GND for normal operation. |
| ENA_HS | 9 | I/O | N/A | After reset: Output signal ENA_HS. Flag indicating that channel is in High-speed mode. Asserted upon: 1. Detection of USB-IF High-speed test fixture from an unconnected state followed by transmission of USB TEST_PACKET pattern. 2. Squelch detection following USB reset with a successful HS handshake [HS handshake is declared to be successful after single chirp J chirp K pair where each chirp is within 18μs – 128μs]. |
| D2P | 7 | I/O | N/A | USB High-speed positive port. |
| D2M | 8 | I/O | N/A | USB High-speed negative port. |
| GND | 10 | P | N/A | Ground |
| D1M | 1 | I/O | N/A | USB High-speed negative port. |
| D1P | 2 | I/O | N/A | USB High-speed positive port. |
| RESERVED | 3 | I/O | 500kΩ PU 1.8 MΩ PD | Reserved pin for TI test purposes. Leave floating for normal operation. |
| VCC | 12 | P | N/A | Supply power |
| RSTN | 5 | I | 500kΩ PU 1.8 MΩ PD | Device disable/enable. Low – Device is at reset and in shutdown, and High - Normal operation. Recommend 0.1μF external capacitor to GND to allow for clean power on reset if not driven. If the pin is driven, it must be held low until the supply voltage for the device reaches within specifications. |
| CD | 4 | O | When RSTN asserted there is a 500kΩ PD | After reset: Output CD. Flag indicating that a USB device is attached (connection detected). Asserted from an unconnected state upon detection of DP or DM pull-up resistor. De-asserted upon detection of disconnect. |

(1) I = input, O = output, P = power

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

| | | MIN | MAX | UNIT |
|--|----------|------|------|------|
| Supply voltage range | VCC | -0.3 | 7 | V |
| Voltage range USB data | DxP, DxM | -0.3 | 5.5 | V |
| Voltage range on EQ pin | EQ | -0.3 | 1.98 | V |
| Voltage range other pins | RSTN | -0.3 | 5.5 | V |
| Storage temperature, T_{stg} | | -65 | 150 | °C |
| Maximum junction temperature, $T_{J(max)}$ | | | 125 | °C |

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

| | | | VALUE | UNIT |
|-------------|-------------------------|---|-------|------|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 ⁽¹⁾ | ±2000 | V |
| | | Charged-device model (CDM), per AEC Q100-011 ⁽²⁾ | ±750 | |

- (1) AEC Q100-002 HBM ESD Classification Level 2
(2) AEC Q100-011 CDM ESD Classification Level C4A

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|----------|---|-----|-----|------|------|
| V_{CC} | Supply voltage | 2.3 | 5 | 6.5 | V |
| T_A | Operating free-air temperature (AEC-Q100) | -40 | | 105 | °C |
| T_J | Junction temperature (AEC-Q100) | | | 115 | °C |
| DxP, DxM | Voltage range USB data | 0 | | 3.6 | V |
| EQ | Voltage range EQ pin | 0 | | 1.98 | V |
| DIGITAL | Voltage range other pins (RSTN) | 0 | | 3.6 | V |

5.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | RWB (X2QFN) | UNIT |
|-------------------------------|--|-------------|------|
| | | 12 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 137.4 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 62 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 67.2 | °C/W |
| ψ_{JT} | Junction-to-top characterization parameter | 1.9 | °C/W |
| ψ_{JB} | Junction-to-board characterization parameter | 67.3 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

5.5 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|----------------------------|--|--|-----|--------------------|------|------|
| POWER | | | | | | |
| I _{ACTIVE_HS} | High Speed Active Current | USB channel = HS mode. 480Mbps traffic. V _{CC} supply stable, with EQ = Max | | 22 | 36 | mA |
| I _{IDLE_HS} | High Speed Idle Current | USB channel = HS mode, no traffic. V _{CC} supply stable, EQ = Max | | 22 | 36 | mA |
| I _{HS_SUSPEND} | High Speed Suspend Current | USB channel = HS Suspend mode. V _{CC} supply stable | | 0.75 | 1.4 | mA |
| I _{FS} | Full-Speed Current | USB channel = FS mode, 12Mbps traffic, V _{CC} supply stable | | 0.75 | 1.4 | mA |
| I _{DISCONN} | Disconnect Power | Host side application. No device attachment. | | 0.80 | 1.4 | mA |
| I _{SHUTDOWN} | Shutdown Power | RSTN driven low, V _{CC} supply stable | | 60 | 115 | μA |
| CONTROL PIN LEAKAGE | | | | | | |
| I _{LKG_FS} | Pin failsafe leakage current for RSTN | V _{CC} = 0V, pin at V _{IH, max} | | 10 | 15 | μA |
| INPUT RSTN | | | | | | |
| V _{IH} | High level input voltage | | 1.5 | | 3.6 | V |
| V _{IL} | Low-level input voltage | | 0 | | 0.5 | V |
| I _{IH} | High level input current | V _{IH} = 3.6V, R _{PU} enabled | | | ±15 | μA |
| I _{IL} | Low level input current | V _{IL} = 0V, R _{PU} enabled | | | ±20 | μA |
| INPUT EQ | | | | | | |
| R _{EQ_LVL0} | External pulldown resistor for EQ Level 0 | | | | 160 | Ω |
| R _{EQ_LVL1} | External pulldown resistor for EQ Level 1 | | 1.5 | 1.8 | 2 | kΩ |
| R _{EQ_LVL2} | External pulldown resistor for EQ Level 2 | | 3.4 | 3.6 | 3.96 | kΩ |
| R _{EQ_LVL3} | External pulldown resistor for EQ Level 3 to remove upper limit for resistor value, can be left open | | 7.5 | | | kΩ |
| OUTPUTS CD, ENA_HS | | | | | | |
| V _{OH} | High level output voltage for CD and ENA_HS | I _O = -50μA, V _{CC} ≥ 3.0V | 2.5 | | | V |
| V _{OH} | High level output voltage for CD | I _O = -25μA, V _{CC} = 2.3V | 1.7 | | | V |
| V _{OH} | High level output voltage for ENA_HS | I _O = -25μA, V _{CC} = 2.3V | 1.8 | | | V |
| V _{OL} | Low level output voltage for CD and ENA_HS | I _O = 50μA | | | 0.3 | V |
| DxP, DxM | | | | | | |
| C _{IO_DXX} | Capacitance to GND | Measured with VNA at 240MHz, V _{CC} supply stable, Redriver off | | 2.5 | | pF |

(1) All typical values are at V_{CC} = 5V, and T_A = 25°C.

5.6 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|-----------------------------|----------------|---|-----|--------------------|-----|------|
| DxP, DxM USB Signals | | | | | | |
| F _{BR_DXX} | Bit Rate | USB channel = HS mode. 480Mbps traffic. V _{CC} supply stable | | | 480 | Mbps |
| t _{R/F_DXX} | Rise/Fall time | | 100 | | | ps |

(1) All typical values are at V_{CC} = 5V, and T_A = 25°C.

5.7 Timing Requirements

| | | MIN | NOM | MAX | UNIT |
|------------------------|--|-----|-----|-----|---------|
| POWER UP TIMING | | | | | |
| T_{RSTN_PW} | Minimum width to detect a valid RSTN signal assert when the pin is actively driven low | 100 | | | μ s |
| T_{STABLE} | VCC must be stable before RSTN de-assertion | 300 | | | μ s |
| T_{READY} | Maximum time needed for the device to be ready after RSTN is de-asserted. | | | 500 | μ s |
| T_{RAMP} | V_{CC} ramp time | | | 100 | ms |
| T_{RAMP} | V_{CC} ramp time | 0.2 | | | ms |

5.8 Typical Characteristics

The typical characteristics shown in this section apply to near-end eye measurements taken at nominal conditions. The eyes are measured with various pre-channel cable lengths applied at the input or post-channel cable lengths applied at the output of the TUSB211A-Q1 as indicated.

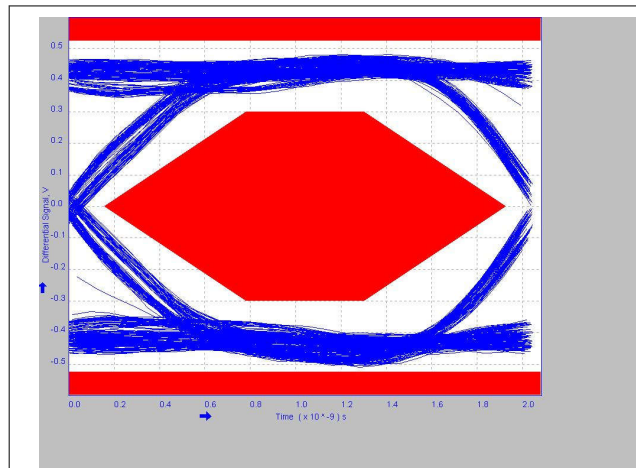


図 5-1. 2 Meter Pre-Channel With TUSB211A-Q1 EQ=1

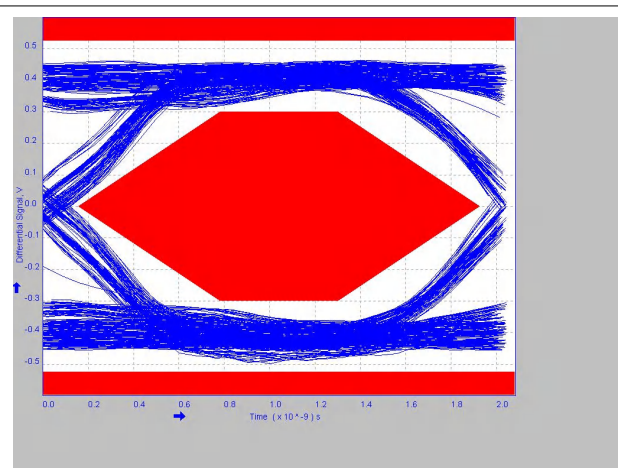


図 5-2. 5 Meter Pre-Channel With TUSB211A-Q1 EQ=2

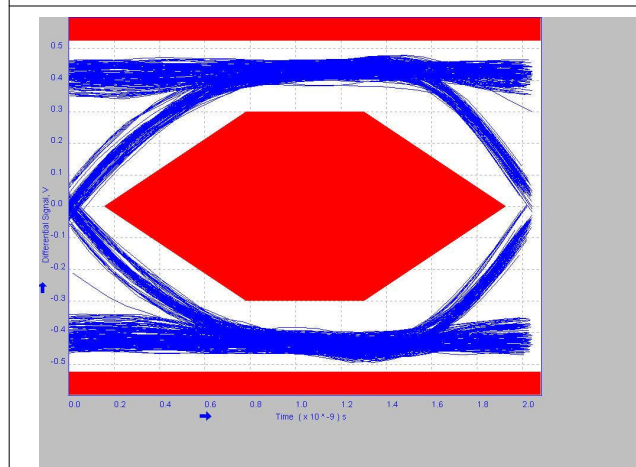


図 5-3. 2 Meter Post-Channel With TUSB211A-Q1 EQ=1

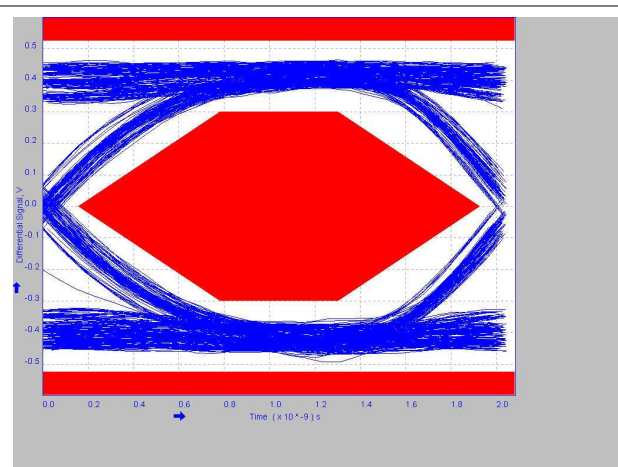


図 5-4. 4 Meter Post-Channel With TUSB211A-Q1 EQ=2

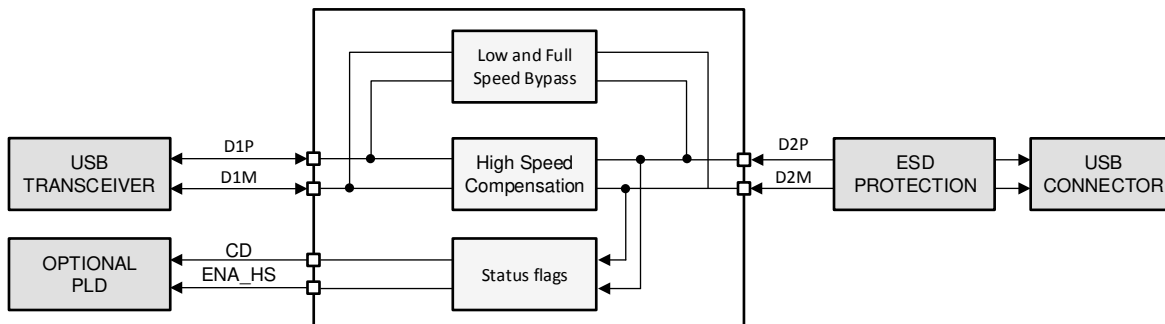
6 Detailed Description

6.1 Overview

The TUSB211A-Q1 is a USB High-Speed (HS) signal conditioner designed to compensate for ISI signal loss in a transmission channel. TUSB211A-Q1 has a patented design for USB Low Speed (LS) and Full Speed (FS) signals. It does not alter the signal characteristics. HS signals are compensated. The design is compatible with USB On-The-Go (OTG) and Battery Charging (BC) specifications.

Programmable signal gain through an external resistor permits fine tuning device performance to optimize signals. This helps pass USB HS electrical compliance tests at the connector. The TUSB211A-Q1 allows application in series to cover longer distances, or high loss transmission paths. A maximum of 4 devices can be daisy-chained.

6.2 Functional Block Diagram



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6.3 Feature Description

6.3.1 High-Speed EQ

The high-speed EQ (combination of edge boost and DC boost) improves the eye width for USB2.0 high-speed signals. It is direction independent, which makes it compatible to OTG systems. The EQ pin is configuring the EQ strength with different values of pull down resistors to set 4 levels of EQ.

6.4 Device Functional Modes

6.4.1 Low-Speed (LS) Mode

TUSB211A-Q1 automatically detects an LS connection and does not enable signal compensation. CD pin is asserted high but ENA_HS will be low.

6.4.2 Full-Speed (FS) Mode

TUSB211A-Q1 automatically detects an FS connection and does not enable signal compensation. CD pin is asserted high but ENA_HS will be low.

6.4.3 High-Speed (HS) Mode

TUSB211A-Q1 automatically detects an HS connection and will enable signal compensation as determined by the external pull down resistance on its EQ pin.

CD pin and ENA_HS pin are asserted high when high-speed EQ is active.

6.4.4 High-Speed Downstream Port Electrical Compliance Test Mode

TUSB211A-Q1 will detect an HS compliance test fixture and enter the downstream port high-speed eye diagram test mode. CD pin will be low and ENA_HS pin is asserted high when TUSB211A-Q1 is in HS eye compliance test mode.

If the RSTN pin is asserted low and de-asserted high while TUSB211A-Q1 is operating in HS functional mode, then TUSB211A-Q1 will transition to HS eye compliance test mode, the CD asserts low, and ENA_HS remains high. When all this occurs, signal compensation is enabled.

6.4.5 Shutdown Mode

TUSB211A-Q1 can be disabled when its RSTN pin is asserted low. DP, DM traces are continuous through the device in shutdown mode. The USB channel is still fully operational, but there is neither signal compensation, nor any indication from the CD pin as to the status of the channel.

表 6-1. CD and ENA_HS Pins in Different Modes

| MODE | CD | ENA_HS |
|--|------|--------|
| Low-speed | HIGH | LOW |
| Full-speed | HIGH | LOW |
| High-speed | HIGH | HIGH |
| High-speed downstream port electrical test | LOW | HIGH |
| Shutdown | LOW | LOW |

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

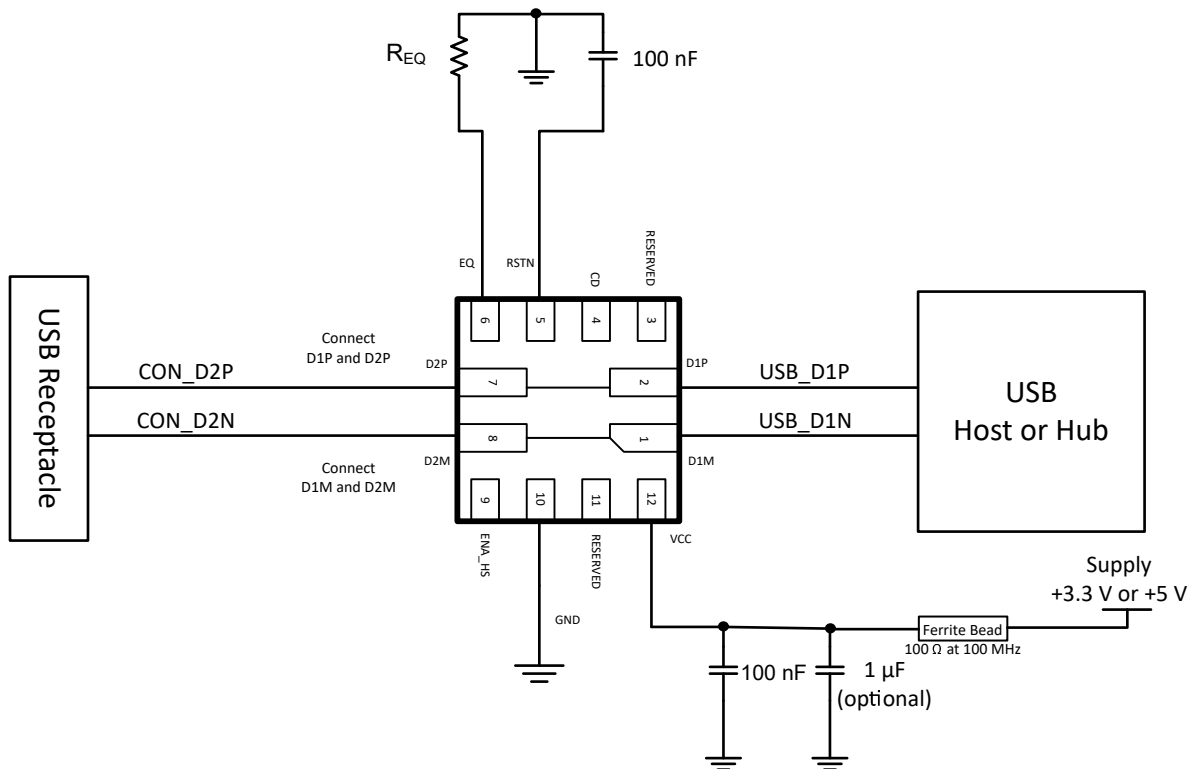
7.1 Application Information

The purpose of the TUSB211A-Q1 is to restore the signal integrity of a USB High-speed channel up to the USB connector. The loss in signal quality stems from reduced channel bandwidth due to high loss PCB trace and other components that contribute a capacitive load. This can cause the channel to fail the USB near end eye mask. Proper use of the TUSB211A-Q1 can help to pass this eye mask.

A secondary purpose is to use the CD pin of the TUSB211A-Q1 to control other blocks on the customer platform, if so desired.

7.2 Typical Application

A typical application for TUSB211A-Q1 is shown in [Figure 7-1](#). In this setup, D2P and D2M face the USB connector while D1P and D1M face the USB host. The orientation may be reversed [that is, D2 faces transceiver and D1 faces connector].



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Figure 7-1. TUSB211A-Q1 Reference Schematic

7.2.1 Design Requirements

TUSB211A-Q1 requires a valid reset signal as described in the *Power Supply Recommendations* section. The capacitor at RSTN pin is not required if a micro controller drives the RSTN pin according to recommendations.

For this design example, use the parameters provided in 表 7-1.

表 7-1. Design Parameters for 3.3V Supply With Low to Medium Loss System

| PARAMETER | | VALUE ⁽¹⁾ |
|--|-----------------------|-------------------------------------|
| V _{CC} | | 3.3V ±10% |
| I ² C support required in system (Yes/No) | | No |
| Edge and DC Boost | R_{EQ} | EQ Level |
| | 0Ω | 0 |
| | 1.8kΩ ±1% | 1 |
| | 3.6kΩ ±1% | 2 |
| Do Not Install (DNI) | | 3 |
| | | EQ Level 0: R _{EQ} = 0Ω |

(1) These parameters are starting values for a low to medium loss system. Further tuning might be required based on specific host or device as well as cable length and loss profile. These settings are not specific to a 3.3V supply system and could be applicable to 5V supply system as well.

7.2.2 Detailed Design Procedure

The best EQ setting is dependent upon the signal chain loss characteristics of the target platform. The recommendation is to start with EQ Level 0, and then increment to EQ Level 1, and so on.

For the TUSB211A-Q1 to recognize any change to the EQ setting, the RSTN pin must be toggled. This is because the EQ pin is latched on power up and the pin is ignored thereafter.

Placement of the device is also dependent on the application goal. 表 7-2 provides TI recommendations.

表 7-2. Platform Placement Guideline

| PLATFORM GOAL | SUGGESTED TUSB211A-Q1 PLACEMENT |
|---|--|
| Pass USB Near End Mask at the receptacle | Close to measurement point (connector) |
| Pass USB Far End Eye Mask at the plug | Close to USB PHY |
| Cascade multiple TUSB211A-Q1s to improve device enumeration | Midway between each USB interconnect |

表 7-3. Table of Recommended Settings

| EQ settings ⁽¹⁾ for channel loss | |
|---|---------|
| Pre-channel cable length (Between USB PHY and TUSB211A-Q1) | EQ |
| 0-3 meter | Level 0 |
| 2-5 meter | Level 1 |
| Post-channel cable length (Between TUSB211A-Q1 and inter-connect) | EQ |
| 0-2 meter | Level 0 |
| 1-4 meter | Level 1 |

(1) These parameters are starting values for different cable lengths. Further tuning might be required based on specific host or device as well as cable length and loss profile.

7.2.2.1 Test Procedure to Construct USB High-Speed Eye Diagram

注

USB-IF certification tests for High-speed eye masks require the *mandated use* of the USB-IF developed test fixtures. These test fixtures do not require the use of oscilloscope probes. Instead they use SMA cables. More information can be found at the USB-IF Compliance Updates Page. It is located under the *Electrical Specifications* section, ID 86 dated March 2013.

The following procedure must be followed before using any oscilloscope compliance software to construct a USB High-speed Eye Mask:

7.2.2.1.1 For a Host Side Application

1. Configure the TUSB211A-Q1 to the desired EQ setting.
2. Power on (or toggle the RSTN pin if already powered on) the TUSB211A-Q1.
3. Using SMA cables, connect the oscilloscope and the USB-IF host-side test fixture to the TUSB211A-Q1.
4. Enable the host to transmit USB TEST_PACKET.
5. Execute the oscilloscope USB compliance software.
6. Repeat the above steps to re-test TUSB211A-Q1 with a different EQ setting (must reset to change).

7.2.2.1.2 For a Device Side Application

1. Configure the TUSB211A-Q1 to the desired EQ setting.
2. Power on (or toggle the RSTN pin if already powered on) the TUSB211A-Q1.
3. Connect a USB host, the USB-IF device-side test fixture, and USB device to the TUSB211A-Q1. Ensure that the USB-IF device test fixture is configured to the 'INIT' position.
4. Allow the host to enumerate the device.
5. Enable the device to transmit USB TEST_PACKET.
6. Using SMA cables, connect the oscilloscope to the USB-IF device-side test fixture and ensure that the device-side test fixture is configured to the 'TEST' position.
7. Execute the oscilloscope USB compliance software.
8. Repeat the above steps to re-test TUSB211A-Q1 with a different EQ setting (must reset to change).

7.2.3 Application Curves

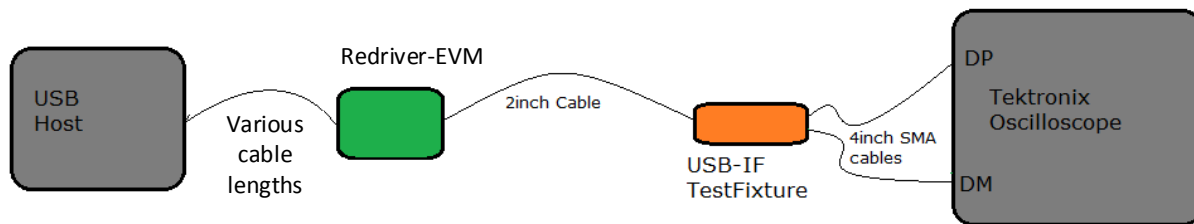


図 7-2. Near End Eye Measurement Set-Up With Pre-Channel Cable

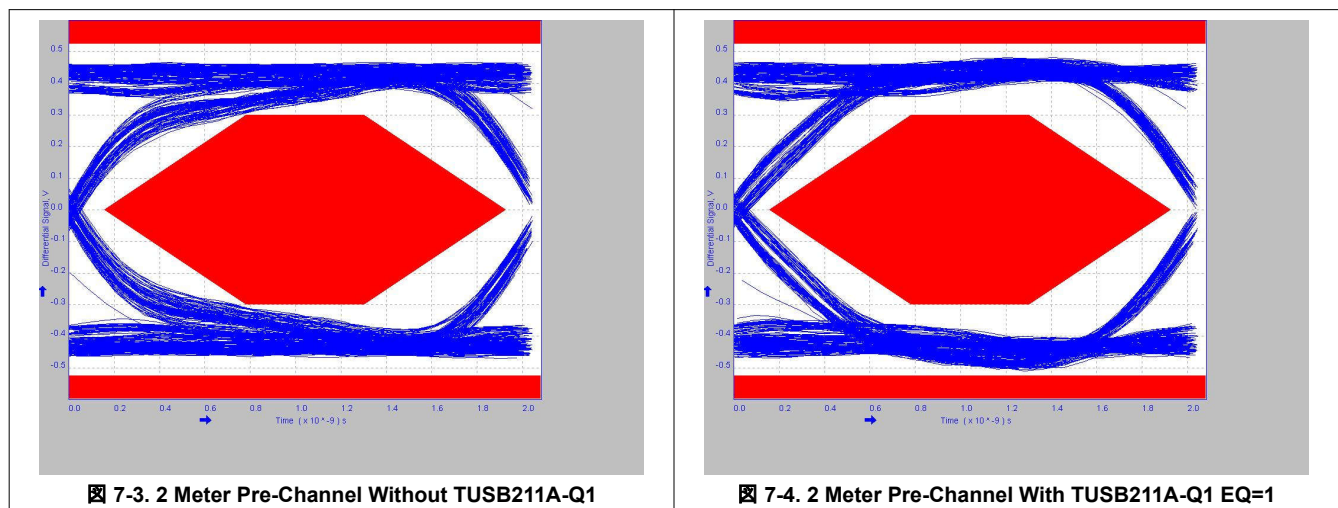


図 7-3. 2 Meter Pre-Channel Without TUSB211A-Q1

図 7-4. 2 Meter Pre-Channel With TUSB211A-Q1 EQ=1

7.2.3 Application Curves (continued)

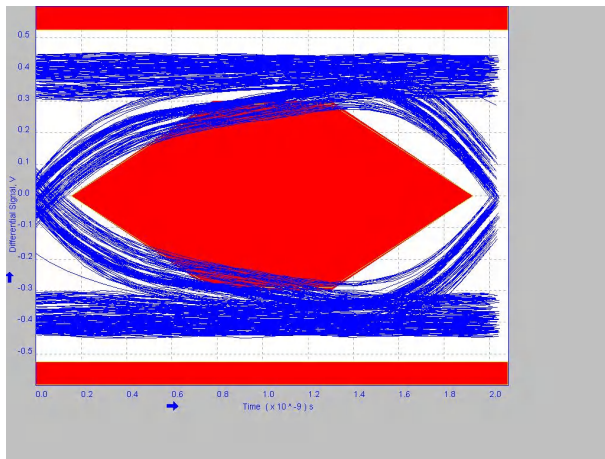


図 7-5. 5 Meter Without TUSB211A-Q1

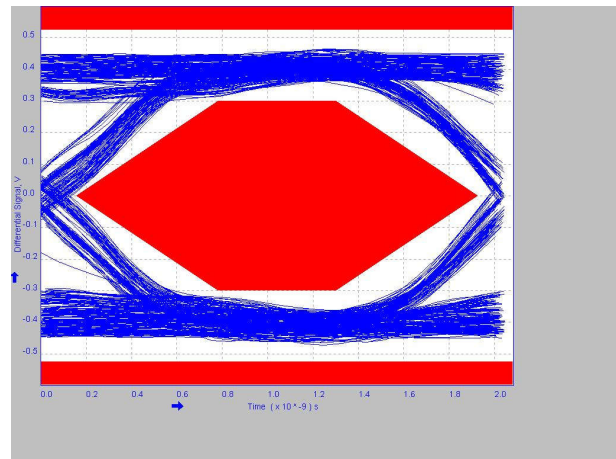


図 7-6. 5 Meter Pre-Channel With TUSB211A-Q1 EQ=1

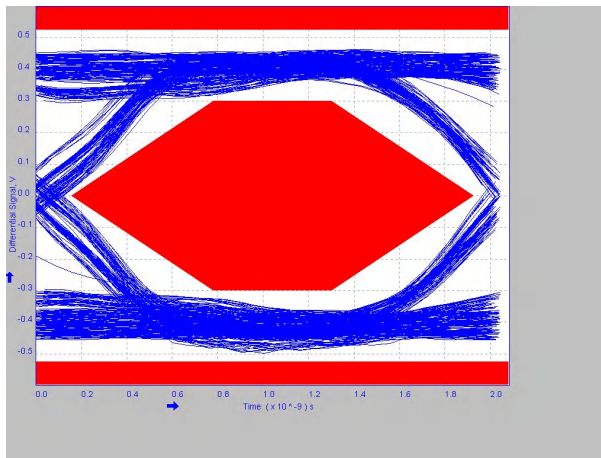


図 7-7. 5 Meter Pre-Channel With TUSB211A-Q1 EQ=2

7.2.3 Application Curves (continued)

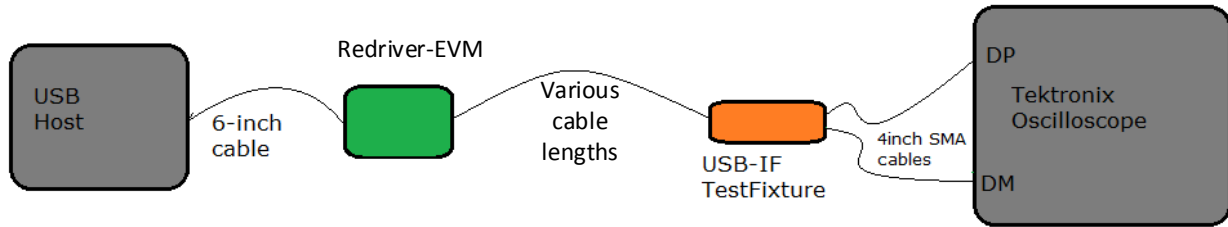


図 7-8. Near End Eye Measurement Set-Up With Post-Channel Cable

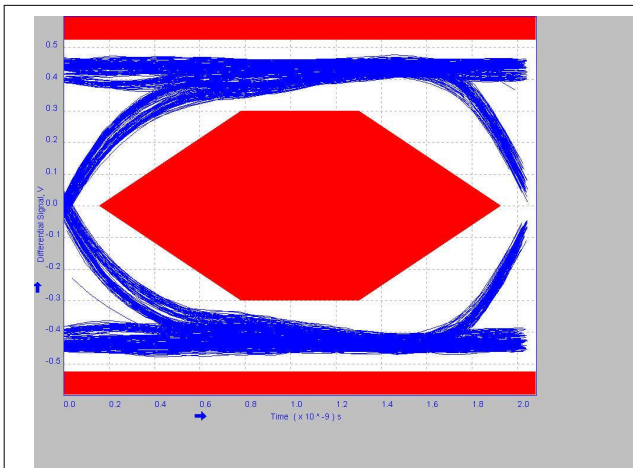


図 7-9. 1 Meter Post-Channel Without TUSB211A-Q1

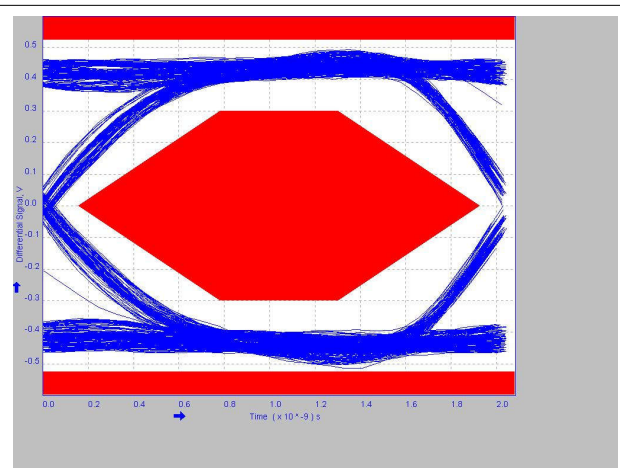


図 7-10. 1 Meter Post-Channel With TUSB211A-Q1 EQ=0

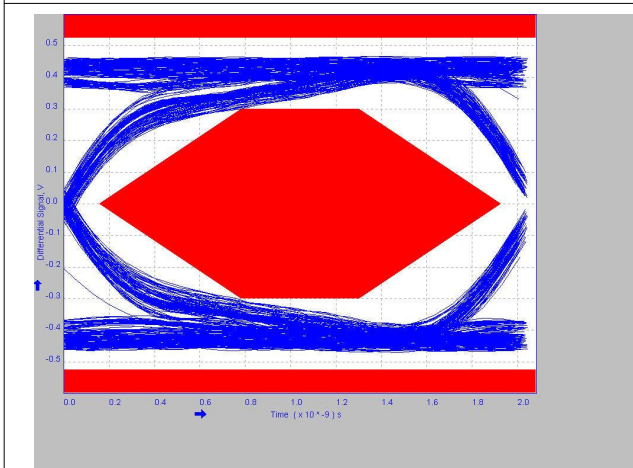


図 7-11. 2 Meter Post-Channel Without TUSB211A-Q1

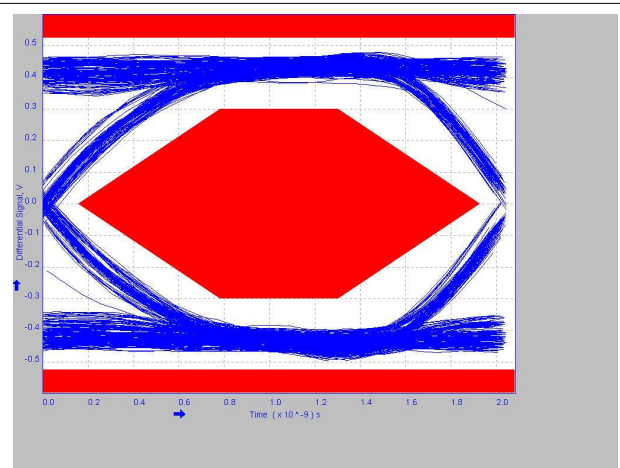


図 7-12. 2 Meter Post-Channel With TUSB211A-Q1 EQ=1

7.2.3 Application Curves (continued)

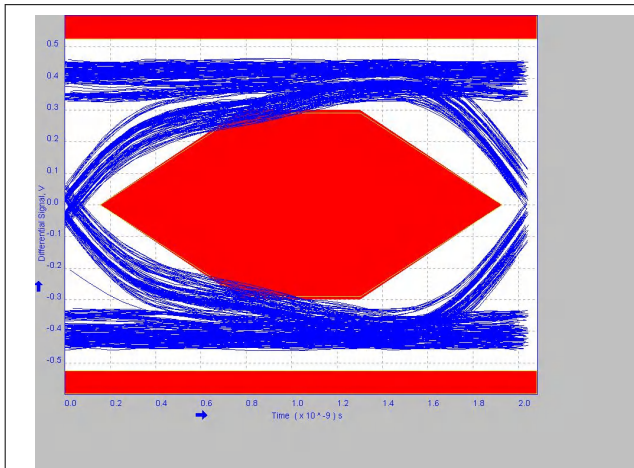


図 7-13. 4 Meter Post-Channel Without TUSB211A-Q1

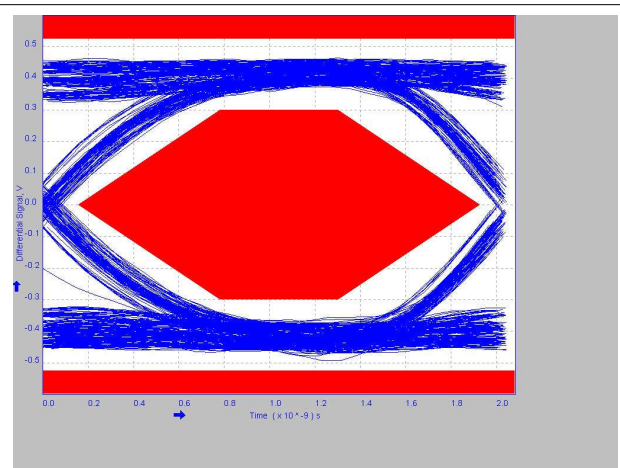


図 7-14. 4 Meter Post-Channel With TUSB211A-Q1 EQ=2

7.3 Power Supply Recommendations

On power up, the interaction of the RSTN pin and power on ramp could result in digital circuits not being set correctly. The device should not be enabled until the power on ramp has settled to the minimum recommended supply voltage or higher for a correct power on reset of the digital circuitry. If RSTN cannot be held low by the microcontroller or other circuitry until the power on ramp has settled, then an external capacitor from the RSTN pin to GND is required to hold the device in the low power reset state.

The RC time constant should be larger than five times of the power on ramp time (0 to V_{CC}). With a typical internal pullup resistance of 500k Ω , the recommended minimum external capacitance is calculated as:

$$[Ramp\ Time \times 5] \div [500\ k\Omega] \tag{1}$$

7.4 Layout

7.4.1 Layout Guidelines

Although the land pattern has matched trace width to pad width, optimal impedance control is based on the user's own PCB stack-up. The recommendation is to maintain 90 Ω differential routing underneath the device.

7.4.2 Layout Example

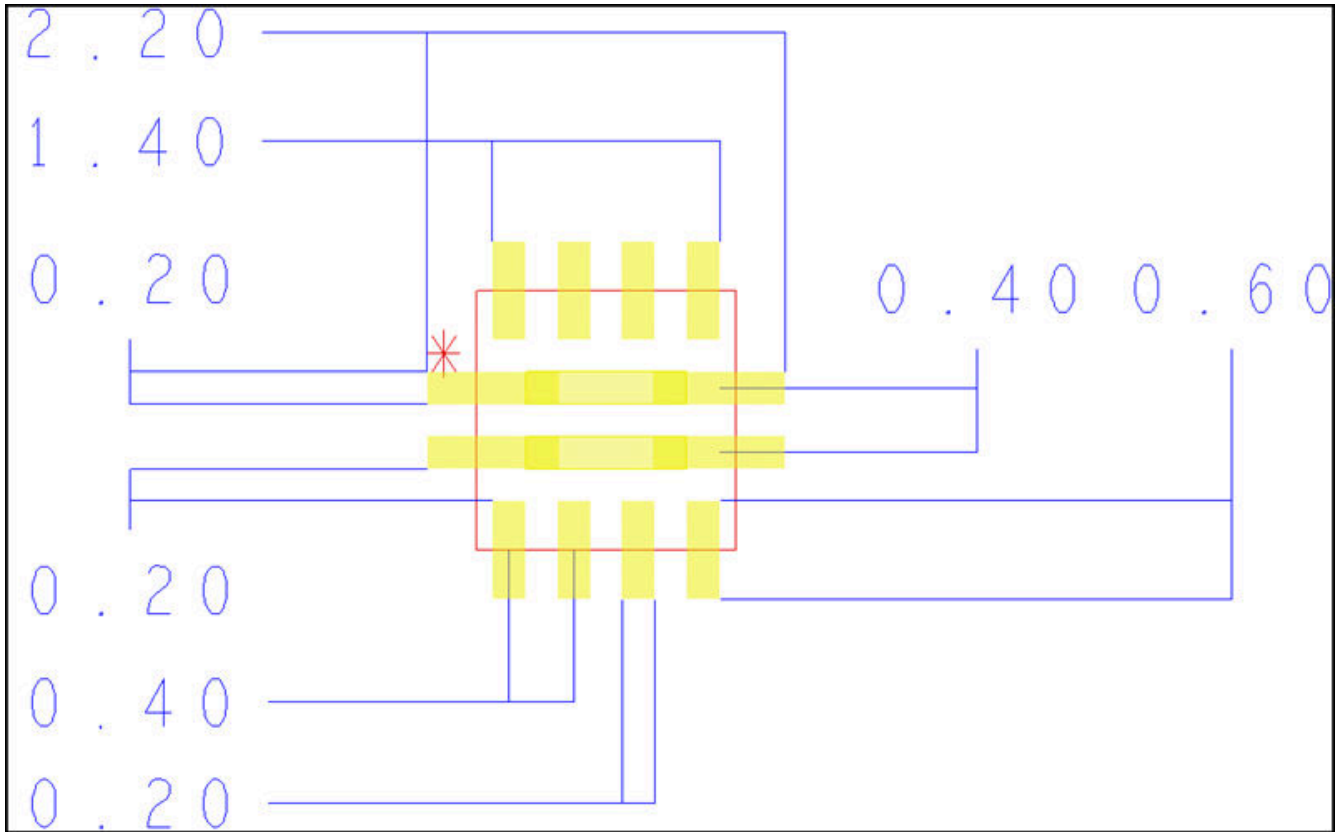


図 7-15. DP and DM Routing Underneath Device Package

8 Device and Documentation Support

8.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。
[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.2 サポート・リソース

[テキサス・インスツルメンツ E2E™ サポート・フォーラム](#) は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

| DATE | REVISION | NOTES |
|---------------|----------|-----------------|
| February 2024 | * | Initial Release |

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TUSB211ARWBRQ1 | ACTIVE | X2QFN | RWB | 12 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | 1Q | Samples |
| TUSB211ARWBTQ1 | ACTIVE | X2QFN | RWB | 12 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | 1Q | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

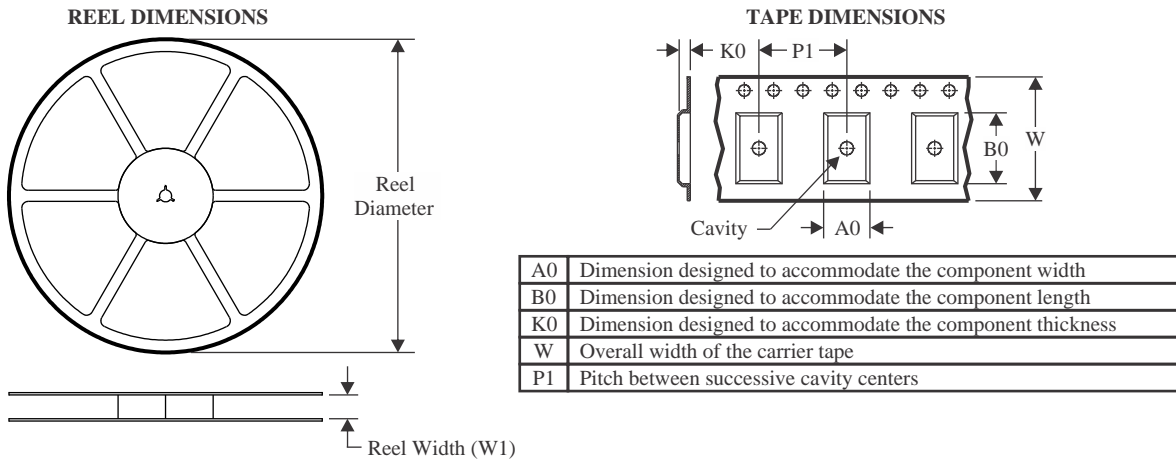
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

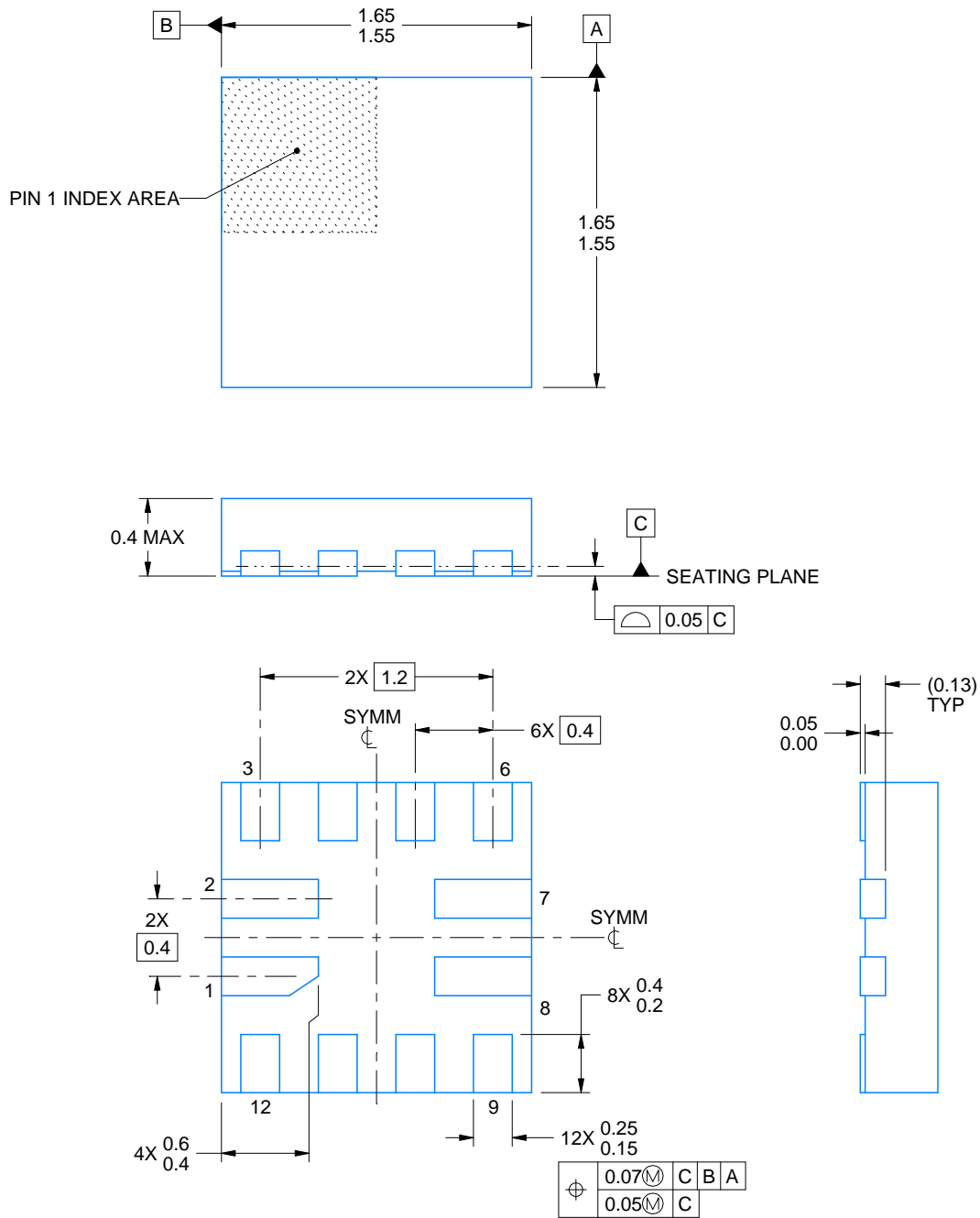
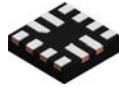

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TUSB211ARWBRQ1 | X2QFN | RWB | 12 | 3000 | 180.0 | 9.5 | 1.8 | 1.8 | 0.45 | 4.0 | 8.0 | Q1 |
| TUSB211ARWBTQ1 | X2QFN | RWB | 12 | 250 | 180.0 | 9.5 | 1.8 | 1.8 | 0.45 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TUSB211ARWBRQ1 | X2QFN | RWB | 12 | 3000 | 189.0 | 185.0 | 36.0 |
| TUSB211ARWBTQ1 | X2QFN | RWB | 12 | 250 | 189.0 | 185.0 | 36.0 |



4221631/B 07/2017

NOTES:

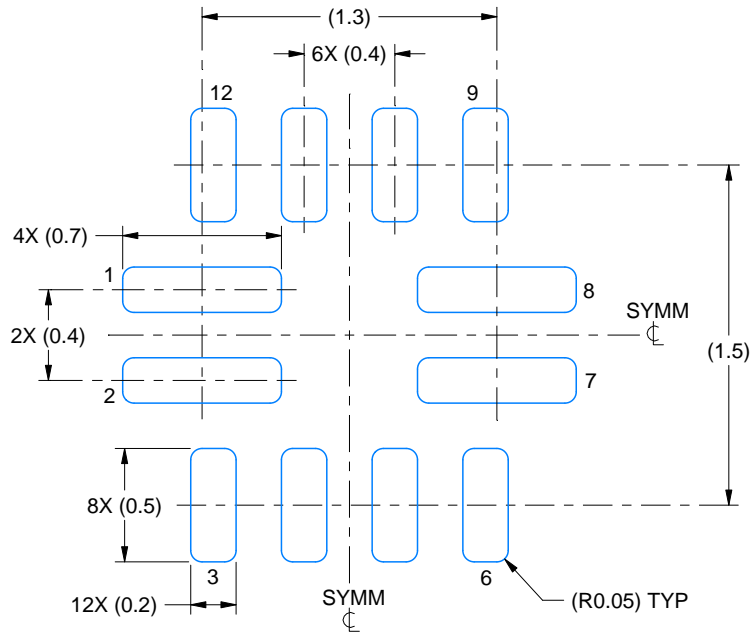
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

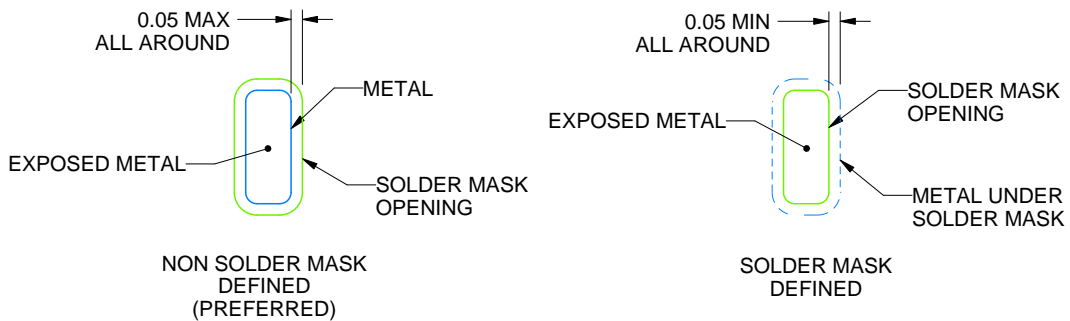
RWB0012A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDER MASK DETAILS

4221631/B 07/2017

NOTES: (continued)

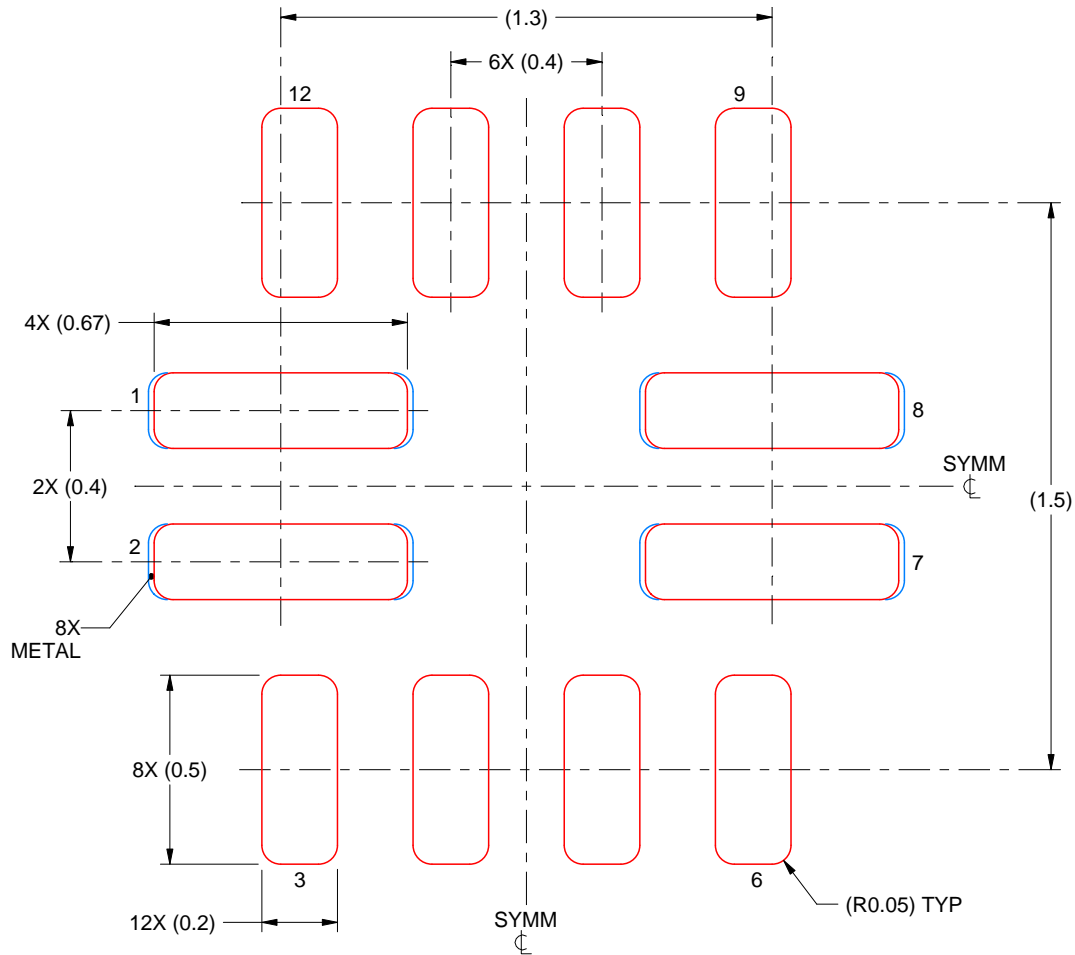
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RWB0012A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
PADS 1,2,7 & 8
96% PRINTED SOLDER COVERAGE BY AREA
SCALE:50X

4221631/B 07/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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