

TXS0102V-Q1 オープンドレインおよびプッシュプルアプリケーション向け 車載用 2 ビット双方向レベルシフト電圧トランスレータ

1 特長

- 車載アプリケーション認定済み
- 以下の結果で AEC-Q100 認定済み:
 - デバイス温度グレード 1: 動作時周囲温度範囲 $-40^{\circ}\text{C} \sim 125^{\circ}\text{C}$
 - デバイス HBM ESD 分類レベル 2
 - デバイス CDM ESD 分類レベル C5
- JESD 22 に準拠した ESD 保護:
 - A ポート:
 - 2000V、人体モデル (A114-B)
 - 500V、デバイス帯電モデル (C101)
 - B ポート:
 - 5000V、人体モデル (A114-B)
 - 500V、デバイス帯電モデル (C101)
- 方向制御信号不要
- 最大データレート:
 - 24Mbps (プッシュプル)
 - 2Mbps (オープンドレイン)
- テキサス・インスツルメンツの NanoStar™ 集積回路パッケージで提供
- 1.65V~3.6V (A ポート)、2.3V~5.5V (B ポート) ($V_{\text{CCA}} \leq V_{\text{CCB}}$)
- V_{CC} 絶縁機能: いずれかの V_{CC} 入力がある GND レベルになると、両方のポートが高インピーダンス状態に移行
- 電源投入のシーケンス不要: V_{CCA} または V_{CCB} のいずれかが最初に立ち上げ可能
- I_{off} により部分的パワーダウン モードでの動作をサポート
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能

2 アプリケーション

- I²C/SMBus
- UART
- GPIO

3 概要

この 2 ビット非反転トランスレータは、双方向の電圧レベルトランスレータであり、これを使用してデジタル スイッチングを確立することにより、動作電圧が混在するシステムへの対応が可能になります。設定可能な 2 本の独立した電源レールを採用しており、1.65V~3.6V の動作電圧に対応する A ポートは V_{CCA} 電源に追従し、2.3V~5.5V の動作電圧に対応する B ポートは V_{CCB} 電源に追従します。このため高低いずれのロジック信号レベルにも対応し、1.8V、2.5V、3.3V、5V の任意の電圧ノード間で双方向変換が可能になります。

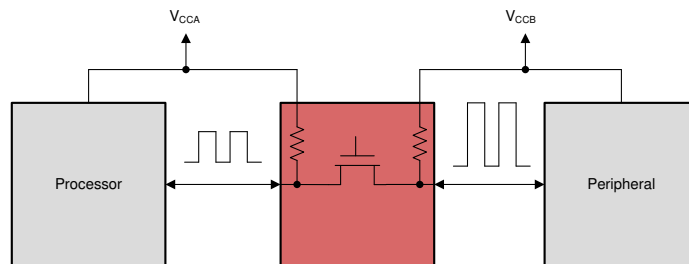
出力イネーブル(OE)入力を Low にすると、全 I/O がハイインピーダンス状態になるため、電源の静止電流を大幅に削減できます。

電源投入時または切断時にデバイスをハイインピーダンス状態にするには、OE をプルダウン抵抗で GND につなぐ必要があります。この抵抗の最小値は、ドライバの電流ソース能力によって決まります。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TXS0102V-Q1	DCU (VSSOP、8)	2mm × 3.1mm

- (1) 詳細については、[セクション 11](#) を参照してください。
- (2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



TXS0102V-Q1 の代表的なアプリケーション ブロック図



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4 Pin Configuration and Functions

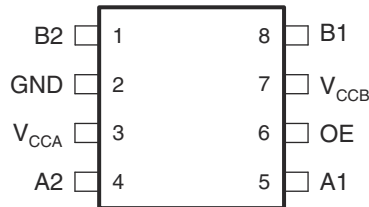


図 4-1. DCU Package, 8-Pin VSSOP (Top View)

表 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
A1	5	I/O	Input/output A. Referenced to V_{CCA} .
A2	4	I/O	Input/output A. Referenced to V_{CCA} .
B1	8	I/O	Input/output B. Referenced to V_{CCB} .
B2	1	I/O	Input/output B. Referenced to V_{CCB} .
GND	2	—	Ground
OE	6	I	Output enable (active High). Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA} .
V_{CCA}	3	P	A-port supply voltage. $1.65V \leq V_{CCA} \leq 3.6V$ and $V_{CCA} \leq V_{CCB}$
V_{CCB}	7	P	B-port supply voltage. $2.3V \leq V_{CCB} \leq 5.5V$

(1) I = input, O = output, I/O = input and output, P = power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CCA}	Supply voltage A		-0.5	4.6	V
V _{CCB}	Supply voltage B		-0.5	6.5	V
V _I	Input Voltage ⁽²⁾	I/O Ports (A Port)	-0.5	4.6	V
		I/O Ports (B Port)	-0.5	6.5	
V _O	Voltage applied to any output in the high-impedance or power-off state ⁽²⁾	A Port	-0.5	4.6	V
		B Port	-0.5	6.5	
V _O	Voltage applied to any output in the high or low state ^{(2) (3)}	A Port	-0.5	V _{CCA} + 0.5	V
		B Port	-0.5	V _{CCB} + 0.5	
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
I _O	Continuous output current			±50	mA
	Continuous current through V _{CC} or GND			±100	mA
T _J	Junction Temperature			150	°C
T _{stg}	Storage temperature		-65	150	°C

- (1) Stresses beyond those listed under [セクション 5.1](#) may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under [セクション 5.3](#). Exposure beyond the limits listed in [セクション 5.3](#) may affect device reliability.
- (2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The output positive-voltage rating may be exceeded up to 6.5 V maximum if the output current rating is observed.

5.2 ESD Ratings

			VALUE	UNIT	
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾	A Port	±2000	V
			B Port	±5000	
		Charged device model (CDM), per AEC Q100-011	A Port	±500	
			B Port	±500	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) ^{(1) (2) (3)}

			V _{CCA}	V _{CCB}	MIN	MAX	UNIT
V _{CCA}	Supply voltage A				1.65	3.6	V
V _{CCB}	Supply voltage B				2.3	5.5	V
V _{IH}	High-level input voltage	A-port I/O's	1.65 V to 1.95 V	2.3 V to 5.5 V	V _{CCI} - 0.2	V _{CCI}	V
			1.65 V to 3.6 V		V _{CCI} - 0.4	V _{CCI}	
		B-port I/O's	1.65 V to 3.6 V	2.3 V to 5.5 V	V _{CCI} - 0.4	V _{CCI}	
			OE Input		1.65 V to 3.6 V	V _{CCA} × 0.65	
V _{IL}	Low-level input voltage	A-port I/O's	1.65 V to 3.6 V	2.3 V to 5.5 V		0.15	V
		B-port I/O's	1.65 V to 3.6 V			0.15	
		OE Input	1.65 V to 3.6 V			V _{CCA} × 0.35	
Δt/Δv	Input transition rise and fall time	Push-Pull Driving	1.65 V to 3.6 V	2.3 V to 5.5 V		10	ns/V
T _A	Operating free-air temperature				-40	125	°C

- (1) V_{CCI} is the V_{CC} associated with the input port.
- (2) V_{CCO} is the V_{CC} associated with the output port.
- (3) All control inputs and data I/Os of this device have weak pulldowns to ensure the line is not floating when undefined external to the device. The input leakage from these weak pulldowns is defined by the I_I specification indicated under [セクション 5.5](#).

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TXS0102V-Q1	
		DCU	
		8 PINS	
			UNIT
R _{θJA}	Junction-to-ambient thermal resistance	239.8	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	88.5	°C/W
R _{θJB}	Junction-to-board thermal resistance	151.6	°C/W
Y _{JT}	Junction-to-top characterization parameter	30.9	°C/W
Y _{JB}	Junction-to-board characterization parameter	150.5	°C/W
R _{θJC(bottom)}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

PARAMETER		TEST CONDITIONS	V _{CCA}	V _{CCB}	Operating free-air temperature (T _A)						UNIT				
					25°C			-40°C to 85°C				-40°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX		MIN	TYP	MAX	
V _{OHA}	Port A output high voltage ⁽³⁾	I _{OH} = -20 μA	1.65 V to 3.6 V	2.3 V to 5.5 V	0.67 x V _{CC} A			0.67 x V _{CC} A			0.67 x V _{CC} A			V	
V _{OLA}	Port A output low voltage ⁽⁴⁾	I _{OL} = 1 mA	1.65 V to 3.6 V	2.3 V to 5.5 V	0.4			0.4			0.4			V	
V _{OHB}	Port B output high voltage		1.65 V to 3.6 V	2.3 V to 5.5 V	0.67 x V _{CC} B			0.67 x V _{CC} B			0.67 x V _{CC} B			V	
V _{OLB}	Port B output low voltage ⁽⁴⁾		1.65 V to 3.6 V	2.3 V to 5.5 V	0.4			0.4			0.4			V	
I _I	Input leakage current	OE V _I = V _{CC} or GND	1.65 V to 3.6 V	2.3 V to 5.5 V	1			2			2			μA	
I _{off}	Partial power down current	A port	0 V	0 V to 5.5 V	1			2			2			μA	
		B port	0 V to 3.6 V	0 V	1			2			2			μA	
I _{OZ}	Tri-state output current	A or B Port: V _I = V _{CCI} or GND V _O = V _{CCO} or GND OE = GND	1.65 V to 3.6 V	2.3 V to 5.5 V	-2			2			-3			3	μA
I _{CCA}	V _{CCA} supply current	V _I = V _{CCI} or GND I _O = 0	1.65 V to V _{CCB}	2.3 V to 5.5 V	3			3			5			μA	
			0 V	5.5 V	-3			-3			-3				
			3.6 V	0 V	2.2			2.2			2.2				
I _{CCB}	V _{CCB} supply current	V _I = V _{CCI} or GND I _O = 0	1.65 V to V _{CCB}	2.3 V to 5.5 V	12			12			21			μA	
			0 V	5.5 V	5			5			8				
			3.6 V	0 V	-1			-1			-1				
I _{CCA} + I _{CCB}	Combined supply current	V _I = V _{CCI} or GND I _O = 0	1.65 V to V _{CCB}	2.3 V to 5.5 V	14.4			14.4			25			μA	
C _i	Input Capacitance	OE	3.3 V	3.3 V	2.5			3.5			3.5			pF	
C _{io}	A or B port	OE = GND, V _O = 1.65V DC +1 MHz -16 dBm sine wave	3.3 V	3.3 V	10									pF	
					5			6			6				
					6			7.5			7.5				

- (1) V_{CCI} is the V_{CC} associated with the input port
- (2) V_{CCO} is the V_{CC} associated with the output port
- (3) Tested at V_I = V_{T+(MAX)}
- (4) Tested at V_I = V_{T-(MIN)}

5.6 Switching Characteristics, $V_{CCA} = 1.8 \pm 0.15 \text{ V}$

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})						UNIT			
					2.5 ± 0.2 V			3.3 ± 0.3 V				5.0 ± 0.5 V		
					MIN	TYP	MAX	MIN	TYP	MAX		MIN	TYP	MAX
t_{PHL}	Propagation Delay (High-to-Low)	A	B	Push-Pull	5			5			6			ns
				Open-Drain	8.8			9.6			10			
t_{PLH}	Propagation Delay (Low-to-High)	A	B	Push-Pull	6.5			7			7			ns
				Open-Drain	250			200			185			
t_{PHL}	Propagation Delay (High-to-Low)	B	A	Push-Pull	4			4			5			ns
				Open-Drain	5.3			4.4			4			
t_{PLH}	Propagation Delay (Low-to-High)	B	A	Push-Pull	5			4			1			ns
				Open-Drain	173			89			66			
t_{en}	Enable Time	OE	A or B	-40°C to 125°C	200			200			200			ns
t_{dis}	Disable Time				250			250			250			
t_{rA}	Output Rise Time	B	A	Push-Pull	9			9			7			ns
				Open-Drain	150			120			80			
t_{rB}	Output Rise Time	A	B	Push-Pull	10			9			7			ns
				Open-Drain	145			106			58			
t_{fA}	Output Fall Time	B	A	Push-Pull	5			6			13			ns
				Open-Drain	6			6			6			
t_{fB}	Output Fall Time	A	B	Push-Pull	7			7			8			ns
				Open-Drain	13			16			16			

5.7 Switching Characteristics, $V_{CCA} = 2.5 \pm 0.2 \text{ V}$

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})						UNIT			
					2.5 ± 0.2 V			3.3 ± 0.3 V				5.0 ± 0.5 V		
					MIN	TYP	MAX	MIN	TYP	MAX		MIN	TYP	MAX
t_{PHL}	Propagation Delay (High-to-Low)	A	B	Push-Pull	3.2			3.7			5			ns
				Open-Drain	6.3			6			5.8			
t_{PLH}	Propagation Delay (Low-to-High)	A	B	Push-Pull	3			4			4			ns
				Open-Drain	200			200			190			
t_{PHL}	Propagation Delay (High-to-Low)	B	A	Push-Pull	3			3			4			ns
				Open-Drain	4.7			4.2			4			
t_{PLH}	Propagation Delay (Low-to-High)	B	A	Push-Pull	2.1			1.6			1			ns
				Open-Drain	170			140			103			
t_{en}	Enable Time	OE	A or B	-40°C to 125°C	200			200			200			ns
t_{dis}	Disable Time				250			250			250			
t_{rA}	Output Rise Time	B	A	Push-Pull	7			6			5			ns
				Open-Drain	156			120			80			
t_{rB}	Output Rise Time	A	B	Push-Pull	8			7			6			ns
				Open-Drain	151			112			64			
t_{fA}	Output Fall Time	B	A	Push-Pull	5.1			5.2			5			ns
				Open-Drain	6			6			5			
t_{fB}	Output Fall Time	A	B	Push-Pull	7			6.4			8.7			ns
				Open-Drain	8			9			10			

5.8 Switching Characteristics, $V_{CCA} = 3.3 \pm 0.3 \text{ V}$

PARAMETER	FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})						UNIT	
				3.3 ± 0.3 V			5.0 ± 0.5 V				
				MIN	TYP	MAX	MIN	TYP	MAX		
t_{PHL}	Propagation Delay (High-to-Low)	A	B	Push-Pull	2.4			3.1			ns
				Open-Drain	4.2			4.6			
t_{PLH}	Propagation Delay (Low-to-High)	A	B	Push-Pull	4			4			ns
				Open-Drain	204			165			
t_{PHL}	Propagation Delay (High-to-Low)	B	A	Push-Pull	2.5			3.3			ns
				Open-Drain	124			97			
t_{PLH}	Propagation Delay (Low-to-High)	B	A	Push-Pull	2.5			2.6			ns
				Open-Drain	139			105			
t_{en}	Enable Time	OE	A or B	-40°C to 125°C	200			200			ns
t_{dis}	Disable Time				250			250			
t_{rA}	Output Rise Time	B	A	Push-Pull	5			4			ns
				Open-Drain	116			85			
t_{rB}	Output Rise Time	A	B	Push-Pull	6			7			ns
				Open-Drain	117			116			
t_{fA}	Output Fall Time	B	A	Push-Pull	5.4			5			ns
				Open-Drain	6			5			
t_{fB}	Output Fall Time	A	B	Push-Pull	7.4			7.6			ns
				Open-Drain	7			8			

5.9 Switching Characteristics: T_{sk} , T_{MAX}

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CCA}	V_{CCB}	Operating free-air temperature (T_A)			UNIT
				-40°C to 125°C			
				MIN	TYP	MAX	
T_{MAX} - Maximum Data Rate	50% Duty Cycle Input One channel switching	Push-Pull Driving	1.8 ± 0.15 V	2.5 V ± 0.2 V			18
				3.3 V ± 0.3 V			21
				5 V ± 0.5 V			23
T_{MAX} - Maximum Data Rate	50% Duty Cycle Input One channel switching	Push-Pull Driving	2.5 V ± 0.2 V	2.5 V ± 0.2 V			20
				3.3 V ± 0.3 V			22
				5 V ± 0.5 V			24
T_{MAX} - Maximum Data Rate	50% Duty Cycle Input One channel switching	Push-Pull Driving	3.3 V ± 0.3 V	3.3 V ± 0.3 V			22
				5 V ± 0.5 V			24
T_{MAX} - Maximum Data Rate	50% Duty Cycle Input One channel switching	Open-Drain Driving	1.8 ± 0.15 V	2.5 V ± 0.2 V			2
				3.3 V ± 0.3 V			2
				5 V ± 0.5 V			2
T_{MAX} - Maximum Data Rate	50% Duty Cycle Input One channel switching	Open-Drain Driving	2.5 V ± 0.2 V	2.5 V ± 0.2 V			2
				3.3 V ± 0.3 V			2
				5 V ± 0.5 V			2
T_{MAX} - Maximum Data Rate	50% Duty Cycle Input One channel switching	Open-Drain Driving	3.3 V ± 0.3 V	3.3 V ± 0.3 V			2
				5 V ± 0.5 V			2
t_w	Pulse Duration, Data Inputs	Push-Pull Driving	1.8 V ± 0.15 V to 3.3 V ± 0.3 V	2.5 V ± 0.2 V 5.0 V ± 0.5 V		41	ns
t_w	Pulse Duration, Data Inputs	Open-Drain Driving	1.8 V ± 0.15 V to 3.3 V ± 0.3 V	2.5 V ± 0.2 V 5.0 V ± 0.5 V		500	ns

5.9 Switching Characteristics: T_{sk} , T_{MAX} (続き)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CCA}	V_{CCB}	Operating free-air temperature (T_A)			UNIT
					-40°C to 125°C			
					MIN	TYP	MAX	
t_{sk} - Output skew	Skew between any two outputs of the same package switching in the same direction	Push-Pull Driving	1.8 V \pm 0.15 V to 3.3 V \pm 0.3 V	2.5 V \pm 0.2 V to 5.0 V \pm 0.5 V			1	ns
t_{sk} - Output skew	Skew between any two outputs of the same package switching in the same direction	Open-Drain Driving	1.8 V \pm 0.15 V to 3.3 V \pm 0.3 V	2.5 V \pm 0.2 V to 5.0 V \pm 0.5 V			1	ns

5.10 Typical Characteristics

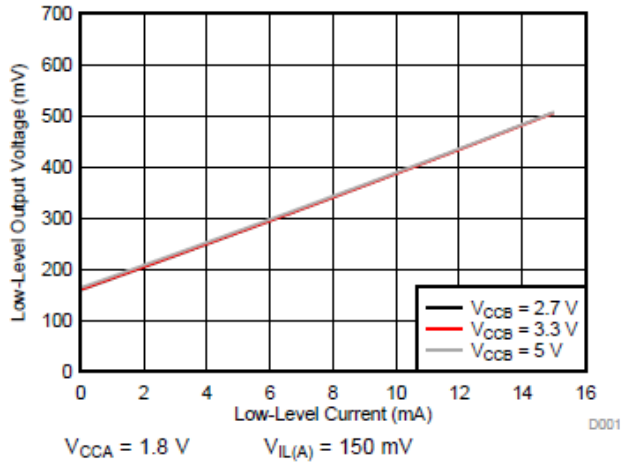


图 5-1. Low-Level Output Voltage ($V_{OL(Bx)}$) vs Low-Level Current ($I_{OL(Bx)}$)

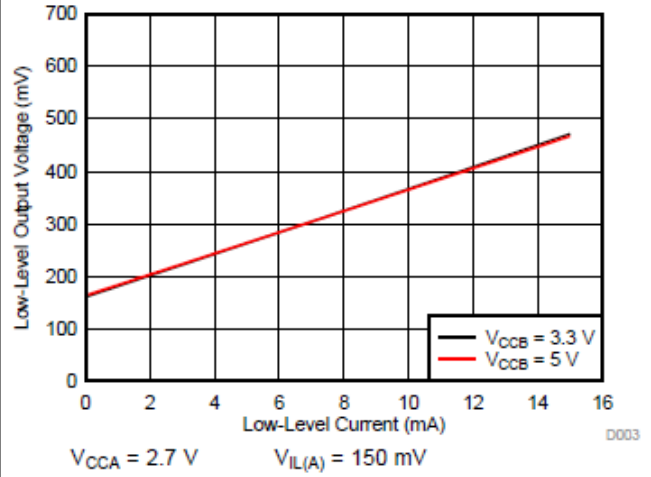


图 5-2. Low-Level Output Voltage ($V_{OL(Bx)}$) vs Low-Level Current ($I_{OL(Bx)}$)

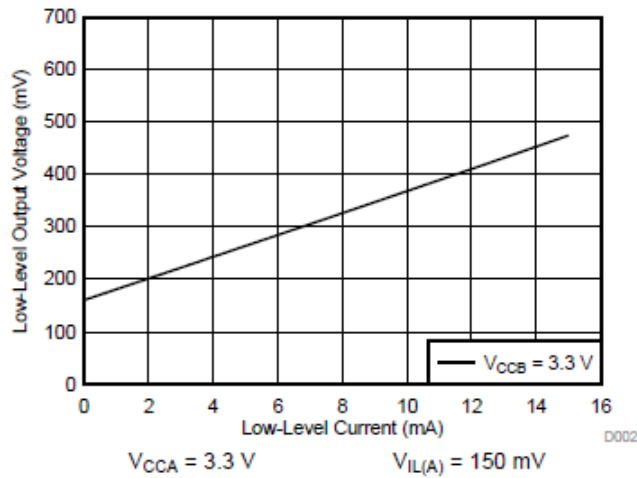


图 5-3. Low-Level Output Voltage ($V_{OL(Bx)}$) vs Low-Level Current ($I_{OL(Bx)}$)

6 Parameter Measurement Information

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- PRR 10MHz
- $Z_O = 50 \Omega$
- $dv/dt \geq 1V/ns$

注

All parameters and waveforms are not applicable to all devices.

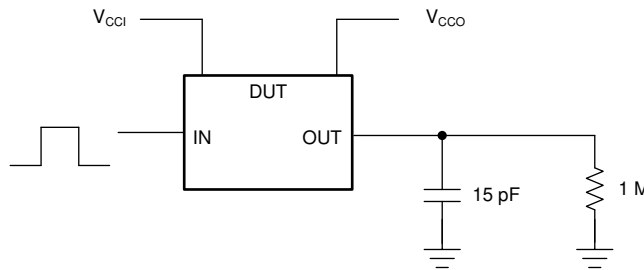


図 6-1. Data Rate, Pulse Duration, Propagation Delay, Output Rise And Fall Time Measurement Using A Push-Pull Driver

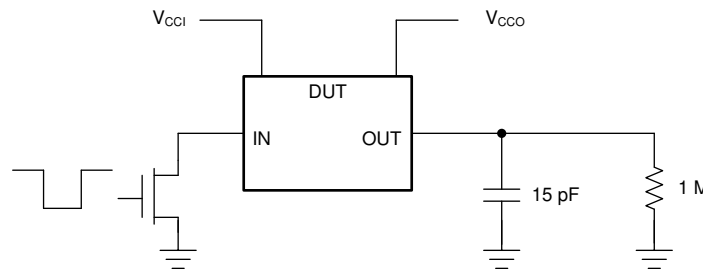


図 6-2. Data Rate, Pulse Duration, Propagation Delay, Output Rise And Fall Time Measurement Using An Open-Drain Driver

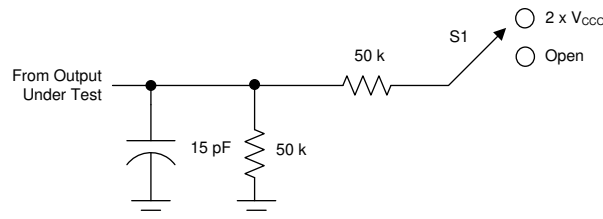
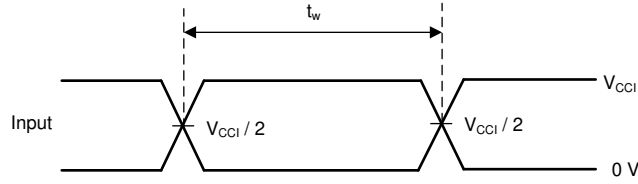


図 6-3. Load Circuit For Enable / Disable Time Measurement

表 6-1. Switch Configuration For Enable / Disable Timing

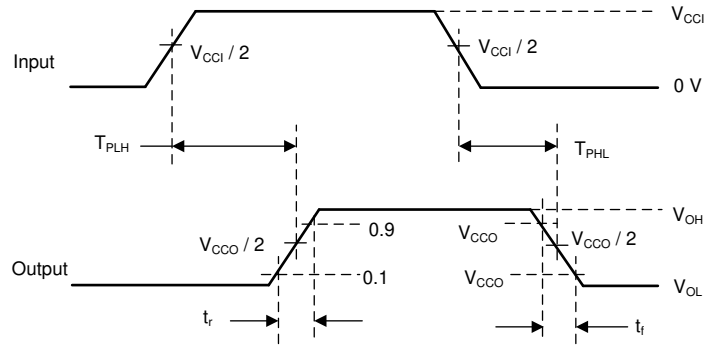
TEST	S1
$t_{PZL}^{(2)}$, $t_{PLZ}^{(1)}$	$2 \times V_{CCO}$
$t_{PHZ}^{(1)}$, $t_{PZH}^{(2)}$	Open

- (1) t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 (2) t_{PZL} and t_{PZH} are the same as t_{en} .



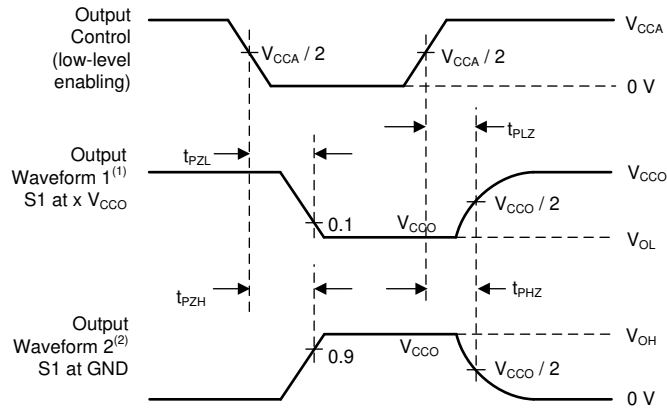
(1) All input pulses are measured one at a time, with one transition per measurement.

6-4. Voltage Waveforms Pulse Duration



(1) All input pulses are measured one at a time, with one transition per measurement.

6-5. Voltage Waveforms Propagation Delay Times



- (1) Waveform 1 is for an output with internal conditions so that the output is low, except when disabled by the output control.
- (2) Waveform 2 is for an output with internal conditions so that the output is high, except when disabled by the output control.

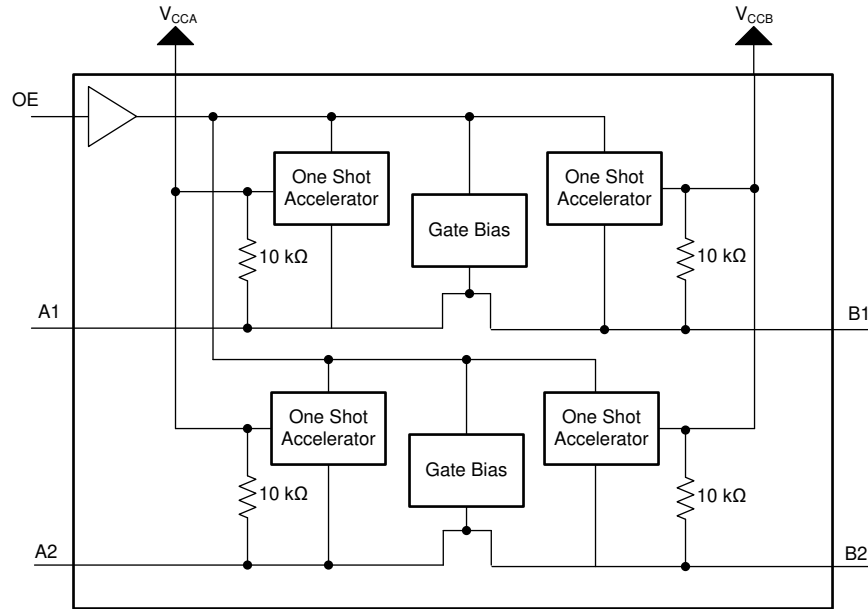
6-6. Voltage Waveforms Enable And Disable Times

7 Detailed Description

7.1 Overview

The TXS0102V-Q1 device is a directionless voltage-level translator specifically designed for translating logic voltage levels. The A port can accept I/O voltages ranging from 1.65V to 3.6V, while the B port can accept I/O voltages from 2.3V to 5.5V. The device is a pass-gate architecture with edge-rate accelerators (one-shots) to improve the overall data rate. 10kΩ pullup resistors, commonly used in open-drain applications, have been conveniently integrated so that an external resistor is not needed. While this device is designed for open-drain applications, the device can also translate push-pull CMOS logic outputs.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Architecture

The TXS0102V-Q1 architecture (see [Figure 7-1](#)) is an auto-direction-sensing based translator that does not require a direction-control signal to control the direction of data flow from A to B or from B to A.

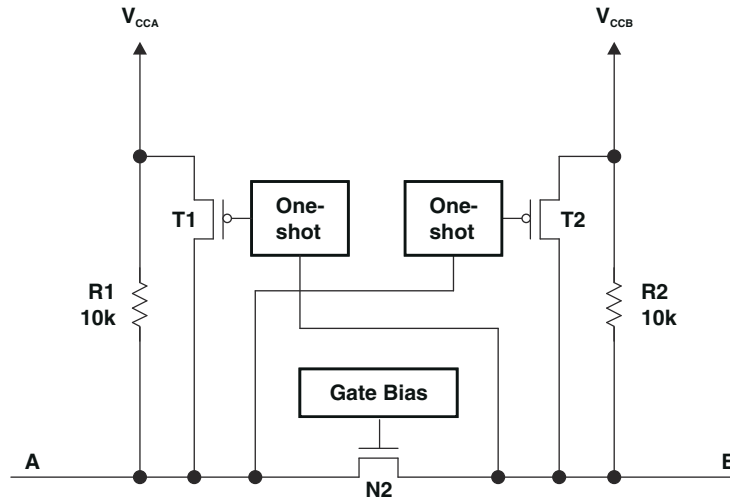


Figure 7-1. Architecture of a TXS0102V-Q1 Cell

These two bidirectional channels independently determine the direction of data flow without a direction-control signal. Each I/O pin can be automatically reconfigured as either an input or an output, which is how this auto-direction feature is realized.

The TXS0102V-Q1 device is part of TI's "Switch" type voltage translator family and employs two key circuits to enable this voltage translation:

1. An N-channel pass-gate transistor topology that ties the A-port to the B-port
2. Output one-shot (O.S.) edge-rate accelerator circuitry to detect and accelerate rising edges on the A or B ports

For bidirectional voltage translation, pull-up resistors are included on the device for dc current sourcing capability. The V_{GATE} gate bias of the N-channel pass transistor is set at approximately one threshold voltage (V_T) above the V_{CC} level of the low-voltage side. Data can flow in either direction without guidance from a control signal.

The O.S. rising-edge rate accelerator circuitry speeds up the output slew rate by monitoring the input edge for transitions, helping maintain the data rate through the device. During a low-to-high signal rising edge, the O.S. circuits turn on the PMOS transistors (T1 and T2) to increase the current drive capability of the driver for approximately 30ns or 95% of the input edge, whichever occurs first. This edge-rate acceleration provides high ac drive by bypassing the internal 10k Ω pull-up resistors during the low-to-high transition to speed up the signal. The output resistance of the driver is decreased to approximately 50 Ω to 70 Ω during this acceleration phase. To minimize dynamic I_{CC} and the possibility of signal contention, the user should wait for the O.S. circuit to turn off before applying a signal in the opposite direction. The worst-case duration is equal to the minimum pulse-width number provided in the [Section 5.6](#) section of this data sheet.

7.3.2 Input Driver Requirements

the external system-level open-drain (or push-pull) drivers that are interfaced to the TXS0102V-Q1 I/O pins determines the continuous dc-current *sinking* capability. Since the high bandwidth of these bidirectional I/O circuits is used to facilitate this fast change from an input to an output and an output to an input, they have a modest dc-current *sourcing* capability of hundreds of micro-Amps, as determined by the internal 10k Ω pullup resistors.

The fall time (t_{fA} , t_{fB}) of a signal depends on the edge-rate and output impedance of the external device driving TXS0102V-Q1 data I/Os, as well as the capacitive loading on the data lines.

Similarly, the t_{PHL} and max data rates also depend on the output impedance of the external driver. The values for t_{fA} , t_{fB} , t_{PHL} , and maximum data rates in the data sheet assume that the output impedance of the external driver is less than 50 Ω .

7.3.3 Output Load Considerations

TI recommends careful PCB layout practices with short PCB trace lengths to avoid excessive capacitive loading and to determine that proper O.S. triggering takes place. PCB signal trace-lengths should be kept short enough so that the round trip delay of any reflection is less than the one-shot duration. This improves signal integrity by allowing any reflection sees a low impedance at the driver. The O.S. circuits are designed to stay on for approximately 30ns.

The maximum capacitance of the lumped load that can be driven also depends directly on the one-shot duration. With very heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. The O.S. duration has been set to best optimize trade-offs between dynamic ICC, load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance that the TXS0102V-Q1 device output sees, so it is recommended that this lumped-load capacitance be considered to avoid O.S. retriggering, bus contention, output signal oscillations, or other adverse system-level affects.

7.3.4 Enable and Disable

The TXS0102V-Q1 device has an OE input that is used to disable the device by setting OE low, which places all I/Os in the Hi-Z state. The disable time (t_{dis}) indicates the delay between the time when OE goes low and when the outputs are disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

7.3.5 Pullup or Pulldown Resistors on I/O Lines

Each A-port I/O has an internal 10k Ω pullup resistor to V_{CCA} , and each B-port I/O has an internal 10k Ω pullup resistor to V_{CCB} . If a smaller value of pullup resistor is required, an external resistor must be added from the I/O to V_{CCA} or V_{CCB} (in parallel with the internal 10k Ω resistors). Adding lower value pull-up resistors will effect V_{OL} levels, however. The internal pull-ups of the TXS0102V-Q1 are disabled when the OE pin is low.

7.4 Device Functional Modes

The device has two functional modes, enabled and disabled. To disable the device set the OE input low, which places all I/Os in a high impedance state. Setting the OE input high will enable the device.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TXS0102V-Q1 device can be used to bridge the digital-switching compatibility gap between two voltage nodes to successfully interface logic threshold levels found in electronic systems. It should be used in a point-to-point topology for interfacing devices or systems operating at different interface voltages with one another. Its primary target application use is for interfacing with open-drain drivers on the data I/Os such as I²C or 1-wire, where the data is bidirectional and no control signal is available. The device can also be used in applications where a push-pull driver is connected to the data I/Os, but the TXB0102 might be a better option for such push-pull applications.

8.2 Typical Application

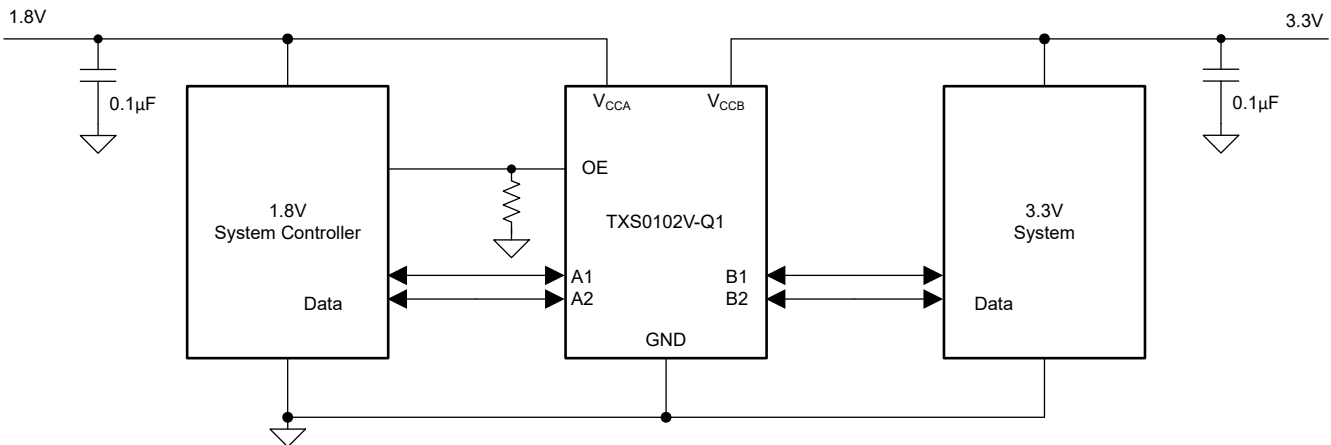


図 8-1. Typical Application Circuit

8.2.1 Design Requirements

Use the parameters listed in 表 8-1 for this design example, and ensure the $V_{CCA} \leq V_{CCB}$.

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.65 to 3.6V
Output voltage range	2.3 to 5.5V

8.2.2 Detailed Design Procedure

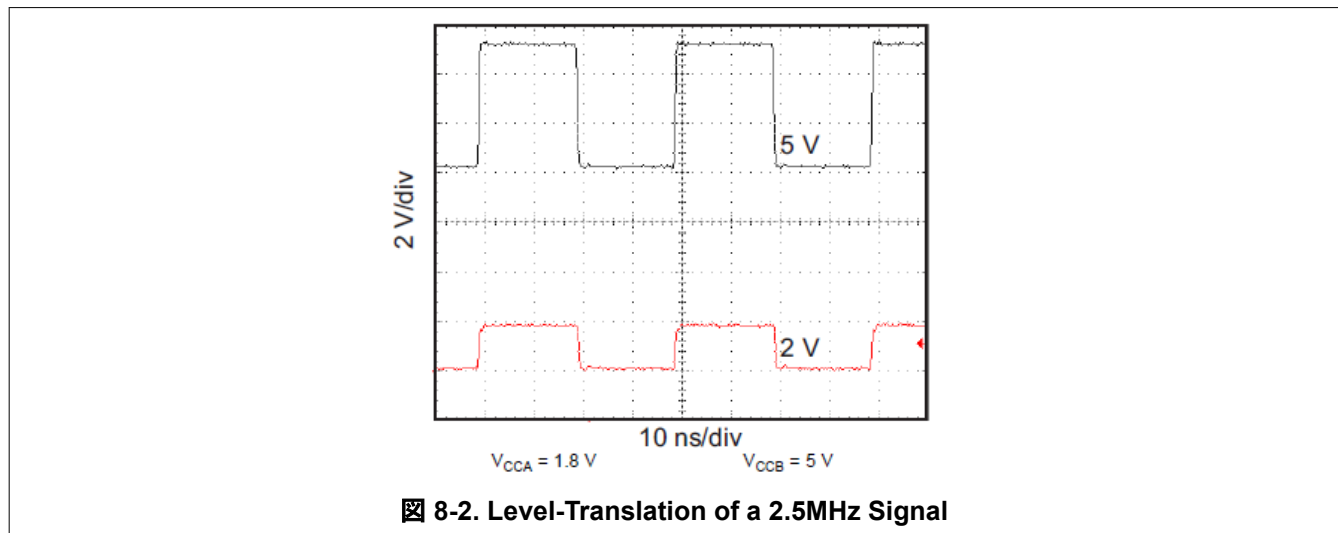
To begin the design process, determine the following:

- Input voltage range
 - Use the supply voltage of the device that is driving the TXS0102V-Q1 device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.
- Output voltage range
 - Use the supply voltage of the device that the TXS0102V-Q1 device is driving to determine the output voltage range.
 - The TXS0102V-Q1 device has $10k\Omega$ internal pullup resistors. External pullup resistors can be added to reduce the total RC of a signal trace if necessary.
- An external pull down resistor decreases the output V_{OH} and V_{OL} . Use 式 1 to calculate the V_{OH} as a result of an external pull down resistor.

$$V_{OH} = V_{CCx} \times R_{PD} / (R_{PD} + 10k\Omega) \quad (1)$$

- Where:
 - V_{CCx} is the supply voltage on either V_{CCA} or V_{CCB}
 - R_{PD} is the value of the external pull down resistor

8.2.3 Application Curves



8.3 Power Supply Recommendations

During operation, ensure that $V_{CCA} \leq V_{CCB}$ at all times. The sequencing of each power supply will not damage the device during the power up operation, so either power supply can be ramped up first. The output-enable (OE) input circuit is designed so that it is supplied by V_{CCA} and when the (OE) input is low, all outputs are placed in the high-impedance state.

To put the outputs in the high-impedance state during power up or power down, the OE input pin must be tied to GND through a pulldown resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The current-sourcing capability of the driver determines the minimum value of the pulldown resistor to ground.

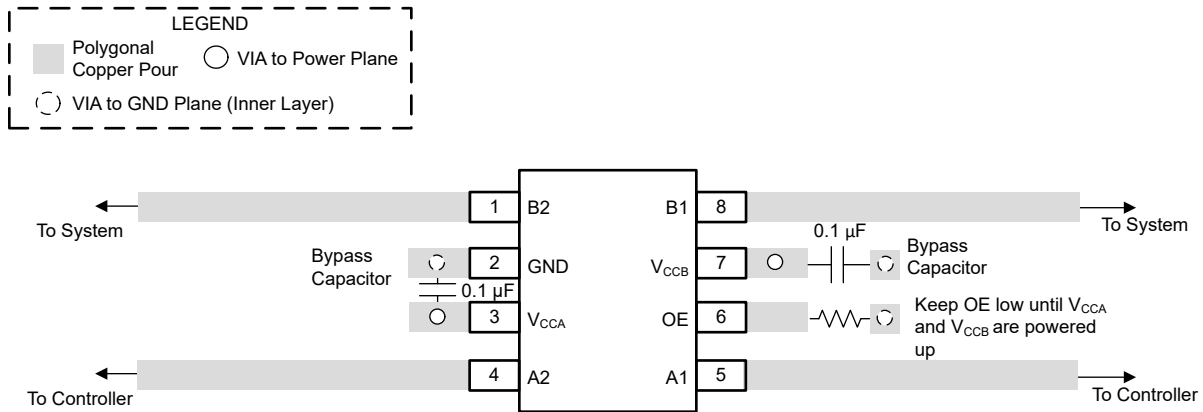
8.4 Layout

8.4.1 Layout Guidelines

For device reliability, it is recommended to follow common printed-circuit board layout guidelines such as follows:

- Bypass capacitors should be used on power supplies and should be placed as close as possible to the V_{CCA} , V_{CCB} pin, and G_{ND} pin.
- Short trace lengths should be used to avoid excessive loading.
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one-shot duration, approximately 30ns, causing any reflection encounters low impedance at the source driver.

8.4.2 Layout Example



8-3. TXS0102V-Q1 Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [A Guide to Voltage Translation With TXS-Type Translators application note](#)
- Texas Instruments, [Factors Affecting VOL for TXS and LSF Auto-bidirectional Translation Devices application note](#)
- Texas Instruments, [Biasing Requirements for TXS, TXB, and LSF Auto-Bidirectional Translators application note](#)
- Texas Instruments, [Effects of pullup and pulldown resistors on TXS and TXB devices application note](#)
- Texas Instruments, [Introduction to logic application note](#)
- Texas Instruments, [TI Logic and Linear Products Guide selection and solution guides](#)
- Texas Instruments, [Washing Machine Solutions Guide selection and solution guides](#)
- Texas Instruments, [TI Smartphone Solutions Guide selection and solution guides](#)

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 サポート・リソース

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9.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (June 2024) to Revision A (September 2024)	Page
• Updated ESD Ratings: 2kV HBM to 2.5kV HBM.....	4

DATE	REVISION	NOTES
June 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TXS0102VQDCURQ1	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125		Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TXS0102V-Q1 :

- Catalog : [TXS0102V](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS0102VQDCURQ1	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS0102VQDCURQ1	VSSOP	DCU	8	3000	180.0	180.0	18.0



4225266/A 09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.

EXAMPLE BOARD LAYOUT

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



4225266/A 09/2014

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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郵送先住所 : Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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