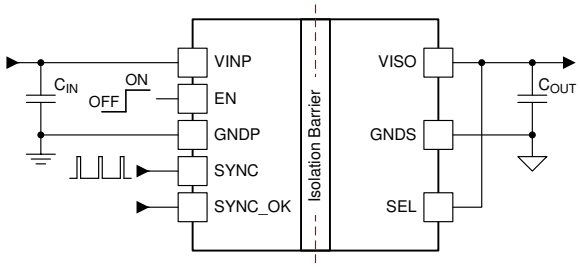
TEXAS INSTRUMENTS
UCC12051-Q1
JAJSK41A – JANUARY 2021 – REVISED JUNE 2021

UCC12051-Q1 高効率、低 EMI、5kV$_{RMS}$ 絶縁 DC/DC コンバータ

1 特長

- 内蔵トランス・テクノロジーを採用した高効率 DC-DC コンバータ
- 下記内容で AEC-Q100 認定済み:
  - デバイス温度グレード 1:-40℃～125℃ の動作時周囲温度範囲
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 出力電力 (標準値):500mW
- 5V または 3.3V 安定化出力 (LDO に給電するための 400mV のヘッドルーム電圧の有無を選択可能)
- 入力電圧:4.5V～5.5V
- 堅牢な絶縁バリア:
  - 絶縁定格:5 kV$_{RMS}$
  - サージ耐性:10kV$_{PK}$
  - 動作電圧:1.2kV$_{RMS}$
  - 最小 CMTI:100V/ns
- 短絡からの回復
- サーマル・シャットダウン
- 沿面距離と空間距離が 8mm を超える 16 ピン幅広 SOIC パッケージ
- 安全関連認証 (予定):
  - DIN V VDE V 0884-11:2017-01 に準拠した強化絶縁耐圧:7071V$_{PK}$
  - UL 1577 に準拠した絶縁耐圧:5000V$_{RMS}$、1 分間
  - IEC 60950-1 および IEC 62368-1 最終機器規格準拠の UL 認証
  - GB4943.1-2011 による CQC 認証



アプリケーション概略

2 アプリケーション

- オンボード・チャージャ
- バッテリ・マネージメント・システム
- トラクション・インバータ
- HEV/EV 用 DC/DC コンバータ

3 概要

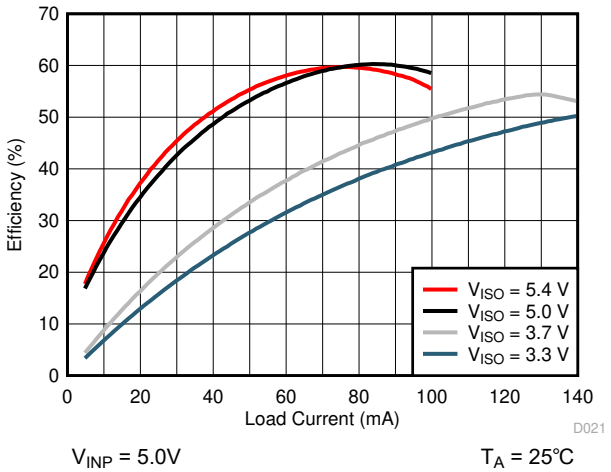
UCC12051-Q1 は、5kV$_{RMS}$ の絶縁を備えた DC/DC パワー・モジュールであり、適切にレギュレートされた出力電圧のバイアス電源を必要とする絶縁回路に、高効率の絶縁電力を供給するよう設計されています。このデバイスは、独自のアーキテクチャによってトランスと DC/DC コントローラを統合しており、500mW (標準値) の絶縁電力を高効率かつ低 EMI で供給できます。

UCC12051-Q1 は、システムの堅牢性を向上させるための保護機能を内蔵しています。このデバイスはイネーブル・ピン、同期機能、5V または 3.3V 安定化出力選択機能 (ヘッドルームを選択可能) も備えています。UCC12051-Q1 は、高さ 2.65mm (標準値) の幅広 SOIC パッケージで供給される薄型の小型ソリューションです。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
UCC12051-Q1	DVE SOIC (16)	10.30mm × 7.50mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



V_{INP} = 5.0V　　T_A = 25℃

代表的な効率と負荷との関係

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (January 2021) to Revision A (June 2021)	Page
• ステータスを「事前情報」から「量産データ」に変更	1

5 Pin Configuration and Functions

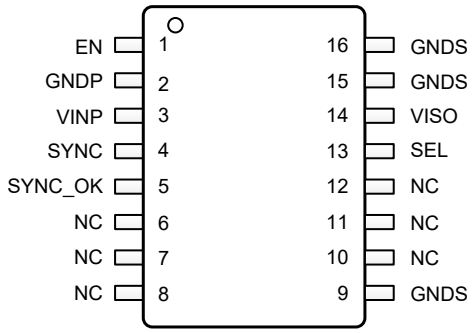


図 5-1. DVE Package 16-Pin SOIC Top View

表 5-1. Pin Functions

PIN		TYPE (1)	DESCRIPTION
NAME	NO.		
EN	1	I	Enable pin. Forcing EN low disables the device. Pull high to enable normal device functionality.
GNDP	2	P	Power ground return connection for VINP.
GNDS	9	P	Connect to GNDS plane on printed circuit board. Do not use as only ground connection for VISO. Ensure pin 15 is connected to circuit ground.
	16		
GNDS	15	P	Secondary side ground return connection for VISO. Connect bypass capacitor from VISO to this pin.
NC	6	—	Pins internally connected together. No other electrical connection. Pins belong to primary-side voltage domain. Connect to GNDP on printed circuit board.
	7		
	8		
	10	—	No internal connection. Pin belongs to isolated voltage domain. Connect to GNDS on printed circuit board.
	11		
	12		
SYNC	4	I	Synchronous clock input pin. Provide a clock signal to synchronize multiple devices or connect to GNDP for standalone operation using the internal oscillator. If the SYNC pin is left open make sure to it separate it from any switching noise to avoid false clock coupling.
SYNC_OK	5	O	Active-low, open-drain diagnostic output. Pin is asserted LOW if there is no external SYNC clock or one that is outside of the operating range of the is detected. In this state, the external clock is ignored and the DC/DC converter is clocked by the internal oscillator. The pin is in high-impedance if a clock is applied on SYNC.
SEL	13	I	V_{ISO} selection pin. V_{ISO} setpoint is 5.0 V when SEL is shorted to V_{ISO}, 5.4 V when SEL is connected to V_{ISO}through a 100-kΩ resistor, 3.3 V when SEL is shorted to GNDS, and 3.7 V when SEL is connected to GNDS through a 100-kΩ resistor. For more information see the *セクション 7.4* section.
VINP	3	P	Primary side input supply voltage pin. A 10-µF ceramic capacitor to GNDP on pin 2, placed close to the device pins, is required.
VISO	14	P	Isolated supply voltage pin. A 10-µF ceramic capacitor to GNDS on pin 15, placed close to the device pins, is required. See *セクション 8.2.2.1* section.

(1) P = Power, G = Ground, I = Input, O = Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
VINP to GNDP	–0.3	6.0	V
EN, SYNC, SYNC_OK, to GNDP	–0.3	VINP + 0.3, ≤ 6.0	V
VISO to GNDS	–0.3	6.0	V
SEL to GNDS	–0.3	VISO + 0.3, ≤ 6.0	V
V_{ISO} output power at T_a = 25°C, P_{OUT_MAX} (2)		675	mW
Operating junction temperature range, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) See the VISO Load Recommended Operating Area section for maximum rated values across temperature and V_{INP} conditions for each different V_{ISO} output mode.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{INP}	Primary side supply voltage	4.5	5.0	5.5	V
V_{EN}	EN pin input voltage	0		5.5	V
V_{SYNC}	SYNC pin input voltage	0		5.5	V
$V_{SYNC-OK}$	SYNC_OK pen drain pin voltage	0		5.5	V
V_{ISO}	Isolated power supply voltage	0		5.7	V
V_{SEL}	Input voltage	0		5.7	V
f_{SYNC}	External DC/DC converter synchronization signal frequency	14.4	16.0	17.6	MHz
P_{VISO}	V_{ISO} output power at T_a = 25°C (1)			500	mW
T_a	Ambient temperature	–40		125	°C
T_J	Junction temperature	–40		150	°C

(1) See the VISO Load Recommended Operating Area section for maximum rated values across temperature and V_{INP} conditions for each different V_{ISO} output mode.

6.4 Thermal Information

THERMAL METRIC(1)		UCC12051-Q1 DVE (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	57.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	21.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33.7	°C/W

6.4 Thermal Information (continued)

THERMAL METRIC[1]		UCC12051-Q1 DVE (SOIC) 16 PINS	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and can not be used for design purposes. This value was calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board when P_{DP} = 129 mW, P_{DS} = 142 mW and P_{DT} = 129 mW. The board temperature is taken from Pin 12. For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Power Ratings

V_{INP} = 5.0V, C_{INP} = C_{OUT} = 10 uF, T_J = 150°C, Internal Clock mode

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Power dissipation	SEL connected to GNDS (3.3-V V_{ISO} output mode), I_{ISO} = 135 mA	460	mW
P_{DP}	Power dissipation by driver side (primary)		148	mW
P_{DS}	Power dissipation by rectifier side (secondary)		164	mW
P_{DT}	Power dissipation by transformer		148	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	> 8	mm
CPG	External creepage[1]	Shortest terminal-to-terminal distance across the package surface	> 8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 120	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage Category	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN V VDE V 0884-11:2017-01[2] (Planned Certification Targets)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1697	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage (sine wave) Time dependent dielectric breakdown (TDDB) test	1200	V_{RMS}
		DC voltage	1697	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM}, t = 60s (qualification); V_{TEST} = 1.2 × V_{IOTM}, t = 1s (100% production)	7071	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[3]	Test method per IEC 62368-1, 1.2/50 µs waveform, V_{TEST} = 1.6 × V_{IOSM} = 10000 V_{PK} (qualification)	6250	V_{PK}
q_{pd}	Apparent charge[4]	Method a: After I/O safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM} = 1696 V_{PK}, t_m = 10 s	≤ 5	pC
		Method a: After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.6 × V_{IORM} = 2262 V_{PK}, t_m = 10 s	≤ 5	
		Method b1: At routine test (100% production) and preconditioning (type test) V_{ini} = 1.2 × V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.875 × V_{IORM} = 2651 V_{PK}, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output[5]	V_{IO} = 0.4 sin (2πft), f = 1 MHz	~3.5	pF
R_{IO}	Isolation resistance, input to output[5]	V_{IO} = 500 V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	> 10^9	
	Pollution degree		2	
	Climatic category		40/125/21	

6.6 Insulation Specifications (continued)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
UL 1577 (Planned Certification Target)				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO} = 5000\ V_{RMS}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO} = 6000\ V_{RMS}$, t = 1 s (100% production)	5000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-terminal device

6.7 Safety-Related Certifications

VDE	UL	UL	CQC
Plan to certify according to DIN V VDE V 0884-11:2017- 01	Plan to certify according to IEC 60950-1 and IEC 62368-1	Plan to certify under UL 1577 Component Recognition Program	Plan to certify according to GB4943.1-2011
Reinforced insulation Maximum transient isolation voltage, 7071 V_{PK}; Maximum repetitive peak isolation voltage, 1697 V_{PK}; Maximum surge isolation voltage, 6250 VPK	Reinforced insulation per UL 60950-1-07+A1+A2, IEC 60950-1 2nd Ed.+A1+A2, UL 62368-1-14 and IEC 62368-1 2nd Ed., 800 V_{RMS} maximum working voltage (pollution degree 2, material group I)	Single protection, 5000 V_{RMS}	Reinforced insulation, Altitude ≤ 5000 m, Tropical Climate, 700 V_{RMS} maximum working voltage
Certificate number: (planned)	Master contract number: (planned)	File number: (planned)	Certificate number: (planned)

6.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MAX	UNIT
I_S	Safety input current (1)	$R_{\theta JA} = 57.5°C/W$, $V_I = 5.5\ V$, $T_J = 150°C$, $T_A = 25°C$	395	mA
		$R_{\theta JA} = 57.5°C/W$, $V_I = 4.5\ V$, $T_J = 150°C$, $T_A = 25°C$	483	
P_S	Safety input power	$R_{\theta JA} = 57.5°C/W$, $T_J = 150°C$, $T_A = 25°C$	2174	mW
T_S	Safety temperature (1)		150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A. The junction-to-air thermal resistance, $R_{\theta JA}$, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter: $T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device. $T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature. $P_S = I_S \times V_I$, where V_I is the maximum input voltage.

6.9 Electrical Characteristics

Over operating temperature range (T_J = –40°C to 150°C), V_{INP} = 4.5V to 5.5V, C_{INP} = C_{OUT} = 10 µF, internal clock mode, unless otherwise noted. All typical values at T_A = 25°C and V_{INP} = 5.0V.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
I_{VINQ}	VINP quiescent current,disabled	EN=LOW			100	uA
I_{VINO}	VINP operating current, no load	EN=HI; SEL shorted to VISO (5.0V output)		52	80	mA
		EN=HI; SEL 100kΩ to VISO (5.4V output)		48	70	
		EN=HI; SEL shorted to GNDS (3.3V output)		96	140	
		EN=HI; SEL 100kΩ to GNDS (3.7V output)		82	120	
I_{VIN_SC}	DC current from VINP supplyunder short circuit on VISO	VISO short to GNDS		245		mA
V_{UVPR}	VINP under-voltage lockout rising threshold			4.25	4.45	V
V_{UVPF}	VINP under-voltage lockout falling threshold		3.5	3.75		V
V_{UVPH}	VINP under-voltage lockout hysteresis			0.5		V
EN, SYNC INPUT PINS						
V_{IR}	Input voltage threshold, logic HIGH	Rising edge			2.2	V
V_{IF}	Input voltage threshold, logic LOW	Falling edge	0.8			V
I_{EN}	Enable Pin Input Current	V_{EN} = 5.0 V		5	10	uA
I_{SYNC}	SYNC Pin Input Current	V_{SYNC} = 5.0 V		0.02	1	uA
SYNC_OK PIN						
V_{OL}	SYNC_OK output low voltage	I_{SYNC_OK} = - 2 mA		0.15		V
$I_{LKG\_SYNC\_OK}$	SYNC_OK pin leakage current	V_{SYNC_OK} = 5.0 V			1	uA
DC/DC CONVERTER						
V_{ISO}	Isolated supply output voltage	SEL shorted to VISO (5.0V output); I_{ISO} = 55 mA (3)	4.8	5	5.2	V
		SEL 100kΩ to VISO (5.4 V output); I_{ISO} = 45 mA (3)	5.18	5.4	5.62	V
		SEL shorted to GNDS (3.3V output); I_{ISO} = 100 mA (3)	3.17	3.3	3.43	V
		SEL 100kΩ to GNDS (3.7 V output); I_{ISO} = 90 mA (3)	3.55	3.7	3.85	V
$V_{ISO(RIP)}$	Voltage ripple on isolated supply output (pk-pk)(1)	20-MHz bandwidth, CLOAD = 10 uF || 0.1 uF, SEL shorted to VISO (5.0V output); I_{ISO} = 100 mA		50		mV
		20-MHz bandwidth, CLOAD = 10 uF || 0.1 uF, SEL 100kΩ to VISO (5.4V output); I_{ISO} = 90 mA		50		mV
		20-MHz bandwidth, CLOAD = 10 uF || 0.1 uF, SEL shorted to GNDS (3.3V output); I_{ISO} = 145 mA		50		mV
		20-MHz bandwidth, CLOAD = 10 uF || 0.1 uF, SEL shorted to GNDS (3.7V output); I_{ISO} = 130 mA		50		mV
$V_{ISO(LINE)}$	V_{ISO} DC line regulation	SEL shorted to VISO (5.0 V output); I_{ISO} = 55 mA, VINP = 4.5 V to 5.5 V			1%	
		SEL shorted to GNDS (3.3 V output); I_{ISO} = 100 mA, VINP = 4.5 V to 5.5 V			1%	

6.9 Electrical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 150°C), V_{INP} = 4.5V to 5.5V, C_{INP} = C_{OUT} = 10 µF, internal clock mode, unless otherwise noted. All typical values at T_A = 25°C and V_{INP} = 5.0V.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ISO(LOAD)}$	V_{ISO} DC load regulation	SEL shorted to VISO (5.0 V output); I_{ISO} = 0 to 100 mA		1.5%		
		SEL shorted to GNDS (3.3 V output); I_{ISO} = 0 to 145 mA		1.5%		
EFF	Efficiency at maximum recommended load (2)	SEL shorted to VISO (5.0 V output); I_{ISO} = 100 mA		60%		
		SEL 100kΩ to VISO (5.4V output); I_{ISO} = 90 mA		60%		
		SEL shorted to GNDS (3.3V output); I_{ISO} = 145 mA		50%		
		SEL 100kΩ to GNDS (3.7V output); I_{ISO} = 130 mA		53%		
t_{RISE}	VISO rise time, 10% - 90%	EN = change from LO to HI, SEL shorted to VISO (5.0V output); I_{ISO} = 1 mA		750	1000	µs
		EN = change from LO to HI, SEL 100kΩ to GNDS (3.3V output); I_{ISO} = 1 mA		300	500	µs
THERMAL SHUTDOWN						
TSD_{THR}	Thermal shutdown threshold(1)	Junction Temperature, Rising		165		°C
TSD_{HYST}	Thermal shutdown hysteresis(1)	Junction Temperature, Falling		27		°C

(1) Not tested in production. Ensured by characterization.
(2) Efficiency calculation: EFF = (V_{ISO} × I_{ISO}) / (V_{INP} × I_{INP})
(3) See the VISO Load Recommended Oeprating Area section for discussion of V_{ISO} regulation across load and temperature conditions for all output voltage settings.

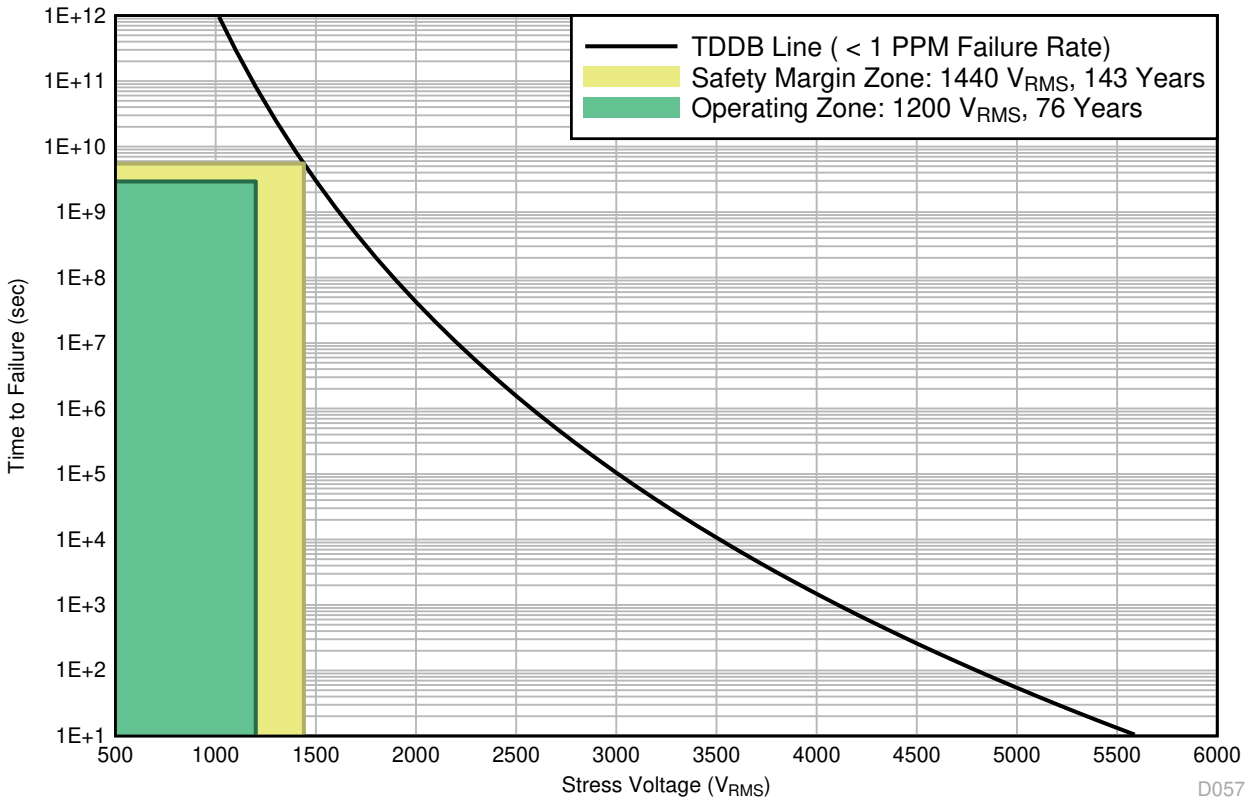
6.10 Switching Characteristics

Over operating temperature range (T_J = –40°C to 150°C), V_{INP} = 4.5V to 5.5V, C_{INP} = C_{OUT} = 10 µF, internal clock mode, unless otherwise noted. All typical values at T_A = 25°C and V_{INP} = 5.0V.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SW_INT}	DC/DC Converter Clock	Internal clock mode		8		MHz
CMTI	Static common-mode transient immunity(1)	Slew Rate of GNDP versus GNDS, V_{CM} = 1000 V	100			V/ns

(1) Not tested in production. Ensured by characterization.

6.11 Insulation Characteristics Curves



Working isolation voltage = 1200 V_{RMS}
T_A up to 150°C

Projected lifetime = 76 years
Stress voltage frequency = 60 Hz

図 6-1. Insulation Lifetime Projection Data

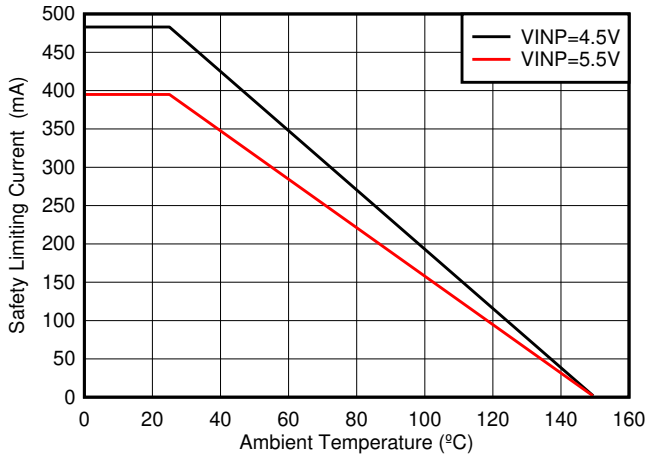


図 6-2. Thermal Derating Curve for Safety Limiting Current per VDE

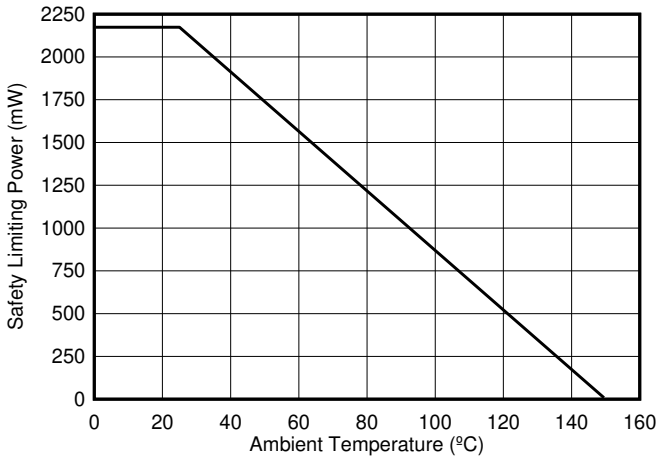
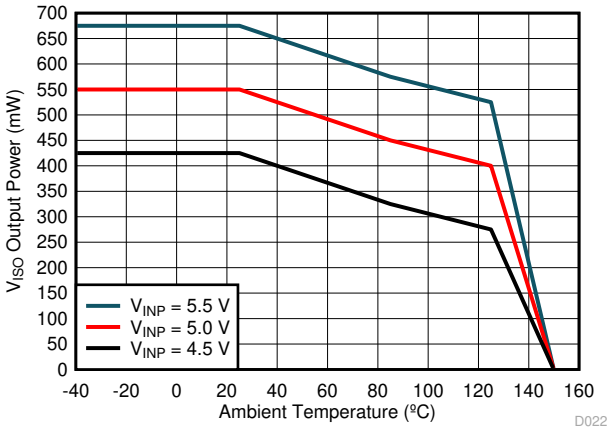


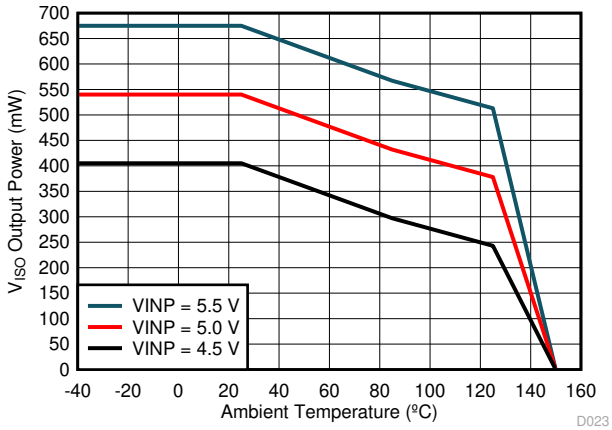
図 6-3. Thermal Derating Curve for Safety Limiting Power per VDE

6.12 Typical Characteristics



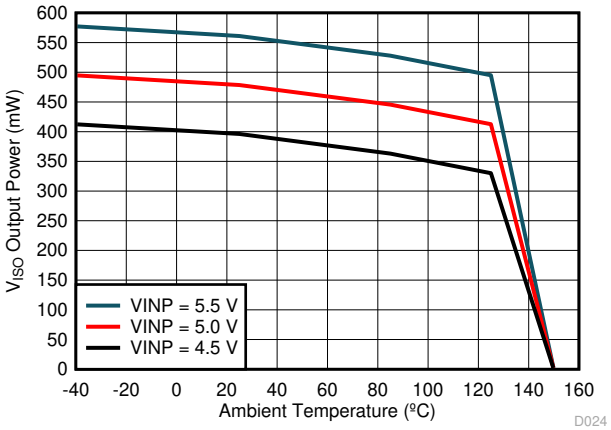
V_{ISO} = 5.0 V

図 6-4. Maximum V_{ISO} Output Power vs. Temperature



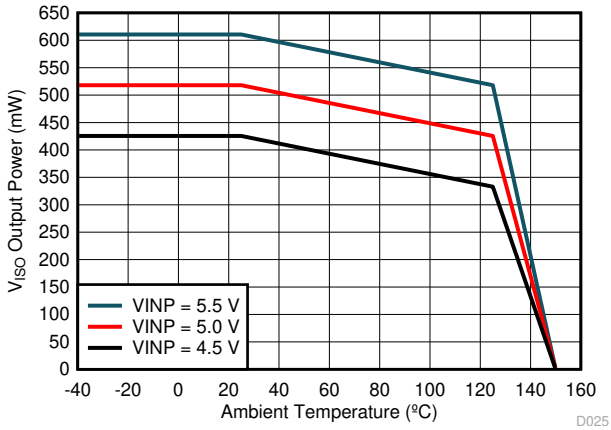
V_{ISO} = 5.4 V

図 6-5. Maximum V_{ISO} Output Power vs. Temperature



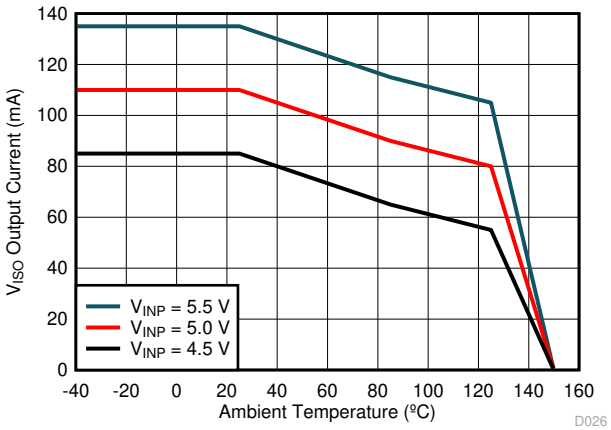
V_{ISO} = 3.3 V

図 6-6. Maximum V_{ISO} Output Power vs. Temperature



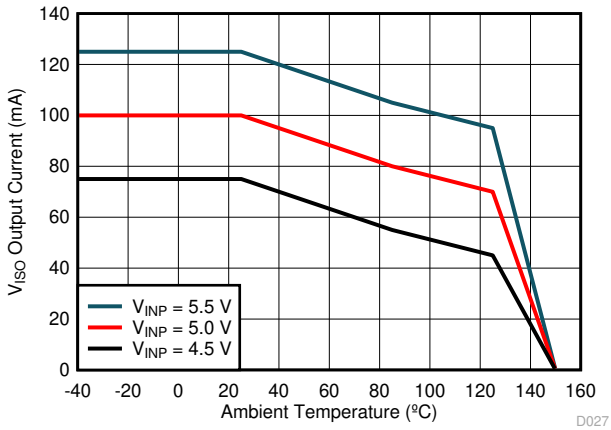
V_{ISO} = 3.7 V

図 6-7. Maximum V_{ISO} Output Power vs. Temperature



V_{ISO} = 5.0 V

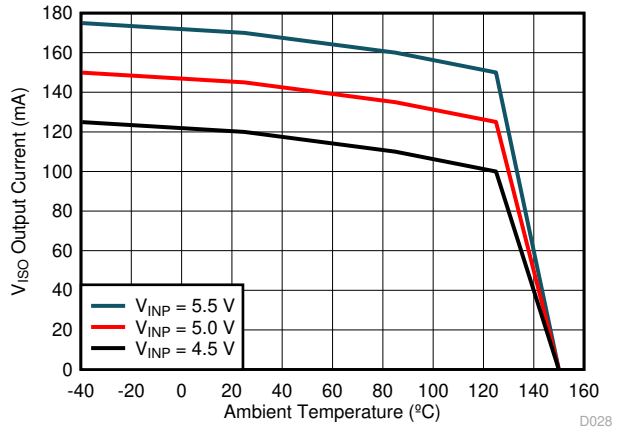
図 6-8. Maximum V_{ISO} Output Current vs. Temperature



V_{ISO} = 5.4 V

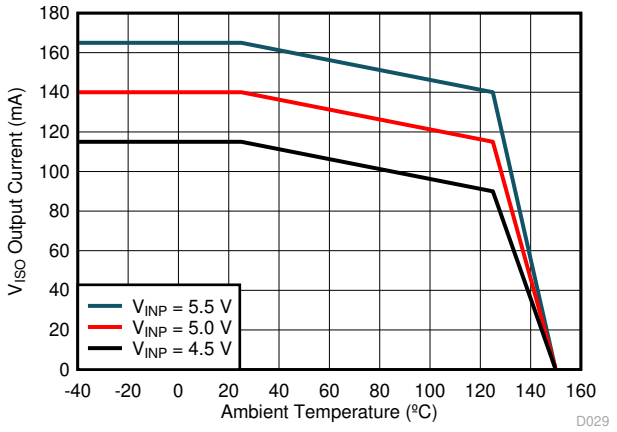
図 6-9. Maximum V_{ISO} Output Current vs. Temperature

6.12 Typical Characteristics (continued)



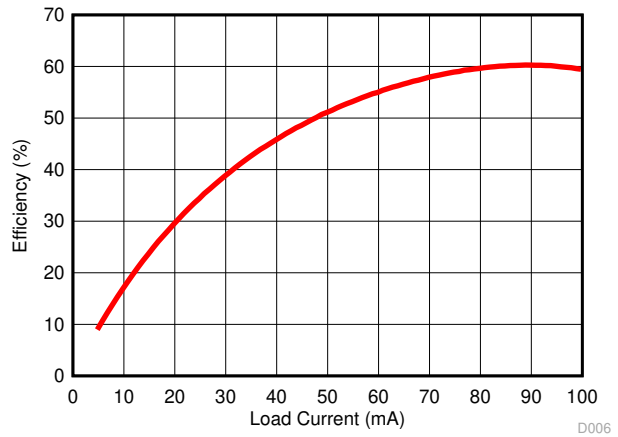
V_{ISO} = 3.3 V

図 6-10. Maximum V_{ISO} Output Current vs. Temperature



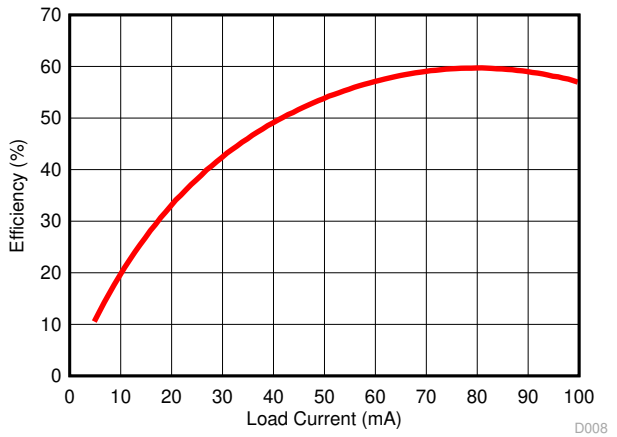
V_{ISO} = 3.7 V

図 6-11. Maximum V_{ISO} Output Current vs. Temperature



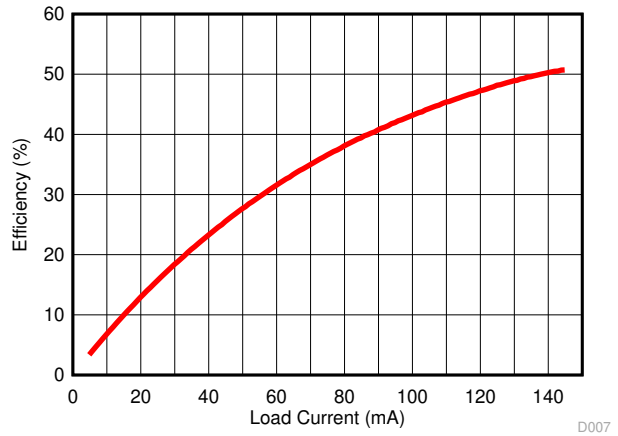
V_{INP} = 5.0 V V_{ISO} = 5.0 V T_A = 25°C

図 6-12. Power Supply Efficiency vs Load Current (I_{ISO})



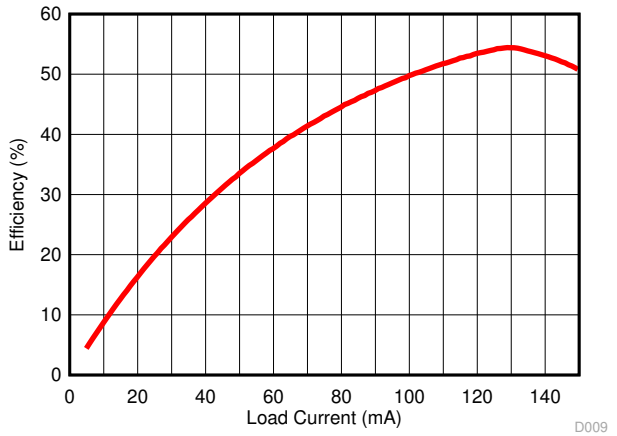
V_{INP} = 5.0 V V_{ISO} = 5.4 V T_A = 25°C

図 6-13. Power Supply Efficiency vs Load Current (I_{ISO})



V_{INP} = 5.0 V V_{ISO} = 3.3 V T_A = 25°C

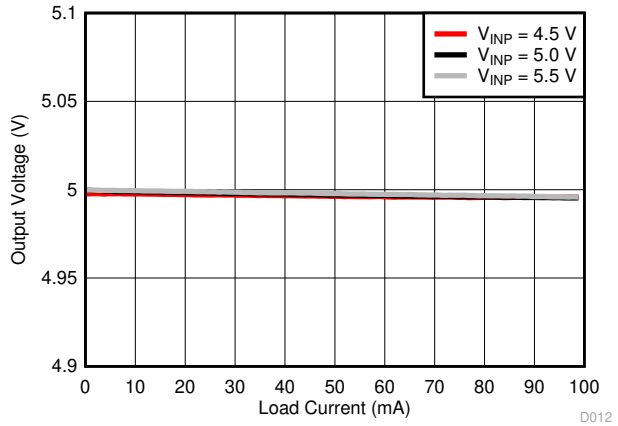
図 6-14. Power Supply Efficiency vs Load Current (I_{ISO})



V_{INP} = 5.0 V V_{ISO} = 3.7 V T_A = 25°C

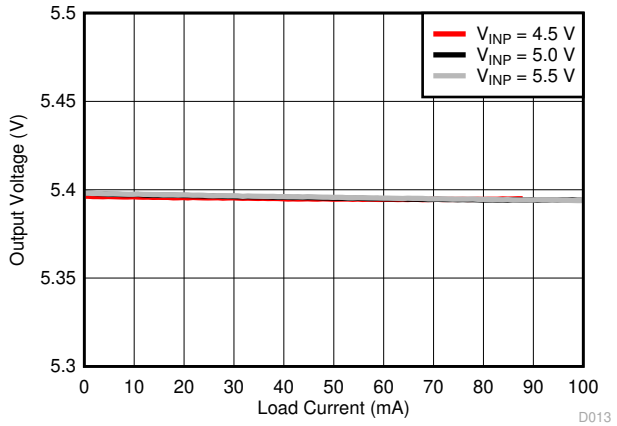
図 6-15. Power Supply Efficiency vs Load Current (I_{ISO})

6.12 Typical Characteristics (continued)



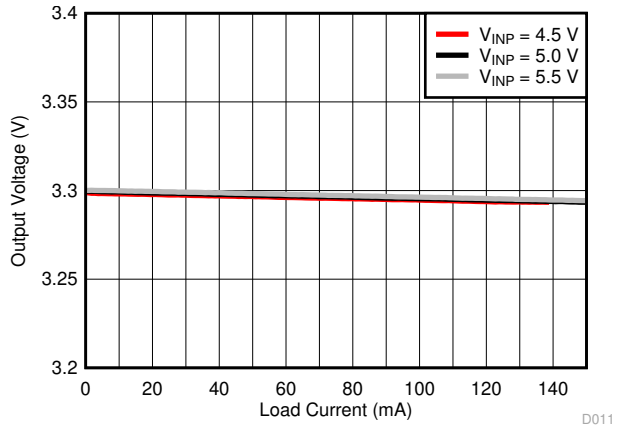
V_{ISO} = 5.0 V T_A = 25°C

図 6-16. Isolated Supply Voltage (V_{ISO}) vs Load Current (I_{ISO})



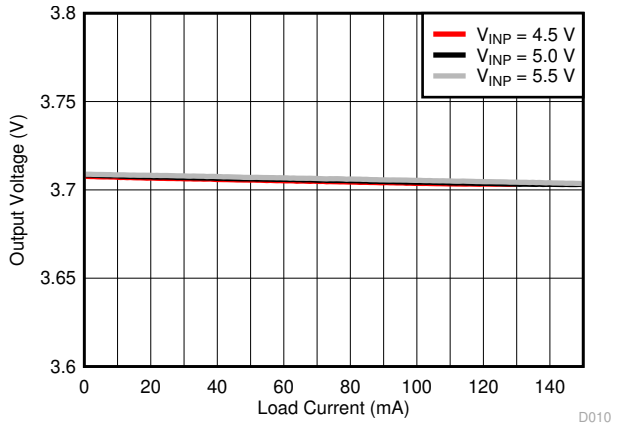
V_{ISO} = 5.4 V T_A = 25°C

図 6-17. Isolated Supply Voltage (V_{ISO}) vs Load Current (I_{ISO})



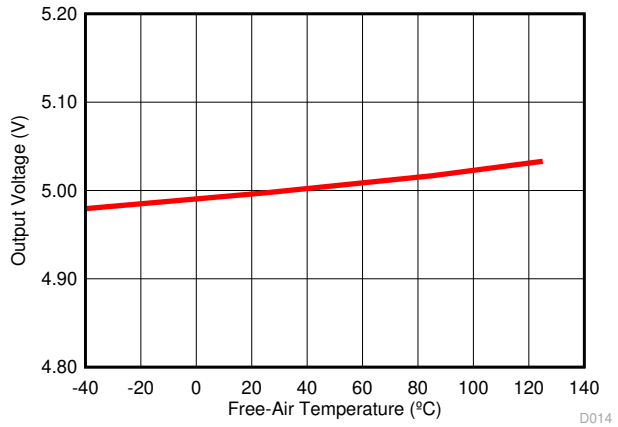
V_{ISO} = 3.3 V T_A = 25°C

図 6-18. Isolated Supply Voltage (V_{ISO}) vs Load Current (I_{ISO})



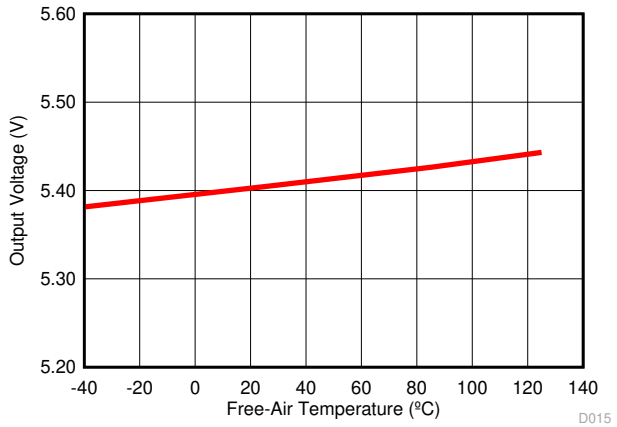
V_{ISO} = 3.7 V T_A = 25°C

図 6-19. Isolated Supply Voltage (V_{ISO}) vs Load Current (I_{ISO})



V_{INP} = 5.0 V V_{ISO} = 5.0 V I_{ISO} = 50 mA

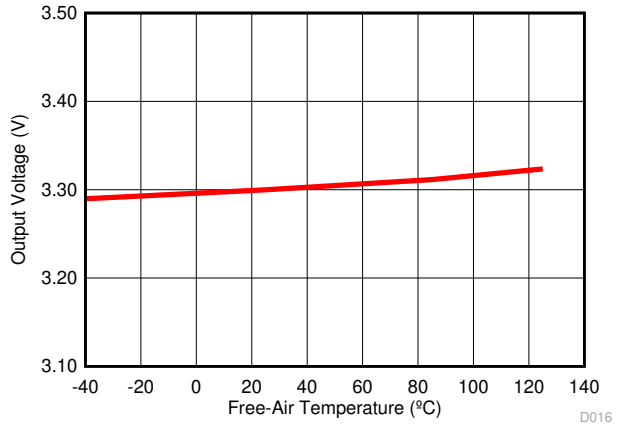
図 6-20. Isolated Supply Voltage (V_{ISO}) vs Free-Air Temperature



V_{INP} = 5.0 V V_{ISO} = 5.4 V I_{ISO} = 50 mA

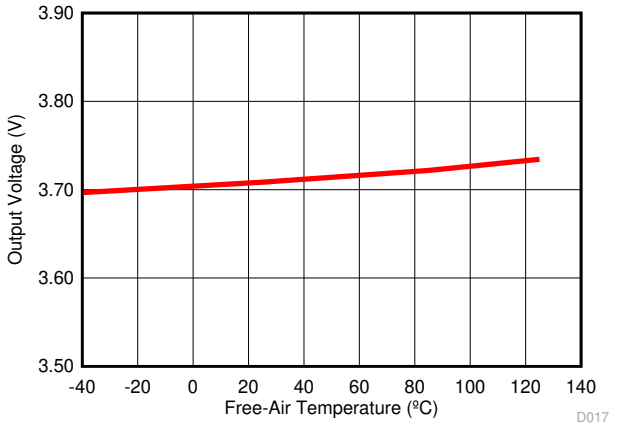
図 6-21. Isolated Supply Voltage (V_{ISO}) vs Free-Air Temperature

6.12 Typical Characteristics (continued)



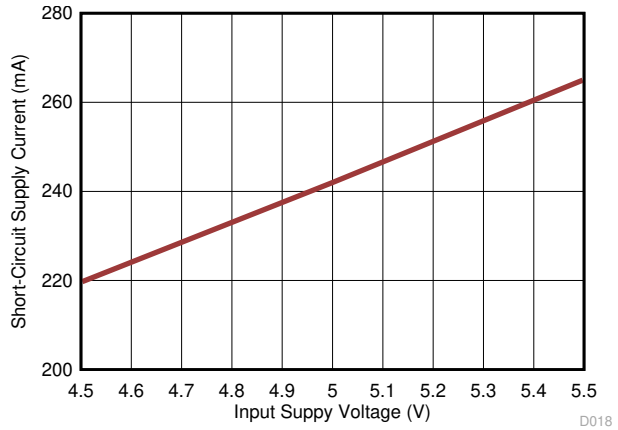
V_{INP} = 5.0 V V_{ISO} = 3.3 V I_{ISO} = 75 mA

図 6-22. Isolated Supply Voltage (V_{ISO}) vs Free-Air Temperature



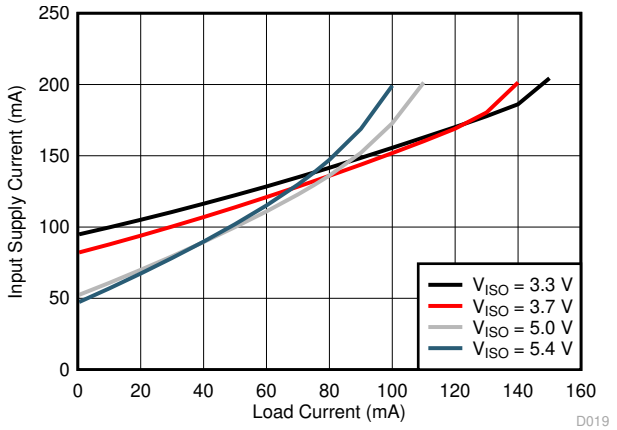
V_{INP} = 5.0 V V_{ISO} = 3.7 V I_{ISO} = 75 mA

図 6-23. Isolated Supply Voltage (V_{ISO}) vs Free-Air Temperature



T_A = 25°C

図 6-24. Short-Circuit Supply Current (I_{VIN_SC}) vs Supply Voltage (V_{INP})



V_{INP} = 5.0 V T_A = 25°C

図 6-25. Input Supply Current (I_{VINP}) vs Load Current (I_{ISO})

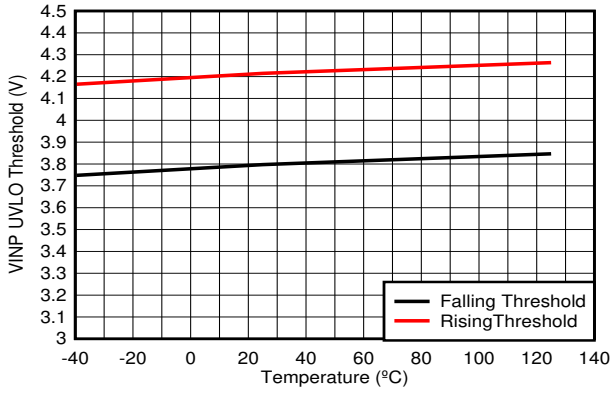


図 6-26. Typical V_{INP} UVLO Threshold vs Junction Temperature (T_J)

7 Detailed Description

7.1 Overview

The UCC12051-Q1 device integrates a high-efficiency, low-emissions isolated DC/DC converter. This approach provides typically 500 mW of clean, steady power across a 5000-V_{RMS} isolation barrier.

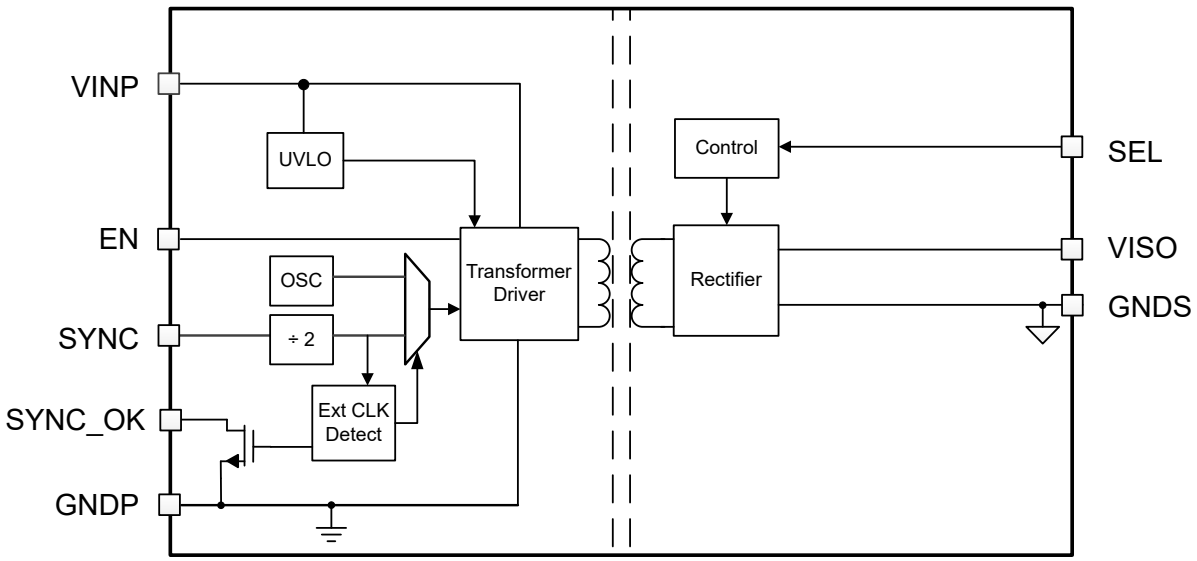
The integrated DC/DC converter uses switched mode operation and proprietary circuit techniques to reduce power losses and boost efficiency. Specialized control mechanisms, clocking schemes, and the use of an on-chip transformer provide high efficiency and low radiated emissions.

The VINP supply is provided to the primary power controller that switches the power stage connected to the integrated transformer. Power is transferred to the secondary side, rectified, and regulated to a level set by the SEL pin condition.

A fast feedback control loop monitors VISO and the output load, and ensures low overshoots and undershoots during load transients. Undervoltage lockout (UVLO) with hysteresis is integrated on the VINP supply, which ensures robust system performance under noisy conditions.

UCC12051-Q1 is suitable for applications that have limited board space and require more integration. These devices are also suitable for very-high voltage applications, where power transformers meeting the required isolation specifications are bulky and expensive.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable and Disable

Forcing EN low disables the device, which greatly reduces the VINP power consumption. Pull the EN pin high to enable normal device functionality. The EN pin has a weak internal pull-down resistor, so the device floats to the disable state if the pin is left open.

7.3.2 UVLO, Power-Up, and Power-Down Behavior

The UCC12051-Q1 has an undervoltage lockout (UVLO) on the VINP power supply. Upon power-up, while the VINP voltage is below the threshold voltage V_{UVPR}, the primary side transformer driver is disabled, and VISO output is off. The output powers up once the threshold is met. Likewise, if VINP falls below V_{UVPF}, the converter is disabled and there is no output at VISO. Both UVLO threshold voltages have hysteresis to avoid chattering.

7.3.3 V_{ISO} Load Recommended Operating Area

図 7-1 depicts the device V_{ISO} regulation behavior across the output load range, including when the output is overloaded. For proper device operation, ensure that the device VISO output load does not exceed the maximum output current (I_{OUT_MAX}). The value for I_{OUT_MAX} over different temperature and V_{INP} conditions are shown from 図 6-8 to 図 6-11. The following protection mechanisms will be engaged if the UCC12051-Q1 is loaded beyond the recommended operating area:

1. The device limits the maximum output power. If a load exceeding I_{OUT_MAX} is applied, V_{ISO} drops accordingly to meet the maximum power limit.
2. If V_{ISO} drops below nominal 3.8 V while operating in the constant power limit region, the over-power fold-back feature will switch the power converter from active rectification to passive rectification, and the built-in recovery hysteresis will ensure the UCC12051-Q1 recovers at a lower output power. The device returns to active rectification when load drops and V_{ISO} increases above nominal 4.3 V.
3. The device triggers a soft-start reset if V_{ISO} drops below the nominal 1.8-V threshold. This reset is designed to protect the device during V_{ISO} short-circuit conditions.
4. Thermal shutdown protection disables the converter if the device is operated in any of the above regions long enough to raise the silicon junction temperature above the thermal shutdown threshold. See the セクション 7.3.4 section for more details on this device feature.

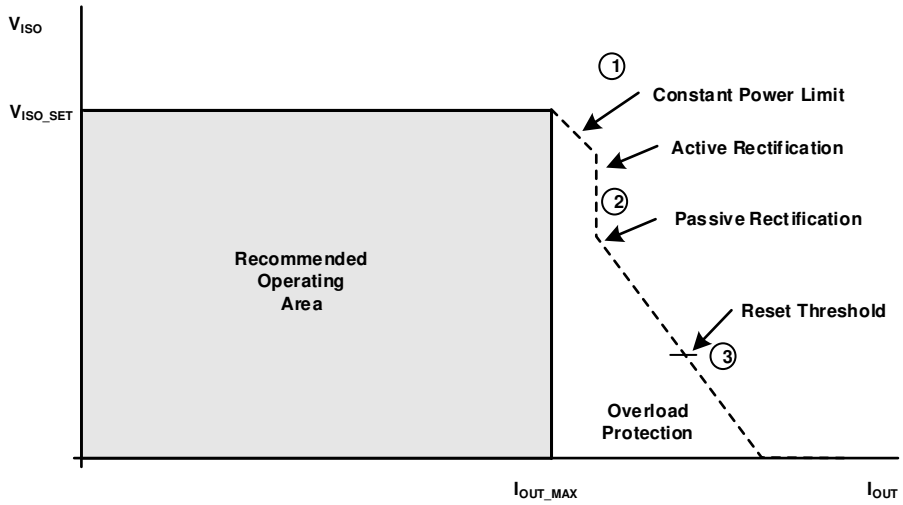


図 7-1. V_{ISO} Load Recommended Operating Area Description

7.3.4 Thermal Shutdown

Thermal protection is also integrated to help prevent the device from getting damaged during overload and short-circuit conditions on the isolated output. Under these conditions, the device temperature starts to increase. When the silicon junction temperature T_j sensed at the primary side die goes above the threshold TSD_{THR}(typical 165°C), thermal shutdown activates and the primary controller turns off which removes the energy supplied to the V_{ISO} load, which causes the device to cool off. When the junction temperature drops approximately 27°C (TSD_{HYST}) from the shutdown point, the device starts to function normally. If an overload or output short-circuit condition prevails, this protection cycle is repeated. Make sure the design prevents the device junction temperatures from reaching such high values.

7.3.5 External Clocking and Synchronization

The UCC12051-Q1 has an internal oscillator trimmed to drive the transformer at 8.0 MHz. An external clock may be applied at the SYNC pin to override the internal oscillator. This external clock will be divided by 2, so the target range for the external clock signal at SYNC is 16 MHz ±10%. When a valid external clock signal is detected, the internal spread spectrum modulation (SSM) algorithm is disabled. This allows an external clock signal with a unique SSM to be applied. The depth and frequency of SSM is a tradeoff verses low frequency modulated VISO voltage ripple. The SYNC_OK pin is asserted LOW if there is no external SYNC clock or one

that is outside of the operating range of the device is detected. In this state, the external clock is ignored and the DC/DC converter is clocked by the internal oscillator. The pin is in high-impedance if a valid clock is applied on SYNC.

7.3.6 V_{ISO} Output Voltage Selection

The SEL pin is monitored during power-up — within the first 1 ms after applying VINP above the UVLO rising threshold or enabling via the EN pin — to detect the desired regulation voltage for the VISO output. Note that after this initial monitoring, the SEL pin no longer affects the VISO output level. In order to change the output mode selection, either the EN pin must be toggled or the VINP power supply must be cycled off and back on. Section6.4 provides more details on the SEL pin functionality.

7.3.7 Electromagnetic Compatibility (EMC) Considerations

UCC12051-Q1 devices use spread spectrum modulation algorithm for the internal oscillator and advanced internal layout scheme to minimize radiated emissions at the system level.

Many applications in harsh environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as CISPR 25. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the device incorporates many chip-level design improvements for overall system robustness.

7.4 Device Functional Modes

表 7-1 lists the supply functional modes for this device.

表 7-1. Device Functional Modes

INPUTS		Isolated Supply Output Voltage (V_{ISO}) Setpoint
EN	SEL	
HIGH	Shorted to VISO	5.0 V
HIGH	100 kΩ to VISO	5.4 V
HIGH	Shorted to GNDS	3.3 V
HIGH	100 kΩ to GNDS	3.7 V
HIGH	OPEN(1)	UNSUPPORTED
LOW	X	0 V

(1) The SEL pin has an internal weak pull-down resistance to ground, but leaving this pin open is not recommended.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The UCC12051-Q1 device is suitable for applications that have limited board space and desire more integration. This device is also suitable for very high voltage applications, where power transformers meeting the required isolation specifications are bulky and expensive.

8.2 Typical Application

図 8-1 shows the typical application schematic for the UCC12051-Q1 device supplying an isolated load.

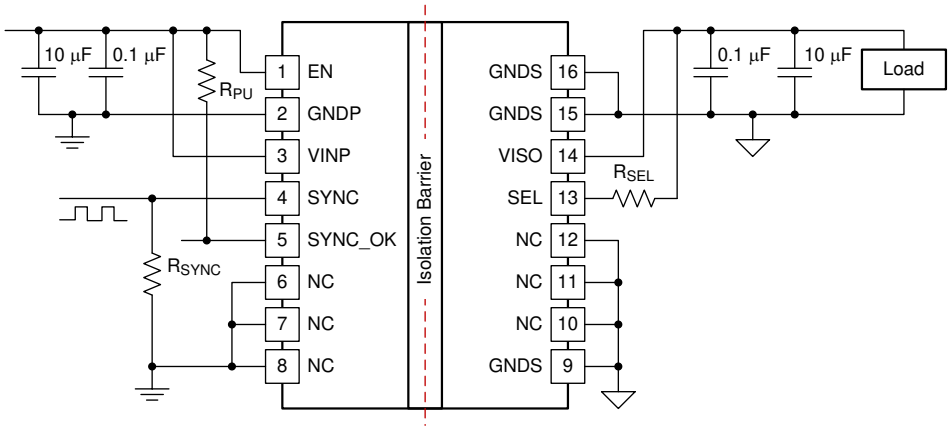


図 8-1. Typical Application

8.2.1 Design Requirements

To design using UCC12051-Q1, a few simple design considerations must be evaluated. 表 8-1 shows some recommended values for a typical application. See Power Supply Recommendations and Layout sections to review other key design considerations for the UCC12051-Q1 .

表 8-1. Design Parameters

PARAMETER	RECOMMENDED VALUE
Input supply voltage, V_{INP}	4.5 V to 5.5 V
Decoupling capacitance between V_{INP} and GNDP	10 µF, 16 V, ± 10%, X7R
Decoupling capacitance between V_{ISO} and GNDS (1)	10 µF, 16 V, ± 10%, X7R
Optional additional capacitance on VISO or VINP to reduce high-frequency ripple	0.1 µF, 50 V, ± 10%, X7R
Pull-up resistor from SYNC_OK to V_{INP}, R_{PU}	100 kΩ
Pull-up resistor from SEL to V_{ISO} for 5.0-V output voltage mode, R_{SEL}	0 Ω
Pull-up resistor from SEL to V_{ISO} for 5.4-V output voltage mode, R_{SEL}	100 kΩ
Optional SYNC signal impedance-matching resistor, R_{SYNC}	Match source — typical values are 50 Ω, 75 Ω, 100 Ω, or 1 kΩ
External clock signal applied on SYNC	16 MHz

(1) See VISO Output Capacitor Selection section.

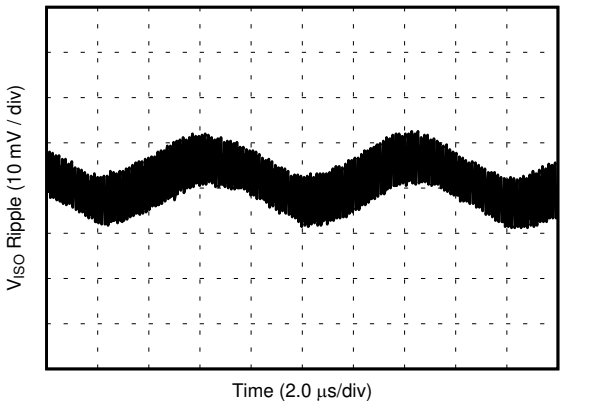
8.2.2 Detailed Design Procedure

Place ceramic decoupling capacitors as close as possible to the device pins. For the input supply, place the capacitor(s) between pin 3 (VINP) and pin 2 (GNDP). For the isolated output supply, place the capacitor(s) between pin 14 (VISO) and pin 15 (GNDS). This location is of particular importance to the input decoupling capacitor, because this capacitor supplies the transient current associated with the fast switching waveforms of the power drive circuits. The recommended capacitor value is 10 µF. Ensure the capacitor dielectric material is compatible with the target application temperature.

8.2.2.1 VISO Output Capacitor Selection

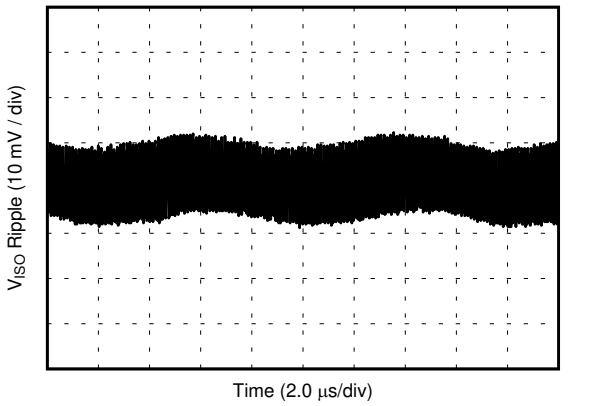
The UCC12051-Q1 is optimized to run with an effective output capacitance of 5 µF to 20 µF. A ceramic capacitor is recommended. Ceramic capacitors have DC-Bias and temperature derating effects, which both have influence the final effective capacitance. Choose the right capacitor carefully in combination with considering its package size, dielectric and voltage rating. It is good design practice to include one 0.1-µF capacitor close to the device for high-frequency noise reduction.

8.2.3 Application Curves



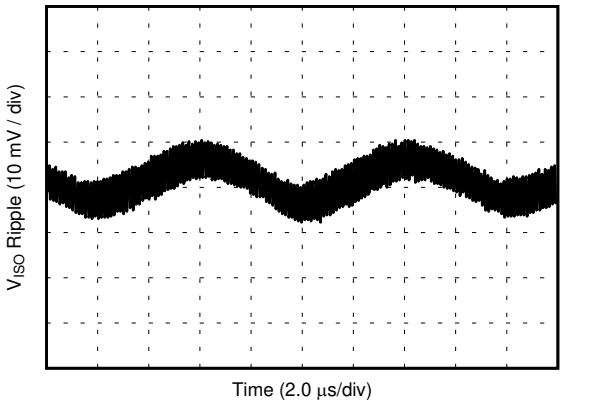
V_{INP} = 5.0 V V_{ISO} = 5.4 V Bandwidth = 20 MHz

図 8-2. V_{ISO} Ripple, 5.4-V Output, 10% Load



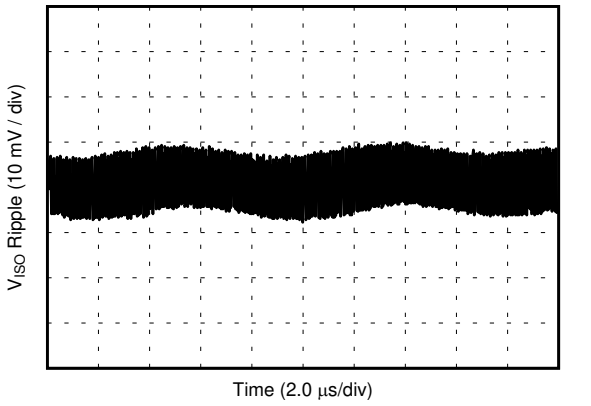
V_{INP} = 5.0 V V_{ISO} = 5.4 V Bandwidth = 20 MHz

図 8-3. V_{ISO} Ripple, 5.4-V Output, 90% Load



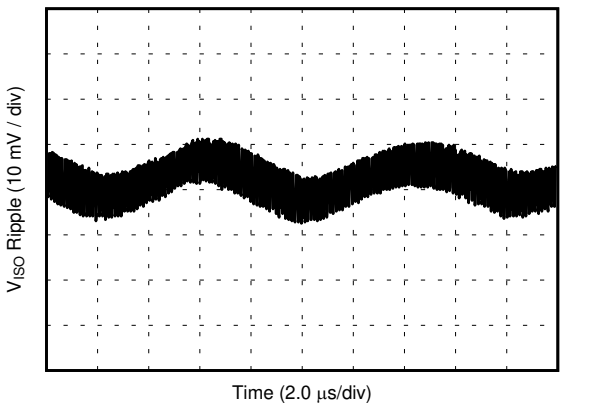
V_{INP} = 5.0 V V_{ISO} = 5.0 V Bandwidth = 20 MHz

図 8-4. V_{ISO} Ripple, 5.0-V Output, 10% Load



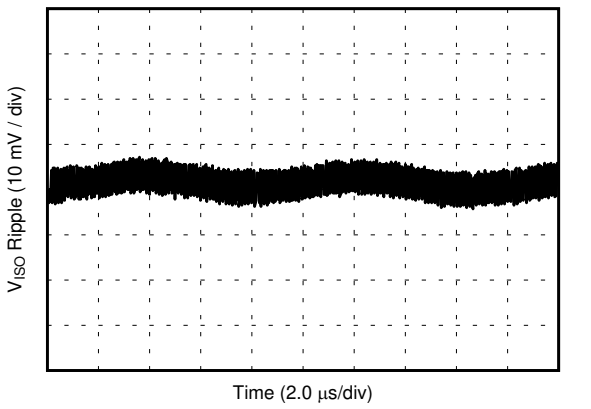
V_{INP} = 5.0 V V_{ISO} = 5.0 V Bandwidth = 20 MHz

図 8-5. V_{ISO} Ripple, 5.0-V Output, 90% Load



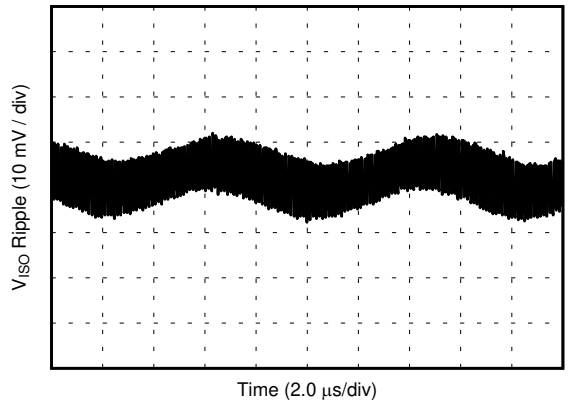
V_{INP} = 5.0 V V_{ISO} = 3.7 V Bandwidth = 20 MHz

図 8-6. V_{ISO} Ripple, 3.7-V Output, 10% Load



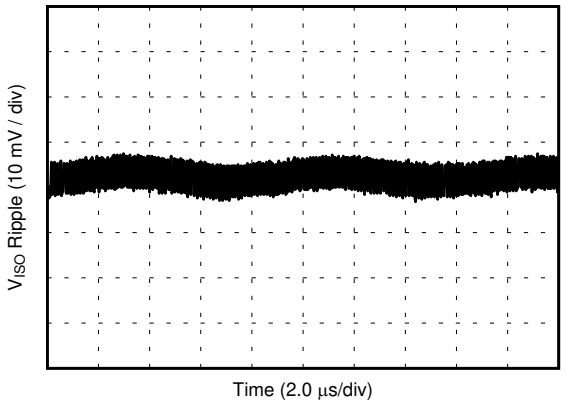
V_{INP} = 5.0 V V_{ISO} = 3.7 V Bandwidth = 20 MHz

図 8-7. V_{ISO} Ripple, 3.7-V Output, 90% Load



V_{INP} = 5.0 V V_{ISO} = 3.3 V Bandwidth = 20 MHz

図 8-8. V_{ISO} Ripple, 3.3-V Output, 10% Load



V_{INP} = 5.0 V V_{ISO} = 3.3 V Bandwidth = 20 MHz

図 8-9. V_{ISO} Ripple, 3.3-V Output, 90% Load

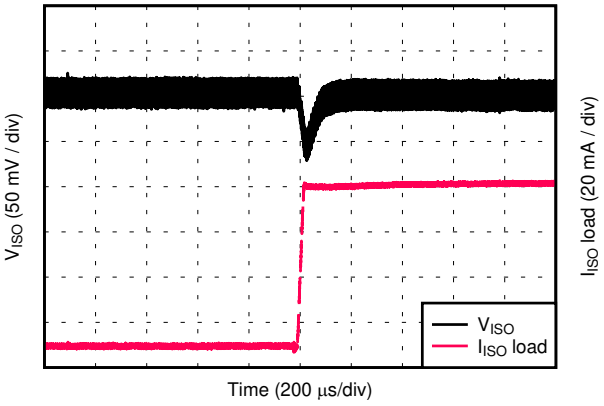


図 8-10. V_{ISO} Load Transient Response, 10% to 90% Load Step, 5.0-V Input, 5.4-V Output

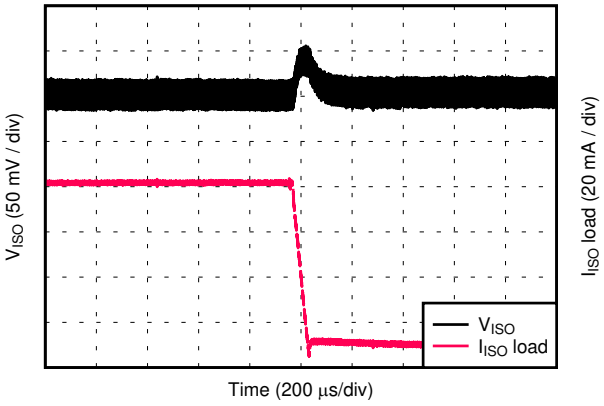


図 8-11. V_{ISO} Load Transient Response, 90% to 10% Load Step, 5.0-V Input, 5.4-V Output

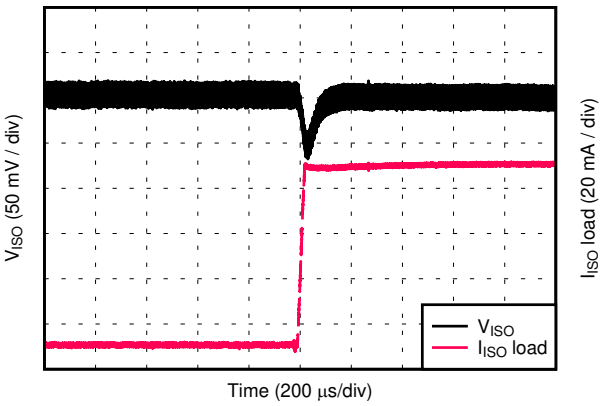


図 8-12. V_{ISO} Load Transient Response, 10% to 90% Load Step, 5.0-V Input, 5.0-V Output

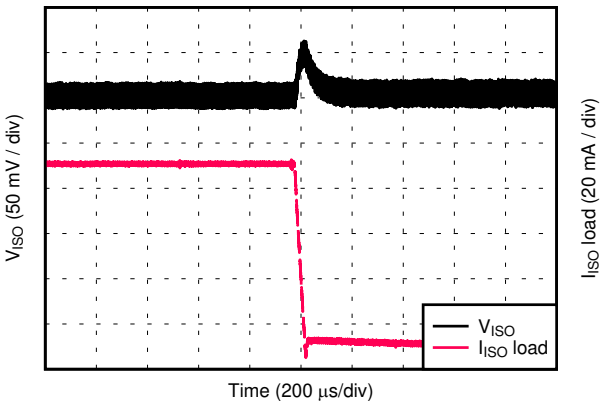


図 8-13. V_{ISO} Load Transient Response, 90% to 10% Load Step, 5.0-V Input, 5.0-V Output

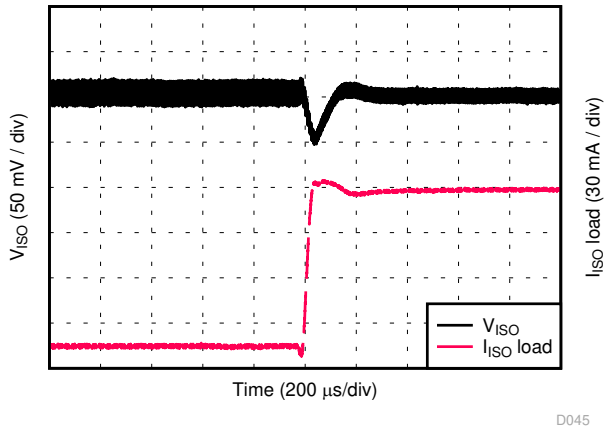


図 8-14. V_{ISO} Load Transient Response, 10% to 90% Load Step, 5.0-V Input, 3.7-V Output

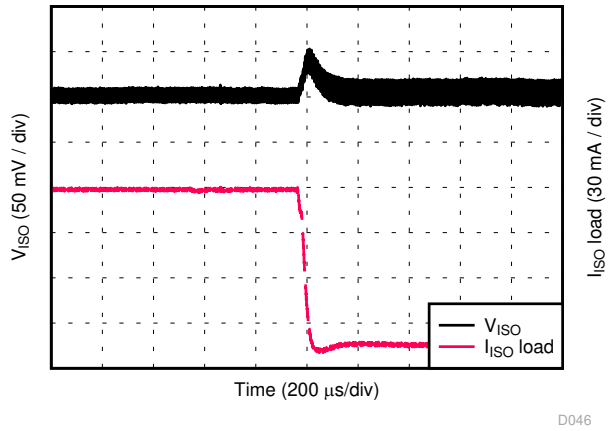


図 8-15. V_{ISO} Load Transient Response, 90% to 10% Load Step, 5.0-V Input, 3.7-V Output

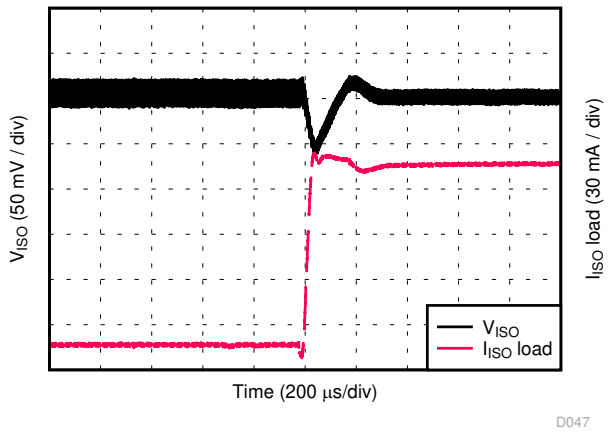


図 8-16. V_{ISO} Load Transient Response, 10% to 90% Load Step, 5.0-V Input, 3.3-V Output

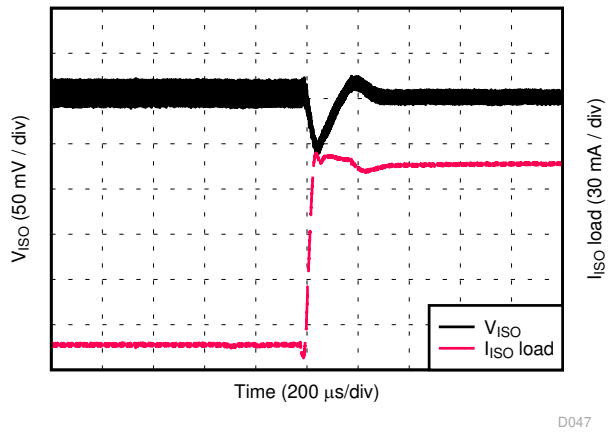


図 8-17. V_{ISO} Load Transient Response, 90% to 10% Load Step, 5.0-V Input, 3.3-V Output

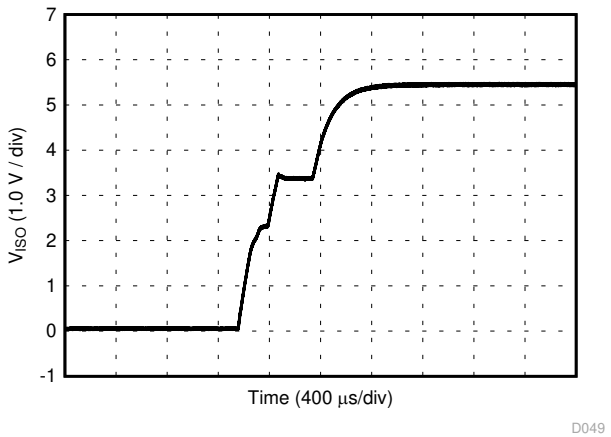


図 8-18. V_{ISO} Soft Start at 10% Rated Load, 5.0-V Input, 5.4-V Output

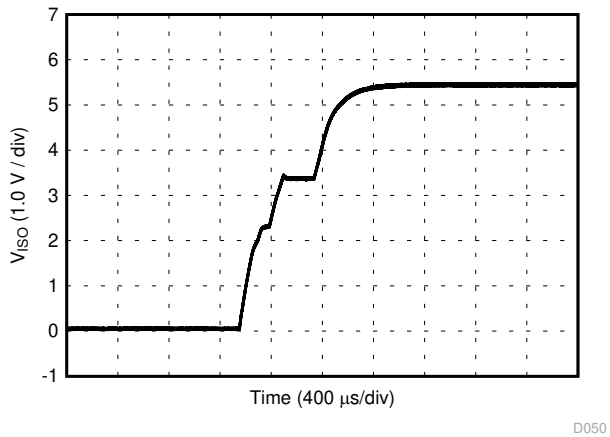


図 8-19. V_{ISO} Soft Start at 90% Rated Load, 5.0-V Input, 5.4-V Output

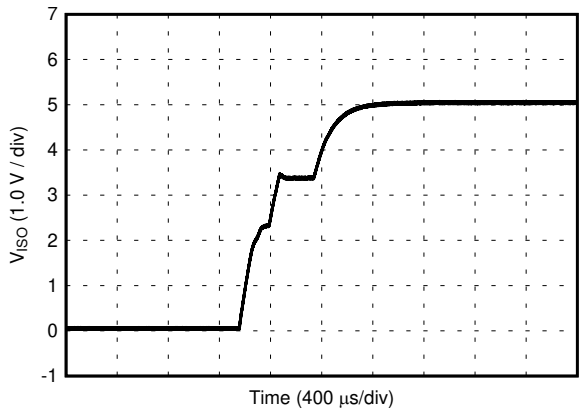


図 8-20. V_{ISO} Soft Start at 10% Rated Load, 5.0-V Input, 5.0-V Output

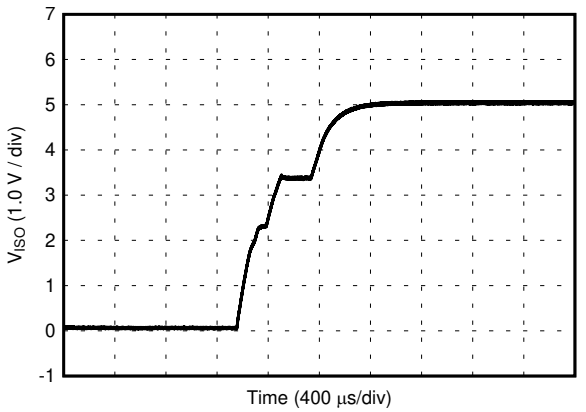


図 8-21. V_{ISO} Soft Start at 90% Rated Load, 5.0-V Input, 5.0-V Output

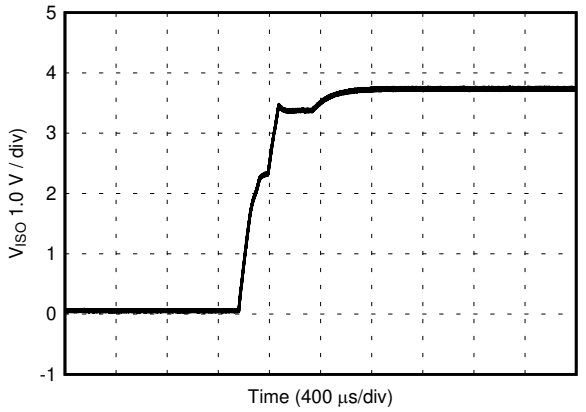


図 8-22. V_{ISO} Soft Start at 10% Rated Load, 5.0-V Input, 3.7-V Output

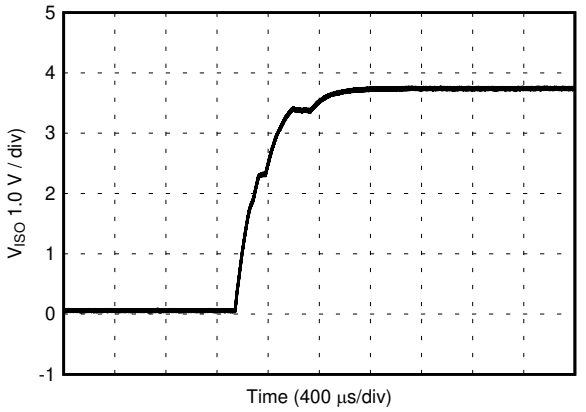


図 8-23. V_{ISO} Soft Start at 90% Rated Load, 5.0-V Input, 3.7-V Output

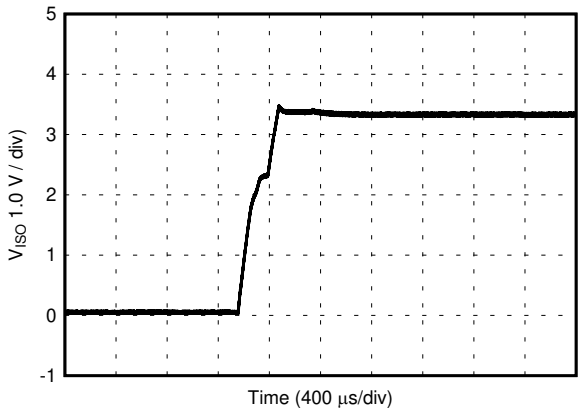


図 8-24. V_{ISO} Soft Start at 10% Rated Load, 5.0-V Input, 3.3-V Output

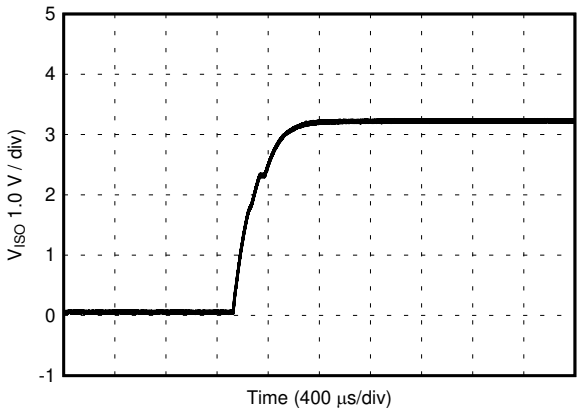


図 8-25. V_{ISO} Soft Start at 90% Rated Load, 5.0-V Input, 3.3-V Output

9 Power Supply Recommendations

The recommended input supply voltage (VINP) for the UCC12051-Q1 is between 4.5 V and 5.5 V. To help ensure reliable operation, adequate decoupling capacitors must be located as close to supply pins as possible. Place local bypass capacitors between the VINP and GNDP pins at the input, and between VISO and GNDS at the isolated output supply. Low ESR, ceramic surface mount capacitors are recommended. It is further suggested that one place two such capacitors: one with a value of 10 µF for supply bypassing, and an additional 100-nF capacitor in parallel for high frequency filtering. The input supply must have an appropriate current rating to support output load required by the end application.

10 Layout

10.1 Layout Guidelines

The UCC12051-Q1 integrated isolated power solution simplifies system design and reduces board area usage. Proper PCB layout is important in order to achieve optimum performance. Here is a list of recommendations:

1. Place decoupling capacitors as close as possible to the device pins. For the input supply, place the capacitor(s) between pin 3 (VINP) and pin 2 (GNDP). For the isolated output supply, place the capacitor(s) between pin 14 (VISO) and pin 15 (GNDS). This location is of particular importance to the input decoupling capacitor, because this capacitor supplies the transient current associated with the fast switching waveforms of the power drive circuits.
2. Because the device does not have a thermal pad for heat-sinking, the device dissipates heat through the respective GND pins. Ensure that enough copper (preferably a connection to the ground plane) is present on all GNDP and GNDS pins for best heat-sinking.
3. If space and layer count allow, it is also recommended to connect the VINP, GNDP, VISO and GNDS pins to internal ground or power planes through multiple vias of adequate size. Alternatively, make traces for these nets as wide as possible to minimize losses.
4. TI also recommends grounding the no-connect pins (NC) to their respective ground planes. For pins 6, 7, and 8, connect to GNDP. For pins 10, 11, and 12, connect to GNDS. This will allow more continuous ground planes and larger thermal mass for heat-sinking.
5. A minimum of four layers is recommended to accomplish a low-EMI PCB design. Inner layers can be spaced closer than outer layers and used to create a high-frequency bypass capacitor between GNDP and GNDS to reduce radiated emissions. Ensure proper spacing, both inter-layer and layer-to-layer, is implemented to avoid reducing isolation capabilities. These spacings will vary based on the printed circuit board construction parameters, such as dielectric material and thickness.
6. Pay close attention to the spacing between primary ground plane (GNDP) and secondary ground plane (GNDS) on the PCB outer layers. The effective creepage and or clearance of the system will be reduced if the two ground planes have a lower spacing than that of the device package.
7. To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the UCC12051-Q1 device on the outer copper layers.

10.2 Layout Example

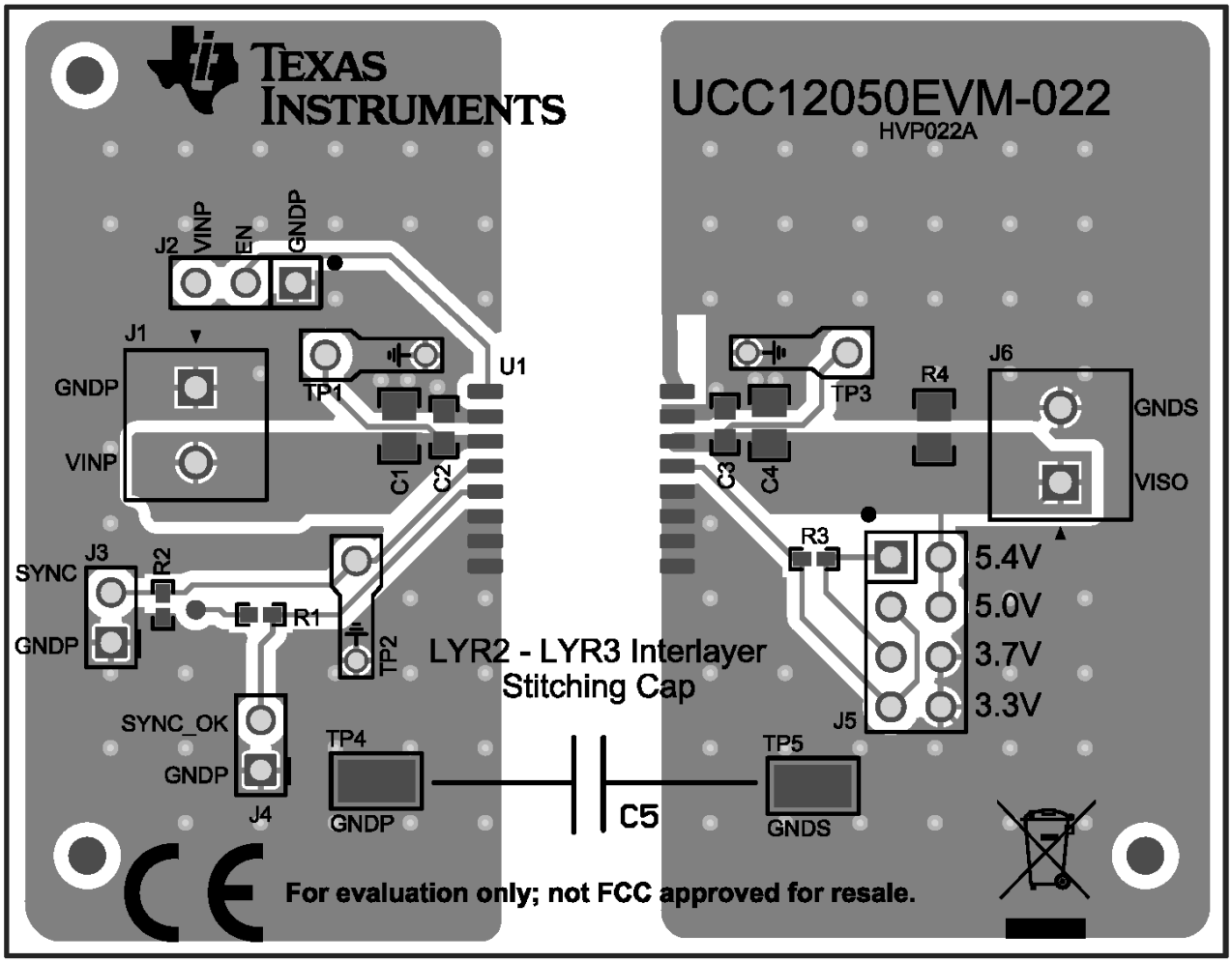


図 10-1. Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

For development support, refer to:

- Isolated 5-V bias supply for automotive CISPR 25, class 5 emissions, reference design

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- UCC12050 Evaluation Module User Guide
- Isolation Glossary

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 サポート・リソース

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11.5 Trademarks

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC12051QDVERQ1	Active	Production	SO-MOD (DVE) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCC12051Q1
UCC12051QDVERQ1.A	Active	Production	SO-MOD (DVE) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCC12051Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

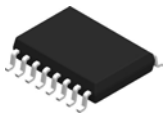
(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

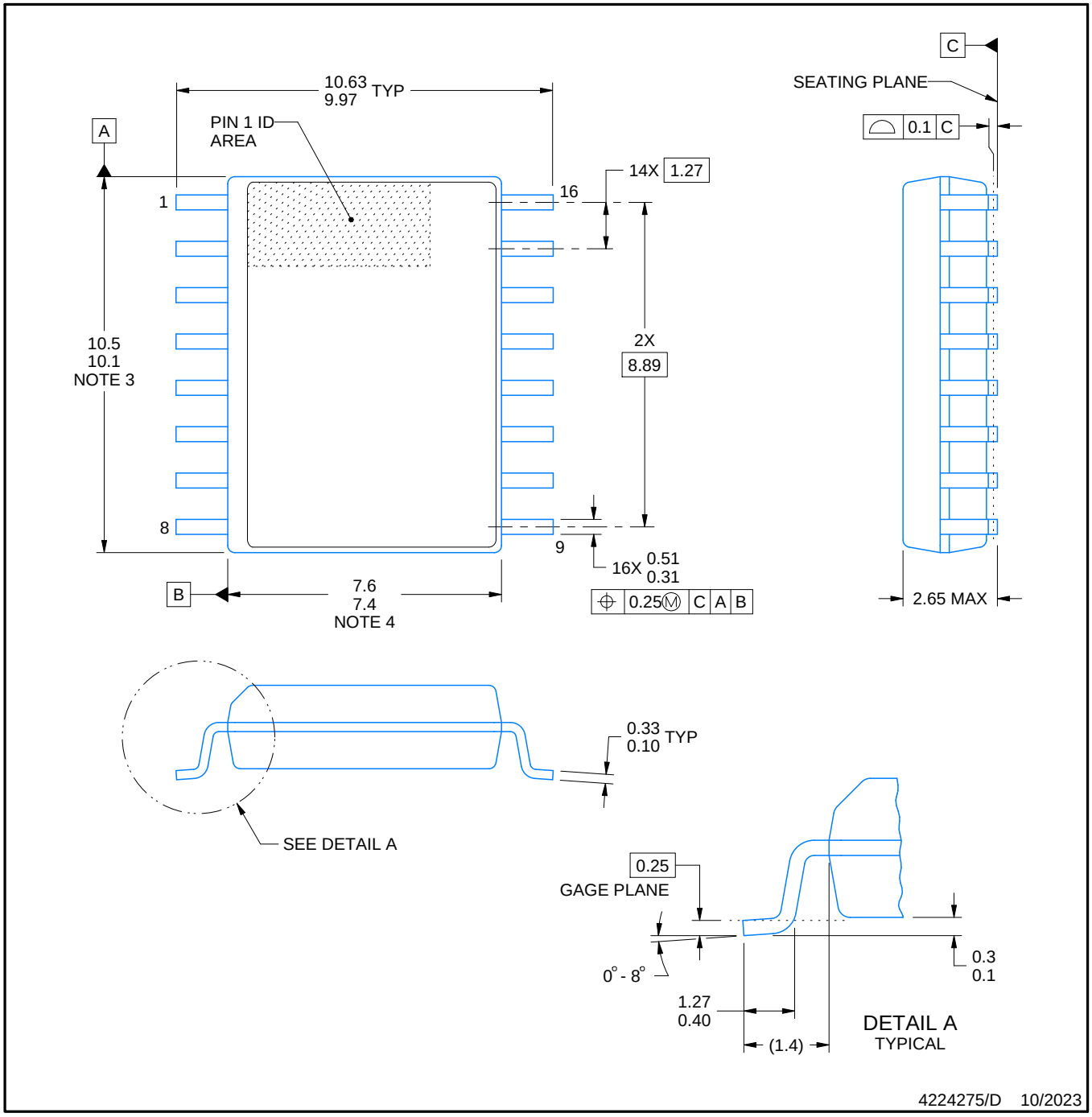


PACKAGE OUTLINE

DVE0016A

SO-MOD - 2.65 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

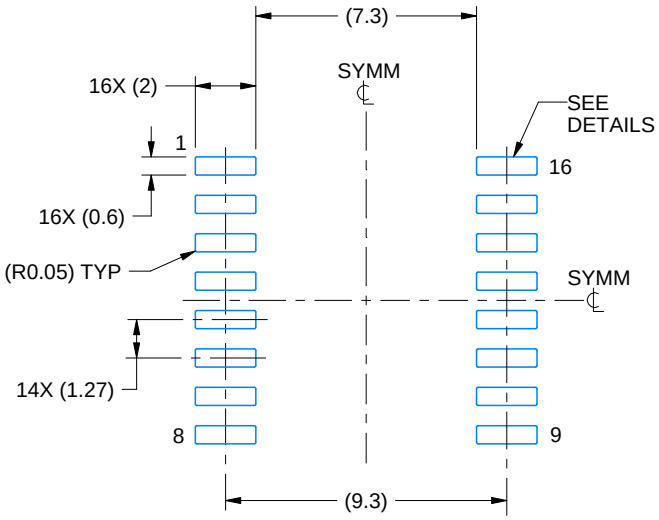
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

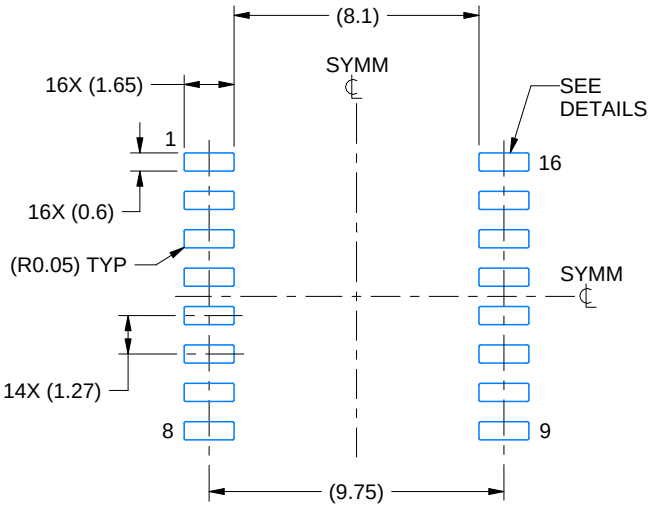
DVE0016A

SO-MOD - 2.65 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

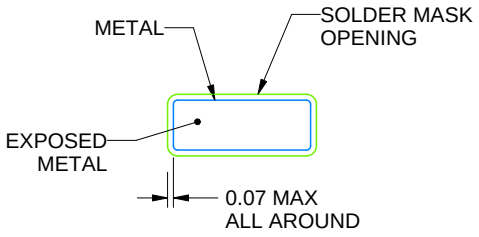


IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

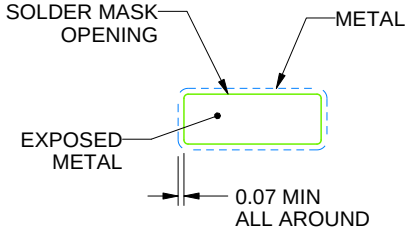


HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:4X



NON SOLDER MASK
DEFINED



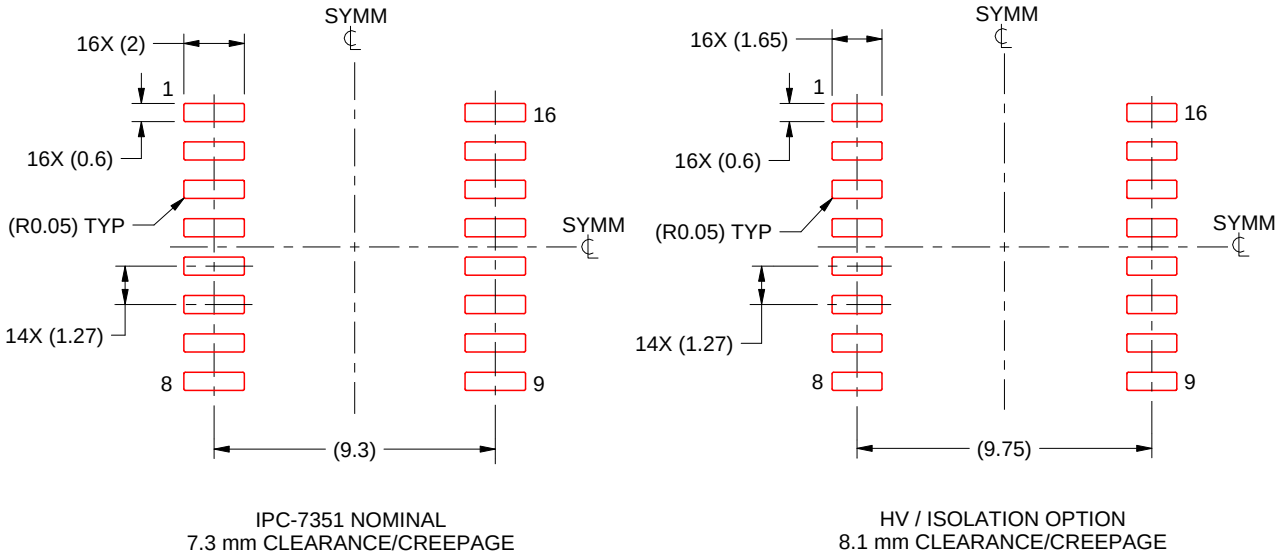
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4224275/A 10/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4224275/D 10/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

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最終更新日：2025 年 10 月