UCC14141-Q1 車載用 1.5W、12V V_{IN}、25V V_{OUT}、高密度、>5kV_{RMS}、絶縁型 DC/DC モジュール

1 特長

- 絶縁変圧器付きの統合型高密度絶縁型 DC/DC モジュール
- 以下のものを駆動する絶縁型 DC/DC：IGBT、SiC FET
- 入力電圧範囲：8V～18V、絶対最大定格 32V
- T_A ≤ 85℃で、10.8V < V_{VIN} < 13.2V に対して 1.5W の出力電力
- T_A ≤ 85℃で、8V < V_{VIN} < 18V に対して 1W の出力電力
- 可変 (VDD - VEE) 出力電圧 (外付け抵抗による)：すべての温度範囲にわたって 15V～25V、±1.3% のレギュレーション精度
- 可変 (COM - VEE) 出力電圧 (外付け抵抗による)：すべての温度範囲にわたって 2.5V～(VDD - VEE)、±1.3% のレギュレーション精度
- スペクトラム拡散変調とトランス内蔵の設計により、低い電磁放射を実現
- イネーブル、パワー・グッド、UVLO、OVLO、ソフトスタート、短絡、電力制限、低電圧、過電圧、過熱からの保護
- CMTI > 150kV/μs
- 車載アプリケーション向けに AEC-Q100 認定済み
  - 温度グレード 1：-40℃ ≤ T_J ≤ 150℃
  - 温度グレード 1：-40℃ ≤ T_A ≤ 125℃
- 機能安全対応
  - 機能安全システム設計に役立つ資料を利用可能
- 安全関連の認証計画：
  - DIN EN IEC 60747-17 (VDE 0884-17) に準拠した強化絶縁耐圧：7071VPK
  - UL 1577 による 5000VRMS 絶縁 (1 分間)
  - CQC GB4943.1 準拠の強化絶縁
- 36 ピンのワイド SSOP パッケージ

2 アプリケーション

- ハイブリッド、電気自動車、およびパワートレイン・システム (EV/HEV)
  - インバータおよびモータ制御
  - オンボード充電器 (OBC) およびワイヤレス充電器
  - DC/DC コンバータ
- グリッド・インフラ
  - EV 充電ステーション向け電源モジュール
  - DC 充電 (パイル) ステーション
  - ストリング・インバータ
- モータ駆動
  - AC インバータと VF ドライブ、ロボット・サーボ・ドライブ
- 産業用輸送
  - オフハイウェイ車両向け電気式ドライブ

3 概要

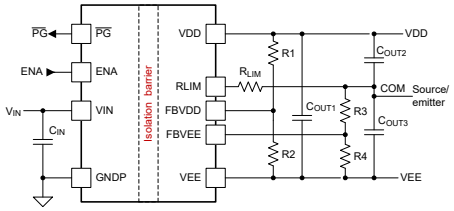
UCC14141-Q1 は、IGBT または SiC ゲート・ドライバへの電力供給を目的として設計された車載認定済み高絶縁電圧 DC/DC 電源モジュールです。UCC14141-Q1 は、独自のアーキテクチャを採用した変圧器と DC/DC コントローラを統合しており、非常に低い放射で高密度を実現します。高精度の出力電圧により優れたチャネル拡張を実現し、パワー・デバイスのゲートに過大なストレスを与えずにシステム効率を向上します。UCC14141-Q1 の入力電圧は、電気自動車の幅広い $LiFePO_4$ バッテリ電圧 (8V～18V) と、レギュレートされた 12V レール (10.8V～13.2V) の両方を、異なる出力電力でサポートしています。

オンチップのデバイス保護機能を備えた高集積モジュールは、必要な外付け部品が最小限で、入力低電圧誤動作防止、過電圧誤動作防止、出力電圧パワーグッド・コンパレータ、過熱シャットダウン、ソフトスタート・タイムアウト、調整可能で絶縁された正負出力電圧、イネーブル・ピン、オープン・ドレイン出力パワーグッド・ピンなどの追加機能を備えています。

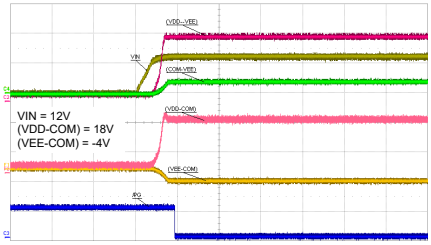
製品情報

発注型番(1)	パッケージ	本体サイズ (公称)
UCC14141QDWNRQ1	SSOP	12.83mm × 7.50mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



アプリケーション概略図



代表的な電源投入シーケンス

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Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (March 2023) to Revision B (June 2023)	Page
• 初版リリース	1

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5 Device Comparison

表 5-1. Device Comparison Table

DEVICE NAME	V_{VIN} Range	Output (VDD-VEE) Adjustable Range	Typical power	Isolation rating
UCC14240-Q1	21 V to 27 V	15 V to 25 V	2 W	Basic
UCC14241-Q1	21 V to 27 V	15 V to 25 V	2 W	Reinforced
UCC14140-Q1	8 V to 18 V	15 V to 25 V	1 W	Basic
	10.8 V to 13.2 V	15 V to 25 V	1.5 W	
UCC14141-Q1	8 V to 18 V	15 V to 25 V	1 W	Reinforced
	10.8 V to 13.2 V	15 V to 25 V	1.5 W	
UCC14341-Q1	13.5 V to 16.5 V	15 V to 25 V	1.5 W	Reinforced
UCC14131-Q1	12 V to 15 V	12 V to 15 V	1.5 W	Reinforced
	15 V to 18 V	15 V to 18 V	1.5 W	
	10 V to 18 V	10 V to 12 V	1 W	
	14 V to 18 V	10 V to 18 V	1 W	

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6 Pin Configuration and Functions

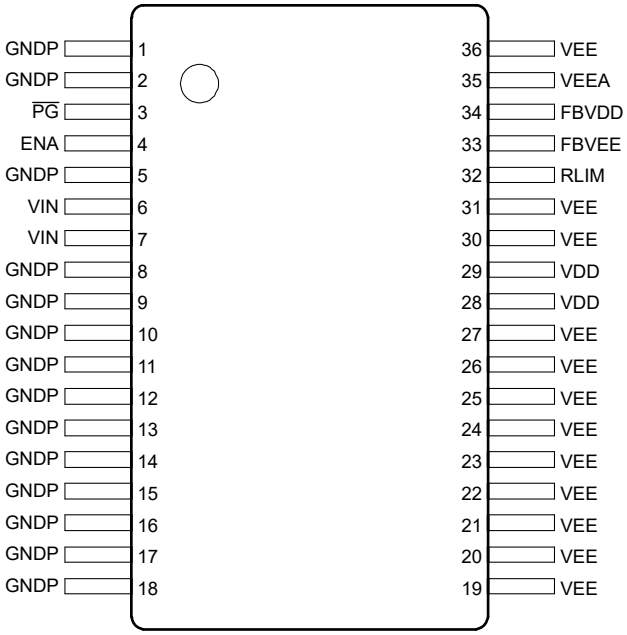

図 6-1. DWN Package, 36-Pin SSOP (Top View)

表 6-1. Pin Functions

PIN		TYPE (1)	DESCRIPTION
NAME	NO.		
GNDP	1, 2, 5, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18	G	Primary-side ground connection for VIN. PIN 1,2, and 5 are analog ground. PIN 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, and 18 are power ground. Place several vias to copper pours for thermal relief. See *Layout Guidelines*.
$\overline{PG}$	3	O	Active low power-good open-drain output pin. $\overline{PG}$ remains low when ($V_{VIN\_UVLOP} \le V_{VIN} \le V_{VIN\_OVLOP}$); ($V_{VDD\_UVP} \le V_{FBVDD} \le V_{VDD\_OVP}$); ($V_{VEE\_UVP} \le V_{FBVEE} \le V_{VEE\_OVP}$); $T_{J\_Primary} \le TSHUTP_{PRIMARY\_RISE}$; and $T_{J\_secondary} \le TSHUTS_{SECONDARY\_RISE}$
ENA	4	I	Enable pin. Forcing ENA LOW disables the device. Pull HIGH to enable normal device functionality. 5.5-V recommended maximum.
VIN	6, 7	P	Primary input voltage. PIN 6 is for analog input, and PIN 7 is for power input. For PIN 7, connect two 10-µF ceramic capacitor from power VIN PIN 7 to power GNDP PIN 8. Connect a 0.1-µF high-frequency bypass ceramic capacitor close to PIN 7 and PIN 8.
VEE	19, 20, 21, 22, 23, 24, 25,26, 27, 30,31, 36	G	Secondary-side reference connection for VDD and COM. The VEE pins are used for the high current return paths.

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表 6-1. Pin Functions (continued)

PIN		TYPE (1)	DESCRIPTION
NAME	NO.		
VDD	28, 29	P	Secondary-side isolated output voltage from transformer. Connect a 10-µF and a parallel 0.1-µF ceramic capacitor from VDD to VEE. The 0.1-µF ceramic capacitor is the high frequency bypass and must be next to the IC pins.
RLIM	32	P	Secondary-side second isolated output voltage resistor to limit the source current from VDD to COM node, and the sink current from COM to VEE. Connect a resistor from RLIM to COM to regulate the (COM – VEE) voltage. See *R_{LIM} Resistor Selection* for more detail.
FBVEE	33	I	Feedback (COM – VEE) output voltage sense pin used to adjust the output (COM – VEE) voltage. Connect a resistor divider from COM to VEE so that the midpoint is connected to FBVEE, and the equivalent FBVEE voltage when regulating is 2.5 V. Add a 330-pF ceramic capacitor for high frequency decoupling in parallel with the low-side feedback resistor. The 330-pF ceramic capacitor for high frequency bypass must be next to the FBVEE and VEEA IC pins on top layer or back layer connected with vias.
FBVDD	34	I	Feedback (VDD – VEE) output voltage sense pin and to adjust the output (VDD – VEE) voltage. Connect a resistor divider from VDD to VEE so that the midpoint is connected to FBVDD, and the equivalent FBVDD voltage when regulating is 2.5 V. Add a 330-pF ceramic capacitor for high frequency decoupling in parallel with the low-side feedback resistor. The 330-pF ceramic capacitor for high frequency bypass must be next to the FBVDD and VEEA IC pins on top layer or back layer connected with vias.
VEEA	35	G	Secondary-side analog sense reference connection for the noise sensitive analog feedback inputs, FBVDD and FBVEE. Connect the low-side feedback resistors and high frequency decoupling filter capacitor close to the VEEA pin and respective feedback pin FBVDD or FBVEE. Connect to secondary-side gate drive lowest voltage reference, VEE. Use a single point connection and place the high frequency decoupling ceramic capacitor close to the VEEA pin. See *Layout Guidelines*.

(1) P = power, G = ground, I = input, O = output

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

Parameter		MIN	TYP	MAX	UNIT
	VIN to GNDP	–0.3		32	V
	ENA, $\overline{PG}$ to GNDP	–0.3		7	V
	VDD, VEE, RLIM, FBVDD, FBVEE to VEE	–0.3		32	V
$P_{OUT\_VDD\_MAX}$	Total (VDD-VEE) output power at T_A=25°C			2.5	W
$I_{RLIM\_MAX\_RMS\_SOURCE}$	Max RLIM pin rms current sourcing from VDD to RLIM. (16% average run time over lifetime of 24,500 hr)			0.125	A
$I_{RLIM\_MAX\_RMS\_SINK}$	Max RLIM pin rms current sinking from RLIM to VEE. (16% average run time over lifetime of 24,500 hr)			0.125	A
T_J	Operating junction temperature range	–40		150	°C
T_{stg}	Storage temperature	–65		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011 Section 7.2	±500	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PIN		MIN	TYP	MAX	UNIT
V_{VIN}	Primary-side input voltage to GNDP	8(1)	12	18	V
V_{ENA}	Enable to GNDP	0		5.5	V
$V_{\overline{PG}}$	Powergood to GNDP	0		5.5	V
V_{VDD}	VDD to VEE	15		25	V
V_{VEE}	COM to VEE	2.5		VDD-VEE	V
V_{FBVDD}, V_{FBVEE}	FBVDD, FBVEE to VEE	0	2.5	5.5	V
T_A	Ambient temperature	–40		125	°C
T_J (2)	Junction temperature	–40		150	°C

(1) See the $V_{VIN\_UVLOP\_RISING}$ and $V_{VIN\_UVLOP\_FALLING}$ electrical characteristics for the miminum operational V_{VIN}. Becasue $V_{VIN\_UVLOP\_FALLING}$ < 8V, V_{VIN} can operate at 8V as long as V_{VIN} > $V_{VIN\_UVLOP\_RISING}$ during start up.
(2) See the (VDD-VEE) and (COM-VEE) Load Recommended Operating Area section for maximum rated values across temperature and V_{VIN} conditions for different (VDD-VEE) and (COM-VEE) output voltage settings.

7.4 Thermal Information

THERMAL METRIC(1)		DWN (SOIC) 36 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	52.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.5	°C/W

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THERMAL METRIC(1)		DWN (SOIC) 36 PINS	UNIT
$R_{\theta JB}$	Junction-to-board thermal resistance	25.9	°C/W
Ψ_{JA}	Junction-to-ambient characterization parameter	29.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	16.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	25.6	°C/W

(1) The thermal resistances (R) are based on JEDEC board, and the characterization parameters (Ψ) are based on the EVM described in the Layout section. For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
General				
CLR	External clearance (1)	Shortest terminal-to-terminal distance through air	> 8	mm
CPG	External creepage (1)	Shortest terminal-to-terminal distance across the package surface	> 8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance – transformer power isolation)	> 120	µm
		Minimum internal gap (internal clearance – capacitive signal isolation)	> 15.4	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17) (Planned Certification Targets) (2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1414	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage (sine wave) Time dependent dielectric breakdown (TDDB) test	1000	V_{RMS}
		DC voltage	1414	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1s (100% production)	7071	V_{PK}
V_{IMP}	Maximum impulse voltage (3)	Tested in air, 1.2/50-µs waveform per IEC 62368-1	7692	V_{PK}
V_{IOSM}	Maximum surge isolation voltage (3)	Tested in oil (qualification test), 1.2/50 µs waveform per IEC 62368-1	10000	V_{PK}
qpd	Apparent charge (4)	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$ = 1696 V_{PK}, t_m = 10 s	≤ 5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$ = 2262 V_{PK}, t_m = 10 s	≤ 5	pC
		Method b1: At routine test (100% production) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$ = 2651 V_{PK}, t_m = 1 s	≤ 5	pC
C_{IO}	Barrier capacitance, input to output (5)	V_{IO} = 0.4 sin (2πft), f = 1 MHz	< 3.5	pF
R_{IO}	Isolation resistance, input to output (5)	V_{IO} = 500 V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	Ω
		V_{IO} = 500 V at T_S = 150°C	> 10^9	Ω
	Pollution degree		2	
	Climatic category		40/125/21	

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PARAMETER		TEST CONDITIONS	VALUE	UNIT
UL 1577 (Planned Certification Target)				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO} = 5000\ V_{RMS}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO} = 6000\ V_{RMS}$, t = 1 s (100% production)	5000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed-circuit board are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package. Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-terminal device.

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7.6 Safety-Related Certifications

VDE	UL	CQC
Plan to certify according to DIN EN IEC 60747-17 (VDE 0884-17)	Plan to certify under UL 1577 Component Recognition Program	Plan to certify according to GB4943.1
Reinforced insulation Maximum transient isolation voltage, 7071 V_{PK}; Maximum repetitive peak isolation voltage, 1414 V_{PK}; Maximum surge isolation voltage, 10000 V_{PK}	Single protection, 5000 V_{RMS}	Reinforced insulation, Altitude ≤ 5000 m, Tropical Climate, 700 V_{RMS} maximum working voltage
Certificate number: (planned)	File number: (planned)	Certificate number: (planned)

7.7 Electrical Characteristics

Over operating temperature range (T_J = –40 °C to 150 °C), V_{VIN} = 8 V to 18 V, C_{IN} = 20 µF, C_{OUT} = 10 µF, R_{LIM} = 1 kΩ, V_{ENA} = 5 V, unless otherwise noted. All typical values at T_A = 25 °C and V_{VIN} = 12 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY (Primary-side. All voltages with respect to GNDP)						
V_{VIN}	Input voltage range, 0.7W@(VDD-VEE)=25V, T_A=85ºC	Primary-side input voltage to GNDP	8[1]	12	18	V
	Input voltage range, 1.2W@(VDD-VEE)=25V, T_A=85ºC	Primary-side input voltage to GNDP	11.4	12	12.6	V
I_{VINQ_OFF}	VIN quiescent current, disabled	V_{ENA} = 0 V; V_{VIN} = 8 V-18 V;			600	µA
$I_{VIN\_ON\_NO\_LOAD}$	VIN operating current, enabled, No Load	V_{ENA} = 5 V; V_{VIN} = 8 V-18 V; (VDD-VEE) = 25 V regulating; $I_{VDD-VEE}$ = 0 mA. Single Output.			40	mA
$I_{VIN\_ON\_FULL\_LOAD}$	VIN operating current, enabled, Full Load	V_{ENA} = 5 V; V_{VIN} = 8 V-18 V; (VDD-VEE) = 25-V regulating; $I_{VDD-VEE}$ = 40 mA. Single Output.		200		mA
	VIN operating current, enabled, Full Load	V_{ENA} = 5 V; V_{VIN} =11.4 V-12.6 V; (VDD-VEE) = 25-V regulating; $I_{VDD-VEE}$ = 60 mA. Single Output.		270		mA
UVLOP COMPARATOR (Primary-side. All voltages with respect to GNDP)						
$V_{VIN\_UVLOP\_RISING}$	VIN analog undervoltage lockout rising threshold	Analog Comparator Always Active First	7.8	8.2	8.5	V
$V_{VIN\_UVLOP\_FALLING}$	VIN analog undervoltage lockout falling threshold	Analog Comparator Always Active First	7	7.4	7.7	V
OVLO COMPARATOR (Primary-side. All voltages with respect to GNDP)						
$V_{VIN\_OVLO\_RISING}$	VIN overvoltage lockout rising threshold		20.9	22	23.1	V
$V_{VIN\_OVLO\_FALLING}$	VIN overvoltage lockout falling threshold		19	20	21	V
TSHUTP THERMAL SHUTDOWN COMPARATOR (Primary-side. All voltages with respect to GNDP)						
$TSHUTP_{PRIMARY\_RISING}$	Primary-side over-temperature shutdown rising threshold	First time at power-up T_J needs to be < 140 °C to turnon	150	160	170	°C
$TSHUTP_{PRIMARY\_HYST}$	Primary-side over-temperature shutdown hysteresis		15	20	25	°C
ENA INPUT PIN (Primary-side. All voltages with respect to GNDP)						
V_{EN_IR}	Input voltage rising threshold, logic HIGH	Rising edge			2.1	V
V_{EN_IF}	Input voltage falling threshold, logic LOW	Falling edge	0.8			V
I_{EN}	Enable Pin Input Current	V_{ENA} = 5.0 V		5	10	µA
$\overline{PG}$ OPEN-DRAIN OUTPUT PIN (Primary-side. All voltages with respect to GNDP)						
$V_{\overline{PG}\_OUT\_LO}$	$\overline{PG}$ output-low saturation voltage	Sink Current = 5 mA, power good			0.5	V
$I_{\overline{PG}\_OUT\_HI}$	$\overline{PG}$ Leakage current	$V_{\overline{PG}}$ = 5.5 V, power not good			5	µA

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Over operating temperature range (T_J = –40 °C to 150 °C), V_{VIN} = 8 V to 18 V, C_{IN} = 20 µF, C_{OUT} = 10 µF, R_{LIM} = 1 kΩ, V_{ENA} = 5 V, unless otherwise noted. All typical values at T_A = 25 °C and V_{VIN} = 12 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Primary-side Control (All voltages with respect to GNDP)						
F_{SW}	Switching frequency	V_{VIN} = 12 V; V_{ENA} = 5 V; (VDD-VEE) = 25 V		16		MHz
F_{SSM}	Frequency of Spread Spectrum Modulation (SSM) triangle waveform	Only during primary-side startup starting after V_{IN} > UVLOP, and ENA = HIGH; $F_{SS\_BURST\_P}$ = 125 kHz		90		kHz
SSM Percentage change of $F_{CARRIER}$	SSM Percent change of carrier frequency during Spread Spectrum Modulation (SSM) by triangle waveform	Only during primary-side startup starting after V_{IN} > UVLOP, and ENA = HIGH; $F_{SS\_BURST\_P}$ = 125 kHz		5		%
$t_{SOFT\_START\_TIME\_OUT}$	Primary-side soft-start time-out	Timer begins when VIN > UVLOP and ENA = High and reset when Powergood pin indicates Good		28.4		ms
(VDD-VEE) OUTPUT VOLTAGE (Secondary-side. All voltages with respect to VEE)						
V_{VDD_RANGE}	(VDD – VEE) Output voltage range		15		25	V
$V_{VDD\_DC\_ACCURACY}$	(VDD – VEE) Output voltage DC regulation accuracy	Secondary-side (VDD – VEE) output voltage, over load, line and temperature range, externally adjust with external resistor divider, within SOA range.	-1.3		1.3	%
(VDD-VEE) REGULATION HYSTERETIC COMPARATOR (Secondary-side. All voltages with respect to VEE)						
V_{FBVDD_REF}	Feedback regulation reference voltage for (VDD – VEE)	(VDD – VEE) output in regulation	2.4675	2.5	2.5325	V
$V_{FBVDD\_HYSTCMP\_HYST}$	(VDD-VEE) Hysteresis comparator hysteresis settings. Hysteresis at the VFBVDD pin.	Hysteresis Setting	9	10	12.3	mV
(COM-VEE) OUTPUT VOLTAGE (Secondary-side. All voltages with respect to VEE)						
V_{VEE_RANGE}	(COM – VEE) Output voltage range	Secondary-side (COM – VEE), adjust with external resistor divider	2.5		(VDD-VEE)	V
$V_{VEE\_DC\_ACURACY}$	(COM - VEE) Output voltage DC regulation accuracy	Secondary-side (COM – VEE) output voltage, over load, line and temperature range, externally adjust with external resistor divider	–1.3		1.3	%
(COM-VEE) REGULATION HYSTERETIC COMPARATOR (Secondary-side. All voltages with respect to VEE)						
V_{FBVEE_REF}	Feedback regulation reference voltage for (COM – VEE)	(COM – VEE) output in regulation	2.4675	2.5	2.5325	V
$V_{RLIM\_SHORT\_CHRG\_CMP\_RISE}$	Rlim Short Charge comparator rising threshold to exit PWM	Rising threshold		0.73		V
$t_{RLIM\_SHORT\_CHRG\_ON\_TIME}$	On-Time during RLIM pin Short Charge PWM mode	RLIM pin < 0.645 V, while FBVEE pin < 2.48 V		1.1		us
$t_{RLIM\_SHORT\_CHRG\_OFF\_TIME}$	Off-Time during RLIM pin Short Charge PWM mode	RLIM pin < 0.645 V, while FBVEE pin < 2.48 V		5		us
(VDD-VEE) UVLOs COMPARATOR (Secondary-side. All voltages with respect to VEE)						
$V_{VDD\_UVLOS\_RISING}$	(VDD – VEE) undervoltage lockout rising threshold	Voltage at FBVDD		0.9		V
$V_{VDD\_UVLOS\_HYST}$	(VDD – VEE) undervoltage lockout hysteresis	Voltage at FBVDD		0.2		V
(VDD-VEE) OVLOs COMPARATOR (Secondary-side. All voltages with respect to VEE)						
$V_{VDD\_OVLOS\_RISING}$	(VDD – VEE) over-voltage lockout rising threshold	Voltage from VDD to VEE, rising	29.45	31	32.55	V

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Over operating temperature range (T_J = –40 °C to 150 °C), V_{VIN} = 8 V to 18 V, C_{IN} = 20 µF, C_{OUT} = 10 µF, R_{LIM} = 1 kΩ, V_{ENA} = 5 V, unless otherwise noted. All typical values at T_A = 25 °C and V_{VIN} = 12 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{VDD\_OVLOS\_FALLING}$	(VDD – VEE) over-voltage lockout falling threshold	Voltage from VDD to VEE, falling	27.55	29	30.45	V
SOFT-START (Secondary-side. All voltages with respect to VEE)						
$t_{deglitch}$	Deglitch time during soft start before $\overline{PG}$ for (VDD-VEE) UVP and (COM-VEE) UVP & OVP			3		ms
(VDD-VEE) UVP, UNDER -VOLTAGE PROTECTION COMPARATOR (Secondary-side. All voltages with respect to VEE)						
$V_{VDD\_UVP\_RISING}$	(VDD – VEE) under-voltage protection rising threshold, $V_{UVP} = V_{REF} \times 90\%$		2.175	2.25	2.35	V
$V_{VDD\_UVP\_HYST}$	(VDD – VEE) under-voltage protection hysteresis			20		mV
(VDD-VEE) OVP, OVER-VOLTAGE PROTECTION COMPARATOR (Secondary-side. All voltages with respect to VEE)						
$V_{VDD\_OVP\_RISING}$	(VDD – VEE) over-voltage protection rising threshold, $V_{OVP} = V_{REF} \times 110\%$		2.7	2.75	2.825	V
$V_{VDD\_OVP\_HYST}$	(VDD – VEE) over-voltage protection hysteresis			20		mV
(COM-VEE) UVP, UNDER -VOLTAGE PROTECTION COMPARATOR (Secondary-side. All voltages with respect to VEE)						
$V_{VEE\_UVP\_RISING}$	(COM – VEE) under-voltage protection rising threshold, $V_{UVP} = V_{REF} \times 90\%$		2.1	2.25	2.4	V
$V_{VEE\_UVP\_HYST}$	(COM – VEE) under-voltage protection hysteresis			20		mV
(COM-VEE) OVP, OVER-VOLTAGE PROTECTION COMPARATOR (Secondary-side. All voltages with respect to VEE)						
$V_{VEE\_OVP\_RISING}$	(COM – VEE) over-voltage protection rising threshold, $V_{OVP} = V_{REF} \times 110\%$		2.7	2.75	2.825	V
$V_{VEE\_OVP\_HYST}$	(COM – VEE) over-voltage protection hysteresis			20		mV
TSHUTS THERMAL SHUTDOWN COMPARATOR (Secondary-side. All voltages with respect to VEE)						
$TSHUTS_{SECONDARY\_RISE}$	Secondary -side over-temperature shutdown rising threshold	First time at power-up Tj needs to be < 140ºC to turnon.	150	160	170	°C
$TSHUTS_{SECONDARY\_HYST}$	Secondary-side over-temperature shutdown hysteresis		15	20	25	°C
CMTI (Common Mode Transient Immunity)						
CMTI	Common Mode Transient Immunity	Positive VEE with respect to GNDP	150			V/ns
		Negative VEE with respect to GNDP			-150	V/ns
INTEGRATED MAGLAM TRANSFORMER (Primary-side to Secondary-side. Note: these values unique for each version of XFMR)						
N	Transformer effective turns ratio	Secondary side to primary side		2.72		-

(1) See the $V_{VIN\_UVLOP\_RISING}$ and $V_{VIN\_UVLOP\_FALLING}$ electrical characteristics for the miminum operational V_{VIN}. Becasue $V_{VIN\_UVLOP\_FALLING}$ < 8V, V_{VIN} can operate at 8V as long as V_{VIN} > $V_{VIN\_UVLOP\_RISING}$ during start up.

7.8 Safety Limiting Values

PARAMETER		TEST CONDITIONS	MAX	UNIT
I_S	Safety input rms current	$R_{\theta JA}$ = 52.3 °C/W, V_{VIN} = 18 V, T_J = 150 °C, T_A = 25 °C, P_{OUT} = 1.5W (1) (2)	220	mA
		$R_{\theta JA}$ = 52.3 °C/W, V_{VIN} = 8 V, T_J = 150 °C, T_A = 25 °C, P_{OUT} = 1.2W (1) (2)	450	mA
P_S	Safety power dissipation (input power - output power)	$R_{\theta JA}$ = 52.3 °C/W, T_J = 150 °C, T_A = 25 °C (1) (2)	2.39	W

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PARAMETER		TEST CONDITIONS	MAX	UNIT
T_S	Safety temperature	(1) (2)	150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power dissipation respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.

(2) The junction-to-air thermal resistance, $R_{\theta JA}$, in the Thermal Information table is that of a device installed on a high-K JEDEC test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter: $T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device. $T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.

7.9 Insulation Characteristics

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforce certification requires additional safety margin of 20% for working voltage and 50% for lifetime which translates into minimum required insulation lifetime of 30 years at a working voltage that's 20% higher than the specified value. The TDDB projection line shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of the insulation is 1000 V_{RMS} with a lifetime >>100 years.

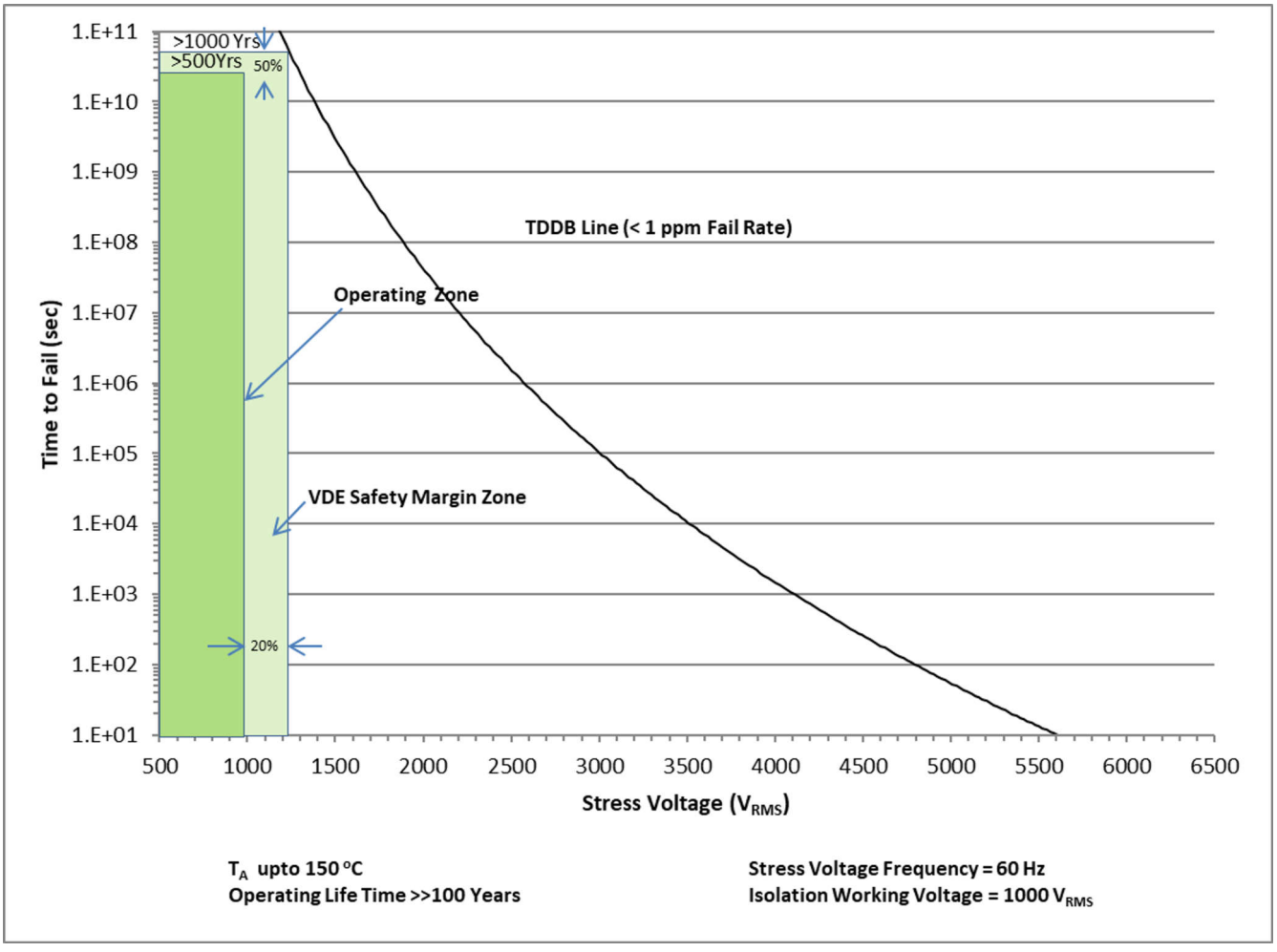

図 7-1. TDDB: Insulation Lifetime Projection for 1000 Vrms Working Voltage.

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7.10 Typical Characteristics

The maximum recommended average power safe operating area (SOA) at each Vin is determined by the lower value of the 1.5W limit (dotted line) and the corresponding thermal derating curve (solid line) at that input voltage. It is not recommended to operate at an ambient temperature higher than 125ºC. The thermal derating power is acquired with an evaluation board similar to the EVM shown in the セクション 9.5.2 section. T_{shut} represents the primary-side over-temperature shutdown rising threshold. As shown in the Electrical Characteristics table, the typical T_{shut} value is 160ºC, and minimal T_{shut} value is 150ºC. The SOA derating curve with both T_{shut} = 160ºC and 150ºC are provided below. The SOA curves under four common VDD-VEE settings, 15V, 18V, 22V, and 25V are characterized. In each SOA curve, the input voltage is swept from 9V to 18V. To represent a worst-case condition with T_{shut} = 150ºC, the test is done in a shieded box to block circulating air in the thermal chamber.

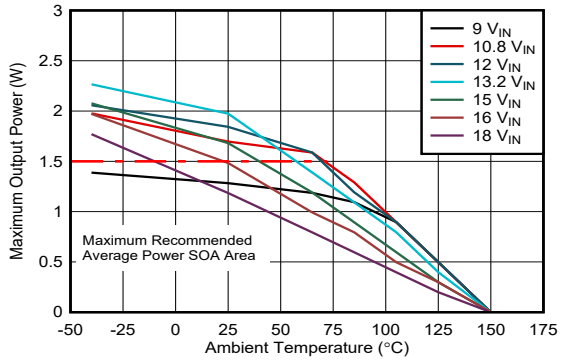

図 7-2. SOA Derating Curves: $V_{VDD-VEE}$ = 15 V, $V_{COM-VEE}$ = 5 V, T_{shut}=160ºC, No Load on $V_{COM-VEE}$

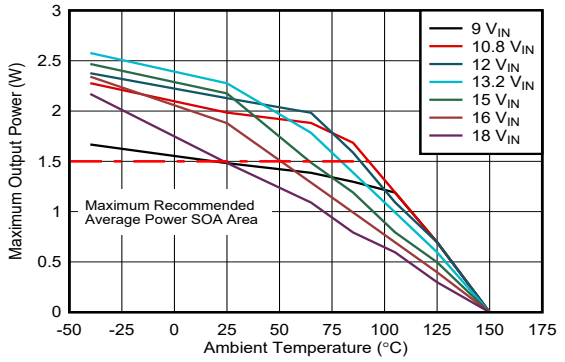

図 7-3. SOA Derating Curves: $V_{VDD-VEE}$ = 18 V, $V_{COM-VEE}$ = 3 V, T_{shut}=160ºC, No Load on $V_{COM-VEE}$

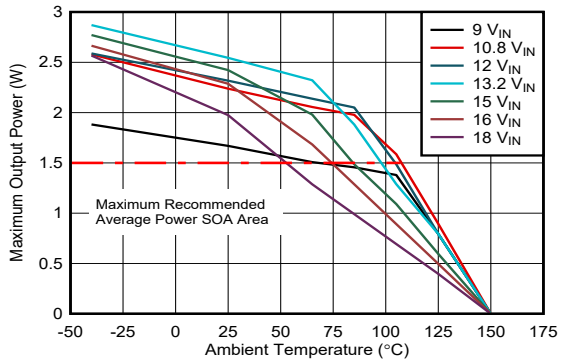

図 7-4. SOA Derating Curves: $V_{VDD-VEE}$ = 22 V, $V_{COM-VEE}$ = 4 V, T_{shut}=160ºC, No Load on $V_{COM-VEE}$

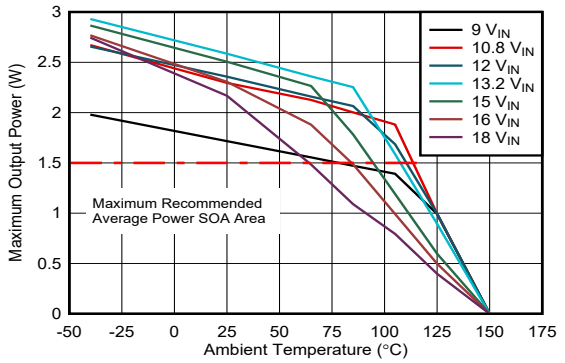

図 7-5. SOA Derating Curves: $V_{VDD-VEE}$ = 25 V, $V_{COM-VEE}$ = 5 V, T_{shut}=160ºC, No Load on $V_{COM-VEE}$

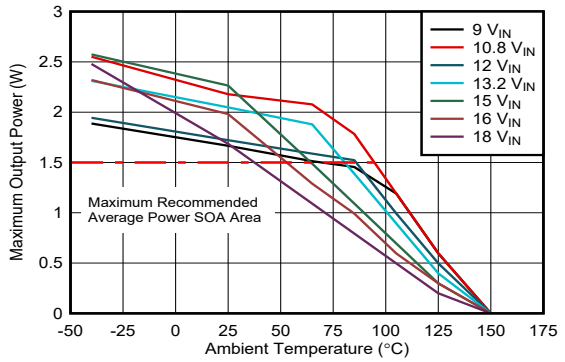

図 7-6. SOA Derating Curves: $V_{VDD-VEE}$ = 22 V, $V_{COM-VEE}$ = 4 V, T_{shut}=150ºC, No Load on $V_{COM-VEE}$, tested in a shielded box.

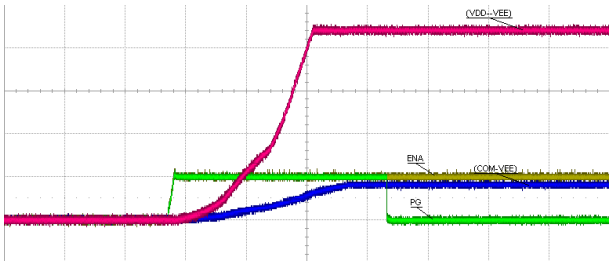

図 7-7. Start-up: V_{IN} = 12 V, $V_{VDD-VEE}$ = 22 V, $V_{COM-VEE}$ = 4 V, No Load on $V_{COM-VEE}$. Voltage Scale: 5V/div, Time Scale: 2ms/div.

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7.10 Typical Characteristics (continued)

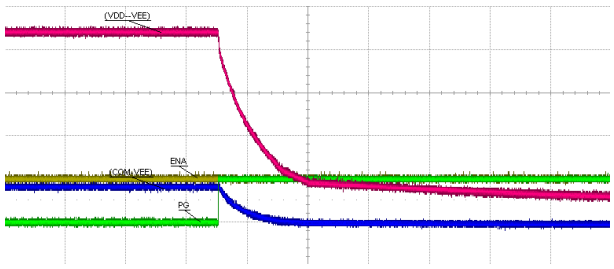

図 7-8. Shutdown: V_{IN} = 12 V, $V_{VDD-VEE}$ = 22 V, $V_{COM-VEE}$ = 4 V, No Load on $V_{COM-VEE}$. Voltage Scale: 5V/div, Time Scale: 50ms/div.

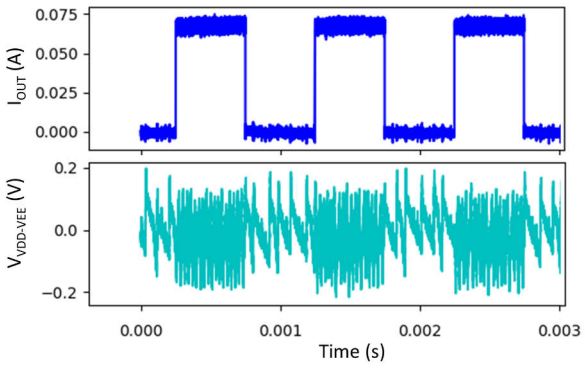

図 7-9. Load Transient Response: Between No Load and 1.5W, V_{IN} = 12 V, $V_{VDD-VEE}$ = 22 V, $V_{COM-VEE}$ = 4 V

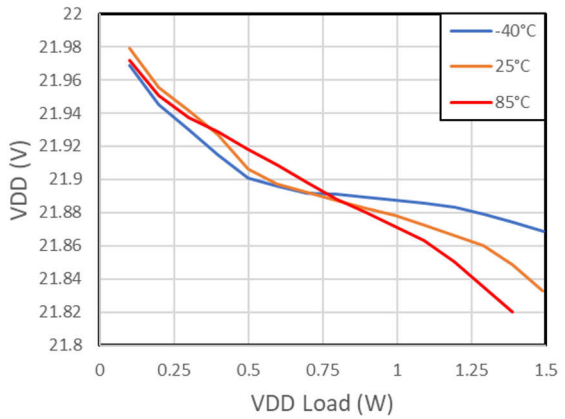

図 7-10. $V_{VDD-VEE}$ Load Regulation: V_{IN} = 9 V, $V_{VDD-VEE}$ = 22 V, $V_{COM-VEE}$ = 4 V

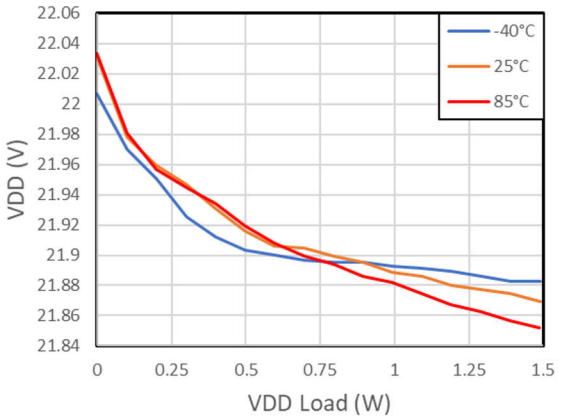

図 7-11. $V_{VDD-VEE}$ Load Regulation: V_{IN} = 12 V, $V_{VDD-VEE}$ = 22 V, $V_{COM-VEE}$ = 4 V

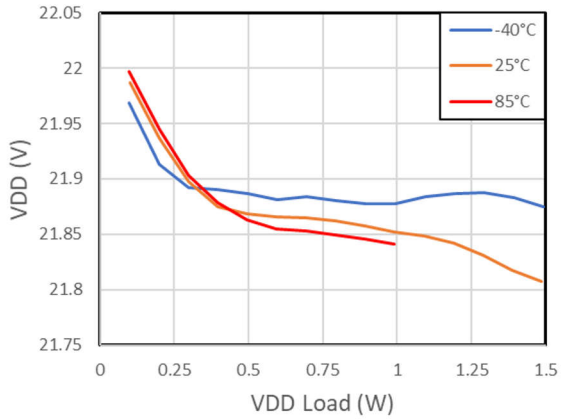

図 7-12. $V_{VDD-VEE}$ Load Regulation: V_{IN} = 18 V, $V_{VDD-VEE}$ = 22 V, $V_{COM-VEE}$ = 4 V

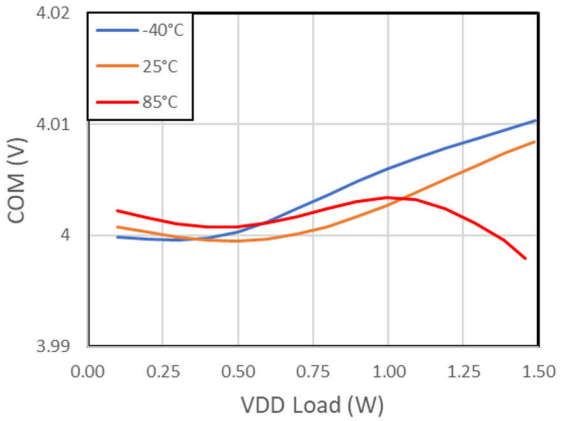

図 7-13. $V_{COM-VEE}$ Load Regulation: V_{IN} = 9 V, $V_{VDD-VEE}$ = 22 V, $V_{COM-VEE}$ = 4 V

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7.10 Typical Characteristics (continued)

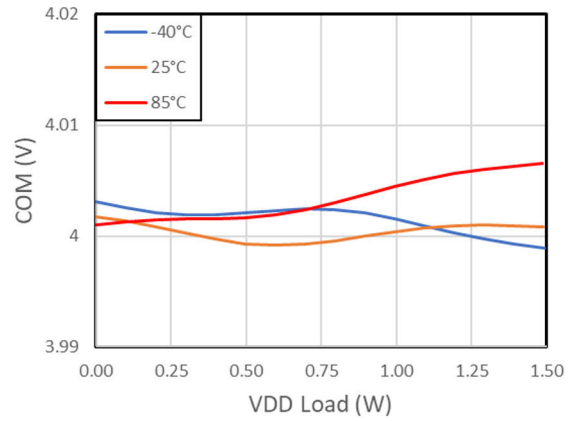

図 7-14. $V_{COM-VEE}$ Load Regulation: V_{IN} = 12 V, $V_{VDD-VEE}$ = 22 V, $V_{COM-VEE}$ = 4 V

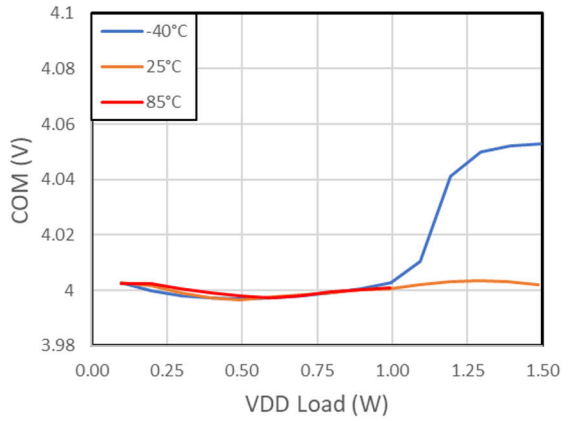

図 7-15. $V_{COM-VEE}$ Load Regulation: V_{IN} = 18 V, $V_{VDD-VEE}$ = 22 V, $V_{COM-VEE}$ = 4 V

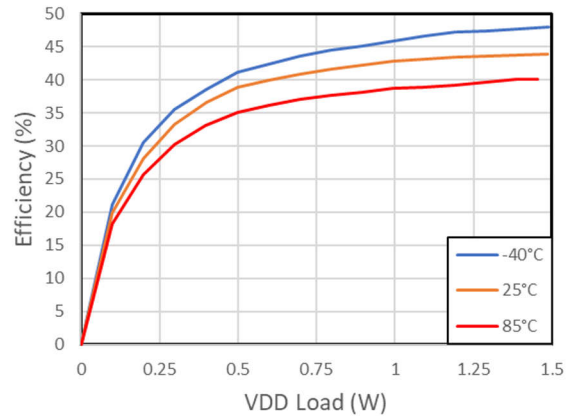

図 7-16. Efficiency vs. Load on $V_{VDD-VEE}$: V_{IN} = 9 V, $V_{VDD-VEE}$ = 22 V, $V_{COM-VEE}$ = 4 V, No Load on $V_{COM-VEE}$

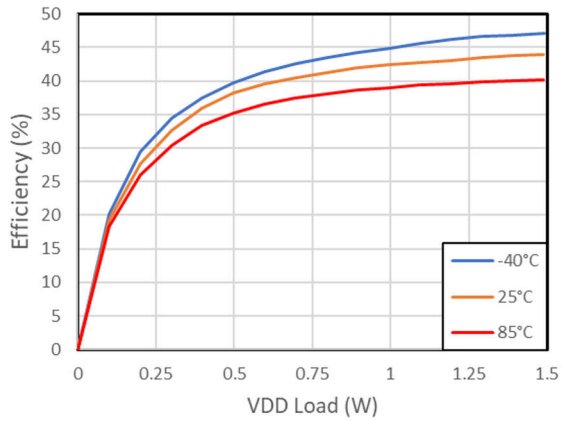

図 7-17. Efficiency vs. Load on $V_{VDD-VEE}$: V_{IN} = 12 V, $V_{VDD-VEE}$ = 22 V, $V_{COM-VEE}$ = 4 V, No Load on $V_{COM-VEE}$

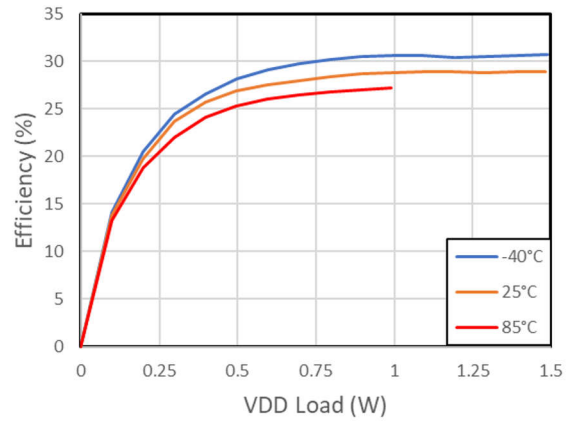

図 7-18. Efficiency vs. Load on $V_{VDD-VEE}$: V_{IN} = 18 V, $V_{VDD-VEE}$ = 22 V, $V_{COM-VEE}$ = 4 V, No Load on $V_{COM-VEE}$

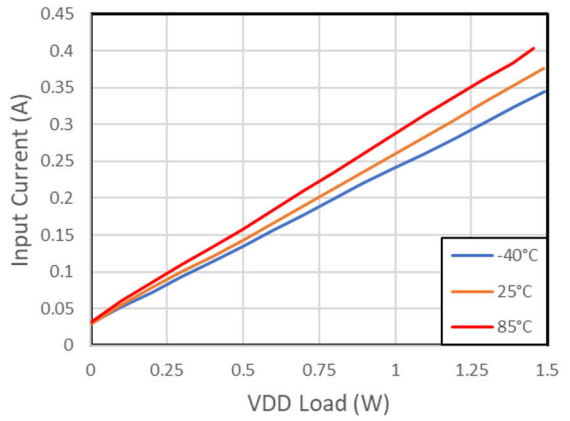

図 7-19. Input Current vs. Load on $V_{VDD-VEE}$: V_{IN} = 9 V, $V_{VDD-VEE}$ = 22 V, $V_{COM-VEE}$ = 4 V, No Load on $V_{COM-VEE}$

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7.10 Typical Characteristics (continued)

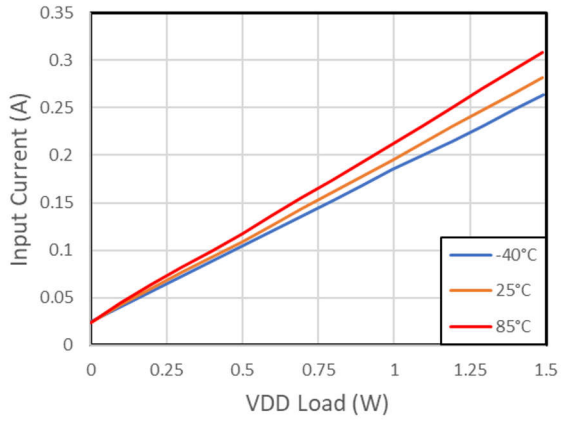

図 7-20. Input Current vs. Load on $V_{VDD-VEE}$: V_{IN} = 12 V, $V_{VDD-VEE}$ = 22 V, $V_{COM-VEE}$ = 4 V, No Load on $V_{COM-VEE}$

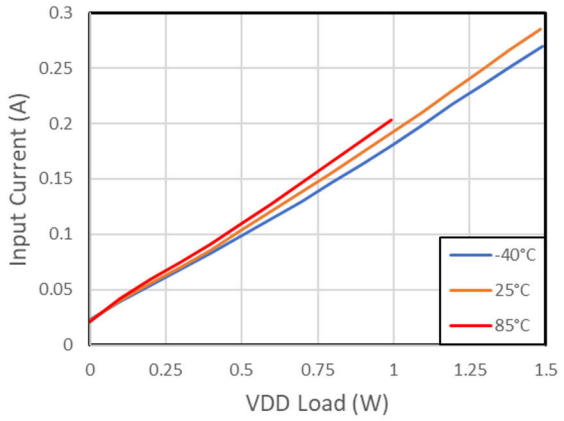

図 7-21. Input Current vs. Load on $V_{VDD-VEE}$: V_{IN} = 18 V, $V_{VDD-VEE}$ = 22 V, $V_{COM-VEE}$ = 4 V, No Load on $V_{COM-VEE}$

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8 Detailed Description

8.1 Overview

UCC14141-Q1 device is suitable for applications that have limited board space and require more integration. These devices are also suitable for very-high voltage applications, where power transformers meeting the required isolation specifications are bulky and expensive. The low-profile, low-center of gravity, and low weight provides a higher vibration tolerance than systems using large bulky transformers. The device is easy-to-use and provides flexibility to adjust both positive and negative output voltages as needed when optimizing the gate voltage for maximum efficiency while protecting gate oxide from over-stress with its tight voltage regulation accuracy.

The device integrates a high-efficiency, low-emissions isolated DC/DC converter for powering the gate drive of SiC or IGBT power devices in traction inverter motor drives, industrial motor drives, or other high voltage DC/DC converters. This DC/DC converter provides greater than 1.5 W of power for $10.8V<V_{VIN}<13.2V$ for regulated rails, and 1 W of power for $8V<V_{VIN}<18V$ for direct connection to a 12-V battery.

The integrated DC/DC converter uses switched mode operation and proprietary circuit techniques to reduce power losses and boost efficiency. Specialized control mechanisms, clocking schemes, and the use of an on-chip transformer provide high efficiency and low radiated emissions.

The integrated transformer provides power delivery throughout a wide temperature range while maintaining a 5000-V_{RMS} isolation, and an 1000-V_{RMS} continuous working voltage. The low isolation capacitance of the transformer provides high CMTI allowing fast dv/dt switching and higher switching frequencies, while emitting less noise.

The V_{VIN} supply is provided to the primary-side power controller that switches the input stage connected to the integrated transformer. Power is transferred to the secondary-side output stage, and regulated to a level set by the resistor divider connected between the (VDD – VEE) pin and the FBVDD pin with respect to the VEE pin. The output voltage is adjustable with an external resistor divider allowing a wide (VDD – VEE) range.

For optimal performance ensure to maintain the V_{VIN} input voltage within the recommended operating voltage range. Do not exceed the absolute maximum voltage rating to avoid over-stressing the input pins.

A fast hysteretic feedback burst control loop monitors (VDD – VEE) and ensures the output voltage is kept within the hysteresis with low overshoots and undershoots during load and line transients. The burst control loop enables efficient operation across full load and allows a wide VOUT adjustability throughout the whole V_{VIN} range. The undervoltage lockout (UVLO) protection monitors the input voltage pin, V_{VIN}, with hysteresis and input filter ensuring robust system performance under noisy conditions. The overvoltage lockout (OVLO) protection monitors the input voltage pin, VIN, protects against over-voltage stress by disabling switching and reducing the internal peak voltage. Controlled soft-start timing, provided throughout the full power-up time, limits the peak input inrush current while charging the output capacitor and load.

The UCC14141-Q1 also provides a second output rail, (COM – VEE), that is used as a negative bias for the gate drivers, allowing quicker turn-off switching for the IGBTs, and also to protect from unwanted turn-on during fast switching of SiC devices. (COM – VEE) has a simple, yet fast and efficient bias controller to ensure the positive and negative rails are regulated during the PWM switching. The COM pin can be connected from the source of SiC device or emitter of an IGBT device. An external current limiting resistor allows the designer to program the sink and source current peak according to the needs of the gate drive system.

A fault protection and powergood status pin provides a mechanism for the host controller to monitor the status of the DC/DC converter and provide proper sequencing of power and PWM control signals to the gate driver. Fault protection includes undervoltage, overvoltage, over-temperature shutdown, and isolated channel communication interface watchdog timer.

A typical soft-start ramp-up time is approximately 3 ms, but varies based on input voltage, output voltage, output capacitance, and load. If either output is shorted or over-loaded, the device is not able to power-up within the 28.4-ms soft-start watch-dog-timer protection time, so the device latches off for protection. The latch can be reset by toggling the ENA pin or powering VIN down and up.

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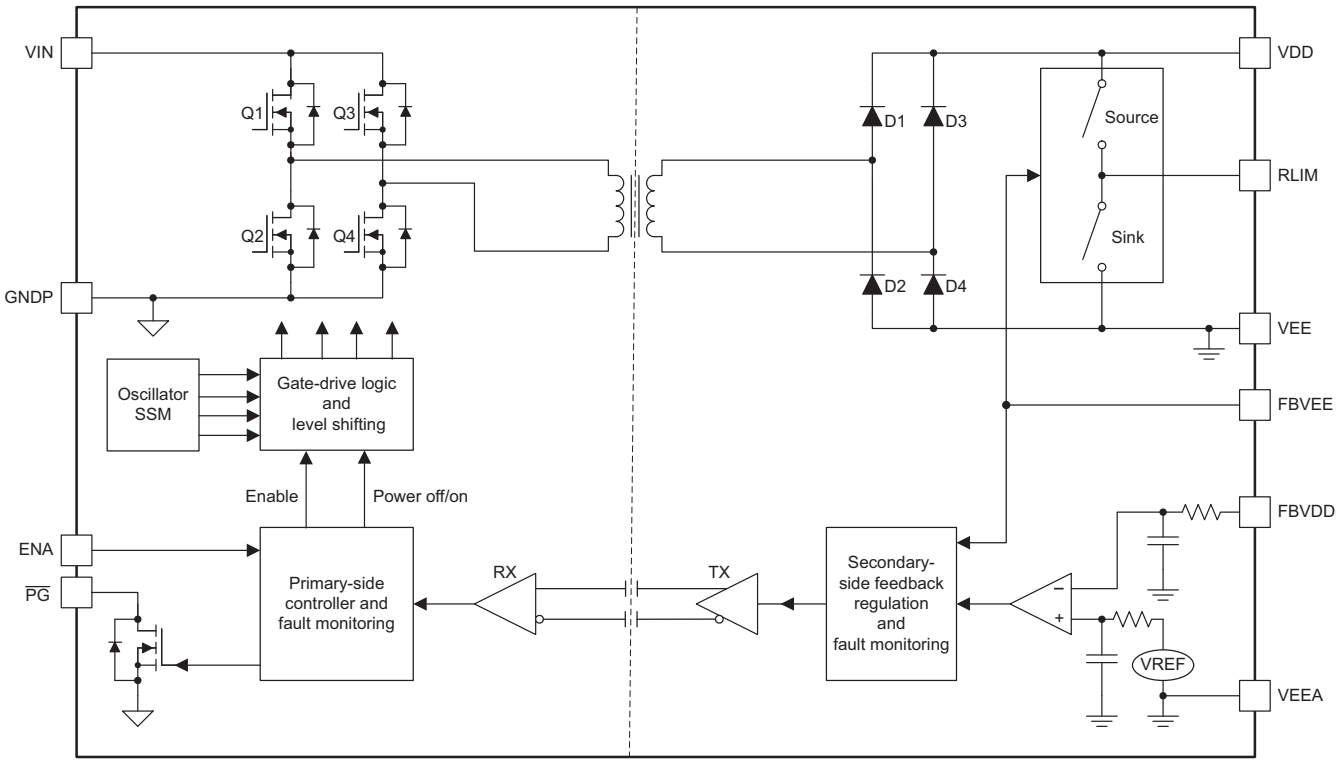
The output load must be kept low until start-up is complete and $\overline{PG}$ pin is low. When powering up, do not apply a heavy load to (VDD – VEE) or (COM – VEE) outputs until the $\overline{PG}$ pin has indicated power is good (pulling logic low) to avoid problems providing the power to ramp-up the voltage.

TI recommends to use the $\overline{PG}$ status indicator as a trigger point to start the PWM signal into the gate driver. $\overline{PG}$ output removes any ambiguity as to when the outputs are ready by providing a robust closed loop indication of when both (VDD –VEE) and (COM – VEE) outputs have reached their regulation threshold within ±10%.

Do not allow the host to begin PWM to gate driver until after $\overline{PG}$ goes low. This action typically occurs less than 28.4 ms after $V_{VIN} > V_{VIN\_UVLOP}$ and ENA goes high. The $\overline{PG}$ status output indicates the power is good after soft-start of (VDD – VEE) and (COM – VEE) and are within ±10% of regulation.

If the host is not monitoring $\overline{PG}$, then ensure that the host does not begin PWM to gate driver until 35 ms after $V_{VIN} > V_{VIN\_UVLOP}$ and ENA goes high in order to allow enough time for power to be good after soft-start of VDD and VEE.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Power Stage Operation

The UCC14141-Q1 module uses an active full-bridge inverter on the primary-side and a passive full-bridge rectifier on the secondary-side. The small integrated transformer has a relatively high carrier frequency to reduce the size for integrating into the 36-pin SSOP package. The power stage carrier frequency operates within 10 MHz to 22 MHz. The power stage carrier frequency is determined by input voltage with a feed-forward control: when V_{VIN} is 8 V, the frequency is 22 MHz; when V_{VIN} is 18 V, the frequency is 10 MHz; when V_{VIN} is between 8 V and 18 V, the frequency reduces gradually from 22 MHz to 10 MHz as V_{VIN} voltage rises. Spread spectrum modulation, SSM, is used to reduce emissions. ZVS operation is maintained to reduce switching power losses.

The UCC14141-Q1 module creates two regulated outputs. It can be configured as a single output converter, VDD to VEE only, or a dual-output converter, VDD to VEE and COM to VEE. Even though the module uses VEE as the reference point to create two positive output voltages, the outputs can use COM as the reference point and become a positive and a negative output.

These two outputs are controlled independently through hysteresis control. Furthermore, the VDD-VEE is the main output, and COM to VEE uses the main output as its input to created a second regulated output voltage.

8.3.1.1 VDD-VEE Voltage Regulation

The VDD-VEE output is the main output of the module. The power stage operation is determined by the sensed VDD-VEE voltage on FBVDD pin. As shown in 図 8-1, the VDD-VEE voltage is sensed through a voltage divider R_{FBVDD_TOP} and R_{FBVDD_BOT}. When FBVDD voltage stays below the turn-off threshold, roughly 10 mV above the V_{FBVDD_REF}, the power stage operates, delivers power to the secondary side and makes the VDD-VEE output voltage rise. After the output reaches the turn-off threshold, the power stage turns off. Output voltage drops because of the load current. After the output voltage drops below the turn-on threshold, roughly 10 mV below the V_{FBVDD_REF}, the power stage is turned on again. With the accurate voltage reference and hysteresis control, the VDD-VEE output voltage can be regulated with high accuracy. To improve the noise immunity, a small capacitor of 330 pF should be added between FBVDD and VEE pins. Excessive capacitor slows down the hysteresis loop and can cause excessive output voltage ripple or even stability issue.

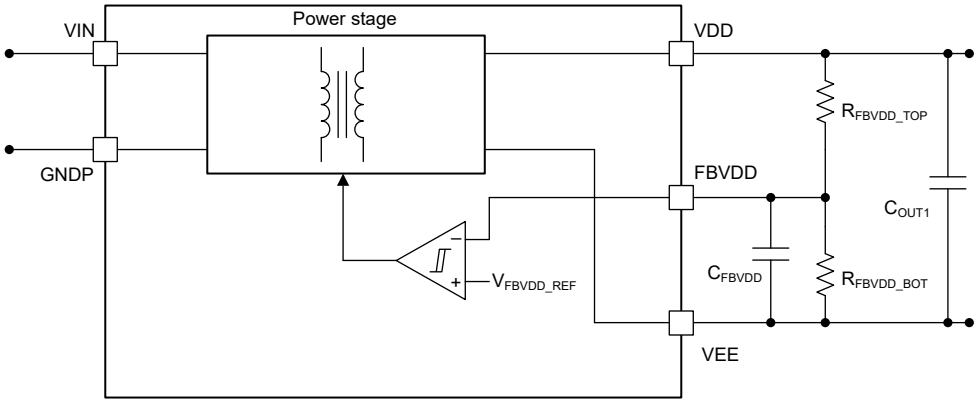

図 8-1. VDD-VEE Voltage Regulation

8.3.1.2 COM-VEE Voltage Regulation

COM-VEE output takes VDD-VEE output as its input and creates a regulated output voltage. It can be considered as an LDO output from VDD-VEE, though the operation principle is not quite the same. Given its input voltage is VDD-VEE, the maximum output voltage from COM to VEE is the voltage between VDD and VEE.

The COM-VEE output regulator stage uses the internal high-side or low-side FETs in series with the external current-limit resistor (R_{LIM}) to charge or discharge the COM-VEE output voltage. The hysteresis control is used to control the switching instance of the two FETs, to achieve an accurately regulated COM-VEE voltage. As shown in 図 8-2, the COM-VEE output voltage is sensed through the voltage divider R_{FBVEE_TOP} and R_{FBVEE_BOT} on FBVEE pin. TI recommends a 330-pF capacitor on FBVEE pin to filter out the switching frequency noise. When the voltage on FBVEE is below the charging threshold, 20 mV below the V_{FBVEE_REF}, the charging resistor is kept on and discharging resistor is kept off. COM-VEE output voltage rises. After FBVEE voltage reaches the stop charging threshold, 20 mV above the V_{FBVEE_REF}, the charging resistor is turned off. Output voltage rise stops. When the charging resistor is turned off, the discharge resistor is controlled by another hysteresis controller, based on FBVEE pin voltage, with the same reference voltage V_{FBVEE_REF}, and 20-mV of hysteresis.

The COM-VEE output regulator stage will protect from having the high-side FET stay ON for a long time during a COM to VEE short. This protection feature is implemented by monitoring the RLIM-pin voltage and controlling the high-side FET duty-ratio. When the COM pin voltage is lower than 0.645 V while the FBVEE voltage is below 2.48 V, the hysteretic control of the COM-VEE regulator is overridden by an approximately 20 % duty-ratio control on high-side FET, with a typical on-time of $t_{RLIM\_SHORT\_CHRG\_ON\_TIME}$ and off-time of $t_{RLIM\_SHORT\_CHRG\_OFF\_TIME}$ in each duty cycle. When the COM pin voltage is higher than $V_{RLIM\_SHORT\_CHRG\_CMP\_RISE}$, the duty ratio control is disabled and the hysteretic control resumes to normal operation.

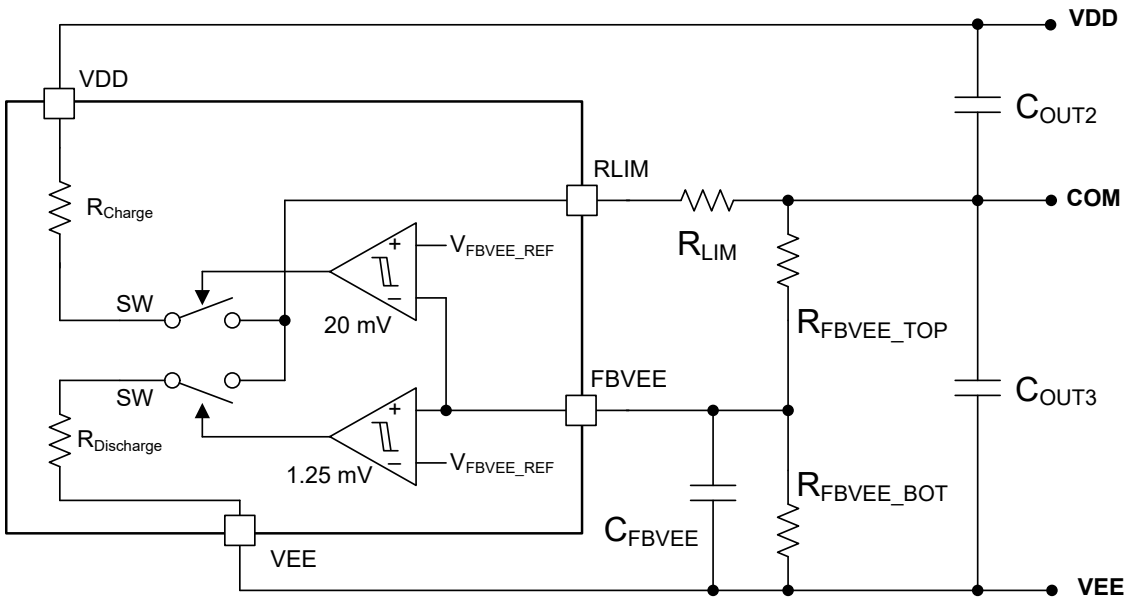

図 8-2. COM-VEE Voltage Regulation

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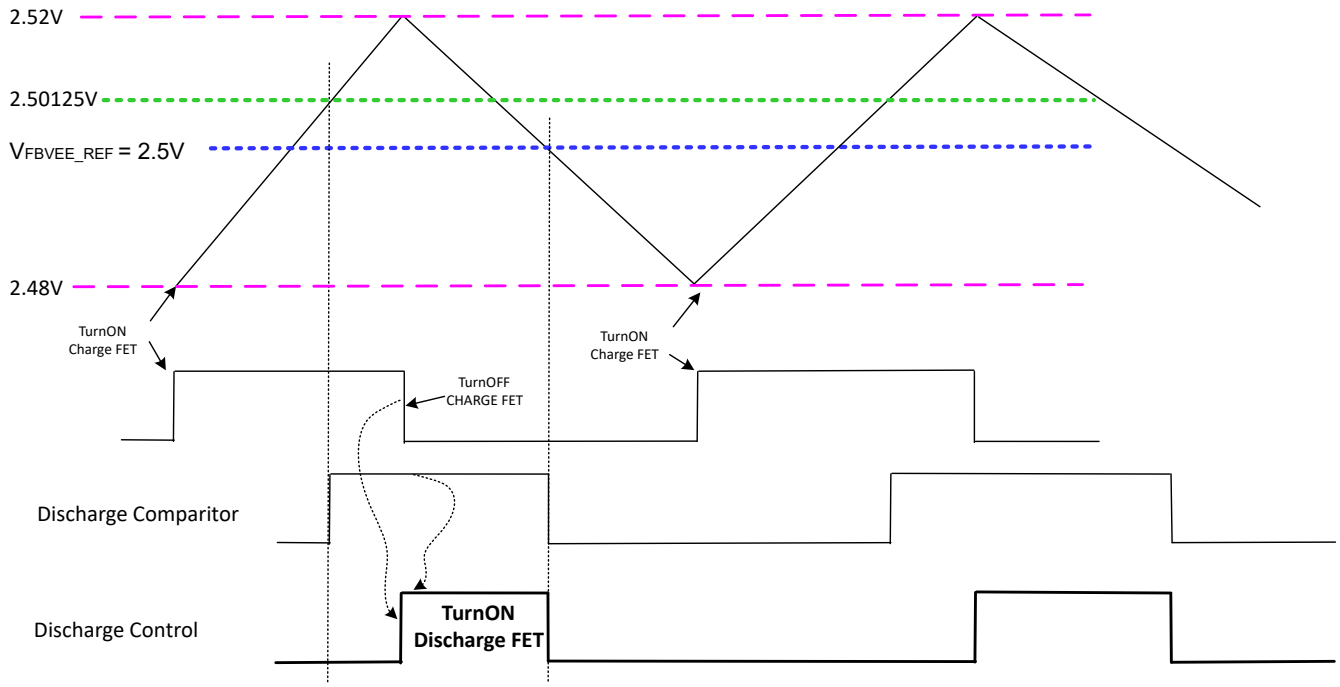

図 8-3. COM-VEE Voltage Regulation Diagram

8.3.1.3 Power Handling Capability

The maximum power handling capability is determined by both circuit operation and thermal condition. For a given output voltage, the maximum power increases with input voltage before triggering the thermal protection. An over-power-protection (OPP) is implemented to limit maximum output power and reduces power stage RMS current at high input voltage. The OPP is implemented by a feed-forward control from the input voltage to the OPP burst duty cycle (D_{OPP}). The D_{OPP} adds a "baby" burst within the on-time of "Mama" burst from the main feedback loop for the (VDD-VEE) regulation. When the input voltage increases, the D_{OPP} reduces automatically to limit the averaged output power.

At high ambient temperature, the thermal performance determines the maximum power and safe operating area (SOA). A protective thermal shut-down is triggered after overtemperature is detected. The high-efficiency and optimized thermal design for transformer and silicon provide a high power handling capability at high ambient temperature in a small package.

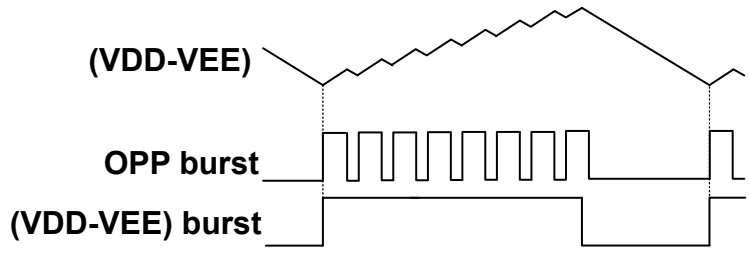

図 8-4. Diagram of Over-Power-Protection with baby burst

8.3.2 Output Voltage Soft Start

UCC14141-Q1 power-up diagram of two output rails with soft start is shown in 図 8-5. After V_{VIN} > V_{VIN_UVLOP} and ENA is pulled high, the soft-start sequence starts with burst duty cycle control with soft duty cycle increment. The burst duty cycle gradually increases from 12.5% to 50% over time by the primary-side control signal (D_{SS_PRI}), so both $V_{VDD-VEE}$ and $V_{COM-VEE}$ increase ratiometrically with a controlled shallow rising slope. When $V_{VDD-VEE}$ is increased above V_{VDD_UVLOS}, there is a sufficient bias voltage for the feedback-loop communication channel, so the burst feedback control on the secondary side takes over. As a result, the D_{SS_PRI} is pulled high and does not affect burst duty cycle anymore. The burst duty cycle is determined by comparing V_{FBVDD} and V_{REF}. V_{REF} increases from 0.9V to 2.5 V with seven increment steps, where the first 0.4-V step boosts V_{REF} from 0.9V to 1.3V, and then the following six 0.2-V steps boosts V_{REF} from 1.3V to 2.5V. Each step lasts 128 µs. After $V_{VDD-VEE}$ > V_{VDD_UVP}, the RLIM source-sink regulator for $V_{COM-VEE}$ is enabled. The polarity of source or sink current of RLIM pin is determined by comparing V_{FBVEE} and V_{REF} so as to keep $V_{COM-VEE}$ in tight regulation. Once $V_{VDD-VEE}$ or $V_{COM-VEE}$ rises across its UVP threshold, there is a 3-ms (typical) deglitch time for $V_{VDD-VEE}$ UVP and $V_{COM-VEE}$ UVP and OVP, and then the power good signal is issued by pulling $\overline{PG}$ voltage low. The 3-ms (typical) deglitch time is only applied during start up before the power good signal is issued. It provides enough time for both $V_{VDD-VEE}$ and $V_{COM-VEE}$ to settle in their hysteresis band of regulation after start up, so that the converter does not shut down due to the overshoot or undershoot during start up.

The soft-start feature greatly reduces the input inrush current during power-up. In addition, if $V_{VDD-VEE}$ cannot reach to V_{VDD_UVLOS} within 28.4 ms, then the device shuts down in a safe-state. The 28.4-ms soft-start time-out protects the module under output short circuit condition before power up.

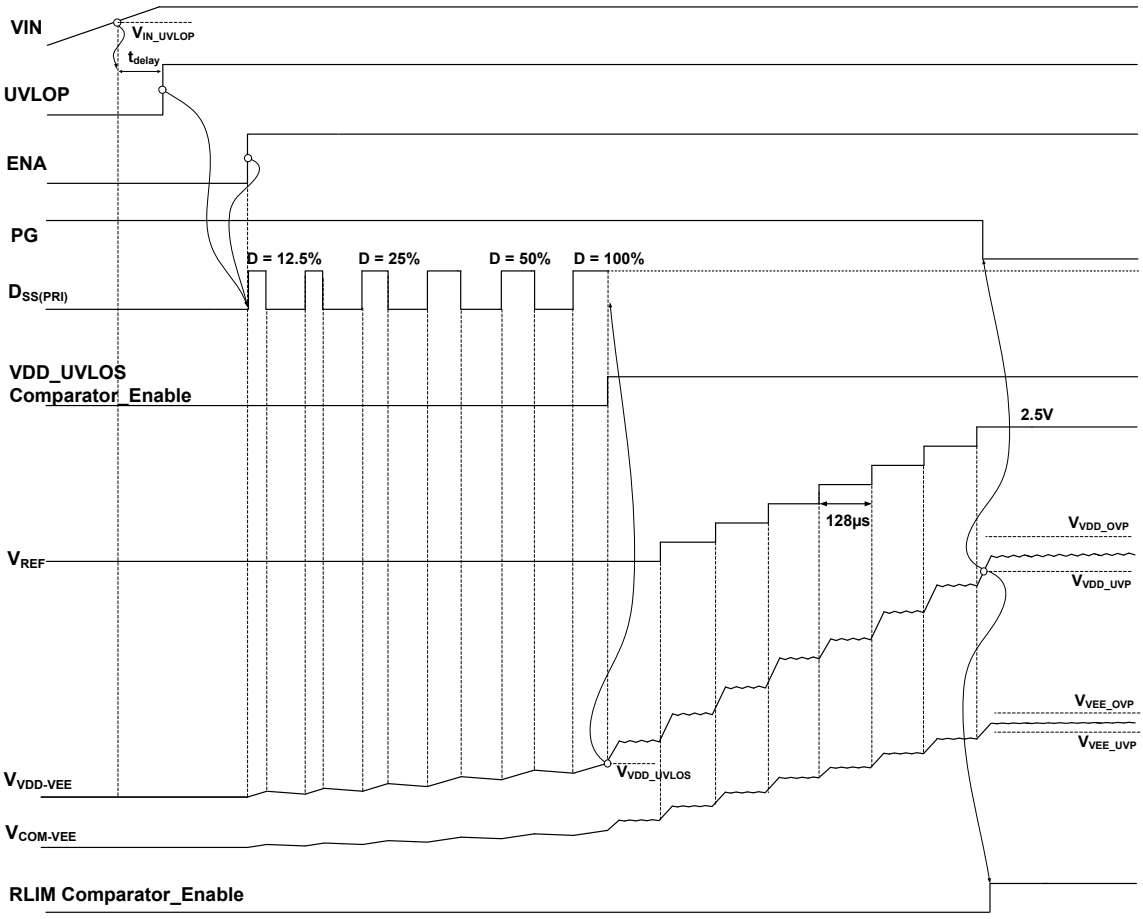

図 8-5. Output voltage Soft-Start Diagram

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8.3.3 ENA and $\overline{PG}$

The ENA input pin and $\overline{PG}$ output pin on the primary-side use 5-V TTL and 3.3-V LVTTL level logic thresholds.

The active-high enable input (ENA) pin is used to turn-on the isolated DC/DC converter of the module. Either 3.3-V or 5-V logic rails can be used. Maintain the ENA pin voltage below 5.5 V. After ENA pin voltage becomes above the enable threshold V_{EN_IR}, UCC14141-Q1 enables, starts switching, goes through the soft-start process and delivers power to the secondary side. After ENA pin voltage falls below the disable threshold V_{EN_IF}, UCC14141-Q1 disables, stops switching.

The ENA pin can also be used to reset the UCC14141-Q1 device after it enters the protection safe-state mode. After a detected fault, the protection logic will latch off and place the device into a safe state. When all the faults are cleared, the ENA-pin can be used to clear the UCC14141-Q1 latch by toggling the ENA pin voltage below V_{EN_IF} for longer than 150 µs, then toggling back up to 3.3 V or 5 V. The device will then exit the latch-off mode and we initiate a soft-start. 図 8-6 illustrates the latch-off reset timing.

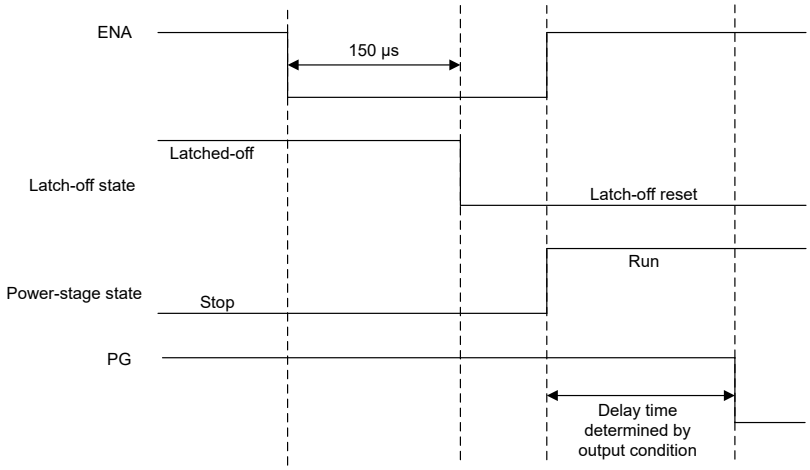

図 8-6. Latch-off Reset Using ENA Pin

The active-low power-good ($\overline{PG}$) pin is an open-drain output that indicates (short) when the module has no fault and the output voltages are within ±10% of the output voltage regulation setpoints. Connect a pull-up resistor (> 1 kΩ) from $\overline{PG}$ pin to either a 5-V or 3.3-V logic rail. Maintain the $\overline{PG}$ pin voltage below 5.5 V without exceeding its recommended operating voltage. The logic of $\overline{PG}$ pin can be illustrated using 図 8-7.

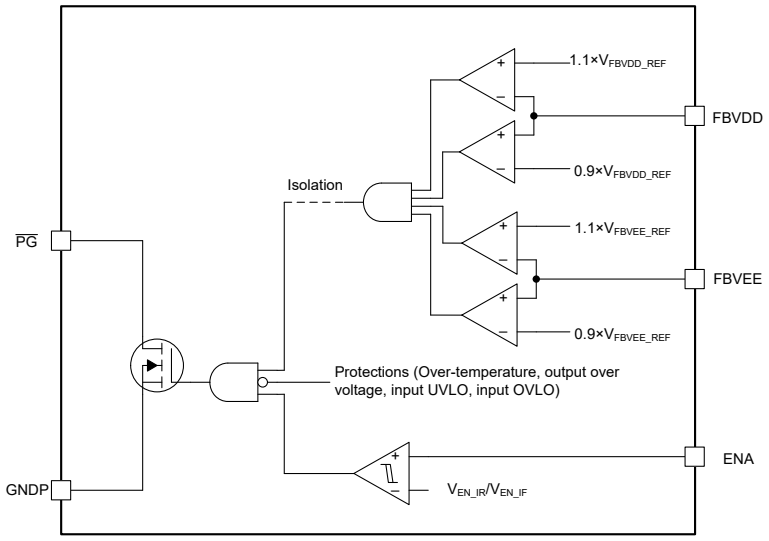

図 8-7. $\overline{PG}$ Pin Logic

8.3.4 Protection Functions

UCC14141-Q1 is equipped with a full feature of protection functions, include input undervoltage lockout, overvoltage lockout protections, output undervoltage protection, overvoltage protection, overpower protection, and over-temperature protection. The input undervoltage and overvoltage lockout protections have the auto recovery response. All other protections have the latch-off response. After the latch-off-response protections are triggered, the converter enters a latch off state, stops switching until the latch is reset by either toggling the ENA pin Off then On, or by lowering the V_{VIN} voltage below the $V_{VIN\_ANALOG\_UVLOP\_FALLING}$ threshold, and then above the $V_{VIN\_UVLOP\_RISING}$ threshold.

8.3.4.1 Input Undervoltage Lockout

UCC14141-Q1 can take wide input voltage range, from 8 V to 18 V. When the input voltage becomes too low, the output either cannot be regulated due to the transformer turns ratio limitation, or the converter operates with too much current stress. Either way, the converter must shut down to protect the system.

The UCC14141-Q1 enters input undervoltage lockout when V_{VIN} voltage becomes lower than the UVLO threshold $V_{VIN\_UVLOP\_FALLING}$. In UVLO mode, the converter stops switching. After VIN pin voltage becomes lower than the VIN analog undervoltage lockout falling threshold $V_{VIN\_VULOP\_FALLING}$, UCC14141-Q1 resets all the protections. After that, after the V_{VIN} voltage becomes above the UVLO threshold $V_{VIN\_UVLOP\_RISING}$, the converter is enabled. Depending on the ENA pin voltage, the converter can start switching, go through the soft-start process, or in the disable mode, waiting for ENA pin voltage becomes high.

8.3.4.2 Input Overvoltage Lockout

The input overvoltage lockout protection is used to protect the UCC14141-Q1 devices from overvoltage damage. It has an auto-recovery response. When the V_{VIN} pin voltage becomes higher than the input overvoltage lockout threshold $V_{VIN\_OVLO\_RISE}$, switching stops, converter stops sending energy to the secondary side. After input overvoltage lockout protection, after V_{VIN} pin voltage drop below the recovery threshold $V_{VIN\_OVLO\_FALLING}$, depending on the ENA pin voltage status, the converter can either resuming operation, go through the full soft-start process, or in the disabled mode, wait for ENA pin becomes high. The input overvoltage lockout does not reset other latch-off protections.

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8.3.4.3 Output Undervoltage Protection

The output voltage under voltage protection is based on the FBVDD and FBVEE pin voltages. When the FBVDD pin voltage becomes lower than its UVP threshold $V_{VDD\_UVP\_FALL}$, or the FBVEE pin voltage becomes lower than its UVP threshold $V_{VEE\_UVP\_FALL}$, the undervoltage protection is activated. The UCC14141-Q1 stops switching, and the PG pin becomes open.

During soft start, the output voltages rise from zero. Both FBVDD and FBVEE pin voltage are below the UVP thresholds. The UVP is disabled during the soft start. If the pin voltage cannot reach the UVP recovery thresholds ($V_{VDD\_UVP\_RISE}$, $V_{VEE\_UVP\_RISE}$) after the soft start completes, undervoltage protection is activated. The UCC14141-Q1 stops switching, and the PG pin becomes open.

The undervoltage protection has a latched-off response. After it is activated, the latch-off state can be cleared by recycling V_{VIN}. Toggling ENA pin can also reset the latch-off state. Refer to ENA and PG section for details.

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8.3.4.4 Output Overvoltage Protection

The UCC14141-Q1 devices sense the output voltage through FBVDD and FBVEE pins to control the output voltage. To prevent the output voltage becomes too high, damages the load or UCC14141-Q1 device itself, the UCC14141-Q1 devices are equipped with the output overvoltage protection. There are two levels of overvoltage protection, based on the feedback pin voltage, and the output voltage.

During the normal operation, because of load transient, or load unbalancing between two outputs, the output voltages can exceed its regulation level. Based on the pin voltages on FBVDD and FBVEE, after the voltage exceeds the threshold, $V_{VDD\_OVP\_RISE}$, or $V_{VEE\_OVP\_RISE}$ (10% above the target regulation voltage), the converter stops switching immediately.

In rare cases, the voltage divider becomes malfunction and gives the wrong output voltage information. In turn, the control loop can regulate the output voltages at a wrong voltage level. The UCC14141-Q1 device is also equipped with a fail-safe overvoltage protection. After the VDD-VEE voltage becomes higher than the overvoltage protection threshold $V_{VDD\_OVLOS\_RISE}$, the converter shuts down immediately. This fail-safe protection level is set at 31 V. It is meant to protect UCC14141-Q1 devices, instead of the load. The design must ensure the voltage feedback divider normal operation at all conditions.

The output overvoltage protections have the latch-off response.

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8.3.4.5 Overpower Protection

The Over Power Protection, OPP, limits the maximum average output power. When the output is overloaded, it is important to shutdown the module to prevent it from further damage, or propagating the fault into other portion of the entire system. Given the extremely high switching frequency, it is not practical to implement the traditional cycle-by-cycle current limit. Instead, the UCC14141-Q1 device relies on the Over Power Protection (OPP) working together with the output undervoltage protection.

As discussed in Power Handling Capability, with the input voltage feedforward, and the "baby" burst duty cycle adjustment, the maximum power delivery capability of the UCC14141-Q1 is well controlled. The impact of OPP on the relationship between Vin and maximum output power is shown in 図 8-8.

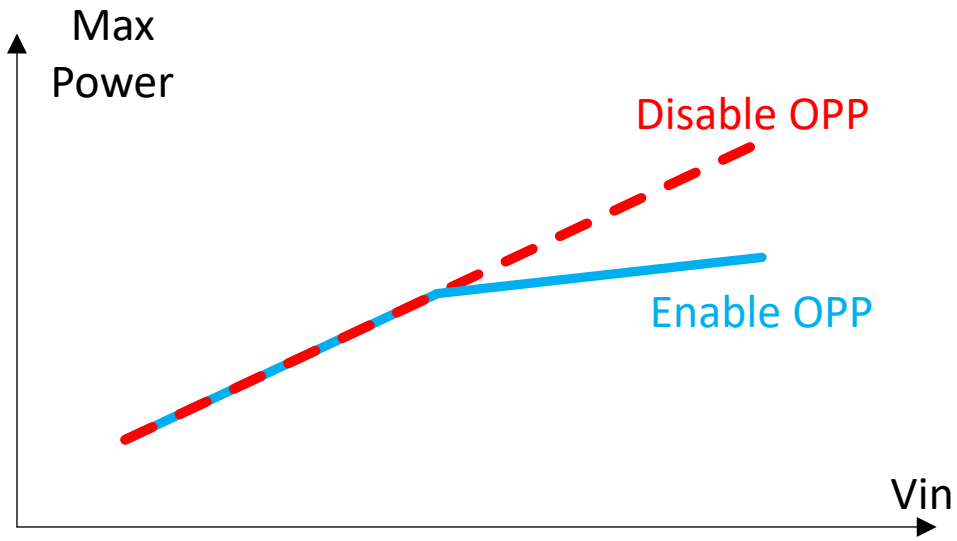

図 8-8. Maximum Output Power Under Different Input Voltage Condition

When the load exceeds the maximum power delivery capability, the output voltage starts to droop. When the output voltage falls below the Under Voltage Protection threshold, the output undervoltage protection is triggered and the parts latches off into a safe state.

8.3.4.6 Overtemperature Protection

UCC14141-Q1 integrates the primary-side, secondary-side power stages, as well as the isolation transformer. The power loss caused by the power conversion causes the module temperature higher than the ambient temperature. To ensure the safe operation of the power module, the UCC14141-Q1 device is equipped with over-temperature protection. Both the primary-side power stage, and the secondary-side power stage temperatures are sensed and compared with the over-temperature protection threshold. If the primary-side power stage temperature becomes higher than $TSHUTP_{PRIMARY\_RISE}$, or the secondary-side power stage temperature becomes higher than $TSHUTS_{SECONDARY\_RISE}$, the module enters over-temperature protection mode. The module stops switching; $\overline{PG}$ pin becomes open. After protection, the module enters latch-off mode. When the power stage temperature drops below the over-temperature recovery threshold, recycling V_{VIN}, or toggling ENA pin voltage brings the model out of latch-off mode. Depending on ENA pin voltage, the module either starts switching, delivering power to the secondary side, or in the standby mode waiting for ENA pin voltage becomes high.

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8.4 Device Functional Modes

Depending on the input and output conditions, ENA pin voltage, as well as the device temperature, the UCC14141-Q1 operates in one of the below operation modes.

1. Disable mode. In this mode, the module is off, but waiting for ENA pin becoming high to start operate.
2. Soft-start mode. In this mode, the module starts to deliver power to the secondary side. The primary-side operation duty cycle and secondary-side references are raised gradually to reduce the stress to the module.
3. Normal operation mode. In this mode, the module operates normally, delivers power to the secondary side.
4. Protection mode, auto-recovery. In this mode, the module is off, due to the input UVLO or OVLO protection. After the input voltage fault is cleared, depending on the ENA pin voltage condition, it either becomes disabled mode if the ENA pin voltage is low, or it goes through soft-start mode to the normal operation mode.
5. Protection mode, latched-off. In this mode, the module is off, due to other protections. The module remains off even the fault causing the protection is cleared. Recycling V_{VIN} operation must ensure the input voltage goes below the analog UVLO falling threshold ($V_{VIN\_ ANALOG\_UVLOP\_FALLING}$) first to reset the latch-off state, or the ENA pin is toggled Low (OFF) then High (ON).

表 8-1 lists the supply functional modes for this device. The ENA pin has an internal weak pull-down resistance to ground, but TI does not recommend leaving this pin open.

表 8-1. Device Functional Modes

INPUT			OUTPUTS			Operation Mode
V_{VIN}	ENA	FAULT	$V_{(VDD-VEE)}$ Isolated Output1	$V_{(COM-VEE)}$ Isolated Output2	PG Open Drain	
$V_{VIN} < V_{VIN\_UVLOP\_RISING}$	X	X	OFF	OFF	High	Protection mode, auto-recovery
$V_{VIN\_UVLOP\_RISING} < V_{VIN} < V_{VIN\_OVLO\_RISING}$	LOW	X	OFF	OFF	High	Disable mode
$V_{VIN\_UVLOP\_RISING} < V_{VIN} < V_{VIN\_OVLO\_RISING}$	HIGH	NO FAULT	Regulating at Setpoint	Regulating at Setpoint	Low	Normal operation
$V_{VIN\_UVLOP\_RISING} < V_{VIN} < V_{VIN\_OVLO\_RISING}$	HIGH	YES FAULT	OFF	OFF	High	Protection mode, latched-off
$V_{VIN} > V_{VIN\_OVLO\_RISING}$	X	X	OFF	OFF	High	Protection mode, auto-recovery

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9 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The UCC14141-Q1 device is suitable for applications that have limited board space and desire more integration. This device is also suitable for very high voltage applications, where power transformers meeting the required isolation specifications are bulky and expensive.

9.2 Typical Application

The following figures show the typical application schematics for the UCC14141-Q1 device configurations supplying an isolated load.

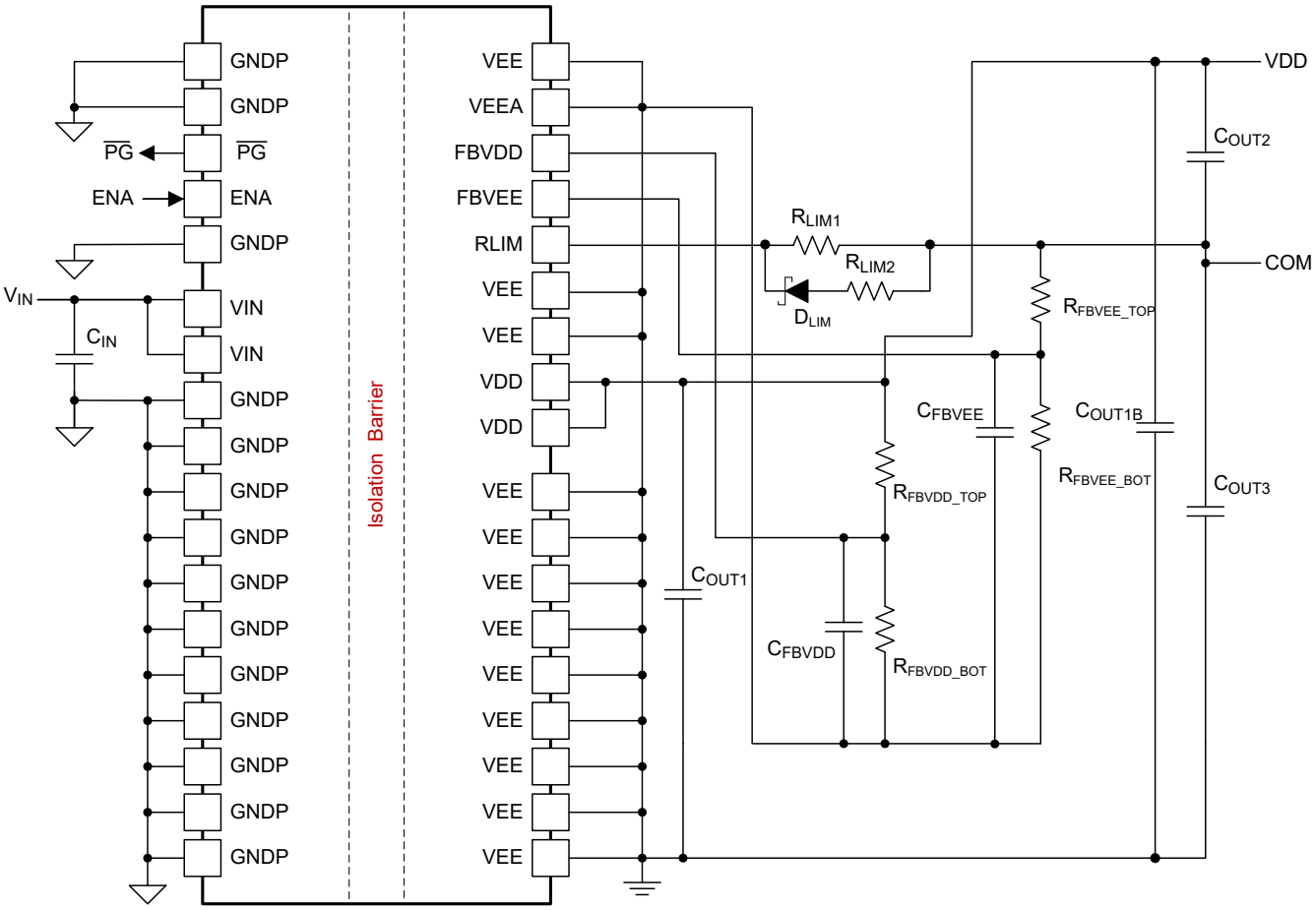

図 9-1. Dual Adjustable Output Configuration

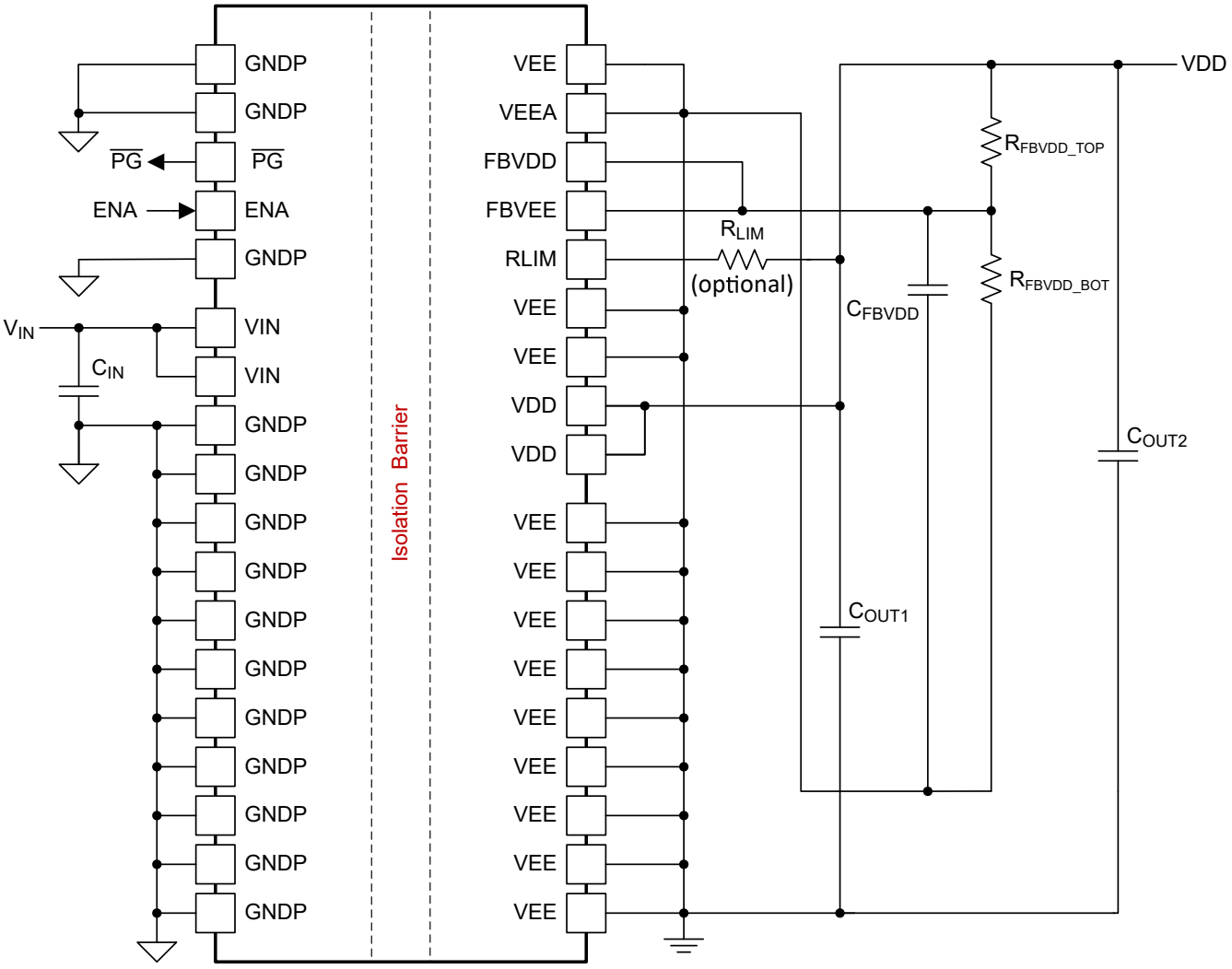

図 9-2. Single Adjustable Output Configuration

9.2.1 Design Requirements

Designing with the UCC14141-Q1 module is simple. First, choose single output or dual output. Determine the voltage for each output and then set the regulation through resistor dividers. Second, select the recommended input and output capacitors according to the procedure in the section of capacitor selection. The gate charge of the power device determines the amount of output decoupling capacitance needed at the gate driver input. Third, calculate the R_{LIM} resistor value for regulating the (COM – VEE) voltage rail for a dual output according to the procedure in the section of R_{LIM} or RDR selection.

For the dual output configuration, the VDD-to-VEE output capacitor placement and the RLIM-to-COM resistance introduce great impact to the power module performance and system BOM cost. 表 9-1 compares four combinations of two different VDD-to-VEE output decoupling capacitor placements and two R_{LIM} current-limit networks. The number 1 ranking represents the best, and the number 4 means the worst. The table indicates that case B offers the best performance and case A offers the lowest BOM cost. As shown in 図 9-1, C_{OUT1} is the decoupling capacitor closest to VDD and VEE pins, while C_{OUT1B} is the decoupling capacitor closest to the output load. Besides, the current-limit resistor network between RLIM pin and COM terminal is called the RDR circuitry, which can program the charge and discharge current of R_{LIM} regulator independently.

For the gate driver application with high di/dt current change as example, the finite impedance between the output terminal of power modules and the input bias terminal of output load greatly affects the transient response at the point of load, so the local decoupling capacitor C_{OUT1B} provides a very effective low-impedance

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decoupling for both $V_{VDD\text{-}to\text{-}COM}$ and $V_{COM\text{-}to\text{-}VEE}$ in the driver switching condition. From the schematic aspect, it seems that adding C_{OUT1B} means one more extra capacitor, but the reality is that it helps to avoid the need of oversizing C_{OUT2} and C_{OUT3}. With C_{OUT1B}, the reduced capacitance and capacitor body size for C_{OUT2} and C_{OUT3} end up a reduced total BOM cost on output capacitor bank. The following セクション 9.2.2.1 will describe the design procedure of C_{OUT1B} for more detail. Another benefit is that when capacitance of C_{OUT2} and C_{OUT3} is reduced, a higher R_{LIM} resistance can be used for COM-to-VEE regulation, so the power loss of RLIM regulator is reduced for higher power module efficiency.

表 9-1. Comparison of four design cases and their system-level implications

	C_{OUT1B}	RDR	Output Ripple	Efficiency	External BOM count/ cost
Case A	Yes	No	3	3	1 (Lowest)
Case B	Yes	Yes	1 (Lowest)	1 (Highest)	2
Case C	No	No	4	4	3
Case D	No	Yes	2	2	4

As shown in 図 9-1, the RDR circuitry is a current-limit resistor network of the RLIM pin to allow R_{LIM} regulator to optimize the charge and discharge current capabilities independently for further increasing the power module efficiency from the reduced power loss of R_{LIM} regulator. The circuity consists of three components, one high-resistance resistor R_{LIM1} in parallel with another resistor-diode branch, a small-resistance resistor R_{LIM2} in series with a small-signal diode D_{LIM}. R_{LIM1} resistance is much higher than R_{LIM2} resistance. Since $V_{VDD\text{-}to\text{-}VEE}$ is usually much higher than $V_{COM\text{-}to\text{-}VEE}$ especially in gate drive application, R_{LIM1} provides a high-resistance path for the internal charge switch to greatly reduce the switch current, so as to reduce the switching loss and conduction loss of the internal charge switch as well as the power loss of R_{LIM1} for higher efficiency. In addition, with a smaller charge current, the disturbance to $V_{VDD\text{-}to\text{-}VEE}$ ripple dipping effect at the charge switch turn-on instance will be minimized, so the total peak-to-peak ripple is reduced.

When the discharge switch turns on, the D_{LIM} provides a unidirectional path to divert most of the RLIM-pin current back to R_{LIM2}. This approach allows the RLIM regulator equipped with strong enough sinking capability to avoid the unbalanced current at COM-pin terminal from charging up $V_{COM\text{-}to\text{-}VEE}$ away from regulation band. Since $V_{COM\text{-}to\text{-}VEE}$ is lower than $V_{VDD\text{-}to\text{-}VEE}$ such as -5V respect to 25V as example, the power loss of the internal discharge switch and R_{LIM2} with larger switching current is less concern. On the contrary, if only one resistor is used to the RLIM pin, the resistor needs to design for worst case with lowest resistance to ensure $V_{COM\text{-}to\text{-}VEE}$ regulation, so the efficiency will be compromised. For example, the RDR circuitry with R_{LIM1} of 1kΩ and R_{LIM2} of 51Ω can increase the converter efficiency 7% higher with 10mA load from VDD to COM and reduce the case temperature 10°C, compared with using one R_{LIM} of 51Ω only.

Based on above, Case B is highly recommended as first choice in application. User can still use other thee design cases for other considerations. The design calculator provides a generic calculation tool to help user optimize each. The equations are based on the below detail descriptions.

9.2.2 Detailed Design Procedure

Place ceramic decoupling capacitors as close as possible to the device pins. For the input supply, place the capacitors between pins 6 to 7 (VIN) and pins 8 to 9 (GNDP). For the isolated output supply, (VDD – VEE), place the capacitors between pins 28 to 29 (VDD) and pins 30 to 31 (VEE). For the isolated output supply, (COM – VEE), place an R_{LIM} resistor between the RLIM pin and the gate driver COM supply input. Also place decoupling capacitors at the gate driver supply pins (VDD and COM) and at gate driver supply pins (COM and VEE) with values according to the following component calculation sections. These locations are of particular importance to all the decoupling capacitors because the capacitors supply the transient current associated with the fast switching waveforms of the power drive circuits. Ensure the capacitor dielectric material is compatible with the target application temperature.

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9.2.2.1 Capacitor Selection

The UCC14141-Q1 device creates an isolated output VDD-VEE as its main output. The device also creates a second output COM-VEE, using VDD-VEE as its power source. Because both outputs are isolated from the input, and sharing VEE as the common reference point, the UCC14141-Q1 outputs can be configured as dual-output two-positive, dual-output two-negative, or dual-output one-positive and one-negative. UCC14141-Q1 output can also be used as a single positive output or single negative output.

When the module is configured as dual-output, one-positive output, one-negative output; it is very important to properly select the output capacitor ratios C_{OUT2} and C_{OUT3} to optimize the regulation and avoid causing an over-voltage or under-voltage fault.

表 9-2. Calculated Capacitor Values

CAPACITOR	VALUE (µF)	NOTES
C_{IN}	20 + 0.1	Place a 20-µF and a 0.1-µF high-frequency decoupling capacitor in parallel close to VIN pins. A capacitance greater than 20 uF can be used to reduce the voltage ripple when the series impedance from the voltage source to the VIN pins is large.
C_{OUT1}	10 + 0.1	Add a 10-µF and a 0.1-µF capacitor for high-frequency decoupling of (VDD – VEE). Place close to the VDD and VEE pins. A capacitance greater than 10 uF can be used to reduce the output voltage ripple.
C_{OUT1B}	See below	Bulk charge, decoupling output capacitors are required to be located next to the gate driver pins. The C_{OUT2} and C_{OUT3} capacitance ratio is important to optimize the dual output voltage divider accuracy during charge or discharge switching cycles; while the C_{OUT1B} capacitor is used to minimize the total capacitance including C_{OUT1B}, C_{OUT2} , and C_{OUT3} capacitance values.
C_{OUT2}	See below	
C_{OUT3}	See below	

Output capacitor decoupling is important for optimal gate driver operation. Best high frequency decoupling can be achieved by reducing the parasitic impedance in the charge/discharge path. Using ceramic capacitors with low ESR and low ESL are important, as well as minimizing the trace impedance.

As described in 図 9-3, a decoupling capacitor C_{OUT1} is required at the $V_{VDD-VEE}$ output pins of the UCC14141-Q1 for high frequency decoupling. C_{OUT2} and C_{OUT3} however, are needed at the gate driver pins for $V_{VDD-COM}$ and $V_{VEE-COM}$ decoupling. The impedance between C_{OUT1} and the C_{OUT2}/C_{OUT3} combo prevents the C_{OUT1} from assisting the high frequency decoupling of the gate driver, requiring the C_{OUT2} and C_{OUT3} to take on the full load. The impedance may be contributed from the PCB traces, socket connections, EMI filters, or ferrite beads etc. This causes the C_{OUT2} and in particular the C_{OUT3} to get relatively large achieve a small voltage droop.

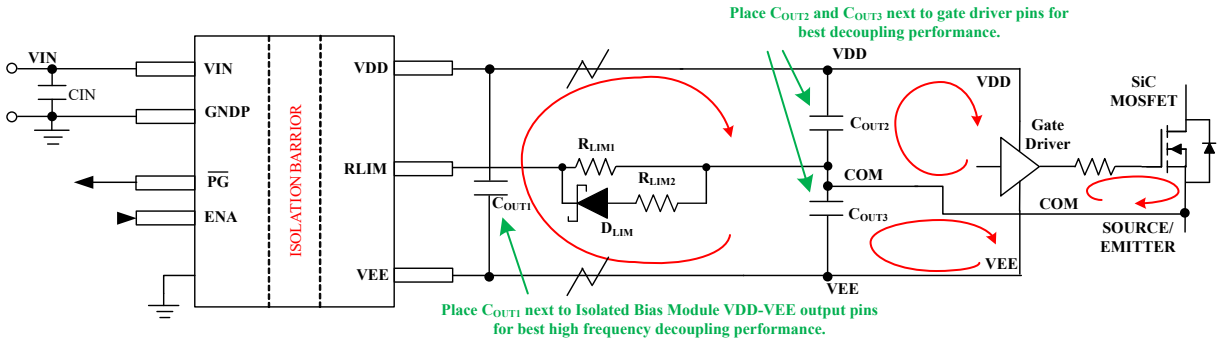

図 9-3. Dual Output Schematic with C_{out1}, C_{out2}, and C_{out3}

The required C_{OUT2} and C_{OUT3} capacitance can be reduced by introducing a C_{OUT1B} capacitor from $V_{VDD-VEE}$ at the gate driver pins next to C_{OUT2} and C_{OUT3} as shown in 図 9-4. The C_{OUT1B} assists with the decoupling total capacitance for both C_{OUT2} and C_{OUT3}; thereby reducing the total capacitance (C_{OUT1B} + C_{OUT2} +C_{OUT3}) needed to achieve the desired voltage droop. 図 9-5 shows that as C_{OUT1B} is increased from “none” to higher C_{OUT1B} values, there is a significant reduction in C_{OUT2} and C_{OUT3} and reduction of the total net capacitance, until a point of diminishing returns is reached (a “knee” point) where any additional C_{OUT1B} will have a relatively small reduction of C_{OUT2} and C_{OUT3}, and starts more significantly increasing the total net capacitance. The optimal

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C_{OUT1B}, C_{OUT2}, and C_{OUT3} at the minimum total net capacitance benefit both output capacitor size reduction and BOM cost reduction.

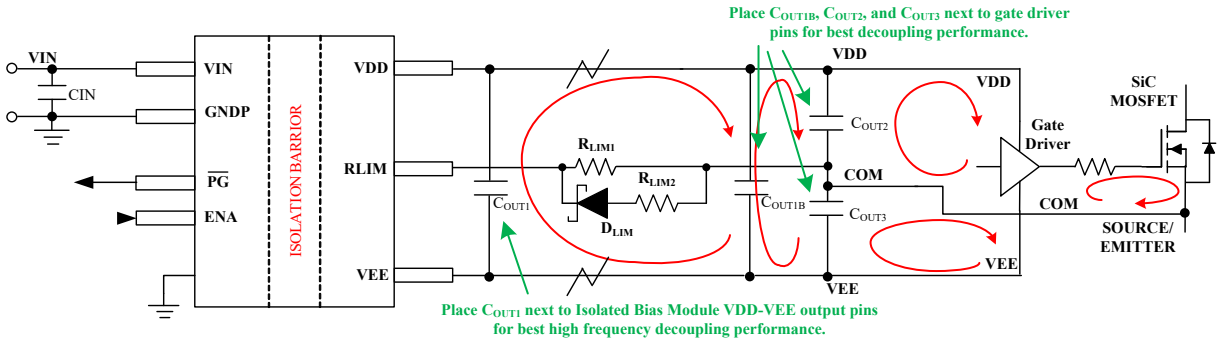

図 9-4. Dual Output Schematic with C_{out1}, C_{out1B}, C_{out2}, and C_{out3}

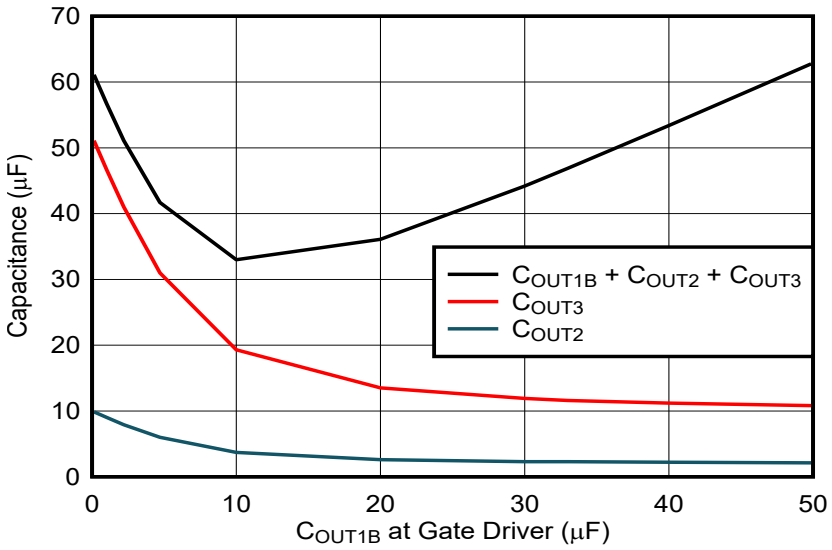

図 9-5. Output Capacitance variation with C_{out1B} selection

To calculate C_{OUT1B}, C_{OUT2}, and C_{OUT3}, we calculate the equivalent (VDD-COM) capacitance, which is equal to the series capacitance of C_{OUT1B} and C_{OUT3} in parallel with C_{OUT2}. This equivalent (VDD-VEE) capacitance will be sized to limit the predetermined (VDD-COM) discharge voltage drop when the power switch (SiC or IGBT) gate charge is turned-on.

$$C_{(VDD\text{-}COM)EQ} = \frac{C_{OUT1B} \times C_{OUT3}}{C_{OUT1B} + C_{OUT3}} + C_{OUT2} \quad (1)$$

Solving for acceptable voltage droop on $V_{VDD\text{-}COM}$ from the load transient, $\Delta V_{(VDD\text{-}COM)\_droop}$,

$$C_{(VDD-COM)_{EQ}} = \frac{Q_g}{\Delta V_{(VDD-COM)\_droop}} \quad (2)$$

The C_{OUT2} over C_{OUT3} ratio is defined as a coefficient of K_{23},which is the multiplication of a voltage divider ratio along with a ratio of differential current. The voltage divider ratio is from the series configuration of the two capacitors. The current divider ratio is calculated based on the charge current through the two capacitors. I_{MAX_POWER} is the maximum instantaneous current from the power module during the burst on-time, which can be obtained from dividing the maximum power on the datasheet SOA curve at T_A of 25°C by $V_{VDD\text{-}VEE}$. $I_{VDD\text{-}COM}$ is the total quiescent current between VDD and COM. For gate driver as example, $I_{VDD\text{-}VEE}$ is the current consumption without switching. $I_{COM\text{-}VEE}$ is the total quiescent current between COM and VEE. Based on KCL,

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the differential current charging up C_{OUT2} during the burst on-time is (I_{MAX_POWER} - $I_{VDD-COM}$), and the one charging up C_{OUT3} is (I_{MAX_POWER} - $I_{COM-VEE}$).

$$C_{OUT3} = C_{OUT2} \times K_{23} \tag{3}$$

where

$$K_{23} = \frac{V_{(VDD-COM)} \times \left(I_{MAX\_POWER} - I_{COM-VEE}\right)}{V_{(COM-VEE)} \times \left(I_{MAX\_POWER} - I_{VDD-COM}\right)} \tag{4}$$

Next, plugging the above C_{OUT3} expression into the 式 1 we get

$$\frac{Q_g}{\Delta V_{(VDD-COM)\_droop}} = \frac{C_{OUT1B} \times (C_{OUT2} \times K_{23})}{C_{OUT1B} + (C_{OUT2} \times K_{23})} + C_{OUT2} \tag{5}$$

The total decoupling capacitance close to the point of load (C_{OUT_Total}) is the summation of C_{OUT1B}, C_{OUT2} and C_{OUT3}. The goal is to find a smallest C_{OUT1B} to reduce C_{OUT_Total} to the minimum for BOM cost and footprint saving, while retaining the desired load transient performance. The optimal C_{OUT1B} can be calculated by solving the partial derivative of C_{OUT_Total} equal to 0.

$$\frac{dC_{OUT\_Total}}{dC_{OUT1B}} = \frac{d}{dC_{OUT1B}}(C_{OUT1B} + C_{OUT2} + C_{OUT3}) = 0 \tag{6}$$

Including the above C_{OUT3} and C_{OUT2} expressions onto 式 6, the optimal C_{OUT1B} is derived as

$$C_{OUT1B} = \frac{K_{23} \times Q_g \times \left({K_{23}}^3 + \sqrt{{K_{23}}^2 + K_{23} + 1} + {K_{23}}^2 \times \sqrt{{K_{23}}^2 + K_{23} + 1} - 1\right)}{\Delta V_{(VDD-COM)\_droop} \times (K_{23} + 1)^2 \times \left({K_{23}}^2 + K_{23} + 1\right)} \tag{7}$$

After that, solving 式 5 including 式 7, C_{OUT2} can be solved as

$$C_{OUT2} = \frac{K_{23} \times Q_g - (1 + K_{23}) \times C_{OUT1B} \times \Delta V_{(VDD-COM)droop}}{2 \times K_{23} \times \Delta V_{(VDD-COM)\_droop}} + \frac{\sqrt{C_{OUT1B}^2 \Delta V_{(VDD-COM)droop}^2 \left({K_{23}}^2 + 2K_{23} + 1\right) + 2C_{OUT1B}K_{23}Q_g \Delta V_{(VDD-COM)droop}(1 - K_{23}) + {K_{23}}^2 Q_g^2}}{2 \times K_{23} \times \Delta V_{(VDD-COM)\_droop}} \tag{8}$$

Overall, the design procedure of the three decoupling capacitors starts with C_{OUT1B} calculation, followed by C_{OUT2} and then C_{OUT3} calculation. The final capacitor values will be used to calculate R_{LIM}, as described in the next section.

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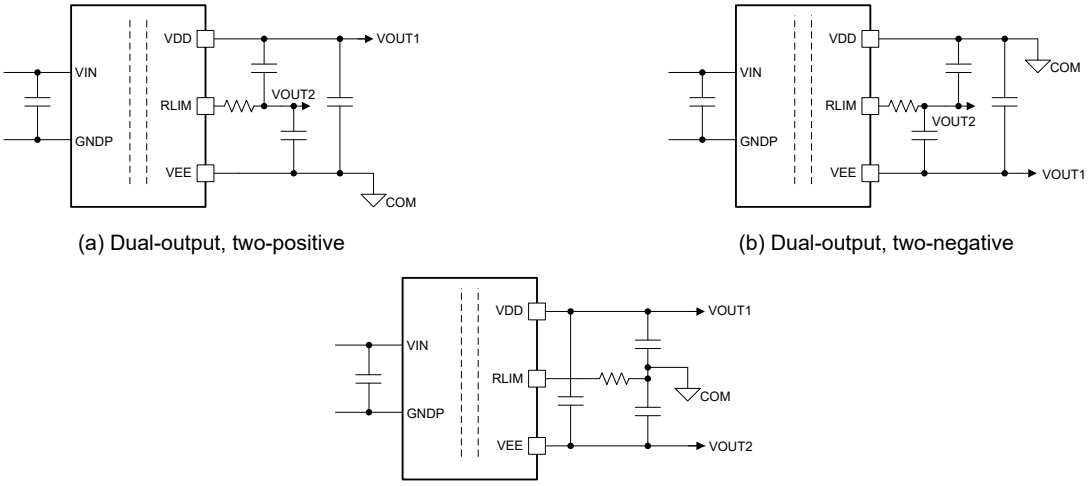
9.2.2.2 Single R_{LIM} Resistor Selection

The UCC14141-Q1 device creates an isolated output VDD-VEE as its main output. It also creates a second output COM-VEE, using VDD-VEE as its power source. Because both outputs are isolated from the input, and sharing VEE as the common reference point, the UCC14141-Q1 outputs can be configured as dual-output two-positive, dual-output two-negative, or dual-output one-positive and one-negative, as shown in 図 9-6.



(a) Dual-output, two-positive

(b) Dual-output, two-negative

(c) Dual-output, one-positive, one-negative

図 9-6. Dual output configurations

When the module is configured as dual-positive or dual-negative outputs, the R_{LIM} resistor is a true current limiting resistor. Set up the R_{LIM} resistor value as the maximum load current needed for V_{OUT2}, using 式 9. I_{VOUT2_max} is the maximum load current for V_{OUT2} output.

$$R_{LIM} = \frac{V_{OUT2}}{I_{VOUT2\_max}} - R_{LIM\_INT} \quad (9)$$

R_{LIM_INT} is the internal switch resistance value of 30 Ω typical.

For isolated gate driver applications, one positive and one negative outputs are needed. In this case, VDD-VEE is the total output voltage, and the middle point becomes the reference point. Because the total voltage between VDD and VEE is always regulated through the FBVDD feedback, the RLIM pin only must regulate the middle point voltage so that it can give the correct positive and negative voltages. The RLIM control is achieved through FBVEE pin as described in COM-VEE Voltage Regulation.

Based on Capacitor Selection, when selecting the output capacitor ratio proportional to the voltage ratio, the capacitors form a voltage divider. The middle point voltage must naturally give the correct positive and negative voltages. At the same time, for the gate driver circuit, the gate charge pulled out from the positive rail capacitor during turn-on is fed back to the negative rail capacitor during turn-off, the two output rail load must always be balanced. However, due to the gate driver circuit quiescent current unbalancing, and the two-rail capacitance tolerances, the middle point voltage can move away with time. The RLIM pin provides an opposite current to keep the middle point voltage at the correct level.

As illustrated in 図 9-7 (a), without considering the gate charge, the gate driver circuit quiescent current loads the positive rail and negative rail differently. The net current shows up as a DC offset current to the middle point.

As illustrated in 図 9-7 (b), every time the gate driver circuit turns-on the main power switch, it pulls the charge out of the positive and negative rail output capacitors. When the module power stage provides energy to the secondary side, refreshing those capacitors, the same charge is fed into both capacitors. If the capacitor values are perfect, the voltage rise in the capacitors will be proportional. The positive and negative voltages would not

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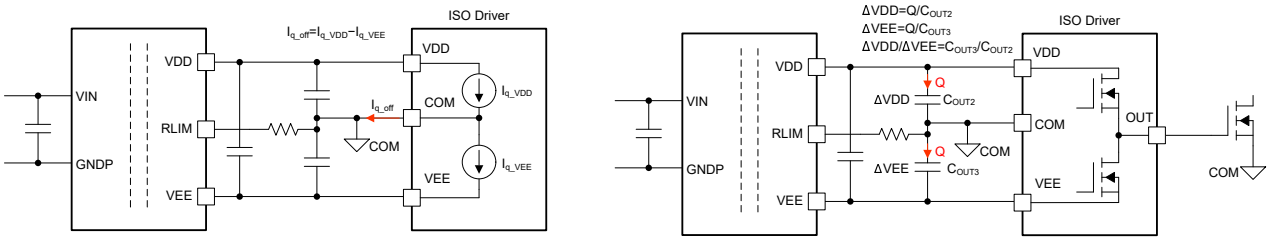
change. However, due to the capacitor tolerances, the capacitor values are not perfectly matched. The voltages will rise at different ratios with the smaller capacitor rising faster. Over time, the middle point voltage, COM, would pull to a different value. A load across one of the capacitors will pull towards a voltage imbalance. The RLIM function counteract the voltage imbalance and bring the COM voltage back into regulation.



(a) Load current unbalancing

(b) Capacitance unbalancing

図 9-7. Source of voltage unbalancing

Considering these two effects, the R_{LIM} must provide enough current to compensate this offset current. The R_{LIM} must be low enough to provide enough current, but not too low otherwise the middle point voltage is corrected at each turn on and turn off edge of the gate driver and excessive power loss is generated.

The R_{LIM} resistor is chosen to provide enough current for the load using the following 3 equations, whichever has lowest value.

$$R_{LIM\_MAX\_H} = \frac{V_{VDD-COM}}{\left[\frac{C_{OUT3}\times(1-\Delta C_{OUT3})}{C_{OUT2}\times(1-\Delta C_{OUT2})+C_{OUT3}\times(1-\Delta C_{OUT3})}-\frac{C_{OUT3}}{C_{OUT2}+C_{OUT3}}\right]\times Q_{G\_Total}\times f_{SW}+\Delta I_{COM\_SOURCE}} - R_{LIM\_INT} \quad (10)$$

where

- Q_{G_Total} is the total gate charge of power switch.
- f_{SW} is the switching frequency of gate drive load.
- $\Delta I_{COM\_SOURCE}=I_{COM-VEE}-I_{VDD-COM}$, when $I_{COM-VEE}>I_{VDD-COM}$. Otherwise, $\Delta I_{COM\_SOURCE}=0A$.

$$R_{LIM\_MAX\_L1} = \frac{V_{COM-VEE}}{\left[\frac{C_{OUT2}\times(1-\Delta C_{OUT2})}{C_{OUT2}\times(1-\Delta C_{OUT2})+C_{OUT3}\times(1-\Delta C_{OUT3})}-\frac{C_{OUT2}}{C_{OUT2}+C_{OUT3}}\right]\times Q_{G\_Total}\times f_{SW}+\Delta I_{COM\_SINK}} - R_{LIM\_INT} \quad (11)$$

where $\Delta I_{COM\_SINK}=I_{VDD-COM}-I_{COM-VEE}$, when $I_{COM-VEE}<I_{VDD-COM}$. Otherwise, $\Delta I_{COM\_SINK}=0A$.

$$R_{LIM\_MAX\_L2} = \frac{V_{COM-VEE}}{\left[(C_{OUT3}+TOLERANCE_{COUT3})\times\frac{0.10\times V_{COM-VEE}}{3\ ms}\right]+\Delta I_{COM\_SINK}} - R_{LIM\_INT} \quad (12)$$

Select R_{LIM} value to be the lowest of either 1) the R_{LIM} needed for capacitor imbalance and the load, calcualted by $R_{LIM\_MAX\_H}$ and $R_{LIM\_MAX\_L1}$, or 2) the R_{LIM} needed to respond to a $V_{COM-VEE}$ transient within 3 ms with the given load current, calcuated by $R_{LIM\_MAX\_L2}$.

R_{LIM} value determines response time of (COM – VEE) regulation. Too low an R_{LIM} value can cause oscillation and can overload (VDD – VEE). Too high an R_{LIM} value can give offset errors, due to slow response. If R_{LIM} is greater than above calculations, then there is not enough current available to replenish the charge to the output capacitors, causing a charge imbalance where the voltage is not able to maintain regulation, and eventually exceeds the OVP or UVP FAULT thresholds and shutting down the device for protection. Choose R_{LIM} value to be close but smaller than the smallest value of the three calculated results.

The power loss of R_{LIM} can be derived as

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$$P_{RLIM} = \frac{V_{VDD-COM}^{2}}{R_{LIM}} Duty_{RLIM} + \left(\left[\frac{C_{OUT2} \times (1 - \Delta C_{OUT2})}{C_{OUT2} \times (1 - \Delta C_{OUT2}) + C_{OUT3} \times (1 - \Delta C_{OUT3})} - \frac{C_{OUT2}}{C_{OUT2} + C_{OUT3}} \right] \times Q_{G\_Total} \times f_{SW} + \Delta I_{COM\_SINK} \right)^{2} \times R_{LIM} \quad (13)$$

where $Duty_{RLIM}$ is the duty cycle of RLIM-pin switch on-time respect to the switching cycle. 33% can be used as a reasonable rule of thumb for power loss calculation purpose.

9.2.2.3 RDR Circuit Component Selection

R_{LIM1} value is chosen by 式 10. R_{LIM2} value is chosen by

$$R_{LIM2} = \frac{V_{COM-VEE} - 0.5}{V_{COM-VEE} \cdot \left(\frac{1}{R_{LIM\_MAX\_L}} - \frac{1}{R_{LIM\_MAX\_H}}\right)} \quad (14)$$

where $R_{LIM\_MAX\_L}$ is the smallest value between $R_{LIM\_MAX\_L1}$ and $R_{LIM\_MAX\_L2}$ in the Single R_{LIM} Resistor Selection Section, and 0.5V represents the diode forward voltage drop of D_{LIM}.

When the calculated R_{LIM1} and R_{LIM2} values have large enough difference, the RDR improvement on efficiency will be significant. If R_{LIM1} and R_{LIM2} values are close, then single R_{LIM} resistor can be considered to reduce the external components.

The power loss of R_{LIM1} can be derived as

$$P_{RLIM1} = \frac{V_{VDD-COM}^2}{R_{LIM1}} Duty_{RLIM} + \left(I_{SINK} \times \frac{V_{COM-VEE} \times R_{LIM2}}{V_{COM-VEE} \times R_{LIM2} + (V_{COM-VEE} - 0.5) \times R_{LIM1}}\right)^2 \times R_{LIM1} \quad (15)$$

where

$$I_{SINK} = \left[\frac{C_{OUT2} \times (1 - \Delta C_{OUT2})}{C_{OUT2} \times (1 - \Delta C_{OUT2}) + C_{OUT3} \times (1 - \Delta C_{OUT3})} - \frac{C_{OUT2}}{C_{OUT2} + C_{OUT3}}\right] \times Q_{G_{Total}} \times f_{SW} + \Delta I_{COM_{SINK}} \quad (16)$$

The power loss of R_{LIM2} can be approximated as

$$P_{RLIM2} = \left(I_{SINK} \times \frac{(V_{COM-VEE} - 0.5) \times R_{LIM1}}{V_{COM-VEE} \times R_{LIM2} + (V_{COM-VEE} - 0.5) \times R_{LIM1}}\right)^2 \times R_{LIM2} \quad (17)$$

The maximum voltage rating of diode D_{LIM} needs to consider the highest $V_{VDD\text{-}to\text{-}VEE}$. The maximum current rating of D_{LIM} can be chosen based on the derating from the worst-case continuous current, ($V_{COM\text{-}to\text{-}VEE}$ – V_{F_DLIM}) / R_{LIM2}, where V_{F_DLIM} is the forward voltage of D_{LIM}. The diode package size is determined based on the power loss in forward conduction, P_{Loss_DLIM} = V_{F_DLIM} x (($V_{COM\text{-}to\text{-}VEE}$ – V_{F_DLIM}) / R_{LIM2}). A Schottky diode is recommended to reduce the power loss.

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9.3 System Examples

The UCC14141-Q1 module is designed to allow a microcontroller host to enable it with the ENA pin for proper system sequencing. The $\overline{PG}$ output also allows the host to monitor the status of the module. The $\overline{PG}$ pin goes low when there are no faults and the output voltage is within ±10% of the set target output voltage. The output voltage is meant to power a gate driver for either IGBT or SiC FET power device. The host can start sending PWM control to the gate driver after the $\overline{PG}$ pin goes low to ensure proper sequencing. The below figures are the system diagrams for the dual-output configuration and for the single output configuration.

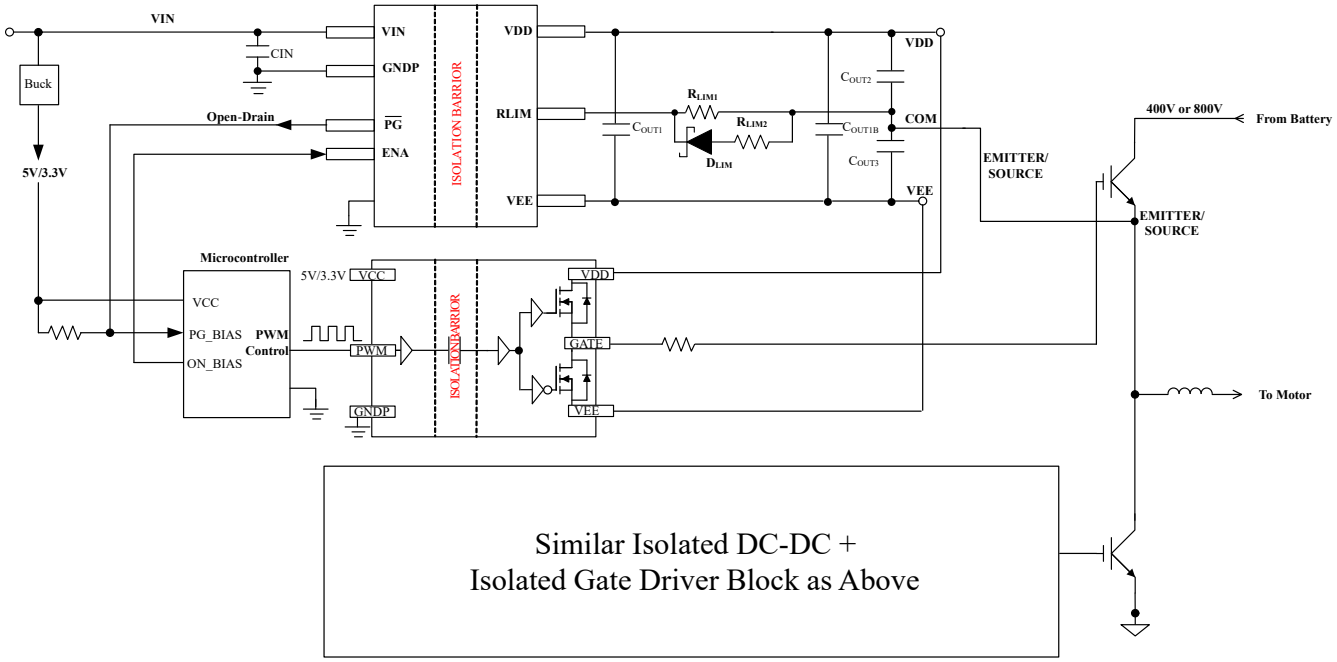

図 9-8. Dual Output System Configuration

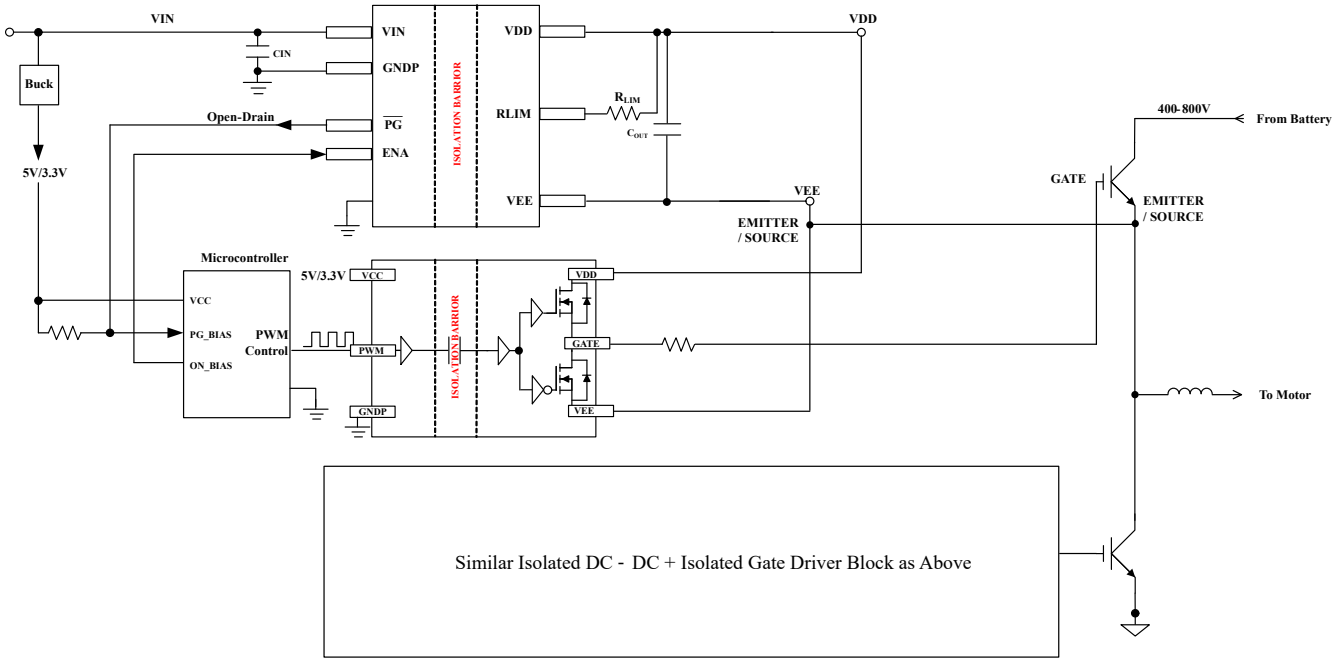

図 9-9. Single Output System Configuration

9.4 Power Supply Recommendations

The recommended input supply voltage (V_{VIN}) for UCC14141-Q1 is between 8 V and 18 V. To help ensure reliable operation, adequate decoupling capacitors must be located as close to supply pins as possible. Local bypass capacitors must be placed between the VIN and GNDP pins at the input; between VDD and VEE at the isolated output supply; and COM and VEE at the lower voltage output supply. TI recommends low ESR, ceramic surface mount capacitors. 表 9-2 provides the recommended capacitance for high frequency decoupling. The input supply must have an appropriate current rating to support output load required by the end application.

9.5 Layout

9.5.1 Layout Guidelines

The UCC14141-Q1 integrated isolated power solution simplifies system design and reduces board area usage. Follow these guidelines for proper PCB layout to achieve optimum performance. A minimum of 4-layer PCB layer stack using 2-ounce copper on external layers is recommended to accomplish a good thermal PCB design.

1. Input capacitors:
   a. Place the 0.1-µF high frequency bypass capacitor (C14) as close as possible to pins 6, 7 (VIN) and pins 8–18 (GNDP) and on the same side of the PCB as the IC. 0402 ceramic SMD or smaller is a desired size for optimal placement. Do not place any vias between the bypass capacitor and the IC pins so as to force the high frequency current through the capacitor.
   b. Place the bulk VIN capacitor(s) (C12, C13) as close as possible and parallel to the 0.1 µF high frequency bypass capacitor (C14) and on the same side of the PCB as the IC.
2. Output capacitors:
   a. Place the 0.1-µF high frequency bypass capacitor (C7) as close as possible to pins 28, 29 (VDD) and pins 30, 31 (VEE) and on the same side of the PCB as the IC. 0402 ceramic SMD or smaller is a desired size for optimal placement. Do not place any vias between the bypass capacitor and the IC pins so as to force the high frequency current through the capacitor.
   b. Place the bulk VDD-VEE capacitor (C8) as close as possible and parallel to the 0.1-µF high frequency bypass capacitor (C7) and on the same side of the PCB as the IC.

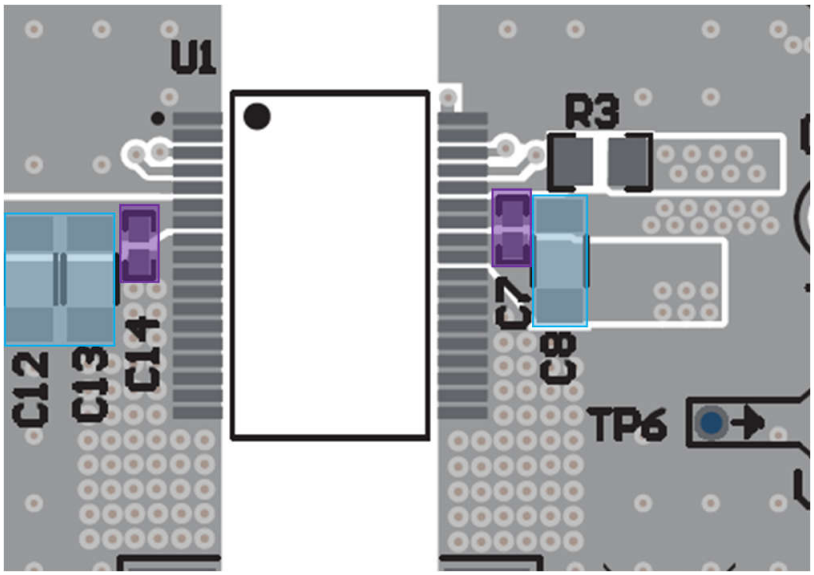

図 9-10.

3. Gate driver output capacitors: C_{OUT2} and C_{OUT3} are reference designators referred to in the Excel calculator tool. C_{OUT2} is the capacitor(s) between VDD-COM and C_{OUT3} is the capacitor(s) between COM-VEE. C_{OUT2} and C_{OUT3} are capacitors required by the gate driver IC. Proper selection and component placement of C_{OUT2} and C_{OUT3} are critical for optimal performance of the UCC14141-Q1 and the gate driver IC.
   a. C_{OUT2} and C_{OUT3} should be placed next to the gate driver IC for best decoupling and gate driver switching performance

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b. Adding a C_{OUT1B} between VDD-VEE but placed at the gate driver in parallel with C_{OUT2} and C_{OUT3} will reduce the total capacitance needed and reduce the sensitivity to capacitor variation, and will allow to use a higher R_{LIM} resistance value.

4. R_{LIM}: Place R_{LIM} (R3) close to pin 32 and between the COM midpoint of the output capacitive divider. The via pattern shown to the right of R3 connects to COM.

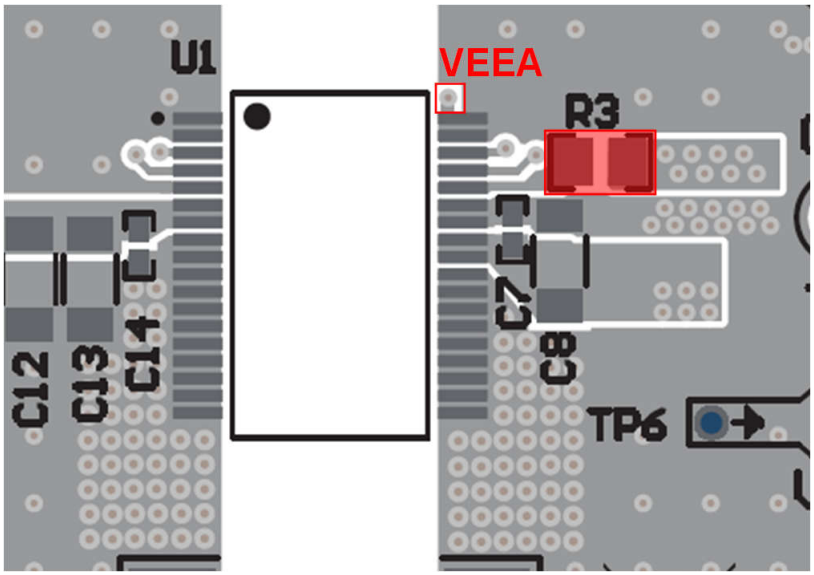

図 9-11.

5. Feedback:

a. VEEA (pin 35) should be isolated through all PCB layers, from the VEE plane as shown in the red box below. Use one via to make a direct connection to the FBVDD and FBVEE low-side resistors and capacitors (C15-16, R6-7), shown on the bottom side of the PCB.

b. Place feedback resistors (R4-7) and 330-pF ceramic capacitor in parallel with low-side resistors (R6-7) close to the IC preferably on the opposite side of IC (as shown in EVM), or on same layer as IC near pin 36.

c. The top-side feedback resistor should be placed next to the low-side resistor with a short, direct connection between both resistors and single connection to FBVDD. The top connection to sense the regulated rail (VDD-VEE) should be routed and connected at the VDD bias capacitor remote location near the gate driver pins for best accuracy and best transient response.

d. The top-side feedback resistor should be placed next to the low-side resistor with a short, direct connection between both resistors and single connection to FBVEE; while the top connection to sense the regulated rail (COM-VEE) should be routed and connected at the COM bias capacitor remote location near the gate driver pins for best accuracy and best transient response.

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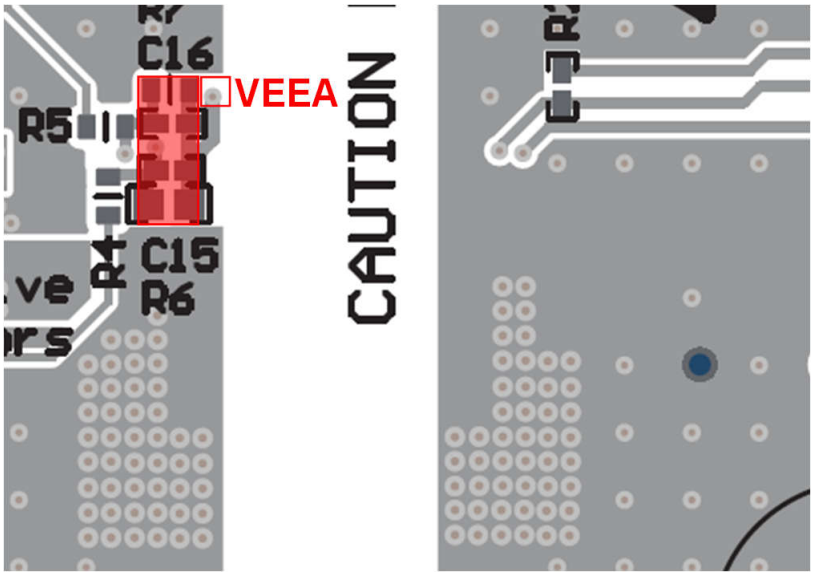

図 9-12.

6. Thermal Vias: TheUCC14141-Q1 internal transformer makes a direct connection to the lead frame. It is therefore critical to provide adequate space and proper heatsinking designed into the PCB as outlined in the steps below.
   a. TI recommends to connect the VIN, GNDP, VDD, and VEE pins to internal ground or power planes through multiple vias. Alternatively, make the polygons connected to these pins as wide as possible.
   b. Use multiple thermal vias connecting PCB top side GNDP copper to bottom side GNDP copper. If possible, it is recommended to use 2-ounce copper on external top and bottom PCB layers.
   c. Use multiple thermal vias connecting PCB top side VEE copper to bottom side VEE copper. If possible, it is recommended to use 2-ounce copper on external top and bottom PCB layers.
   d. Thermal vias connecting top and bottom copper can also connect to internal copper layers for further improved heat extraction.
   e. Thermal vias should be similar to pattern shown below but apply as many as the copper area will allow. The UCC14141EVM-068 uses thermal via arrays of approximately 220 mil x 350 mil (48 thermal vias on GNDP primary and 54 thermal vias on VEE secondary). Thermal via is 30 mil diameter, 12 mil hole size.

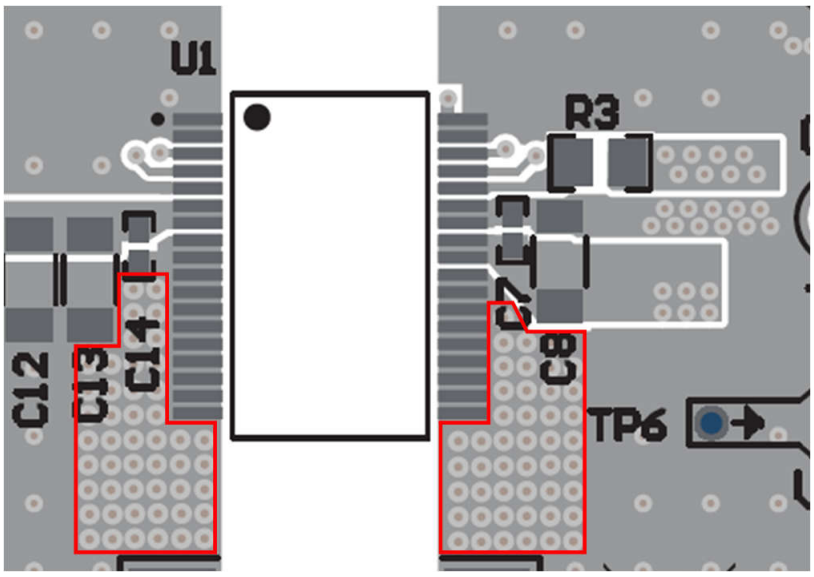

図 9-13.

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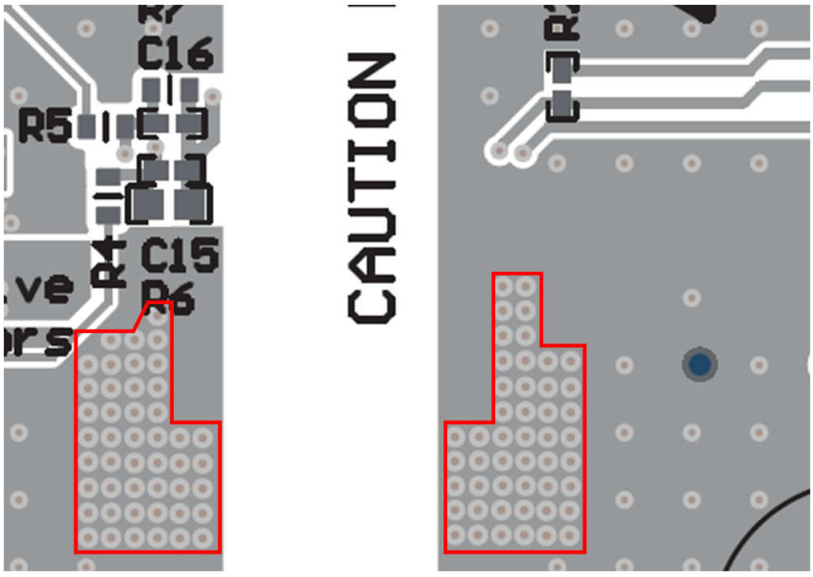

図 9-14.

f. As seen in the Thermal Image, there is a point of diminishing return, regarding the number of vias and size of the thermal via array. For 1.5-W of output power, heat transfer is shown to quickly diminish just beyond C12 and C8. The distance from the inner pad line of U1 to C12 is 320 mils.

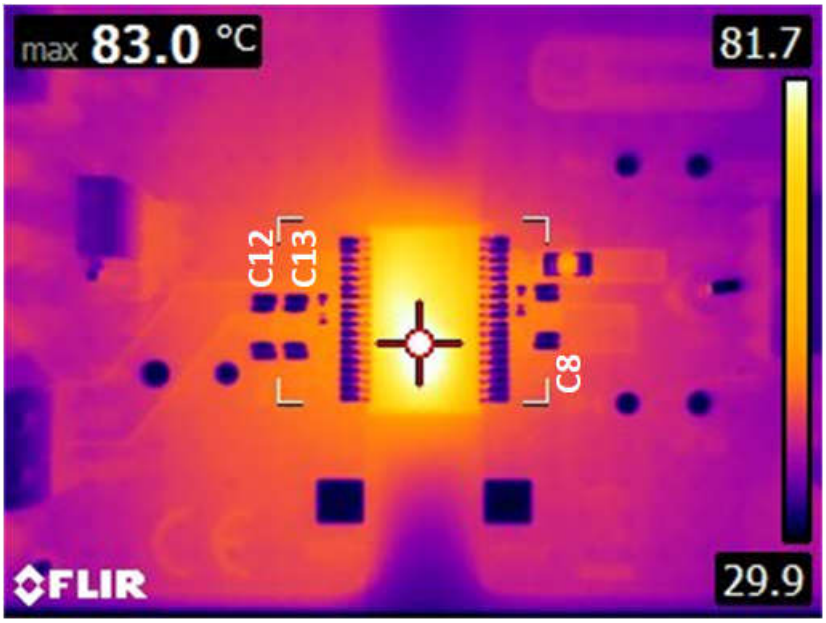

図 9-15. Thermal Image

7. Creepage clearance: Avoid routing copper under the UCC14141-Q1 , to maintain the full creepage, clearance and basic voltage isolation ratings specified in the data sheet. Maintain the clearance width highlighted in red, throughout the entire defined isolation barrier. Keep-out clearance for basic isolation can be 50% less than the reinforced isolation requirement (8mm). Using 8mm provides additional margin.

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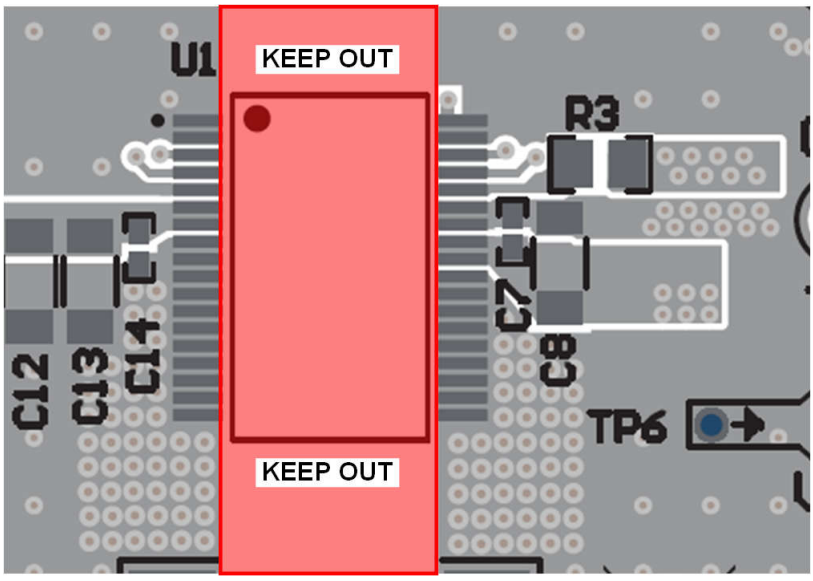

図 9-16.

8. Gate driver capacitors and feedback routing:
   a. VDD-COM and VEE-COM capacitors are populated on the UCC14141EVM-068 but these capacitors need to be placed as close to the associated gate driver pins as possible.
   b. For optimal voltage regulation, the feedback trace from COM (COM FB) and VDD (VDD FB) should be as direct as possible so that the voltage feedback is being sensed directly at the VDD and COM capacitors near the gate driver IC.

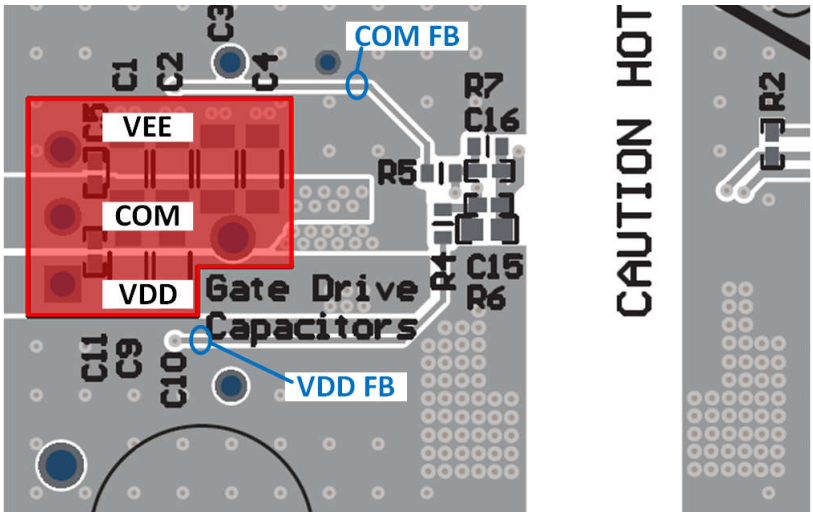

図 9-17.

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9.5.2 Layout Example

The layout example shown in the following figures is from the evaluation board UCC14141-Q1EVM, UCC14141EVM-068, and based on the 図 9-1 design.

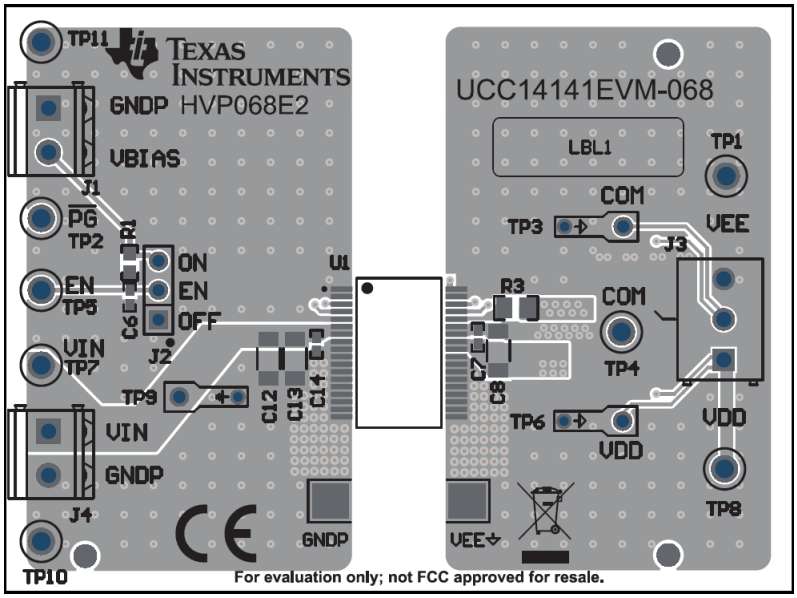

図 9-18. UCC14141-Q1EVM, PCB Top Layer, Assembly

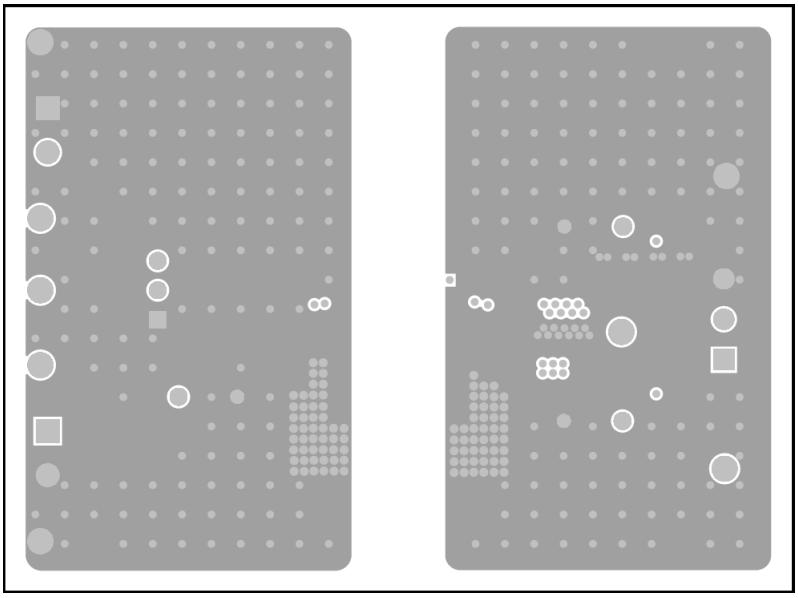

図 9-19. UCC14141-Q1EVM, Signal Layer 2 (Same as Layer 3)

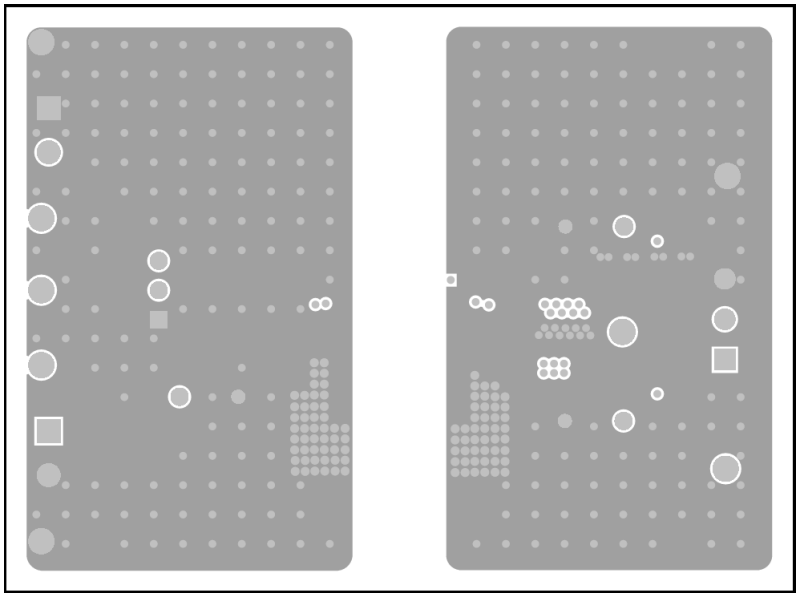

図 9-20. UCC14141-Q1EVM, Signal Layer 3 (Same as Layer 2)

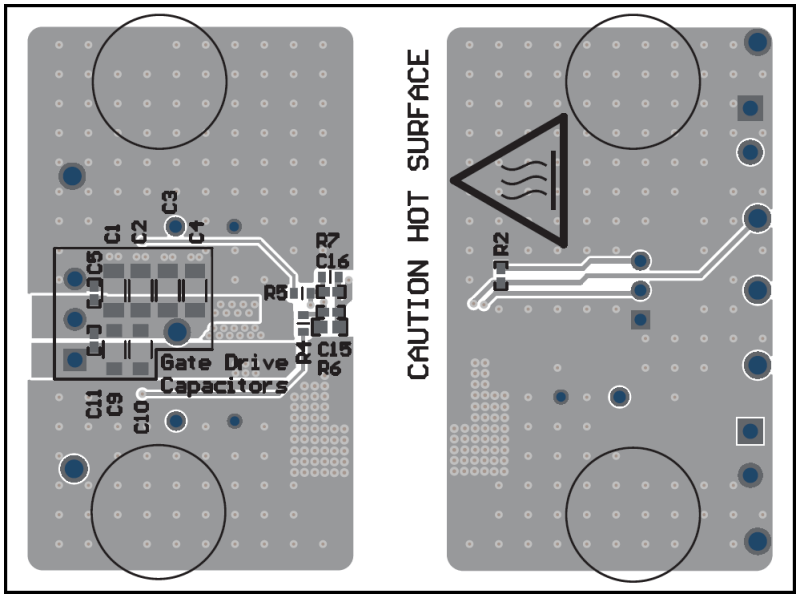

図 9-21. UCC14141-Q1EVM, PCB Bottom Layer, Assembly (Mirrored View)

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10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Using the UCC14240EVM-052 for Biasing Traction Inverter Gate Driver ICs Requiring Single, Positive or Dual, Positive/Negative Bias Power user's guide*
- Texas Instruments, *Isolation Glossary*

10.2 ドキュメントの更新通知を受け取る方法

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10.6 用語集

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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC14141QDWNRQ1	Active	Production	SO-MOD (DWN) | 36	750 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCC14141-Q1
UCC14141QDWNRQ1.A	Active	Production	SO-MOD (DWN) | 36	750 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCC14141-Q1
UCC14141QDWNRQ1.B	Active	Production	SO-MOD (DWN) | 36	750 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF UCC14141-Q1 :

- Catalog : UCC34141-Q1

NOTE: Qualified Version Definitions:

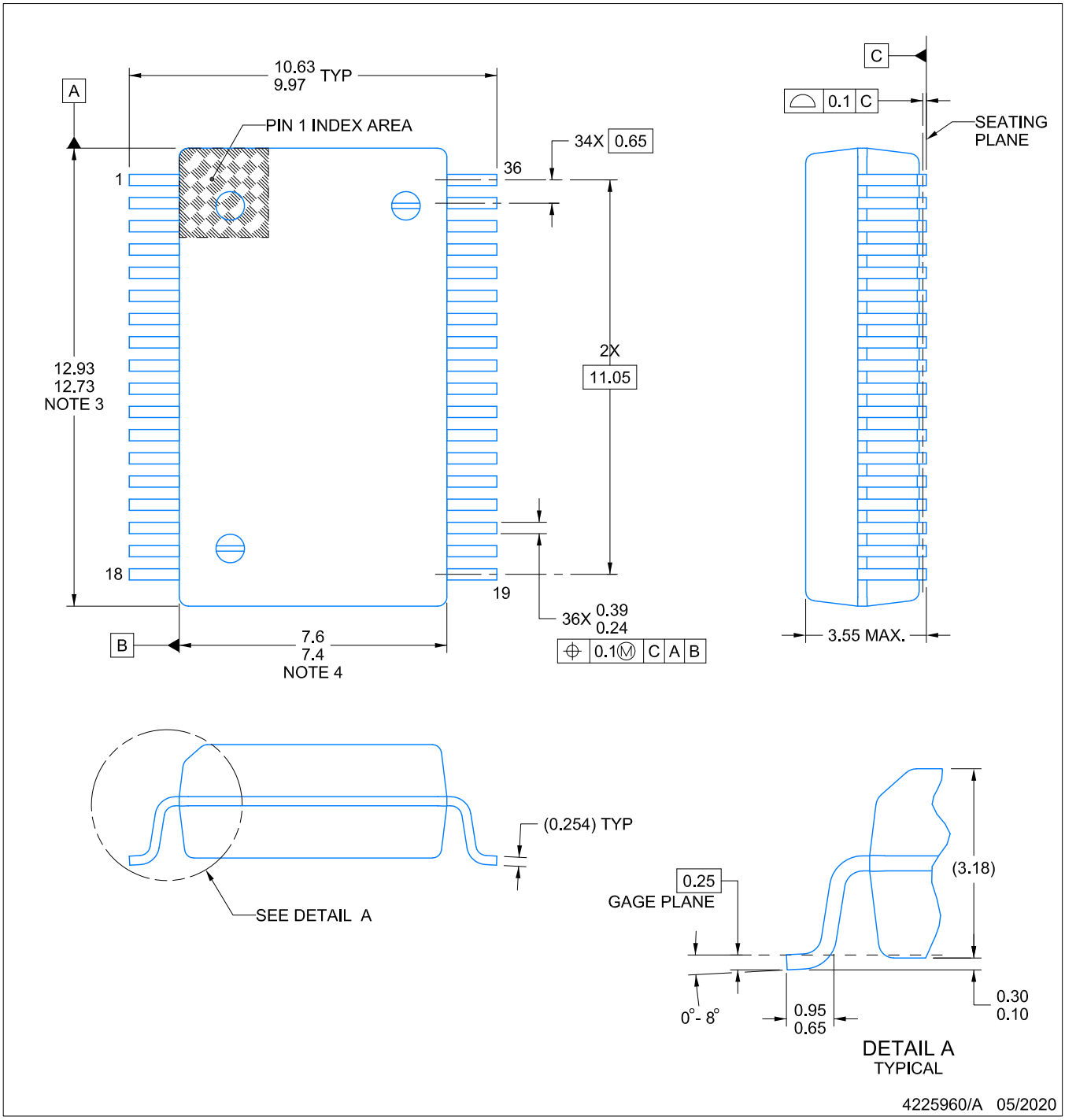
- Catalog - TI's standard catalog product

PACKAGE OUTLINE

DWN0036A

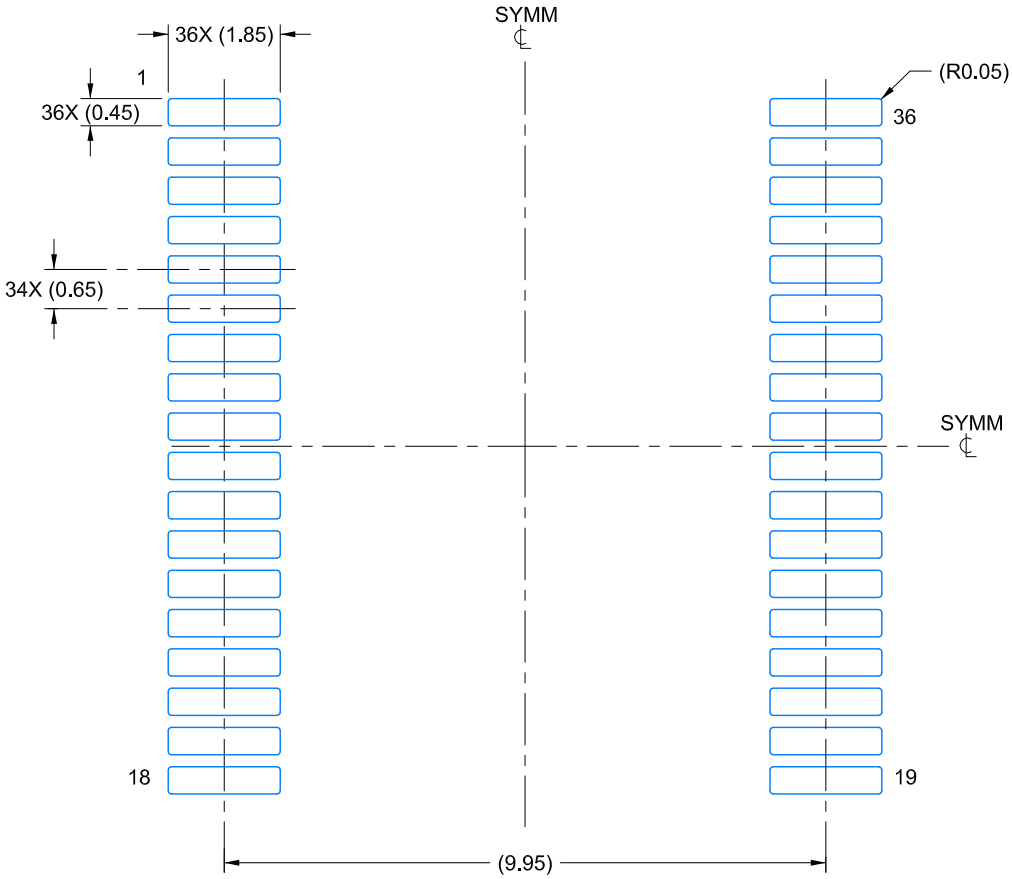
SSOP - 3.55 mm max height

SMALL OUTLINE PACKAGE

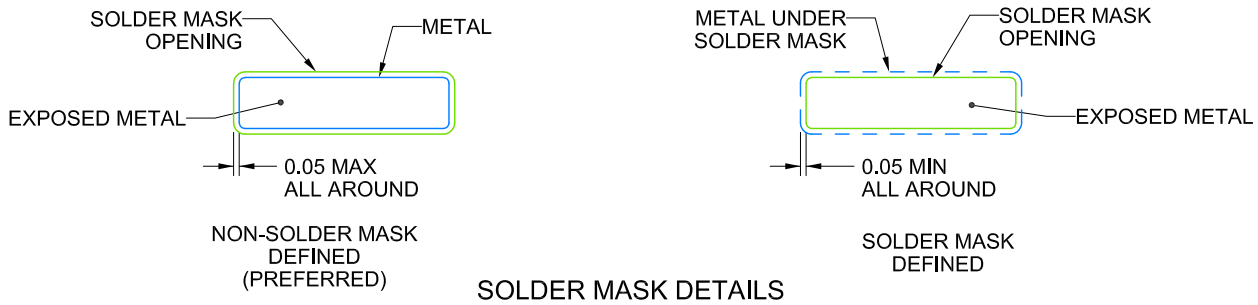


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

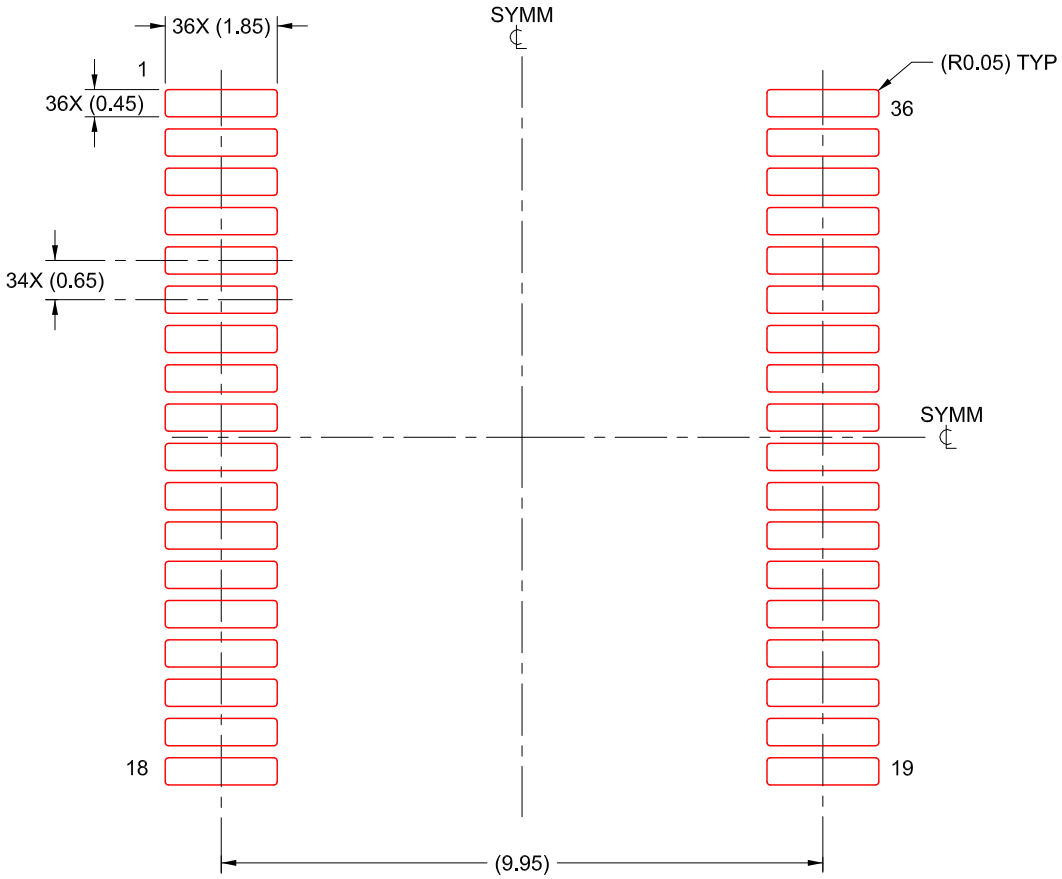


SOLDER MASK DETAILS

4225960/A 05/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

4225960/A 05/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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