UCC21222-Q1 車載用 4A、6A、3kVRMS 絶縁型デュアル チャネル ゲート ドライバ、デッドタイム機能付き

1 特長

- 汎用:デュアル ローサイド、デュアル ハイサイド、またはハーフ ブリッジ ドライバ
- 次の結果で AEC Q100 認定済み
  - デバイス温度グレード 1
  - デバイス HBM ESD 分類レベル H2
  - デバイス CDM ESD 分類レベル C4B
- 接合部温度範囲:-40°C～+150°C
- ピーク ソース 4A、ピーク シンク 6A の出力
- 125V/ns を超える同相過渡耐性 (CMTI)
- 最大 25V の VDD 出力駆動電源
  - VDD UVLO:8V
- スイッチング パラメータ:
  - 伝搬遅延時間:33ns (代表値)
  - 最大パルス幅歪み:5ns
  - 最大 VDD 電源オン遅延:10µs
- あらゆる電源に対応する UVLO 保護
- 高速なディセーブルによる電源シーケンス

2 アプリケーション

- HEV および EV バッテリ充電器
- AC/DC および DC/DC 電源の絶縁型コンバータ
- モータ ドライブとインバータ

3 概要

UCC21222-Q1 デバイスは、デッドタイムをプログラムでき広い温度範囲に対応する絶縁型デュアル チャネル ゲートドライバです。極端な温度条件下でも安定した性能を提供し、堅牢性に優れています。ピーク電流はソース 4A、シンク 6A で、パワー MOSFET、IGBT、GaN トランジスタを駆動するように設計されています。

UCC21222-Q1 デバイスは、2 つのローサイド ドライバ、2 つのハイサイド ドライバ、または 1 つのハーフ ブリッジ ドライバとして構成可能です。5ns の遅延マッチング性能により、内部貫通電流のリスクを伴わずに、2 つの出力を並列化して 2 倍の駆動力で重負荷条件に対応できます。

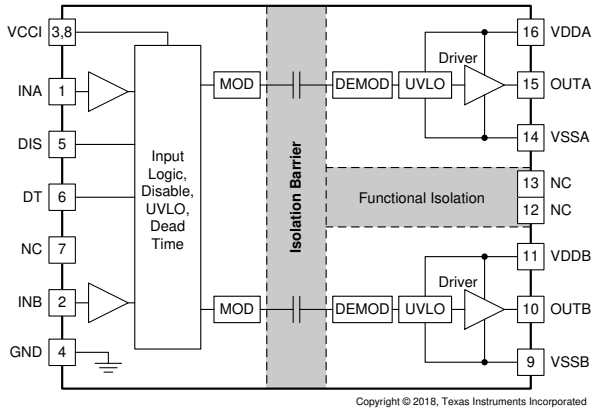
入力側は、3.0kV$_{RMS}$ の絶縁バリアによって 2 つの出力ドライバと分離されており、同相過渡耐性 (CMTI) は 125V/ns 以上です。

抵抗によるデッドタイムのプログラミングが可能なため、システムの制約に合わせてデッドタイムを調整することにより、効率を高め、出力のオーバーラップを防止できます。その他の保護機能として、DIS を High に設定した場合に 2 つの出力を同時にシャットダウンするディスエーブル機能、5ns 未満の入力過渡を除去する内蔵グリッチ除去フィルタ、入力 / 出力ピンでの 200ns にわたる最大 -2V のスパイクに対応する負電圧処理機能があります。すべての電源が UVLO 機能を備えています。

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
UCC21222-Q1	D (SOIC 16)	9.9mm × 3.91mm

(1) 供給されているすべてのパッケージについては、セクション 13 を参照してください。



機能ブロック図

Table of Contents

1 特長 1
2 アプリケーション 1
3 概要 1
4 Pin Configuration and Functions 3
5 Specifications 4
5.1 Absolute Maximum Ratings 4
5.2 ESD Ratings (Automotive) 4
5.3 Recommended Operating Conditions 4
5.4 Thermal Information 4
5.5 Power Ratings 5
5.6 Insulation Specifications 6
5.7 Safety Limiting Values 7
5.8 Electrical Characteristics 8
5.9 Switching Characteristics 9
5.10 Insulation Characteristics Curves 10
5.11 Typical Characteristics 11
6 Parameter Measurement Information 15
6.1 Minimum Pulses 15
6.2 Propagation Delay and Pulse Width Distortion 15
6.3 Rising and Falling Time 15
6.4 Input and Disable Response Time 16
6.5 Programmable Dead Time 16
6.6 Power-Up UVLO Delay to OUTPUT 17
6.7 CMTI Testing 18
7 Detailed Description 19
7.1 Overview 19
7.2 Functional Block Diagram 19
7.3 Feature Description 20
7.4 Device Functional Modes 23
8 Application and Implementation 25
8.1 Application Information 25
8.2 Typical Application 25
9 Power Supply Recommendations 35
10 Layout 36
10.1 Layout Guidelines 36
10.2 Layout Example 37
11 Device and Documentation Support 39
11.1 Device Support 39
11.2 Documentation Support 39
11.3 ドキュメントの更新通知を受け取る方法 39
11.4 サポート・リソース 39
11.5 Trademarks 39
11.6 静電気放電に関する注意事項 40
11.7 用語集 40
12 Revision History 40
13 Mechanical, Packaging, and Orderable Information 40

4 Pin Configuration and Functions

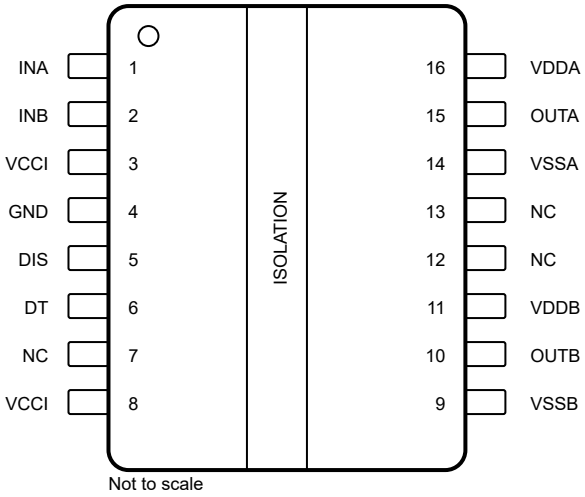


図 4-1. D Package 16-Pin SOIC Top View

表 4-1. Pin Functions

PIN		TYPE (1)	Description
NAME	NO.		
DIS	5	I	Disable both driver outputs if asserted high, enable both outputs if set low. It is recommended to tie this pin to ground if not used to achieve better noise immunity. This pin is internally pulled high if left floating. It is recommended to use an RC filter on DIS pin to filter high frequency noise when connecting to a microcontroller, with R = 0 Ω to 100 Ω and C = 100 pF to 1000 pF.
DT	6	I	DT pin configurations: • DT pin float or short to VCCI disables dead time interlock function (allows outputs to overlap) • Place 1.7-kΩ to 100-kΩ resistor (RDT) between DT and GND to set minimum dead time between driver outputs • Place 0-Ω to 150-Ω resistor, or short DT pin to GND to have two outputs interlocked
GND	4	P	Primary-side ground reference. All signals in the primary side are referenced to this ground.
INA	1	I	Input signal for A channel. INA input has a TTL/CMOS compatible input threshold. This pin is pulled low internally if left open. Tie this pin to ground if not used to achieve better noise immunity.
INB	2	I	Input signal for B channel. INB input has a TTL/CMOS compatible input threshold. This pin is pulled low internally if left open. Tie this pin to ground if not used to achieve better noise immunity.
NC	7	—	No internal connection
	12		
	13		
OUTA	15	O	Output of driver A. Connect to the gate of the A channel FET or IGBT.
OUTB	10	O	Output of driver B. Connect to the gate of the B channel FET or IGBT.
VCCI	3	P	Primary-side supply voltage. Locally decoupled to GND using a low ESR/ESL capacitor located as close to the device as possible
VCCI	8	P	This pin is internally shorted to pin 3.
VDDA	16	P	Secondary-side power for driver A. Locally decoupled to VSSA using a low ESR/ESL capacitor located as close to the device as possible
VDDB	11	P	Secondary-side power for driver B. Locally decoupled to VSSB using a low ESR/ESL capacitor located as close to the device as possible.
VSSA	14	P	Ground for secondary-side driver A. Ground reference for secondary side A channel
VSSB	9	P	Ground for secondary-side driver B. Ground reference for secondary side B channel

(1) P = power, I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VCCI to GND	Input bias supply voltage	–0.3	6	V
VDDA, VDDB to VSS	Output bias supply voltage	–0.3	30	V
OUTA to VSSA, OUTB to VSSB	Output signal DC voltage	–0.3	VDDA/B + 0.3	V
	Output signal transient voltage for 200-ns	–2	VDDA/B + 0.3	V
INA, INB to GND	Input signal DC voltage	–0.3	VCCI + 0.3(2)	V
DT, DIS to GND		–0.3	VCCI + 0.3(2)	V
Channel to channel isolation voltage	|VSSA-VSSB| in D package		1500	V
T_J	Junction temperature	–40	150	℃
T_{stg}	Storage temperature	–65	150	℃

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime
(2) Maximum voltage must not exceed 6 V.

5.2 ESD Ratings (Automotive)

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CCI}	Input bias pin supply voltage	3.0		5.5	V
VDDA, VDDB	UCC21222-Q1 - 8V UVLO Output bias supply voltage, VDDA-VSSA, VDDB-VDDB	9.2		25	V
T_J	Junction temperature	–40		150	℃

5.4 Thermal Information

THERMAL METRIC(1)		UCC21222 D 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	80.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45	°C/W
Ψ_{JT}	Junction-to-top(center) characterization parameter	28	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	44.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)	VCCI = 5V, VDDA/VDDB = 20V, INA/B = 3.3V, 460kHz 50% duty cycle square wave, C_L=2.2nF, T_J=150℃, T_A=25℃			950	mW
P_{DI}	Maximum power dissipation by transmitter side				50	mW
P_{DA}, P_{DB}	Maximum power dissipation by each driver side				450	mW

5.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
General				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	>4	mm
CPG	External Creepage(1)	Shortest terminal-to-terminal distance across the package surface	>4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>17	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 400	V
	Material Group	According to IEC 60664-1	II	
	Overvoltage category	Rated mains voltage ≤ 150 V_{RMS}	I-III	
		Rated mains voltage ≤ 300 V_{RMS}	I-II	
DIN EN IEC 60747-17 (VDE 0884-17)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1200	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test; see Figure 6-1	850	V_{RMS}
		DC voltage	1200	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification) $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production)	4242	V_{PK}
V_{IMP}	Maximum inpulse voltage	Tested in air, 1.2/50-µs waveform per IEC 62368-1	5000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(2)	$V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	6500	V_{PK}
q_{pd}	Apparent charge(3)	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.3 \times V_{IORM}$, t_m = 10 s	≤5	
		Method b1: At routine test (100% production) and preconditioning (type test), $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.5 \times V_{IORM}$, t_m = 1 s	≤5	
C_{IO}	Barrier capacitance, input to output(4)	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	~1.2	pF
R_{IO}	Insulation resistance, input to output(4)	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage for UCC2155x	$V_{TEST} = V_{ISO}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	3000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed-circuit board are used to help increase these specifications.
(2) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(3) Apparent charge is electrical discharge caused by a partial discharge (pd).
(4) All pins on each side of the barrier tied together creating a two-pin device.

5.7 Safety Limiting Values

PARAMETER		TEST CONDITIONS	SIDE	MIN	TYP	MAX	UNIT
I_S	Safety output supply current	$R_{\theta JA}$ = 80.2°C/W, $V_{DDA/B}$ = 15 V, T_J = 150°C, T_A = 25°C	DRIVER A, DRIVER B			50	mA
		$R_{\theta JA}$ = 80.2°C/W, $V_{DDA/B}$ = 25 V, T_J = 150°C, T_A = 25°C				30	
P_S	Safety supply power	$R_{\theta JA}$ = 80.2°C/W, T_J = 150°C, T_A = 25°C	INPUT			50	mW
			DRIVER A			750	
			DRIVER B			750	
			TOTAL			1550	
T_S	Maximum safety temperature(1)					150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J , specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A. The junction-to-air thermal resistance, R_{qJA}, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter: $T_J = T_A + R_{qJA} \times P$, where P is the power dissipated in the device. $T_{J(max)} = T_S = T_A + R_{qJA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature. $P_S = I_S \times V_I$, where VI is the maximum supply voltage.

5.8 Electrical Characteristics

V_{VCCI} = 3.3 V or 5.0 V, 0.1-µF capacitance from VCCI to GND, V_{VDDx} = 12V (for 8V UVLO), , 1-µF + 100-nF capacitance from VDDA and VDDB to VSSA and VSSB, DT pin floating, EN = VCC or DIS = GND, T_J = –40°C to +150°C, C_L = 0 pF, unless otherwise noted (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS						
I_{VCC}	VCC quiescent current	V_{INx} = 0 V, EN = VCC; VCC=3.3V		1.4	2	mA
		V_{INx} = 0 V, EN = VCC; VCC=5V		1.4	2	
		V_{INx} = VCC, EN = VCC; VCC=3.3V		4.2	4.8	
		V_{INx} = VCC, EN = VCC; VCC=5V		4.2	4.8	
		V_{INx} PWM at 0V to VCC at f_{SW} = 500kHz, EN = VCC; VCC=3.3V		2.7	3.2	
		V_{INx} PWM at 0V to VCC at f_{SW} = 500kHz, EN = VCC; VCC=5V		2.7	3.2	
I_{VDDx}	VDDx quiescent current	V_{INx} = 0 V, EN = VCC;		1.2	2	mA
		V_{INx} = 0 V, EN = VCC;VDD=25V		1.4	2.3	
		V_{INx} = VCC, EN = VCC;		1.4	2.2	
		V_{INx} = VCC, EN = VCC; VDD=25V		1.5	2.5	
		V_{INx} PWM at 0V to VCC at f_{SW} = 500kHz, EN = VCC;		2.7	4.4	
		V_{INx} PWM at 0V to VCC at f_{SW} = 500kHz, EN = VCC; VDD=25V		2.7	4.4	
VCC SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLDS						
V_{VCC_ON}	VCC UVLO Rising Threshold		2.55	2.7	2.85	V
V_{VCC_OFF}	VCC UVLO Falling Threshold		2.35	2.5	2.65	
V_{VCC_HYS}	VCC UVLO Threshold Hysteresis			0.2		
$t_{VCC+\ to\ OUT}$	VCC UVLO ON Delay		18	42	80	µs
$t_{VCC-\ to\ OUT}$	VCC UVLO OFF Delay		0.5	1.2	7	
t_{VCCFIL}	VCC UVLO Deglitch Filter		0.4	0.9	3.1	
VDD SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLDS AND DELAY						
V_{VDD_ON}	VDDx UVLO Rising Threshold	8-V UVLO Option	7.7	8.5	8.9	V
V_{VDD_OFF}	VDDx UVLO Falling Threshold		7.2	7.9	8.4	
V_{VDD_HYS}	VDDx UVLO Threshold Hysteresis			0.6		
$t_{VDD+\ to\ OUT}$	VDDx UVLO ON Delay				10	µs
$t_{VDD-\ to\ OUT}$	VDDx UVLO OFF Delay		0.1	0.5	2	
t_{VDDFIL}	VDDx UVLO Deglitch Filter		0.1	0.17		
INA, INB, AND / DIS						
V_{INx_H}, V_{DIS_H} ,	Input High Threshold Voltage			2	2.3	V
V_{INx_L}, V_{DIS_L} ,	Input Low Threshold Voltage		0.8	1		
V_{INx_HYS}, V_{DIS_HYS} ,	Input Threshold Hysteresis			1		
R_{INxD}	INx Pin Pull Down Resistance	INx = 3.3V	50	90	185	kΩ
R_{DISD}	DIS Pin Pull Up Resistance	DIS= 3.3V	50	90	185	kΩ
OUTPUT DRIVER STAGE						
I_{O+}	Peak Output Source Current	C_{VDDx} = 10 µF, C_L = 0.22 µF, f = 1 kHz		–4		A
I_{O-}	Peak Output Sink Current	C_{VDDx} = 10 µF, C_L = 0.22 µF, f = 1 kHz		6		A
R_{OH}	Pull up resistance. R_{OH} does not represent drive pull-up performance. See Section 8.3.4 for details.	I_{OUTx} = –0.05A		5		Ω
R_{OL}	Pull down resistance	I_{OUTx} = 0.05A		0.55		
ACTIVE PULL-DOWN						
V_{OUTPD}	Output Active Pull Down on OUTx	I_{OUT} = 200mA, VDDx floating and unpowered.		1.6	2	V

5.8 Electrical Characteristics (続き)

V_{VCCI} = 3.3 V or 5.0 V, 0.1-µF capacitance from VCCI to GND, V_{VDDx} = 12V (for 8V UVLO), , 1-µF + 100-nF capacitance from VDDA and VDDB to VSSA and VSSB, DT pin floating, EN = VCC or DIS = GND, T_J = –40°C to +150°C, C_L = 0 pF, unless otherwise noted (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUTPD}	Output Active Pull Down on OUTx	I_{OUT} = 200mA, C_{VDD}=100nF and unpowered.		1.6	2	V
DEADTIME AND OVERLAP PROGRAMMING						
DT_S	Disable DT Function	DT pin open or pull DT pin to VCC	Output overlapping determined by INA, INB			-
	Deadtime Programming for R_{DT}≤0.15kΩ	R_{DT}=0~0.15kΩ	-6	0.2	6	ns
	Deadtime Programming for 1.7kΩ≤R_{DT}≤100kΩ DT (ns) = 8.6×R_{DT}(kΩ) + 13	R_{DT} = 10 kΩ	86	99	112	ns
		R_{DT} = 20 kΩ	167	185	203	
		R_{DT} = 50 kΩ	399	443	487	

(1) Current direction in the testing conditions are defined to be positive into the pin and negative out of the specified terminal (unless otherwise noted)

5.9 Switching Characteristics

V_{VCCI} = 3.3 V or 5.0 V, 0.1-µF capacitance from VCCI to GND, V_{VDDx} = 12V (for 5V and 8V UVLO) , 1-µF+100-nF capacitance from VDDA and VDDB to VSSA and VSSB, DT pin floating, EN = VCC or DIS = GND, T_J = –40°C to +150°C, C_L = 0 pF, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RISE}	Output Rise Time	C_L=1.8nF, VDDx=12V, 20% to 80%		8		ns
		C_L=1.8nF, VDDx=25V, 20% to 80%		8		
t_{FALL}	Output Fall Time	C_L=1.8nF, VDDx=12V, 10% to 90%		8		ns
		C_L=1.8nF, VDDx=25V, 10% to 90%		8		
t_{PDLH}	Propagation Delay – Low to High	Input Pulse Width = 100ns, 500kHz, measure with Input VIH to output 10%	26	33	45	ns
t_{PDHL}	Propagation Delay – High to Low	Input Pulse Width = 100ns, 500kHz, measure with Input VIL to output 90%	26	33	45	ns
$t_{PD\_DIS\_HL}$	DIS Response Delay – High to Low	t_{EN/DIS_FIL} = 20 ns (typ), VDD=VDD_ON+0.2V and above, Input Pulse Width = 100ns, 500kHz	27	49	80	ns
$t_{PD\_DIS\_LH}$	DIS Response Delay – Low to High		27	49	80	ns
t_{PWmin}	Minimum Input Pulse Width That Passes to Output	VDD=VDD_ON+0.2V and above	4	12	30	ns
t_{DM}	Propagation Delay Matching for Dual Channel Driver	Input Pulse Width = 100ns, 500kHz, T_J = -40°C to -10°C $\lvert t_{PDLHA} - t_{PDLHB}\rvert$, $\lvert t_{PDHLA} - t_{PDHLB}\rvert$	0		6.5	ns
t_{DM}	Propagation Delay Matching for Dual Channel Driver	Input Pulse Width = 100ns, 500kHz, T_J = -10°C to +150°C $\lvert t_{PDLHA} - t_{PDLHB}\rvert$, $\lvert t_{PDHLA} - t_{PDHLB}\rvert$	0		5	ns
t_{PWD}	Pulse Width Distortion	Input Pulse Width = 100ns, 500kHz $\lvert t_{PDLHA} - t_{PDHLA}\rvert$, $\lvert t_{PDLHB} - t_{PDHLB}\rvert$	0		5	ns
$\lvert CM_H\rvert$	High-level Common Mode Transient Immunity	V_{CM} = 1500V	125			V/ns
$\lvert CM_L\rvert$	Low-level Common Mode Transient Immunity		125			V/ns

5.10 Insulation Characteristics Curves

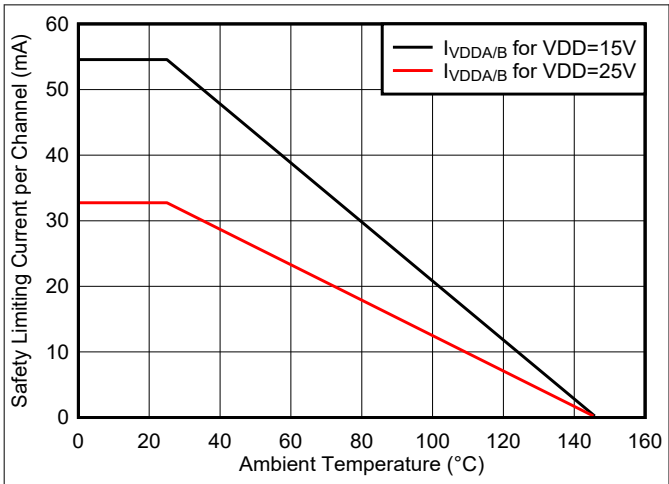


図 5-1. Thermal Derating Curve for Limiting Current per VDE (current in each channel with both channels running simultaneously)

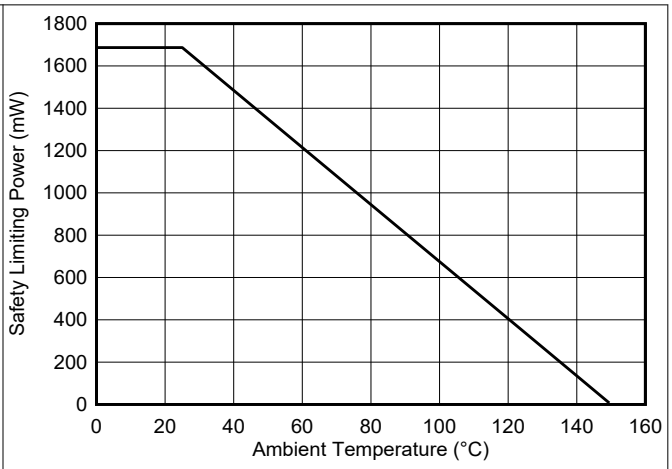


図 5-2. Thermal Derating Curve for Safety-Related Limiting Power per VDE

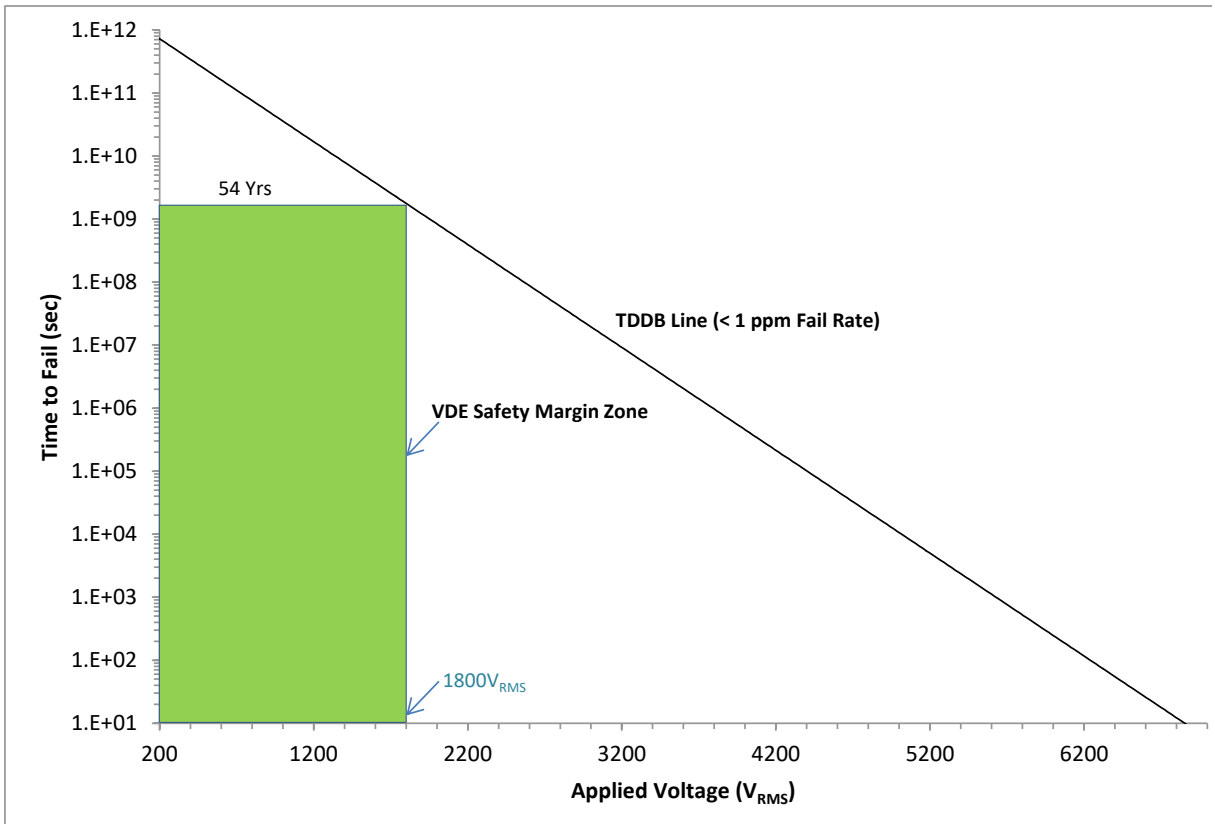


図 5-3. Reinforced Isolation Capacitor Life Time Projection

5.11 Typical Characteristics

VDDA = VDDB= 15 V, VCCI = 3.3 V, T_A = 25°C, No load unless otherwise noted.

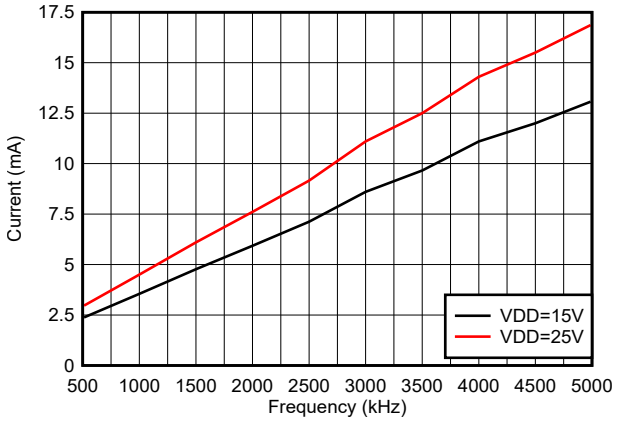


図 5-4. Per Channel Current Consumption ($I_{VDDA/B}$) vs Frequency (no load, VDD = 15V or 25V)

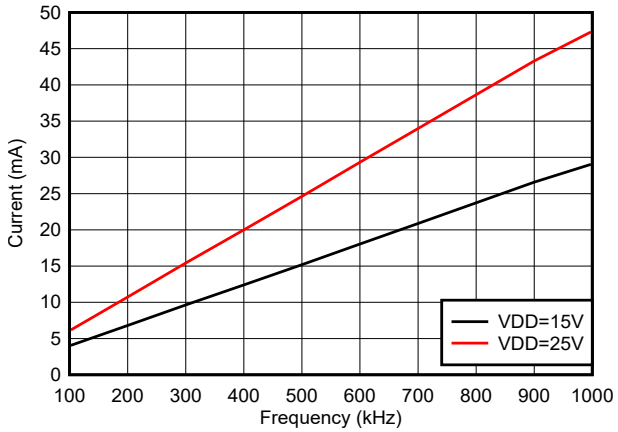


図 5-5. Per Channel Current Consumption ($I_{VDDA/B}$) vs Frequency (1-nF load, VDD = 15V or 25V)

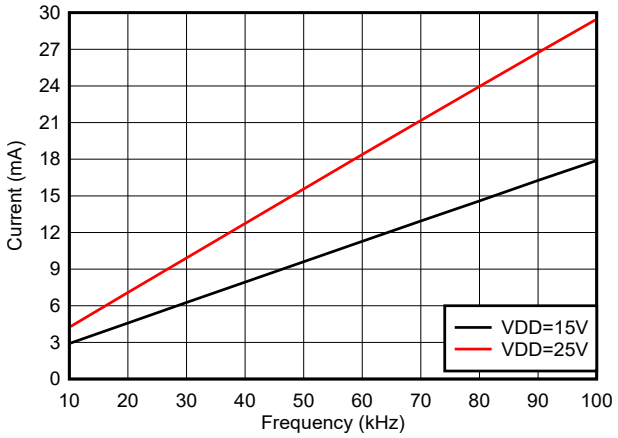


図 5-6. Per Channel Current Consumption ($I_{VDDA/B}$) vs Frequency (10-nF load, VDD = 15V or 25V)

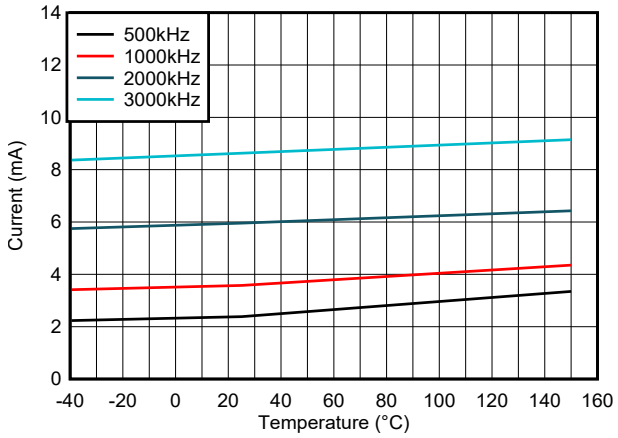


図 5-7. Per Channel ($I_{VDDA/B}$) Supply Current vs Temperature (no load, different switching frequencies)

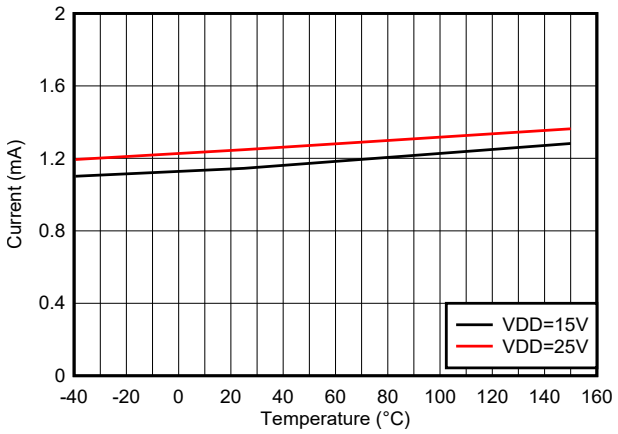


図 5-8. Per Channel ($I_{VDDA/B}$) Quiescent Supply Current vs Temperature (no load, input low, no switching)

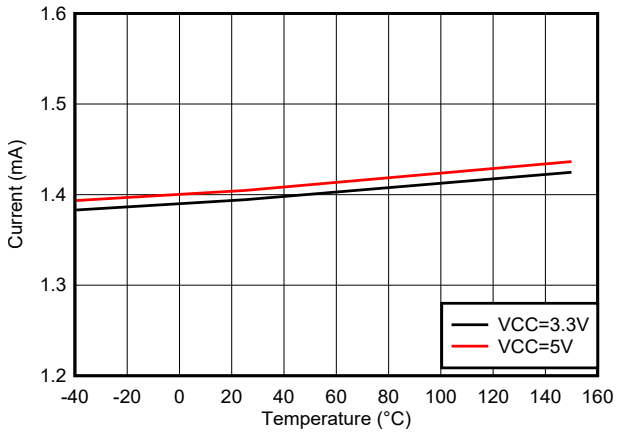


図 5-9. I_{VCCI} Quiescent Supply Current vs Temperature (no load, input low, no switching)

5.11 Typical Characteristics (continued)

VDDA = VDDB= 15 V, VCCI = 3.3 V, T_A = 25°C, No load unless otherwise noted.

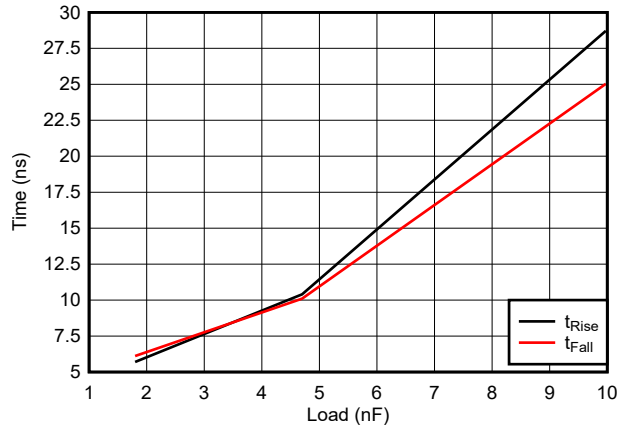


図 5-10. Rising and Falling Times vs Load (VDD = 15V)

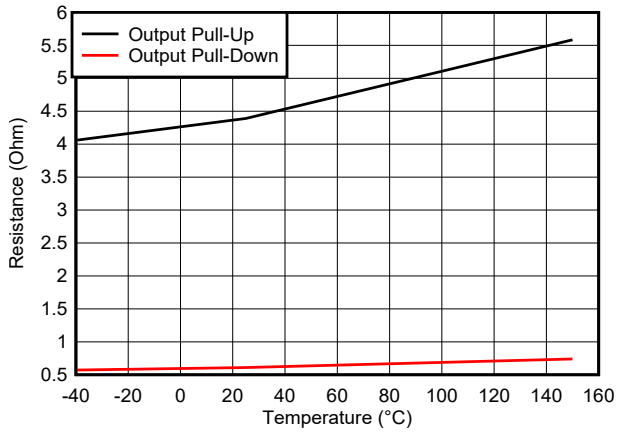


図 5-11. Output Resistance vs Temperature

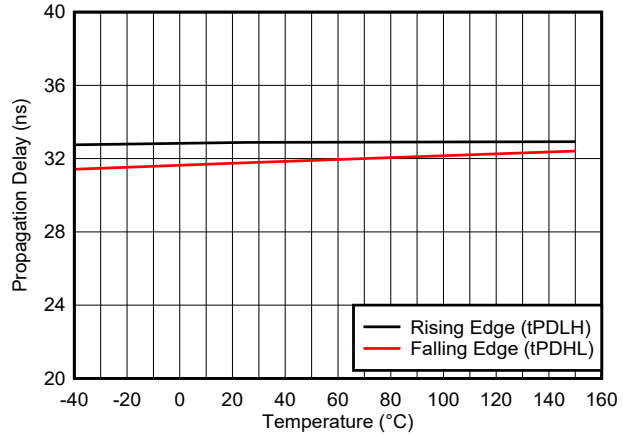


図 5-12. Propagation Delay vs Temperature

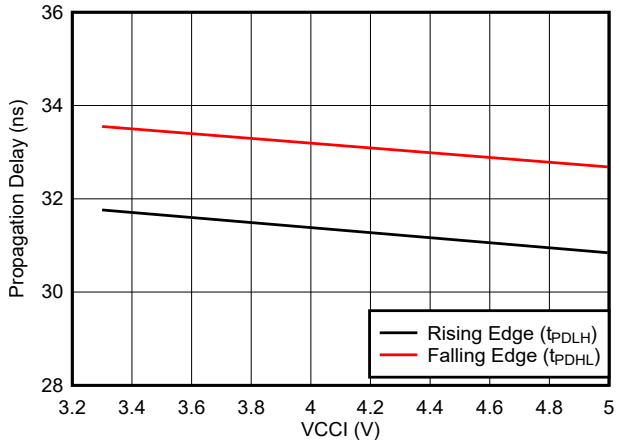


図 5-13. Propagation Delay vs VCCI

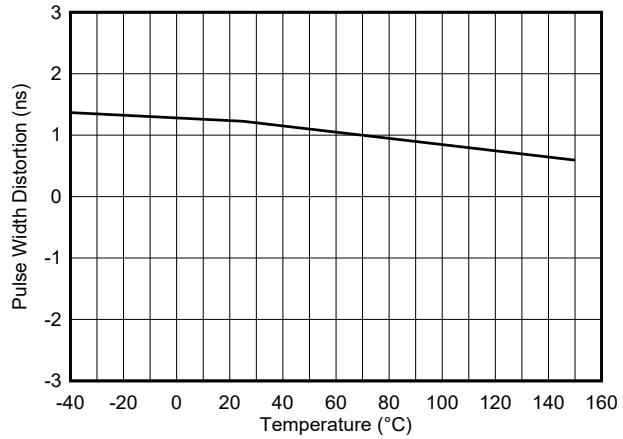


図 5-14. Pulse Width Distortion vs Temperature

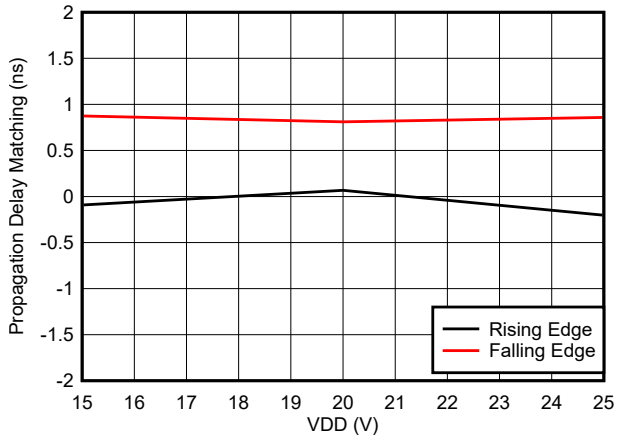


図 5-15. Propagation Delay Matching (t_{DM}) vs VDD

5.11 Typical Characteristics (continued)

VDDA = VDDB= 15 V, VCCI = 3.3 V, T_A = 25°C, No load unless otherwise noted.

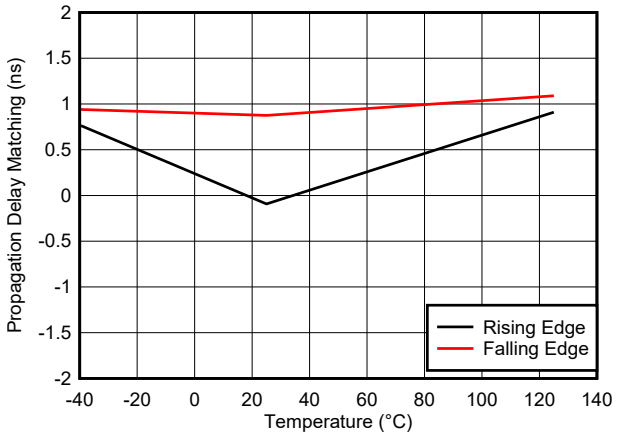


図 5-16. Propagation Delay Matching (t_{DM}) vs Temperature

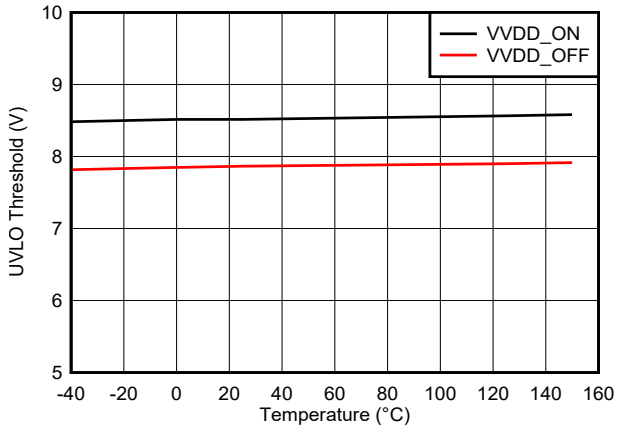


図 5-17. VDD 8-V UVLO Threshold vs Temperature

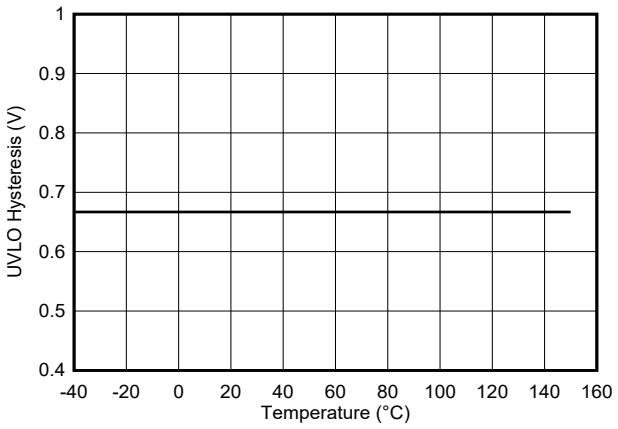


図 5-18. VDD 8-V UVLO Hysteresis vs Temperature

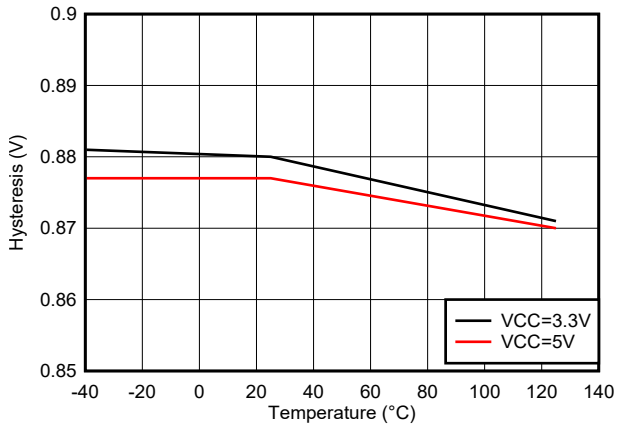


図 5-19. IN/EN Hysteresis vs Temperature

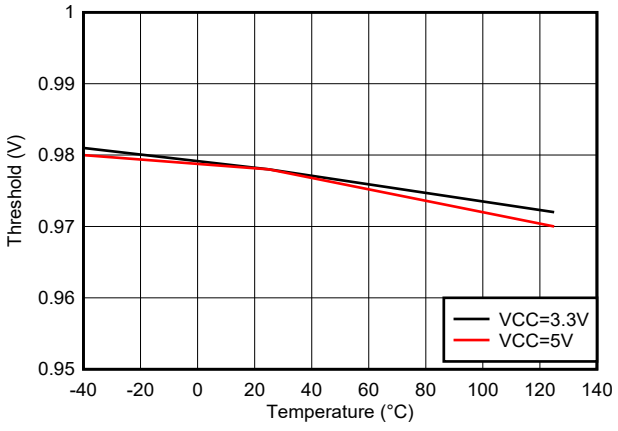


図 5-20. IN/EN Low Threshold

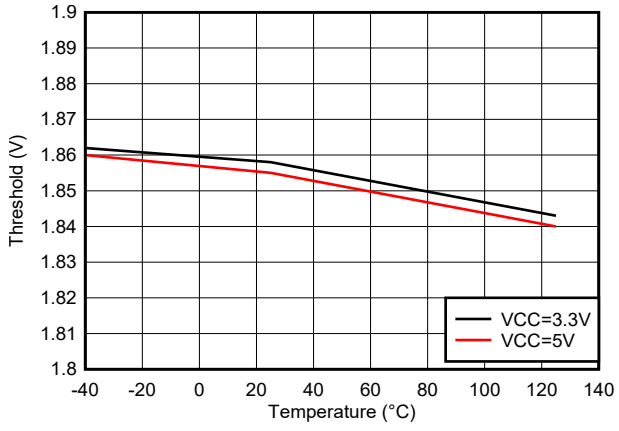


図 5-21. IN/EN High Threshold

5.11 Typical Characteristics (continued)

VDDA = VDDB= 15 V, VCCI = 3.3 V, T_A = 25°C, No load unless otherwise noted.

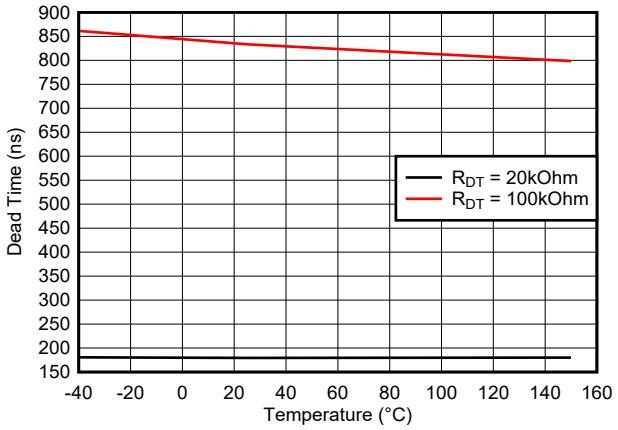


図 5-22. Dead Time vs Temperature (with R_{DT} = 20kΩ and 100kΩ)

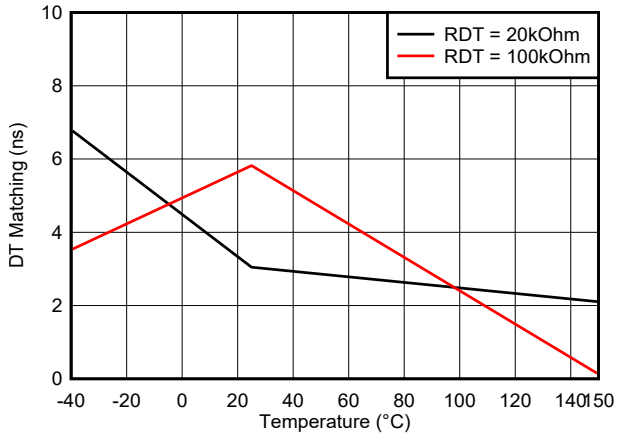


図 5-23. Dead Time Matching vs Temperature (with R_{DT} = 20kΩ and 100kΩ)

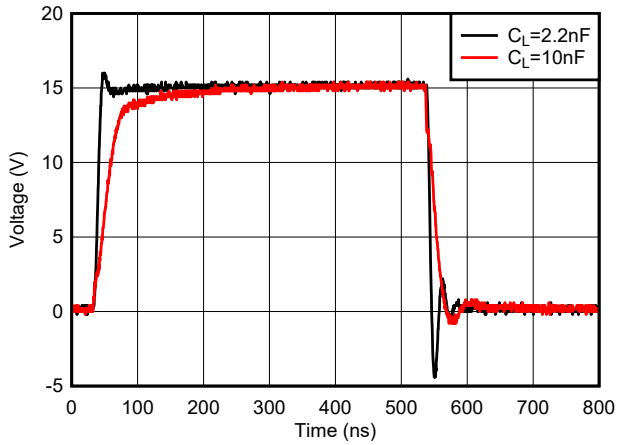


図 5-24. Typical Output Waveforms

6 Parameter Measurement Information

6.1 Minimum Pulses

A typical 5-ns deglitch filter removes small input pulses introduced by ground bounce or switching transients. An input pulse with duration longer than t_{PWmin}, typically 10 ns, must be asserted on INA or INB to guarantee an output state change at OUTA or OUTB. See 図 6-1 and 図 6-2 for detailed information of the operation of deglitch filter.

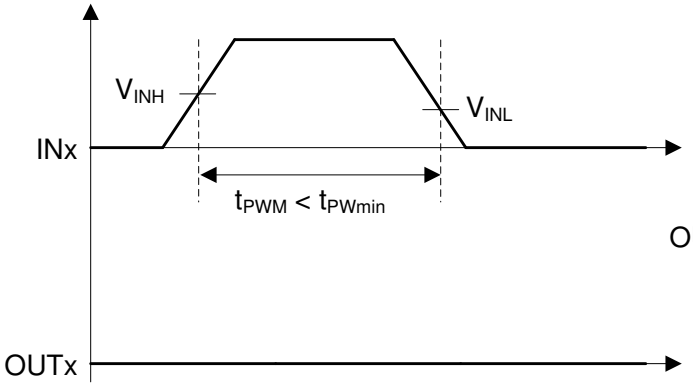


図 6-1. Deglitch Filter – Turn ON

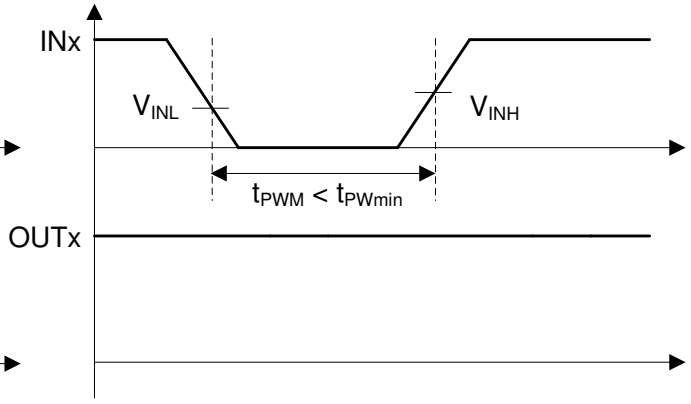


図 6-2. Deglitch Filter – Turn OFF

6.2 Propagation Delay and Pulse Width Distortion

図 6-3 shows calculation of pulse width distortion (t_{PWD}) and delay matching (t_{DM}) from the propagation delays of channels A and B. To measure delay matching, both inputs must be in phase, and the DT pin must be shorted to VCCI to enable output overlap.

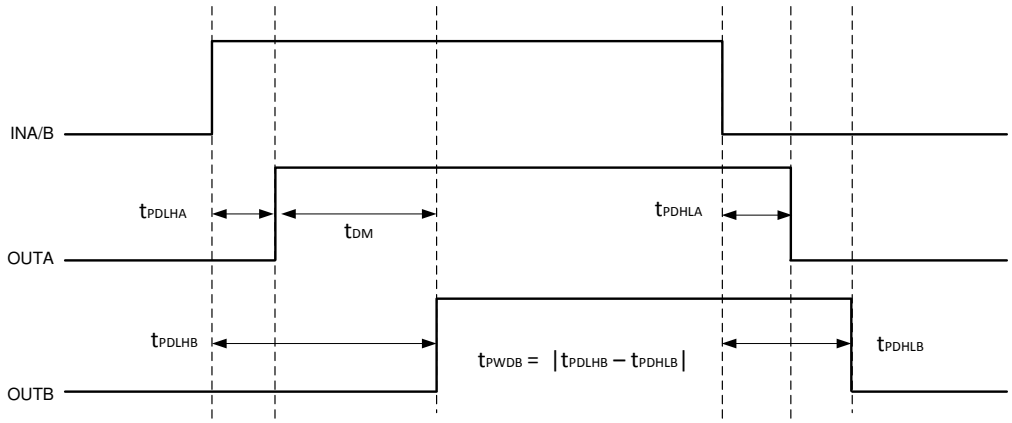


図 6-3. Delay Matching and Pulse Width Distortion

6.3 Rising and Falling Time

図 6-4 shows the criteria for measuring rising (t_{RISE}) and falling (t_{FALL}) times. For more information on how short rising and falling times are achieved see セクション 7.3.4.

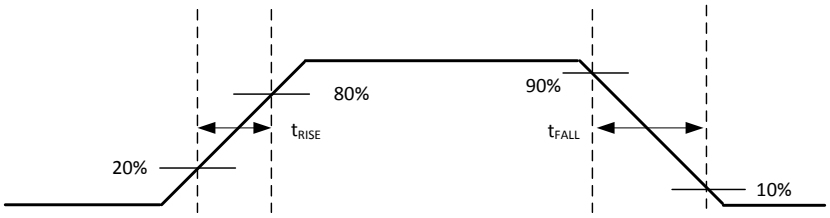


図 6-4. Rising and Falling Time Criteria

6.4 Input and Disable Response Time

図 6-5 shows the response time of the disable function. For more information, see セクション 7.4.1.

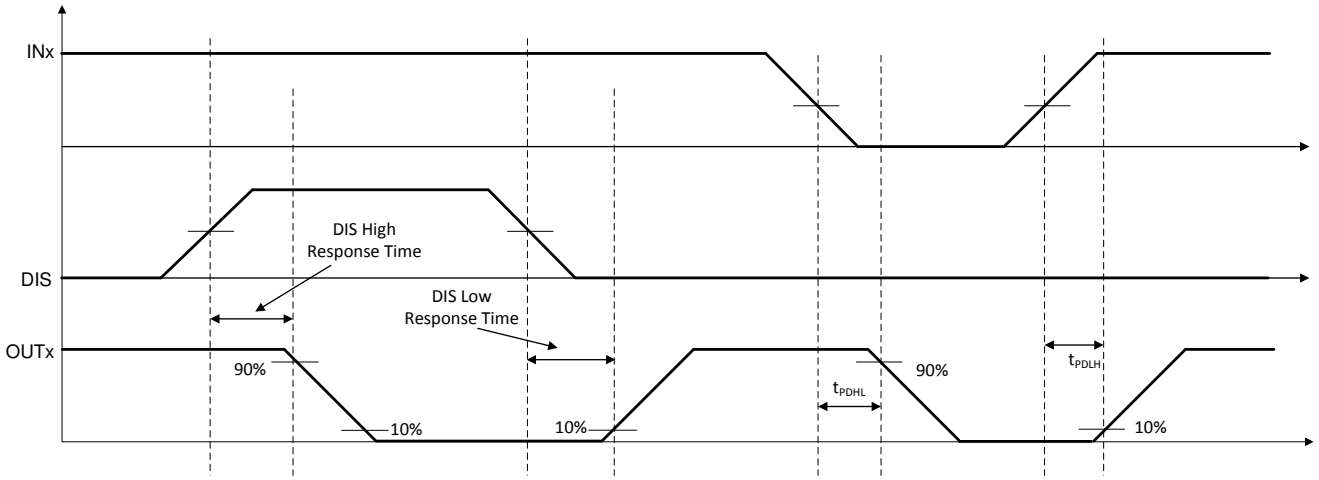


図 6-5. Disable Pin Timing

6.5 Programmable Dead Time

Connecting the DT pin to GND through an appropriate resistor (R_{DT}) sets a dead-time interval. For more details on dead time, refer to セクション 7.4.2.

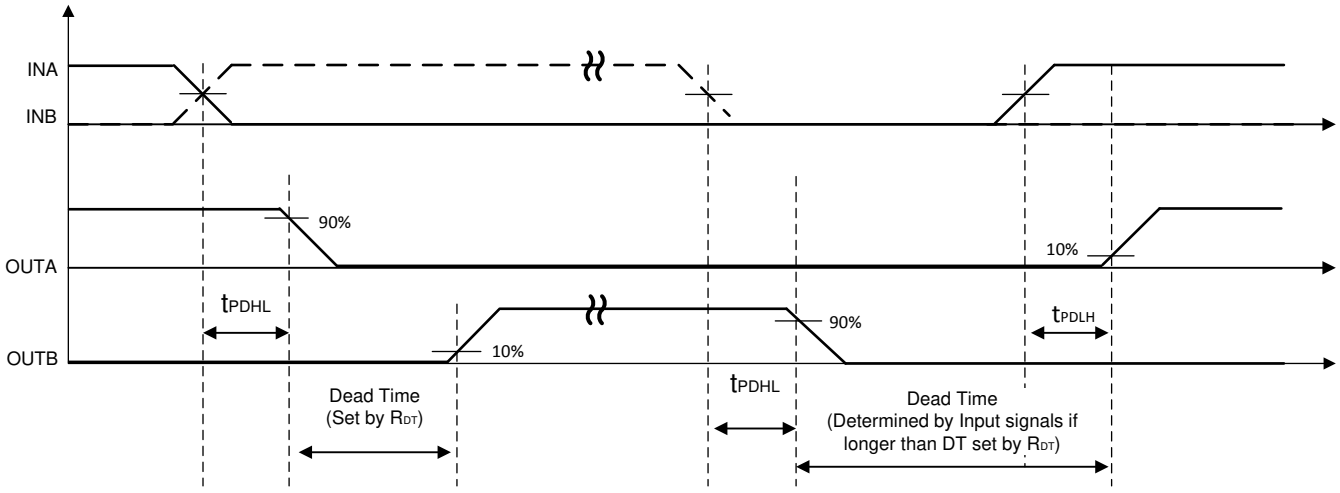


図 6-6. Dead Time Switching Parameters

6.6 Power-Up UVLO Delay to OUTPUT

Before the driver is ready to deliver a proper output state, there is a power-up delay from the UVLO rising edge to output and it is defined as $t_{VCCI+\ to\ OUT}$ for VCCI UVLO (typically 40us) and $t_{VDD+\ to\ OUT}$ for VDD UVLO (typically 5us). It is recommended to consider proper margin before launching PWM signal after the driver's VCCI and VDD bias supply is ready. 図 6-7 and 図 6-8 show the power-up UVLO delay timing diagram for VCCI and VDD.

If INA or INB are active before VCCI or VDD have crossed above their respective on thresholds, the output will not update until $t_{VCCI+\ to\ OUT}$ or $t_{VDDx+\ to\ OUT}$ after VCCI or VDD crossing its UVLO rising threshold. However, when either VCCI or VDD receive a voltage less than their respective off thresholds, there is <2µs delay, depending on the voltage slew rate on the supply pins, before the outputs are held low. This asymmetric delay is designed to ensure safe operation during VCCI or VDD brownouts.

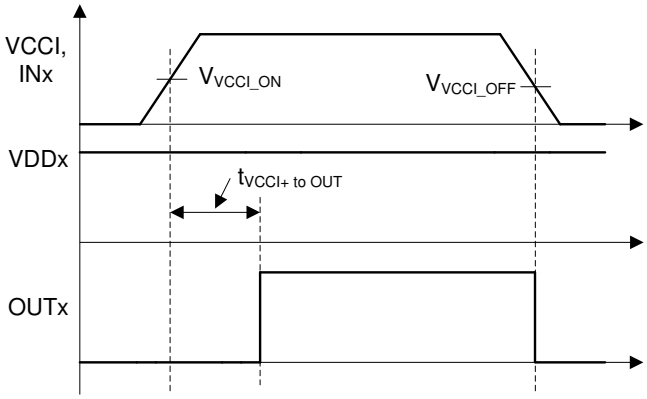


図 6-7. VCCI Power-Up UVLO Delay

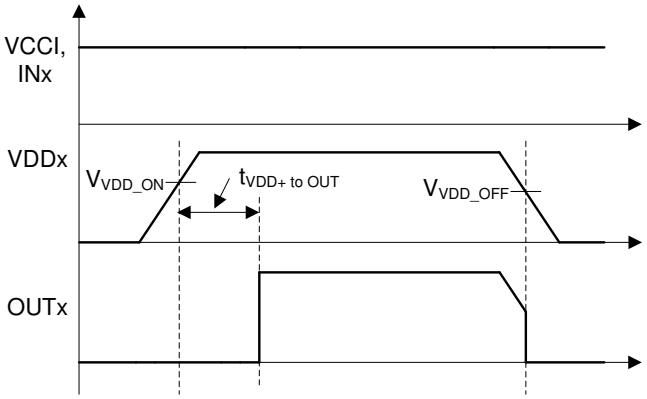


図 6-8. VDDA/B Power-Up UVLO Delay

6.7 CMTI Testing

図 6-9 is a simplified diagram of the CMTI testing configuration.

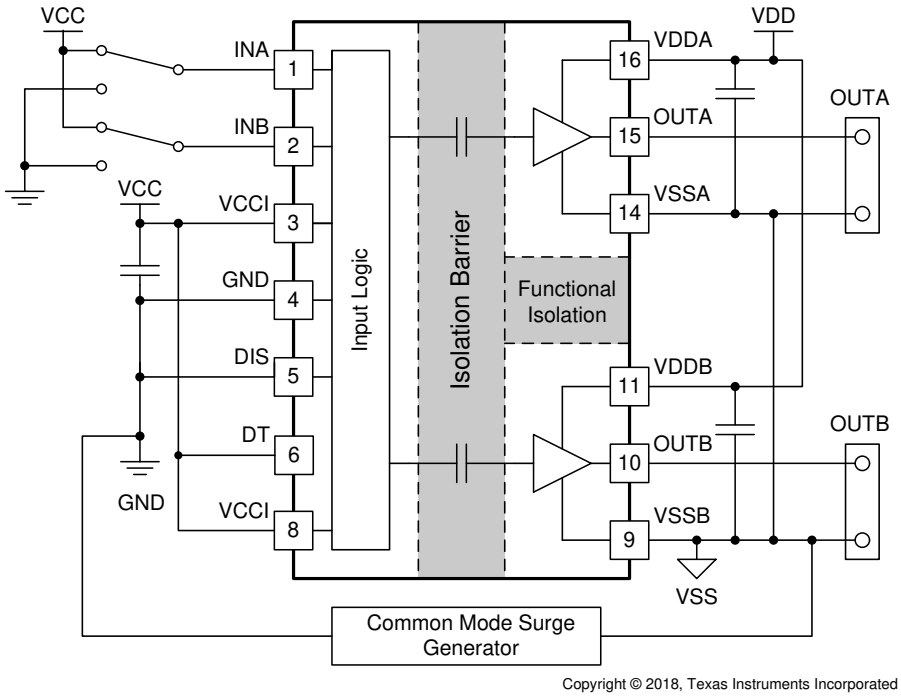


図 6-9. Simplified CMTI Testing Setup

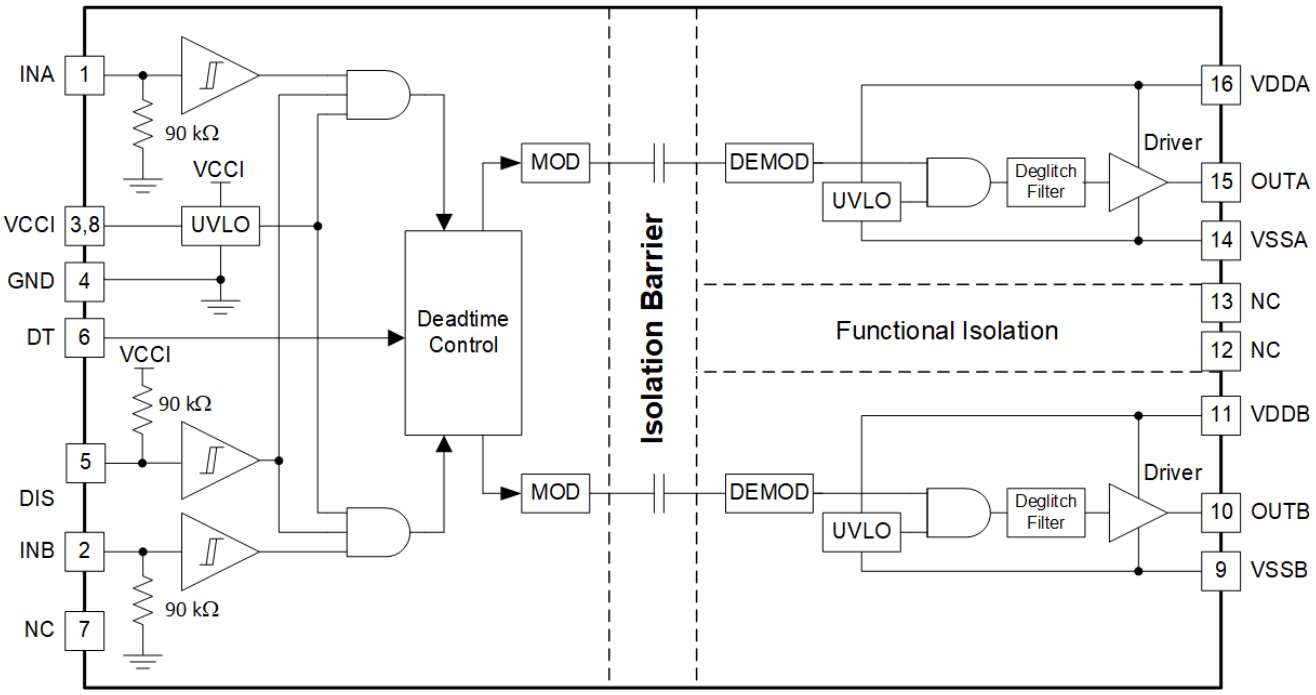
7 Detailed Description

7.1 Overview

In order to switch power transistors rapidly and reduce switching power losses, high-current gate drivers are often placed between the output of control devices and the gates of power transistors. There are several instances where controllers are not capable of delivering sufficient current to drive the gates of power transistors. This is especially the case with digital controllers, since the input signal from the digital controller is often a 3.3-V logic signal capable of only delivering a few mA.

The UCC21222-Q1 is a flexible dual gate driver which can be configured to fit a variety of power supply and motor drive topologies, as well as drive several types of transistors. The UCC21222-Q1 has many features that allow it to integrate well with control circuitry and protect the gates it drives such as: resistor-programmable dead time (DT) control, disable pin, and under voltage lock out (UVLO) for both input and output supplies. The UCC21222-Q1 also holds its outputs low when the inputs are left open or when the input pulse duration is too short. The driver inputs are CMOS and TTL compatible for interfacing with digital and analog power controllers alike. Each channel is controlled by its respective input pins (INA and INB), allowing full and independent control of each of the outputs.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 VDD, VCCI, and Undervoltage Lock Out (UVLO)

The UCC21222-Q1 has an internal under voltage lock out (UVLO) protection feature on each supply voltage between the VDD and VSS pins for both outputs. When the VDD bias voltage is lower than V_{VDD_ON} at device start-up or lower than V_{VDD_OFF} after start-up, the VDD UVLO feature holds the channel output low, regardless of the status of the input pins.

When the output stages of the driver are in an unbiased or UVLO condition, the driver outputs are held low by an active clamp circuit that limits the voltage rise on the driver outputs (illustrated in 図 7-1). In this condition, the upper PMOS is resistively held off by R_{Hi-Z} while the lower NMOS gate is tied to the driver output through R_{CLAMP}. In this configuration, the output is effectively clamped to the threshold voltage of the lower NMOS device, typically around 1.5V, regardless of whether bias power is available.

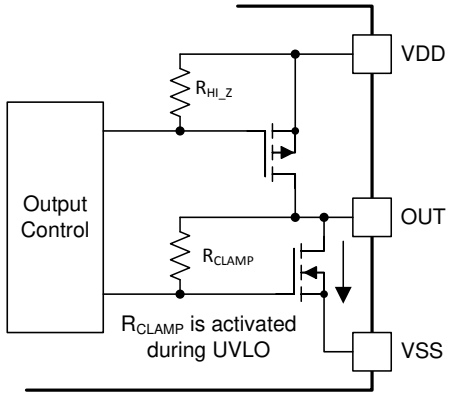


図 7-1. Simplified Representation of Active Pull Down Feature

The VDD UVLO protection has a hysteresis feature (V_{VDD_HYS}). This hysteresis prevents chatter when there is ground noise from the power supply. This also allows the device to accept small drops in bias voltage, which commonly occurs when the device starts switching and operating current consumption increases suddenly.

The inputs of the UCC21222-Q1 also have an internal under voltage lock out (UVLO) protection feature. The inputs cannot affect the outputs unless the supply voltage VCCI exceeds V_{VCCI_ON} on start-up. The outputs are held low and cannot respond to inputs when the supply voltage VCCI drops below V_{VCCI_OFF} after start-up. Like the UVLO for VDD, there is hystersis (V_{VCCI_HYS}) to ensure stable operation.

表 7-1. VCCI UVLO Feature Logic

CONDITION	INPUTS		OUTPUTS	
	INA	INB	OUTA	OUTB
VCCI-GND < V_{VCCI_ON} during device start up	H	L	L	L
VCCI-GND < V_{VCCI_ON} during device start up	L	H	L	L
VCCI-GND < V_{VCCI_ON} during device start up	H	H	L	L
VCCI-GND < V_{VCCI_ON} during device start up	L	L	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	H	L	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	L	H	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	H	H	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	L	L	L	L

表 7-2. VDD UVLO Feature Logic

CONDITION	INPUTS		OUTPUTS	
	INA	INB	OUTA	OUTB
VDD-VSS < V_{VDD_ON} during device start up	H	L	L	L
VDD-VSS < V_{VDD_ON} during device start up	L	H	L	L
VDD-VSS < V_{VDD_ON} during device start up	H	H	L	L
VDD-VSS < V_{VDD_ON} during device start up	L	L	L	L
VDD-VSS < V_{VDD_OFF} after device start up	H	L	L	L
VDD-VSS < V_{VDD_OFF} after device start up	L	H	L	L
VDD-VSS < V_{VDD_OFF} after device start up	H	H	L	L
VDD-VSS < V_{VDD_OFF} after device start up	L	L	L	L

7.3.2 Input and Output Logic Table

Assume VCCI, VDDA, VDDB are powered up (see セクション 7.3.1 for more information on UVLO operation modes). 表 7-3 shows the operation with INA, INB and DIS and the corresponding output state.

表 7-3. INPUT/OUTPUT Logic Table(1)

INPUTS		DIS	OUTPUTS		NOTE
INA	INB		OUTA	OUTB	
L	L	L	L	L	If the dead time function is used, output transitions occur after the dead time expires. See セクション 7.4.2.
L	H	L	L	H	
H	L	L	H	L	
H	H	L	L	L	DT is programmed with R_{DT}.
H	H	L	H	H	DT pin is left open or pulled to VCCI.
Left Open	Left Open	L	L	L	
X	X	H or Left Open	L	L	

(1) "X" means L, H or left open. For improved noise immunity, TI recommends connecting INA, INB, and DIS to GND, and DT to VCCI, when these pins are not used.

7.3.3 Input Stage

The input pins (INA, INB, and DIS) of the UCC21222-Q1 are based on a TTL and CMOS compatible input-threshold logic that is totally isolated from the VDD supply voltage of the output channels. The input pins are easy to drive with logic-level control signals (such as those from 3.3-V microcontrollers), since the UCC21222-Q1 has a typical high threshold (V_{INAH}) of 2 V and a typical low threshold of 1 V. A wide hysterisis (V_{INA_HYS}) of 1 V makes for good noise immunity and stable operation. If any of the inputs are ever left open, internal pull-down resistors force the pin low. These resistors are typically 90 kΩ (see セクション 7.2). TI recommends grounding any unused inputs.

The amplitude of any signal applied to the inputs must *never* be at a voltage higher than VCCI.

7.3.4 Output Stage

The UCC21222-Q1 output stages feature a pull-up structure which delivers the highest peak-source current when it is most needed, during the Miller plateau region of the power-switch turn on transition (when the power switch drain or collector voltage experiences dV/dt). The output stage pull-up structure features a P-channel MOSFET and an additional *Pull-Up* N-channel MOSFET in parallel. The function of the N-channel MOSFET is to provide a brief boost in the peak-sourcing current, enabling fast turn on. This is accomplished by briefly turning on the N-channel MOSFET during a narrow instant when the output is changing states from low to high.

The R_{OH} parameter is a DC measurement and it is representative of the on-resistance of the P-channel device only. This is because the *Pull-Up* N-channel device is held in the off state in DC condition and is turned on only for a brief instant when the output is changing states from low to high. This N-channel device has an on-resistance of approximately 1.47 Ω. Therefore the effective resistance of the UCC21222-Q1 pull-up stage during this brief turn-on phase is the parallel resistance between the pull-up NMOS and pull-up PMOS, which is 1.47Ω // 5Ω, much lower than what is represented by the R_{OH} parameter. The value of R_{OH} belies the fast nature of the UCC21222-Q1 turn-on time.

The pull-down structure in the UCC21222-Q1 is simply composed of an N-channel MOSFET. The R_{OL} parameter, which is also a DC measurement, is representative of the impedance of the pull-down state in the device. Both outputs of the UCC21222-Q1 are capable of delivering 4-A peak source and 6-A peak sink current pulses. The output voltage swings between VDD and VSS provides rail-to-rail operation, thanks to the MOS-out stage which delivers very low drop-out.

To ensure robust and reliable operation of gate drivers, pay special attention to the minimum pulse width. The minimum pulse width shown in the electrical characteristics table describes the minimum input pulse that would be passed to the output in an unloaded driver. This is dictated by the deglitch filter present in the driver IC. An input ON or OFF pulse width longer than the maximum specification is needed to guarantee an output state change and avoid potential shoot-through. With a loaded driver, extra precaution must be taken to ensure robust operation of the system. During gate switching, if the output state changes before the driver completes each transition, a non-zero current switching event occurs. Combined with layout parasitics, non-zero current switching can cause internal rail overshoot and EOS damage of the gate driver. Thus, a minimum output width is needed for reliable system operation. This minimum output pulse width is dependent on several factors: gate capacitance, VDD supply voltage, gate resistance, and PCB layout parasitics. The minimum pulse width for robust operation might be magnitudes larger than the minimum pulse width shown in the electrical characteristics table. System-level study should be carried out to determine the minimum output pulse width required for each system.

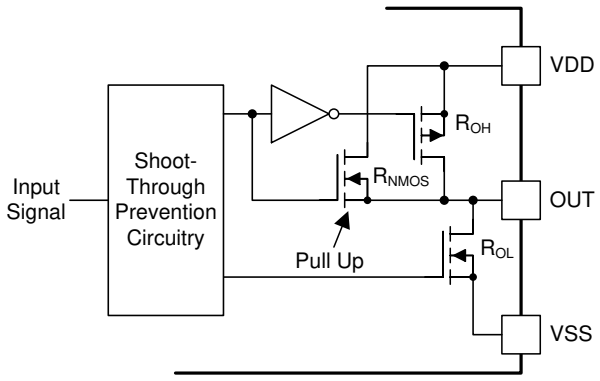


図 7-2. Output Stage

7.3.5 Diode Structure in the UCC21222-Q1

図 7-3 illustrates the multiple diodes involved in the ESD protection components. This provides a pictorial representation of the absolute maximum rating for the device.

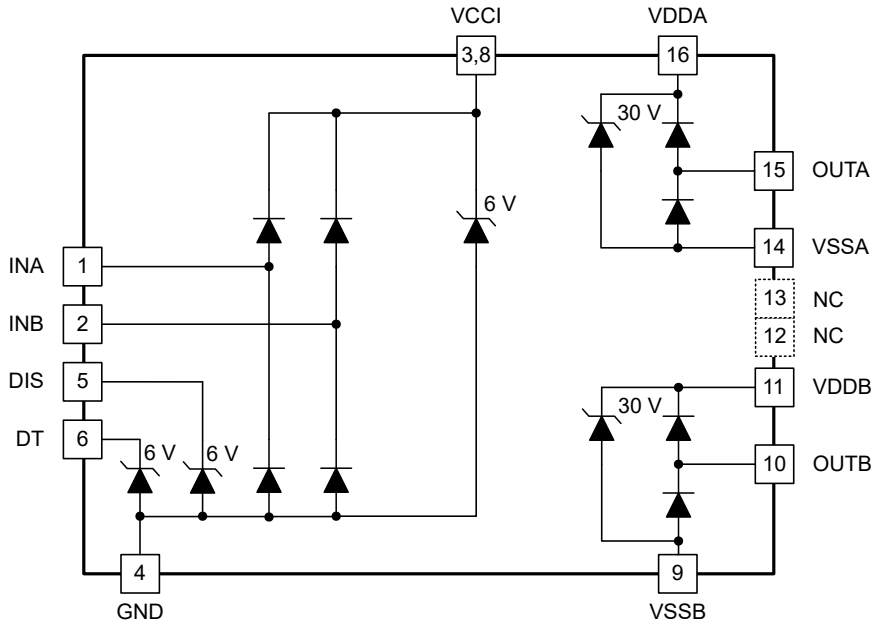


図 7-3. ESD Structure

7.4 Device Functional Modes

7.4.1 Disable Pin

Setting the DIS pin high (or left open) shuts down both outputs simultaneously. Grounding the DIS pin allows the UCC21222-Q1 to operate normally. The DIS response time is in the range of 48 ns and quite responsive, which is as fast as propagation delay. The DIS pin is only functional (and necessary) when VCCI stays above the UVLO threshold. It is recommended to tie this pin to ground if the DIS pin is not used to achieve better noise immunity, and it is recommended to bypass using a ≈1-nF low ESR/ESL capacitor close to DIS pin when connecting DIS pin to a micro controller with distance.

7.4.2 Programmable Dead Time (DT) Pin

The UCC21222-Q1 allows the user to adjust dead time (DT) in the following ways:

7.4.2.1 DT Pin Tied to VCCI or DT Pin Left Open

Outputs completely match inputs, so no minimum dead time is asserted. This allows the outputs to overlap. TI recommends connecting this pin directly to VCCI if it is not used to achieve better noise immunity.

7.4.2.2 Connecting a Programming Resistor between DT and GND Pins

Program t_{DT} by placing a resistor, R_{DT}, between the DT pin and GND. The appropriate R_{DT} value can be determined, where R_{DT} is in kΩ and t_{DT} is in ns:

$$t_{DT} \approx 8.6 \times R_{DT} + 13 \quad (1)$$

where

- t_{DT} is the programmed dead time, in nanoseconds.
- R_{DT} is the value of resistance between DT pin and GND, in kilo-ohms.

t_{DT} is true when R_{DT} is in the range of 1.7 kΩ to 100 kΩ. It is not recommended to use a R_{DT} with value greater than 100 kΩ.

An input signal's falling edge activates the programmed dead time for the other signal. The output signals' dead time is always set to the longer of either the driver's programmed dead time or the input signal's own dead time. If both inputs are high simultaneously, both outputs will immediately be set low. This feature is used to prevent shoot-through, and it does not affect the programmed dead time setting for normal operation. Various driver dead time logic operating conditions are illustrated and explained in 図 7-4.

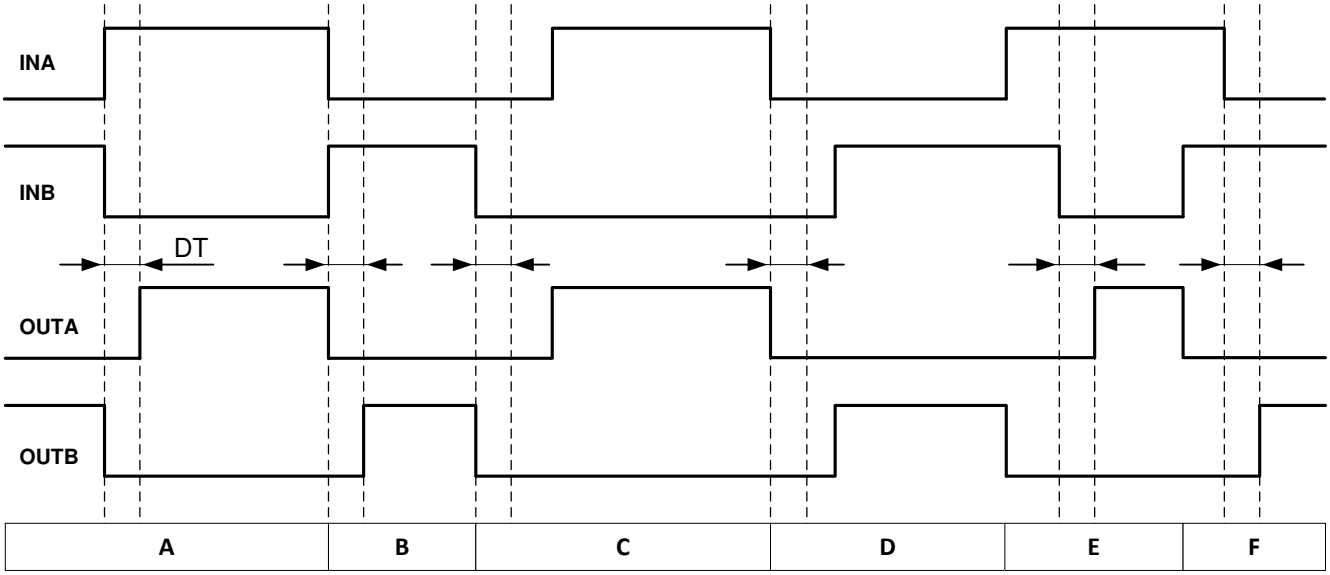


図 7-4. Input and Output Logic Relationship with Input Signals

Condition A: INB goes low, INA goes high. INB sets OUTB low immediately and assigns the programmed dead time to OUTA. OUTA is allowed to go high after the programmed dead time.

Condition B: INB goes high, INA goes low. Now INA sets OUTA low immediately and assigns the programmed dead time to OUTB. OUTB is allowed to go high after the programmed dead time.

Condition C: INB goes low, INA is still low. INB sets OUTB low immediately and assigns the programmed dead time for OUTA. In this case, the input signal dead time is longer than the programmed dead time. When INA goes high after the duration of the input signal dead time, it immediately sets OUTA high.

Condition D: INA goes low, INB is still low. INA sets OUTA low immediately and assigns the programmed dead time to OUTB. In this case, the input signal dead time is longer than the programmed dead time. When INB goes high after the duration of the input signal dead time, it immediately sets OUTB high.

Condition E: INA goes high, while INB and OUTB are still high. To avoid overshoot, OUTB is immediately pulled low. After some time OUTB goes low and assigns the programmed dead time to OUTA. OUTB is already low. After the programmed dead time, OUTA is allowed to go high.

Condition F: INB goes high, while INA and OUTA are still high. To avoid overshoot, OUTA is immediately pulled low. After some time OUTA goes low and assigns the programmed dead time to OUTB. OUTA is already low. After the programmed dead time, OUTB is allowed to go high.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The UCC21222-Q1 effectively combines both isolation and buffer-drive functions. The flexible, universal capability of the UCC21222-Q1 (with up to 5.5-V VCCI and 18-V VDDA/VDDB) allows the device to be used as a low-side, high-side, high-side/low-side or half-bridge driver for MOSFETs, IGBTs or GaN transistor. With integrated components, advanced protection features (UVLO, dead time, and disable) and optimized switching performance, the UCC21222-Q1 enables designers to build smaller, more robust designs for enterprise, telecom, automotive, and industrial applications with a faster time to market.

8.2 Typical Application

The circuit in 図 8-1 shows a reference design with the UCC21222-Q1 driving a typical half-bridge configuration which could be used in several popular power converter topologies such as synchronous buck, synchronous boost, half-bridge/full bridge isolated topologies, and 3-phase motor drive applications.

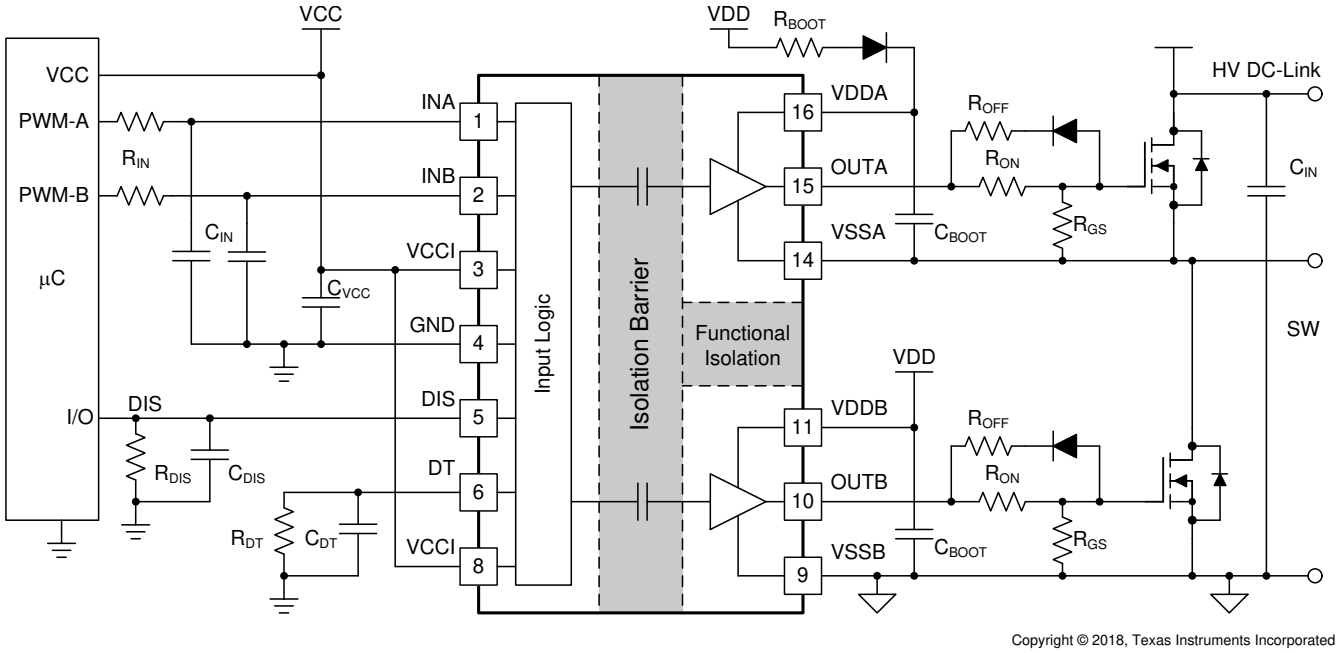


図 8-1. Typical Application Schematic

8.2.1 Design Requirements

表 8-1 lists reference design parameters for the example application: UCC21222-Q1 driving 650-V MOSFETs in a high side-low side configuration.

表 8-1. UCC21222-Q1 Design Requirements

PARAMETER	VALUE	UNITS
Power transistor	650-V, 150-mΩ R_{DS_ON} with 12-V V_{GS}	-
VCC	5.0	V
VDD	12	V
Input signal amplitude	3.3	V
Switching frequency (f_s)	100	kHz
Dead Time	200	ns
DC link voltage	400	V

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the UCC21222-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Designing INA/INB Input Filter

It is recommended that users avoid shaping the signals to the gate driver in an attempt to slow down (or delay) the signal at the output. However, a small input R_{IN}-C_{IN} filter can be used to filter out the ringing introduced by non-ideal layout or long PCB traces.

Such a filter should use an R_{IN} in the range of 0 Ω to 100 Ω and a C_{IN} between 10 pF and 100 pF. In the example, an R_{IN} = 51 Ω and a C_{IN} = 33 pF are selected, with a corner frequency of approximately 100 MHz.

When selecting these components, it is important to pay attention to the trade-off between good noise immunity and propagation delay.

8.2.2.3 Select Dead Time Resistor and Capacitor

From 式 1, a 20-kΩ resistor is selected to set the dead time to 185 ns. A 2.2-nF capacitor is placed in parallel close to the DT pin to improve noise immunity.

8.2.2.4 Select External Bootstrap Diode and its Series Resistor

The bootstrap capacitor is charged by VDD through an external bootstrap diode every cycle when the low side transistor turns on. Charging the capacitor involves high-peak currents, and therefore transient power dissipation in the bootstrap diode may be significant. Conduction loss also depends on the diode's forward voltage drop. Both the diode conduction losses and reverse recovery losses contribute to the total losses in the gate driver circuit.

When selecting external bootstrap diodes, it is recommended that one chose high voltage, fast recovery diodes or SiC Schottky diodes with a low forward voltage drop and low junction capacitance in order to minimize the loss introduced by reverse recovery and related grounding noise bouncing. In the example, the DC-link voltage is 400 V_{DC}. The voltage rating of the bootstrap diode should be higher than the DC-link voltage with a good margin. Therefore, a 600-V ultrafast diode, MURA160T3G, is chosen in this example.

A bootstrap resistor, R_{BOOT}, is used to reduce the inrush current in D_{BOOT} and limit the ramp up slew rate of voltage of VDDA-VSSA during each switching cycle, especially when the VSSA(SW) pin has an excessive negative transient voltage. The recommended value for R_{BOOT} is between 1 Ω and 20 Ω depending on the diode used. In the example, a current limiting resistor of 2.2 Ω is selected to limit the inrush current of bootstrap diode. The estimated worst case peak current through D_{Boot} is,

$$I_{DBoot(pk)} = \frac{V_{DD} - V_{BDF}}{R_{Boot}} = \frac{12V - 1.5V}{2.7\Omega} \approx 4A \tag{2}$$

where

- V_{BDF} is the estimated bootstrap diode forward voltage drop around 4 A.

8.2.2.5 Gate Driver Output Resistor

The external gate driver resistors, R_{ON}/R_{OFF}, are used to:

1. Limit ringing caused by parasitic inductances/capacitances.
2. Limit ringing caused by high voltage/current switching dv/dt, di/dt, and body-diode reverse recovery.
3. Fine-tune gate drive strength; that is, peak sink and source current to optimize the switching loss.
4. Reduce electromagnetic interference (EMI).

As mentioned in セクション 7.3.4, the UCC21222-Q1 has a pullup structure with a P-channel MOSFET and an additional *pull-up* N-channel MOSFET in parallel. The combined peak source current is 4 A. Therefore, the peak source current can be predicted with:

$$I_{OA+} = \min\left(4A, \frac{V_{DD} - V_{BDF}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET\_Int}}\right) \tag{3}$$

$$I_{OB+} = \min\left(4A, \frac{V_{DD}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET\_Int}}\right) \tag{4}$$

where

- R_{ON}: External turn-on resistance.
- R_{GFET_INT}: Power transistor internal gate resistance, found in the power transistor data sheet.
- I_{O+} = Peak source current – The minimum value between 4 A, the gate driver peak source current, and the calculated value based on the gate drive loop resistance.

In this example:

$$I_{OA+} = \frac{V_{DD} - V_{BDF}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET\_Int}} = \frac{12V - 0.8V}{1.47\Omega \,||\, 5\Omega + 2.2\Omega + 1.5\Omega} \approx 2.3A \tag{5}$$

$$I_{OB+} = \frac{V_{DD}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET\_Int}} = \frac{12V}{1.47\Omega \,||\, 5\Omega + 2.2\Omega + 1.5\Omega} \approx 2.5A \quad (6)$$

Therefore, the high-side and low-side peak source current is 2.3 A and 2.5 A respectively. Similarly, the peak sink current can be calculated with:

$$I_{OA-} = \min\left(6A, \frac{V_{DD} - V_{BDF} - V_{GDF}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET\_Int}}\right) \quad (7)$$

$$I_{OB-} = \min\left(6A, \frac{V_{DD} - V_{GDF}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET\_Int}}\right) \quad (8)$$

where

- R_{OFF}: External turn-off resistance, R_{OFF}=0 in this example;
- V_{GDF}: The anti-parallel diode forward voltage drop which is in series with R_{OFF}. The diode in this example is an MSS1P4.
- I_{O-}: Peak sink current – the minimum value between 6 A, the gate driver peak sink current, and the calculated value based on the gate drive loop resistance.

In this example,

$$I_{OA-} = \frac{V_{DD} - V_{BDF} - V_{GDF}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET\_Int}} = \frac{12V - 0.8V - 0.85V}{0.55\Omega + 0\Omega + 1.5\Omega} \approx 5.0A \quad (9)$$

$$I_{OB-} = \frac{V_{DD} - V_{GDF}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET\_Int}} = \frac{12V - 0.85V}{0.55\Omega + 0\Omega + 1.5\Omega} \approx 5.4A \quad (10)$$

Therefore, the high-side and low-side peak sink current is 5.0 A and 5.4 A, respectively.

Importantly, the estimated peak current is also influenced by PCB layout and load capacitance. Parasitic inductance in the gate driver loop can slow down the peak gate drive current and introduce overshoot and undershoot. Therefore, it is strongly recommended that the gate driver loop should be minimized. On the other hand, the peak source/sink current is dominated by loop parasitics when the load capacitance (C_{ISS}) of the power transistor is very small (typically less than 1 nF), because the rising and falling time is too small and close to the parasitic ringing period.

8.2.2.6 Estimating Gate Driver Power Loss

The total loss, P_G, in the gate driver subsystem includes the power losses of the UCC21222-Q1 (P_{GD}) and the power losses in the peripheral circuitry, such as the external gate drive resistor. Bootstrap diode loss is not included in P_G and not discussed in this section.

P_{GD} is the key power loss which determines the thermal safety-related limits of the UCC21222-Q1, and it can be estimated by calculating losses from several components.

The first component is the static power loss, P_{GDQ}, which includes quiescent power loss on the driver as well as driver self-power consumption when operating with a certain switching frequency. P_{GDQ} is measured on the bench with no load connected to OUTA and OUTB at a given VCCI, VDDA/VDDB, switching frequency and ambient temperature. In this example, V_{VCCI} = 5 V and V_{VDD} = 12 V. The current on each power supply, with

INA/INB switching from 0 V to 3.3 V at 100 kHz is measured to be I_{VCCI} ≈ 2.5 mA, and I_{VDDA} = I_{VDDB} ≈ 1.5 mA. Therefore, the P_{GDQ} can be calculated with

$$P_{GDQ} = V_{VCCI} \times I_{VCCI} + V_{VDDA} \times I_{DDA} + V_{VDDB} \times I_{DDB} = 50mW \tag{11}$$

The second component is switching operation loss, P_{GDO}, with a given load capacitance which the driver charges and discharges the load during each switching cycle. Total dynamic loss due to load switching, P_{GSW}, can be estimated with

$$P_{GSW} = 2 \times V_{DD} \times Q_G \times f_{SW} \tag{12}$$

where

- Q_G is the gate charge of the power transistor.

If a split rail is used to turn on and turn off, then VDD is going to be equal to difference between the positive rail to the negative rail.

So, for this example application:

$$P_{GSW} = 2 \times 12V \times 100nC \times 100kHz = 240mW \tag{13}$$

Q_G represents the total gate charge of the power transistor switching 480 V at 14 A provided by the datasheet, and is subject to change with different testing conditions. The UCC21222-Q1 gate driver loss on the output stage, P_{GDO}, is part of P_{GSW}. P_{GDO} will be equal to P_{GSW} if the external gate driver resistances are zero, and all the gate driver loss is dissipated inside the UCC21222-Q1. If there are external turn-on and turn-off resistances, the total loss will be distributed between the gate driver pull-up/down resistances and external gate resistances. Importantly, the pull-up/down resistance is a linear and fixed resistance if the source/sink current is not saturated to 4 A/6 A, however, it will be non-linear if the source/sink current is saturated. Therefore, P_{GDO} is different in these two scenarios.

Case 1 - Linear Pull-Up/Down Resistor:

$$P_{GDO} = \frac{P_{GSW}}{2} \times \left(\frac{R_{OH} \,||\, R_{NMOS}}{R_{OH} \,||\, R_{NMOS} + R_{ON} + R_{GFET\_Int}} + \frac{R_{OL}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET\_Int}} \right) \tag{14}$$

In this design example, all the predicted source/sink currents are less than 4 A/6 A, therefore, the UCC21222-Q1 gate driver loss can be estimated with:

$$P_{GDO} = \frac{240mW}{2} \times \left(\frac{5\Omega \,||\, 1.47\Omega}{5\Omega \,||\, 1.47\Omega + 2.2\Omega + 1.5\Omega} + \frac{0.55\Omega}{0.55\Omega + 0\Omega + 1.5\Omega} \right) \approx 60mW \tag{15}$$

Case 2 - Nonlinear Pull-Up/Down Resistor:

$$P_{GDO} = 2 \times f_{SW} \times \left[4A \times \int_0^{T_{R\_Sys}} \left(V_{DD} - V_{OUTA/B}(t) \right) dt + 6A \times \int_0^{T_{F\_Sys}} V_{OUTA/B}(t) dt \right] \tag{16}$$

where

- $V_{OUTA/B}(t)$ is the gate driver OUTA and OUTB pin voltage during the turn on and off transient, and it can be simplified that a constant current source (4 A at turn-on and 6 A at turn-off) is charging/discharging a load capacitor. Then, the $V_{OUTA/B}(t)$ waveform will be linear and the T_{R_Sys} and T_{F_Sys} can be easily predicted.

For some scenarios, if only one of the pull-up or pull-down circuits is saturated and another one is not, the P_{GDO} will be a combination of Case 1 and Case 2, and the equations can be easily identified for the pull-up and pull-down based on the above discussion. Therefore, total gate driver loss dissipated in the gate driver UCC21222-Q1 P_{GD}, is:

$$P_{GD} = P_{GDQ} + P_{GDO} \tag{17}$$

which is equal to 127 mW in the design example.

8.2.2.7 Estimating Junction Temperature

The junction temperature of the UCC21222-Q1 can be estimated with:

$$T_J = T_C + \Psi_{JT} \times P_{GD} \tag{18}$$

where

- T_J is the junction temperature.
- T_C is the UCC21222-Q1 case-top temperature measured with a thermocouple or some other instrument.
- ψ_{JT} is the junction-to-top characterization parameter from the Thermal Information table.

Using the junction-to-top characterization parameter (Ψ_{JT}) instead of the junction-to-case thermal resistance ($R_{\Theta JC}$) can greatly improve the accuracy of the junction temperature estimation. The majority of the thermal energy of most ICs is released into the PCB through the package leads, whereas only a small percentage of the total energy is released through the top of the case (where thermocouple measurements are usually conducted). $R_{\Theta JC}$ can only be used effectively when most of the thermal energy is released through the case, such as with metal packages or when a heatsink is applied to an IC package. In all other cases, use of $R_{\Theta JC}$ will inaccurately estimate the true junction temperature. Ψ_{JT} is experimentally derived by assuming that the amount of energy leaving through the top of the IC will be similar in both the testing environment and the application environment. As long as the recommended layout guidelines are observed, junction temperature estimates can be made accurately to within a few degrees Celsius. For more information, see the セクション 10.1 and *Semiconductor and IC Package Thermal Metrics application report*.

8.2.2.8 Selecting VCCI, VDDA/B Capacitor

Bypass capacitors for VCCI, VDDA, and VDDB are essential for achieving reliable performance. It is recommended that one choose low ESR and low ESL surface-mount multi-layer ceramic capacitors (MLCC) with sufficient voltage ratings, temperature coefficients and capacitance tolerances. Importantly, DC bias on an MLCC will impact the actual capacitance value. For example, a 25-V, 1-µF X7R capacitor is measured to be only 500 nF when a DC bias of 15 V_{DC} is applied.

8.2.2.8.1 Selecting a VCCI Capacitor

A bypass capacitor connected to VCCI supports the transient current needed for the primary logic and the total current consumption, which is only a few mA. Therefore, a 25-V MLCC with over 100 nF is recommended for this application. If the bias power supply output is a relatively long distance from the VCCI pin, a tantalum or electrolytic capacitor, with a value over 1 µF, should be placed in parallel with the MLCC.

8.2.2.8.2 Selecting a VDDA (Bootstrap) Capacitor

A VDDA capacitor, also referred to as a *bootstrap capacitor* in bootstrap power supply configurations, allows for gate drive current transients up to 6 A, and needs to maintain a stable gate drive voltage for the power transistor.

The total charge needed per switching cycle can be estimated with

$$Q_{Total} = Q_G + \frac{I_{VDD}@100kHz(No\ Load)}{f_{SW}} = 100nC + \frac{1.5mA}{100kHz} = 115nC \quad (19)$$

where

- Q_G: Gate charge of the power transistor.
- I_{VDD}: The channel self-current consumption with no load at 100kHz.

Therefore, the absolute minimum C_{Boot} requirement is:

$$C_{Boot} = \frac{Q_{Total}}{\Delta V_{VDDA}} = \frac{115nC}{0.5V} = 230nF \quad (20)$$

where

- ΔV_{VDDA} is the voltage ripple at VDDA, which is 0.5 V in this example.

In practice, the value of C_{Boot} is greater than the calculated value. This allows for the capacitance shift caused by the DC bias voltage and for situations where the power stage would otherwise skip pulses due to load transients. Therefore, it is recommended to include a safety-related margin in the C_{Boot} value and place it as close to the VDD and VSS pins as possible. A 50-V 1-µF capacitor is chosen in this example.

$$C_{Boot} = 1\mu F \quad (21)$$

To further lower the AC impedance for a wide frequency range, it is recommended to have bypass capacitor with a low capacitance value, in this example a 100 nF, in parallel with C_{Boot} to optimize the transient performance.

注

Too large C_{BOOT} is not good. C_{BOOT} may not be charged within the first few cycles and V_{BOOT} could stay below UVLO. As a result, the high-side FET does not follow input signal command. Also during initial C_{BOOT} charging cycles, the bootstrap diode has highest reverse recovery current and losses.

8.2.2.8.3 Select a VDDB Capacitor

Chanel B has the same current requirements as Channel A, Therefore, a VDDB capacitor (Shown as C_{VDD} in 図 8-1) is needed. In this example with a bootstrap configuration, the VDDB capacitor will also supply current for VDDA through the bootstrap diode. A 50-V, 10-µF MLCC and a 50-V, 220-nF MLCC are chosen for C_{VDD}. If the bias power supply output is a relatively long distance from the VDDB pin, a tantalum or electrolytic capacitor with a value over 10 µF, should be used in parallel with C_{VDD}.

8.2.2.9 Application Circuits with Output Stage Negative Bias

When parasitic inductances are introduced by non-ideal PCB layout and long package leads (e.g. TO-220 and TO-247 type packages), there could be ringing in the gate-source drive voltage of the power transistor during high di/dt and dv/dt switching. If the ringing is over the threshold voltage, there is the risk of unintended turn-on and even shoot-through. Applying a negative bias on the gate drive is a popular way to keep such ringing below the threshold. Below are a few examples of implementing negative gate drive bias.

図 8-2 shows the first example with negative bias turn-off on the channel-A driver using a Zener diode on the isolated power supply output stage. The negative bias is set by the Zener diode voltage. If the isolated power supply, V_A, is equal to 17 V, the turn-off voltage will be –5.1 V and turn-on voltage will be 17 V – 5.1 V ≈ 12 V. The channel-B driver circuit is the same as channel-A, therefore, this configuration needs two power supplies for a half-bridge configuration, and there will be steady state power consumption from R_Z.

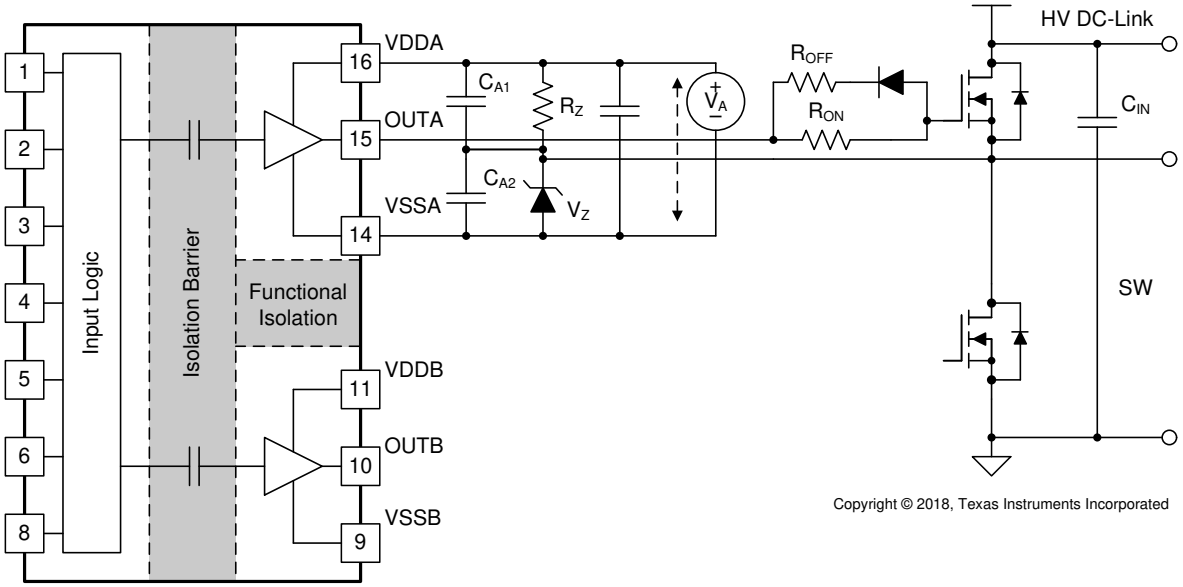


図 8-2. Negative Bias with Zener Diode on Iso-Bias Power Supply Output

図 8-3 shows another example which uses two supplies (or single-input-double-output power supply). Power supply V_{A+} determines the positive drive output voltage and V_{A-} determines the negative turn-off voltage. The configuration for channel B is the same as channel A. This solution requires more power supplies than the first example, however, it provides more flexibility when setting the positive and negative rail voltages.

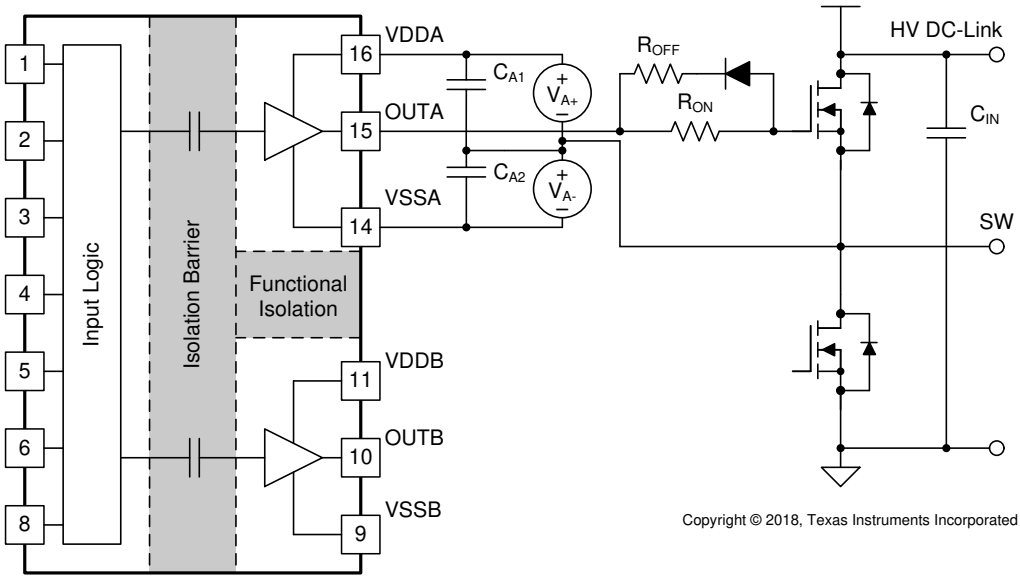


図 8-3. Negative Bias with Two Iso-Bias Power Supplies

The last example, shown in 図 8-4, is a single power supply configuration and generates negative bias through a Zener diode in the gate drive loop. The benefit of this solution is that it only uses one power supply and the bootstrap power supply can be used for the high side drive. This design requires the least cost and design effort among the three solutions. However, this solution has limitations:

1. The negative gate drive bias is not only determined by the Zener diode, but also by the duty cycle, which means the negative bias voltage will change when the duty cycle changes. Therefore, converters with a fixed duty cycle (~50%) such as variable frequency resonant convertors or phase shift convertors which favor this solution.

2. The high side VDDA-VSSA must maintain enough voltage to stay in the recommended power supply range, which means the low side switch must turn-on or have free-wheeling current on the body (or anti-parallel) diode for a certain period during each switching cycle to refresh the bootstrap capacitor. Therefore, a 100% duty cycle for the high side is not possible unless there is a dedicated power supply for the high side, like in the other two example circuits.

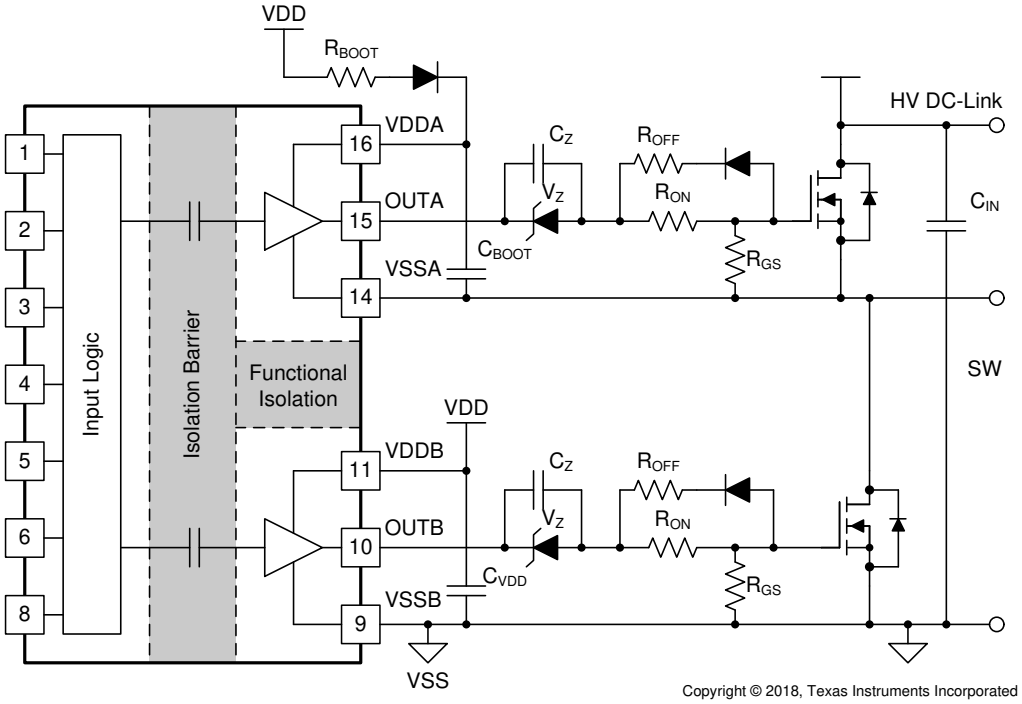


図 8-4. Negative Bias with Single Power Supply and Zener Diode in Gate Drive Path

8.2.3 Application Curves

図 8-5 and 図 8-6 shows the bench test waveforms for the design example shown in 図 8-1 under these conditions: VCC = 5.0 V, VDD = 12 V, f_{SW} = 100 kHz, $V_{DC-Link}$ = 400 V.

Channel 1 (Blue): Gate-source signal on the high side power transistor.

Channel 2 (Cyan): Gate-source signal on the low side power transistor.

Channel 3 (Pink): INA pin signal.

Channel 4 (Green): INB pin signal.

In 図 8-5, INA and INB are sent complimentary 3.3-V, 20%/80% duty-cycle signals. The gate drive signals on the power transistor have a 200-ns dead time with 400V high voltage on the DC-Link, shown in the measurement section of 図 8-5. Note that with high voltage present, lower bandwidth differential probes are required, which limits the achievable accuracy of the measurement.

図 8-6 shows a zoomed-in version of the waveform of 図 8-5, with measurements for propagation delay and dead time. Importantly, the output waveform is measured between the power transistors' gate and source pins, and is not measured directly from the driver OUTA and OUTB pins.

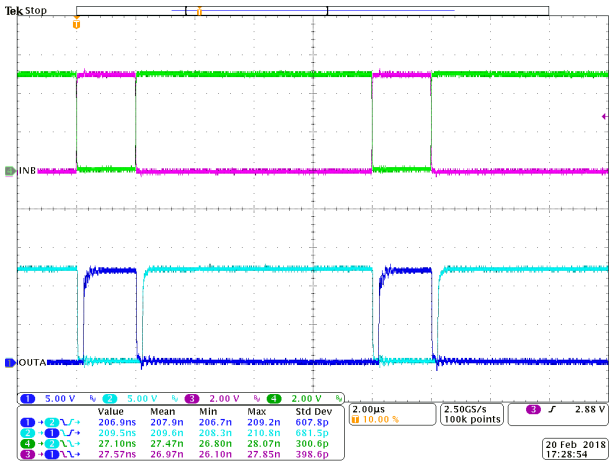


図 8-5. Bench Test Waveform for INA/B and OUTA/B

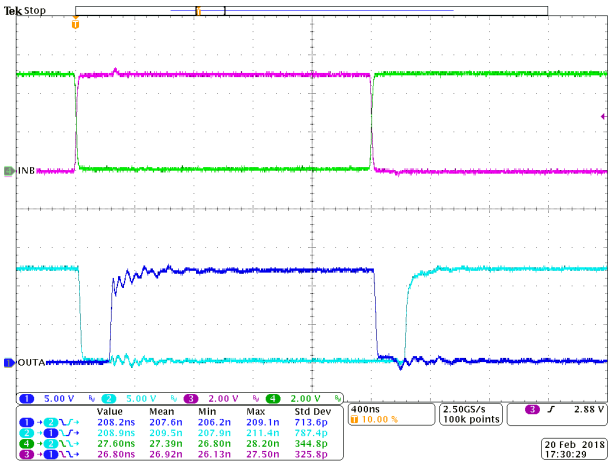


図 8-6. Zoomed-In bench-test waveform

9 Power Supply Recommendations

The recommended input supply voltage (VCCI) for the UCC21222-Q1 is between 3 V and 5.5 V. The output bias supply voltage (VDDA/VDDB) ranges from 9.2 V to 18 V. The lower end of this bias supply range is governed by the internal under voltage lockout (UVLO) protection feature of each device. VDD and VCCI must not fall below their respective UVLO thresholds during normal operation. (For more information on UVLO see セクション 7.3.1). The upper end of the VDDA/VDDB range depends on the maximum gate voltage of the power device being driven by the UCC21222-Q1. The recommended maximum VDDA/VDDB is 18 V.

A local bypass capacitor should be placed between the VDD and VSS pins, to supply current when the output goes high into a capacitive load. This capacitor should be positioned as close to the device as possible to minimize parasitic impedance. A low ESR, ceramic surface mount capacitor is recommended. If the bypass capacitor impedance is too large, resistive and inductive parasitics could cause the supply voltage seen at the IC pins to dip below the UVLO threshold unexpectedly. To filter high frequency noise between VDD and VSS, it can be helpful to place a second capacitor with lower impedance at higher frequency. As an example, the primary bypass capacitor could be 1 µF, with a secondary high frequency bypass capacitor of 100 pF.

Similarly, a bypass capacitor should also be placed between the VCCI and GND pins. Given the small amount of current drawn by the logic circuitry within the input side of the UCC21222-Q1, this bypass capacitor has a minimum recommended value of 100 nF.

10 Layout

10.1 Layout Guidelines

Consider these PCB layout guidelines for in order to achieve optimum performance for the UCC21222-Q1.

10.1.1 Component Placement Considerations

- Low-ESR and low-ESL capacitors must be connected close to the device between the VCCI and GND pins and between the VDD and VSS pins to support high peak currents when turning on the external power transistor.
- To avoid large negative transients on the switch node VSSA (HS) pin in bridge configurations, the parasitic inductances between the source of the top transistor and the source of the bottom transistor must be minimized.
- To improve noise immunity when driving the DIS pin from a distant microcontroller, TI recommends adding a small bypass capacitor, ≥ 1000 pF, between the DIS pin and GND.
- If the dead time feature is used, TI recommends placing the programming resistor R_{DT} and capacitor close to the DT pin of the UCC21222-Q1 to prevent noise from unintentionally coupling to the internal dead time circuit. The capacitor should be ≥ 2.2 nF.

10.1.2 Grounding Considerations

- It is essential to confine the high peak currents that charge and discharge the transistor gates to a minimal physical area. This will decrease the loop inductance and minimize noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.
- Pay attention to high current path that includes the bootstrap capacitor, bootstrap diode, local VSSB-referenced bypass capacitor, and the low-side transistor body/anti-parallel diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode by the VDD bypass capacitor. This recharging occurs in a short time interval and involves a high peak current. Minimizing this loop length and area on the circuit board is important for ensuring reliable operation.

10.1.3 High-Voltage Considerations

- To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the driver device. A PCB cutout is recommended in order to prevent contamination that may compromise the isolation performance.
- For half-bridge or high-side/low-side configurations, maximize the clearance distance of the PCB layout between the high and low-side PCB traces.

10.1.4 Thermal Considerations

- A large amount of power may be dissipated by the UCC21222-Q1 if the driving voltage is high, the load is heavy, or the switching frequency is high (refer to セクション 8.2.2.6 for more details). Proper PCB layout can help dissipate heat from the device to the PCB and minimize junction to board thermal impedance (θ_{JB}).
- Increasing the PCB copper connecting to VDDA, VDDB, VSSA and VSSB pins is recommended, with priority on maximizing the connection to VSSA and VSSB (see 図 10-2 and 図 10-3). However, high voltage PCB considerations mentioned above must be maintained.
- If there are multiple layers in the system, it is also recommended to connect the VDDA, VDDB, VSSA and VSSB pins to internal ground or power planes through multiple vias of adequate size. Ensure that no traces or copper from different high-voltage planes overlap.

10.2 Layout Example

図 10-1 shows a 2-layer PCB layout example with the signals and key components labeled.

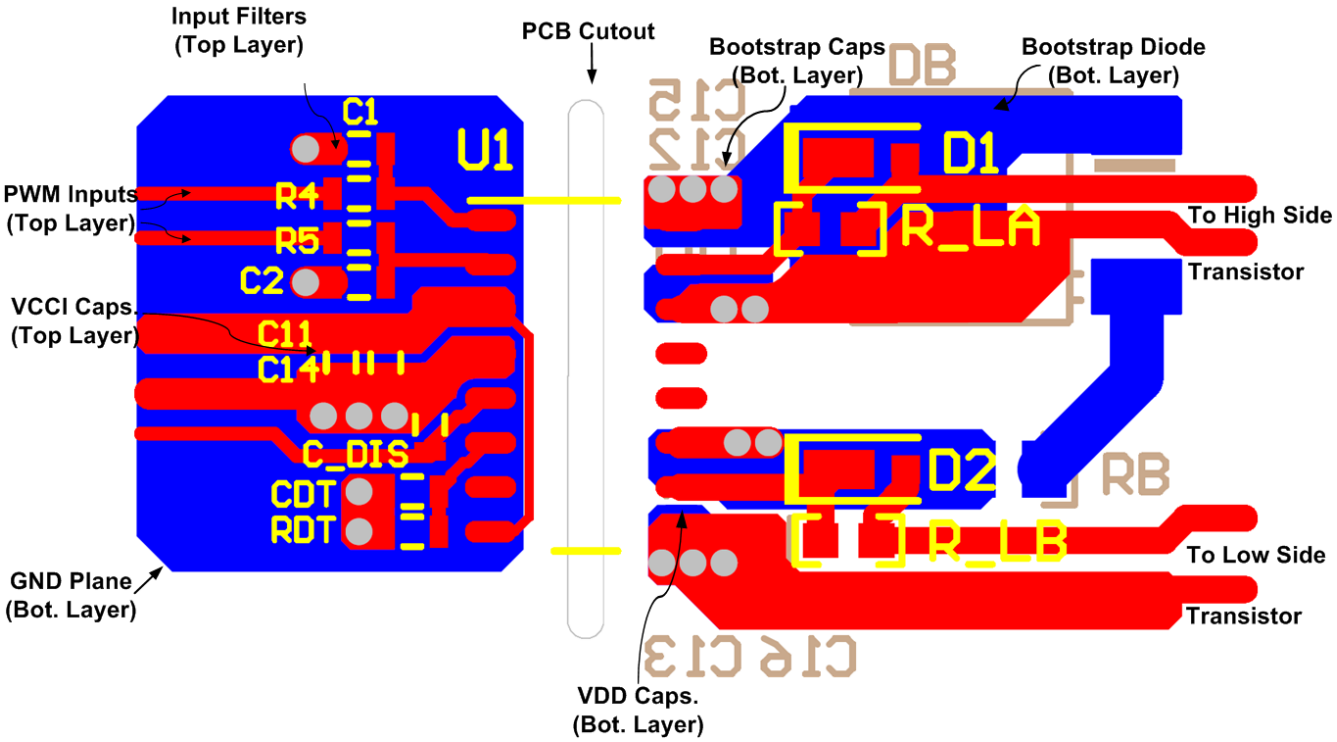


図 10-1. Layout Example

図 10-2 and 図 10-3 shows top and bottom layer traces and copper.

注

There are no PCB traces or copper between the primary and secondary side, which ensures isolation performance.

PCB traces between the high-side and low-side gate drivers in the output stage are increased to maximize the creepage distance for high-voltage operation, which will also minimize cross-talk between the switching node VSSA (SW), where high dv/dt may exist, and the low-side gate drive due to the parasitic capacitance coupling.

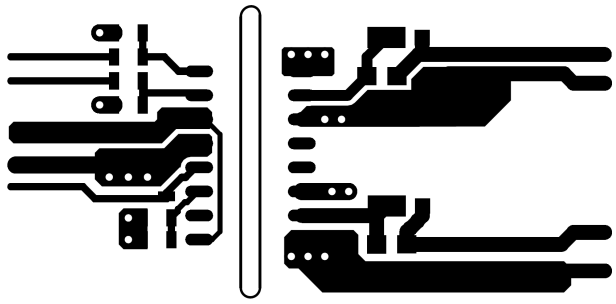


図 10-2. Top Layer Traces and Copper

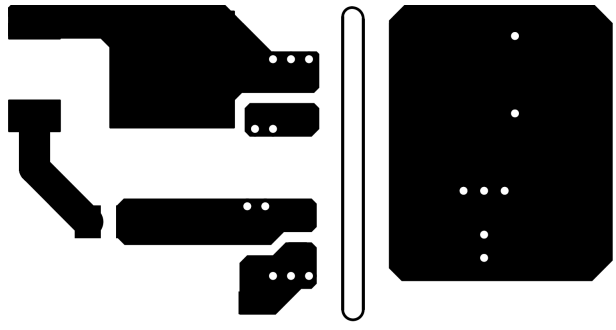


図 10-3. Bottom Layer Traces and Copper (Flipped)

図 10-4 and 図 10-5 are 3-D layout pictures with top view and bottom views.

注

The location of the PCB cutout between the primary side and secondary sides, which ensures isolation performance.

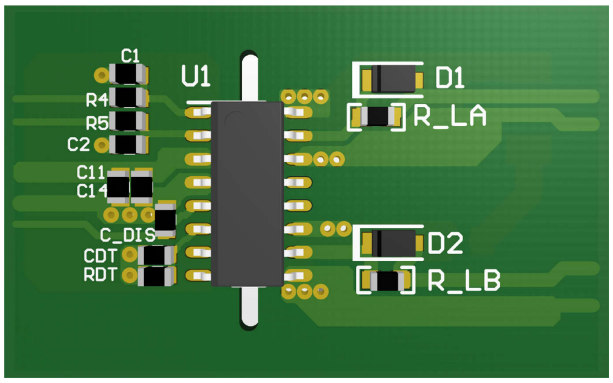


図 10-4. 3-D PCB Top View

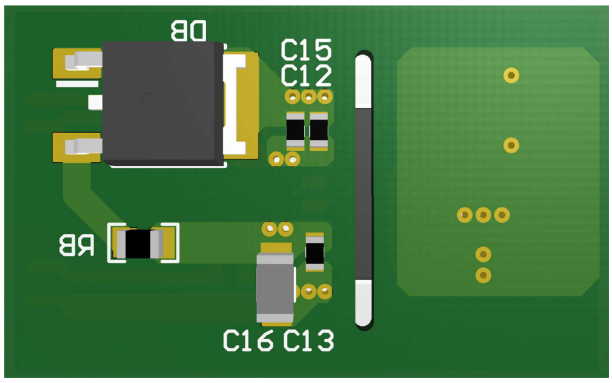


図 10-5. 3-D PCB Bottom View

11 Device and Documentation Support

11.1 Device Support

11.1.1 サード・パーティ製品に関する免責事項

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11.1.2 Development Support

11.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the UCC21222-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *Semiconductor and IC Package Thermal Metrics Application Report*
- Isolation Glossary

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (February 2024) to Revision B (April 2024) **Page**

- 「特長」セクションを更新 1
- 「概要」セクションを更新 1
- Updated DIS pin and DT pin descriptions in section Pin Configuration and Functions 3
- Updated section 5.1 Absolute Maximum Ratings 4
- Updated section 5.2 ESD Ratings (Automotive) 4
- Updated section 5.3 Recommended Operating Conditions 4
- Updated section 5.4 Thermal Information 4
- Updated section 5.5 Power Ratings 5
- Updated section 5.6 Insulation Specifications 6
- Deleted Safety-Related Certification section 7
- Updated section 5.7 Safety Limiting Values 7
- Updated section 5.8 Electrical Characteristics 8
- Updated section 5.9 Switching Characteristics 9
- Changed section name from Thermal Derating Curves to Insulation Characteristics Curves 10
- Updated section Typical Characteristics 11
- Updated section Programmable Dead Time 16
- Updated timings called out in section Power-Up UVLO Delay to OUTPUT 17
- Updated internal resistor structure in section Functional Block Diagram 19
- Updated section Input and Output Logic Table 21
- Updated section Input Stage to match new specifications 21
- Updated section Output Stage to address minimum pulse widths 22
- Updated ESD cell structure figure in section Diode Structure in the UCC21222-Q1 23
- Updated section Disable Pin verbiage 23
- Updated new deadtime equation in section Connecting a Programming Resistor between DT and GND Pins 23
- Updated deadtime value due to change in deadtime equation in section Select Dead Time Resistor and Capacitor 26

Changes from Revision * (February 2018) to Revision A (February 2024) **Page**

- Changed CTI and Material Group values in Insulation Secifications and added table note 4

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC21222QDQ1	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 125	21222Q	
UCC21222QDRQ1	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	21222Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF UCC21222-Q1 :

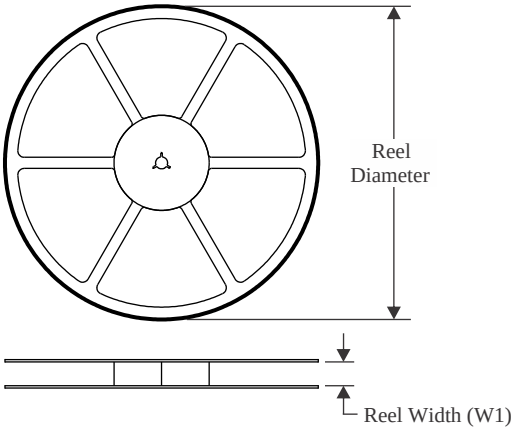
- Catalog : UCC21222

NOTE: Qualified Version Definitions:

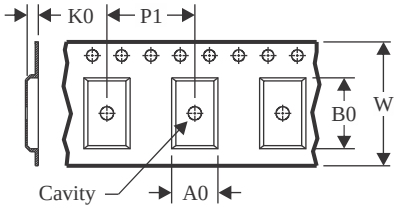
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

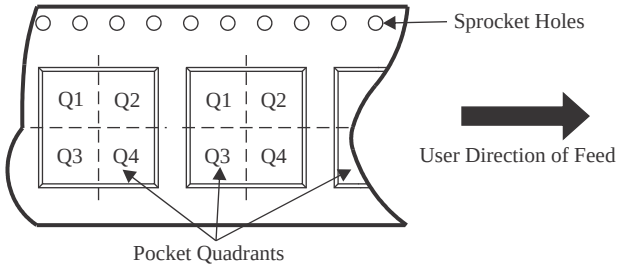


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

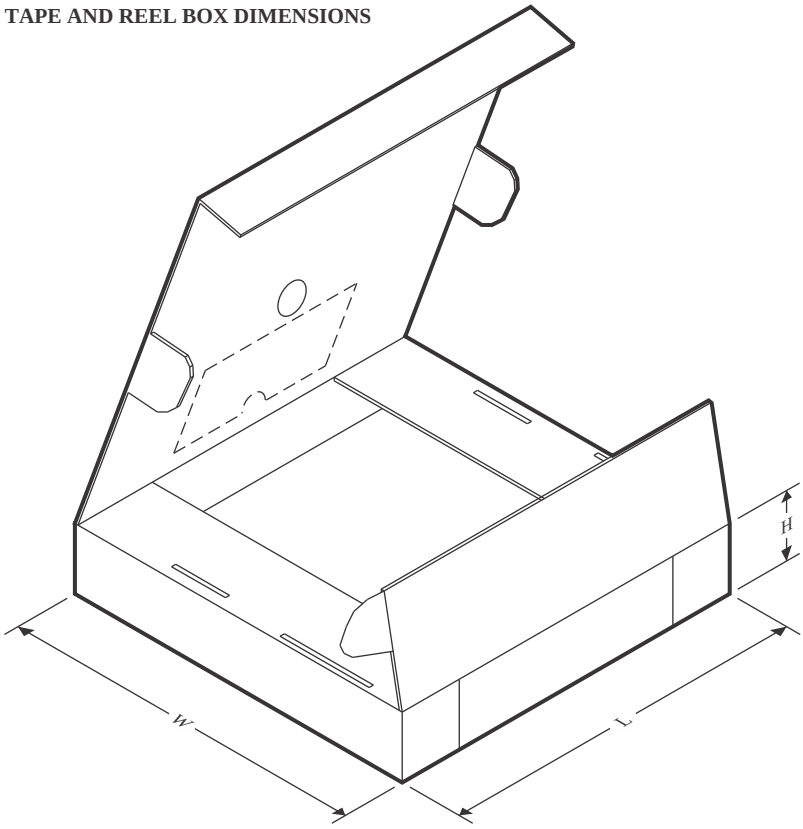
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC21222QDRQ1	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC21222QDRQ1	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

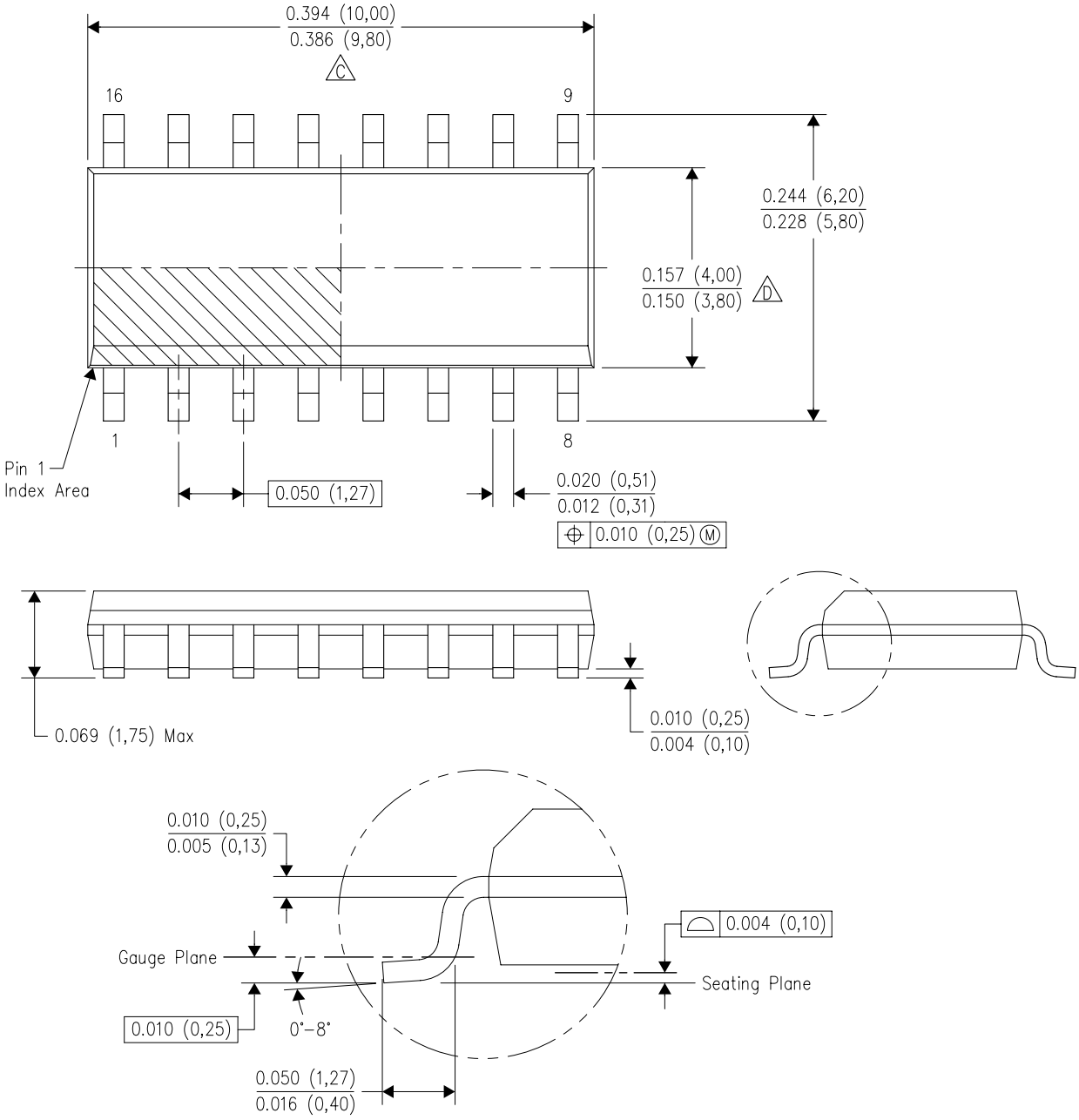
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC21222QDRQ1	SOIC	D	16	2500	350.0	350.0	43.0
UCC21222QDRQ1	SOIC	D	16	2500	356.0	356.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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