UCC27531-Q1 2.5-A and 5-A, 35-V_{MAX} VDD FET and IGBT Single-Gate Driver

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C4B
- Low Cost Gate Driver (Offering Optimal Solution for Driving Fet And Igbts)
- Superior Replacement to Discrete Transistor Pair Drive (Providing Easy Interface With Controller)
- TTL and CMOS Compatible Input Logic Threshold, (Independent of Supply Voltage)
- Split Output Options Allow for Tuning of Turn-On and Turn-Off Currents
- Enable with Fixed TTL Compatible Threshold
- High 2.5-A Source and 5-A Sink Peak Drive Currents at 18-V VDD
- Wide VDD Range From 10 V up to 35 V
- Input and Enable Pins Capable of Withstanding up to –5-V DC Below Ground
- Output Held Low When Inputs are Floating or During VDD UVLO
- Fast Propagation Delays (17-ns Typical)
- Fast Rise and Fall Times
  (15-ns and 7-ns Typical With 1800-pF Load)
- Undervoltage Lockout (UVLO)
- Used as a High-Side or Low-Side Driver (if Designed With Proper Bias and Signal Isolation)
- Low-Cost, Space-Saving 6-Pin DBV (SOT-23) Package Options
- Operating Temperature Range of –40°C to 140°C

2 Applications

- Automotive
- Switch-Mode Power Supplies
- DC-to-DC Converters
- Solar Inverters, Motor Control, UPS
- HEV and EV Chargers
- Home Appliances
- Renewable Energy Power Conversion
- SiC FET Converters

3 Description

The UCC27531-Q1 is a single-channel, high-speed, gate driver capable of effectively driving MOSFET and IGBT power switches by using up to 2.5-A source and 5-A sink (asymmetrical drive) peak current. Strong sink capability in asymmetrical drive boosts immunity against parasitic Miller turn-on effect. The UCC27531-Q1 device can also feature a split-output configuration where the gate-drive current is sourced through the OUTH pin and sunk through the OUTL pin. This pin arrangement allows the user to apply independent turn-on and turn-off resistors to the OUTH and OUTL pins respectively and easily control the switching slew rates.

The driver has rail-to-rail drive capability and an extremely small propagation delay of typically 17 ns.

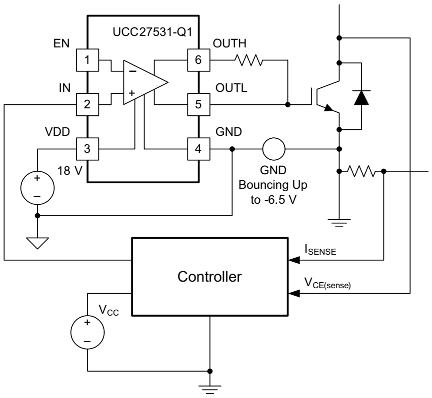
The input threshold of UCC27531-Q1 is based on TTL and CMOS compatible low-voltage logic, which is fixed and independent of VDD supply voltage. The 1-V typical hysteresis offers excellent noise immunity.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC27531-Q1	SOT-23 (6)	1.6 mm × 2.9 mm

[1] For all available packages, see the orderable addendum at the end of the data sheet.

Driving IGBT Without Negative Bias



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 2013) to Revision B	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

Changes from Original (August 2013) to Revision A	Page
• Changed document from *Product Preview* to *Production Data*	1

5 Description (continued)

The driver has the EN pin with fixed TTL compatible threshold. The EN pin is internally pulled up; pulling the EN pin low disables driver, while leaving it open provides normal operation. The EN pin can be used as an additional input with the same performance as the IN pin.

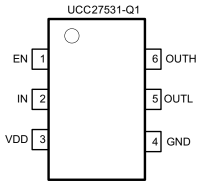
Leaving the input pin of driver open holds the output low. The logic behavior of the driver is shown in the application diagram, timing diagram and input and output logic truth table.

Internal circuitry on the VDD pin provides an UVLO function that holds output low until VDD supply voltage is within operating range.

The UCC27531-Q1 driver is offered in a 6-pin standard SOT-23 (DBV) package. The device operates over wide temperature range of –40°C to 140°C.

6 Pin Configuration and Functions

DBV Package
6-Pin SOT-23
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	1	I	Enable (Pull EN to GND in order to disable output, pull it high or leave open to enable output)
GND	4	—	Ground (all signals are referenced to this node)
IN	2	I	Driver non-inverting input
OUTH	6	O	2.5-A Source Current Output of driver
OUTL	5	O	5-A sink current output of driver
VDD	3	I	Bias supply input

7 Specifications

7.1 Absolute Maximum Ratings(1)(2)(3)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage	VDD	–0.3	35	V
Continuous	OUTH, OUTL, OUT	–0.3	VDD + 0.3	V
Pulse	OUTH, OUTL, OUT (200 ns)	–2	VDD + 0.3	V
Continuous IN, EN, IN+, IN-, IN1, IN2		–5	27	V
Pulse IN, EN, IN+, IN-, IN1, IN2 (1.5 µs)		–6.5	27	V
Operating virtual junction temperature, T_J		–40	150	°C
Lead temperature	Soldering, 10 sec.		300	°C
	Reflow		260	
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. See Packaging Section of the datasheet for thermal limitations and considerations of packages.
(3) These devices are sensitive to electrostatic discharge; follow proper device handling procedures.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage range, VDD	10	18	32	V
Ambient temperature range	–40		140	°C
Input voltage, IN, IN+, IN-, IN1, IN2	–5		25	V
Enable, EN	–5		25	V

7.4 Thermal Information

THERMAL METRIC(1)		UCC27531-Q1 DBV (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	178.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	109.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	27.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Unless otherwise noted, VDD = 18 V, T_A = –40°C to 140°C, 1-µF capacitor from VDD to GND, f = 100 kHz. Currents are positive into, negative out of the specified terminal. OUTH and OUTL are tied together for UCC27531-Q1. Typical condition specifications are at 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS CURRENTS						
I_{DDoff}	Startup current	VDD = 7, IN, EN = VDD	100	200	300	µA
		IN, EN = GND	100	217	300	
UVLO						
V_{ON}	Supply start threshold		8	8.9	9.8	V
V_{OFF}	Minimum operating voltage after supply start		7.3	8.2	9.1	V
V_{DD_H}	Supply voltage hysteresis			0.7		V
INPUT (IN)						
V_{IN_H}	Input signal high threshold, output high	Output High, EN = HIGH	1.8	2	2.2	V
V_{IN_L}	Input signal low threshold, output low	Output Low, EN = HIGH	0.8	1	1.2	V
V_{IN_HYS}	Input signal hysteresis			1		V
ENABLE (EN)						
V_{EN_H}	Enable signal high threshold	Output High	1.7	1.9	2.1	V
V_{EN_L}	Enable signal low threshold	Output Low	0.8	1	1.2	V
V_{EN_HYS}	Enable signal hysteresis			0.9		V
OUTPUTS (OUTH/OUTL)						
$I_{SRC/SNK}$	Source peak current (OUTH)/ sink peak current (OUTL)	CLOAD = 0.22 µF, f = 1 kHz	–2.5 / +5			A
V_{OH}	OUTH, high voltage	I_{OUTH} = –10 mA	VDD - 0.2	VDD - 0.12	VDD - 0.07	V
V_{OL}	OUTL, low voltage	I_{OUTL} = 100 mA		0.065	0.125	V
R_{OH}	OUTH, pullup resistance	T_A = 25°C, I_{OUT} = –10 mA	11	12	12.5	Ω
		T_A = –40°C to 140°C, I_{OUT} = –10 mA	7	12	20	
R_{OL}	OUTL, pulldown resistance	T_A = 25°C, I_{OUT} = 100 mA	0.45	0.65	0.85	Ω
		T_A = –40°C to 140°C, I_{OUT} = 100 mA	0.3	0.65	1.25	

7.6 Switching Characteristics

Unless otherwise noted, VDD = 18 V, T_A = –40°C to 140°C, 1-µF capacitor from VDD to GND, f = 100 kHz. Currents are positive into, negative out of the specified terminal. OUTH and OUTL are tied together for UCC27531-Q1. Typical condition specifications are at 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R	Rise time	C_{LOAD} = 1.8 nF		15		ns
t_F	Fall time	C_{LOAD} = 1.8 nF		7		ns
t_{D1}	Turn-on propagation delay	C_{LOAD} = 1.8 nF, IN = 0 V to 5 V		17	26	ns
t_{D2}	Turn-off propagation delay	C_{LOAD} = 1.8 nF, IN = 5 V to 0 V		17	26	ns

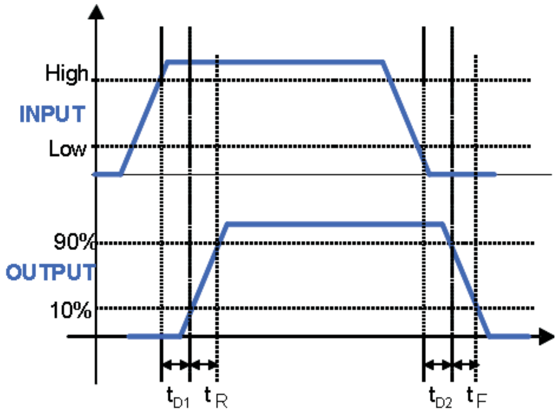


Figure 1. Timing Diagram (OUTPUT = OUTH tied to OUTL) INPUT = IN, (EN = VDD), or INPUT = EN, (IN = VDD)

7.7 Typical Characteristics

If not specified, INPUT refers to non-inverting input

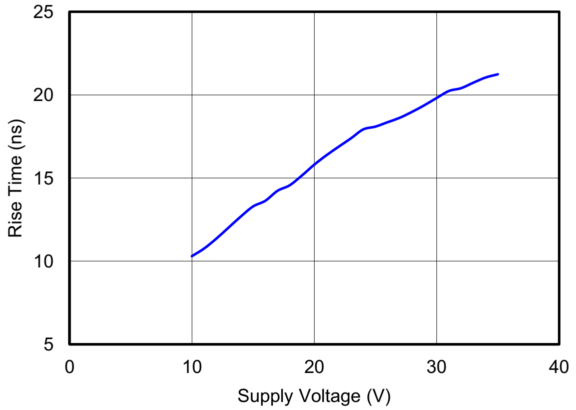


Figure 2. Rise Time vs Supply Voltage

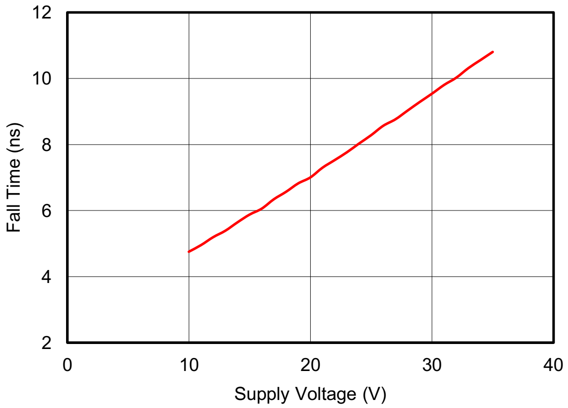


Figure 3. Fall Time vs Supply Voltage

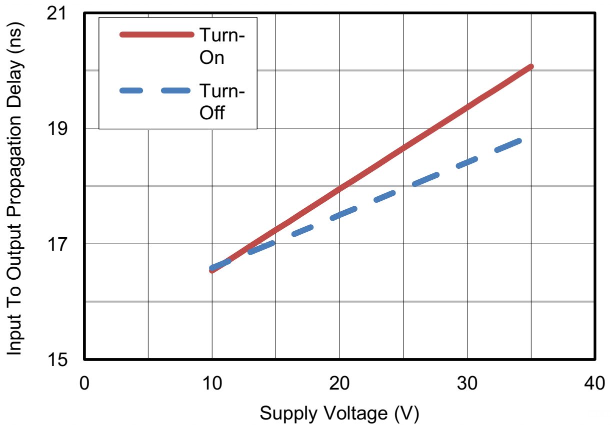


Figure 4. Propagation Delay vs Supply Voltage

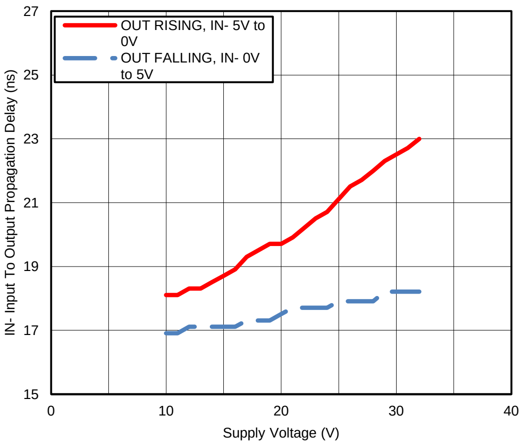


Figure 5. IN - Propagation Delay vs Supply

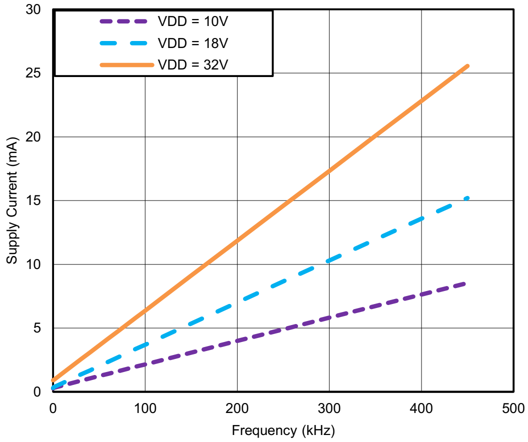


Figure 6. Operating Supply Current vs Frequency

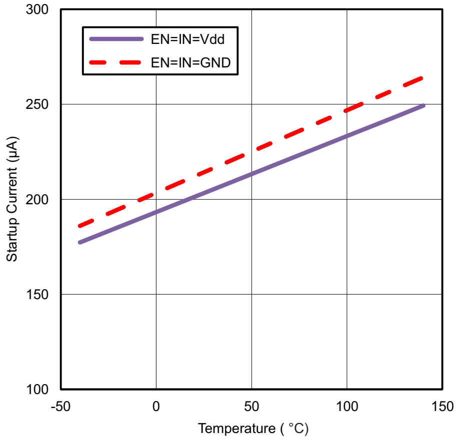


Figure 7. Start-Up Current vs Temperature

Typical Characteristics (continued)

If not specified, INPUT refers to non-inverting input

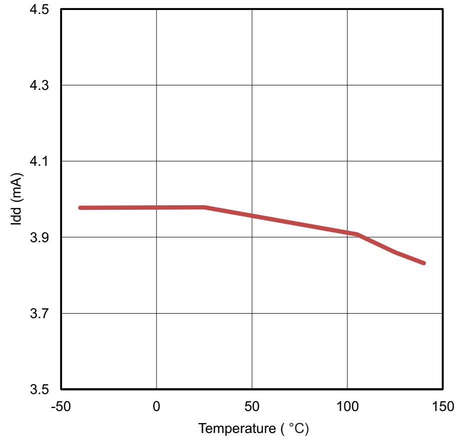


Figure 8. Operating Supply Current vs Temperature (Output Switching)

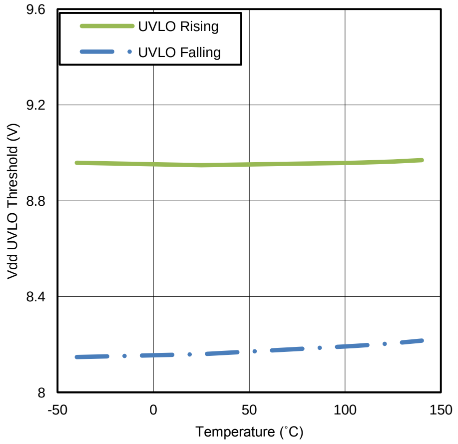


Figure 9. UVLO Threshold Voltage vs Temperature

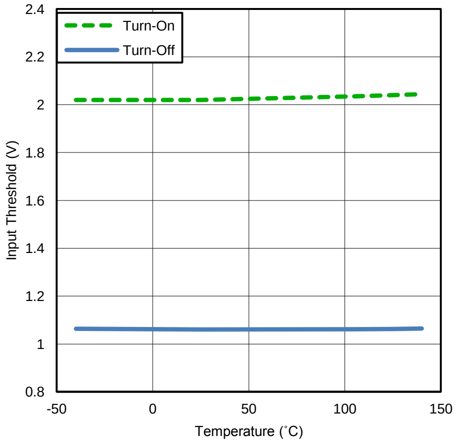


Figure 10. Input Threshold vs Temperature

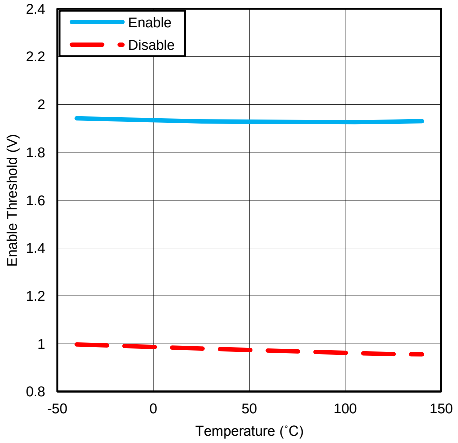


Figure 11. Enable Threshold vs Temperature

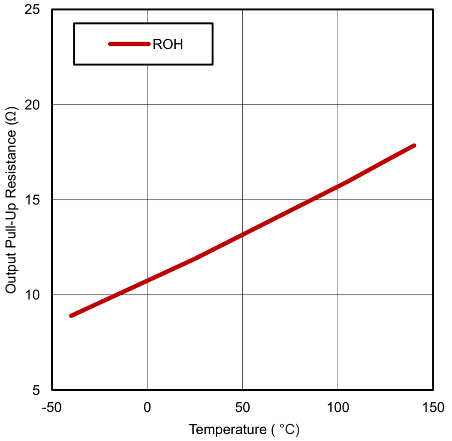


Figure 12. Output Pullup Resistance vs Temperature

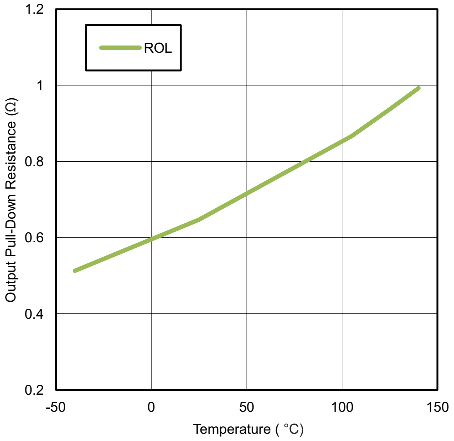


Figure 13. Output Pulldown Resistance vs Temperature

Typical Characteristics (continued)

If not specified, INPUT refers to non-inverting input

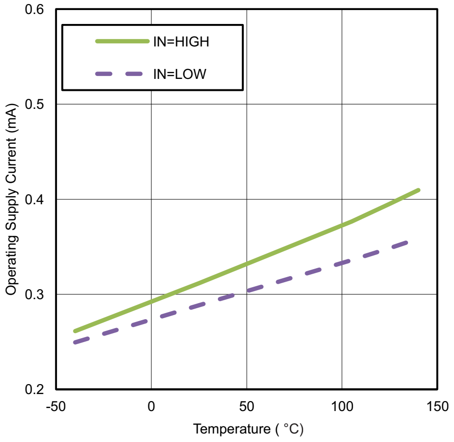


Figure 14. Operating Supply Current vs Temperature (Output in DC ON/OFF Condition)

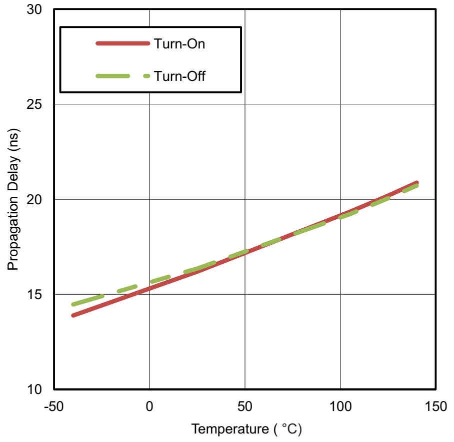


Figure 15. Input-to-Output Propagation Delay vs Temperature

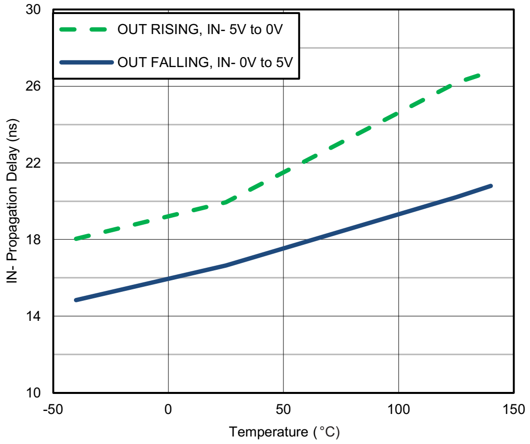


Figure 16. IN- Input-to-Output Propagation Delay vs Temperature

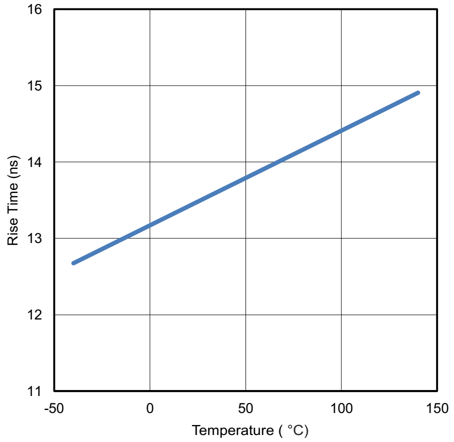


Figure 17. Rise Time vs Temperature

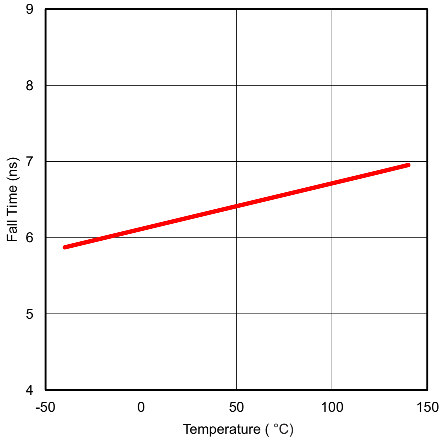


Figure 18. Fall Time vs Temperature

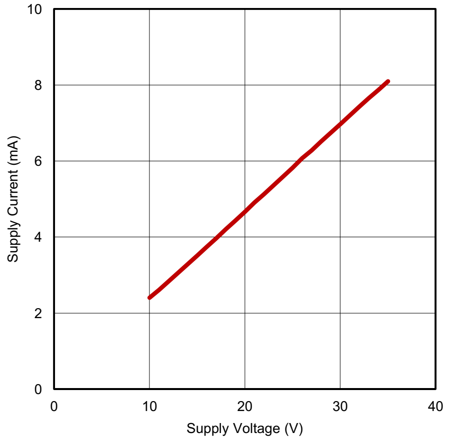


Figure 19. Operating Supply Current vs Supply Voltage (Output Switching)

Typical Characteristics (continued)

If not specified, INPUT refers to non-inverting input

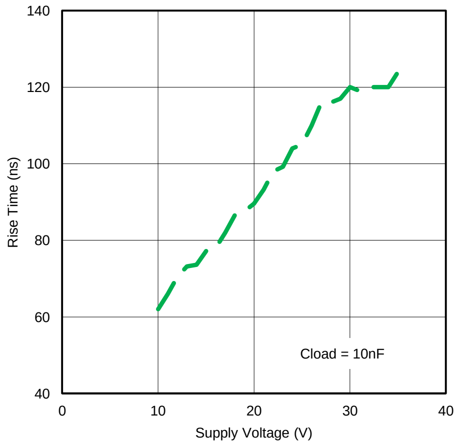


Figure 20. Rise Time vs Supply Voltage

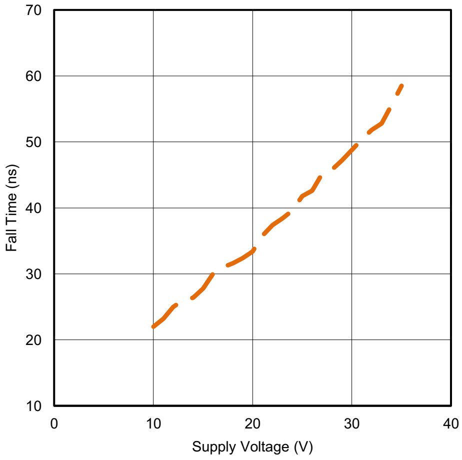


Figure 21. Fall Time vs Supply Voltage

8 Detailed Description

8.1 Overview

The UCC27531-Q1 is a single-channel, high-speed, gate driver capable of effectively driving MOSFET and IGBT power switches by up to 2.5-A source and 5-A sink (asymmetrical drive) peak current. Strong sink capability in asymmetrical drive boosts immunity against parasitic Miller turn-on effect. The UCC27531-Q1 device can also feature a split-output configuration where the gate-drive current is sourced through the OUTH pin and sunk through the OUTL pin. This pin arrangement allows the user to apply independent turn-on and turn-off resistors to the OUTH and OUTL pins, respectively, and easily control the switching slew rates.

The driver has rail-to-rail drive capability and extremely small propagation delay, typically 17 ns.

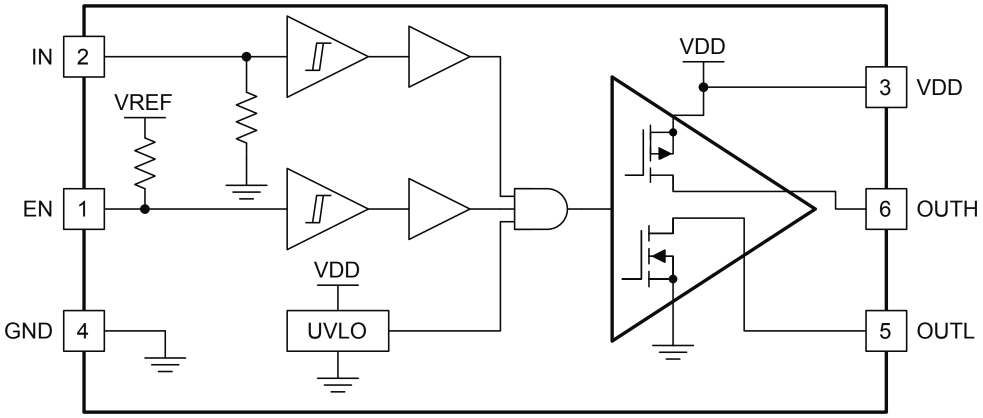
The input threshold of UCC27531-Q1 is based on TTL and CMOS compatible low-voltage logic, which is fixed and independent of VDD supply voltage. The 1-V typical hysteresis offers excellent noise immunity.

The driver has an EN pin with fixed TTL compatible threshold. EN is internally pulled up; pulling EN low disables the driver, while leaving EN open provides normal operation. The EN pin can be used as an additional input with the same performance as the IN, IN+, IN1, and IN2 pins.

Table 1. UCC27531-Q1 Features and Benefits

FEATURE	BENEFIT
High source and sink current capability, 2.5 A and 5 A (asymmetrical).	High current capability offers flexibility in employing UCC27531-Q1 device to drive a variety of power switching devices at varying speeds.
Low 17 ns (typ) propagation delay.	Extremely low pulse transmission distortion.
Wide VDD operating range of 10 V to 32 V.	Flexibility in system design.
	Can be used in split-rail systems such as driving IGBTs with both positive and negative(relative to Emitter) supplies.
	Optimal for many SiC FETs.
VDD UVLO protection.	Outputs are held Low in UVLO condition, which ensures predictable, glitch-free operation at power up and power down.
	High UVLO of 8.9 V typical ensures that power switch is not on in high-impedance state which could result in high power dissipation or even failures.
Outputs held low when input pin (INx) in floating condition.	Safety feature, especially useful in passing abnormal condition tests during safety certification
Split output structure option (OUTH, OUTL).	Allows independent optimization of turn-on and turn-off speeds using series gate resistors.
Strong sink current (5 A) and low pull-down impedance (0.65 Ω).	High immunity to high dV/dt Miller turn-on events.
CMOS and TTL compatible input threshold logic with wide hysteresis.	Enhanced noise immunity, while retaining compatibility with microcontroller logic level input signals (3.3 V, 5 V) optimized for digital power.
Input capable of withstanding –6.5 V.	Enhanced signal reliability in noisy environments that experience ground bounce on the gate driver.

8.2 Functional Block Diagram



(EN Pullup Resistance to VREF = 500 kΩ, VREF = 5.8 V, in Pulldown Resistance to GND = 230 kΩ)

8.3 Feature Description

8.3.1 VDD UVLO

The UCC27531-Q1 device has internal under voltage lockout (UVLO) protection feature on the VDD pin supply circuit blocks. To ensure an acceptable power dissipation in the power switch, this UVLO prevents the operation of the gate driver at low supply voltages. Whenever the driver is in UVLO condition (when VDD voltage less than V_{ON} during power-up and when VDD voltage is less than V_{OFF} during power down), this circuit holds all outputs LOW, regardless of the status of the inputs. The UVLO is typically 8.9 V with 700-mV typical hysteresis. This hysteresis helps prevent chatter when low VDD supply voltages have noise from the power supply and also when there are droops or dips in the VDD bias voltage when the system commences switching and there is a sudden increase in I_{DD}. The capability to operate at voltage levels such as 10 V to 32 V provides flexibility to drive Si MOSFETs, IGBTs, and emerging SiC FETs.

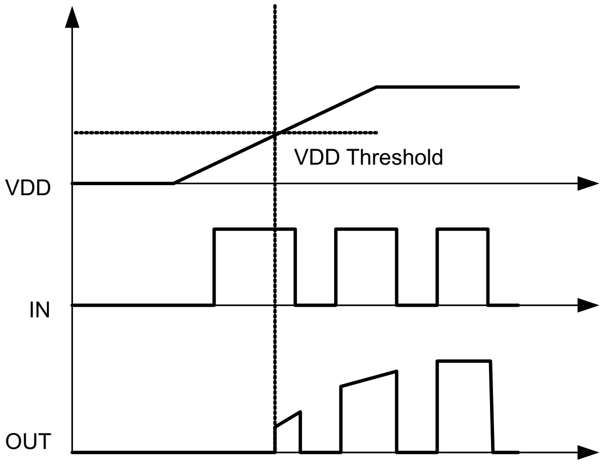


Figure 22. Power Up

8.3.2 Input Stage

The input pins of UCC27531-Q1 device are based on a TTL and CMOS compatible input threshold logic that is independent of the VDD supply voltage. With typical high threshold = 2 V and typical low threshold = 1 V, the logic level thresholds can be conveniently driven with PWM control signals derived from 3.3-V or 5-V logic. Wider hysteresis (typically 1 V) offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5 V. This device also features tight control of the input pin threshold voltage levels which eases system design considerations and guarantees stable operation across temperature. The very low input capacitance , typically 20 pF, on these pins reduces loading and increases switching speed.

Feature Description (continued)

The device features an important safety function wherein, whenever the input pin is in a floating condition, the output is held in the low state. This is achieved using pullup or pulldown resistors on the input pins as shown in the block diagrams.

The input stage of the driver should preferably be driven by a signal with a short rise or fall time. Caution must be exercised whenever the driver is used with slowly varying input signals, especially in situations where the device is located in a separate daughter board or PCB layout has long input connection traces:

- High dI/dt current from the driver output coupled with board layout parasitics can cause ground bounce. Since the device features just one GND pin which may be referenced to the power ground, this may interfere with the differential voltage between Input pins and GND and trigger an unintended change of output state. Because of fast 17 ns propagation delay, this can ultimately result in high-frequency oscillations, which increases power dissipation and poses risk of damage
- 1-V Input threshold hysteresis boosts noise immunity compared to most other industry standard drivers.

If limiting the rise or fall times to the power device to reduce EMI is necessary, then an external resistance is highly recommended between the output of the driver and the power device instead of adding delays on the input signal. This external resistor has the additional benefit of reducing part of the gate charge related power dissipation in the gate driver device package and transferring it into the external resistor itself.

Finally, because of the unique input structure that allows negative voltage capability on the Input and Enable pins, caution must be used in the following applications:

- Input or Enable pins are switching to amplitude > 15 V
- Input or Enable pins are switched at dV/dt > 2 V/ns

If both of these conditions occur, it is advised to add a series 150-Ω resistor for the pin(s) being switched to limit the current through the input structure.

8.3.3 Enable Function

The Enable (EN) pin of the UCC27531-Q1 has an internal pullup resistor to an internal reference voltage so leaving Enable floating turns on the driver and allows it to send output signals properly. If desired, the Enable can also be driven by low-voltage logic to enable and disable the driver.

8.3.4 Output Stage

The output stage of the UCC27531-Q1 device is illustrated in Figure 23. The UCC27531-Q1 device features a unique architecture on the output stage which delivers the highest peak source current when it is most needed during the Miller plateau region of the power switch turn-on transition (when the power switch drain/collector voltage experiences dV/dt). The device output stage features a hybrid pullup structure using a parallel arrangement of N-Channel and P-Channel MOSFET devices. By turning on the N-Channel MOSFET during a narrow instant when the output changes state from low to high, the gate driver device is able to deliver a brief boost in the peak sourcing current enabling fast turn on.

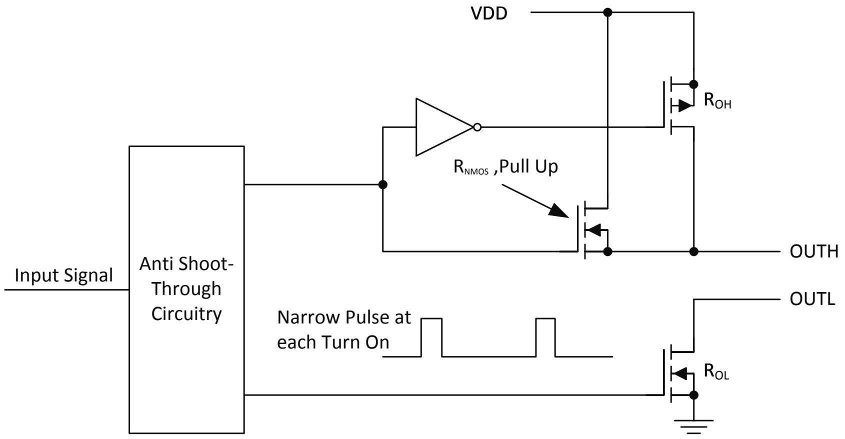


Figure 23. UCC27531-Q1 Gate Driver Output Stage

Feature Description (continued)

Split output depicted in Figure 23. For devices with single OUT pin, OUTH and OUTL are connected internally and then connected to OUT.

The R_{OH} parameter (see *Electrical Characteristics*) is a DC measurement and it is representative of the on-resistance of the P-Channel device only, because the N-Channel device is turned-on only during output change of state from low to high. Thus the effective resistance of the hybrid pullup stage is much lower than what is represented by ROH parameter. The pulldown structure is composed of a N-Channel MOSFET only. The ROL parameter (see *Electrical Characteristics*), which is also a DC measurement, is representative of true impedance of the pulldown stage in the device. In UCC27531-Q1, the effective resistance of the hybrid pullup structure is approximately 3 x R_{OL}.

The UCC27531-Q1 is capable of delivering 2.5-A source, and up to 5-A sink at VDD = 18 V. Strong sink capability results in a very low pulldown impedance in the driver output stage which boosts immunity against the parasitic Miller turn-on (high slew rate dV/dt turn on) effect that is seen in both IGBT and FET power switches .

An example of a situation where Miller turn on is a concern is synchronous rectification (SR). In SR application, the dV/dt occurs on MOSFET drain when the MOSFET is already held in Off state by the gate driver. The current charging the C_{GD} Miller capacitance during this high dV/dt is shunted by the pulldown stage of the driver. If the pulldown impedance is not low enough then a voltage spike can result in the V_{GS} of the MOSFET, which can result in spurious turn on. This phenomenon is illustrated in Figure 24.

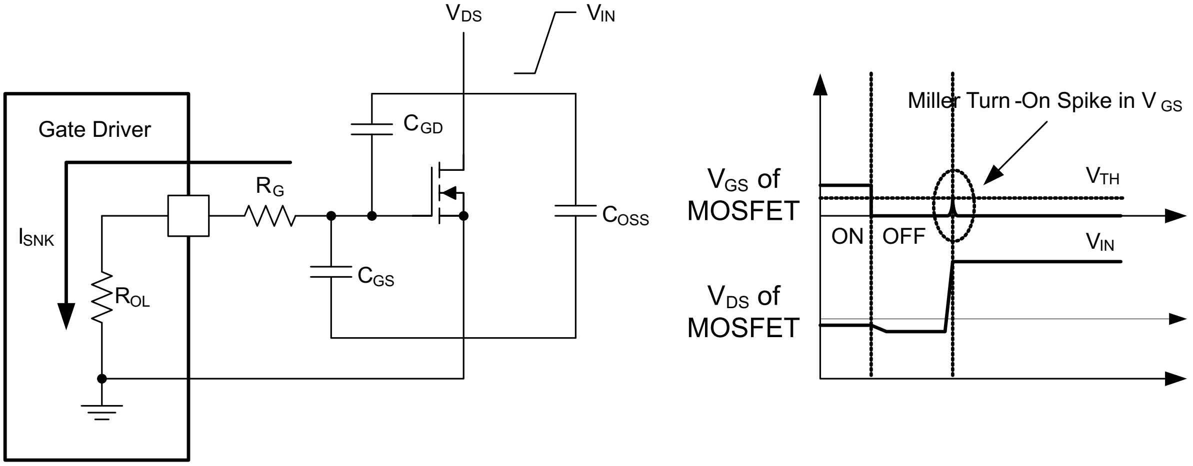


Figure 24. Low Pulldown Impedance in UCC27531-Q1 (Output Stage Mitigates Miller Turn-on Effect)

The driver output voltage swings between VDD and GND providing rail-to-rail operation, thanks to the MOS output stage which delivers very low dropout. The presence of the MOSFET body diodes also offers low impedance to switching overshoots and undershoots. This means that in many cases, external Schottky diode clamps may be eliminated.

8.4 Device Functional Modes

The UCC227531-Q1 device operates in normal mode and UVLO mode (see *VDD UVLO* section for information on UVLO operation). In normal mode, the output state is dependent on the states of the device, and the input pins.

The UCC27531-Q1 features a single, non-inverting input, but also contains enable and disable functionality through the EN pin. Setting the EN pin to logic HIGH will enable the non-inverting input to output on the IN pin. The device uses a split output (OUTH, and OUTL) to allow for separate sourcing and sinking pins, which can help reduce ground de-bouncing.

Table 2. UCC27531QDBVRQ1 Input/Output Logic Truth Table (For Single Output Driver)

IN PIN	EN PIN	OUTH PIN	OUTL PIN	OUT (OUTH and OUTL pins tied together)
L	L	High-impedance	L	L
L	H	High-impedance	L	L
H	L	High-impedance	L	L
H	H	H	High-impedance	H
H	FLOAT	H	High-impedance	H
FLOAT	H	High-impedance	L	L

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

High-current gate driver devices are required in switching power applications for a variety of reasons. In order to enable fast switching of power devices and reduce associated switching power losses, a powerful gate driver can be employed between the PWM output of controllers or signal isolation devices and the gates of the power semiconductor devices. Further, gate drivers are indispensable when sometimes it is just not feasible to have the PWM controller directly drive the gates of the switching devices. The situation is encountered often because the PWM signal from a digital controller or signal isolation device is often a 3.3-V or 5-V logic signal which is not capable of effectively turning on a power switch. A level shifting circuitry is needed to boost the logic-level signal to the gate-drive voltage in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar, (or p- n-channel MOSFET), transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate for this because they lack level-shifting capability and low-drive voltage protection. Gate drivers effectively combine both the level-shifting, buffer drive and UVLO functions. Gate drivers also find other needs such as minimizing the effect of switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses into itself.

The UCC27531-Q1 is very flexible in this role with a strong current drive capability and wide supply voltage range up to 32 V. This allows the driver to be used in 12-V Si MOSFET applications, 20-V and –5-V (relative to Source) SiC FET applications, 15-V and –15-V(relative to Emitter) IGBT applications and many others. As a single-channel driver, the UCC27531-Q1 can be used as a low-side or high-side driver. To use as a low-side driver, the switch ground is usually the system ground so it can be connected directly to the gate driver. To use as a high-side driver with a floating return node however, signal isolation is needed from the controller as well as an isolated bias to the UCC27531-Q1. Alternatively, in a high-side drive configuration the UCC27531-Q1 can be tied directly to the controller signal and biased with a non-isolated supply. However, in this configuration the outputs of the UCC27531-Q1 need to drive a pulse transformer which then drives the power-switch to work properly with the floating source and emitter of the power switch. Further, having the ability to control turn-on and turn-off speeds independently with both the OUTH and OUTL pins ensures optimum efficiency while maintaining system reliability. These requirements coupled with the need for low propagation delays and availability in compact, low-inductance packages with good thermal capability makes gate driver devices such as the UCC27531-Q1 extremely important components in switching power combining benefits of high-performance, low cost, component count and board space reduction and simplified system design.

9.2 Typical Applications

9.2.1 Driving IGBT Without Negative Bias

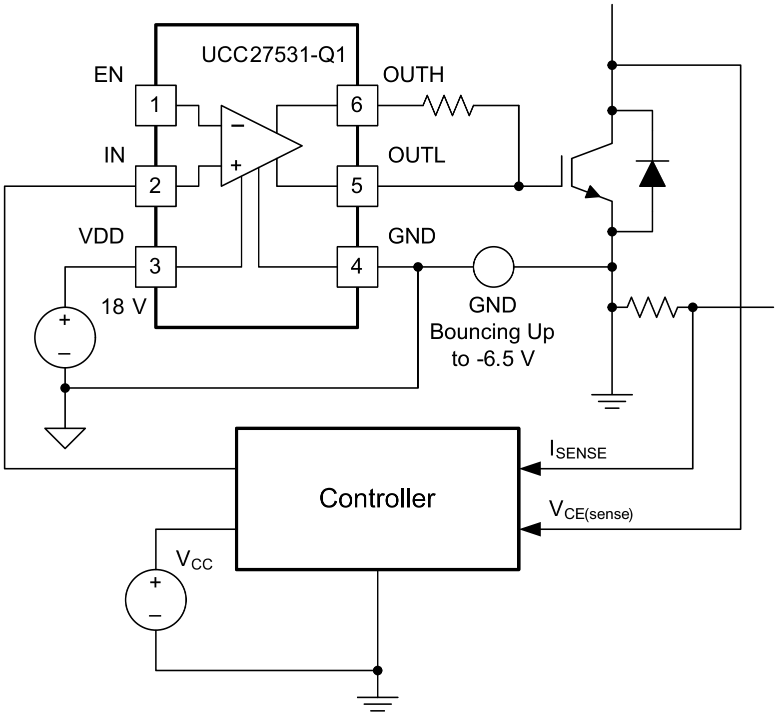


Figure 25. Driving IGBT Without Negative Bias

9.2.1.1 Design Requirements

When selecting the proper gate driver device for an end application, some design considerations must be evaluated first in order to make the most appropriate selection. The following design parameters should be used when selecting the proper gate driver device for an end application: input-to-output configuration, the input threshold type, bias supply voltage levels, peak source and sink currents, availability of independent enable and disable functions, propagation delay, power dissipation, and package type. See the example design parameters and requirements in Table 3.

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
IN-OUT configuration	Noninverting
Input threshold type	CMOS
Bias supply voltage levels	+18 V
Negative output low voltage	N/A
dVDS/dt(1)	20 V/ns
Enable function	Yes
Disable function	N/A
Propagation delay	<30 ns
Power dissipation	<0.25 W
Package type	DBV

(1) dVDS/dt is a typical requirement for a given design. This value can be used to find the peak source/sink currents needed as shown in *Peak Source and Sink Currents*.

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Input-to-Output Configuration

See the *Device Functional Modes* section for information on individual device functionality.

9.2.1.2.2 Input Threshold Type

The type of Input voltage threshold determines the type of controller that can be used with the gate driver device. The UCC27531-Q1 device features a TTL and CMOS-compatible input threshold logic, with wide hysteresis. The threshold voltage levels are low voltage and independent of the VDD supply voltage, which allows compatibility with both logic-level input signals from microcontrollers as well as higher-voltage input signals from analog controllers. See the *Electrical Characteristics* table for the actual input threshold voltage levels and hysteresis specifications for the UCC227531-Q1 device.

9.2.1.2.3 VDD Bias Supply Voltage

The bias supply voltage to be applied to the VDD pin of the device should never exceed the values listed in the *Recommended Operating Conditions* table. However, different power switches demand different voltage levels to be applied at the gate terminals for effective turnon and turnoff. With certain power switches, a positive gate voltage may be required for turnon and a negative gate voltage may be required for turnoff, in which case the VDD bias supply equals the voltage differential. With an operating range from 10 V to 32 V, the UCC227531-Q1 device can be used to drive a power switches such as power MOSFETS and IGBTs (VGE = 15 V, 18 V).

9.2.1.2.4 Peak Source and Sink Currents

Generally, the switching speed of the power switch during turnon and turnoff should be as fast as possible to minimize switching power losses. The gate driver device must be able to provide the required peak current for achieving the targeted switching speeds for the targeted power MOSFET.

Using the example of a power MOSFET, the system requirement for the switching speed is typically described in terms of the slew rate of the drain-to-source voltage of the power MOSFET (such as dVDS/dt). For example, the system requirement might state that a SPP20N60C3 power MOSFET must be turned on with a dVDS/dt of 20 V/ns or higher under a DC bus voltage of 400 V in a continuous-conduction-mode (CCM) boost PFC-converter application. This type of application is an inductive hard-switching application and reducing switching power losses is critical. This requirement means that the entire drain-to-source voltage swing during power MOSFET turn-on event (from 400 V in the OFF state to VDS(on) in on state) must be completed in approximately 20 ns or less. When the drain-to-source voltage swing occurs, the Miller charge of the power MOSFET (QGD parameter in SPP20N60C3 power MOSFET data sheet = 33 nC typical) is supplied by the peak current of gate driver. According to power MOSFET inductive switching mechanism, the gate-to-source voltage of the power MOSFET at this time is the Miller plateau voltage, which is typically a few volts higher than the threshold voltage of the power MOSFET, VGS(TH).

To achieve the targeted dVDS/dt, the gate driver must be capable of providing the QGD charge in 20 ns or less. In other words a peak current of 1.65 A (= 33 nC / 20 ns) or higher must be provided by the gate driver. The UCC27531-Q1 series of gate drivers can provide 2.5-A peak sourcing current, and 5A peak sinking current which clearly exceeds the design requirement and has the capability to meet the switching speed needed. The 1.5x sourcing, and 3x sinking overdrive capability provides an extra margin against part-to-part variations in the QGD parameter of the power MOSFET along with additional flexibility to insert external gate resistors and fine tune the switching speed for efficiency versus EMI optimizations. However, in practical designs the parasitic trace inductance in the gate drive circuit of the PCB will have a definitive role to play on the power MOSFET switching speed. The effect of this trace inductance is to limit the dI/dt of the output current pulse of the gate driver. To illustrate this, consider output current pulse waveform from the gate driver to be approximated to a triangular profile, where the area under the triangle (½ ×IPEAK × time) would equal the total gate charge of the power MOSFET (QG parameter in SPP20N60C3 power MOSFET datasheet = 87 nC typical). If the parasitic trace inductance limits the dI/dt then a situation may occur in which the full peak current capability of the gate driver is not fully achieved in the time required to deliver the QG required for the power MOSFET switching. In other words, the time parameter in the equation would dominate and the IPEAK value of the current pulse would be much less than the true peak current capability of the device, while the required QG is still delivered. Because of this, the desired switching speed may not be realized, even when theoretical calculations indicate the gate driver can achieve the targeted switching speed. Thus, placing the gate driver device very close to the power MOSFET and designing a tight gate drive-loop with minimal PCB trace inductance is important to realize the full peak-current capability of the gate driver.

9.2.1.2.5 Enable and Disable Function

Certain applications demand independent control of the output state of the driver without involving the input signal. A pin which offers an enable and disable function achieves this requirement. For these applications, the UCC27531-Q1 is suitable as it features an input pin and an Enable pin.

9.2.1.2.6 Propagation Delay

The acceptable propagation delay from the gate driver is dependent on the switching frequency at which it is used and the acceptable level of pulse distortion to the system. The UCC27531-Q1 device features 17-ns (typical) propagation delay which ensures very little pulse distortion and allows operation at very higher frequencies.

9.2.1.2.7 Power Dissipation

Power dissipation of the gate driver has two portions as shown in Equation 1.

$$P_{DISS} = P_{DC} + P_{SW} \tag{1}$$

The DC portion of the power dissipation is $P_{DC} = I_Q \times VDD$ where I_Q is the quiescent current for the driver. The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections etc and also any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of parasitic capacitances, parasitic shoot-through). The UCC27531-Q1 features very low quiescent currents (less than 1 mA) and contains internal logic to eliminate any shoot-through in the output driver stage. Thus the effect of the P_{DC} on the total power dissipation within the gate driver can be safely assumed to be negligible. In practice this is the power consumed by driver when its output is disconnected from the gate of power switch.

The power dissipated in the gate driver package during switching (P_{SW}) depends on the following factors:

- Gate charge required of the power device (usually a function of the drive voltage V_G, which is very close to input bias supply voltage VDD due to low V_{OH} drop-out)
- Switching frequency
- Use of external gate resistors

When a driver device is tested with a discrete, capacitive load it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given in Equation 2.

$$E_G = \frac{1}{2} C_{LOAD} V_{DD}^2$$

where

- C_{LOAD} is load capacitor and V_{DD} is bias voltage feeding the driver. (2)

There is an equal amount of energy dissipated when the capacitor is discharged. During turn off the energy stored in capacitor is fully dissipated in drive circuit. This leads to a total power loss during switching cycle given by Equation 3.

$$P_G = C_{LOAD} V_{DD}^2 f_{sw}$$

where

- f_{SW} is the switching frequency (3)

The switching load presented by a power FET and IGBT can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications of typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_g, one can determine the power that must be dissipated when charging a capacitor. This is done by using the equivalence, $Q_g = C_{LOAD}V_{DD}$, to provide Equation 4 for power

$$P_G = C_{LOAD} V_{DD}^2 f_{sw} = Q_g V_{DD} f_{sw} \tag{4}$$

This power P_G is dissipated in the resistive elements of the circuit when the MOSFET and IGBT is being turned on or off. Half of the total power is dissipated when the load capacitor is charged during turn-on, and the other half is dissipated when the load capacitor is discharged during turn-off. When no external gate resistor is employed between the driver and MOSFET and IGBT, this power is completely dissipated inside the driver package. With the use of external gate drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistances (more power dissipated in the higher resistance component). Based on this simplified analysis, the driver power dissipation during switching is calculated in Equation 5.

$$P_{SW} = 0.5 \times Q_g \times V_{DD} \times f_{sw} \left(\frac{R_{OFF}}{(R_{OFF} + R_{GATE})} + \frac{R_{ON}}{(R_{ON} + R_{GATE})} \right)$$

where

- $R_{OFF} = R_{OL}$ and R_{ON} (effective resistance of pullup structure) = 3 x R_{OL} (5)

9.2.1.3 Application Curves

Figure 26, Figure 27 and Figure 28 were observed using the UCC27531-Q1 on the UCC27531EVM-184.

NOTE

Legend: Green: EVM PWM Input, Blue: UCC27531-Q1 IN, Red: EVM GATE Output

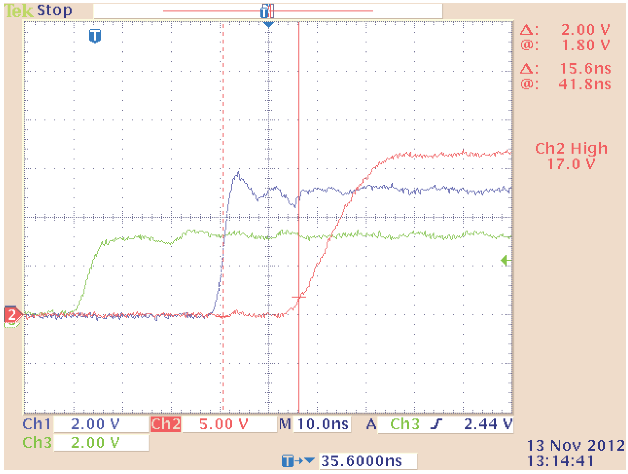


Figure 26. UCC27531-Q1 Input vs. Output PWM Propagation Delay (High)

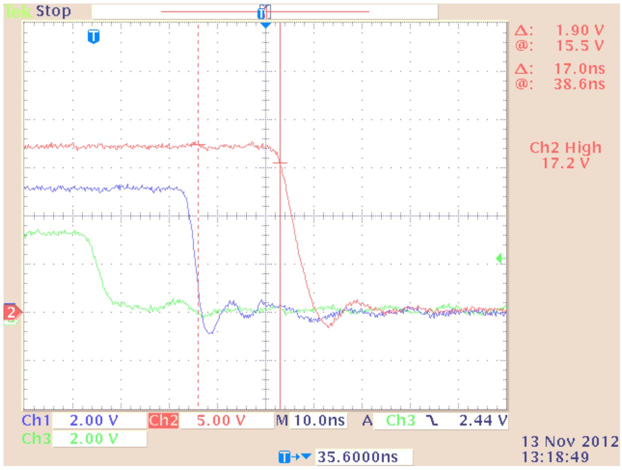


Figure 27. UCC27531-Q1 Input vs. Output PWM Propagation Delay (Low)

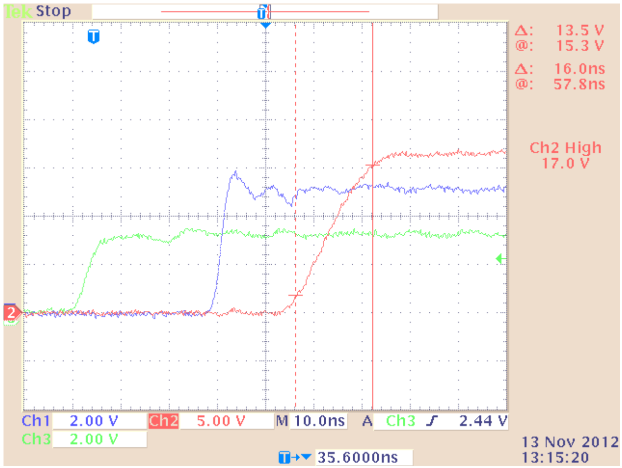


Figure 28. UCC27531-Q1 Input vs. Output PWM Rise Time

9.2.2 Driving IGBT With 13-V Negative Turn-Off Bias

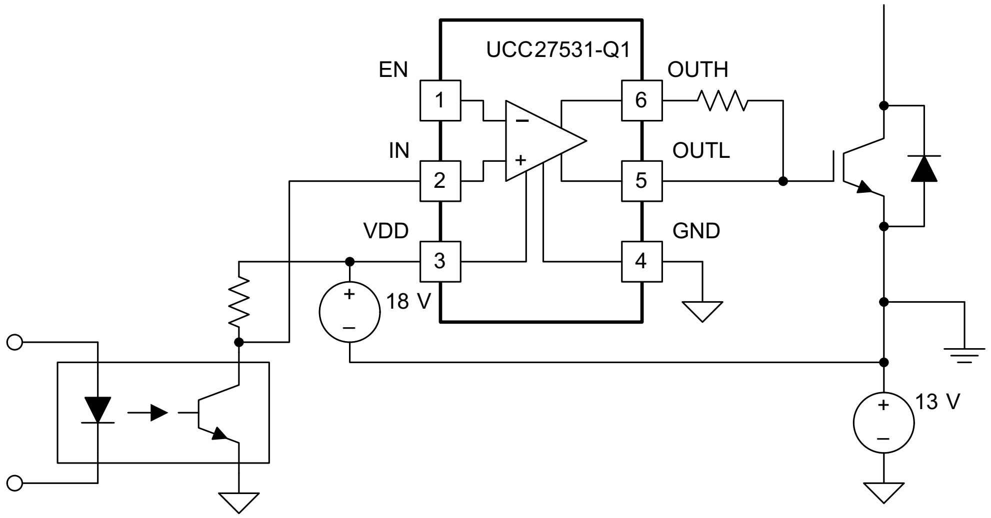


Figure 29. Driving IGBT With 13-V Negative Turn-Off Bias

9.2.2.1 Design Requirements

Refer to the previous *Design Requirements* section.

9.2.2.2 Detailed Design Procedure

Refer to the previous *Detailed Design Procedure* section.

9.2.2.3 Application Curves

Refer to the previous *Application Curves* section.

9.2.3 Using UCC27531-Q1 Drivers in an Inverter

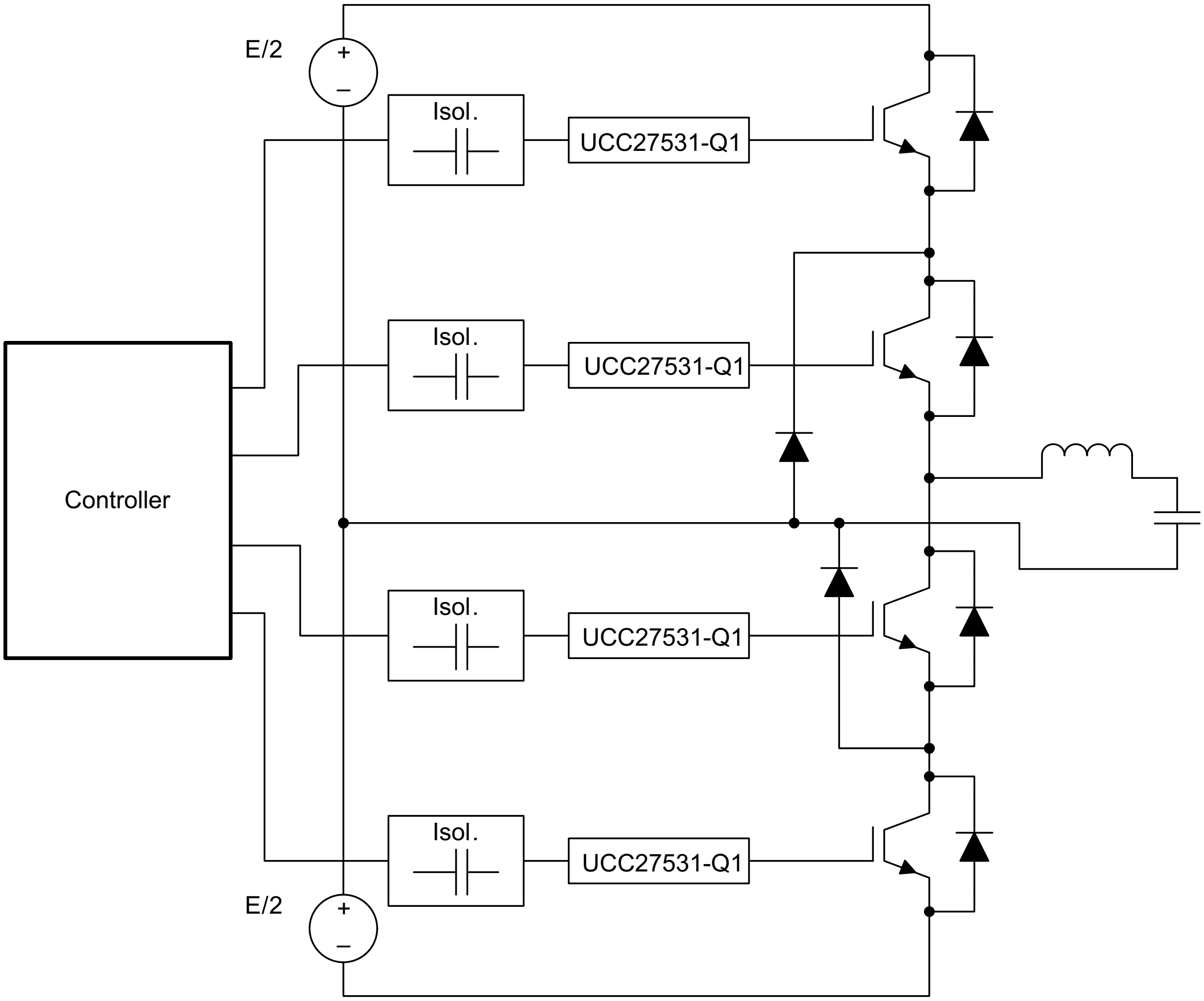


Figure 30. Using UCC27531-Q1 Drivers in an Inverter

9.2.3.1 Design Requirements

Refer to the previous *Design Requirements* section.

9.2.3.2 Detailed Design Procedure

Refer to the previous *Detailed Design Procedure* section.

9.2.3.3 Application Curves

Refer to the previous *Application Curves* section.

10 Power Supply Recommendations

The bias supply voltage range for which the UCC2753x devices are rated to operate is from 10 V to 32 V. The lower end of this range is governed by the internal UVLO protection feature on the VDD pin supply circuit blocks. Whenever the driver is in UVLO condition when the VDD pin voltage is below the V(ON) supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 35-V absolute maximum voltage rating of the VDD pin of the device (which is a stress rating). Keeping a 3-V margin to allow for transient voltage spikes, the maximum recommended voltage for the VDD pin is 32 V.

The UVLO protection feature also involves a hysteresis function. This means that when the VDD pin bias voltage has exceeded the threshold voltage and device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification VDD(hys). Therefore, ensuring that, while operating at or near the 9.8 V range, the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device is important to avoid triggering device shutdown.

During system shutdown, the device operation continues until the VDD pin voltage has dropped below the V(OFF) threshold which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system start-up, the device does not begin operation until the VDD pin voltage has exceeded above the V(ON) threshold. The quiescent current consumed by the internal circuit blocks of the device is supplied through the VDD pin. Although this fact is well known, recognizing that the charge for source current pulses delivered by the OUT pin is also supplied through the same VDD pin is important. As a result, every time a current is sourced out of the output pin (OUT), a corresponding current pulse is delivered into the device through the VDD pin. Thus ensuring that local bypass capacitors are provided between the VDD and GND pins and located as close to the device as possible for the purpose of decoupling is important. A low-ESR, ceramic surface-mount capacitor is mandatory.

11 Layout

11.1 Layout Guidelines

Proper PCB layout is extremely important in a high current, fast switching circuit to provide appropriate device operation and design robustness. The UCC27531-Q1 gate driver incorporates short propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of power switch to facilitate voltage transitions very quickly. At higher VDD voltages, the peak current capability is even higher (2.5-A and 5-A peak current is at VDD = 18 V). Very high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit layout guidelines are strongly recommended when designing with these high-speed drivers.

- Locate the driver device as close as possible to power device in order to minimize the length of high-current traces between the driver Output pins and the gate of the power switch device.
- Locate the VDD bypass capacitors between VDD and GND as close as possible to the driver with minimal trace length to improve the noise filtering. These capacitors support high peak current being drawn from VDD during turn-on of power switch. The use of low inductance SMD components such as chip resistors and chip capacitors is highly recommended.
- The turn-on and turn-off current loop paths (driver device, power switch and VDD bypass capacitor) should be minimized as much as possible in order to keep the stray inductance to a minimum. High di/dt is established in these loops at two instances – during turn-on and turn-off transients, which induces significant voltage transients on the output pins of the driver device and gate of the power switch.
- Wherever possible, parallel the source and return traces of a current loop, taking advantage of flux cancellation
- Separate power traces and signal traces, such as output and input signals.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver should be connected to the other circuit nodes such as source of power switch, ground of PWM controller etc at one, single point. The connected paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT may corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well.

11.2 Layout Example

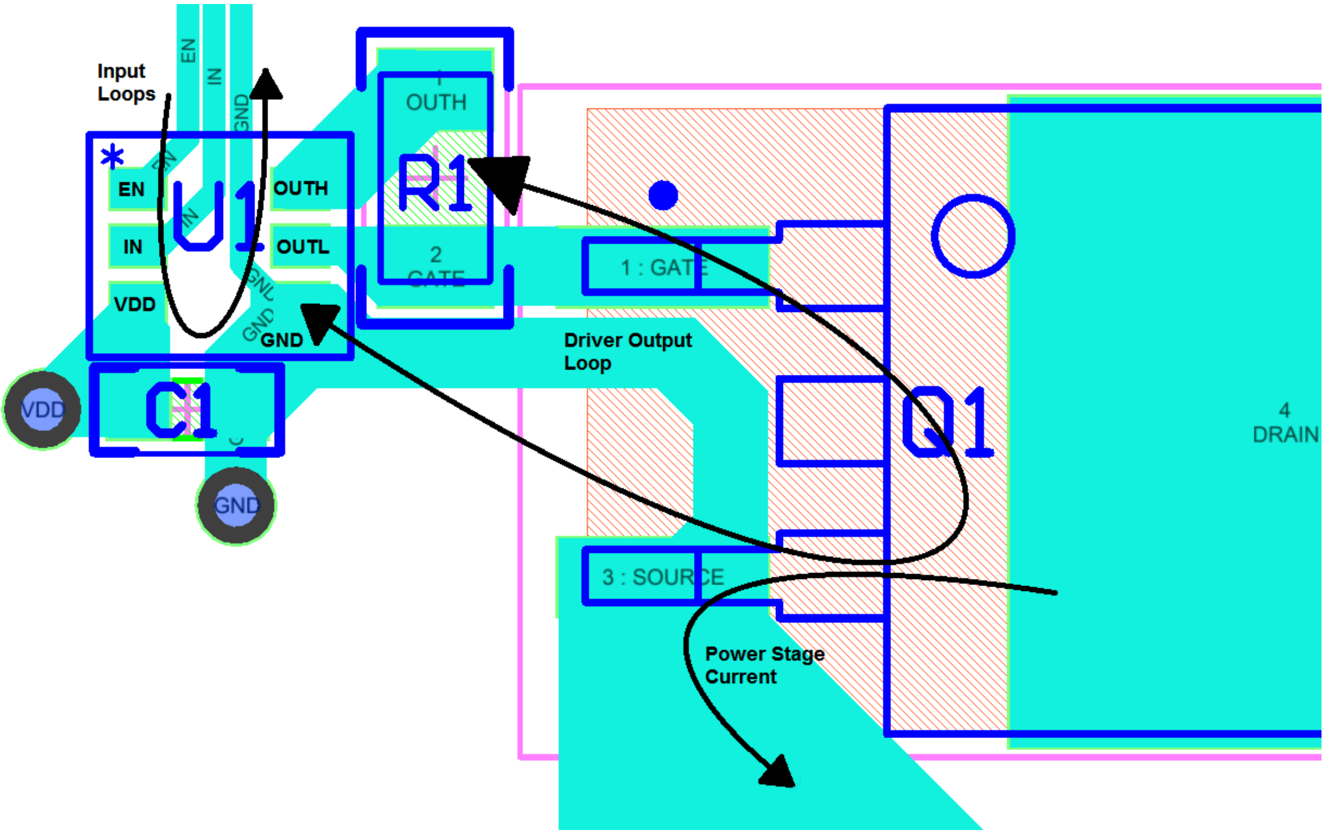


Figure 31. UCC27531-Q1 Layout Example

11.3 Thermal Considerations

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the package. In order for a gate driver to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The thermal metrics for the driver package are summarized in the *Thermal Information* section of the datasheet. For detailed information regarding the thermal information table, please refer to the TI Application Note, *Semiconductor and IC Package Thermal Metrics* (SPRA953).

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27531QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	EAHQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UCC27531-Q1 :

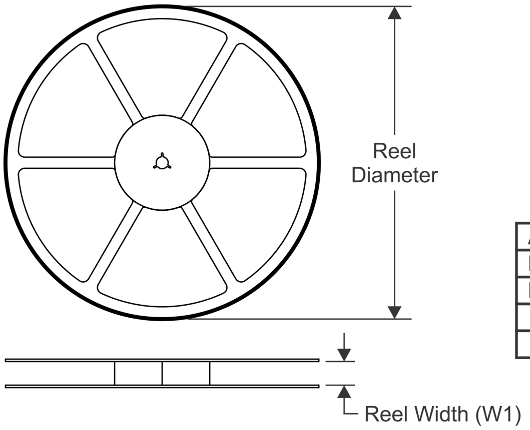
- Catalog: UCC27531

NOTE: Qualified Version Definitions:

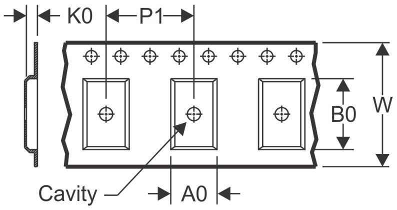
  - Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

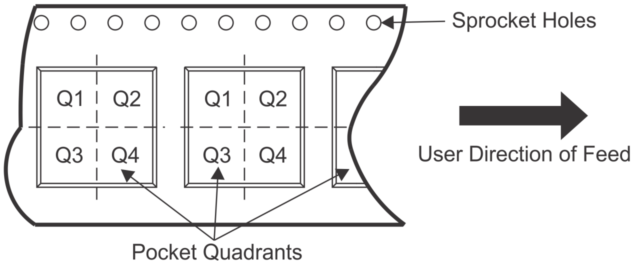


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

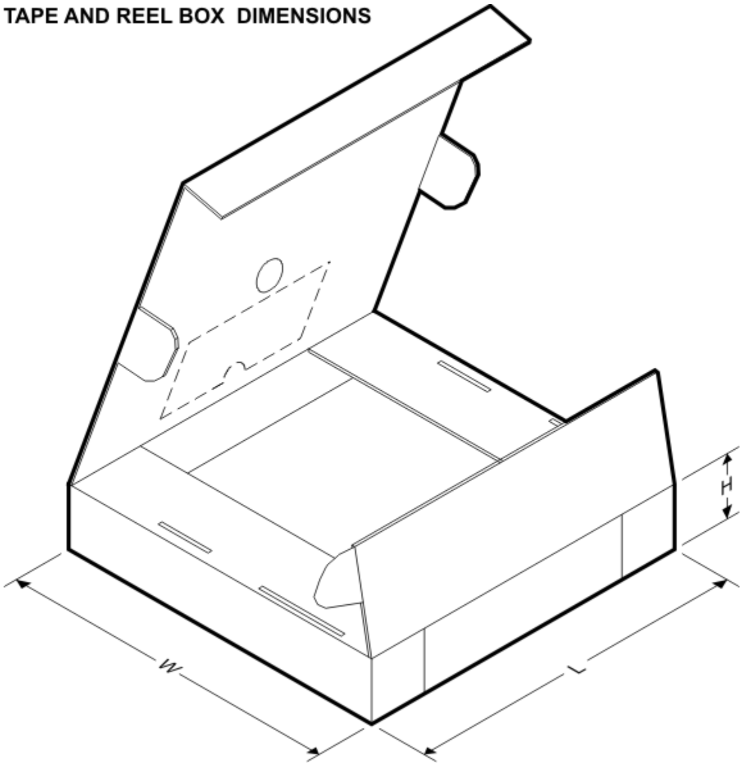
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

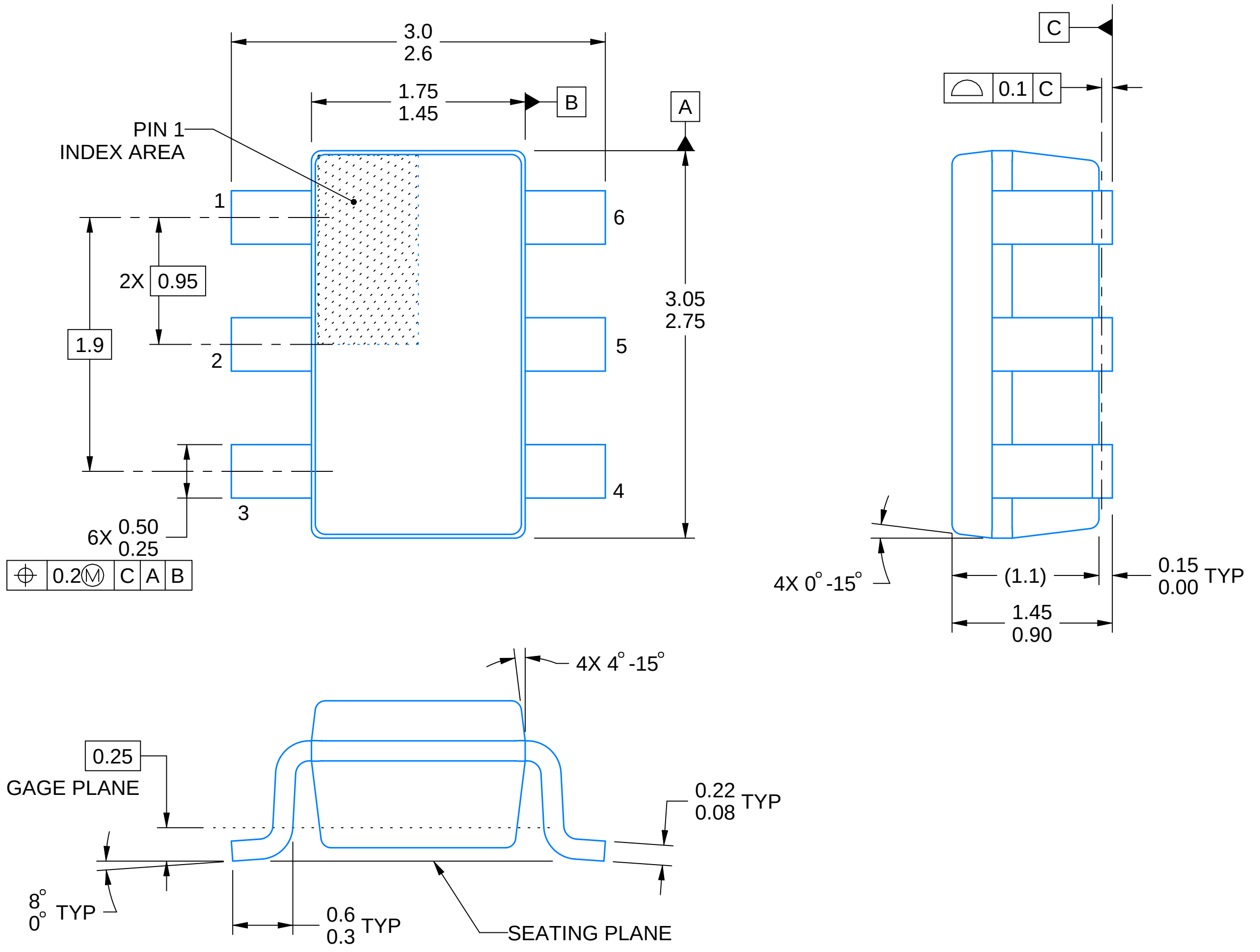
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27531QDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27531QDBVRQ1	SOT-23	DBV	6	3000	180.0	180.0	18.0



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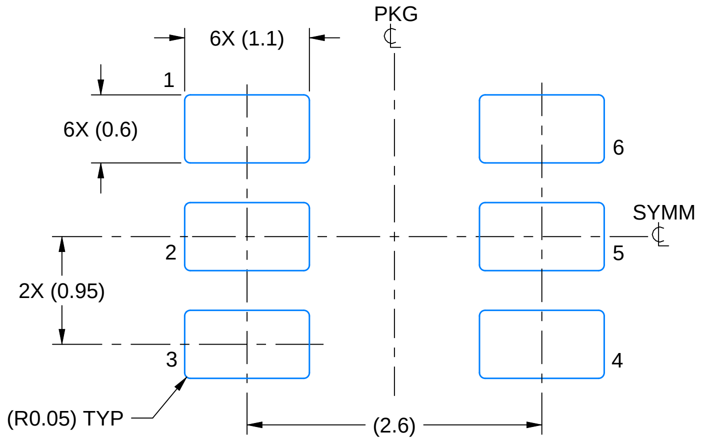
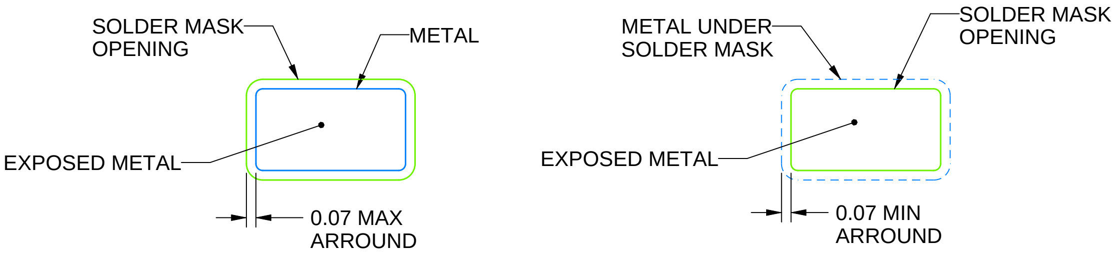
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

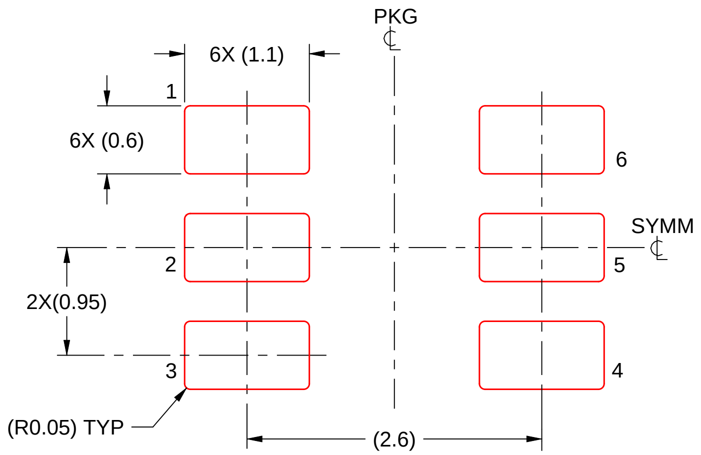
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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