UCC27614-Q1 30V、10A シングル チャネル、ローサイド ゲート ドライバ、-10V 入力機能付き、車載用アプリケーション向け

1 特長

- 車載アプリケーション用に認定済み
- AEC-Q100 認定済み
  - デバイス温度グレード 1
- 10A シンク、10A ソース出力電流 (標準値)
- –10V まで耐える入力およびイネーブル ピン
- VDD 電圧の絶対最大値:30 V
- 4.5V～26V の広い VDD 動作範囲 (UVLO 付き)
- 2mm × 2mm の SON8 パッケージで供給されます
- 伝搬遅延時間:17.5ns (標準値)
- EN (イネーブル) ピン (SOIC8 および VSSOP8 パッケージの場合)
- イネーブル / ディセーブル機能として使用可能な IN ピン (SON8 パッケージの場合)
- VDD と無関係な入力スレッショルド (TTL 互換)
- 反転または非反転ドライバとして使用可能
- 動作時の接合部温度範囲:–40℃～150℃

2 アプリケーション

- テレコムのスイッチ モード電源
- 力率改善 (PFC) 回路
- ソーラー電源
- モータドライブ
- 高周波ライン ドライバ
- パルス トランス ドライバ
- ハイパワー バッファ

3 概要

UCC27614-Q1 は、MOSFET、IGBT、SiC、GaN パワー スイッチを効率的に駆動できるシングル チャネル高速ローサイド ゲート ドライバです。UCC27614-Q1 は 10A (代表値) のピーク駆動能力を持っています。これにより、パワー スイッチの立ち上がり / 立ち下がり時間を短縮し、スイッチング損失を低減し、効率を向上させます。UCC27614-Q1 は、伝搬遅延が小さく、システムのデッドタイム最適化、パルス幅利用率、制御ループ応答、過渡性能の改善により、電力段の効率を向上させます。

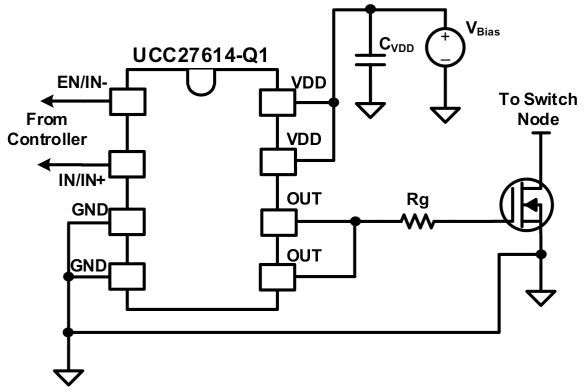
UCC27614-Q1 は、入力で -10V を扱えるため、中程度のグランド バウンスが発生するシステムの堅牢性を向上させることができます。これらの入力は電源電圧の影響を受けず、ほとんどのコントローラ出力に接続できるため、制御の柔軟性を最大限に高めることができます。独立したイネーブル信号を使うと、メイン制御ロジックとは無関係に電力段を制御できます。システムでフォルトが発生した場合 (パワー トレインをオフにする必要がある場合)、ゲート ドライバは電力段を素早く遮断できます。イネーブル機能は、システムの堅牢性も向上させます。多くの高周波スイッチング電源では、電源デバイスのゲートに高周波ノイズを生じさせます。このノイズがゲート ドライバの出力ピンに注入され、ドライバを誤動作させる可能性があります。UCC27614-Q1 は、その過渡逆電流および逆電圧特性により、そのような条件でも優れた性能を発揮します。

規定された UVLO スレッショルドを VDD 電圧が下回ると、強力な内部プルダウン MOSFET が出力を LOW に保持します。このアクティブ プルダウン機能は、システムの堅牢性をさらに向上させます。2mm × 2mm のパッケージに収容された UCC27614-Q1 は、10A の駆動電流を備えており、システムの電力密度を向上させます。この小型パッケージは、ゲート ドライバの配置の最適化とレイアウトの改善も可能にします。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)	本体サイズ (公称)
UCC27614-Q1	DSG (SON 8)	2.0mm × 2.0mm	2.0 mm × 2.0mm
UCC27614-Q1	D (SOIC 8)	4.9mm × 6mm	4.9mm × 3.9mm
UCC27614-Q1	DGN (VSSOP 8)	3.0mm × 4.9mm	3.0 mm × 3.0mm

(1) 供給されているすべてのパッケージについては、セクション 12 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



アプリケーション概略図

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4 Pin Configuration and Functions

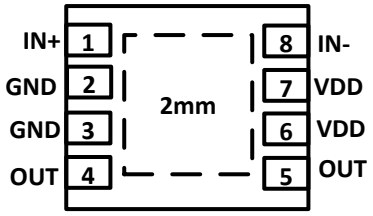


図 4-1. DSG Package 8-Pin SON Top View

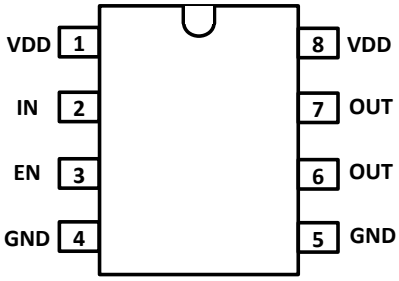


図 4-2. D Package 8-Pin SOIC Top View

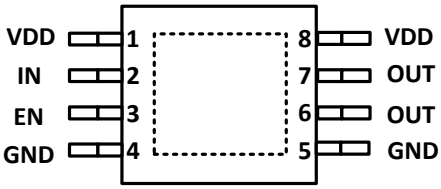


図 4-3. DGN Package 8-Pin VSSOP Top View

表 4-1. Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	DSG NO.	D DGN NO.		
GND	2,3	4,5	G	Device ground or reference
EN	—	3	I	Enable or disable control pin. If not used, connect to VDD.
IN	—	2	I	Non-inverting PWM input
IN+	1	—	I	Non-inverting PWM input. If not used, connect to VDD.
IN-	8	—	I	Inverting PWM input. If not used, connect to GND.
OUT	4,5	6,7	O	Output of the driver
VDD	6,7	1,8	P	Driver bias supply. Connect the positive node of the voltage source to this pin through an impedance for high common mode noise rejection. Bypass this pin with two ceramic capacitors, generally >=1 µF and 0.1 µF, which are referenced to GND pin of this device.
	Thermal Pad	Thermal Pad(2)	—	Connect to GND through large copper plane. This pad is not a low-impedance path to GND.

(1) I/O = Digital input/output, IA = Analog input, AO= Analog output, P = Power connection
(2) Applies to DGN package.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

		MIN	MAX	UNIT
Supply voltage	VDD	–0.3	30	V
Output Voltage (DC)	VOUT	–0.3	VDD +0.3	V
Output Voltage (200-ns Pulse)	VOUT	–2	VDD +3	V
Input Voltage IN, EN, IN+, IN–		–10	30	V
Operating junction temperature, T_J		–40	150	°C
Lead temperature	Soldering, 10 s		300	°C
	Reflow		260	
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. See *セクション 5.4* of the data sheet for thermal limitations and considerations of packages.
(3) These devices are sensitive to electrostatic discharge; follow proper device handling procedures.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range. All voltages are with reference to GND (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, VDD	4.5	12	26	V
Input voltage, IN, IN+, IN-, EN	–10		26	V
Output Voltage, OUT	0		VDD	V
Operating junction temperature, T_J	–40		150	°C

5.4 Thermal Information

THERMAL METRIC(1)		UCC27614			UNIT
		DSG (SON)	DGN (VSSOP)	D (SOIC)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	67.9	48.9	126.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	81.1	71.8	67.0	
$R_{\theta JB}$	Junction-to-board thermal resistance	33.4	22.3	69.9	
ψ_{JT}	Junction-to-top characterization parameter	2.4	2.6	19.2	
ψ_{JB}	Junction-to-board characterization parameter	33.4	22.3	69.1	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	12.2	4.5	n/a	

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics Application Report* (SPRA953).

5.5 Electrical Characteristics

Unless otherwise noted, VDD = 12 V, $T_A = T_J$ = –40°C to 150°C, 1-µF capacitor from VDD to GND, No load on the output. Typical condition specifications are at 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS CURRENTS						
I_{VDDq}	VDD quiescent supply current	V_{IN+}/V_{IN} = 3.3 V, V_{IN-} = 0 V, EN=VDD, VDD = 3.4 V		305	500	µA
I_{VDD}	VDD static supply current	V_{IN+}/V_{IN} = 3.3 V, V_{IN-} = 0 V, EN = VDD		0.64	0.92	mA
I_{VDD}	VDD static supply current	V_{IN+}/V_{IN} = 0 V, V_{IN-} = 0 V, EN = VDD		0.71	1.0	mA
I_{VDDO}	VDD dynamic operating current	f_{SW} = 1000 kHz, EN = VDD, V_{IN+}/V_{IN} = 0 V to 3.3 V PWM, V_{IN-} = 0 V			4.0	mA
I_{DIS}	VDD disable current	V_{IN+}/V_{IN} = 0 V, V_{IN-} = 3.3 V, EN = 0 V		0.75	1.0	mA
UNDERVOLTAGE LOCKOUT (UVLO)						
V_{VDD_ON}	VDD UVLO rising threshold		3.8	4.1	4.4	V
V_{VDD_OFF}	VDD UVLO falling threshold		3.5	3.8	4.1	V
V_{VDD_HYS}	VDD UVLO hysteresis			0.3		V
INPUT (IN, IN+)						
V_{IN_H}	Input signal high threshold, output high	Output high, IN- = LOW, EN=HIGH	1.8	2	2.3	V
V_{IN_L}	Input signal low threshold, output low	Output low, IN- = LOW, EN=HIGH	0.8	1	1.2	V
V_{IN_HYS}	Input signal hysteresis			1		V
R_{IN}	INx pin Pulldown resistance	IN+/IN = 3.3 V		120		kΩ
INPUT (IN-)						
V_{IN-_H}	Input signal high threshold, output low	Output low, IN+ = HIGH, EN = high	1.8	2	2.3	V
V_{IN-_L}	Input signal low threshold, output high	Output high, IN+ = HIGH, EN = high	0.8	1	1.2	V
V_{IN-_HYS}	Input signal hysteresis			1		V
R_{IN-}	IN- pin pullup resistance	IN- = 0 V		200		kΩ
ENABLE (EN)						
V_{EN_H}	Enable signal high threshold	Output high, IN+/IN = high, IN- =0 V	1.8	2	2.3	V
V_{EN_L}	Enable signal low threshold	Output low, IN+/IN = high, IN- = 0 V	0.8	1	1.2	V
V_{EN_HYS}	Enable signal hysteresis			1		V
R_{EN}	EN pin pullup resistance	EN = 0 V		200		kΩ
OUTPUT (OUT)						
I_{SRC} (1)	Peak output source current	VDD = 12 V, C_{VDD} = 10 µF, C_L = 0.1 µF, f = 1 kHz		10		A
I_{SNK} (1)	Peak output sink current	VDD = 12 V, C_{VDD} = 10 µF, C_L = 0.1 µF, f = 1 kHz		–10		A
R_{OH} (2)	OUTH, pullup resistance	I_{OUT} = –50 mA See: セクション 6.3.4		2.5	4.5	Ω
R_{OL}	OUTL, pulldown resistance	I_{OUT} = 50 mA		0.34	0.55	Ω

(1) Parameter not tested in production.
(2) Output pullup resistance here is a DC measurement that measures resistance of PMOS structure only, not N-channel structure.

5.6 Switching Characteristics

Unless otherwise noted, VDD = V_{EN} = 12 V, IN- = GND, T_A = T_J = –40°C to 150°C, 1-µF capacitor from VDD to GND, No load on the output. Typical condition specifications are at 25°C (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R	Rise time	C_{LOAD} = 1.8 nF, 20% to 80%, V_{IN} = 0 V to 3.3 V		4.5	6	ns
t_F	Fall time	C_{LOAD} = 1.8 nF, 90% to 10%, V_{IN} = 0 V to 3.3 V		4	5.5	ns
t_{D1}	Turnon propagation delay	C_{LOAD} = 1.8 nF, V_{IN_H} of the input rise to 10% of output rise, V_{IN} = 0 V to 3.3 V, Fsw=500 kHz, 50% duty cycle, T_J = 125°C		17.5	27	ns
t_{D2}	Turn-off propagation delay	C_{LOAD} = 1.8 nF, V_{IN_L} of the input fall to 90% of output fall, V_{IN} = 0 V to 3.3 V, Fsw=500 kHz, 50% duty cycle, T_J = 125°C		17.5	27	ns
t_{PD_EN}	Enable propagation delay	C_{LOAD} = 1.8 nF, V_{EN_H} of the enable rise to 10% of output rise, V_{IN} = 0 V to 3.3 V, Fsw=500 kHz, 50% duty cycle, T_J = 125°C		17.5	27	ns
t_{PD_DIS}	Disable propagation delay	C_{LOAD} = 1.8 nF, V_{EN_L} of the enable fall to 90% of output fall, V_{IN} = 0 V to 3.3 V, Fsw = 500 kHz, 50% duty cycle, T_J = 125°C		17.5	27	ns
t_{VDD+_OUT}	VDD UVLO ON delay	VDD = 0 V to 4.5 V in 100 ns. Measured delay from VDD = 4.5 V to 10% of OUT		3.2	6	µs
t_{VDD-_OUT}	VDD UVLO OFF delay	VDD = 4.5 V to 3.4 V in 100 ns. Measured delay from VDD = 3.4 V to 90% of OUT			7.5	us
t_{PWmin}	Minimum input pulse width that passes to the output	C_{LOAD} = 1.8 nF, V_{IN} = 0 V to 3.3 V, Fsw = 500 kHz, Vo > 1.5 V		9	15	ns

(1) Switching parameters are not tested in production.

5.7 Timing Diagrams

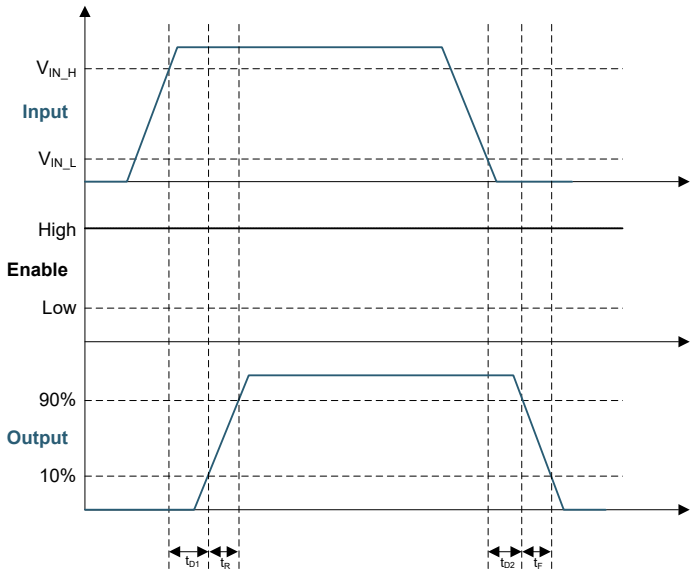


図 5-1. Single Input Version, IN = PWM

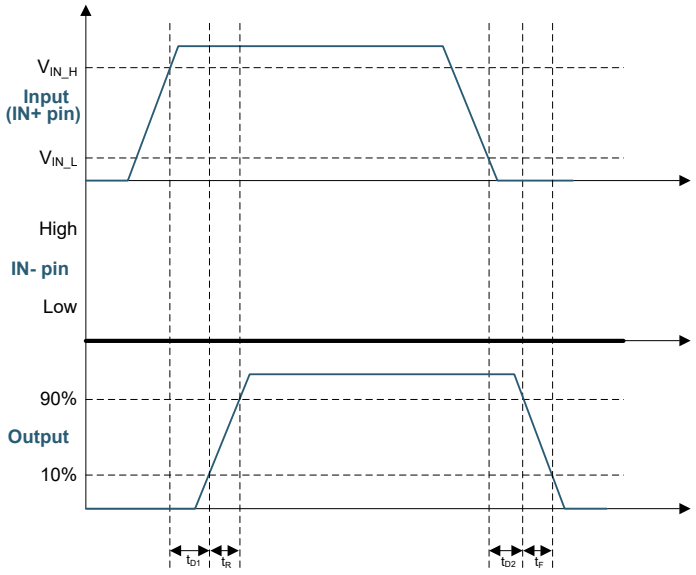


図 5-2. Dual Input Version, IN+ = PWM, IN- = GND

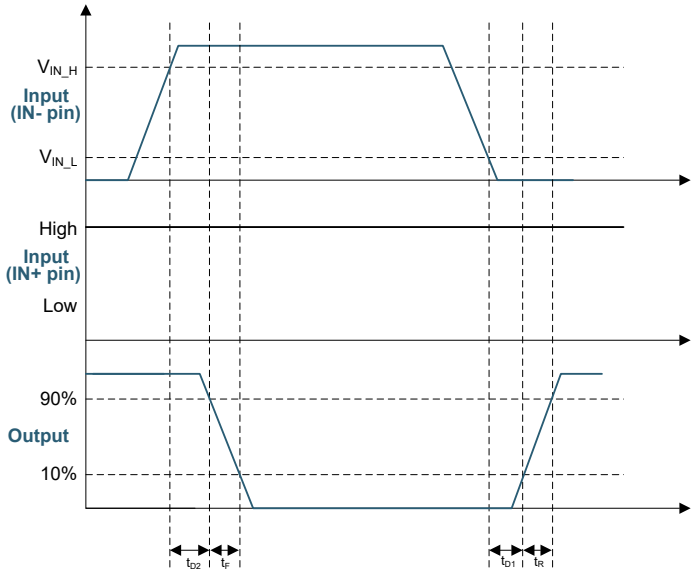


図 5-3. Dual Input Version, IN- = PWM, IN+ = High (or VDD)

5.8 Typical Characteristics

Unless otherwise specified, VDD = 12 V, IN+ = 3.3 V, IN- = GND, T_J = 25 °C, No load

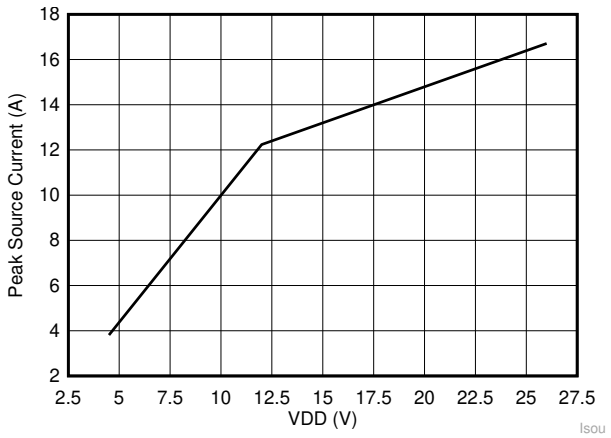


図 5-4. Peak Source Current vs VDD

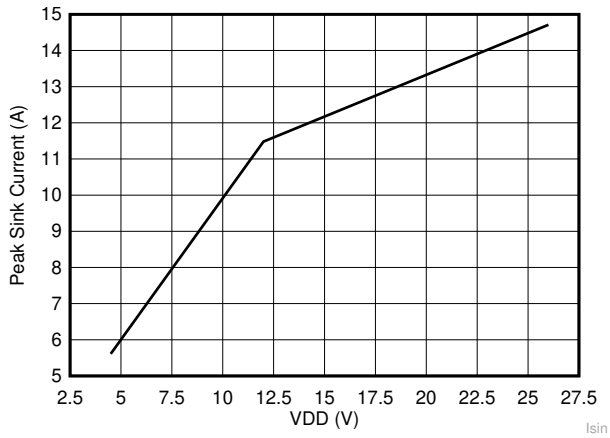
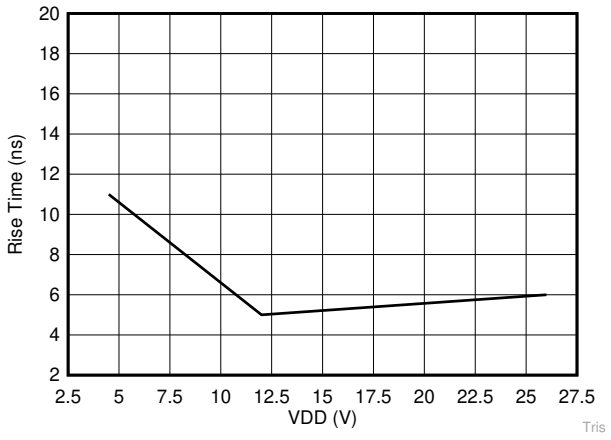
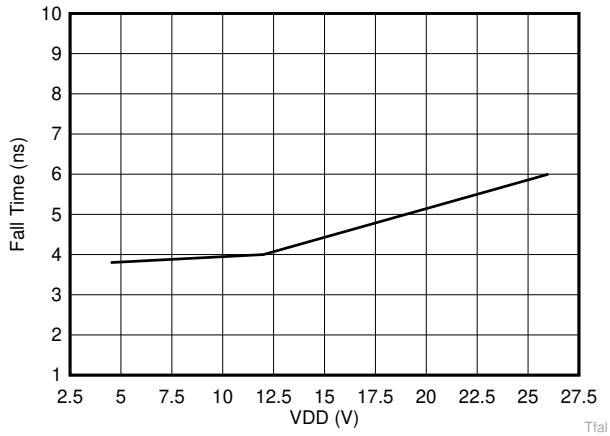


図 5-5. Peak Sink Current vs VDD



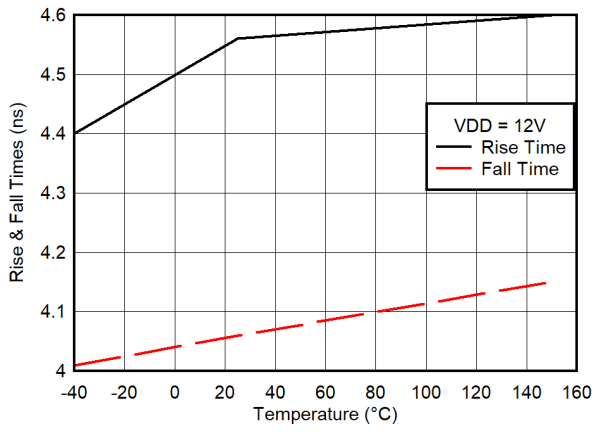
C_{LOAD} = 1.8 nF

図 5-6. Output Rise Time vs VDD



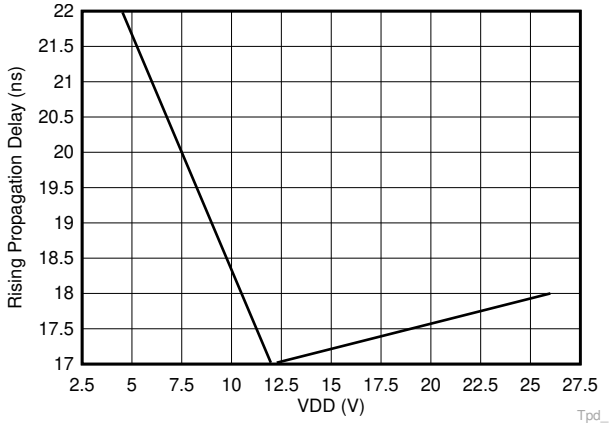
C_{LOAD} = 1.8 nF

図 5-7. Output Fall Time vs VDD



C_{LOAD} = 1.8 nF

図 5-8. Output Rise and Fall Time vs Temperature

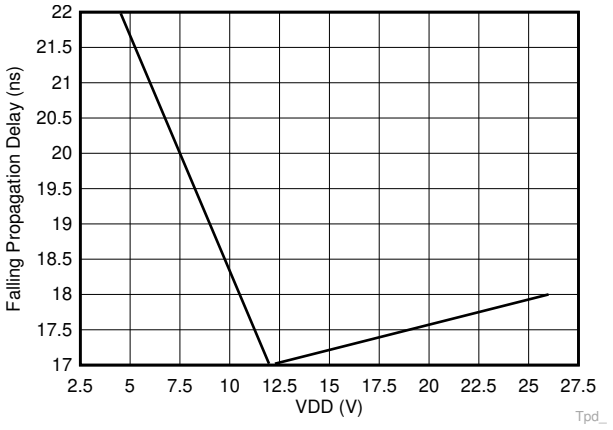


C_{LOAD} = 1.8 nF

図 5-9. Rising (Turnon) Propagation Delay vs VDD

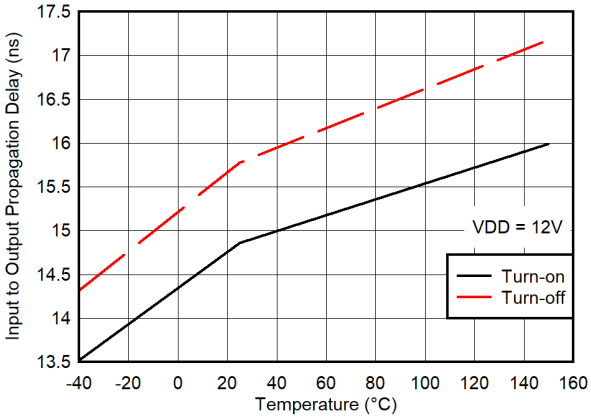
5.8 Typical Characteristics (continued)

Unless otherwise specified, VDD = 12 V, IN+ = 3.3 V, IN- = GND, T_J = 25 °C, No load



C_{LOAD} = 1.8 nF

図 5-10. Falling (Turnoff) Propagation Delay vs VDD



C_{LOAD} = 1.8 nF

図 5-11. Propagation Delay vs Temperature

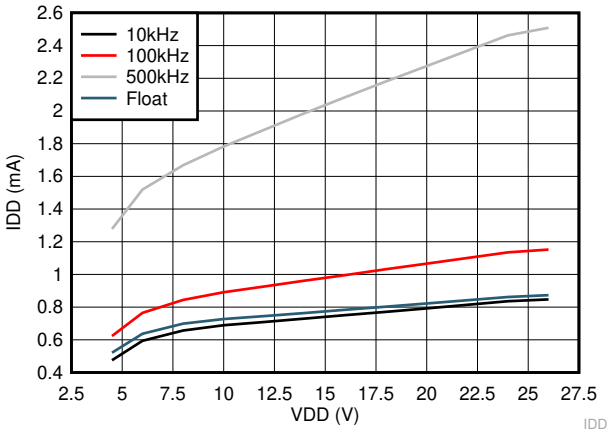


図 5-12. Operating Supply Current vs VDD

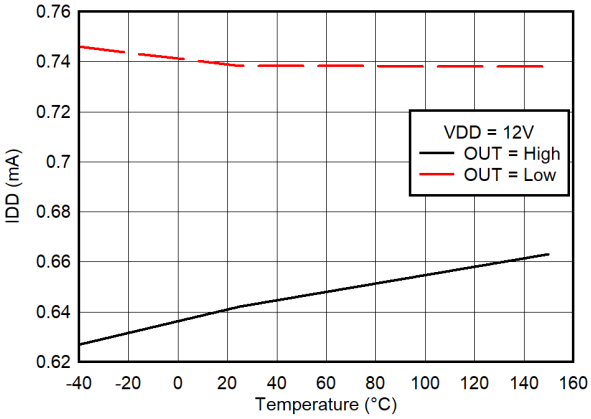


図 5-13. Operating Static Supply Current vs Temperature

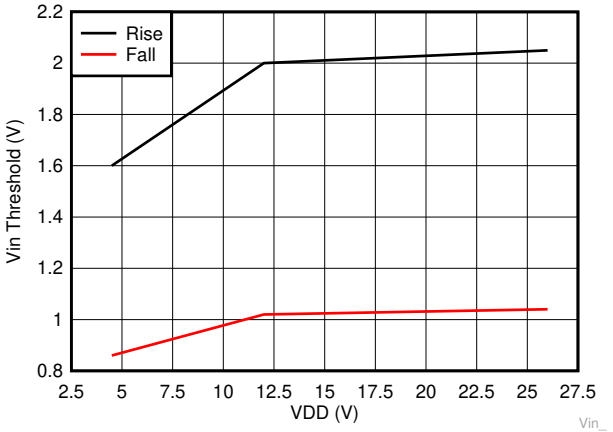


図 5-14. Input Threshold vs VDD

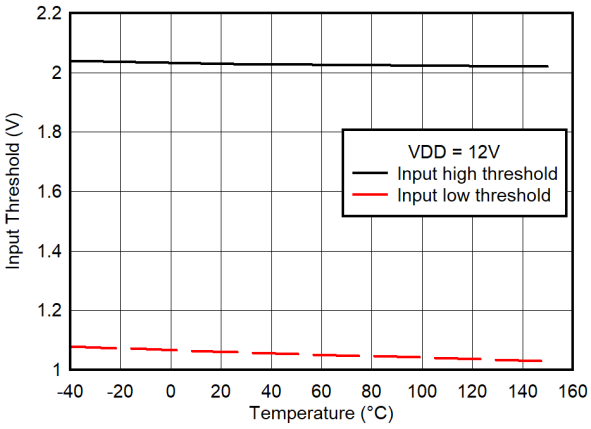


図 5-15. Input Threshold vs Temperature

5.8 Typical Characteristics (continued)

Unless otherwise specified, VDD = 12 V, IN+ = 3.3 V, IN- = GND, T_J = 25 °C, No load

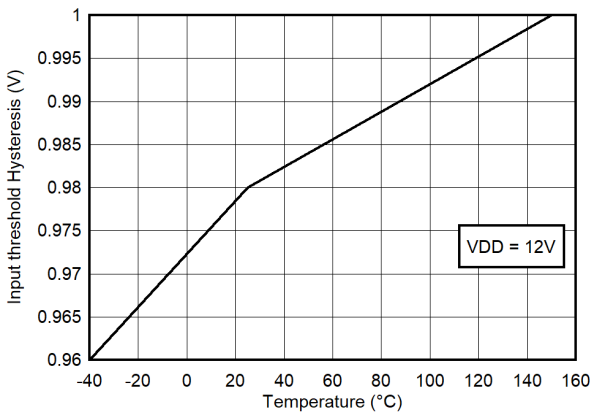


図 5-16. Input Threshold Hysteresis vs Temperature

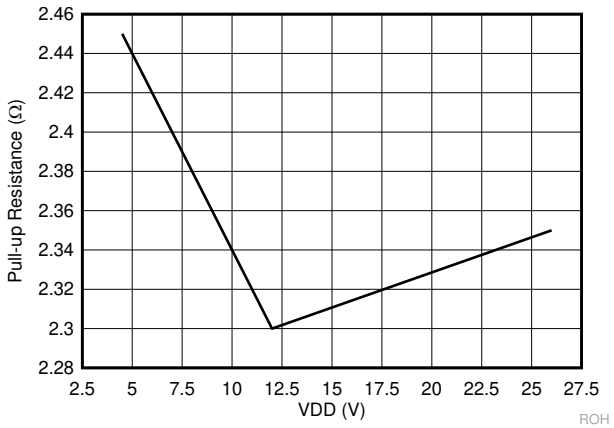


図 5-17. Output Pullup Resistance vs VDD

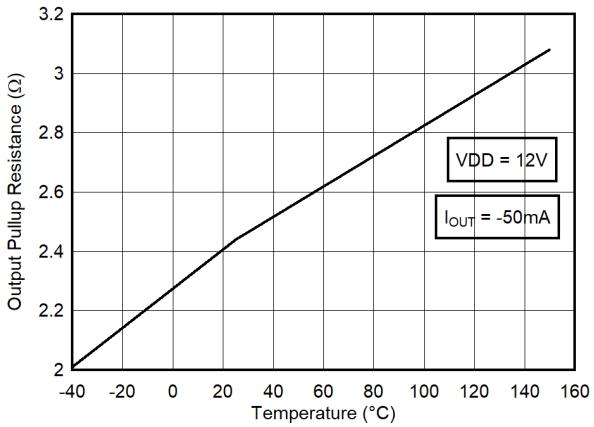


図 5-18. Output Pullup Resistance vs Temperature

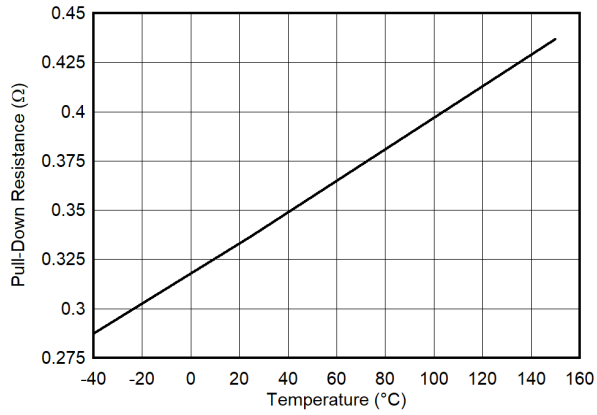


図 5-19. Output Pulldown Resistance vs VDD

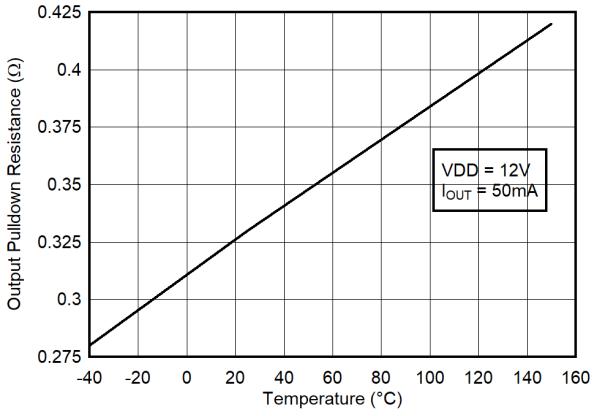


図 5-20. Output Pulldown Resistance vs Temperature

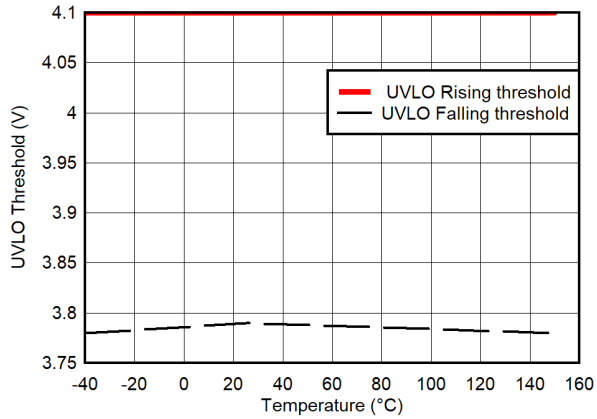


図 5-21. UVLO Threshold vs Temperature

5.8 Typical Characteristics (continued)

Unless otherwise specified, VDD = 12 V, IN+ = 3.3 V, IN- = GND, T_J = 25 °C, No load

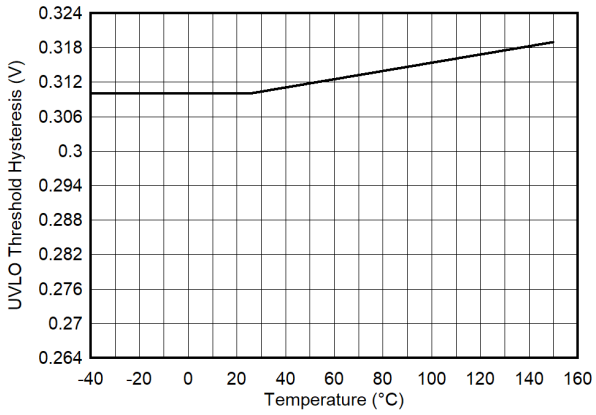


図 5-22. UVLO Hysteresis vs Temperature

6 Detailed Description

6.1 Overview

The UCC27614-Q1 device is a single-channel, high-speed, gate drivers capable of effectively driving MOSFET, SiC MOSFET, and IGBT power switches with 10-A source and 10-A sink (symmetrical drive) peak current. A strong source and sink capability boost immunity against a parasitic Miller turnon effect. The UCC27614-Q1 device can be directly connected to the gate driver transformer or line driver transformer as the inputs of the UCC27614-Q1 can handle –10V. The driver has a good transient handling capability on its output due to reverse currents, as well as rail-to-rail drive capability and small propagation delay, typically 17.5 ns.

The input threshold of the UCC27614-Q1 is compatible to TTL low-voltage logic, which is fixed and independent of VDD supply voltage. The driver can also work with CMOS based controllers as long as the threshold requirement is met. The 1-V typical hysteresis offers excellent noise immunity.

The driver has an EN pin with fixed TTL compatible threshold. EN is internally pulled up; pulling EN low disables the driver, while leaving EN open provides normal operation. The EN pin can be used as an additional input with the same performance as the IN, IN+, and IN- pins.

表 6-1. UCC27614-Q1 Features and Benefits

FEATURE	BENEFIT
–10 V IN and EN capability	Enhanced signal reliability and device robustness in noisy environments that experience ground bounce on the gate driver.
High source and sink current capability, 10 A	High current capability helps drive large gate charge loads to minimize switching losses.
Low 17.5 ns (typ) propagation delay.	Extremely low pulse transmission distortion
Wide VDD operating range of 4.5 V to 26 V	Flexibility in system design
VDD UVLO protection	Outputs are held Low in UVLO condition, which ensures predictable, glitch-free operation at power up and power down.
	UVLO of 4 V (typical) allows use in high switching frequency applications at low bias voltage to reduce switching losses.
Outputs held low when input pin (INx) in floating condition	Safety feature, especially useful in passing abnormal condition tests during safety certification
EN can float	Safe operation when the output of the controller, ties to the EN pin in tristate
Strong sink current (10 A) and low pulldown impedance (0.34 Ω)	High immunity to high dV/dt Miller turnon events

表 6-1. UCC27614-Q1 Features and Benefits (続き)

FEATURE	BENEFIT
TTL compatible input threshold logic with wide hysteresis	Enhanced noise immunity, while retaining compatibility with microcontroller logic level input signals (3.3 V, 5 V) optimized for digital power

6.2 Functional Block Diagram

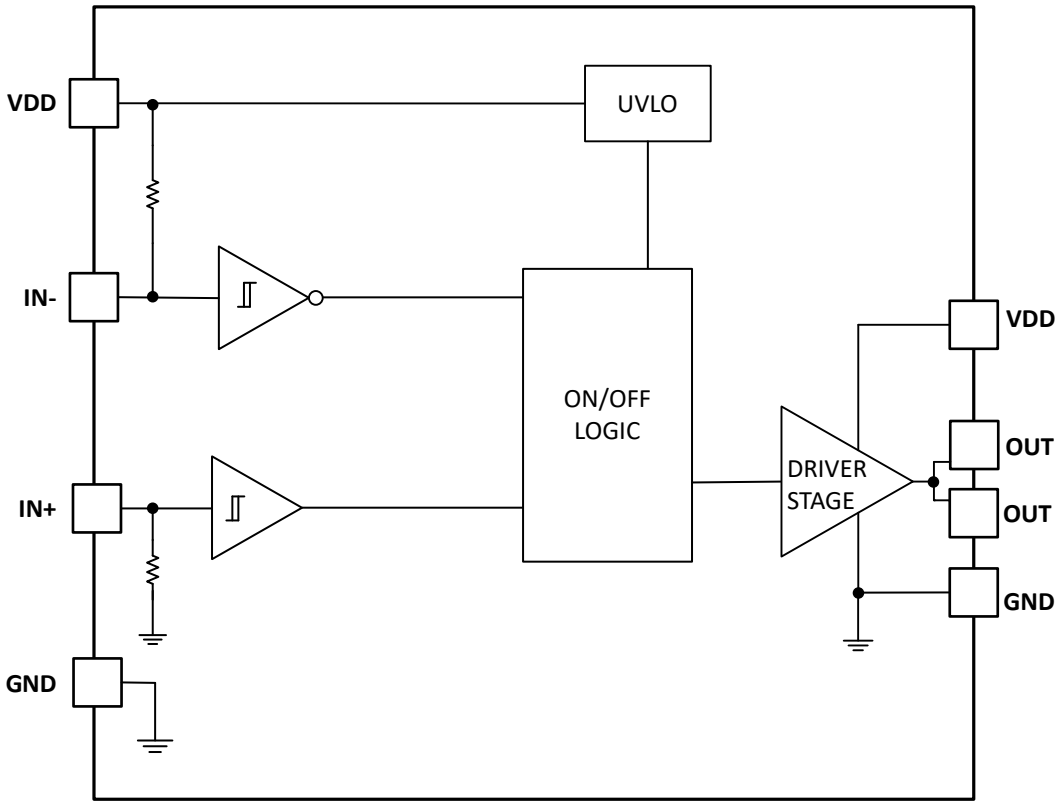
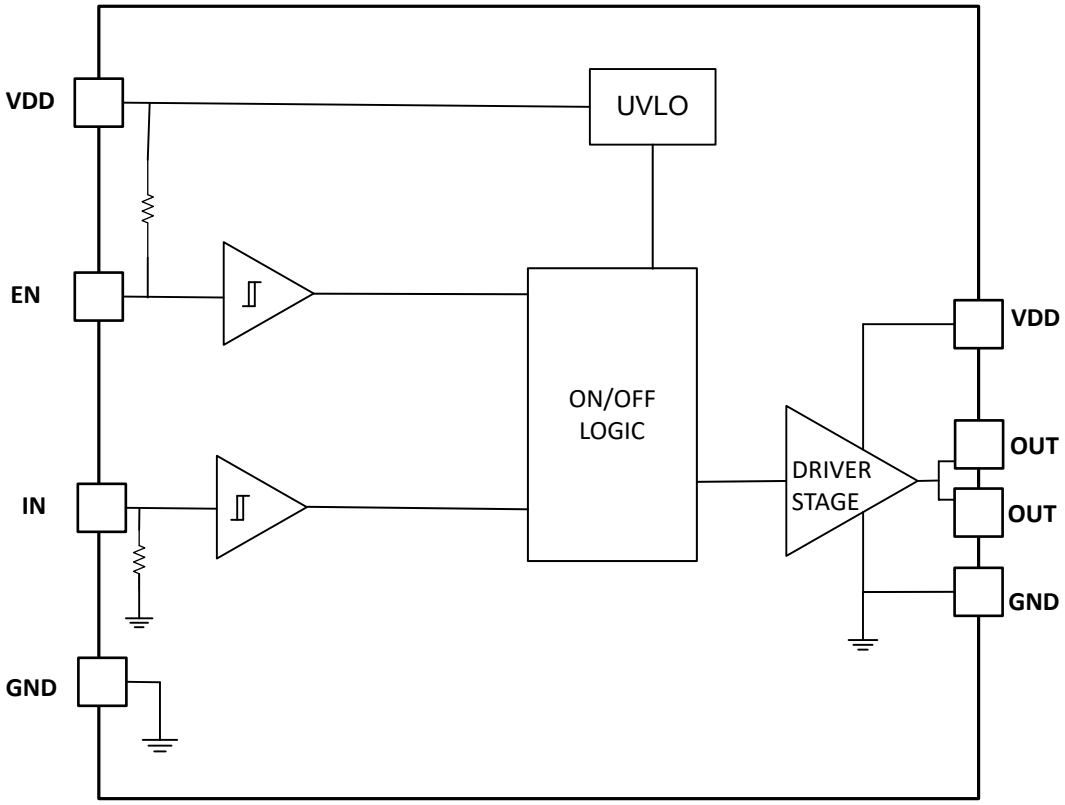


図 6-1. DSG



Typical - EN/IN- pullup resistance is 200 kΩ and IN/IN+ pulldown resistance is 120 kΩ.

図 6-2. D and DGN

6.3 Feature Description

6.3.1 VDD Undervoltage Lockout

The UCC27614-Q1 device offers an undervoltage lockout threshold of 4 V. The device's hysteresis range helps to avoid any chattering due to the presence of noise on the bias supply. 0.3 V of typical UVLO hysteresis is expected for 4-V UVLO devices. There is no significant driver output turnon delay due to the UVLO feature, and 5 µs of UVLO delay is expected. The UVLO turn-off delay is also minimized as much as possible. The UVLO delay is designed to minimize chattering that may occur due to very fast transients that may appear on VDD. When the bias supply is below UVLO thresholds, the outputs are held actively low irrespective of the state of input pins and enable pin. The device accepts a wide range of slew rates on its VDD pin, and VDD noise within the hysteresis range does not affect the output state of the driver (neither ON nor OFF).

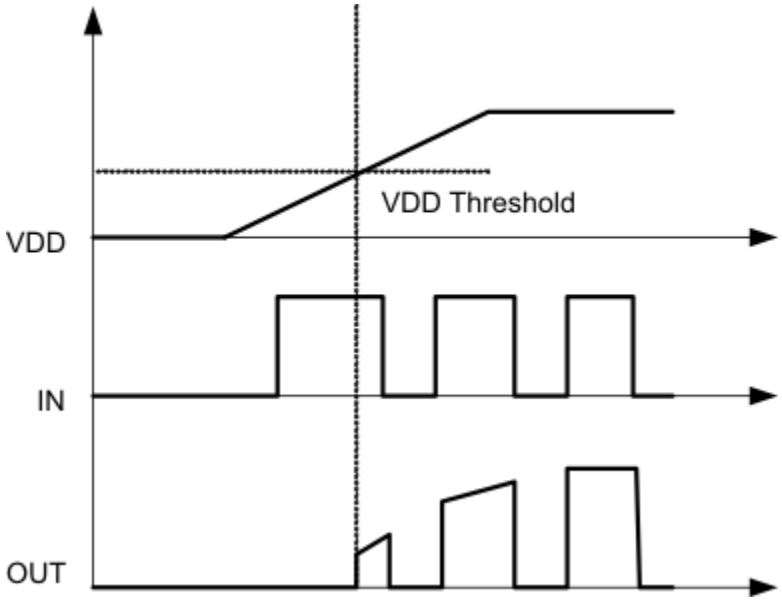


図 6-3. Power Up

6.3.2 Input Stage

The inputs of the UCC27614-Q1 device are compatible with TTL based threshold logic and the inputs are independent of the VDD supply voltage. With typical high threshold of 2 V and typical low threshold of 1 V, the logic level thresholds can be conveniently driven with PWM control signals derived from 3.3-V or 5-V logic. Wider hysteresis (typically 1 V) offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5 V. This device also features tight control of the input pin threshold voltage levels which eases system design considerations and ensures stable operation across temperature. The very low input capacitance, typically less than 8 pF, on these pins reduces loading and increases switching speed.

The device features an important protection function wherein, whenever the input pin is in a floating condition, the output is held in the low state. This is achieved with internal pullup or pulldown resistors on the input pins as shown in the simplified functional block diagrams. In some applications, due to difference in bias supply sequencing, different devices power-up at different times. This may cause output of the controller to be in tri-state. This output of the controller gets connected to the input of the driver device. If the driver device does not have a pulldown resistor then the output of the driver may go high erroneously and damage the switching power device.

The input stage of the driver should preferably be driven by a signal with a short rise or fall time. Caution must be exercised whenever the driver is used with slowly varying input signals, especially in situations where the device is located in a separate daughter board or PCB layout has long input connection traces:

- High dI/dt current from the driver output coupled with board layout parasitics can cause ground bounce. Because the device features just one GND pin which may be referenced to the power ground, this may interfere with the differential voltage between Input pins and GND and trigger an unintended change of output state. Because of fast 17.5-ns propagation delay, this can ultimately result in high-frequency oscillations, which increases power dissipation and poses risk of damage.
- 1-V Input threshold hysteresis boosts noise immunity compared to most other industry standard drivers.

An external resistance is highly recommended between the output of the driver and the power device instead of adding delays on the input signal. This also limits the rise or fall times to the power device which reduces the EMI. The external resistor has the additional benefit of reducing part of the gate charge related power dissipation in the gate driver device package and transferring it into the external resistor itself.

Finally, because of the unique input structure that allows negative voltage capability on the Input and Enable pins, caution must be used in the following applications:

- Input or Enable pins are switched to amplitude > 15 V.
- Input or Enable pins are switched at dV/dt > 2 V/ns.

If both of these conditions occur, add a series 150-Ω resistor for the pin(s) being switched to limit the current through the input structure.

6.3.3 Enable Function

The Enable (EN) pin of the UCC27614-Q1 device also has TTL compatible input thresholds with wide hysteresis. The typical turnon threshold is 2 V and the typical turn-off threshold is 1 V with typical hysteresis of 1 V. The Enable (EN) pin of the UCC27614-Q1 has an internal pullup resistor to an internal reference voltage. Thus, leaving the Enable pin floating turns on the driver and allows it to send output signals properly. If desired, the Enable can also be driven by low-voltage logic to enable and disable the driver. There is minimum delay from the enable block to the output for fast system response time. Similar to the input pins, the enable pin can also handle significant negative voltage and therefore provides system robustness. The enable pin can withstand wide range of slew rate such as 1 V/ns to 1 V/ms. The enable signal is independent of VDD voltage and stable across the full operating temperature range.

6.3.4 Output Stage

The output stage of the UCC27614-Q1 device is illustrated in UCC27614-Q1 Gate Driver Output section. . The UCC27614-Q1 device features a unique architecture on the output stage which delivers the highest peak source current when it is most needed during the Miller plateau region of the power switch turnon transition (when the power switch drain/collector voltage experiences dV/dt). The device output stage features a hybrid pullup structure using a parallel arrangement of N-Channel and P-Channel MOSFET devices. By turning on the N-Channel MOSFET during a narrow instant when the output changes state from low to high, the gate driver device is able to deliver a brief boost in the peak sourcing current enabling fast turnon. The on-resistance of this N-channel MOSFET (R_{NMOS}) is approximately 0.52 Ω when activated.

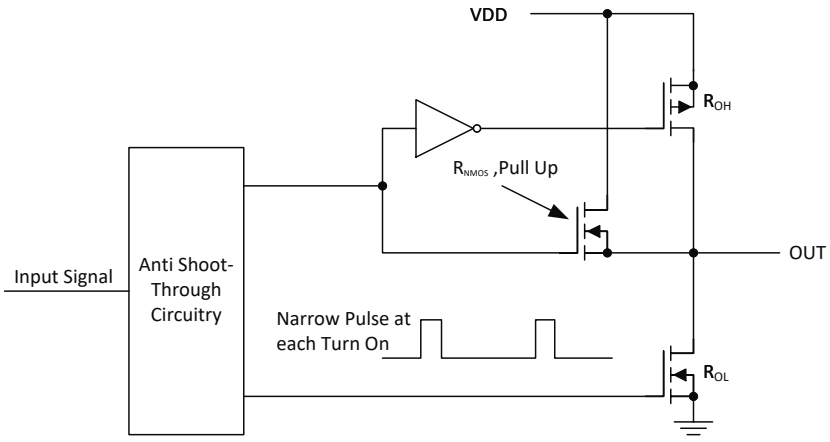


図 6-4. UCC27614-Q1 Gate Driver Output Stage

The R_{OH} parameter (see Electrical Table) is a DC measurement and it is representative of the on-resistance of the P-Channel device only, because the N-Channel device is turned on only during output change of state from low to high. Thus, the effective resistance of the hybrid pullup stage is much lower than what is represented by R_{OH} parameter. The pulldown structure is composed of a N-channel MOSFET only. The R_{OL} is also a DC measurement, and it is representative of true impedance of the pulldown stage in the device.

The UCC27614-Q1 can deliver 10-A source, and up to 10-A sink at VDD = 12 V. Strong sink capability results in a very low pulldown impedance in the driver output stage which boosts immunity against the parasitic Miller turnon (high slew rate dV/dt turnon) effect that is seen in both IGBT and FET power switches.

An example of a situation where Miller turnon is a concern is synchronous rectification (SR). In SR application, the dV/dt occurs on MOSFET drain when the MOSFET is already held in OFF state by the gate driver. The current charging the C_{GD} Miller capacitance during this high dV/dt is shunted by the pulldown stage of the driver. If the pulldown impedance is not low enough then a voltage spike can result in the V_{GS} of the MOSFET, which can result in spurious turnon. This phenomenon is illustrated in 図 6-5.

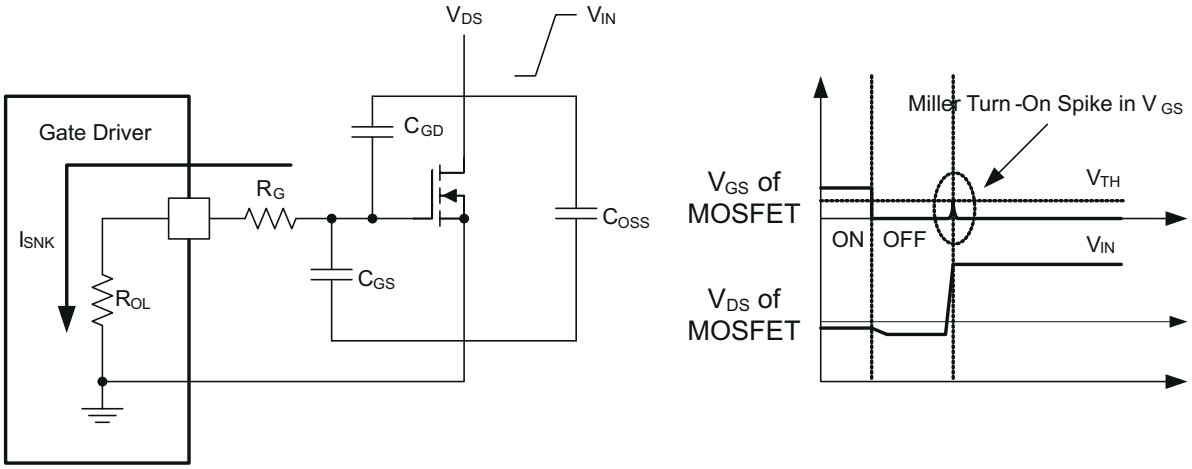


図 6-5. Low Pull-Down Impedance in UCC27614-Q1 (Output Stage Mitigates Miller Turnon Effect)

The driver output voltage swings between VDD and GND providing rail-to-rail operation because of the low dropout of the output stage. In most applications, the external Schottky diode clamps may be eliminated because the presence of the MOSFET body diodes offers low impedance to switching overshoots and undershoots. The output stage of the UCC27614-Q1 devices can handle significant transient reverse current. The two OUT pins of the device should be shorted on the application board. The application may use resistor and parallel diode-resistor combination at the gate of the MOSFET or IGBT to program different rise (pullup current) time and fall (pulldown) time.

6.4 Device Functional Modes

The UCC27614-Q1 devices operate in normal mode and UVLO mode (see セクション 6.3.1 for information on UVLO operation). In normal mode, the output state is dependent on the states of the device, and the input pins.

The UCC27614-Q1 DSG features dual input, one inverting (IN-), and one non-inverting (IN+). This device does not contain a dedicated enable (EN) pin as in the UCC27614-Q1 D and DGN.

The UCC27614-Q1 D and DGN feature a single, non-inverting input, but also contain enable and disable functionality through the EN pin. Setting the EN pin to logic HIGH enables the non-inverting input to output on the IN pin. The two OUT pins are internally shorted and shall be shorted on the application board as well.

表 6-2. UCC27614-Q1DSG Truth Table

IN+	IN-	OUT
H	L	H
H	H	L
L	H	L
L	L	L
Float	Any	L
Any	Float	L

表 6-3. UCC27614-Q1D and DGN Truth Table

IN	EN	OUT
H	L	L
H	H	H
L	H	L
L	L	L
Float	Any	L
Any	Float	IN

7 Applications and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

High-current gate driver devices are required in switching power applications for a variety of reasons. To enable fast switching of power devices and reduce associated switching power losses, a powerful gate driver can be employed between the PWM output of controllers or signal isolation devices and the gates of the power semiconductor devices. Further, gate drivers are indispensable when sometimes it is just not feasible to have the PWM controller directly drive the gates of the switching devices. The situation will be often encountered because the PWM signal from a digital controller or signal isolation device is often a 3.3-V or 5-V logic signal which is not capable of effectively turning on a power switch. A level-shifting circuitry is needed to boost the logic-level signal to the gate-drive voltage in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar, (or P- N-channel MOSFET), transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate for this because they lack level-shifting capability and low-drive voltage protection. Gate drivers effectively combine both the level-shifting, buffer drive and UVLO functions. Gate drivers also find other needs such as minimizing the effect of switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses into itself.

The UCC27614-Q1 is very flexible in this role with a strong drive current capability and wide recommended supply voltage range of 4.5 V to 26 V. This allows the driver to be used in 5-V bias logic level very high frequency MOSFET applications, 12-V MOSFET applications, 20-V and -5-V (relative to source) SiC FET applications, 15-V and -8-V (relative to Emitter) IGBT applications and many others. As a single-channel driver, the UCC27614-Q1 can be used as a low-side or high-side driver. To use as a low-side driver, the switch ground is usually the system ground so it can be connected directly to the gate driver. To use as a high-side driver with a floating return node however, signal isolation is needed from the controller as well as a bias supply that is referenced to the UCC27614-Q1 ground pin. Alternatively, in a high-side drive configuration the UCC27614-Q1 can be tied directly to the controller signal and biased with a nonisolated supply. However, in this configuration the output of the UCC27614-Q1 must drive a pulse transformer which then drives the power-switch to work properly with the floating source and emitter of the power switch.

These requirements, coupled with the need for low propagation delays and availability in compact, and low-inductance packages with good thermal capability, make gate driver devices such as the UCC27614-Q1 extremely important components in switching power combining benefits of high-performance, low cost, low component count, board space reduction and simplified system design.

7.2 Typical Application

7.2.1 Driving MOSFET/IGBT/SiC MOSFET

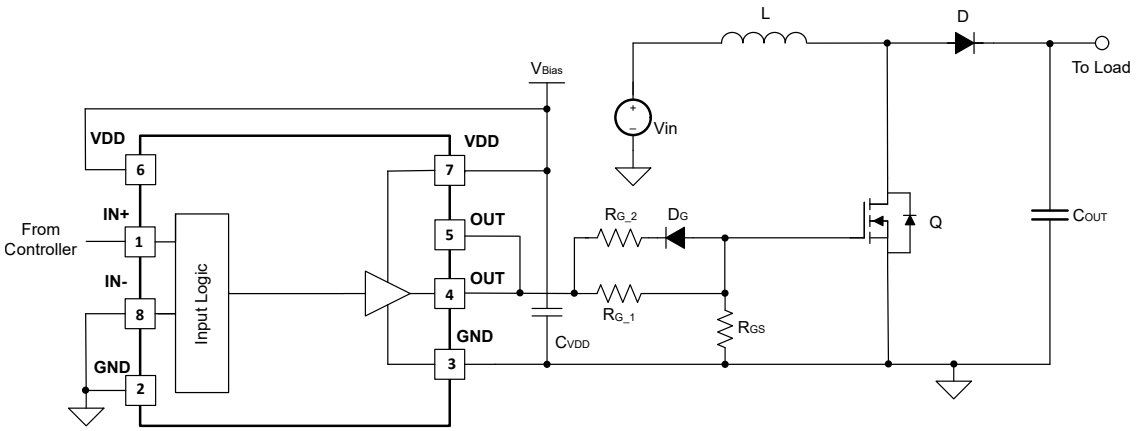


図 7-1. Driving a MOSFET/IGBT/SiC MOSFET in a Boost Converter

7.2.1.1 Design Requirements

When selecting the gate driver device for an end application, some design considerations must be evaluated in order to make the most appropriate selection. Following are some of the design parameters that should be used when selecting the gate driver device for an end application: input-to-output configuration, the input threshold type, bias supply voltage levels, peak source and sink currents, availability of independent enable and disable functions, propagation delay, power dissipation, and package type. See the example design parameters and requirements in 表 7-1.

表 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input to output logic	Non-inverting
Input threshold type	TTL
Bias supply voltage levels	+18 V
Negative output low voltage	N/A
dV_{DS}/dt(1)	100 V/ns
Enable function	Yes
Disable function	N/A
Propagation delay	<30 ns
Power dissipation	<1 W
Package type	SON8 or SOIC8

(1) dV_{DS}/dt is a typical requirement for a given design. This value can be used to find the peak source/sink currents needed as shown in セクション 7.2.1.2.4.

7.2.1.2 Detailed Design Procedure

7.2.1.2.1 Input-to-Output Configuration

The design should specify which type of input-to-output configuration should be used. If turning on the power MOSFET or IGBT when the input signal is in high state is preferred, then a device capable of the non-inverting configuration must be selected. If turning off the power MOSFET or IGBT when the input signal is in high state is preferred, then a device capable of the inverting configuration must be chosen. UCC27614-Q1DSG offers non-inverting output when IN+ pin is used as PWM input while IN- is grounded. When IN- pin is used as PWM input and IN+ is pulled high, the UCC27614-Q1DSG works as inverting output gate driver.

If ground-bouncing is a potential issue, a gate driver with negative voltage handling capability should be chosen. UCC27614-Q1 devices can handle -10-V at its input and -2-V on its output. The input of the UCC27614-Q1 devices can handle wide range of slew rate at its input and the inputs have wide hysteresis.

7.2.1.2.2 Input Threshold Type

The type of Input voltage threshold determines the type of controller that can be used with the gate driver device. The UCC27614-Q1 devices feature a TTL compatible input threshold logic, with wide hysteresis. The threshold voltage levels are low voltage and independent of the VDD supply voltage, which allows compatibility with both logic-level input signals from microcontrollers as well as higher-voltage input signals from analog controllers. See the Electrical Characteristics table for the actual input threshold voltage levels and hysteresis specifications for the UCC27614-Q1 devices.

7.2.1.2.3 VDD Bias Supply Voltage

The bias supply voltage to be applied to the VDD pin of the device should not exceed the values listed in the Recommended Conditions table. However, different power switches demand different voltage levels to be applied at the gate terminals for effective turnon and turn-off. With certain power switches, a positive gate voltage may be required for turnon and a negative gate voltage may be required for turn-off, in which case the VDD bias supply equals the voltage differential. With an operating range from 4.5 V to 26 V, the UCC27614-Q1 devices can be used to drive a power switches such as logic level MOSFETs, power MOSFETS, SiC MOSFETs, and IGBTs.

7.2.1.2.4 Peak Source and Sink Currents

Generally, the switching speed of the power switch during turnon and turn-off should be as fast as possible to minimize switching power losses. The gate driver device must be able to provide the required peak current for achieving the targeted switching speeds for the targeted power switching devices such as logic level MOSFETs, power MOSFETs, SiC MOSFETs, and IGBTs.

Using the example of a power MOSFET, the system requirement for the switching speed is typically described in terms of the slew rate of the drain-to-source voltage of the power MOSFET (such as dV_{DS}/dt). For example, the system requirement might state that a 600-V power MOSFET must be turned on with a dV_{DS}/dt of 100 V/ns or higher under a DC bus voltage of 400 V in a continuous-conduction-mode (CCM) boost PFC-converter application. This type of application is an inductive hard-switching application and reducing switching power losses is critical. This requirement means that the entire drain-to-source voltage swing during power MOSFET turnon event (from 400 V in the OFF state to $V_{DS(on)}$ in on state) must be completed in approximately 4 ns or less. When the drain-to-source voltage swing occurs, the Miller charge of the power MOSFET (Q_{GD} parameter of the 600-V power MOSFET, let us say, is 32 nC) is supplied by the peak current of gate driver. According to power MOSFET inductive switching mechanism, the gate-to-source voltage of the power MOSFET at this time is the Miller plateau voltage, which is typically a few volts higher than the threshold voltage of the power MOSFET, $V_{GS(th)}$.

To achieve the targeted dV_{DS}/dt, the gate driver must be capable of providing the Q_{GD} charge in 4 ns or less. In other words a peak current of 8 A (= 32 nC / 4 ns) or higher must be provided by the gate driver. The UCC27614-Q1 series of gate drivers can provide 10-A peak sourcing current, and 10-A peak sinking current which clearly exceeds the design requirement and has the capability to meet the switching speed needed. The significantly high drive capability provides an extra margin against part-to-part variations in the Q_{GD} parameter of the power MOSFET along with additional flexibility to insert external gate resistors and fine tune the switching

speed for efficiency versus EMI optimizations. However, in practical designs the parasitic trace inductance in the gate drive circuit of the PCB will have a definitive role to play on the power MOSFET switching speed. The effect of this trace inductance is to limit the dI/dt of the output current pulse of the gate driver. To illustrate this, consider output current pulse waveform from the gate driver to be approximated to a triangular profile, where the area under the triangle (½ ×I_{Peak} × time) would equal the total gate charge of the 600-V power MOSFET (Q_G parameter in the power MOSFET datasheet). If the parasitic trace inductance limits the dI/dt then a situation may occur in which the full peak current capability of the gate driver is not fully achieved in the time required to deliver the Q_G of the switching power MOSFET. In other words, the time parameter in the above equation would dominate and the I_{Peak} value of the current pulse would be much less than the true peak current capability of the driver, while the required Q_G is still delivered. Because of this, the desired switching speed may not be realized, even when theoretical calculations indicate the gate driver can achieve the targeted switching speed. Thus, placing the gate driver device very close to the power MOSFET and designing a very small gate drive-loop with minimal PCB trace inductance is important to realize fast switching.

7.2.1.2.5 Enable and Disable Function

Certain applications demand independent control of the output state of the driver without involving the input PWM signal. A pin which offers an enable and disable function achieves this requirement. For these applications, the UCC27614-Q1 D and DGN are suitable as they feature an input pin (IN) and an Enable pin (EN). Both of these pins are independent of each other and are also independent of VDD.

Other applications require multiple inputs. For such applications the UCC27614-Q1 DSG is suitable. The UCC27614-Q1DSG features an IN+ and IN– pin, both of which control the state of the output as listed in the Device Functional Modes truth table. Based on whether an inverting or non-inverting input signal is provided to the driver, the appropriate input pin can be selected as the primary input for controlling the gate driver. The other unused input pin can be conveniently used for the enable and disable functionality if needed. If the design does not require an enable function, the unused input pin can be tied to either the VDD pin (IN+ is the unused pin), or GND (in case IN– is unused pin) in order to ensure it does not affect the output status.

7.2.1.2.6 Propagation Delay and Minimum Input Pulse Width

The acceptable propagation delay from the gate driver is dependent on the switching frequency at which it is used and the acceptable level of pulse distortion to the system. The UCC27614-Q1 devices feature 17.5-ns (typical) propagation delays which ensures very little pulse distortion and allows operation at very high frequencies. Very high switching frequency applications also need the gate driver to satisfactorily produce the output pulse when the input pulse width is very small. The UCC27614-Q1 devices can typically handle less than 10 ns at its input and produce satisfactory output depending on the load. See Switching Characteristics table for the propagation and other timing specifications of the UCC27614-Q1 devices.

7.2.1.2.7 Power Dissipation

Power dissipation of the gate driver has two portions as shown in equation below:

$$P_{DISS} = P_{DC} + P_{SW} \tag{1}$$

The DC portion of the power dissipation is $P_{DC} = I_Q \times VDD$ where I_Q is the quiescent current for the driver. The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections, and so on, and any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of internal parasitic capacitances, parasitic shoot-through). The UCC27614-Q1 features low quiescent currents (less than 1 mA) and contains internal logic to minimize any shoot-through (PMOS to NMOS and vice versa) in the output driver stage. Thus, the effect of the P_{DC} on the total power dissipation within the gate driver can be assumed to be negligible. In practice this is the power consumed by driver when its output is disconnected from the gate of power switch.

As explained in earlier sections, the output stage of the gate driver is based on PMOS and NMOS. These NMOS and PMOS are designed in such a way that they offer very low resistance during switching. And therefore they

have very low drop-out. The power dissipated in the gate driver package during switching (P_{SW}) depends on the following factors:

- Gate charge required of the power device (usually a function of the drive voltage V_G, which is very close to input bias supply voltage VDD due to low V_{Ox} drop-out)
- Switching frequency
- Power MOSFET internal and external gate resistor

When a driver device is tested with a discrete, capacitive load it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by:

$$E_G = \frac{1}{2} C_{LOAD} V_{DD}^2 \tag{2}$$

where

- C_{LOAD} is load capacitor and V_{DD} is bias voltage feeding the driver.

There is an equal amount of energy dissipated when the capacitor is discharged. During turnoff the energy stored in capacitor is fully dissipated in drive circuit. This leads to a total power loss during switching cycle given by the following:

$$P_G = C_{LOAD} V_{DD}^2 f_{sw} \tag{3}$$

where

- f_{SW} is the switching frequency

The switching load presented by a power FET and IGBT can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications of typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_g, one can determine the power that must be dissipated when charging a capacitor. This is done by using the equivalence, $Q_g = C_{LOAD} V_{DD}$, to provide the following equation for power:

$$P_G = C_{LOAD} V_{DD}^2 f_{sw} = Q_g V_{DD} f_{sw} \tag{4}$$

This power P_G is dissipated in the resistive elements of the circuit when the MOSFET and IGBT is being turned on or off. Half of the total power is dissipated when the load capacitor is charged during turnon, and the other half is dissipated when the load capacitor is discharged during turn-off. When no external gate resistor is employed between the driver device and MOSFET/IGBT, this power is completely dissipated inside the driver device. With the use of external gate drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistances (more power dissipated in the higher resistance component). Based on this simplified analysis, the driver power dissipation during switching is calculated as shown in following equation. This primarily applies to those applications where total external gate resistor is significantly large to limit the peak current of the gate driver.

$$P_{SW} = 0.5 \times Q_g \times V_{DD} \times f_{sw} \left(\frac{R_{OFF}}{(R_{OFF} + R_{GATE})} + \frac{R_{ON}}{(R_{ON} + R_{GATE})} \right) \tag{5}$$

where

- $R_{OFF} = R_{OL}$ and R_{ON} (effective resistance of pullup structure)

7.2.1.3 Application Curves

Many telecom and datacom isolated power modules employ synchronous rectification on the secondary side with center tap topology (as shown in UCC27614-Q1DSG Used to Drive Secondary Side Synchronous Rectifiers). The low-side driver UCC27614-Q1 can drive these synchronous rectifier MOSFETs as they are referenced to the output ground. These power modules are very power dense and the printed circuit board real estate is at a premium. These power modules may also have very high output current requirements and therefore either need very small Rds(on) MOSFETs or parallel multiple MOSFETs to achieve lower total Rds(on). In either case, the total get charge increases and therefore such applications need a gate driver with high drive current capability. UCC27614-Q1DSG fulfills all these requirements. The UCC27614-Q1DSG device is used in one such application of a 400-V to 12-V isolated DC-DC converter. Waveforms shown here are captured in this actual application power supply.

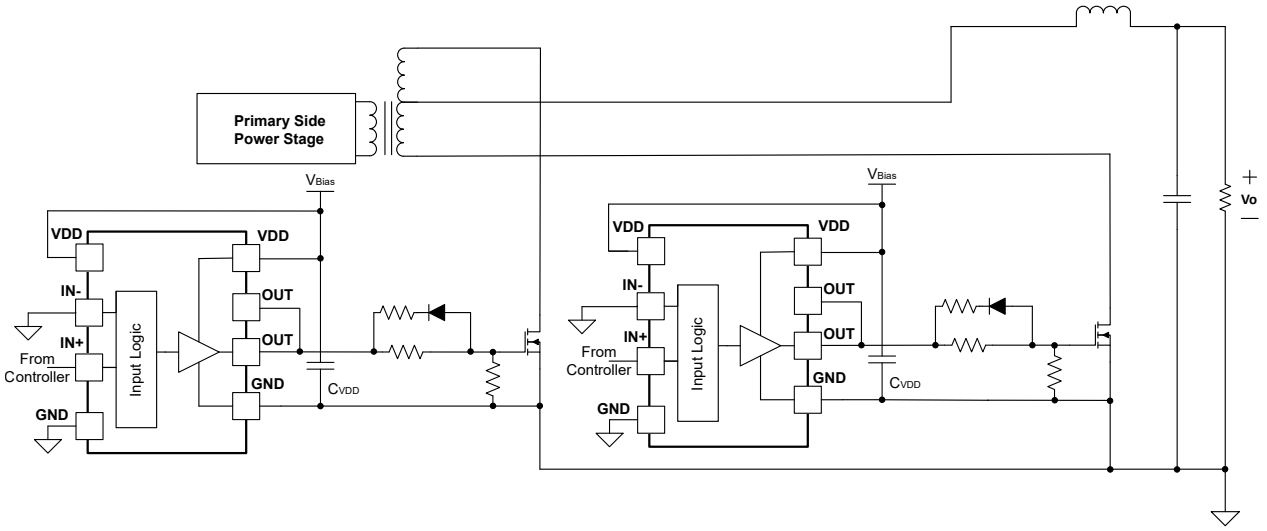


図 7-2. UCC27614-Q1DSG Used to Drive Secondary Side Synchronous Rectifiers

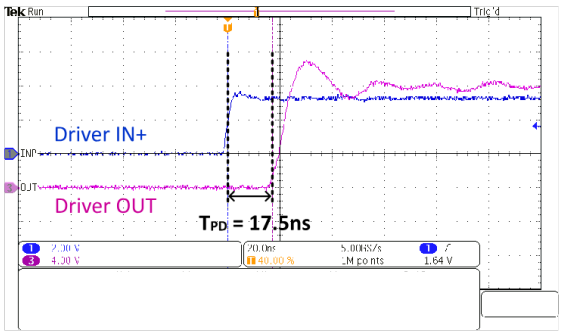


図 7-3. UCC27614-Q1 Rising (Turn-On) Propagation Delay

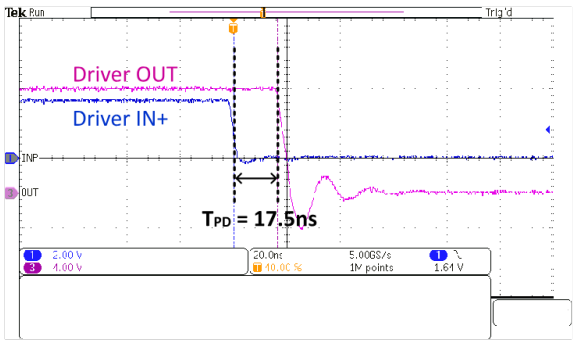


図 7-4. UCC27614-Q1 Falling (Turn-Off) Propagation Delay

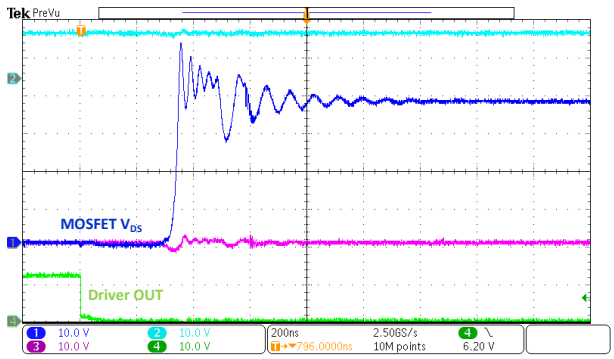


図 7-5. Synchronous Rectifier MOSFET V_{DS} Rising Edge Using UCC27614-Q1DSG

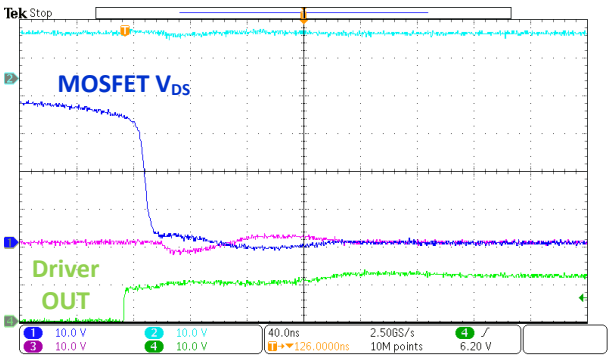


図 7-6. Synchronous Rectifier MOSFET VDS Falling Edge Using UCC27614-Q1DSG

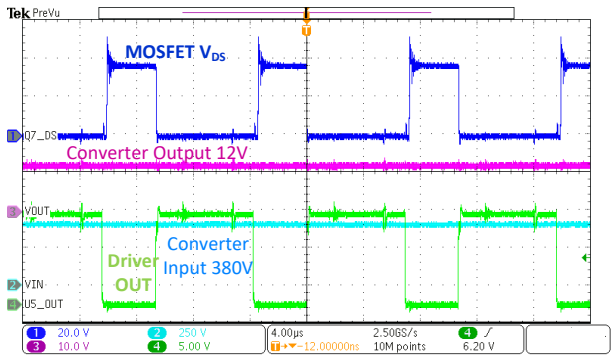


図 7-7. Input and Output Voltage of Converter Using UCC27614-Q1DSG

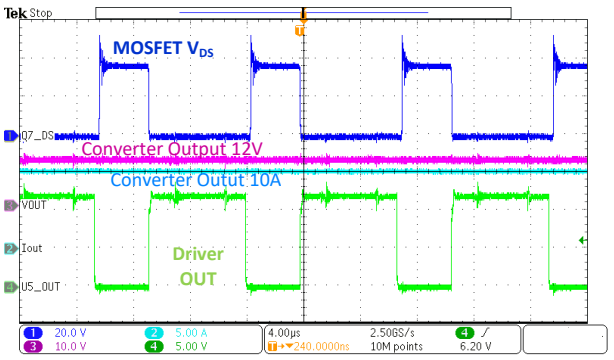


図 7-8. Output Voltage and Current of a Converter Using UCC27614-Q1DSG

8 Power Supply Recommendations

The bias supply voltage range for which the UCC27614-Q1 devices are recommended to operate is from 4.5 V to 26 V. The lower end of this range is governed by the internal UVLO protection feature on the VDD pin supply circuit blocks. Whenever the driver is in UVLO condition when the VDD pin voltage is below the $V_{(ON)}$ supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 26-V recommended maximum voltage rating of the VDD pin of the device. The absolute maximum voltage for the VDD pin is 30 V.

The UVLO protection feature also involves a hysteresis function. This means that when the VDD pin bias voltage has exceeded the threshold voltage and device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification. Therefore, ensuring that, while operating at or near the 4.5 V range, the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device is important to avoid triggering device shutdown.

During system shutdown, the device operation continues until the VDD pin voltage has dropped below the VDD UVLO falling threshold which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system start-up, the device does not begin operation until the VDD pin voltage has exceeded above the VDD UVLO rising threshold. The quiescent current consumed by the internal circuit blocks of the device is supplied through the VDD pin. Although this fact is well known, recognizing that the charge for source current pulses delivered by the OUT pin is also supplied through the same VDD pin is important. As a result, every time a current is sourced out of the output pin (OUT), a corresponding current pulse is delivered into the device through the VDD pin. Thus ensuring that local bypass capacitors are provided between the VDD and GND pins and located as close to the device as possible for the purpose of decoupling is important. A low-ESR, ceramic surface-mount capacitor is needed. TI recommends having two capacitors; a 100-nF ceramic surface-mount capacitor placed less than 1mm from the VDD pin of the device and another ceramic surface-mount capacitor of few microfarads added in parallel.

UCC27614-Q1 is a high current gate driver. If the gate driver is placed far from the switching power device such as MOSFET then that may create large inductive loop. Large inductive loop may cause excessive ringing on any and all pins of the gate driver. This may result in stress exceeding device recommended rating. Therefore, it is recommended to place the gate driver as close to the switching power device as possible. It is also advisable to use an external gate resistor to damp any ringing due to the high switching currents and board parasitic elements.

9 Layout

9.1 Layout Guidelines

Proper PCB layout is extremely important in a high-current, fast-switching circuit to provide appropriate device operation and design robustness. The UCC27614-Q1 gate driver incorporates short propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of power switch to facilitate voltage transitions very quickly. Very high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit layout guidelines are recommended when designing with these high-speed drivers.

- Place the driver device as close as possible to power device to minimize the length of high-current traces between the driver output pins and the gate of the power switch device.
- Place the bypass capacitors between VDD pin and the GND pin as close to the driver pins as possible to minimize trace length for improved noise filtering. TI recommends having two capacitors; a 100-nF ceramic surface-mount capacitor placed less than 1mm from the VDD pin of the device and another ceramic surface-mount capacitor of few microfarads added in parallel. These capacitors support high peak current being drawn from VDD during turnon of power switch. The use of low inductance surface-mount components such as chip capacitors is highly recommended.
- The turnon and turn-off current loop paths (driver device, power switch and VDD bypass capacitor) should be minimized as much as possible in order to keep the stray inductance to a minimum. High di/dt is established in these loops at two instances – during turnon and turn-off transients, which induces significant voltage transients on the output pins of the driver device and gate of the power switch.
- Wherever possible, parallel the source and return traces of a current loop, taking advantage of flux cancellation
- Separate power traces and signal traces, such as output and input signals.
- To minimize switch node transients and ringing, adding some gate resistance and/or snubbers on the power devices may be necessary. These measures may also reduce EMI.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver should be connected to the other circuit nodes such as source of power switch, ground of PWM controller, and so forth, at a single point. The connected paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT pin may corrupt the input signals during transitions. The ground plane must not be a conduction path for any current loop. Instead the ground plane should be connected to the star-point with one trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well.

9.2 Layout Example

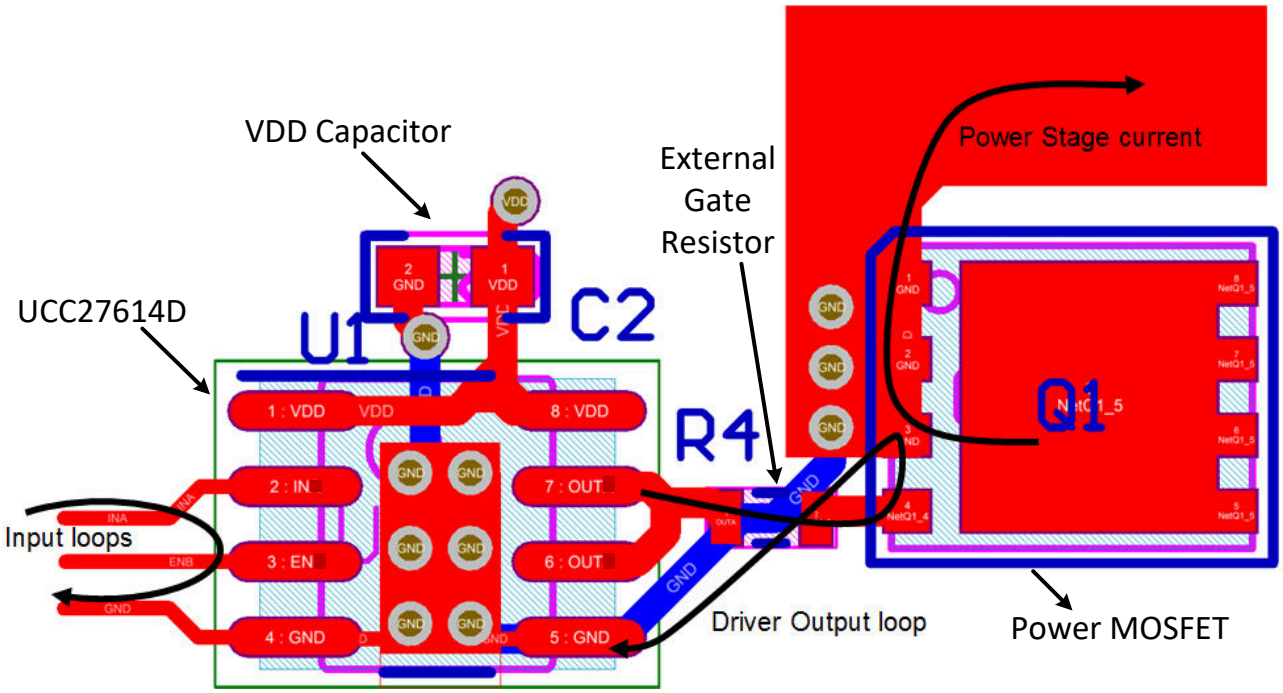


図 9-1. Layout Example: UCC27614-Q1

9.3 Thermal Consideration

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the package. In order for a gate driver to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The thermal metrics for the driver package is summarized in the Thermal Characteristics section of the data sheet. For detailed information regarding the thermal information table, refer to *IC Package Thermal Metrics Application Note* (SPRA953).

10 Device and Documentation Support

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テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (April 2024) to Revision A (October 2024)	Page
• 「特長」の HBM および CDM ESD 分類を更新	1
• D および DGN パッケージについて、「事前情報」を「量産データ」に変更	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC27614QDGNRQ1	Active	Production	HVSSOP (DGN) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	614Q
UCC27614QDGNRQ1.A	Active	Production	HVSSOP (DGN) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	614Q
UCC27614QDRQ1	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27614Q
UCC27614QDRQ1.A	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27614Q
UCC27614QDSGRQ1	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	614Q
UCC27614QDSGRQ1.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	614Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF UCC27614-Q1 :

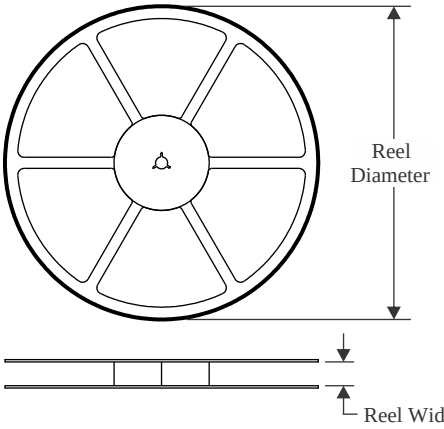
- Catalog : UCC27614

NOTE: Qualified Version Definitions:

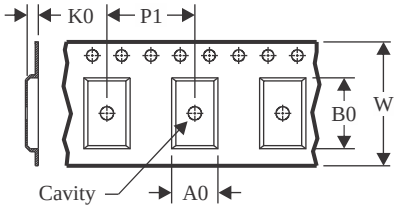
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

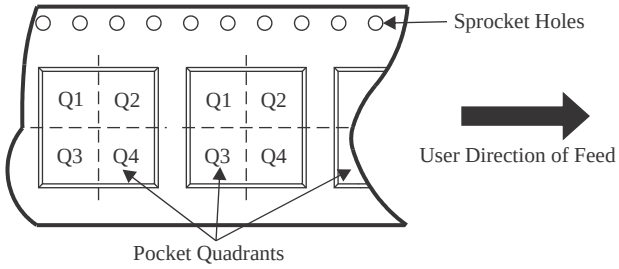


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

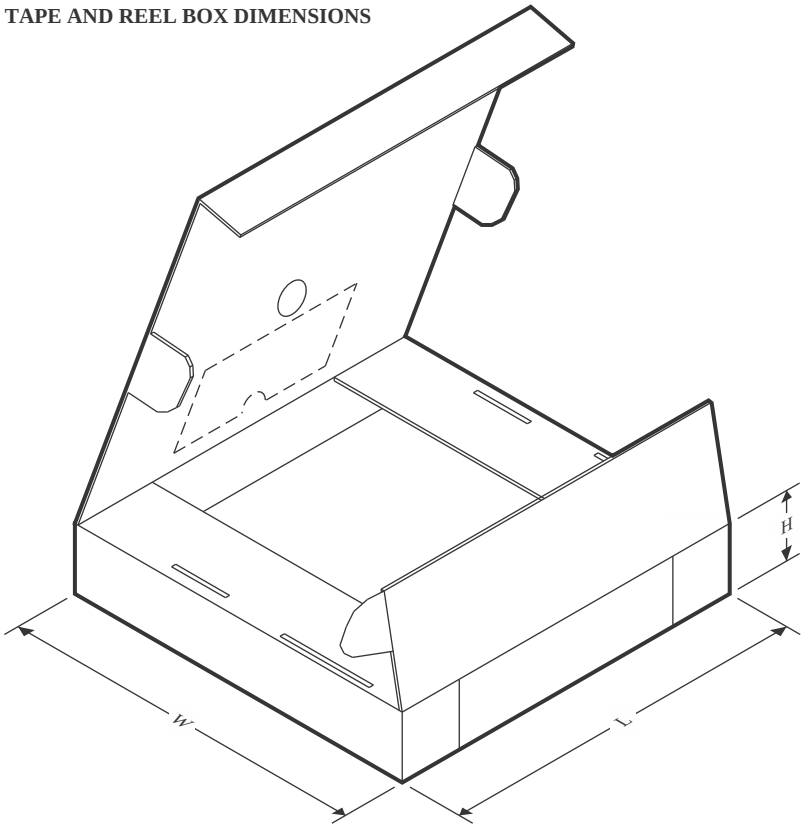
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27614QDGNRQ1	HVSSOP	DGN	8	3000	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27614QDRQ1	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27614QDSGRQ1	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27614QDGNRQ1	HVSSOP	DGN	8	3000	353.0	353.0	32.0
UCC27614QDRQ1	SOIC	D	8	3000	353.0	353.0	32.0
UCC27614QDSGRQ1	WSON	DSG	8	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

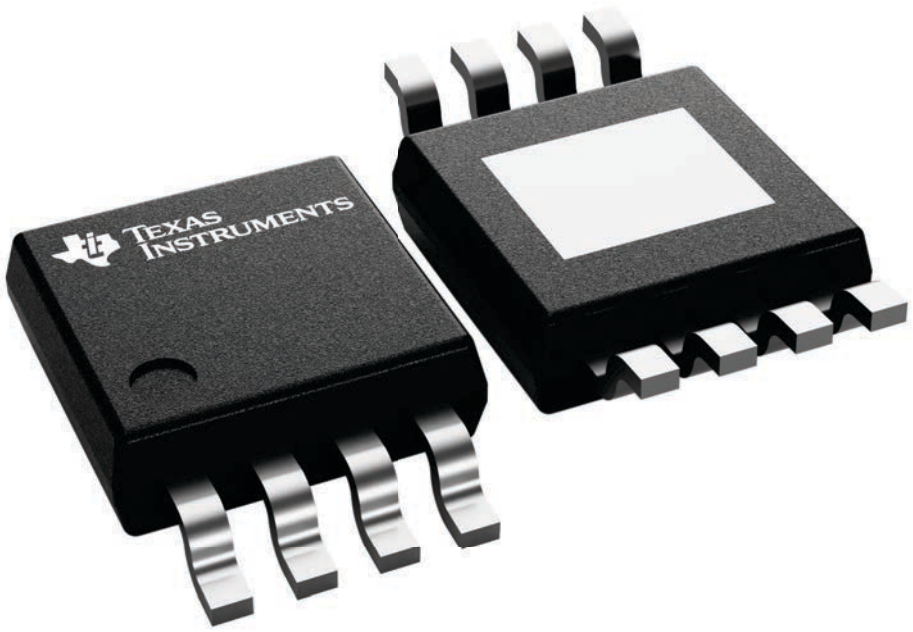
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



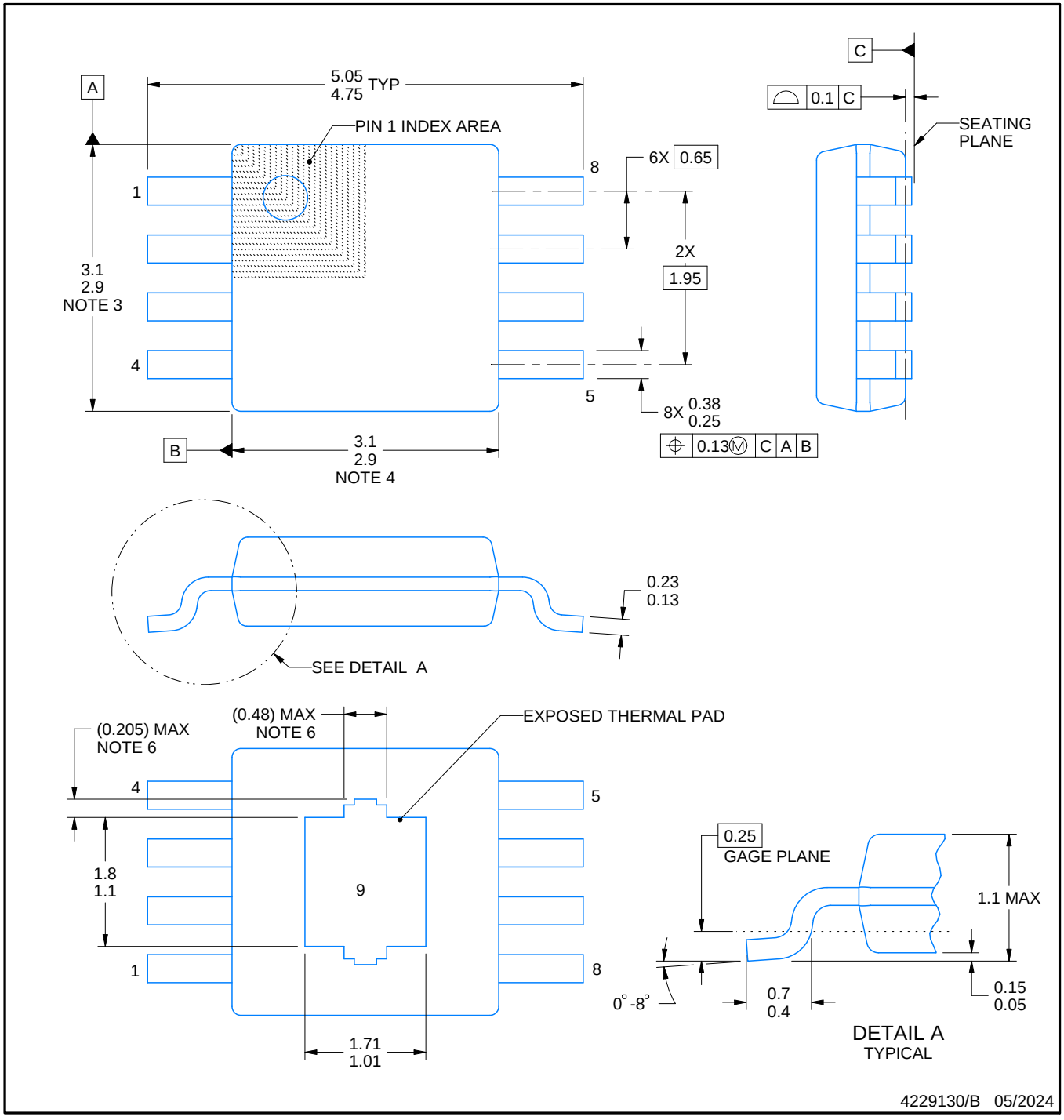
4225482/B

PACKAGE OUTLINE

DGN0008H

PowerPAD™ VSSOP - 1.1 mm max height

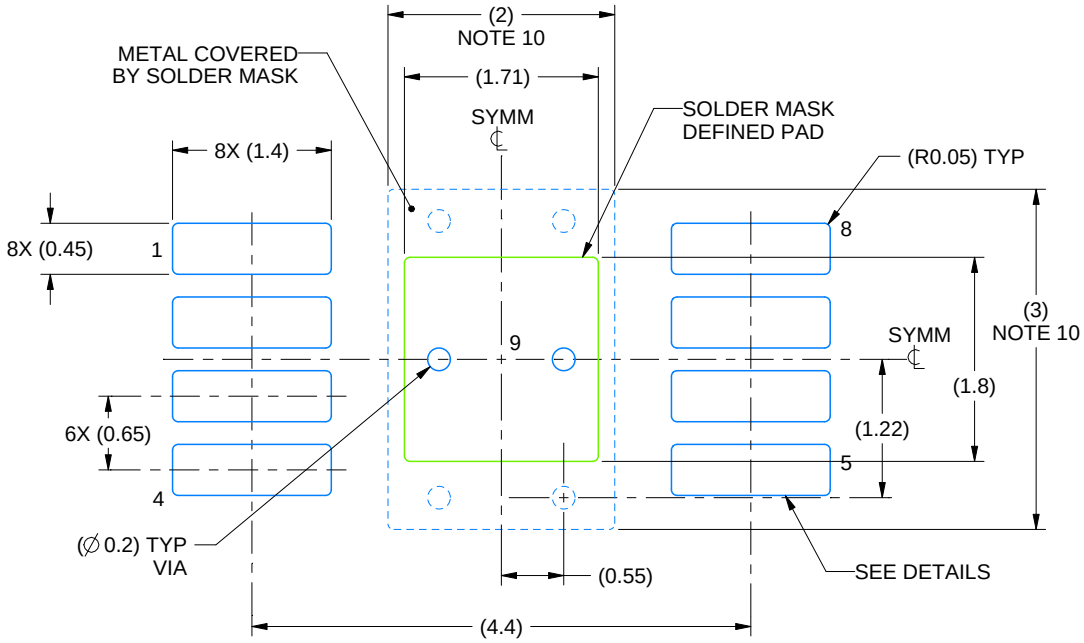
SMALL OUTLINE PACKAGE



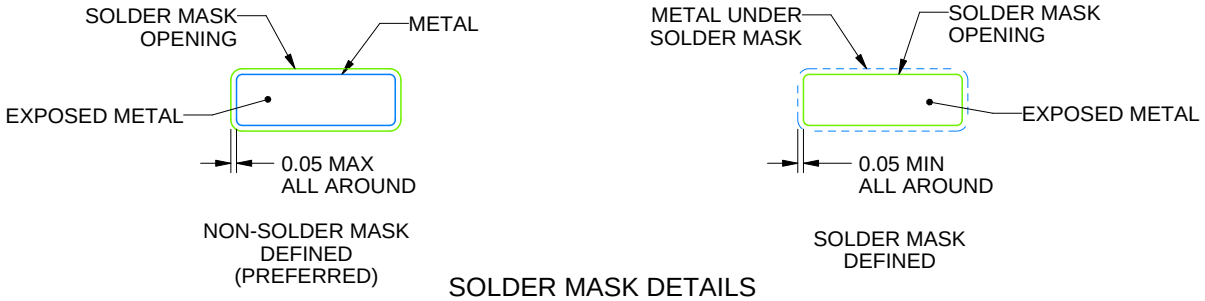
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.
6. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

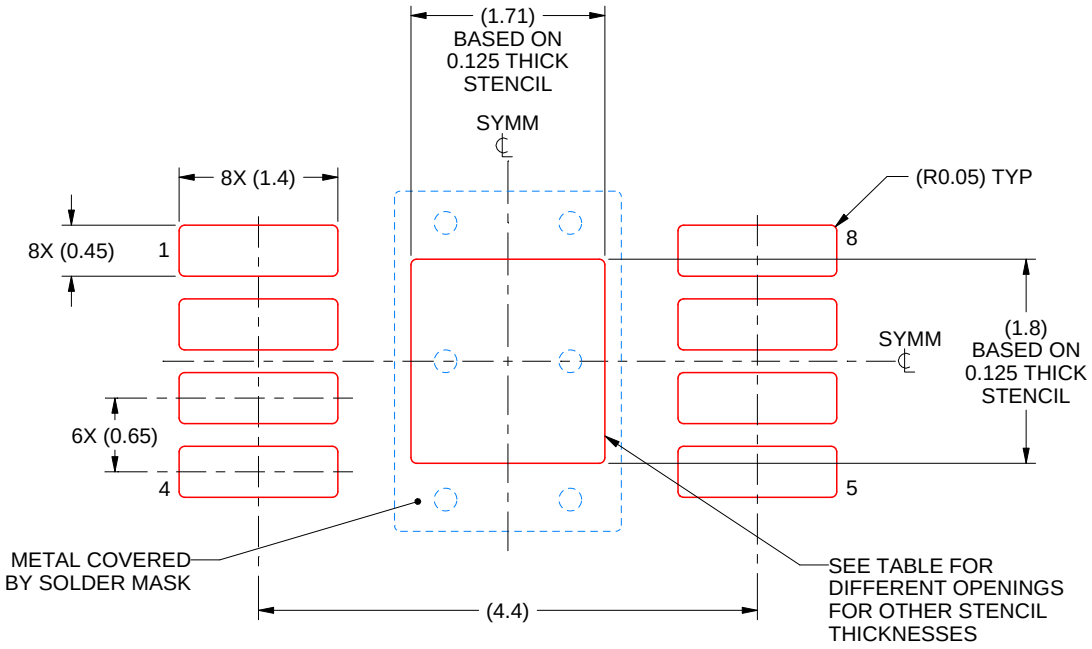


SOLDER MASK DETAILS

4229130/B 05/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



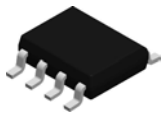
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.91 X 2.01
0.125	1.71 X 1.80 (SHOWN)
0.15	1.56 X 1.64
0.175	1.45 X 1.52

4229130/B 05/2024

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

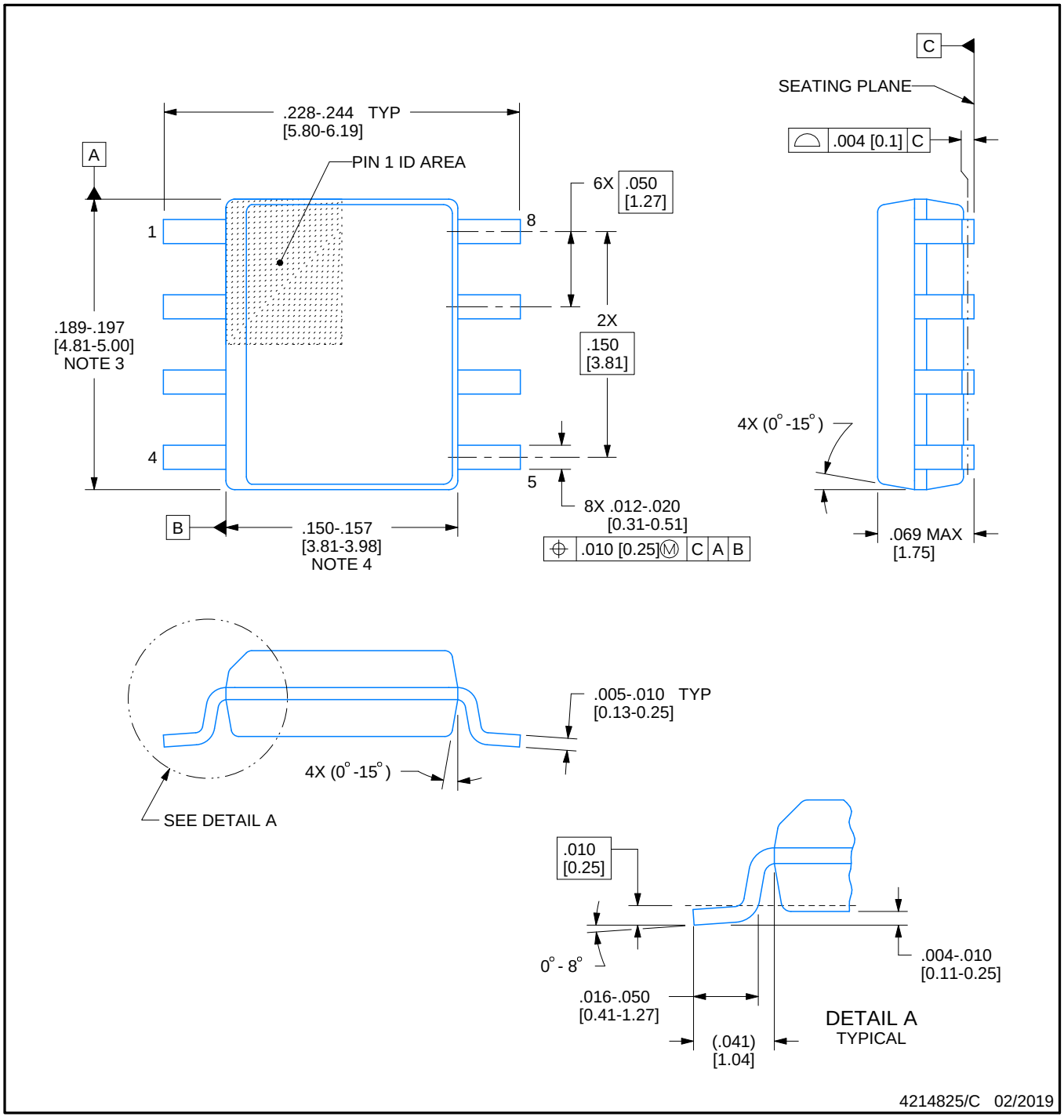


PACKAGE OUTLINE

D0008A

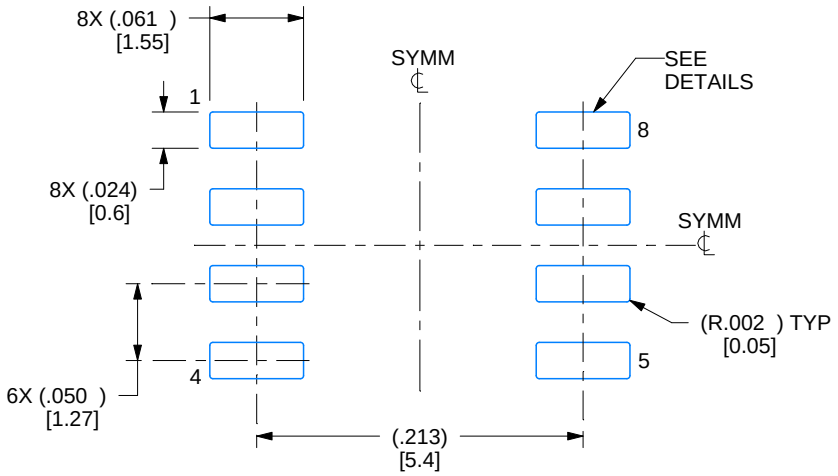
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

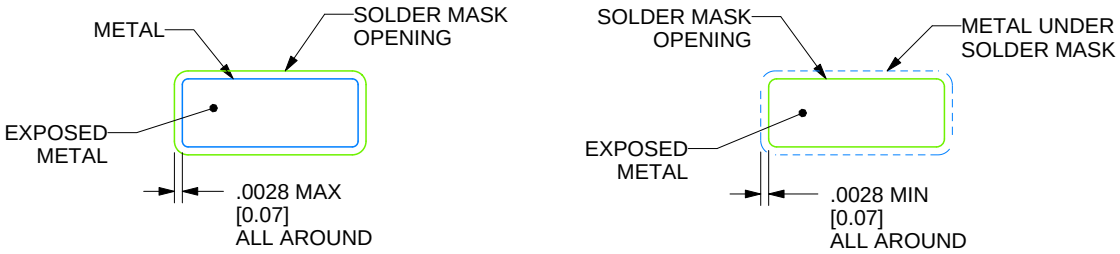


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

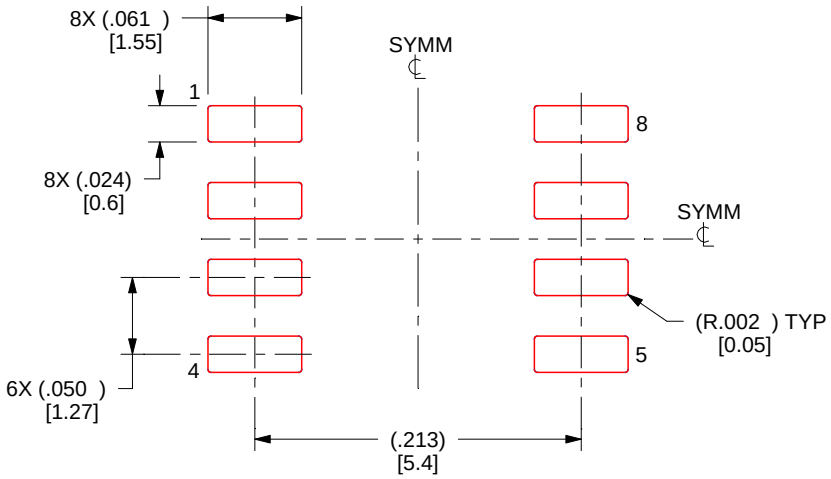
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

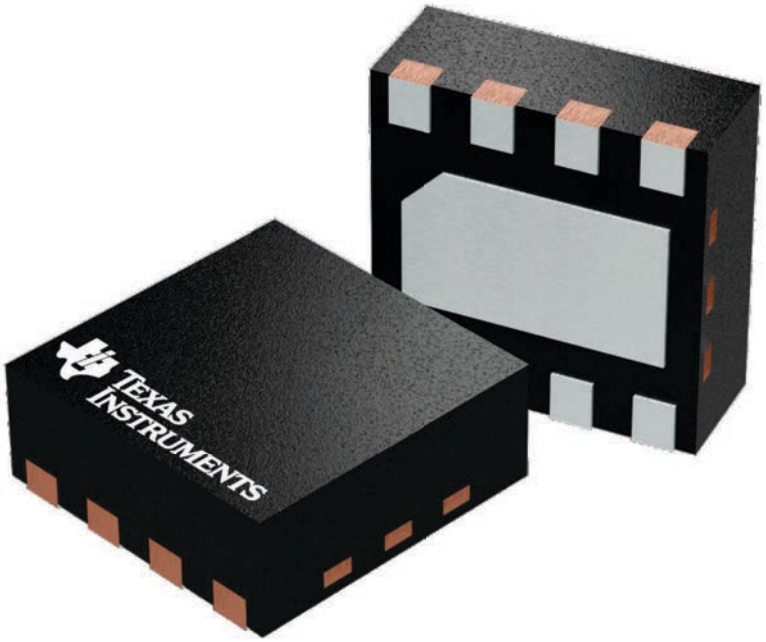
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



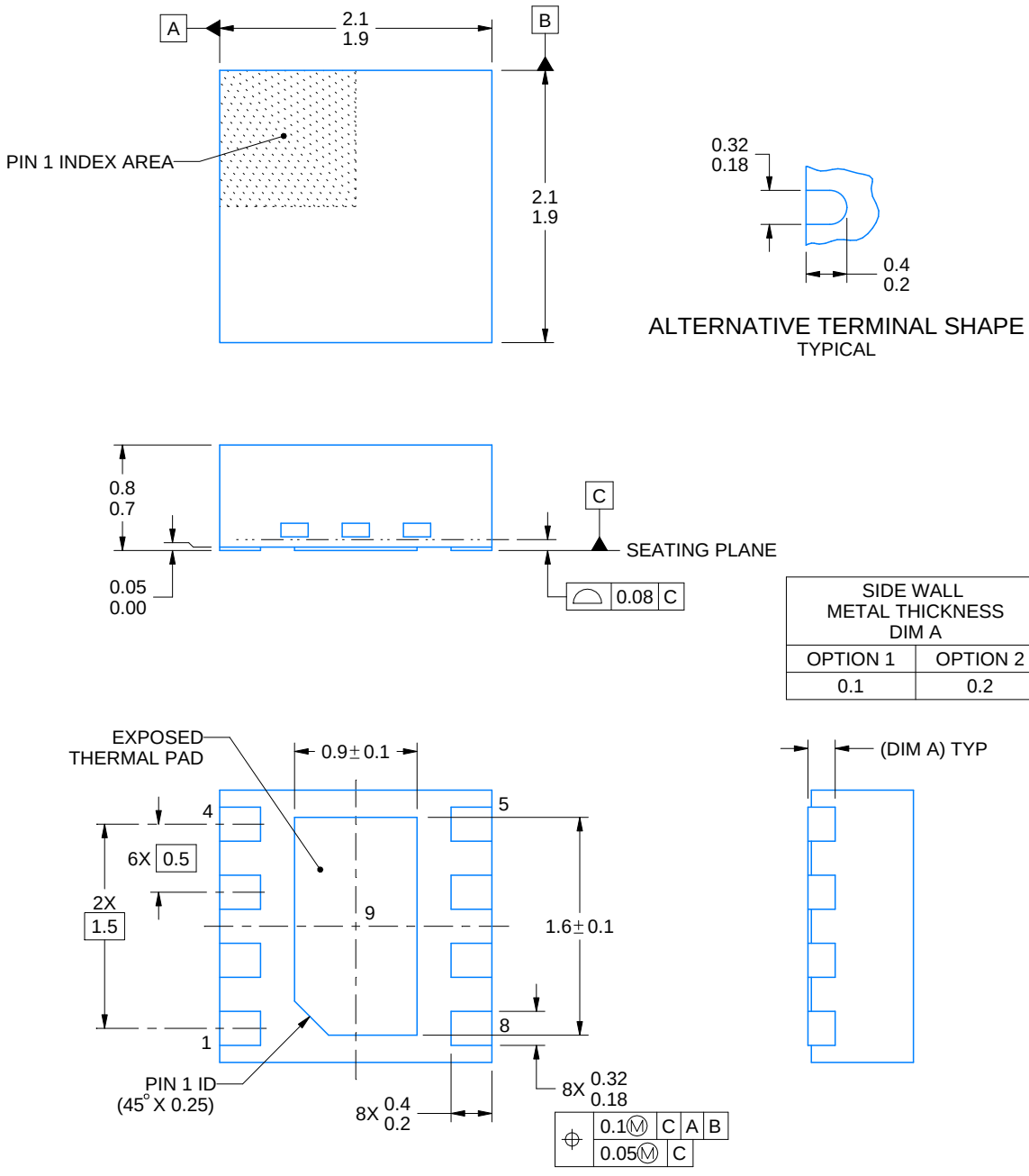
4224783/A

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

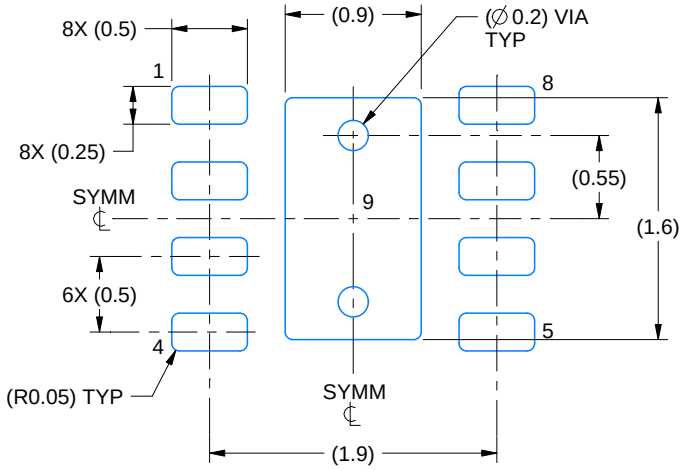
PLASTIC SMALL OUTLINE - NO LEAD



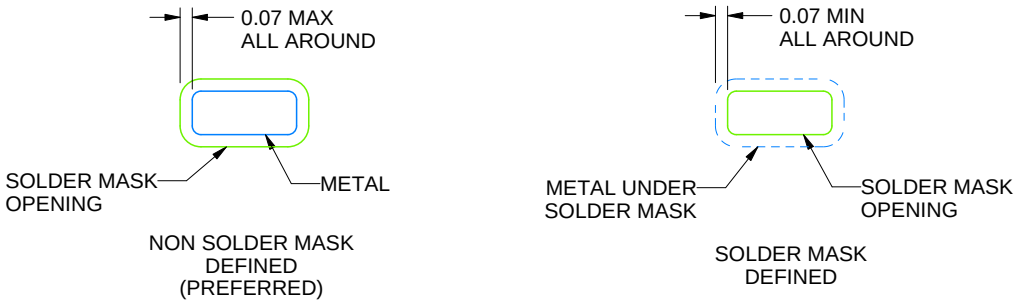
4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

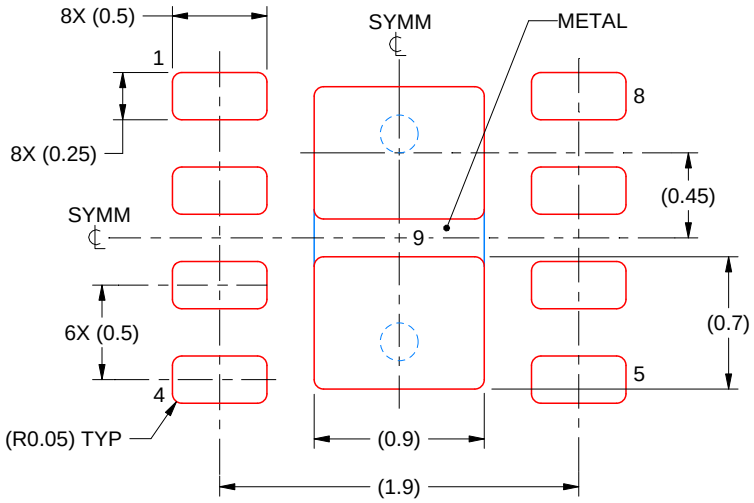


SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月