# UCC28731-Q1 Zero-Power 車載用スタンバイ PSR フライバック コントローラ

## 1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
  - デバイス温度グレード 1:-40℃～+125℃
  - デバイス HBM 分類レベル 2:±2kV
  - デバイス CDM 分類レベル C4B:±750V
- 機能安全対応
  - 機能安全システム設計に役立つ資料を利用可能
- Zero-Power: 5mW 未満の待機電力を実現
- 1 次側レギュレーション (PSR) によりオプトカプラが不要
- ラインおよび負荷範囲全体にわたる ±5% の電圧レギュレーションおよび電流レギュレーション
- 30V の最小スタートアップ電圧で 700V のスタートアップ スイッチ
- 83kHz の最大スイッチング周波数により低待機電力の充電器を設計可能
- 共振リング バレー スイッチング動作により全体効率を向上
- 周波数ディザリングにより EMI 準拠が容易
- クランプされた MOSFET 用ゲート駆動出力
- 過電圧、低ライン、過電流保護機能
- プログラミング可能なケーブル補償
- SOIC-7 パッケージ

## 2 アプリケーション

- ハイブリッド、電気自動車、およびパワートレイン システム
- トラクション インバータ:高電圧冗長およびバックアップ電源
- オンボード チャージャの 1 次側バイアス電源
- DC/DC コンバータのスタンバイ電源および補助電源

## 3 概要

UCC28731-Q1 絶縁型フライバック電源コントローラは、定電圧 (CV) および定電流 (CC) 出力レギュレーションをフォトカップラなしで実現することで基板面積と BOM (部品表) 点数を削減し、その寿命を通して高い信頼性を確保します。1 次側電源スイッチおよび補助フライバック巻線からの情報を処理することで、出力電圧および電流を精密にレギュレーションするため、「PSR」というラベルが付けられています。

32Hz の最小スイッチング周波数により、5mW 未満の無負荷時消費電力を容易に実現できます。内部の 700V スタートアップ スイッチ、動的に制御される動作状態、および適切に調整された変調プロファイルにより、スタートアップ時間を犠牲にすることなく、非常に低い待機電力を実現します。UCC28731-Q1 では、制御アルゴリズムによって、適用される規格を満たすまたは上回る動作効率を実現できます。バレー スイッチングによる不連続導通モード (DCM) 動作でスイッチング損失が低減されます。スイッチング周波数の変調 (FM) および 1 次側電流のピーク振幅の変調 (AM) により、負荷およびライン範囲の全体にわたって高い変換効率を保持します。

**製品情報**

| 部品番号 (1) | パッケージ | 本体サイズ (公称) |
|---|---|---|
| UCC28731QDRQ1 | SOIC (7) | 4.90 mm × 3.90mm |

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

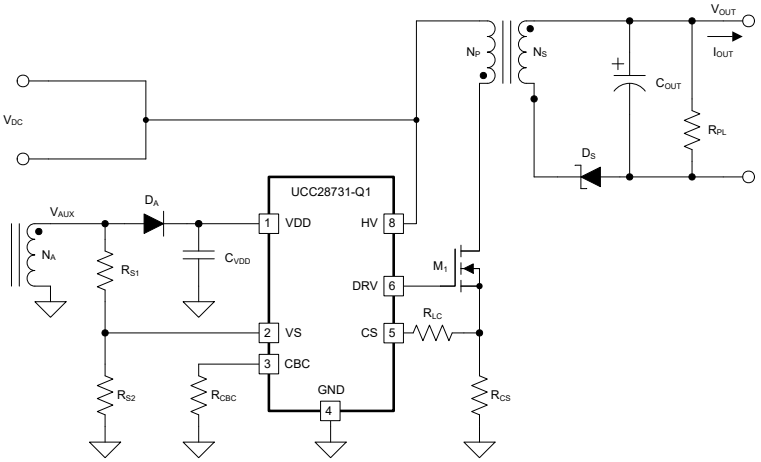


**図 3-1. 概略回路図**

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# 4 Pin Configuration and Functions

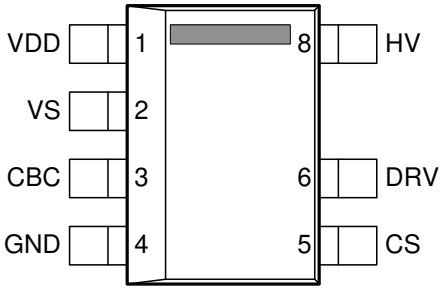



**図 4-1. D Package 7-Pin SOIC Top View**

## Pin Functions

| PIN[1] | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| CBC | 3 | I | This pin programs compensation of cable voltage drop with a resistor to GND. |
| CS | 5 | I | The current sense input pin connects to a ground-referenced current-sense resistor in series with the power switch. The resulting voltage is used to monitor and control the peak primary current. A series resistor can be added to this pin to compensate the peak switch current levels as the rectified bulk voltage varies. |
| DRV | 6 | O | This pin drives the gate of an external high-voltage MOSFET switching transistor. |
| GND | 4 | G | This pin is both the reference pin for the controller and the low-side return for the drive output. Special care should be taken to return all AC decoupling capacitors as close as possible to this pin and avoid any common trace length with power and signal return paths. |
| HV | 8 | I | This pin connects directly to the rectified bulk voltage and provides charge to the VDD capacitor for start-up of the power supply. |
| VDD | 1 | P | This pin supplies biased input to the controller and requires a carefully-placed bypass capacitor to GND. |
| VS | 2 | I | This pin provides voltage feed-back and demagnetization timing to the controller. This pin facilitates output voltage regulation, frequency limiting, constant-current control, line voltage detection, and output overvoltage detection. Connect this pin to a voltage divider between an auxiliary winding and GND. The value of the high-side resistor of this divider is used to program the AC-mains run and stop thresholds and line compensation at the CS pin. |

(1) P = Power, G = Ground, I = Input, O = Output, I/O = Input/Output

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage | HV | | 700 | V |
| | VDD | | 38 | V |
| | VS | –0.75 | 7 | V |
| | CS, CBC | –0.5 | 5 | V |
| | DRV | –0.5 | Self-limiting | V |
| Current | DRV, continuous sink | | 50 | mA |
| | DRV, source | | Self-limiting | mA |
| | VS, peak, 1% duty-cycle | | –1.2 | mA |
| Lead temperature 0.6 mm from case for 10 seconds | | | 260 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002(1) | ±2000 | V |
| | | Charged-device model (CDM), per AEC Q100-011(1) | ±750 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{VDD}$ | Bias-supply operating voltage | 9 | | 35 | V |
| $C_{VDD}$ | VDD by-pass capacitor | 0.047 | | | µF |
| $R_{CBC}$ | Cable-compensation resistance | 10 | | | kΩ |
| $I_{VS}$ | VS pin current, out of pin | | | 1 | mA |
| $T_J$ | Operating junction temperature | –40 | | 135 | °C |

## 5.4 Thermal Information

| THERMAL METRIC(1) | | UCC28731-Q1 D (SOIC) 7 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 128.0 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 59.3 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 66.7 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 17.0 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 65.9 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 5.5 Electrical Characteristics

over operating free-air temperature range, $V_{VDD}$ = 25 V, HV = open, $R_{CBC}$ = open, $T_A$ = -40°C to 125°C (unless otherwise noted)

| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **HIGH-VOLTAGE START-UP** | | | | | | |
| $I_{HV}$ | Start-up current out of VDD | $V_{HV}$ = 100V, $V_{VDD}$ = 0V, start state | 100 | 250 | 500 | µA |
| | | $V_{HV}$ = 30V, $V_{VDD}$ = $V_{VDD(on)}$–0.5V, start state | 100 | | 410 | |
| $I_{HVLKG25}$ | Leakage current into HV | $V_{HV}$ = 400V, run state, $T_J$ = 25°C | | 0.01 | 0.5 | µA |
| **BIAS SUPPLY INPUT CURRENT** | | | | | | |
| $I_{RUN}$ | Supply current, run | Run state, $I_{DRV}$ = 0A | | 2.1 | 2.65 | mA |
| $I_{WAIT}$ | Supply current, wait | Wait state, $I_{DRV}$ = 0A, $V_{VDD}$ = 20V | | 52 | 75 | µA |
| $I_{START}$ | Supply current, start | Start state, $I_{DRV}$ = 0A, $V_{VDD}$ = 18V, $I_{HV}$ = 0A | | 18 | 30 | µA |
| $I_{FAULT}$ | Supply current, fault | Fault state, $I_{DRV}$ = 0A | | 54 | 75 | µA |
| **UNDER-VOLTAGE LOCKOUT** | | | | | | |
| $V_{VDD(on)}$ | VDD turn-on threshold | $V_{VDD}$ low to high | 17.5 | 21 | 23 | V |
| $V_{VDD(off)}$ | VDD turn-off threshold | $V_{VDD}$ high to low | 7.3 | 7.7 | 8.1 | V |
| **VS INPUT** | | | | | | |
| $V_{VSR}$ | Regulating level | Measured at no-load condition, $T_J$ = 25°C | 4.00 | 4.04 | 4.08 | V |
| $V_{VSNC}$ | Negative clamp level below GND | $I_{VSLS}$ = –300µA | 190 | 250 | 325 | mV |
| $I_{VSB}$ | Input bias current | $V_{VS}$ = 4V | –0.25 | 0 | 0.25 | µA |
| **CS INPUT** | | | | | | |
| $V_{CST(max)}$ | CS maximum threshold voltage (2) | $V_{VS}$ = 3.7V | 710 | 740 | 770 | mV (2) |
| $V_{CST(min)}$ | CS minimum threshold voltage | $V_{VS}$ = 4.35V | 230 | 249 | 270 | mV |
| $K_{AM}$ | AM control ratio, $V_{CST(max)}$ / $V_{CST(min)}$ | | 2.75 | 2.99 | 3.20 | V/V |
| $V_{CCR}$ | Constant-current regulation factor | | 310 | 319 | 329 | mV |
| $K_{LC}$ | Line compensation current ratio, $I_{VSLS}$ / current out of CS pin | $I_{VSLS}$ = –300µA | 24 | 25.3 | 28 | A/A |
| **DRIVER** | | | | | | |
| $I_{DRS}$ | DRV source current | $V_{DRV}$ = 8V, $V_{VDD}$ = 9V | 20 | 29 | 35 | mA |
| $R_{DRVLS}$ | DRV low-side drive resistance | $I_{DRV}$ = 10mA | | 6 | 12 | Ω |
| $V_{DRCL}$ | DRV clamp voltage | $V_{VDD}$ = 35V | 13 | 14.5 | 16 | V |
| $R_{DRVSS}$ | DRV pull-down in start state | | 150 | 190 | 230 | kΩ |

over operating free-air temperature range, $V_{VDD}$ = 25 V, HV = open, $R_{CBC}$ = open, $T_A$ = -40°C to 125°C (unless otherwise noted)

| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **PROTECTION** | | | | | | |
| $V_{OVP}$ | Over-voltage threshold(1) | At VS input, $T_J$ = 25°C | 4.52 | 4.62 | 4.71 | V(1) |
| $V_{OCP}$ | Over-current threshold | At CS input | 1.4 | 1.5 | 1.6 | V |
| $I_{VSL(run)}$ | VS line-sense run current | Current out of VS pin increasing | 190 | 225 | 275 | µA |
| $I_{VSL(stop)}$ | VS line-sense stop current | Current out of VS pin decreasing | 70 | 80 | 100 | µA |
| $K_{VSL}$ | VS line-sense ratio, $I_{VSL(run)}$ / $I_{VSL(stop)}$ | | 2.45 | 2.8 | 3.05 | A/A |
| $T_{J(stop)}$ | Thermal shut-down temperature | Internal junction temperature | | 165 | | °C |
| **CABLE COMPENSATION** | | | | | | |
| $V_{CBC(max)}$ | Cable compensation output maximum voltage | Voltage at CBC at full load | 2.9 | 3.13 | 3.5 | V |
| $V_{CVS(min)}$ | Minimum compensation at VS | $V_{CBC}$ = open, change in VS regulating level from no load to full load | –50 | –15 | 20 | mV |
| $V_{CVS(max)}$ | Maximum compensation at VS | $V_{CBC}$ = 0V, change in VS regulating level from no load to full load | 275 | 325 | 375 | mV |

(1) The regulating level and OV threshold at VS decrease with increasing temperature by 1mV/°C. This compensation over temperature is included to reduce the variances in power supply output regulation and over-voltage detection with respect to the external output rectifier.
(2) These threshold voltages represent average levels. This device automatically varies the current sense thresholds to improve EMI performance.

## 5.6 Timing Requirements

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{CSLEB}$ | Leading-edge blanking time , DRV output duration, $V_{CS}$ = 1V | 170 | 225 | 280 | ns |
| $t_{ZTO}$ | Zero-crossing timeout delay, no zero-crossing detected | 1.6 | 2.2 | 2.9 | µs |

## 5.7 Switching Characteristics

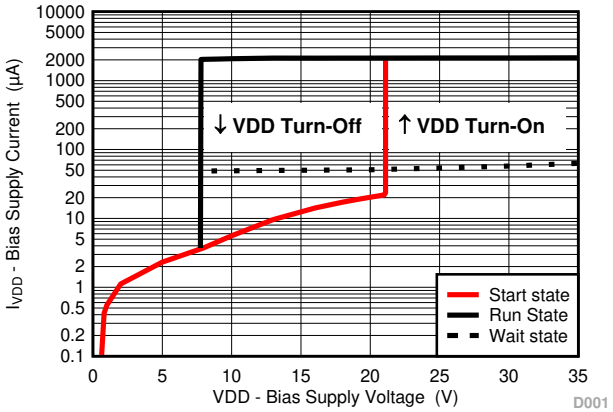
over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{SW(max)}$ | Maximum switching frequency(1) | $V_{VS}$ = 3.7V | 76.0 | 83.3 | 90.0 | kHz |
| $f_{SW(min)}$ | Minimum switching frequency | $V_{VS}$ = 4.35V | 25 | 32 | 37 | Hz |

(1) These frequency limits represent average levels. This device automatically varies the switching frequency to improve EMI performance.

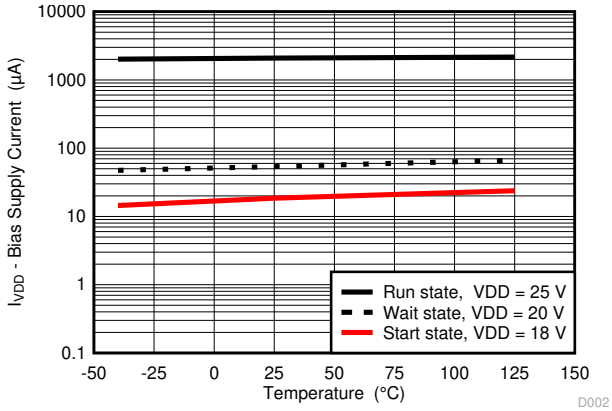
## 5.8 Typical Characteristics

$V_{VDD}$ = 25 V, $T_J$ = 25°C, unless otherwise noted.



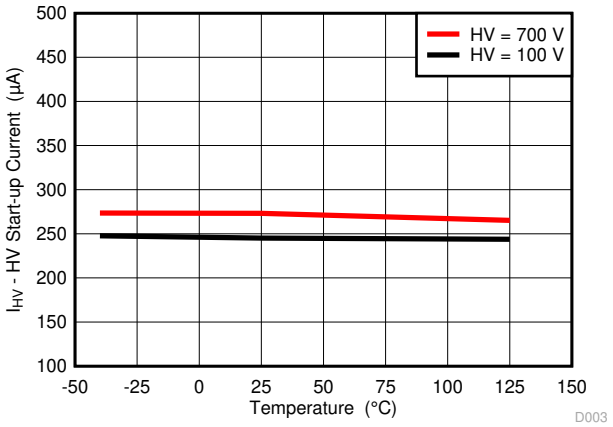

$I_{HV}$ = 0 A $I_{DRV}$ = 0 A

**図 5-1. Bias Supply Current vs. Bias Supply Voltage**



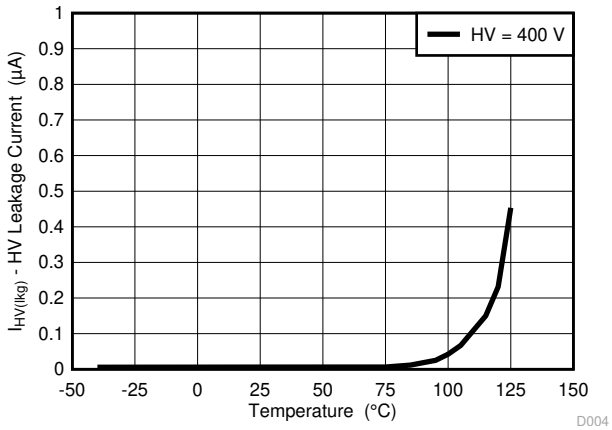

$I_{HV}$ = 0 A $I_{DRV}$ = 0 A

**図 5-2. Bias Supply Current vs. Temperature**




$V_{VDD}$ = 0 V

**図 5-3. HV Start-up Current vs. Temperature**




$V_{VDD}$ = 25 V

**図 5-4. HV Leakage Current vs. Temperature**

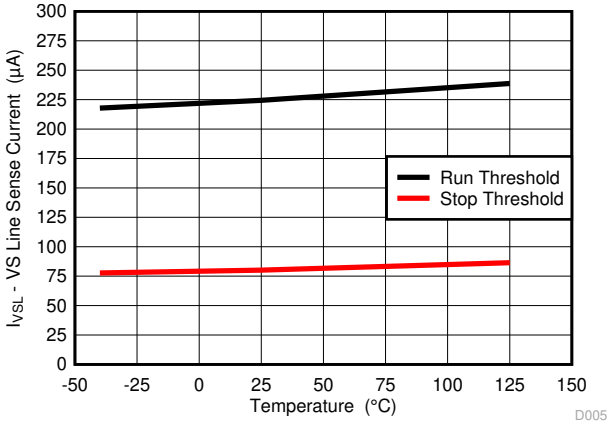



**図 5-5. VS Line-Sense Current vs. Temperature**

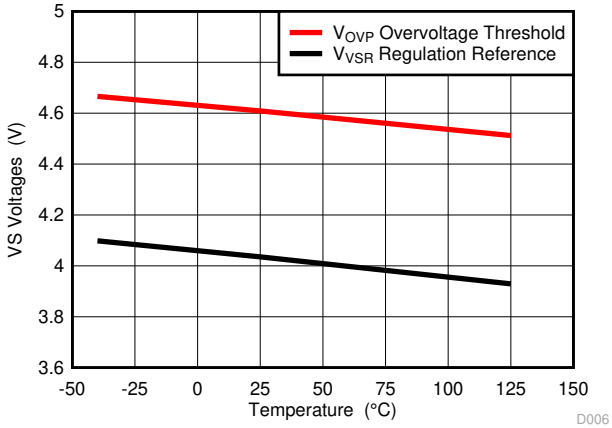



**図 5-6. VS Voltages vs. Temperature**

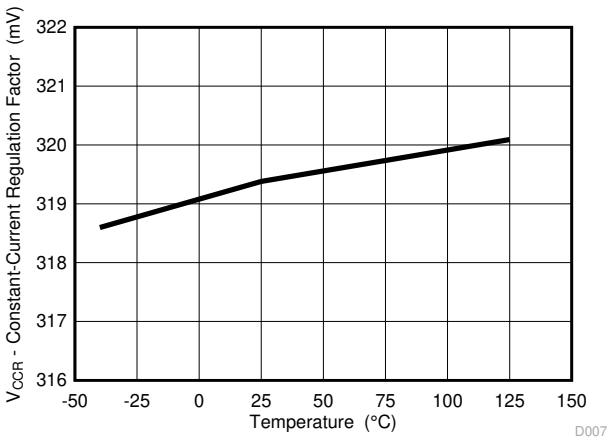



**図 5-7. Constant-Current Regulation Factor vs. Temperature**

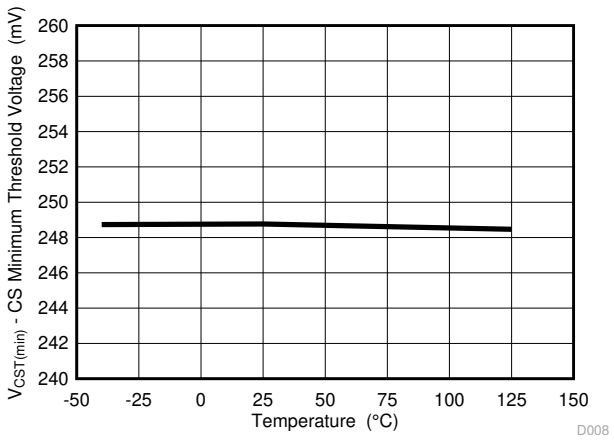
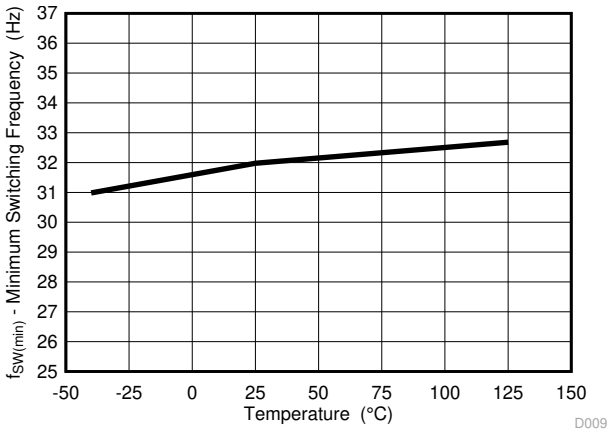
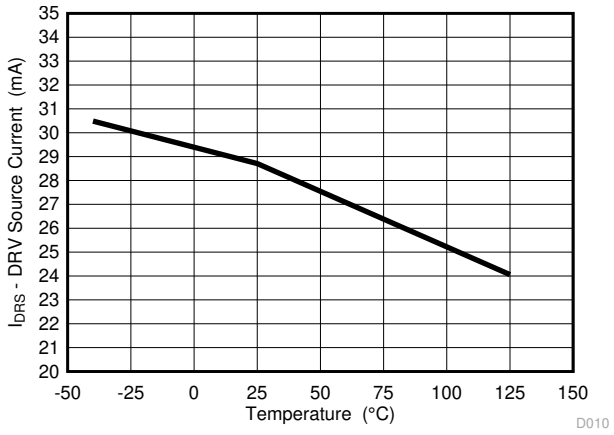



**図 5-8. CS Minimum Threshold Voltage vs. Temperature**




$V_{VS}$ = 4.35 V

**図 5-9. Minimum Switching Frequency vs. Temperature**




$V_{VDD}$ = 9 V $V_{DRV}$ = 8 V

**図 5-10. DRV Source Current vs. Temperature**

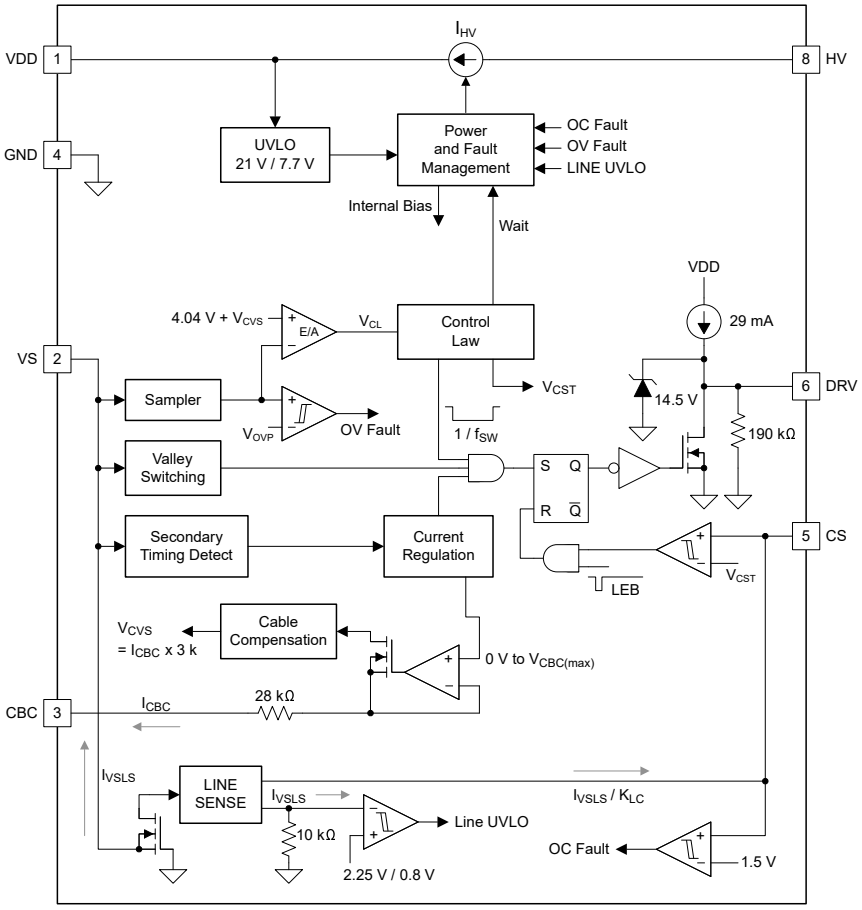
# 6 Detailed Description

## 6.1 Overview

The UCC28731-Q1 is an isolated-flyback power supply controller which provides accurate voltage and constant current regulation using primary-side winding sensing, eliminating the need for opto-coupler feedback circuits. The controller operates in discontinuous conduction mode with valley switching to minimize switching losses. The modulation scheme is a combination of frequency modulation and primary peak-current modulation to provide high conversion efficiency across the load range.

During low-power operating levels the device reduces the device operating current at switching frequencies less than 28 kHz. The UCC28731-Q1 includes features in the pulse-width modulator to reduce the EMI peak energy at the fundamental switching frequency and its harmonics. Accurate voltage and current regulation, fast dynamic response, and fault protection are achieved with primary-side control. A complete converter solution can be realized with a straightforward design process, low cost, and low component-count.

## 6.2 Functional Block Diagram



## 6.3 Feature Description

### *6.3.1 Detailed Pin Description*

#### 6.3.1.1 VDD (Device Bias Voltage Supply)

The VDD pin connects to a by-pass capacitor to ground. The turn-on UVLO threshold is 21V and turn-off UVLO threshold is 7.7V with an available operating range up to 35V on VDD. The typical USB charging specification requires the output current to operate in Constant-Current mode from 5V down to at least 2V, which is easily achieved with a nominal $V_{VDD}$ of approximately 20V. The additional VDD headroom up to 35V allows for $V_{VDD}$ to rise due to the leakage energy delivered to the VDD capacitor during high-load conditions.

#### 6.3.1.2 GND (Ground)

UCC28731-Q1 has a single ground reference external to the device for the gate-drive current and analog signal reference. Place the VDD-bypass capacitor close to GND and VDD with short traces to minimize noise on the VS and CS signal pins.

#### 6.3.1.3 HV (High Voltage Startup)

The HV pin connects directly to the bulk capacitor to provide startup current to the VDD capacitor. The typical startup current is approximately 250µA which provides fast charging of the VDD capacitor. The internal HV startup device is active until $V_{VDD}$ exceeds the turn-on UVLO threshold of 21V at which time the HV startup device turns off. In the off state the HV leakage current is very low to minimize stand-by losses of the controller. When $V_{VDD}$ falls below the 7.7V UVLO turn-off threshold the HV startup device turns on.

#### 6.3.1.4 DRV (Gate Drive)

The DRV pin connects to the MOSFET gate pin, usually through a series resistor. The gate driver provides a gate-drive signal limited to 14V. The turn-on characteristic of the driver is a 29mA current source which limits the turn-on dv/dt of the MOSFET drain and reduces the leading-edge current spike, while still providing a gate-drive current to overcome the Miller plateau. The gate-drive turn-off current is determined by the $R_{DS(on)}$ of the low-side driver and any external gate drive resistance. Adding external gate resistance reduces the MOSFET drain turn-off dv/dt, if necessary. Such resistance value is generally higher than the typical 10Ω commonly used to damp resonance. However, calculation of the external resistance value to achieve a specific dv/dt involves MOSFET parameters beyond the scope of this datasheet.

#### 6.3.1.5 CBC (Cable Compensation)

The cable compensation pin is connected to a resistor to ground to program the amount of output voltage compensation needed to offset cable resistance. The cable compensation circuit generates a 0 to 3.13V voltage level on the CBC pin corresponding to 0A to $I_{OCC}$ maximum output current. The resistance selected on the CBC pin programs a current mirror that is summed into the VS feedback divider therefore increasing the regulation voltage as $I_{OUT}$ increases. There is an internal series resistance of 28kΩ to the CBC pin which sets a maximum cable compensation for a 5V output to approximately 400mV when CBC is shorted to ground. The CBC resistance value can be determined using 式 1.

$$R_{CBC} = \frac{V_{CBC\,(max)} \times (V_{OCV} + V_F) \times 3\ k\Omega}{V_{VSR} \times V_{OCBC}} - 28\ k\Omega \quad (1)$$

where

- $V_{CBC(max)}$ is the maximum voltage at the cable compensation pin at the maximum converter output current (see セクション 5.5),
- $V_{OCV}$ is the regulated output voltage,
- $V_F$ is the diode forward voltage,
- $V_{VSR}$ is the CV regulating level at the VS input (see セクション 5.5),
- $V_{OCBC}$ is the target cable compensation voltage at the output terminals.

Note that the cable compensation does not change the overvoltage protection (OVP) threshold, $V_{OVP}$ (see セクション 5.5), so the operating margin to OVP is less when cable compensation is used.

#### 6.3.1.6 VS (Voltage Sense)

The VS pin connects to a resistor-divider from the auxiliary winding to ground and is used to sense input voltage, output voltage, and event timing. The auxiliary voltage waveform is sampled at the end of the transformer secondary current demagnetization time to provide an accurate representation of the output voltage. The waveform on the VS pin determines the timing information to achieve valley-switching, and the timing to control the duty-cycle of the transformer secondary current when in Constant-Current Mode. Avoid placing a filter capacitor on this input which interferes with accurate sensing of this waveform.

During the MOSFET on-time, this pin also senses VS current generated through $R_{S1}$ by the reflected bulk-capacitor voltage to provide for AC-input Run and Stop thresholds, and to compensate the current-sense threshold across the AC-input range. For the AC-input Run/Stop function, the Run threshold on VS is 225µA and the Stop threshold is 80µA.

At the end of off-time demagnetization, the reflected output voltage is sampled at this pin to provide regulation and overvoltage protection. The values for the auxiliary voltage-divider high-side-resistor, $R_{S1}$, and lower-resistor, $R_{S2}$, are determined by 式 2 and 式 3.

$$R_{S1} = \frac{\sqrt{2} \times V_{IN(run)}}{N_{PA} \times I_{VSL(run)}} \tag{2}$$

where

- $V_{IN(run)}$ is the target AC RMS voltage to enable turn-on of the controller (Run) (in case of DC input, leave out the $\sqrt{2}$ term in the equation),
- $I_{VSL(run)}$ is the Run-threshold for the current pulled out of the VS pin during the switch on-time (see セクション 5.5),
- $N_{PA}$ is the transformer primary-to-auxiliary turns-ratio.

$$R_{S2} = \frac{R_{S1} \times V_{VSR}}{N_{AS} \times (V_{OCV} + V_F) - V_{VSR}} \tag{3}$$

where

- $V_{OCV}$ is the converter regulated output voltage,
- $V_F$ is the output rectifier forward drop at near-zero current,
- $N_{AS}$ is the transformer auxiliary-to-secondary turns-ratio,
- $R_{S1}$ is the VS divider high-side resistance,
- $V_{VSR}$ is the CV regulating level at the VS input (see セクション 5.5).

When the UCC28730-Q1 is operating in the Wait state, the VS input is receptive to a wake-up signal superimposed upon the auxiliary winding waveform after the waveform meets either of two qualifying conditions. A high-level wake-up signal is considered to be detected if the amplitude at the VS input exceeds VWU(high) (2V) provided that any voltage at VS has been continuously below VWU(high) for the wake-up qualification delay tWDLY (8.5µs) after the demagnetization interval. A low-level wake-up signal is considered to be detected if the amplitude at the VS input exceeds VWU(low) (57mV) provided that any voltage at VS has been continuously below VWU(low) for the wake-up qualification delay tWDLY (8.5µs) after the demagnetization interval. The high\u0002level threshold accommodates signals generated by a low-impedance secondary-side driver while the low-level threshold detects signals generated by a high-impedance driver

#### 6.3.1.7 CS (Current Sense)

The current-sense pin connects to a series resistor ($R_{LC}$) to the current-sense resistor ($R_{CS}$). The maximum current-sense threshold ($V_{CST(max)}$) is approximately 0.74V for $I_{PP(max)}$ and minimum current-sense threshold ($V_{CST(min)}$) is approximately 0.25V for $I_{PP(min)}$. $R_{LC}$ provides the function of feed-forward line compensation to eliminate changes in $I_{PP}$ with input voltage due to the propagation delay of the internal comparator and MOSFET turn-off time. An internal leading-edge blanking time of 225ns eliminates sensitivity to the MOSFET turn-on current spike. It should not be necessary to place a bypass capacitor on the CS pin. The target output current in constant-current (CC) regulation determines the value of $R_{CS}$. The values of $R_{CS}$ and $R_{LC}$ are calculated by 式 4 and 式 5. The term $V_{CCR}$ is the product of the demagnetization constant, 0.432, and $V_{CST(max)}$. $V_{CCR}$ is held to a tighter accuracy than either of its constituent terms. The term $\eta_{XFMR}$ accounts for the energy stored in the transformer but not delivered to the secondary. This term includes transformer resistance and core loss, bias power, and primary-to-secondary leakage ratio.

**Example:** With a transformer core and winding loss of 5%, primary-to-secondary leakage inductance of 3.5%, and bias-power to output-power ratio of 0.5%, the $\eta_{XFMR}$ value at full-power is: 1 - 0.05 - 0.035 - 0.005 = 0.91.

$$R_{CS} = \frac{V_{CCR} \times N_{PS}}{2 \times I_{OCC}} \times \sqrt{\eta_{XFMR}} \tag{4}$$

where

- $V_{CCR}$ is a constant-current regulation factor (see セクション 5.5),
- $N_{PS}$ is the transformer primary-to-secondary turns-ratio, (a ratio of 13 to 15 is typical for a 5V output),
- $I_{OCC}$ is the target output current in constant-current regulation,
- $\eta_{XFMR}$ is the transformer efficiency at full-power output.

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times N_{PA} \times t_D}{L_P} \tag{5}$$

where

- $K_{LC}$ is a current-scaling constant for line compensation (see セクション 5.5),
- $R_{S1}$ is the VS pin high-side resistor value,
- $R_{CS}$ is the current-sense resistor value,
- $N_{PA}$ is the transformer primary-to-auxiliary turns-ratio,
- $t_D$ is the total current-sense delay consisting of MOSFET turn-off delay, plus approximately 50-ns internal delay,
- $L_P$ is the transformer primary inductance.

### 6.3.2 Primary-Side Regulation (PSR)

図 6-1 illustrates a simplified isolated-flyback convertor with the main voltage regulation blocks of the device shown. The power train operation is the same as any DCM flyback circuit but accurate output voltage and current sensing is the key to primary-side control. The output voltage is sensed as a reflected voltage during the transformer demagnetization time using a divider network at the VS input. The primary winding current is sensed at the CS input using a current-sense resistor, $R_{CS}$.

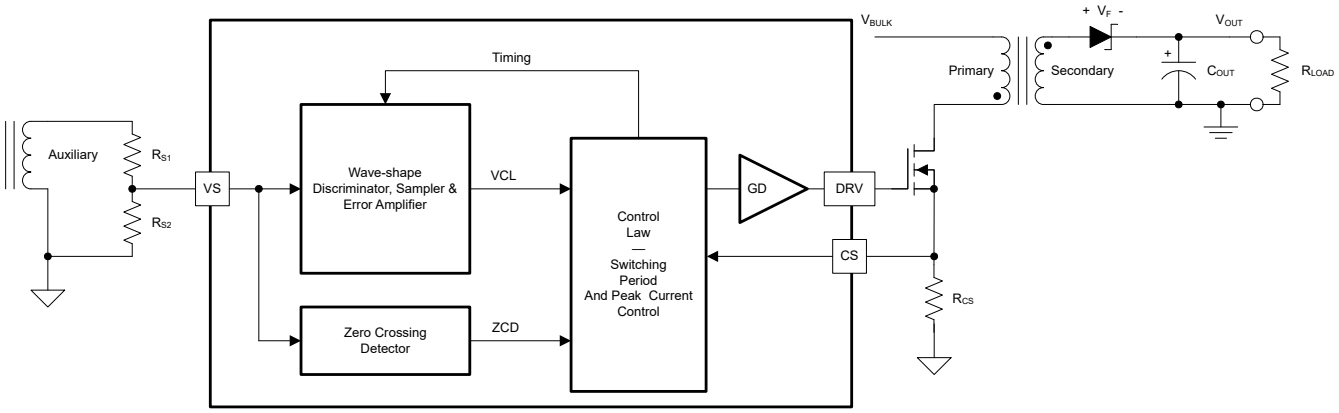



**図 6-1. Simplified Flyback Convertor (with the main voltage regulation blocks)**

In primary-side control, the output voltage is indirectly sensed on the auxiliary winding at the end of the transfer of stored transformer energy to the secondary. As shown in 図 6-2 it is clear there is a down slope representing a decreasing total rectifier $V_F$ and resistance voltage drop as the secondary current decreases to zero. To achieve an accurate representation of the secondary output voltage on the auxiliary winding, the discriminator reliably blocks the leakage inductance reset and ringing, continuously samples the auxiliary voltage during the down slope after the ringing is diminished, and captures the error signal at the time the secondary winding reaches zero current. The internal reference on VS is 4.04V. Temperature compensation on the VS reference voltage of -1mV/°C offsets the change in the forward voltage of the output rectifier with temperature. The resistor divider is selected as outlined in the VS pin description.

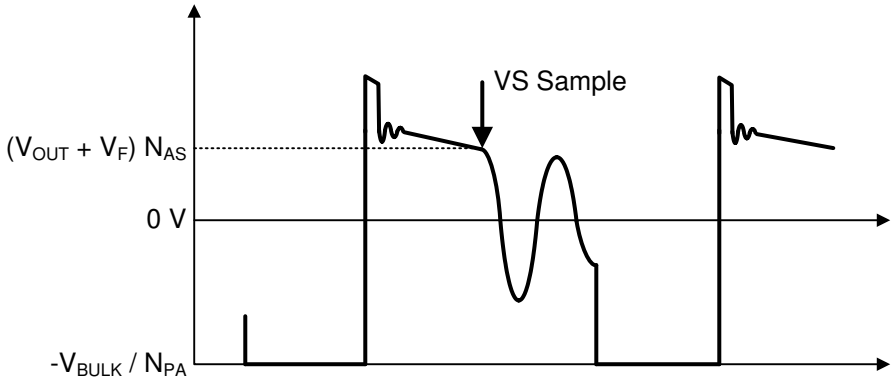



**図 6-2. Auxiliary Winding Voltage**

The UCC28731-Q1 VS-signal sampler includes signal discrimination methods to ensure an accurate sample of the output voltage from the auxiliary winding. There are, however, some details of the auxiliary winding signal which require attention to ensure reliable operation, specifically the reset time of the leakage inductance and the duration of any subsequent leakage inductance ring. Refer to 図 6-3 below for a detailed illustration of waveform criteria to ensure a reliable sample on the VS pin.

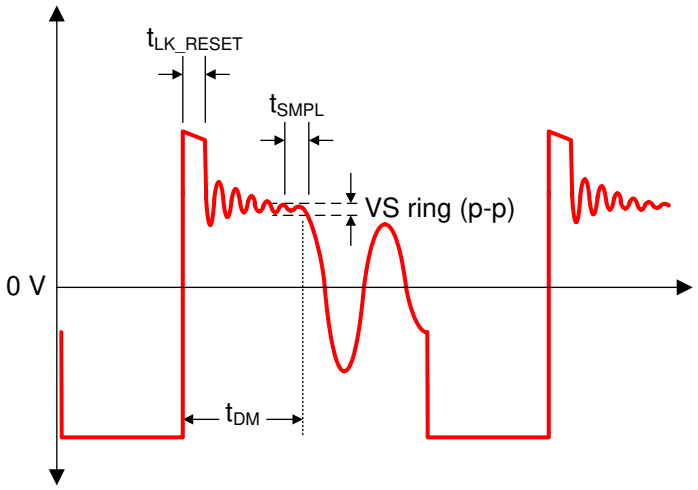



**図 6-3. Auxiliary Waveform Details**

The first detail to examine is the duration of the leakage inductance reset pedestal, $t_{LK\_RESET}$ in 図 6-3. Since this can mimic the waveform of the secondary current decay, followed by a sharp downslope, it is important to keep the leakage reset time to less than 750ns for $I_{PRI}$ minimum, and to less than 2.25µs for $I_{PRI}$ maximum.

The second detail is the amplitude of ringing on the $V_{AUX}$ waveform following $t_{LK\_RESET}$. The peak-to-peak voltage at the VS pin should be less than 125mV for at least 200ns before the end of the demagnetization time, $t_{DM}$. If there is a concern with excessive ringing, it usually occurs during light-load or no-load conditions, when $t_{DM}$ is at the minimum. To avoid distorting the signal waveform at VS with oscilloscope probe capacitance, it is recommended to probe the auxiliary winding to view the VS waveform characteristics. The tolerable ripple on VS is scaled up to the auxiliary-winding voltage by $R_{S1}$ and $R_{S2}$, and is equal to 125mV x ($R_{S1}$ + $R_{S2}$) / $R_{S2}$.

### *6.3.3 Primary-Side Constant Voltage Regulation*

During voltage regulation, the controller operates in frequency modulation and amplitude modulation modes according to the control law as illustrated in 図 6-4 below. The control law voltage $V_{CL}$ reflects the internal operating level based on the voltage-error amplifier output signal. Neither of these signals is accessible to the user, however the approximate $V_{CL}$ may be inferred from the frequency and amplitude of the current sense signal at the CS input. As the line and load conditions vary, $V_{CL}$ adjusts the operating frequency and amplitude as required to maintain regulation of the output voltage. Because the UCC28731-Q1 incorporates internal loop compensation, no external stability compensation is required.

The internal operating frequency limits of the device are $f_{SW(max)}$ and $f_{SW(min)}$, typically 83.3kHz and 32Hz, respectively. The choice of transformer primary inductance and primary-peak current sets the maximum operating frequency of the converter, which must be equal to or lower than $f_{SW(max)}$. Conversely, the choice of maximum target operating frequency and primary-peak current determines the transformer primary-inductance value. The actual minimum switching frequency for any particular converter depends on several factors, including minimum loading level, leakage inductance losses, switched-node capacitance losses, other switching and conduction losses, and bias-supply requirements. In any case, the minimum steady-state frequency of the converter must always exceed $f_{SW(min)}$ or the output voltage may rise to the overvoltage protection level (OVP) and the controller responds as described in セクション 6.3.7.

The steady-state Control-Law voltage, $V_{CL}$, ranges between 1.3 to 4.85V, depending on load, but may occasionally move below 0.75V or above 4.85V on load transients. Dropping below 0.75V shifts the switching frequency to a lower range at light loads, while exceeding 4.85V enters the constant-current mode of operation. There are 3 lower operating frequency ranges for progressively lighter loads, each overlapping the previous range to some extent, to provide stable regulation at very low frequencies. Peak-primary current is always maintained at $I_{PP(max)}/3$ in these lower frequency levels. Transitions between levels is automatically accomplished by the controller depending on the internal control-law voltage, $V_{CL}$.

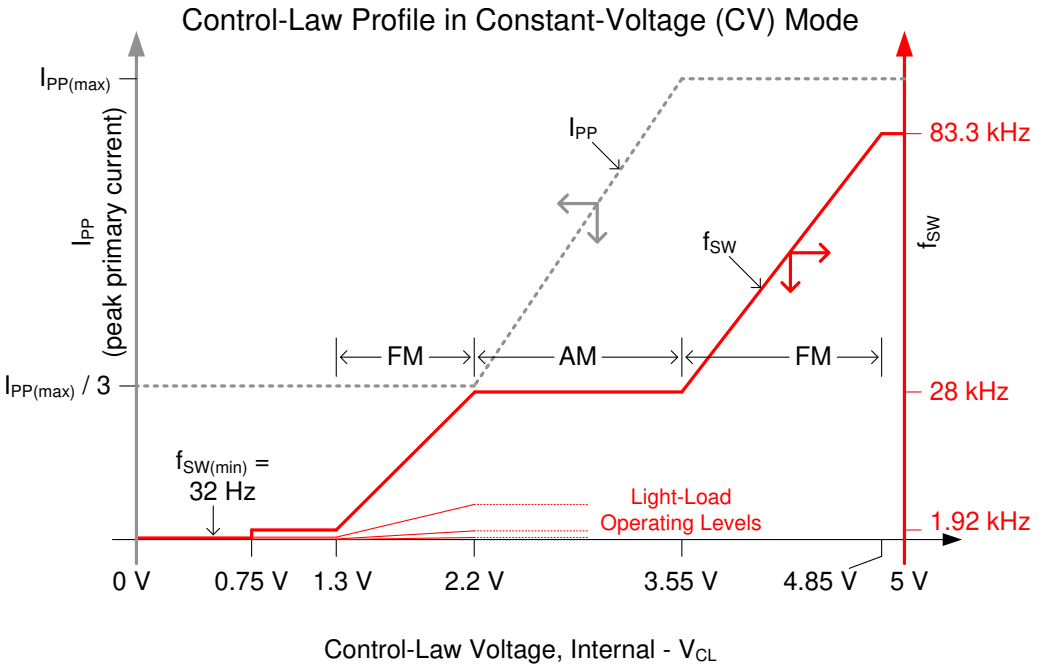



**図 6-4. Frequency and Amplitude Modulation Modes (during voltage regulation)**

### 6.3.4 Primary-Side Constant Current Regulation

Timing information at the VS pin and current information at the CS pin allow accurate regulation of the secondary average current. The control law dictates that as power is increased in CV regulation and approaching CC regulation the primary-peak current will be at $I_{PP(max)}$. Referring to 図 6-5 below, the primary-peak current, turns ratio, secondary demagnetization time ($t_{DM}$), and switching period ($t_{SW}$) determine the secondary average output current. Ignoring leakage inductance effects, the average output current is given by 式 6.

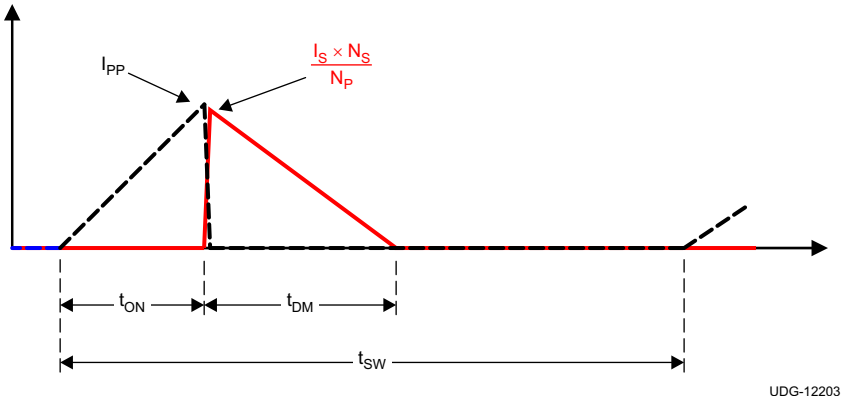



**図 6-5. Transformer Currents Relationship**

$$I_{OUT} = \frac{I_{PP}}{2} \times \frac{N_P}{N_S} \times \frac{t_{DM}}{t_{SW}} \quad (6)$$

When the average output current reaches the CC regulation reference in the current control block, the controller operates in frequency modulation mode to control the output current, $I_{OCC}$, at any output voltage down to or below the minimum operating voltage target, $V_{OCC}$ (as seen in 図 6-6), as long as the auxiliary winding can keep VDD voltage above the UVLO turn-off threshold. When $V_O$ falls so low that VDD cannot be sustained above UVLO, the device shuts down.

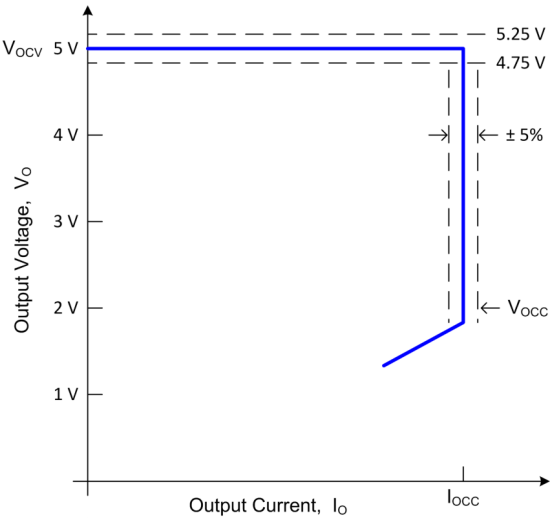



**図 6-6. Typical Output V-I Target Characteristic**

### 6.3.5 Valley-Switching and Valley-Skipping

The UCC28731-Q1 utilizes valley-switching to reduce switching losses in the MOSFET, to reduce induced-EMI, and to minimize the turn-on current spike at the current-sense resistor. The controller operates in valley-switching in all load conditions unless the $V_{DS}$ ringing is diminished to the point where valleys are no longer detectable.

As shown in 図 6-7, the UCC28731-Q1 operates in a valley-skipping mode (also known as valley-hopping) in most load conditions to maintain an accurate voltage or current regulation point and still switch on the lowest available $V_{DS}$ voltage.

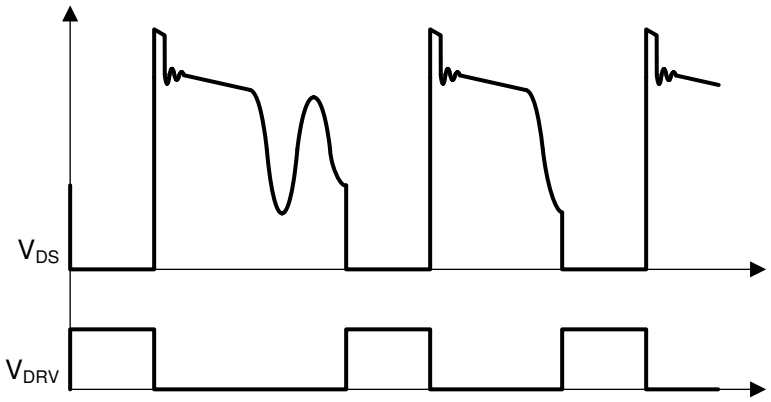



**図 6-7. Valley-Skipping Mode**

Valley-skipping modulates each switching cycle into discrete period durations. During FM operation, the switching cycles are periods when energy is delivered to the output in fixed packets, and the power delivered varies inversely with the switching period. During operating conditions when the switching period is relatively short, such as at high-load and low-line, the average power delivered per cycle varies significantly based on the number of valleys skipped between cycles. As a consequence, valley-skipping adds additional low-amplitude ripple voltage to the output with a frequency dependent upon the rate of change of the bulk voltage. For a load with an average power level between that of cycles with fewer valleys skipped and cycles with more valleys skipped, the voltage-control loop modulates the control law voltage and toggles between longer and shorter switching periods to match the required average output power.

### 6.3.6 Startup Operation

An internal high-voltage startup switch, connected to the bulk capacitor voltage ($V_{BULK}$) through the HV pin, charges the VDD capacitor. This startup switch functions similarly to a current source providing typically 250µA to charge the VDD capacitor. When $V_{VDD}$ reaches the 21V UVLO turn-on threshold, the controller is enabled, the converter starts switching, and the startup switch turns off.

At initial turn-on, the output capacitor is often in a fully-discharged state. The first 4 switching-cycle current peaks are limited to $I_{PP(min)}$ to monitor for any initial input or output faults with limited power delivery. After these 4 cycles, if the sampled voltage at VS is less than 1.32V, the controller operates in a special startup mode. In this mode, the primary-current-peak amplitude of each switching cycle is limited to approximately 0.67 x $I_{PP(max)}$ and $D_{MAGCC}$ increases from 0.432 to 0.650. These modifications to $I_{PP(max)}$ and $D_{MAGCC}$ during startup allow high-frequency charge-up of the output capacitor to avoid audible noise while the demagnetization voltage is low. Once the sampled VS voltage exceeds 1.36V, $D_{MAGCC}$ is restored to 0.432 and the primary-current peak resumes as $I_{PP(max)}$. While the output capacitor charges, the converter operates in CC mode to maintain a constant output current until the output voltage enters regulation. Thereafter, the controller responds to conditions as dictated by the control law. The time to reach output regulation consists of the time the VDD capacitor charges to $V_{VDD(on)}$ plus the time the output capacitor charges.

### 6.3.7 Fault Protection

The UCC28731-Q1 provides comprehensive fault protection. The protection functions include:

1. Output Overvoltage
2. Input Undervoltage
3. Internal Overtemperature
4. Primary Overcurrent fault
5. CS-pin Fault
6. VS-pin Fault

A UVLO reset and restart sequence applies to all fault-protection events.

The output-overvoltage function is determined by the voltage feedback on the VS pin. If the voltage sample of VS exceeds 4.6V for three consecutive switching cycles, the device stops switching and the internal current consumption becomes $I_{FAULT}$ which discharges the VDD capacitor to the UVLO-turn-off threshold. After that, the device returns to the start state and a start-up sequence ensues.

Current into the VS pin during the MOSFET on time determines the line-input run and stop voltages. While the VS pin clamps close to GND during the MOSFET on time, the current through $R_{S1}$ is monitored to determine a sample of $V_{BULK}$. A wide separation of the run and stop thresholds allows clean start-up and shut-down of the power supply with line voltage. The run-current threshold is 225µA and the Stop-current threshold is 80µA. The input AC voltage to run at start-up always corresponds to the peak voltage of the rectified line, because there is no loading on $C_{BULK}$ before start-up. The AC input voltage to stop varies with load since the minimum $V_{BULK}$ depends on the loading and the value of $C_{BULK}$. At maximum load, the stop voltage is close to the run voltage, but at no-load condition the stop voltage can be approximately 1/3 of the run voltage.

The UCC28731-Q1 always operates with cycle-by-cycle primary-peak current control. The normal operating range of the CS pin is 0.74 to 0.249V. An additional protection occurs if the CS pin reaches 1.5V after the leading-edge blanking interval for three consecutive cycles, which results in a UVLO reset and restart sequence.

Normally at initial start-up, the peak level of the primary current of the first four power cycles is limited to the minimum $V_{CST(min)}$. If the CS input is shorted or held low such that the $V_{CST(min)}$ level is not reached within 4µs on the first cycle, the CS input is presumed to be shorted to GND and the fault protection function results in a UVLO reset and restart sequence. Similarly, if the CS input is open, the internal voltage is pulled up to 1.5V for three consecutive switching cycles and the fault protection function results in a UVLO reset and restart sequence.

The internal overtemperature-protection threshold is 165°C. If the junction temperature reaches this threshold, the device initiates a UVLO-reset cycle. If the temperature is still high at the end of the UVLO cycle, the protection cycle repeats.

Protection is included in the event of component failures on the VS pin. If complete loss of feedback information on the VS pin occurs, the controller stops switching and restarts.

## 6.4 Device Functional Modes

According to the input voltage, the VDD voltage, and the output load conditions, the device can operate in different modes:

1. At start-up, when VDD is less than the $V_{VDD(on)}$ turn-on threshold, the HV internal current source is on and charging the VDD capacitor at a ($I_{HV}$ – $I_{START}$) rate.
2. When VDD exceeds $V_{VDD(on)}$, the HV source is turned Off and the device starts switching to deliver power to the converter output. Depending on the load conditions, the converter operates in CC mode or CV mode.
   a. CC mode means that the converter keeps the output current constant. When the output voltage is below the regulation level, the converter operates in CC mode to restore the output to the regulation voltage.
   b. CV mode means that the converter keeps the output voltage constant. When the load current is less than the current limit level, the converter operates in CV mode to keep the output voltage at the regulation level over the full load and input line ranges.
3. When operating in CV or CC mode where $I_{PP}$ is greater than 0.55 X $I_{PP(max)}$, the UCC28731-Q1 operates continuously in the run state. In this state, the VDD bias current is always at $I_{RUN}$ plus the average gate-drive current.
4. When operating in CV mode where $I_{PP}$ is less than 0.55 X $I_{PP(max)}$, the UCC28731-Q1 operates in the Wait state between switching cycles and in the run state during a switching cycle. In the Wait state, the VDD bias current is reduced to $I_{WAIT}$ after each switching cycle to improve efficiency at light loads.
5. The device operation can be stopped by the events listed below:
   a. If VDD drops below the $V_{VDD(off)}$ threshold, the device stops switching, its bias current consumption is lowered to $I_{START}$ and the internal HV current source is turned on until VDD rises above the $V_{VDD(on)}$ threshold. The device then resumes switching.
   b. If a fault condition is detected, the device stops switching and its bias current consumption is lowered to $I_{FAULT}$. This current level slowly the discharges VDD to $V_{VDD(off)}$ where the bias current changes from $I_{FAULT}$ to $I_{START}$ and the internal HV current source is turned on until VDD rises above the $V_{VDD(on)}$ threshold.
6. If a fault condition persists, the operation sequence described above in 2 repeats until the fault condition or the input voltage is removed.

# 7 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 7.1 Application Information

The UCC28731-Q1 device is a PSR controller optimized for isolated-flyback AC or DC-to-DC supply applications in the 5W to 50W range, providing constant-voltage (CV) mode control and constant current (CC) mode control for precise output regulation. Higher-power, multiple-output applications and other variations may also be supported. It is capable of switching at a very low frequency to facilitate achieving stand-by input power consumption of less than 5mW.

## 7.2 Typical Application

A typical application for the UCC28731-Q1 includes isolated DC-to-DC conversion from high voltage batteries to lower voltage rails like 12V or 15V. Commonly used in hyrbrid or electric vehicle powertrain systems, this type of power supply can provide a redundant power path. In case the 12V battery fails by crash or another malfunction, safety critial low voltage electronics for diagnostics, monitoring,and communication need to stay on. For applications demanding particularly high efficiency performance, a ground-referenced synchronous rectifier may also be used.

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This figure is simplified to illustrate the basic application of the UCC28731-Q1 and does not show all of the components and networks needed for an actual converter design, nor all of the possible circuit variations.

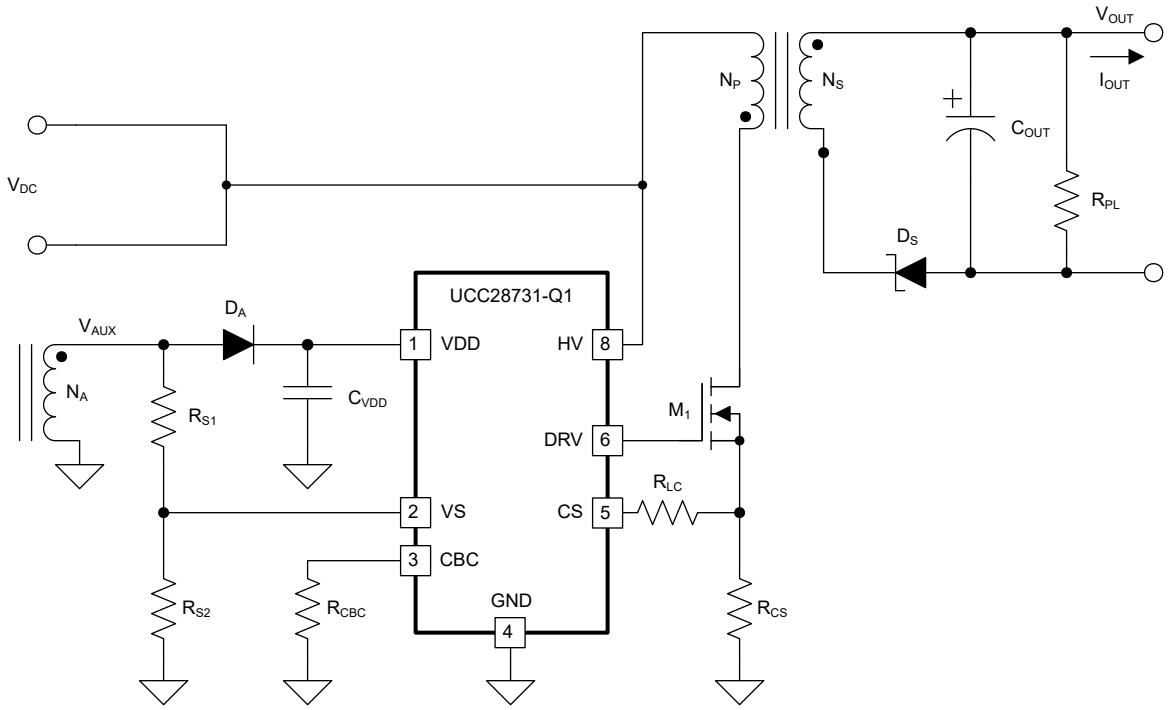


**図 7-1. Simplified Application with Ground Referenced Diode**

### 7.2.1 Design Requirements

The following table illustrates a typical subset of high-level design requirements for a particular converter, of which many of the parameter values are used in the various design equations in this section.

**表 7-1. Design Example Performance Requirements**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| $V_{IN}$ | AC-Line Input Voltage | | 85 | 115 / 230 | 264 | $V_{RMS}$ |
| $f_{LINE}$ | Line Frequency | | 47 | 50 / 60 | 63 | Hz |
| $V_{OCV}$ | Output Voltage, CV Mode | $V_{IN(min)} \le V_{IN} \le V_{IN(max)}$, $I_{OUT} \le I_{OCC}$ | 4.75 | 5.0 | 5.25 | V |
| $I_{OCC}$ | Output Current, CC Mode | $V_{IN(min)} \le V_{IN} \le V_{IN(max)}$, $I_{OUT} = I_{OCC}$ | 2.0 | 2.1 | 2.2 | A |
| $V_{RIPPLE}$ | Output Voltage Ripple | $V_{IN(min)} \le V_{IN} \le V_{IN(max)}$, $I_{OUT} \le I_{OCC}$ | | | 80 | $mV_{pp}$ |
| | Output Over-Voltage Limit | | | 5.6 | | V |
| | Output Over-Current Limit | | | 2.1 | | A |
| $V_{IN(run)}$ | Start-Up Input Voltage | $I_{OUT} = I_{OCC}$ | | 72 | | $V_{RMS}$ |
| $V_{OCC}$ | Minimum Output Voltage, CC Mode | $I_{OUT} = I_{OCC}$ | | | 2 | V |
| $\eta_{AVG}$ | Average Efficiency | Average of 25%, 50%, 75% 100% Load, at $V_{IN}$ = $115V_{RMS}$ and $230V_{RMS}$ | 80% | | | |
| $\eta_{10}$ | Light-Load Efficiency | 10 % Load, at $V_{IN}$ = $115V_{RMS}$ and $230V_{RMS}$ | 75% | | | |
| $P_{STBY}$ | Stand-by Input Power Consumption | $V_{IN}$ = $115V_{RMS}$ and $230V_{RMS}$ | | | 4.5 | mW |

Many other necessary design parameters, such as $f_{MAX}$ and $V_{BULK(min)}$ for example, may not be listed in such a table. These values may be selected based on design experience or other considerations, and may be iterated to obtain optimal results.

### 7.2.2 Detailed Design Procedure

This procedure outlines the steps to design a constant-voltage, constant-current flyback converter using the UCC28731-Q1 controller. Refer to 図 7-6 for component names and network locations. The design procedure equations use terms that are defined below. The primary-side and secondary-side snubbers or clamps are not designed in this procedure.

#### 7.2.2.1 Input Bulk Capacitance and Minimum Bulk Voltage

Bulk capacitance may consist of one or more capacitors connected in parallel, often with some inductance between them to suppress differential-mode conducted noise. EMI filter design is beyond the scope of this procedure.

Determine the minimum voltage on the input capacitance, $C_{B1}$ and $C_{B2}$ total, in order to determine the maximum $N_P$ to $N_S$ turns ratio of the transformer. The input power of the converter based on target full-load efficiency, minimum input RMS voltage, and minimum AC input frequency are used to determine the input capacitance value.

Maximum input power is used in the $C_{BULK}$ calculation and is determined by the $V_{OCV}$, $I_{OCC}$, and full-load efficiency targets.

$$P_{IN} = \frac{V_{OCV} \times I_{OCC}}{\eta} \tag{7}$$

The below equation provides an accurate solution for input capacitance needed to achieve a minimum bulk valley voltage target $V_{BULK(min)}$, accounting for hold-up during any loss of AC power for a certain number of half-cycles, $N_{HC}$, by an AC-line drop-out condition. Alternatively, if a given input capacitance value is prescribed, iterate the $V_{BULK(min)}$ value until that target capacitance is obtained, which determines the $V_{BULK(min)}$ expected for that capacitance.

$$C_{BULK} \geq \frac{2P_{IN} \times \left(0.25 + 0.5\, N_{HC} + \frac{1}{2\pi} \times \arcsin\left(\frac{V_{BULK\,(min)}}{\sqrt{2} \times V_{IN\,(min)}}\right)\right)}{\left(2\, V_{IN\,(min)}^2 - V_{BULK\,(min)}^2\right) \times f_{LINE}} \tag{8}$$

#### 7.2.2.2 Transformer Turns Ratio, Inductance, Primary-Peak Current

The maximum primary-to-secondary turns ratio can be determined by the target maximum switching frequency at full load, the minimum input capacitor bulk voltage, and the estimated DCM quasi-resonant time.

First, determine the maximum duty cycle of the MOSFET based on the target maximum switching frequency, $f_{MAX}$, the secondary conduction duty cycle, $D_{MAGCC}$, and the DCM resonant period, $t_R$. For $t_R$, assume 2µs (500kHz resonant frequency), if you do not have an estimate from experience or previous designs. For the transition mode operation limit, the time interval from the end of the secondary current conduction to the first resonant valley of the $V_{DS}$ voltage is ½ of the DCM resonant period, or 1µs assuming 500kHz. Actual designs vary. $D_{MAX}$ can be determined using the equation below.

$$D_{MAX} = 1 - D_{MAGCC} - \left(\frac{t_R}{2} \times f_{MAX}\right) \quad (9)$$

$D_{MAGCC}$ is defined as the secondary diode conduction duty cycle during constant current, CC, operation. In the UCC28731-Q1, it is fixed internally at 0.432. Once $D_{MAX}$ is known, the ideal turns ratio of the primary-to-secondary windings can be determined with the equation below. The total voltage on the secondary winding needs to be determined, which is the total of $V_{OCV}$, the secondary rectifier drop $V_F$, and cable compensation voltage $V_{OCBC}$, if used. For 5V USB charger applications, for example, a turns ratio in the range of 13 to 15 is typically used.

$$N_{PS(ideal)} = \frac{D_{MAX} \times V_{BULK(min)}}{D_{MAGCC} \times (V_{OCV} + V_F + V_{OCBC})} \quad (10)$$

The actual turns ratio depends on the actual number of turns on each of the transformer windings. Choosing $N_{PS} > N_{PS(ideal)}$ results in an output power limit lower than ($V_{OCV}$ x $I_{OCC}$) when operating at $V_{IN(min)}$, and line-frequency ripple may appear on $V_{OUT}$. Choosing $N_{PS} < N_{PS(ideal)}$ allows full-power regulation down to $V_{IN(min)}$, but increases conduction losses and the reverse voltage stress on the output rectifier.

Once the actual turns ratio is determined from a detailed transformer design, use this ratio for the following parameter calculations.

The UCC28731-Q1 constant-current regulation is achieved by maintaining a maximum $D_{MAGCC}$ duty cycle of 0.432 at the maximum primary current setting. The transformer turns ratio and constant-current regulating factor determine the current-sense resistor, $R_{CS}$, for a regulated constant-current target, $I_{OCC}$. Actual implementation of $R_{CS}$ may consist of multiple parallel resistors to meet power rating and accuracy requirements.

Since not all of the energy stored in the transformer is transferred to the secondary output, a transformer efficiency term, $\eta_{XFMR}$, is used to account for the core and winding loss ratio, leakage inductance loss ratio, and primary bias power ratio with respect to the rated output power. At full load, an overall transformer efficiency estimate of 0.91, for example, includes ~3% leakage inductance loss, ~5% core and winding loss, and ~1% bias power. Actual loss ratios may vary from this example.

$$R_{CS} = \frac{V_{CCR} \times N_{PS}}{2I_{OCC}} \times \sqrt{\eta_{XFMR}} \tag{11}$$

The primary-transformer inductance can be calculated using the standard energy storage equation for flyback transformers. Primary current, maximum switching frequency and output and transformer power losses are included in the equation below.

Initially, determine the transformer peak primary current, $I_{PP(max)}$.

Peak-primary current is simply the maximum current-sense threshold divided by the current-sense resistance.

$$I_{PP(max)} = \frac{V_{CST(max)}}{R_{CS}} \tag{12}$$

Then, calculate the primary inductance of the transformer, $L_P$.

$$L_P = \frac{2 \times (V_{OCV} + V_F + V_{OCBC}) \times I_{OCC}}{I_{PP(max)}^2 \times f_{MAX} \times \eta_{XFMR}} \tag{13}$$

The auxiliary winding to secondary winding turns ratio, $N_{AS}$, is determined by the lowest target operating output voltage in constant current regulation, the VDD turn-off threshold of the UCC28731-Q1, and the forward diode drops in the respective winding networks.

$$N_{AS} = \frac{V_{VDD(off)} + V_{FA}}{V_{OCC} + V_F} \tag{14}$$

There is additional energy supplied to VDD from the transformer leakage inductance energy which may allow a lower turns ratio to be used in many designs.

#### 7.2.2.3 Transformer Parameter Verification

The transformer turns ratio selected affects the MOSFET $V_{DS}$ and secondary rectifier reverse voltage $V_{REV}$, these should be reviewed.

The secondary rectifier reverse voltage stress is determined by the equation below. A snubber around the rectifier may be necessary to suppress any voltage spike, due to secondary leakage inductance, which adds to $V_{REV}$.

$$V_{REV} = \frac{V_{IN(max)} \times \sqrt{2}}{N_{PS}} + V_{OCV} + V_{OCBC} \quad (15)$$

For the MOSFET $V_{DS}$ peak stress, an estimated leakage inductance voltage spike, $V_{LK}$, should to be included.

$$V_{DSPK} = \left(V_{IN(max)} \times \sqrt{2}\right) + \left(V_{OCV} + V_F + V_{OCBC}\right) \times N_{PS} + V_{LK} \quad (16)$$

In the high-line, minimum-load condition, the UCC28731-Q1 requires a minimum on-time of the MOSFET ($t_{ON(min)}$) and minimum demagnetization time of the secondary rectifier ($t_{DMAG(min)}$). The selection of $f_{MAX}$, $L_P$ and $R_{CS}$ affects the actual minimum $t_{ON}$ and $t_{DMAG}$ achieved. The following equations are used to determine if the minimum $t_{ON}$ is greater than $t_{CSLEB}$ and minimum $t_{DMAG}$ target of >1.2µs is achieved.

$$t_{ON(min)} = \frac{L_P}{V_{IN(max)} \times \sqrt{2}} \times \frac{I_{PP(max)}}{K_{AM}} \quad (17)$$

$$t_{DMAG(min)} = \frac{t_{ON(min)} \times V_{IN(max)} \times \sqrt{2}}{N_{PS} \times \left(V_{OCV} + V_F\right)} \quad (18)$$

#### 7.2.2.4 Output Capacitance

With ordinary flyback converters, the output capacitance value is typically determined by the transient response requirement for a specific load step, $I_{TRAN}$, sometimes from a no-load condition. For example, in some USB charger applications, there is requirement to maintain a transient minimum $V_O$ of 4.1V with a load-step of 0mA to 500mA. 式 19 below assumes that the switching frequency can be at the UCC28730 minimum of $f_{SW(min)}$.

$$C_{OUT(No\_Wake)} \geq \frac{I_{TRAN} \left(\frac{1}{f_{SW(min)}} + 150\ \mu s\right)}{V_{O\Delta}} \quad (19)$$

This results in a $C_{OUT}$ value of over 17,000µF, unless a substantial pre-load is used to raise the minimum switching frequency. However, the wake-up feature allows the use of a much smaller value for $C_{OUT}$ because the wake-up response immediately cancels the Wait state and provides high-frequency power cycles to recover the output voltage from the load transient. The secondary-side voltage monitor UCC24650 provides the UCC28730 with a *wake-up* signal when it detects a -3% droop in output voltage.

$$C_{OUT} \geq \frac{1.2 \times I_{TRAN}}{\left(dV_{OUT}/dt\right)} \quad (20)$$

where

- $(dV_{OUT}/dt)$ is the slope at which the UCC24650 must detect the $V_{OUT}$ droop. Use a slope factor of 3700V/s or lower for this calculation.

The UCC28730 incorporates internal voltage-loop compensation circuits so that external compensation is not necessary, provided that the value of $C_{OUT}$ is high enough. The following equation determines a minimum value of $C_{OUT}$ necessary to maintain a phase margin of about 40 degrees over the full-load range. $K_{Co}$ is a dimensionless factor which has a value of 100.

$$C_{OUT} \geq K_{Co} \times \frac{I_{OCC}}{V_{OCV} \times f_{MAX}} \quad (21)$$

Another consideration for selecting the output capacitor(s) is the maximum ripple voltage requirement, $V_{RIPPLE(max)}$, which is reviewed based on the maximum output load, the secondary-peak current, and the equivalent series resistance (ESR) of the capacitor. The two major contributors to the output ripple voltage are the change in $V_{OUT}$ due to the charge and discharge of $C_{OUT}$ between each switching cycle and the step in $V_{OUT}$ due to the ESR of $C_{OUT}$. TI recommends an initial allocation of 33% of $V_{RIPPLE(max)}$ to ESR, 33% to $C_{OUT}$, and the remaining 33% to account for additional low-level ripple from EMI-dithering, valley-hopping, sampling noise and other random contributors. In 式 22, a margin of 50% is applied to the capacitor ESR requirement to allow for aging. In 式 23, set $\Delta V_{CQ}$ = 0.33 x $V_{RIPPLE(max)}$ to determine the minimum value of $C_{OUT}$ with regard to ripple voltage limitation. If other allocations of the allowable ripple voltage are desired, these equations may be adjusted accordingly.

$$ESR \leq \frac{0.33 \times V_{RIPPLE\ (max)}}{I_{PP\,(max)} \times N_{PS}} \times 0.50 \quad (22)$$

$$C_{OUT} \geq \frac{I_{OCC}}{\Delta V_{CQ} \times f_{MAX}} \quad (23)$$

Choose the largest value of the previous $C_{OUT}$ calculations for the minimum output capacitance. If the value of $C_{OUT}$ becomes excessive to meet a stringent ripple limitation, a C-L-C pi-filter arrangement can be considered to as an alternative to a simple capacitor-only filter. This arrangement is beyond the scope of this datasheet.

#### 7.2.2.5 VDD Capacitance, $C_{VDD}$

A capacitor is required on VDD to provide:

1. Run-state bias current during start-up while VDD falls toward UVLO, until $V_{OCC}$ is reached,
2. Wait-state bias current between steady-state low-frequency power cycles and
3. Wait-state bias current between minimum-frequency power cycles while $V_{OUT}$ recovers from a transient overshoot.

Generally, the value to satisfy (3) also satisfies (2) and (1), however the value for (1) may be the largest if the converter must provide high output current at a voltage below $V_{OCC}$ during power up.

The capacitance on VDD needs to supply the device operating current until the output of the converter reaches the target minimum operating voltage in constant-current regulation, $V_{OCC}$. At that point, the auxiliary winding can sustain the bias voltage to the UCC28731-Q1 above the UVLO shutdown threshold. The total current available to charge the output capacitors and supply an output load and is the constant-current regulation target, $I_{OCC}$.

式 24 assumes that all of the output current of the flyback is available to charge the output capacitance until the minimum output voltage is achieved. For margin, there is an estimated 1mA of average gate-drive current added to the run current and 1V added to the minimum VDD.

$$C_{VDD} \geq \frac{(I_{RUN} + 1\ mA) \times \frac{C_{OUT} \times V_{OCC}}{I_{OCC}}}{V_{VDD\,(on)} - (V_{VDD\,(off)} + 1\ V)} \tag{24}$$

At light loads, the UCC28731-Q1 enters a Wait-state between power cycles to minimize bias power and improve efficiency. 式 25 estimates the minimum capacitance needed to obtain a target maximum ripple voltage on VDD ($V_{VDD(max\Delta)}$ < 1V, for example) during the Wait state, which occurs at the lowest possible switching frequency.

$$C_{VDD} \geq \frac{I_{WAIT}}{V_{VDD\,(max\,\Delta)} \times f_{SW\,(min)}} \tag{25}$$

Choose the largest value of the previous $C_{VDD}$ calculations for the minimum VDD capacitance.

#### 7.2.2.6 VS Resistor Divider, Line Compensation, and Cable Compensation

The VS divider resistors determine the output voltage regulation point of the flyback converter. Also, the high-side divider resistor, $R_{S1}$, determines the line voltage at which the controller enables continuous DRV operation. $R_{S1}$ is initially determined based on the transformer primary to auxiliary turns ratio and the desired input voltage operating threshold.

$$R_{S1} = \frac{\sqrt{2} \times V_{IN(run)}}{N_{PA} \times I_{VSL(run)}} \tag{26}$$

The low-side VS divider resistor, $R_{S2}$, is selected based on the desired constant-voltage output regulation target, $V_{OCV}$.

$$R_{S2} = \frac{R_{S1} \times V_{VSR}}{N_{AS} \times (V_{OCV} + V_F) - V_{VSR}} \tag{27}$$

The UCC28731-Q1 can maintain tight constant-current regulation over input line by utilizing the line compensation feature. The line compensation resistor value, $R_{LC}$, is determined by various system parameters and the combined gate-drive turn-off and MOSFET turn-off delays, $t_D$. Assume a 50ns internal propagation delay in the UCC28731-Q1.

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times N_{PA} \times t_D}{L_P} \tag{28}$$

The UCC28731-Q1 provides adjustable cable compensation of up to approximately +8% of $V_{OCV}$ by connecting a resistor between the CBC terminal and GND. This compensation voltage, $V_{OCBC}$, represents the incremental increase in voltage, above the nominal no-load output voltage, needed to cancel or reduce the incremental decrease in voltage at the end of a cable due to its resistance. The programming resistance required for the desired cable compensation level at the converter output terminals can be determined using the equation below. As the load current changes, the cable compensation voltage also changes slowly to avoid disrupting control of the main output voltage. A sudden change in load current will induce a step change of output voltage at the end of the cable until the compensation voltage adjusts to the required level. Note that the cable compensation does not change the overvoltage protection (OVP) threshold,$V_{OVP}$ (see セクション 5.5), so the operating margin to OVP is less when cable compensation is used. If cable compensation is not required, CBC may remain unconnected.

$$R_{CBC} = \frac{V_{CBC(max)}}{V_{OCBC} \times \frac{V_{VSR}}{(V_{OCV} + V_F)}} \times 3\ k\Omega - 28\ k\Omega \tag{29}$$

### 7.2.3 Application Curves

The following figures indicate the transient response of a 5V, 10W flyback converter which receives a pulsed step-load of 2A while operating in the no-load stand-by condition. 図 7-5 indicates the no-load stand-by input power consumption achieved by this converter over the full AC input range. Zero-Power operation is achieved while retaining fast transient response to a full load step.

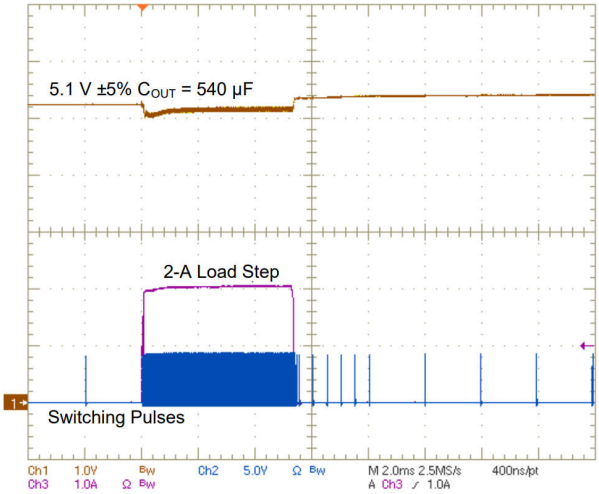


図 7-2. 2A Load Step During Stand-by Operation

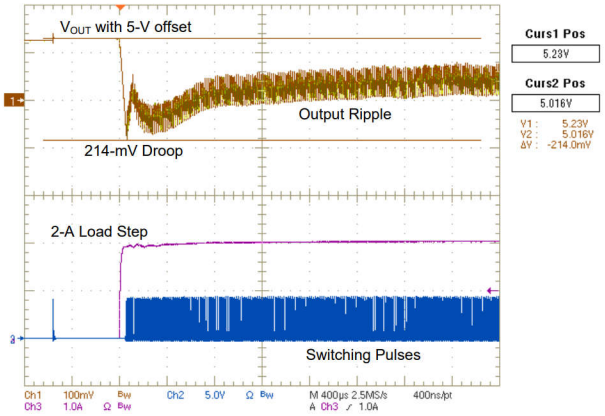


図 7-3. Transient Response Detail for 2A Load Step

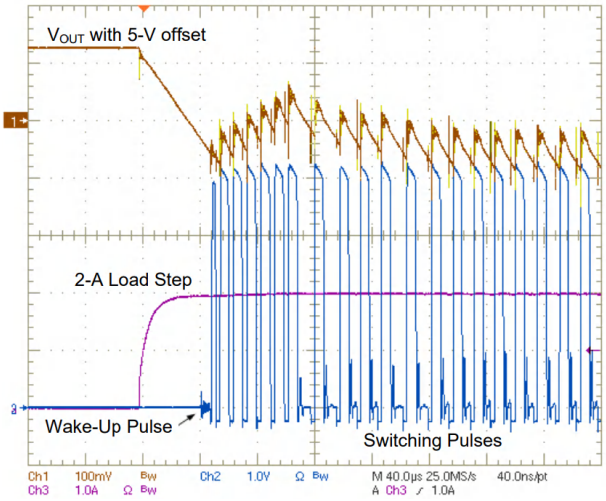


図 7-4. Wake-Up Pulse Triggering Response from UCC28730 Primary-Side Controller

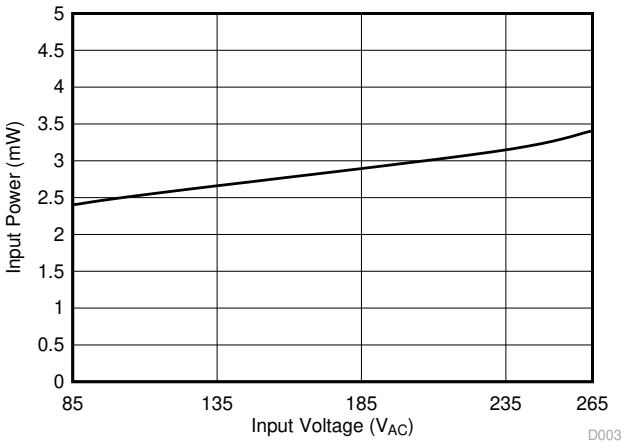


図 7-5. No-Load Input Power Consumption for a 5V, 10W Converter

## 7.3 Do's and Don'ts

- During no-load operation, do allow sufficient margin for variations in VDD level to avoid the UVLO shutdown threshold. Also, at no-load, keep the average switching frequency, <$f_{SW}$>, greater than 2 x $f_{SW(min)}$ to avoid a rise in output voltage.
- Do clean flux residue and contaminants from the PCB after assembly. Uncontrolled leakage current from VS to GND causes the output voltage to increase, while leakage current from HV or VDD to VS causes output voltage to decrease.
- If ceramic capacitors are used for VDD, do use quality parts with X7R or X5R dielectric rated 50 V or higher to minimize reduction of capacitance due to dc-bias voltage and temperature variation.
- Do not use leaky components if less than 5-mW stand-by input power consumption is a design requirement.
- Do not probe the VS node with an ordinary oscilloscope probe; the probe capacitance can alter the signal and disrupt regulation.
- Do observe VS indirectly by probing the auxiliary winding voltage at $R_{S1}$ and scaling the waveform by the VS divider ratio.

## 7.4 Power Supply Recommendations

The UCC28731-Q1 is intended for DC-to-DC converters using flyback toplogy in automotive systems like backsup supply in high voltage traction inverter, or On-Board Charger (OBC). It can also be used in other applications and converter topologies with different input voltages. Be sure that all voltages and currents are within the recommended operating conditions and absolute maximum ratings of the device.

The DRV output normally begins PWM pulses approximately 55µs after VDD exceeds the turn-on threshold $V_{VDD(on)}$. Avoid excessive dv/dt on VDD. Positive dv/dt greater than 1V/µs may delay the start of PWM . Negative dv/dt greater than 1V/µs on VDD which does not fall below the UVLO turn-off threshold $V_{VDD(off)}$ may result in a temporary dip in the output voltage.

## 7.5 Layout

### 7.5.1 Layout Guidelines

In order to increase the reliability and feasibility of the project it is recommended to adhere to the following guidelines for PCB layout.

1. Minimize stray capacitance on the VS node. Place the voltage sense resistors ($R_{S1}$ and $R_{S2}$ in セクション 7.2and セクション 7.5.2) close to the VS pin. Do not place tracks or planes under the VS net.
2. TI recommends to connect the HV input to a non-switching source of high voltage, not to the MOSFET drain, to avoid injecting high-frequency capacitive current pulses into the device.
3. Arrange the components to minimize the loop areas of the switching currents as much as possible. These areas include such loops as the transformer primary winding current loop, the MOSFET gate-drive loop, the primary snubber loop, the auxiliary winding loop and the secondary output current loop.

### 7.5.2 Layout Example

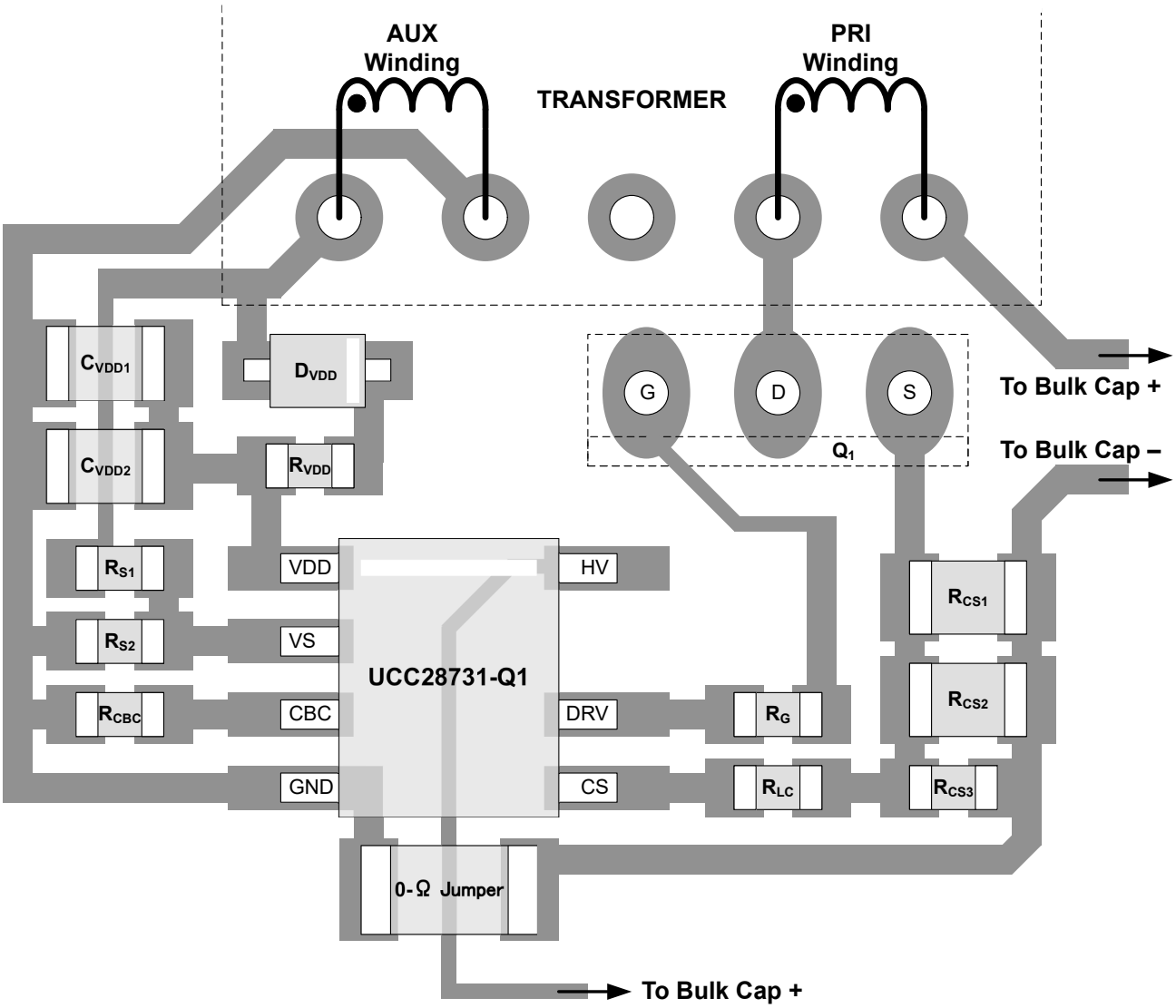


**図 7-6. UCC28731-Q1 Partial Layout Example**

# 8 Device and Documentation Support

## 8.1 Device Support

### *8.1.1 Device Nomenclature*

#### 8.1.1.1 Capacitance Terms in Farads

- $C_{BULK}$: total input capacitance of $C_{B1}$ and $C_{B2}$
- $C_{VDD}$: minimum required capacitance on the VDD pin
- $C_{OUT}$: minimum required output capacitance

#### 8.1.1.2 Duty-Cycle Terms

- $D_{MAGCC}$: secondary diode conduction duty-cycle constant while in CC mode, = 0.432
- $D_{MAX}$: maximum allowable MOSFET on-time duty-cycle
- $N_{HC}$: Number of half-cycles of the AC line frequency during a line drop-out

#### 8.1.1.3 Frequency Terms in Hertz

- $f_{LINE}$: minimum line frequency
- $f_{MAX}$: target full-load maximum switching frequency of the converter
- $f_{MIN}$: actual minimum switching frequency of the converter
- $f_{SW(max)}$: maximum switching frequency capability of the controller (see セクション 5.5)
- $f_{SW(min)}$: minimum switching frequency capability of the controller (see セクション 5.5)

#### 8.1.1.4 Current Terms in Amperes

- $I_{OCC}$: converter output constant-current target
- $I_{PP(max)}$: maximum transformer primary peak current
- $I_{START}$: VDD bias current before start-up (see セクション 5.5)
- $I_{TRAN}$: required positive load-step current
- $I_{WAIT}$: VDD bias current during the Wait-state (see セクション 5.5)
- $I_{VSL(run)}$: VS pin run current (see セクション 5.5)

#### 8.1.1.5 Current and Voltage Scaling Terms

- $K_{AM}$: ratio of maximum to minimum primary current peak amplitude (see セクション 5.5)
- $K_{LC}$: current scaling constant for line compensation (see セクション 5.5)
- $K_{Co}$: stability factor of 100, used in calculations for $C_{OUT}$

#### 8.1.1.6 Transformer Terms

- $L_P$: transformer primary inductance
- $N_{AS}$: transformer auxiliary to secondary turns ratio
- $N_{PA}$: transformer primary to auxiliary turns ratio
- $N_{PS}$: transformer primary to secondary turns ratio

#### 8.1.1.7 Power Terms in Watts

- $P_{IN}$: maximum input power of the converter at full-load
- $P_{OUT}$: output power of the converter at full-load
- $P_{STBY}$: total input power of the converter in stand-by condition

#### 8.1.1.8 Resistance Terms in Ω

- $R_{CS}$: primary-current programming resistance
- $R_{ESR}$: total ESR of the output capacitor(s)
- $R_{PL}$: pre-load resistance on the output of the converter
- $R_{S1}$: high-side resistance on VS input
- $R_{S2}$: low-side resistance on VS input

#### 8.1.1.9 Timing Terms in Seconds

- $t_D$: total current-sense delay including MOSFET turn-off delay; add 50 ns to MOSFET delay
- $t_{DMAG(min)}$: minimum secondary rectifier conduction time (transformer demagnetization time)
- $t_{ON(min)}$: minimum MOSFET on time
- $t_R$: period of the resonant ringing after $t_{DMAG}$

#### 8.1.1.10 DC Voltage Terms in Volts

- $V_{BULK}$: maximum bulk-capacitor voltage for standby power measurement
- $V_{BULK(min)}$: minimum valley voltage on bulk capacitor(s) at full power
- $V_{OCBC}$: target cable compensation voltage at the output terminals
- $V_{CBC(max)}$: maximum voltage at the CBC pin at maximum output current (see セクション 5.5)
- $V_{CCR}$: constant-current regulating factor voltage (see セクション 5.5)
- $V_{CST(max)}$: CS pin maximum current-sense threshold (see セクション 5.5)
- $V_{CST(min)}$: CS pin minimum current-sense threshold (see セクション 5.5)
- $V_{VDD(off)}$: UVLO turn-off threshold voltage (see セクション 5.5)
- $V_{VDD(on)}$: UVLO turn-on threshold voltage (see セクション 5.5)
- $V_{VDD(max\Delta)}$: maximum drop in VDD voltage between switching cycles during Wait state
- $V_{O\Delta}$: output voltage drop allowed during an output load transient
- $V_{DSPK}$: peak MOSFET drain-to-source voltage at high line
- $V_F$: secondary rectifier forward voltage drop at near-zero current
- $V_{FA}$: auxiliary rectifier forward voltage drop
- $V_{LK}$: estimated reset voltage of primary leakage inductance energy
- $V_{OCV}$: regulated output voltage of the converter
- $V_{OCC}$: target lowest output voltage in constant-current regulation
- $V_{REV}$: peak reverse voltage on the secondary rectifier
- $V_{RIPPLE}$: output peak-to-peak ripple voltage at full-load
- $V_{VSR}$: constant-voltage regulating level at the VS input (see セクション 5.5)
- $\Delta V_{CQ}$: allowable change in $C_{OUT}$ voltage due to load discharge between switching cycles

#### 8.1.1.11 AC Voltage Terms in Volts

- $V_{IN(max)}$: maximum AC input voltage to the converter
- $V_{IN(min)}$: minimum AC input voltage to the converter
- $V_{IN(run)}$: converter start-up (run) input voltage

#### 8.1.1.12 Efficiency Terms

- $\eta_{SB}$: estimated internal preload power efficiency of the flyback converter when its output power is zero. This efficiency is calculated by the converter internal preload power dissipated through $R_{PL}$, divided by total input power of the converter in stand-by condition, $P_{STBY}$. An estimation 50% can be used at beginning of a design.
- $\eta$: overall efficiency of the converter at full rated output power
- $\eta_{XFMR}$: power transfer efficiency of the transformer

## 8.2 Documentation Support

### *8.2.1 Related Documentation*

- UCC28730-Q1 Zero-Power Standby PSR Flyback Controller for Automotive, SLUSCR9
- Designing a Robust Traction Inverter Redundant Power Supply From 800 V Battery, SLUA987

## 8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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## 8.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

# 9 Revision History

| Changes from Revision * (June 2023) to Revision A (November 2024) | Page |
|---|---|
| • マーケティング ステータスを事前情報から初回リリースに更新 | 1 |

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| UCC28731QDRQ1 | Active | Production | SOIC (D) \| 7 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 28731Q |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

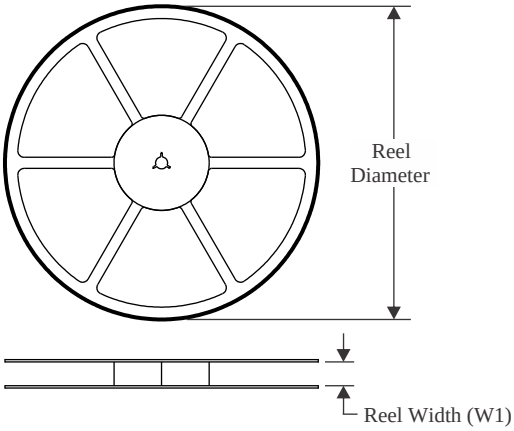
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

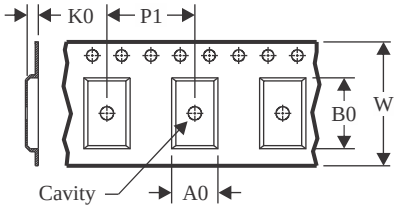
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

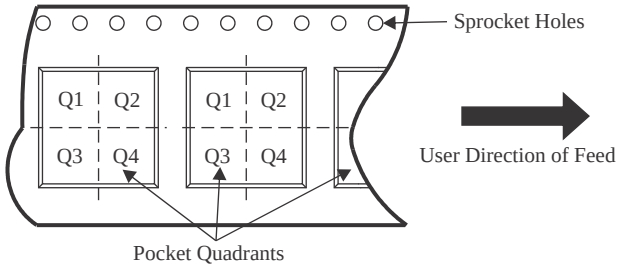



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

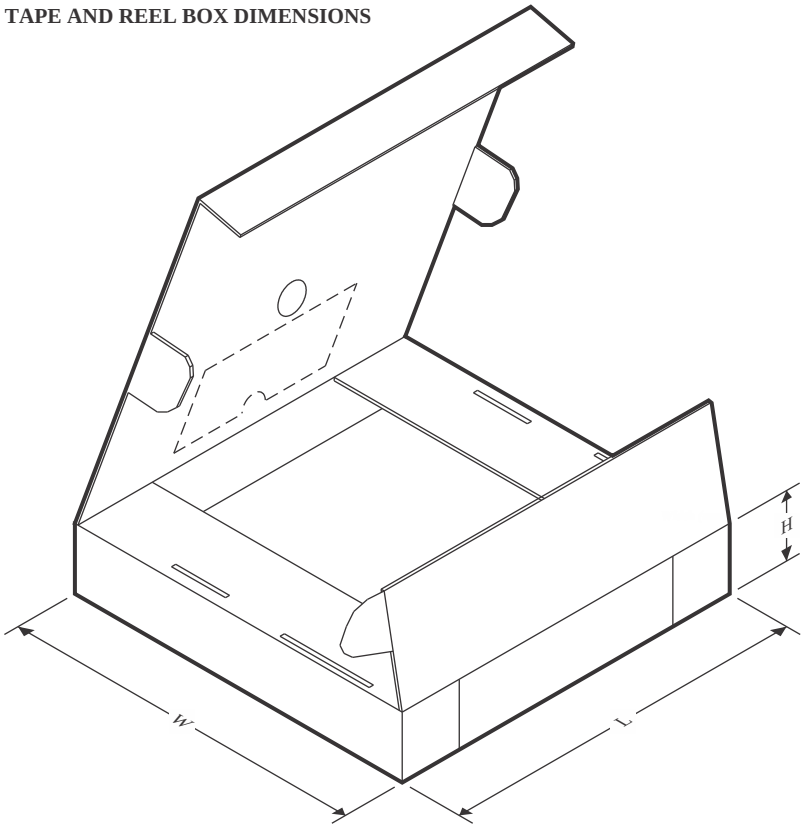
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

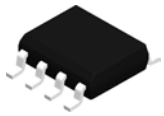
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UCC28731QDRQ1 | SOIC | D | 7 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| UCC28731QDRQ1 | SOIC | D | 7 | 2500 | 353.0 | 353.0 | 32.0 |

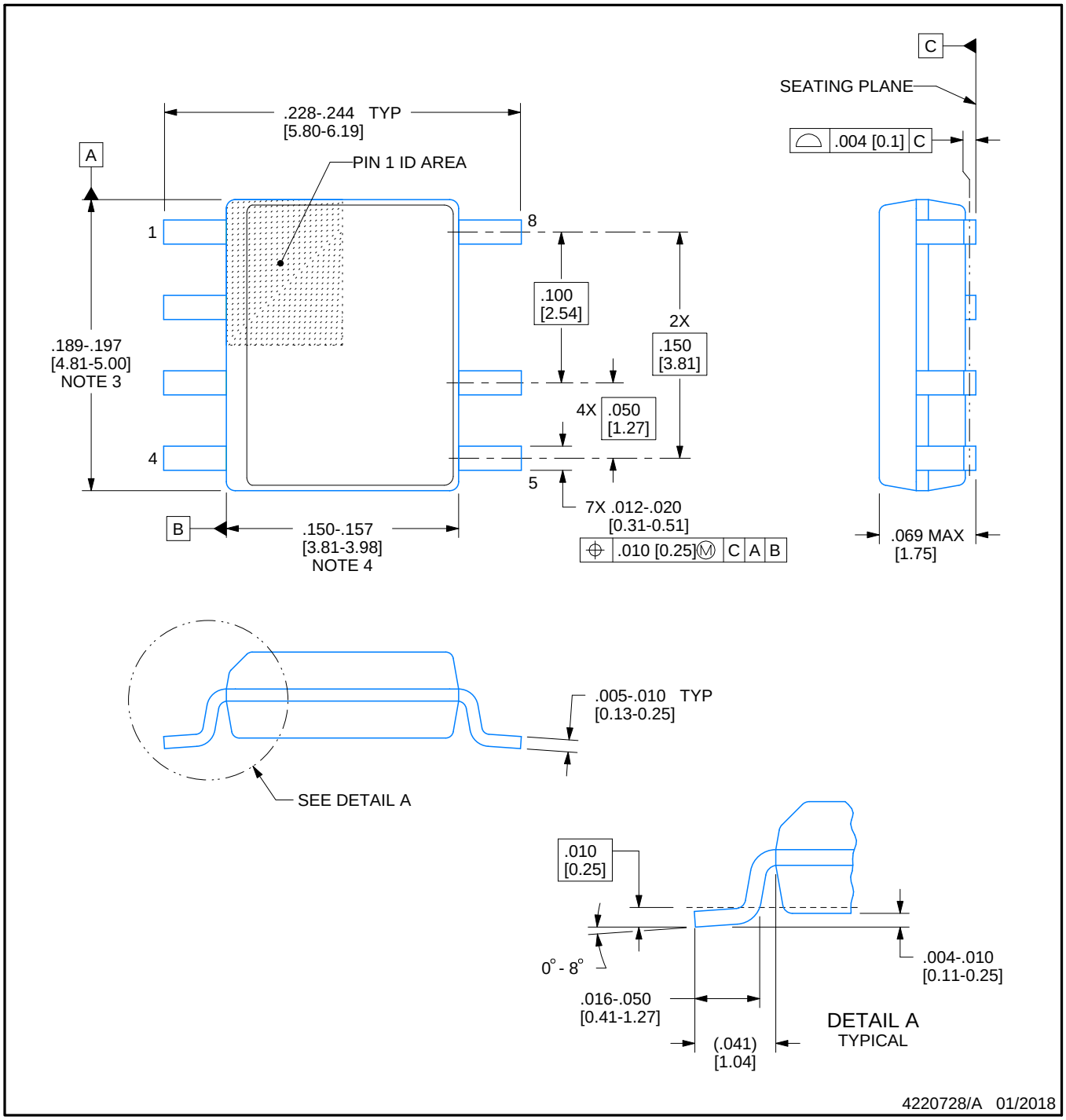


# PACKAGE OUTLINE

## D0007A

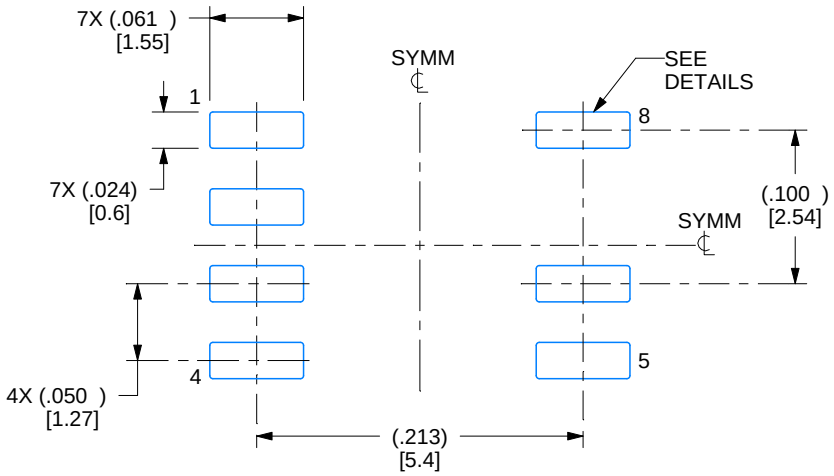
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

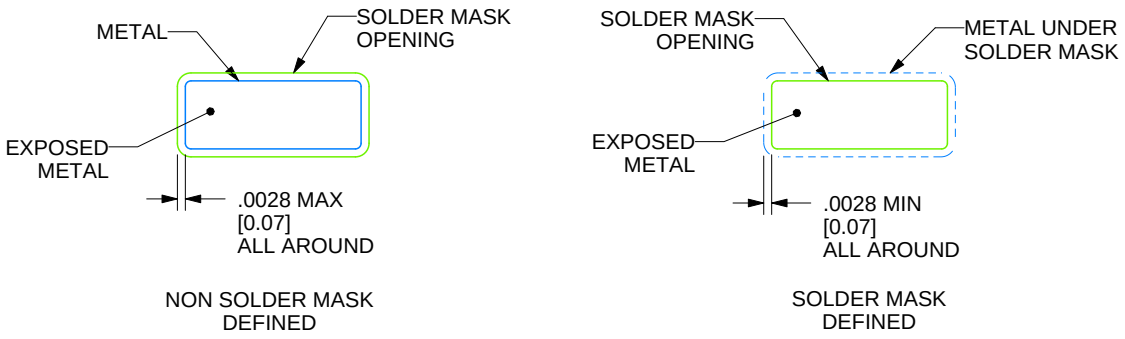



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4220728/A 01/2018

NOTES: (continued)

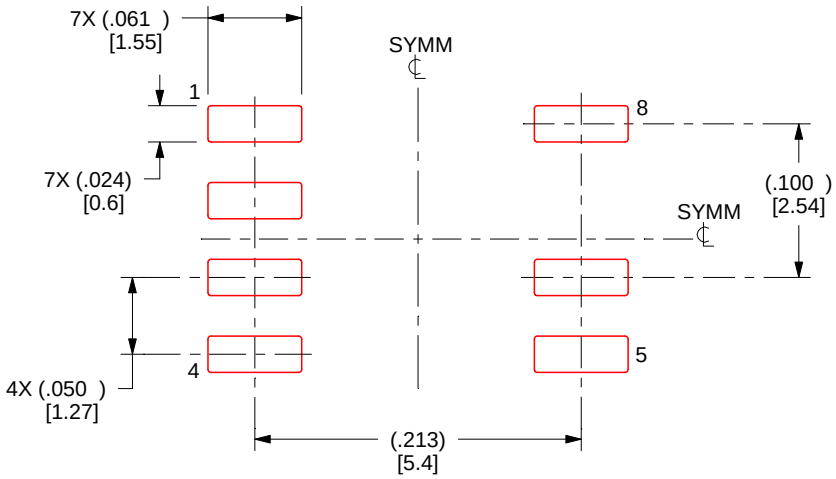
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0007A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4220728/A 01/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月