UCC33421-Q1 超小型、1.5 W、5.0V、5kV$_{RMS}$ 絶縁、車載用 DC/DC モジュール

1 特長

- 1.5 W の最大出力電力
- 4.5V～5.5V の入力電圧動作範囲
- 安定化出力電圧として 5.0V、5.5V を選択可能
  - 5.0V：300mA の負荷電流を供給可能
- 0.5% のロード レギュレーション (標準値)
- 2mV/V のライン レギュレーション (標準値)
- 堅牢な絶縁バリア：
  - 絶縁定格：5kV$_{RMS}$
  - サージ耐性：10.4kV$_{PK}$
  - 動作電圧：1700V$_{PK}$
  - 絶縁バリアの両側で ±8KV の IEC 61000-4-2 接触放電保護
  - 250V/ns の同相過渡耐性
- トランス技術を内蔵した電力密度の高い絶縁型 DC-DC モジュール
- 適応型スペクトラム拡散変調 (SSM)
- CISPR-25 Class 5 の放射規格に適合
- 強磁界耐性
- 過負荷および短絡保護
- サーマル シャットダウン
- 小さい突入電流 (ソフトスタート)
- フォルト通知メカニズムを備えたイネーブル ピン
- 機能安全対応
- 安全関連の認証計画：
  - DIN EN IEC 60747-17 (VDE 0884-17) に準拠した強化絶縁耐圧
  - UL 1577/CSA に準拠した絶縁耐圧：5kV$_{RMS}$ (1 分間)
- 以下の結果で AEC-Q100 認定済み：
  - デバイス温度グレード 1：–40℃～125℃の動作時周囲温度
- SOIC-16 (5.85mm × 7.50mm) パッケージ

2 アプリケーション

- バッテリ管理システム (BMS)
- HEV/EV の OBC (オンボード チャージャ) と DC/DC コンバータ
- トラクション インバータ
- デジタル アイソレータ向けの絶縁バイアス電源
- RS-485、RS-422、CAN 向けの絶縁バイアス電源

3 概要

UCC33421-Q1 は、トランス技術を内蔵し、1.5 W の絶縁出力電力を供給するように設計された、車載認定済み DC/DC パワー モジュール です。4.5V～5.5V の入力電圧動作範囲に対応し、5.0V の安定化出力電圧を供給し、5.5V のヘッドルームを選択可能です。

UCC33421-Q1 は、5kV$_{RMS}$ の絶縁定格を達成する独自のトランス アーキテクチャを採用すると同時に、低 EMI と優れた負荷レギュレーションを備えています。

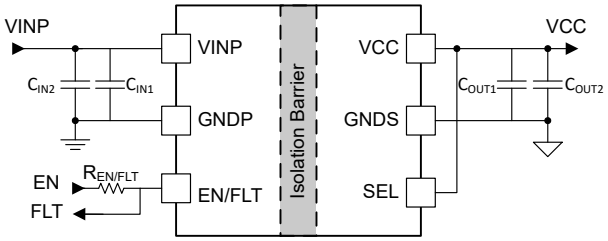
UCC33421-Q1 には、フォルト通知メカニズム付きのイネーブル ピン、短絡保護、サーマル シャットダウンなど、システムの堅牢性を向上させる保護機能が内蔵されています。

UCC33421-Q1 は、高さ 2.65mm、沿面距離および空間距離 8.2mm 超の小型低プロファイル ソリューション SOIC (5.85mm × 7.50mm) パッケージで供給されます。

製品情報 (1)

部品番号	パッケージ	本体サイズ (公称)
UCC33421-Q1	DHA SOIC (16)	5.85mm × 7.50mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



アプリケーション概略図

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4 Device Comparison

表 4-1. Device Comparison Table

DEVICE NAME	V_{VIN} Range	Output (VCC)	Typical power	Isolation rating
UCC33420-Q1	4.5V to 5.5V	5.0V / 5.5V	1.5W	Basic
UCC33420	4.5V to 5.5V	5.0V / 5.5V	1.5W	Basic
UCC33410-Q1	4.5V to 5.5V	3.3V / 3.7V	1.0W	Basic
UCC33410	4.5V to 5.5V	3.3V / 3.7V	1.0W	Basic
UCC33421-Q1	4.5V to 5.5V	5.0V / 5.5V	1.5W	Reinforced

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5 Pin Configuration and Functions

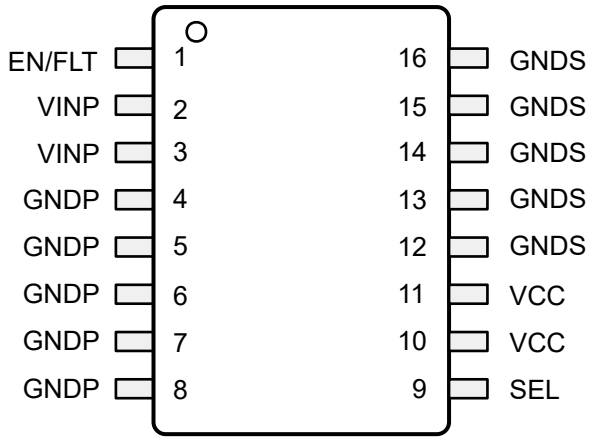

図 5-1. DHA SOIC 16-pin Package (Top View)

表 5-1. Pin Functions

PIN		TYPE (1)	DESCRIPTION
NAME	NO.		
EN/FLT	1	I/O	Multi-function Enable input pin and fault output pin. Connect to microcontroller through an 18kΩ or greater pull-up resistor. Enable input pin: Forcing EN low disables the device. Pull high to enable normal device functionality. Fault output pin: This pin is pulled low for 200µs to alert that power converter is shutdown due to fault condition
VINP	2	P	Primary side input supply voltage pin. 15nF (C_{IN1}) and 10µF (C_{IN2}) ceramic bypass capacitors placed close to device pins are required between VINP and GNDP pins
	3		
GNDP	4	G	Power ground return connection for VINP.
	5		
	6		
	7		
	8		
SEL	9	I	VCC selection pin. VCC setpoint is 5.0V when SEL is connected to VCC, and 5.5V when SEL is shorted to GNDS
VCC	10	P	Isolated supply output voltage pin. 15nF (C_{OUT1}) and 22µF (C_{OUT2}) ceramic bypass capacitors placed close to device pins are required between VCC and GNDS pins
	11		
GNDS	12	G	Power ground return connection for VCC.
	13		
	14		
	15		
	16		

(1) P = Power, G = Ground, I = Input, O = Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PIN	MIN	TYP	MAX	UNIT
VINP to GNDP(3)	–0.3		6	V
EN/FLT to GNDP	–0.3		6	V
VCC to GNDS (3)	–0.3		6	V
SEL to GNDS (3)	–0.3		6	V
Total VCC output power at T_A=25°C, $P_{OUT\_VCC\_MAX}$ (2)			1.65	W
Operating junction temperature range, T_J	–40		150	°C
Storage temperature, T_{stg}	–65		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) See the VCC Load Recommended Operating Area section for maximum rated values across temperature and VINP conditions for different VCC output voltage settings.
(3) Less than 1ms. Extended time at this voltage can affect lifetime reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011 Section 7.2	±750	V
		Contact discharge per IEC 61000-4-2; Isolation barrier withstand test (2)	±8000	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification
(2) IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PIN		MIN	TYP	MAX	UNIT
V_{VINP}	Primary-side input voltage to GNDP	4.5		5.5	V
$V_{EN/FLT}$	EN/FLT pin voltage to GNDP	0		5.5	V
V_{VCC}	Secondary-side Isolated output voltage to GNDS	0		5.7	V
V_{SEL}	SEL pin input voltage to GNDS	0		5.7	V
P_{VCC}	VCC output power at VINP=5.0V±10%, VCC = 5.0V, T_A=25°C - 85°C (1)		1.5		W
P_{VCC}	VCC output power at VINP=5.0V±10%, VCC = 5.0V, T_A=105°C (1)		1		W
P_{VCC}	VCC output power at VINP=5.0V±10%, VCC = 5.0V, T_A=125°C (1)		0.4		W
Static CMTI	Static Common mode transient immunity rating (dV/dt rate across the isolation barrier)			250	V/ns
Dynamic CMTI	Dynamic Common mode transient immunity rating (dV/dt rate across the isolation barrier)			250	V/ns
T_A	Ambient temperature	–40		125	℃
T_J	Junction temperature	–40		150	℃

(1) See the VCC Load Recommended Operating Area section for maximum rated values across temperature and VINP conditions for different VCC output voltage settings.

6.4 Thermal Information

THERMAL METRIC(1)		DHA SOIC 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	61.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	5.88	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.2	°C/W
Ψ_{JA}	Junction-to-ambient characterization parameter	59.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	5.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	23.6	°C/W

(1) The thermal resistances (R) are based on JEDEC board, and the characterization parameters (Ψ) are based on the EVM described in the Layout section. For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
CLR	External clearance (1)	Shortest terminal-to-terminal distance through air	> 8.2	mm
CPG	External creepage (1)	Shortest terminal-to-terminal distance across the package surface	> 8.2	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 70	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category	Rated mains voltage ≤ 300V_{RMS}	I-IV	
		Rated mains voltage ≤ 600V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000V_{RMS}	I-III	
DIN EN IEC60747-17 (VDE 0884-17) (2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1700	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage (sine wave) Time dependent dielectric breakdown (TDDB) test	1202	V_{RMS}
		DC voltage	1700	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM}, t = 60s (qualification)	7071	V_{PK}
		V_{TEST} = 1.2 × V_{IOTM} , t = 1s (100%) production	8485	V_{PK}
V_{IMP}	Impulse Voltage (3)	Tested in air, 1.2/50µs waveform per IEC 62368-1	8000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage (4)	Tested in oil (qualification test), 1.2/50µs waveform per IEC 62368-1.	10400	V_{PK}
q_{pd}	Apparent charge (5)	Method a: After I/O safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60s; $V_{pd(m)}$ = 1.2 × V_{IORM}, t_m = 10s	≤ 5	pC
		Method a: After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60s; $V_{pd(m)}$ = 1.6 × V_{IORM}, t_m = 10s	≤ 5	pC
		Method b1: At routine test (100% production) and preconditioning (type test), V_{ini} = V_{IOTM}, t_{ini} = 1s; $V_{pd(m)}$ = 1.875 × V_{IORM}, t_m = 1s	≤ 5	pC
C_{IO}	Barrier capacitance, input to output (6)	V_{IO} = 0.4 sin (2πft), f = 1MHz	< 3	pF
R_{IO}	Isolation resistance, input to output (6)	V_{IO} = 500V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	Ω
		V_{IO} = 500V at T_S = 150°C	> 10^9	Ω
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	Withstand isolation voltage V_{TEST} = V_{ISO}, t = 60s (qualification) V_{TEST} = 1.2 × V_{ISO}, t=1s (100% production)	5000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed-circuit board are used to help increase these specifications.
(2) This coupler is suitable for *basic electrical insulation* only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier tied together creating a two-terminal device

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6.6 Safety-Related Certifications

VDE	UL	UL
Plan to certify according to DIN EN IEC 60747-17 (VDE 0884-17)	Plan to certify under UL 1577 / CSA Component Recognition program	Plan to certify according to IEC 60601-1
Reinforced insulation Maximum transient isolation voltage, 7071V_{PK}; Maximum repetitive peak isolation voltage, 1700V_{PK}; Maximum surge isolation voltage, 10400V_{PK}	Single protection, 5000V_{RMS}	Reinforced insulation per UL 60601- 1:14 and IEC 60601-1 d.3+A1,AAMI ES 60601- 1:2005/(R)2012 and A1:2012, C1:2009/(R)2012 and A2:2010/(R)2012 CSA C22.2 No. 60601-1:2014 IEC 60601-1:2012, 250V_{RMS} maximum working voltage, 2 MOPP (Means of patient protection)
Certificate number: (planned)	Certificate number: (planned)	Certificate number: (planned)

6.7 Electrical Characteristics

Over operating temperature range (T_J = –40°C to 150°C), VINP = 5.0V, C_{IN1} = C_{OUT1} = 15nF, C_{IN2} = 10µF, C_{OUT2} = 22µF SEL connected to VCC, EN/FLT = 5.0V unless otherwise noted. All typical values at VINP=5.0V, T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY (Primary-side. All voltages with respect to GNDP)						
I_{VINP_Q}	VINP quiescent current,disabled	EN/FLT=Low, VINP=5.0V, no load			180	uA
I_{VINP_NL}	VINP operating current, no load	EN/FLT=High; VINP=4.5V-5.5V; VCC=5.0V no load		7	15	mA
		EN/FLT=High; VINP=4.5V-5.5V; VCC=5.5V no load		7	15	mA
I_{VINP_FL}	VINP operating current, full load	EN/FLT=High; VINP=5.0V; VCC=5.0V, I_{out}=300mA, T_A=25°C	489	508	529	mA
UVLOP COMPARATOR (Primary-side. All voltages with respect to GNDP)						
$V_{VINP\_UVLO\_R}$	VINP under-voltage lockout rising threshold			2.8	2.9	V
$V_{VINP\_UVLO\_F}$	VINP under-voltage lockout falling threshold		2.6	2.7		V
V_{UVLO_H}	VINP under-voltage lockout hysteresis			0.1		V
OVLO COMPARATOR (Primary-side. All voltages with respect to GNDP)						
$V_{VINP\_OVLO\_R}$	VINP over-voltage lockout rising threshold			5.77	5.9	V
$V_{VINP\_OVLO\_F}$	VINP over-voltage lockout falling threshold		5.55	5.72		V
V_{VINP_H}	VINP over-voltage lockout hysteresis			0.05		V
Switching Charactarestics						
f_{Sw}	DC-DC Converter switching frequency			64.5	67.3	MHz
PRIMARY SIDE THERMAL SHUTDOWN						
TSD_{P_R}	Primary-side over-temperature shutdown rising threshold		150	165		ºC
TSD_{P_F}	Primary-side over-temperature shutdown falling threshold		130			ºC
TSD_{P_H}	Primary-side over-temperature shutdown hysteresis			20		ºC
EN/FLT PIN						
V_{EN_R}	Enable voltage rising threshold	EN/FLT = 0V to 5.0V			2.1	V
V_{EN_F}	Enable voltage falling threshold	EN/FLT = 5.0V to 0V	0.8			V
I_{EN}	Enable Pin Input Current	EN/FLT = 5.0V			10	uA
V_{FLT}	EN/FLT pin voltage when faults occur	With a minimum 18kohm (10% tolerance) resistor connected to EN/FLT pin			0.5	V
t_{Fault}	EN/FLT pull down interval when faults occur	EN/FLT > 0.5V , Fault occur		200		us

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Over operating temperature range (T_J = –40°C to 150°C), VINP = 5.0V, C_{IN1} = C_{OUT1} = 15nF, C_{IN2} = 10µF, C_{OUT2} = 22µF SEL connected to VCC, EN/FLT = 5.0V unless otherwise noted. All typical values at VINP=5.0V, T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCC OUTPUT VOLTAGE (Secondary-side. All voltages with respect to GNDS)						
V_{CC}	Isolated supply regulated output voltage	VINP = 5.0V; VCC = 5.0V, I_{out} = 0 - 300mA	4.85	5	5.15	V
		VINP = 5.0V; VCC = 5.5V, I_{out} = 0 - 200mA	5.34	5.5	5.67	V
	Isolated supply regulated output voltage accuracy	VINP = 4.5V - 5.5V; VCC = 5.0V / 5.5V	-4		4	%
V_{CC_Line}	V_{cc} DC line regulation	VINP = 4.5V - 5.5V; VCC =5.0V, I_{out} = 150mA		2		mV/V
		VINP = 4.5V - 5.5V; VCC = 5.5V, I_{out} = 150mA		2		mV/V
V_{CC_Load}	V_{cc} DC load regulation	VINP = 5.0V; VCC = 5.0V, I_{out} = 0-300mA		0.5		%
		VINP = 5.0V; VCC = 5.5V, I_{out} = 0-200mA		0.5		%
V_{CC_Ripple}	Voltage ripple on isolated supply output	20-MHz bandwidth, VINP = 5.0V , VCC = 5.0V, I_{out} = 300mA, T_A=25°C		50	75	mV
EFF	Efficiency P_{VCC} to P_{VINP}	VINP = 5.0V, VCC = 5.0V, I_{out} = 300mA, T_A = 25°C		59		%
V_{CC_Rise}	VCC rise time from 10% - 90%	VINP = 4.5V - 5.5V, VCC = 5.0V, I_{out} = 70mA			500	us
		VINP = 4.5V - 5.5V, VCC = 5.5V, I_{out} = 70mA			500	us
VCC UVP UNDER -VOLTAGE PROTECTION (Secondary-side. All voltages with respect to GNDS)						
K_{VCC_UVP}	VCC under-voltage protection threshold ratio	V_{UVP} = VCC * 90%		90		%
V_{UVP_H}	VCC under-voltage protection hysteresis	VCC = 5.0V	79	100	121	mV
V_{UVP_H}	VCC under-voltage protection hysteresis	VCC = 5.5V	87	110	133	mV
VCC OVP OVER -VOLTAGE PROTECTION (Secondary-side. All voltages with respect to GNDS)						
$V_{VCC\_OVP\_R}$	VCC over-voltage protection rising threshold	VCC = 5.0V		5.45	5.5	V
$V_{VCC\_OVP\_H}$	VCC over-voltage protection hysterisis	VCC = 5.0V		0.1		V
$V_{VCC\_OVP\_R}$	VCC over-voltage protection rising threshold	VCC = 5.5V		5.9	5.95	V
$V_{VCC\_OVP\_H}$	VCC over-voltage protection hysterisis	VCC = 5.5V		0.12		V
SECONDARY SIDE THERMAL SHUTDOWN						
TSD_{S_R}	Secondary-side over-temperature shutdown rising threshold		150	165		ºC
TSD_{S_F}	Secondary-side over-temperature shutdown falling threshold		130			ºC
TSD_{S_H}	Secondary-side over-temperature shutdown hysteresis			20		ºC

6.8 External BOM Components

Over recommended conditions

COMPONENT		NOTES	MIN	TYP	MAX	UNIT
C_{IN1}	VINP first decoupling capacitor			15		nF
C_{IN2}	VINP second decouling capacitor		10	22		µF
C_{OUT1}	VCC first decoupling capacitor			15		nF
C_{OUT2}	VCC second decoupling capacitor		10	22		µF

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7 Detailed Description

7.1 Overview

The UCC33421-Q1 device integrates a high-efficiency, low-emissions isolated DC/DC converter. Requiring minimum passive componenets to form a completely functional DC/DC power module, the device can deliver a maxiumum power of 1.5 W across a 5kV$_{RMS}$ 強化 isolation barrier over a wide range of operating temperatures in a low profile , high power density SOIC - 16-pin package.

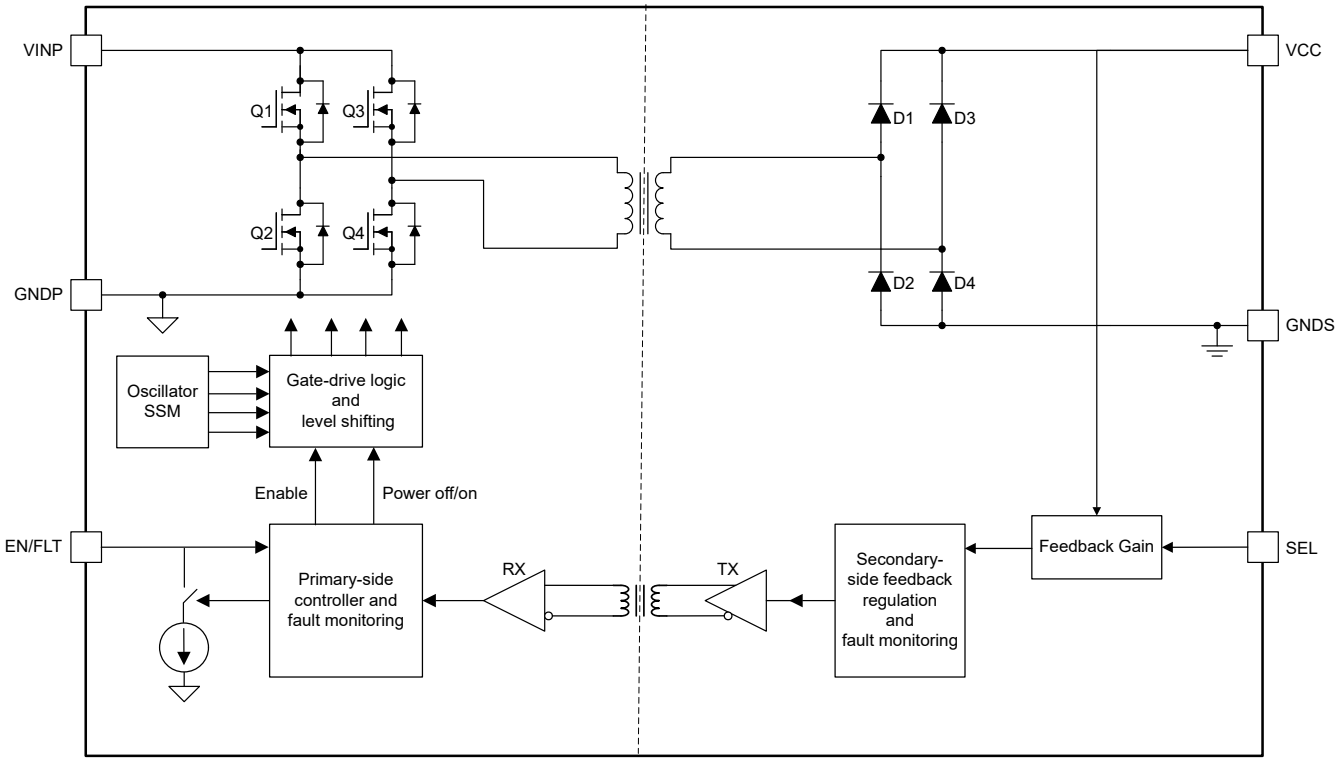
The easy-to-use feature, low profile and high power density promotes this device for size limited, cost sensitive systems with a minimum design effort replacing bulky and expensive transformer based designs.

The integrated DC/DC converter uses switched mode operation and proprietary circuit techniques to reduce power losses and boost efficiency across all loading conditions. Specialized control mechanisms, clocking schemes, and the use of an on-chip transformer provide high efficiency and low radiated emissions.

The VINP supply is provided to the primary power controller that switches the power stage connected to the integrated transformer. Power is transferred to the secondary side, rectified, and regulated using a fast hysteritic burst mode control scheme that monitors VCC and ensures it is kept within the hysterisis band under normal and transient loading events while maintaining efficient operation across all loading conditions. The VCC is regulated to 5.0V or 5.5V by SEL pin connection to have enough headrome for a post regulator LDO for tighter regulation or lower output ripple requirement applications .

The device has an enable pin to turn the device on or off depending on the system requirement. Pulling enable pin low will reduce the quiscent current significantly if the system wants to operate in a low power conumption mode. The enable pin can also be used as a fault reporting pin, when connected to 18kΩ, the pin will be pulled low for 200µs for any fault shutdown of the device. The device has a soft-start mechanism for a smooth and fast VCC ramp up with minimum input inrush current to avoid oversizing front-end power supplies powering the device's input.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable and Disable

Forcing EN/FLT pin low disables the device, which greatly reduces the VINP power consumption. Pull the EN/FLT pin high to enable normal device functionality. The EN/FLT pin has a weak internal pull-down resistor so it is not recommended to leave this pin floating in noisy systems.

7.3.2 Output Voltage Soft-Start

The UCC33421-Q1 has soft-start mechanism that ensures a smooth and fast soft-start operation with minimum input inrush current. The output voltage Soft-Start diagram is shown in 図 7-1. After VINP > $V_{VINP\_UVLO\_R}$ and EN/FLT is pulled high, the soft-start sequence starts with a primary duty cycle open loop control. The power stage operates with a fixed burst frequency with an incremental increasing duty cycle starting at 6.5% . The rate of change of the duty cycle is pre-programmed in the part to reduce the input inrush current while building the output voltage VCC. The primary side limits the maximum duty cycle to 62.5% during this phase till the secondary side VCC voltage passes V_{VCC_UVLO} = 2.7V threshold before releasing this duty cycle limit. This limit will ensure minimum input current in case the device starts on a short circuit and the VCC is not building up.

The soft-start time will vary depending on the output capacitors, input voltage and loading conditions. The UCC33421-Q1 has a soft-start timeout feature by which the VCC output voltage state is monitored during soft-start. In certain conditions the VCC might not reach steady-state regulation threshold due to short circuit on the output voltage as shown in 図 7-2 , heavy loading conditions above recommended operating conditions or higher output capacitor values as shown in 図 7-3. In these conditions, if the soft-start timout duration of 16ms expires without the VCC reaching steady-state regulation, the part will shutdown and EN/FLT pin will be pulled low for 200us to report the fault condition. An auto-restart timer will start afterwards, the part will attempt to restart after that timer expires. More details regarding fault reporting and auto-restart can be found in Fault Reporting and Auto-Restart. If the same conditions continue to exist the same cycle will repeat again as shown in 図 7-2and 図 7-3 below.

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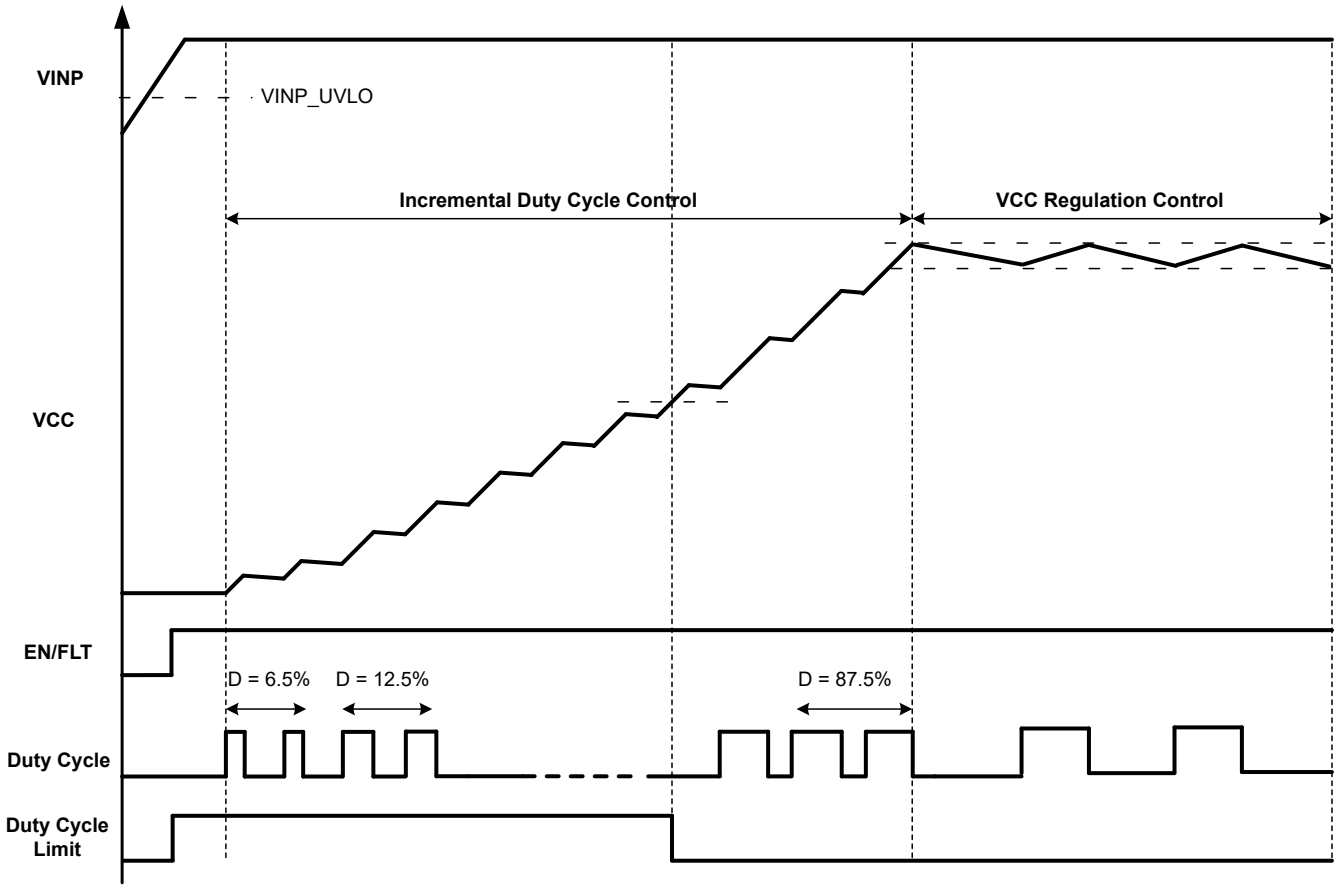

図 7-1. Output Voltage Soft-Start Diagram

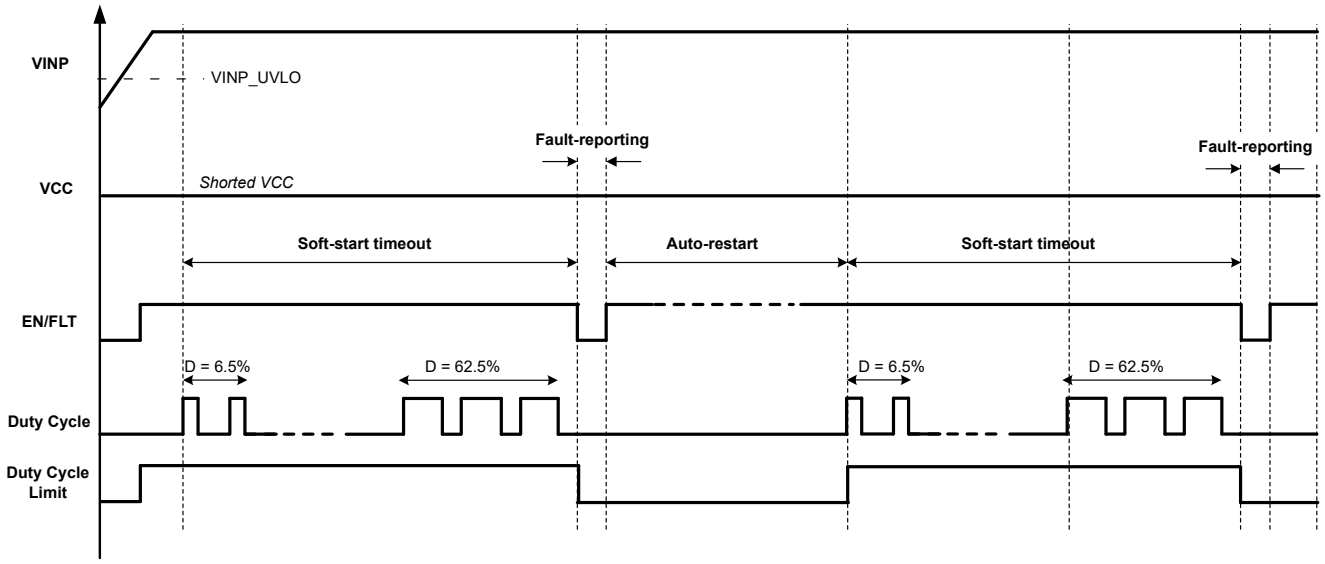

図 7-2. Soft-start under short-circuit output

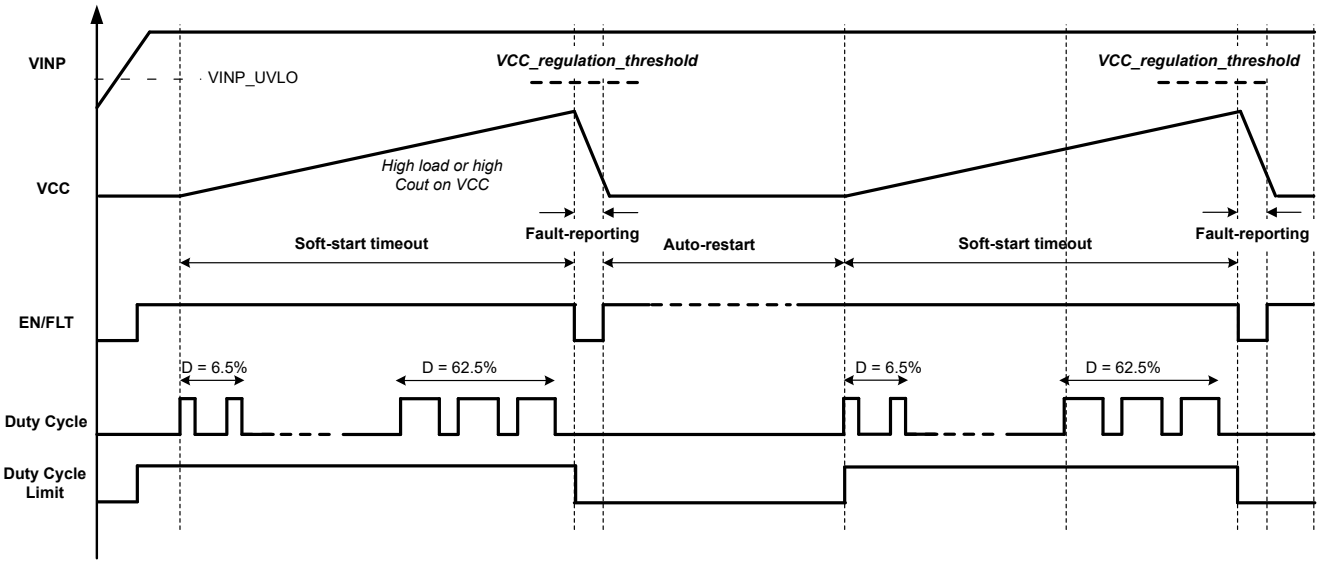

図 7-3. Soft-start underhigh load or high output capacitor conditions

7.3.3 Output Voltage Steady-State Regulation

The UCC33421-Q1 uses hysteritic control to regulate the output voltage between upper and lower bands as shown in 図 7-4. The regulation block on the secondary side senses the regulated output voltage and sends a feedback signal to the primary side through the inductive communication channel to turn the primary power stage On or Off to maintain the regulated output whithin the hysterisis bands. During steady-state regulation, the burst frequency will change according to the output capacitors and loading conditions. The burst frequency will be highest at higher loading conditions and lowest at light loading conditions by which light load efficiency improvments can be achieved. The Burst-On duration (t_{ON}) will increase with heavy loading conditions recommended operating conditions or higher output capacitor values . The UCC33421-Q1 has an overpower protection feature that will limit the maximum t_{ON} value to typical of 13us.

The UCC33421-Q1 can program the VCC_REG voltage accoring to the SEL pin connection. The SEL pin voltage is monitored during soft-start sequence when VCC < V_{VCC_UVLO} threshold . The output voltage is then programmed to 5.0V with SEL = VCC or 5.5V with SEL = GNDS. Note that after this initial monitoring, the SEL pin no longer affects the VCC output level. In order to change the output mode selection, either the EN/FLT pin must be toggled or the VINP power supply must be cycled off and back on.

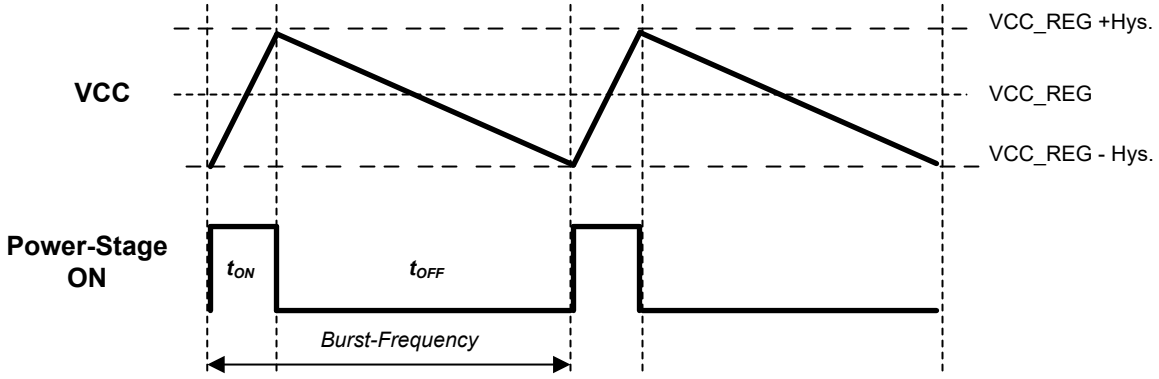

図 7-4. Output voltage hysterisis mode control

7.3.4 Protection Features

The UCC33421-Q1 is equipped with full feature of protection functions including input under-voltage lockout, input over-voltage lockout, output under-voltage protection and over-temperature protection. In addition, the

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device has a fault reporting mechanism that can be utilized on the system level to report faulty conditions of the device that caused a shutdown. Under certain faulty conditions the device will shutdown and attempt an auto-restart after defined duration.

7.3.4.1 Input Under-voltage and Over-Voltage Lockout

The UCC33421-Q1 can operate at input voltage range from 4.5V to 5.5V. If the VINP < $V_{VINP\_UVLO\_F}$ or VINP > $V_{VINP\_OVLO\_R}$ conditions occured, the converter will stop switching and part will shutdown. Once the VINP gets back in normal operation range , VINP > $V_{VINP\_UVLO\_R}$ or VINP < $V_{VINP\_OVLO\_F}$. The part will resume switching immediately without waiting for the auto-restart timer.

7.3.4.2 Output Under-Voltage Protection

The UCC33421-Q1 has under voltage protection feature to protect the part when overload condition occurs. If an overload or a short circuit occurs at VCC such that VCC < 0.9 ×VCC condition occurs, the converter will go into the duty cycle limit mode as in the soft-start operation then will shutdown after a certain deglitch time. The deglitch time is added to accommodate for any instantaneous overloading or short circuit conditions that might be removed quickly and normal operation can resume. Once the part shuts down, the part will attempt an auto-restart after 160ms. If the fault condition remains, the part will shutdown again and attempt another auto-restart.

7.3.4.3 Output Over-Voltage Protection

The UCC33421-Q1 has over voltage protection feature to protect the load against over-voltage conditions . If an over-voltage , the converter will go into the duty cycle limit mode as in the soft-start operation then will shutdown after a certain deglitch time. Once the part shuts down, the part will attempt an auto-restart after 160ms. If the fault condition remains, the part will shutdown again and attempt another auto-restart.

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7.3.4.4 Over-Temperature Protection

The UCC33421-Q1 integrates the primary-side, secondary-side power stages, as well as the isolation transformer. The power loss caused by the power conversion causes the module temperature higher than the ambient temperature. To ensure the safe operation of the power module, the device is equipped with over-temperature protection. Both the primary-side power stage, and the secondary-side power stage temperatures are sensed and compared with the over-temperature protection threshold. If the primary-side power stage temperature becomes higher TSD_{P_R}, or the secondary-side power stage temperature becomes higher than TSD_{S_R} , the module enters over-temperature protection mode. The module stops switching after a defined deglitch time, report the fault and attempt an auto-restart after 160ms.

7.3.4.5 Fault Reporting and Auto-Restart

The UCC33421-Q1 has a fault reporting mechanism that can alert a system level MCU or monitoring circuitry of faulty onditions on the device that resulted in a shutdown. If an input over-voltage , over-temperature or output under voltage protection faults occur. The primary-side controller and fault monitoring system will enable a current source that will sink I_{Fault} current for t_{Fault} duration. If a resistor >18kΩ is connected between the MCU and the EN/FLT pin, the V_{FLT} will be pulled low for the same t_{Fault} duration whenever one of the abovementioned faults occur that resulted in a shutdown of the device as shown in 図 7-5. If the fault reporting mechanism is not required on the system, the EN/FLT pin can be connected directly to the enable source voltage without the 18kΩ resistor.

The device has a auto-restart feature that occur after the device is shutdown only due to when output under-voltage or over-temperature faults occur. After the t_{Fault} time expires, a 160ms timer will start and the part will attemp a new soft-start sequence as shown in 図 7-6. If the fault has been removed, the VCC will soft-start to regulation successfully. If the fault remains , the part will shutdown again and report the fault. The device can continuously operate safely in hiccup mode as long as the fault occurs.

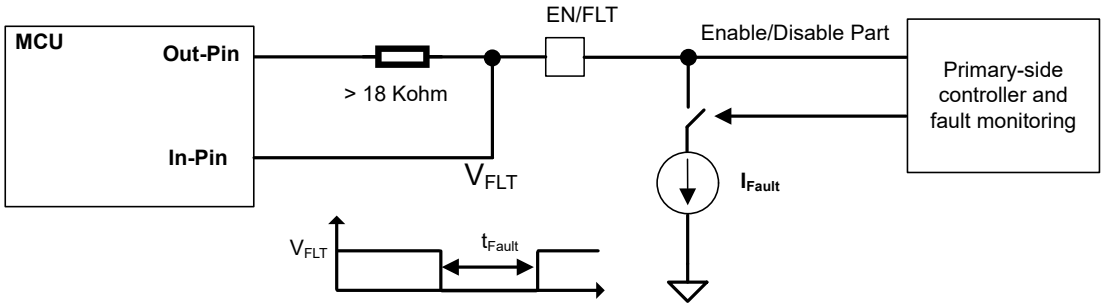

図 7-5. Fault Reporting Mechanism

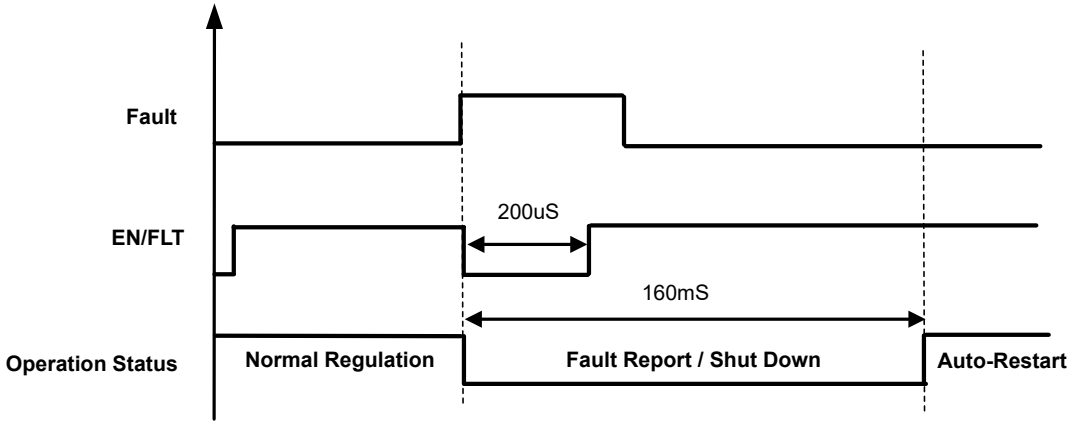

図 7-6. Auto-restart operation

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7.3.5 VCC Load Recommended Operating Area

図 7-7 depicts the device VCC regulation behavior across the output load range, including when the output is overloaded. For proper device operation, ensure that the device VCC output load does not exceed the maximum output current I_{OUT_MAX}. If the UCC33421-Q1 is loaded beyond the recommended operating area, the VCC will drop and once it goes below the VCC_UVP threshold, the part enters a power limiting mode to avoid stressing the device till power stage stop switching and shutdown.

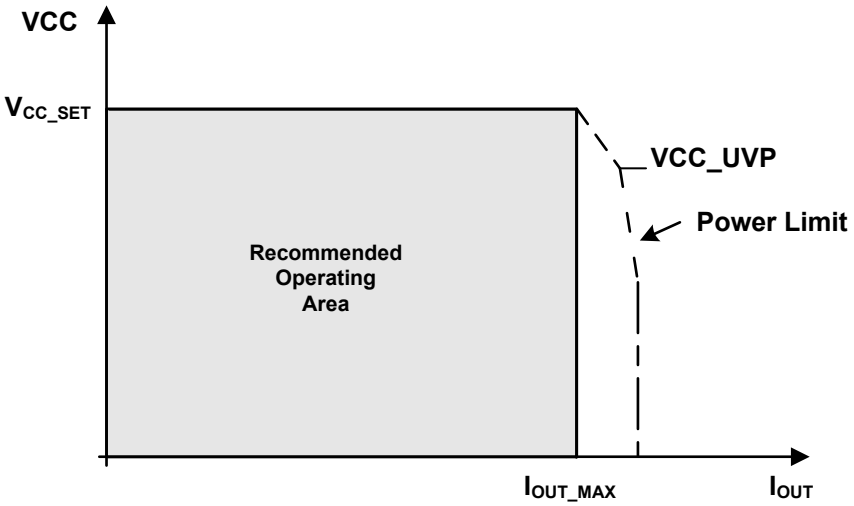

図 7-7. VCC Load Recommended Operating Area Description

7.3.6 Electromagnetic Compatibility (EMC) Considerations

UCC33421-Q1 devices use adaptive spread spectrum modulation (SSM) algorithm for the internal oscillator to reduce the noise emmissions from the device. The adaptive SSM algorithm ensures a full switching frequency scan between two bands during each burst cycle regardless of the loading consitions to ensure similair impact of SSM at different loading conditions. In addition, the UCC33421-Q1 uses advanced internal layout scheme to minimize radiated emissions at the system level.

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x , CISPR-32 and CISPR-25. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the device incorporates many chip-level design improvements for overall system robustness.

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7.4 Device Functional Modes

表 7-1 lists the supply functional modes for this device.

表 7-1. Device Functional Modes

INPUTS		Isolated Supply Output Voltage (VCC) Setpoint
EN/FLT	SEL	
HIGH	Shorted to VCC	5.0V
HIGH	Shorted to GNDS	5.5V
Low	x	0V
OPEN(1)	OPEN(1)	UNSUPPORTED

(1) The SEL and EN/FLT pins has an internal weak pull-down resistance to ground, but leaving this pin open is not recommended.

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8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The UCC33421-Q1 device is suitable for applications that have limited board space and desire more integration. This device is also suitable for very high voltage applications, where power transformers meeting the required isolation specifications are bulky and expensive.

8.2 Typical Application

Typical Application shows the schematic for the UCC33421-Q1 device supplying an isolated load.

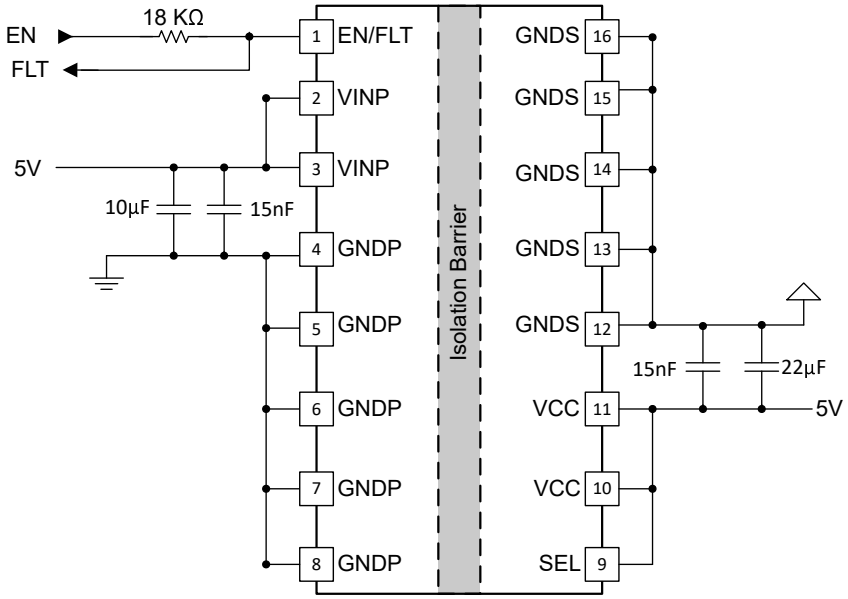

図 8-1. Typical Application

8.2.1 Design Requirements

To design using UCC33421-Q1, a few simple design considerations must be evaluated. 表 8-1 shows some recommended values for a typical application. See セクション 8.3 and セクション 8.4 sections to review other key design considerations for the UCC33421-Q1.

表 8-1. Design Parameters

PARAMETER	RECOMMENDED VALUE
Input supply voltage, VINP	4.5V to 5.5V
First Decoupling capacitance between VINP and GNDP	15nF, 50V, ± 10%, X7R
Second Decoupling capacitance between VINP and GNDP	10µF, 10V, X7R
First Decoupling capacitance between VCC and GNDS	15nF, 50V, ± 10%, X7R
Second Decoupling capacitance between VCC and GNDS	22µF, 10V, X7R
EN/FLT pin resistor for fault reporting	18kΩ

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8.2.2 Detailed Design Procedure

The UCC33421-Q1 design procedure is very simple, the device requires two decoupling capacitors connected between VINP and GNDP pins for the input supply, and two decoupling capacitors for the isolated output supply placed between VCC and GNDS pins to form a completely functinoal DC/DC converter.

A low ESR, ESL ceramic capacitors are recommended to be connected close to the device pins. It should be noted that the effective burst frequency would be impacted by the selected VCC output capacitor

8.3 Power Supply Recommendations

The recommended input supply voltage (VINP) for the UCC33421-Q1 is between 4.5V and 5.5V. To help ensure reliable operation, adequate decoupling capacitors must be located as close to supply pins as possible. Place local bypass capacitors between the VINP and GNDP pins at the input, and between VCC and GNDS at the isolated output supply. The input supply must have an appropriate current rating to support output load required by the end application.

8.4 Layout

8.4.1 Layout Guidelines

The UCC33421-Q1 integrated isolated power solution simplifies system design and reduces board area usage. Proper PCB layout is important in order to achieve optimum performance. Here is a list of recommendations:

- Place decoupling capacitors as close as possible to the device pins. For the input supply, place 0402 and 0805 ceramic capacitor between pins 2 and 3 (VINP) and pins 4, 5, 6, 7 and 8 (GNDP). For the isolated output supply, place 0402 and 0805 ceramaic capacitora between pins 10 and 11 (VCC) and pins 12, 13, 14, 15 and 16 (GNDS). This location is of particular importance to the input decoupling capacitor, because this capacitor supplies the transient current associated with the fast switching waveforms of the power drive circuits.
- Because the device does not have a thermal pad for heat-sinking, the device dissipates heat through the respective GND pins. Ensure that enough copper (preferably a connection to the ground plane) is present on all GNDP and GNDS pins for best heat-sinking. Placing vias close to the device pins and away from the high frequency path between the ceramic capacitors and the device pins is essential for better thermal performance.
- If space and layer count allow, it is also recommended to connect the VINP, GNDP, VCC and GNDS pins to internal ground or power planes through multiple vias of adequate size. Alternatively, make traces for these nets as wide as possible to minimize losses.
- Pay close attention to the spacing between primary ground plane (GNDP) and secondary ground plane (GNDS) on the PCB outer layers. The effective creepage and or clearance of the system reduces if the two ground planes have a lower spacing than that of the device package.
- To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the UCC33421-Q1 device on the outer copper layers.

ADVANCE INFORMATION

8.4.2 Layout Example

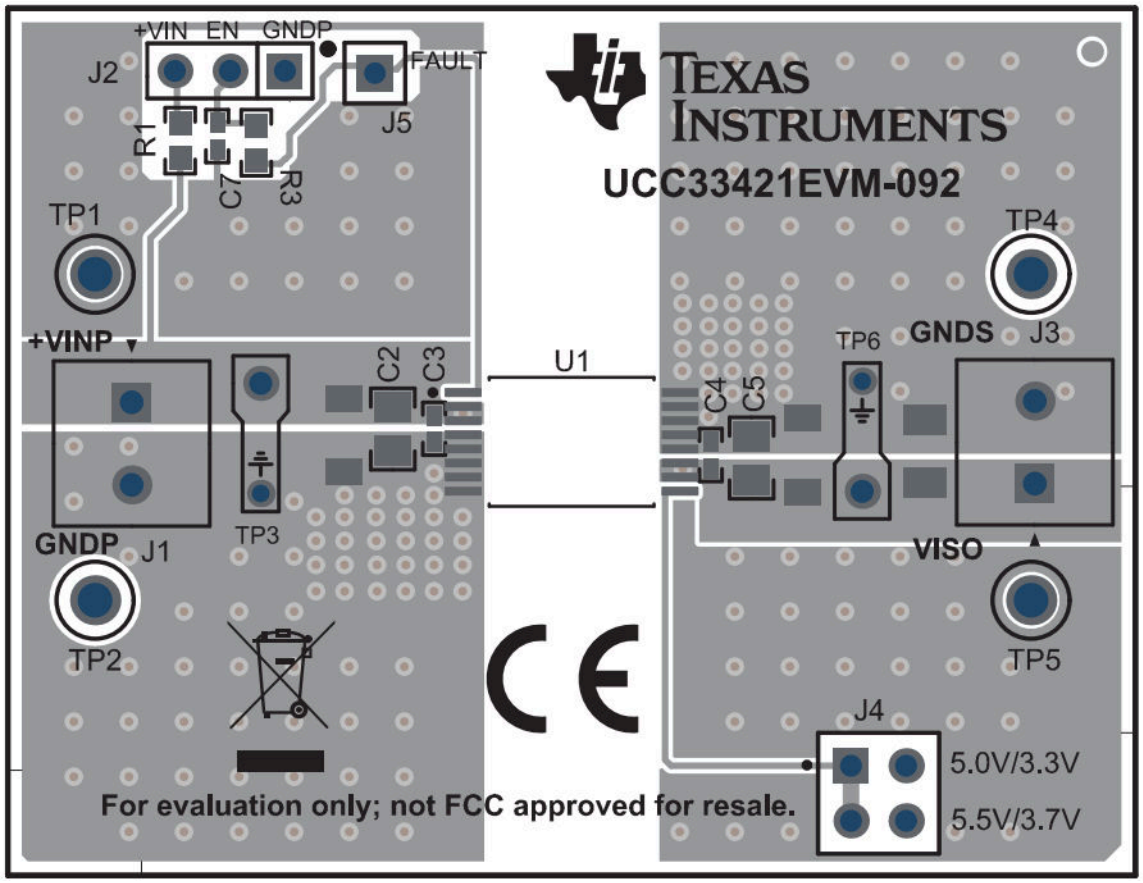

図 8-2. Layout Example

ADVANCE INFORMATION

9 Device and Documentation Support

9.1 Device Support

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Isolation Glossary

9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.4 サポート・リソース

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9.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

DATE	REVISION	NOTES
November 2024	*	Advance Information Release

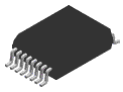
ADVANCE INFORMATION

11 Mechanical and Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

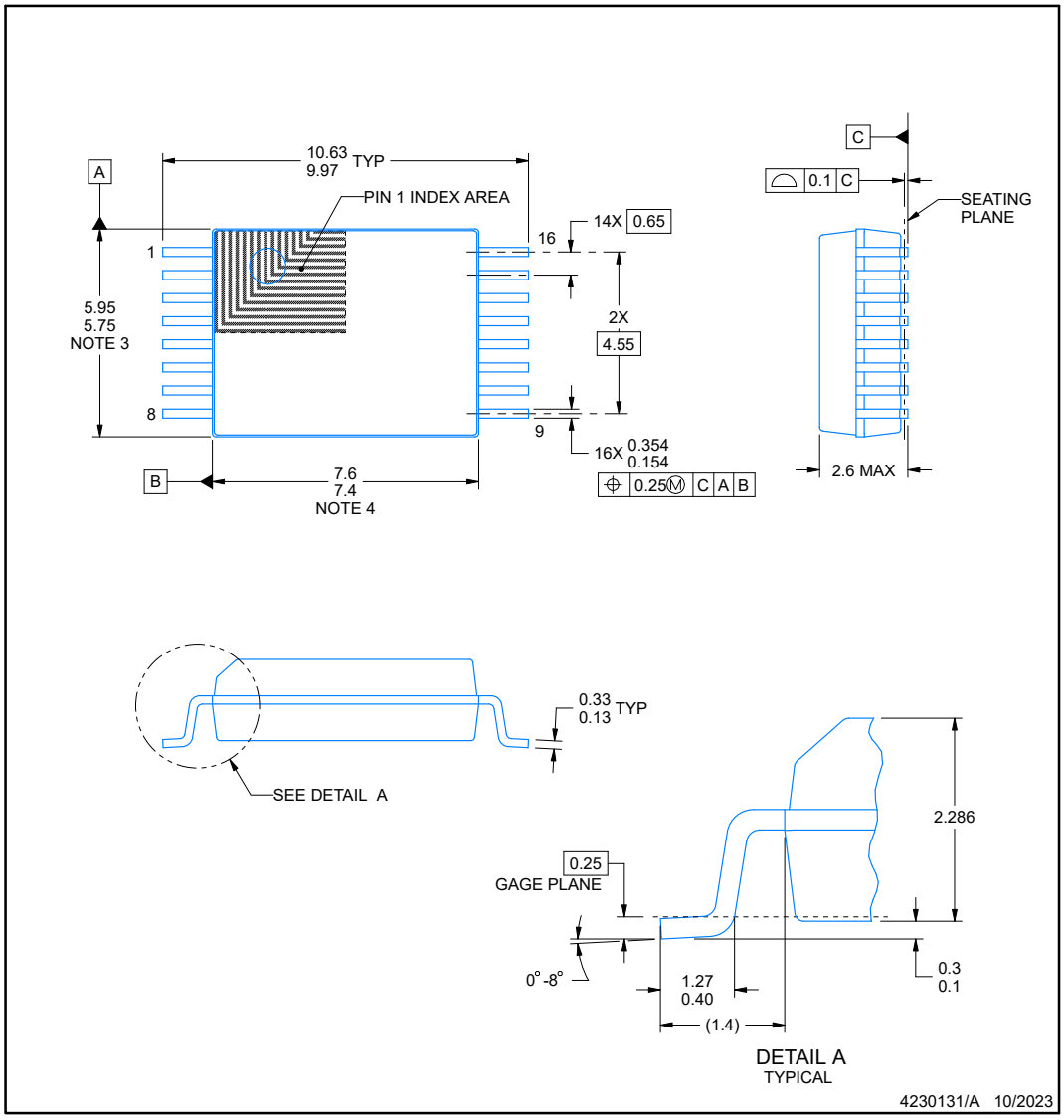
PACKAGE OUTLINE

DHA0016A



SSOP - 2.6 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

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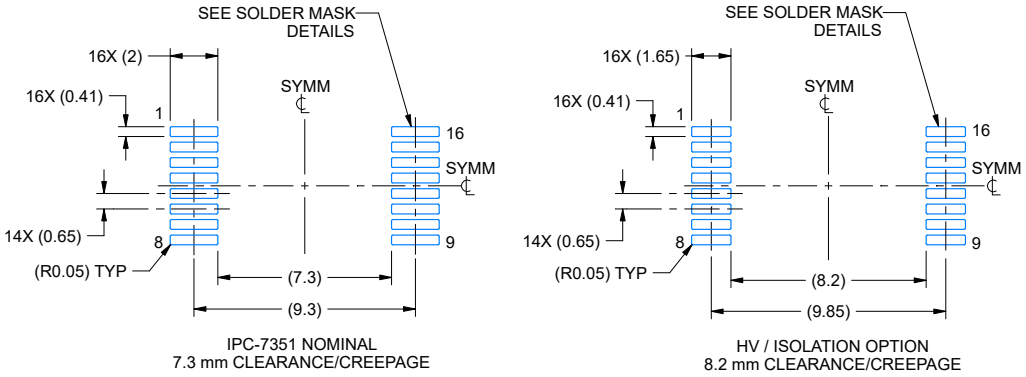
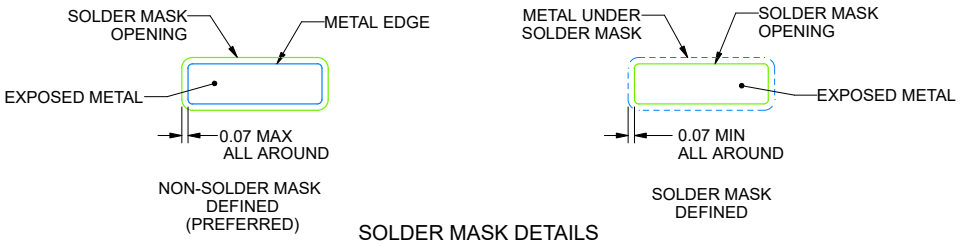
EXAMPLE BOARD LAYOUT

DHA0016A — **SSOP - 2.6 mm max height**

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLES
EXPOSED METAL SHOWN
SCALE: 4X



SOLDER MASK DETAILS

4230131/A 10/2023

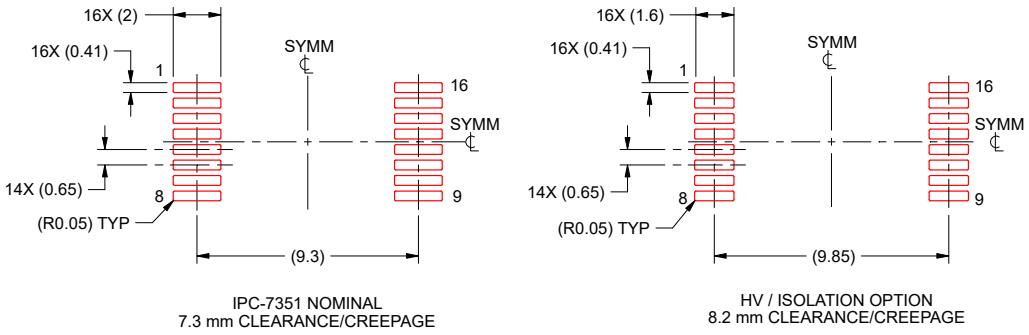
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DHA0016A — **SSOP - 2.6 mm max height**

SMALL OUTLINE PACKAGE



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.2 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLES
BASED ON 0.125 mm THICK STENCIL
SCALE: 4X

4230131/A 10/2023

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PUCC33421QDHARQ1	Active	Preproduction	SO-MOD (DHA) | 16	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PUCC33421QDHARQ1.A	Active	Preproduction	SO-MOD (DHA) | 16	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PUCC33421QDHARQ1.B	Active	Preproduction	SO-MOD (DHA) | 16	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
UCC33421QDHARQ1	Active	Production	SO-MOD (DHA) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	UC33421Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF UCC33421-Q1 :

- Catalog : UCC33421

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

GENERIC PACKAGE VIEW

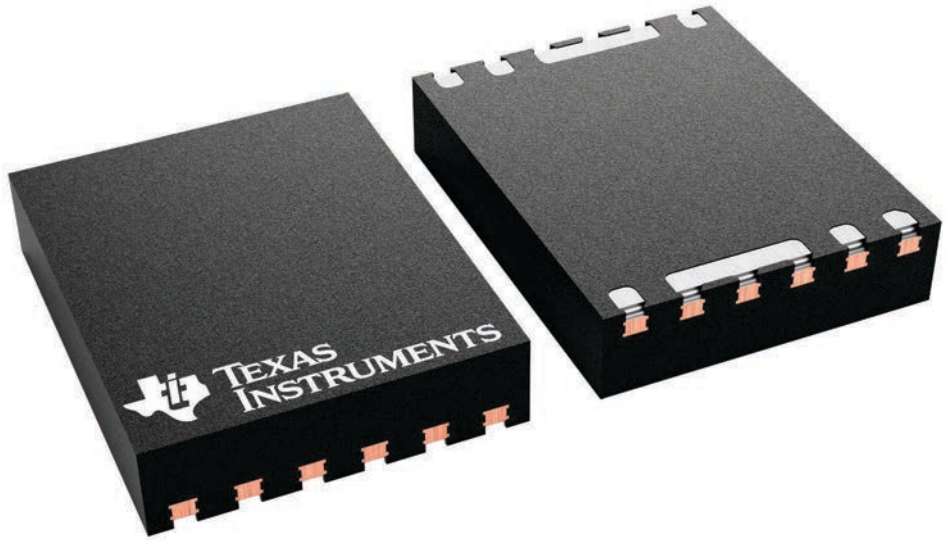
RAQ 12

VSON-FCRLF - 1.05 mm max height

5 x 4, 0.65 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



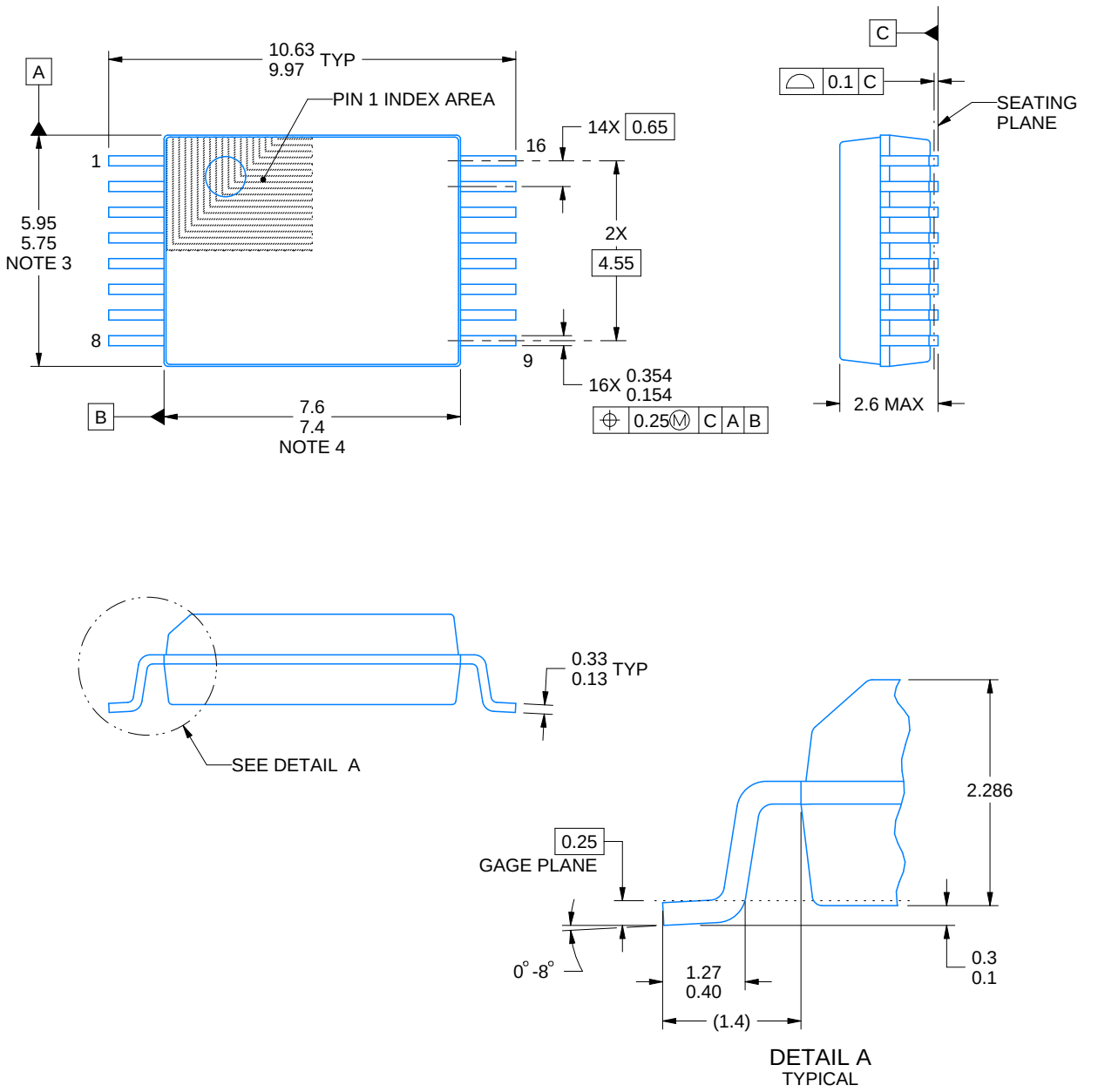
4229417/A

PACKAGE OUTLINE

DHA0016A

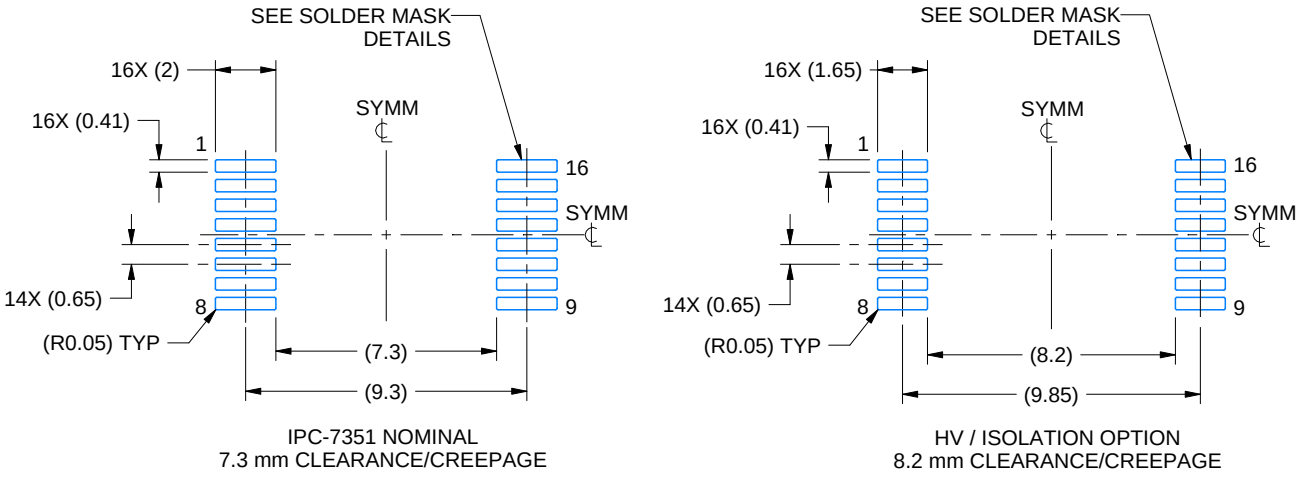
SSOP - 2.6 mm max height

SMALL OUTLINE PACKAGE

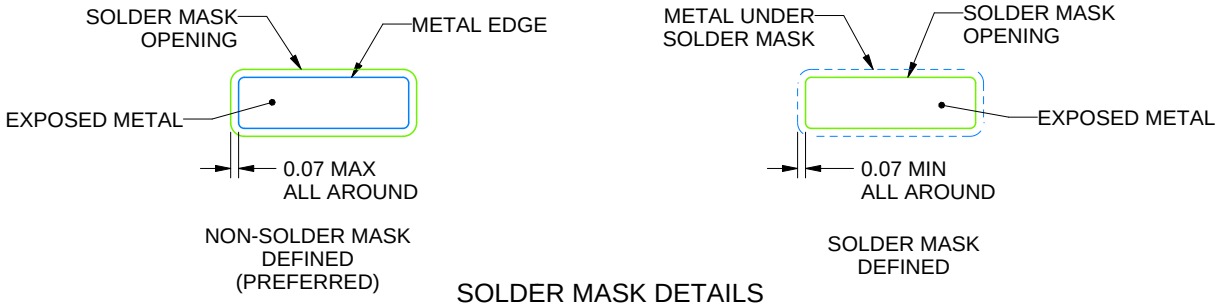


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLES
EXPOSED METAL SHOWN
SCALE: 4X



SOLDER MASK DETAILS

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NOTES: (continued)

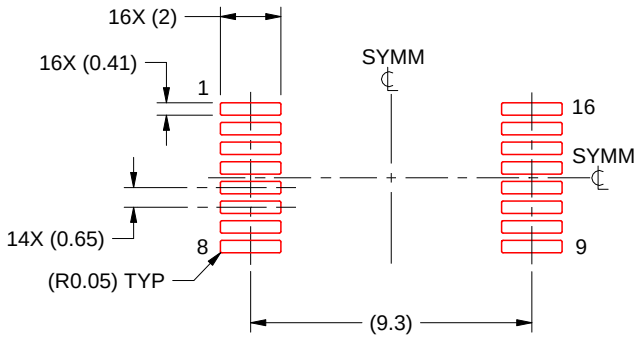
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

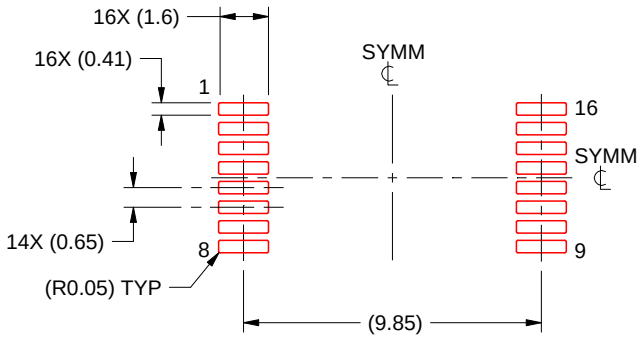
DHA0016A

SSOP - 2.6 mm max height

SMALL OUTLINE PACKAGE



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE



HV / ISOLATION OPTION
8.2 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLES
BASED ON 0.125 mm THICK STENCIL
SCALE: 4X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月