UCC21520-Q1-Q1 4A、6A、5.7kV$_{RMS}$ の車載用絶縁型デュアル チャネル ゲート ドライバ

1 特長

- 車載アプリケーション認定済み
- 以下の結果で AEC-Q100 認定済み:
  - デバイス温度グレード 1
- 機能安全品質管理
  - 機能安全システムの設計に役立つ資料を利用可能
- 接合部温度範囲:–40～+150℃
- スイッチング パラメータ:
  - 伝搬遅延時間:33ns (代表値)
  - 最小パルス幅:20ns
  - 最大パルス幅歪み:6ns
- 125V/ns を超える同相過渡耐性 (CMTI)
- 最大 10kV のサージ耐性
- 絶縁バリアの寿命:40 年超
- ピーク ソース 4A、ピーク シンク 6A の出力
- 3V～18V の入力 VCCI 範囲により、デジタルとアナログの両方のコントローラと接続可能
- 最大 25V の VDD 出力駆動電源
  - 5V および 8V VDD UVLO オプション
- オーバーラップおよびデッド タイムをプログラミング可能
- 高速なディセーブルによる電源シーケンス
- 安全関連認証:
  - DIN EN IEC 60747-17 (VDE 0884-17) に準拠した強化絶縁耐圧:8000V$_{PK}$
  - UL 1577 に準拠した絶縁耐圧:5.7kV$_{RMS}$ (1 分間)
  - IEC 60950-1、IEC 62368-1、IEC 61010-1、IEC 60601-1 最終製品規格による CSA 認証
  - GB4943.1-2022 準拠の CQC 認証

2 アプリケーション

- HEV および BEV バッテリ充電器
- DC-DC および AC-DC 電源の絶縁コンバータ
- 無停電電源 (UPS)

3 概要

UCC21520-Q1 は絶縁されたデュアル チャネルのゲート ドライバで、ピーク電流はソース 4A、シンク 6A です。パワー MOSFET、IGBT、SiC MOSFET (最大 5MHz) を駆動するように設計されています。

入力側は、5.7kV$_{RMS}$ の強化絶縁バリアによって 2 つの出力ドライバと分離されており、同相過渡耐性 (CMTI) は 125V/ns 以上です。2 つの 2 次側ドライバ間は、内部的に機能絶縁されているため、1500V$_{DC}$ までの電圧で動作します。

すべてのドライバは、2 つのローサイド ドライバ、2 つのハイサイド ドライバ、またはデッドタイム (DT) をプログラム可能な 1 つのハーフ ブリッジ ドライバとして構成可能です。ディセーブル ピンは、両方の出力を同時にシャットダウンし、オープンまたは接地されると通常動作になります。フェイルセーフ手法として、1 次側のロジック障害が発生すると、両方の出力が強制的に Low になります。

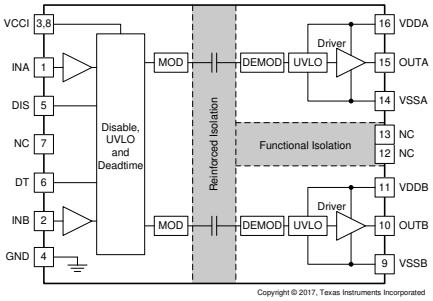
各デバイスは、最大 25V の VDD 電源電圧に対応できます。VCCI 入力範囲が 3V～18V と広いため、このドライバはアナログとデジタル両方のコントローラとの接続に適しています。すべての電源電圧ピンには、低電圧誤動作防止 (UVLO) 保護機能が搭載されています。

これらの高度な機能により、UCC21520-Q1 は高効率、高電力密度、および堅牢性を実現します。

デバイスの比較

部品番号	パッケージ (1)	UVLO レベル
UCC21520-Q1	DW (SOIC 16)	8 V
UCC21520A-Q1	DW (SOIC 16)	5 V

(1) 供給されているすべてのパッケージについては、セクション 13 を参照してください。



機能ブロック図

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4 Pin Configuration and Functions

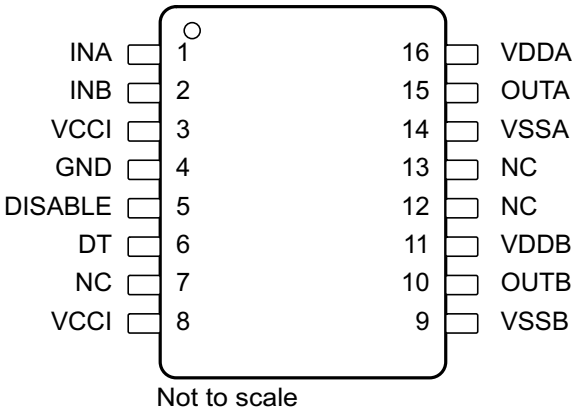


図 4-1. DW Package 16-Pin SOIC Top View

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
DISABLE	5	I	Disables both driver outputs if asserted high, enables if set low or left open. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity. Bypass using a ≈1nF low ESR/ESL capacitor close to DIS pin when connecting to a micro controller with distance.
DT	6	I	Programmable dead time function. Tying DT to VCCI allows the outputs to overlap. Placing a 2-kΩ to 500-kΩ resistor (RDT) between DT and GND adjusts dead time according to: DT (in ns) = 10 x R_{DT} (in kΩ). It is recommended to parallel a ceramic capacitor, <1nF, close to the DT pin with R_{DT} to achieve better noise immunity. It is not recommended to leave DT floating.

表 4-1. Pin Functions (続き)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
GND	4	P	Primary-side ground reference. All signals in the primary side are referenced to this ground.
INA	1	I	Input signal for A channel. INA input has a TTL/CMOS compatible input threshold. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity.
INB	2	I	Input signal for B channel. INB input has a TTL/CMOS compatible input threshold. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity.
NC	7	–	No Internal connection.
NC	12	–	No internal connection.
NC	13	–	No internal connection.
OUTA	15	O	Output of driver A. Connect to the gate of the A channel FET or IGBT.
OUTB	10	O	Output of driver B. Connect to the gate of the B channel FET or IGBT.
VCCI	3	P	Primary-side supply voltage. Locally decoupled to GND using a low ESR/ESL capacitor located as close to the device as possible.
VCCI	8	P	Primary-side supply voltage. This pin is internally shorted to pin 3.
VDDA	16	P	Secondary-side power for driver A. Locally decoupled to VSSA using a low ESR/ESL capacitor located as close to the device as possible.
VDDB	11	P	Secondary-side power for driver B. Locally decoupled to VSSB using low ESR/ESL capacitor located as close to the device as possible.
VSSA	14	P	Ground for secondary-side driver A. Ground reference for secondary side A channel.
VSSB	9	P	Ground for secondary-side driver B. Ground reference for secondary side B channel.

(1) P = Power, G = Ground, I = Input, O = Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Input bias pin supply voltage	VCCI to GND	–0.3	20	V
Driver bias supply	VDDA-VSSA, VDDB-VSSB	–0.3	30	V
Output signal voltage	OUTA to VSSA, OUTB to VSSB	–0.3	VDDA/B + 0.3	V
	OUTA to VSSA, OUTB to VSSB, Transient for 200 ns	–2	VDDA/B + 0.3	V
Input signal voltage	INA, INB, DIS, DT to GND	–0.3	VCCI + 0.3	V
	INA, INB Transient for 50ns	–5	VCCI + 0.3	V
Junction temperature, T_J [2]		–40	150	℃
Storage temperature, T_{stg}		–65	150	℃

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) To maintain the recommended operating conditions for TJ, see the Section 6.4

5.2 ESD Ratings (Automotive)

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]	±2000	V
		Charged device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCI}	VCCI Input supply voltage		3	18	V
VDDA, VDDB	Driver output bias supply	UCC21520A 5-V UVLO version	6.5	25	V
VDDA, VDDB	Driver output bias supply	UCC21520 8-V UVLO version	9.2	25	V
T_J	Junction temperature		–40	150	℃

5.4 Thermal Information

THERMAL METRIC(1)		UCC21520-Q1 DW-16 (SOIC)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	69.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36.9	°C/W
Ψ_{JT}	Junction-to-top(center) characterization parameter	22.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	36	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)	VCCI = 5V, VDDA/VDDB = 20V, INA/B = 3.3V, 460kHz 50% duty cycle square wave, CL=2.2nF, T_J=150℃, T_A=25℃			950	mW
P_{DI}	Maximum power dissipation by transmitter side				50	mW
P_{DA}, P_{DB}	Maximum power dissipation by each driver side				450	mW

5.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
General				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	>8	mm
CPG	External Creepage(1)	Shortest terminal-to-terminal distance across the package surface	>8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>17	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material Group	According to IEC 60664-1	I	
	Overvoltage category IEC 60664-1	Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17) (2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test	1500	V_{RMS}
		DC voltage	2121	V_{DC}
V_{IMP}	Maximum inpulse voltage	Tested in air, 1.2/50-µs waveform per IEC 62368-1	7692	V_{PK}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification) $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production)	8000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(3)	$V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	10000	V_{PK}
q_{pd}	Apparent charge(4)	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤5	
		Method b1: At routine test (100% production) and preconditioning (type test), $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	~1.2	pF
R_{IO}	Insulation resistance, input to output(5)	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$ = 5700 V_{RMS}, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$ = 6840 V_{RMS}, t = 1 s (100% production)	5700	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed-circuit board are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-pin device.

5.7 Safety Limiting Values

PARAMETER		TEST CONDITIONS	SIDE	MIN	TYP	MAX	UNIT
I_S	Safety output supply current	$R_{\theta JA}$ = 69.8°C/W, $V_{DDA/B}$ = 15 V, T_J = 150°C, T_A = 25°C	DRIVER A, DRIVER B			58	mA
		$R_{\theta JA}$ = 69.8°C/W, $V_{DDA/B}$ = 25 V, T_J = 150°C, T_A = 25°C				34	
P_S	Safety supply power	$R_{\theta JA}$ = 69.8°C/W, T_J = 150°C, T_A = 25°C	INPUT			50	mW
			DRIVER A			870	
			DRIVER B			870	
			TOTAL			1790	
T_S	Maximum safety temperature(1)					150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J , specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A. The junction-to-air thermal resistance, R_{qJA}, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter: $T_J = T_A + R_{qJA} \times P$, where P is the power dissipated in the device. $T_{J(max)} = T_S = T_A + R_{qJA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature. $P_S = I_S \times V_I$, where VI is the maximum supply voltage.

5.8 Electrical Characteristics

V_{VCCI} = 3.3 V or 5 V, 0.1-µF capacitor from VCCI to GND, V_{VDDA} = V_{VDDB} = 15 V, 1-µF capacitor from VDDA and VDDB to VSSA and VSSB, T_J = –40°C to +150°C, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS						
I_{VCCI}	VCCI quiescent current	V_{INA} = 0 V, V_{INB} = 0 V		1.4	2.0	mA
I_{VDDA}, I_{VDDB}	VDDA and VDDB quiescent current	V_{INA} = 0 V, V_{INB} = 0 V		1.0	2.5	mA
I_{VCCI}	VCCI operating current	(f = 500 kHz) current per channel		3	3.5	mA
I_{VDDA}, I_{VDDB}	VDDA and VDDB operating current	(f = 500 kHz) current per channel, C_{OUT} = 100 pF		2.5	4.2	mA
VCC SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLDS						
V_{VCCI_ON}	UVLO Rising threshold		2.55	2.7	2.85	V
V_{VCCI_OFF}	UVLO Falling threshold		2.35	2.5	2.65	V
V_{VCCI_HYS}	UVLO Threshold hysteresis			0.2		V
VDD SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLDS						
V_{VDDA_ON}, V_{VDDB_ON}	UVLO Rising threshold	5-V UVLO	5.7	6.0	6.3	V
V_{VDDA_OFF}, V_{VDDB_OFF}	UVLO Falling threshold	5-V UVLO	5.4	5.7	6.0	V
V_{VDDA_HYS}, V_{VDDB_HYS}	UVLO Threshold hysteresis	5-V UVLO		0.3		V
V_{VDDA_ON}, V_{VDDB_ON}	UVLO Rising threshold	8-V UVLO	7.7	8.5	8.9	V
V_{VDDA_OFF}, V_{VDDB_OFF}	UVLO Falling threshold	8-V UVLO	7.2	7.9	8.4	V
V_{VDDA_HYS}, V_{VDDB_HYS}	UVLO Threshold hysteresis	8-V UVLO		0.6		V
INA, INB AND ENABLE						
V_{INAH}, V_{INBH}, V_{ENH}	Input high threshold voltage		1.2	1.8	2	V
V_{INAL}, V_{INBL}, V_{ENL}	Input low threshold voltage		0.8	1	1.2	V
V_{INA_HYS}, V_{INB_HYS}, V_{EN_HYS}	Input threshold hysteresis			0.8		V
V_{INA}, V_{INB}	Negative transient, ref to GND, 100 ns pulse	Not production tested, bench test only	–5			V
OUTPUT						

5.8 Electrical Characteristics (続き)

V_{VCCI} = 3.3 V or 5 V, 0.1-µF capacitor from VCCI to GND, V_{VDDA} = V_{VDDB} = 15 V, 1-µF capacitor from VDDA and VDDB to VSSA and VSSB, T_J = –40°C to +150°C, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OA+}, I_{OB+}	Peak output source current	C_{VDD} = 10 µF, C_{LOAD} = 0.18 µF, f = 1 kHz, bench measurement		4		A
I_{OA-}, I_{OB-}	Peak output sink current	C_{VDD} = 10 µF, C_{LOAD} = 0.18 µF, f = 1 kHz, bench measurement		6		A
R_{OHA}, R_{OHB}	Output resistance at high state	I_{OUT} = –10 mA, T_A = 25°C, R_{OHA}, R_{OHB} do not represent drive pull-up performance. See t_{RISE} in セクション 5.10 and セクション 7.3.4 for details.		5		Ω
R_{OLA}, R_{OLB}	Output resistance at low state	I_{OUT} = 10 mA, T_A = 25°C		0.55		Ω
V_{OHA}, V_{OHB}	Output voltage at high state	V_{VDDA}, V_{VDDB} = 15 V, I_{OUT} = –10 mA, T_A = 25°C		14.95		V
V_{OLA}, V_{OLB}	Output voltage at low state	V_{VDDA}, V_{VDDB} = 15 V, I_{OUT} = 10 mA, T_A = 25°C		5.5		mV

5.9 Timing Requirements

DEADTIME AND OVERLAP PROGRAMMING		MIN	NOM	MAX	UNIT
DT	DT pin tied to VCCI	Ovelap determined by INA, INB	Ovelap determined by INA, INB	Ovelap determined by INA, INB	ns
DT	Dead time, R_{DT} = 10 kΩ	80	100	120	ns
DT	Dead time, R_{DT} = 20 kΩ	160	200	240	ns
DT	Dead time, R_{DT} = 50 kΩ	400	500	600	ns

5.10 Switching Characteristics

V_{VCCI} = 3.3 V or 5 V, 0.1-µF capacitor from VCCI to GND, V_{VDDA} = V_{VDDB} = 12 V, 1-µF capacitor from VDDA and VDDB to VSSA and VSSB, load capacitance C_{OUT} = 0 pF, T_J = –40°C to +150°C. (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RISE}	Output rise time, 20% to 80% measured points	C_{OUT} = 1.8 nF		6	16	ns
t_{FALL}	Output fall time, 90% to 10% measured points	C_{OUT} = 1.8 nF		7	12	ns
t_{PWmin}	Minimum pulse width	Output off for less than minimum, C_{OUT} = 0pF			20	ns
t_{PDHL}	Propagation delay from INx to OUTx falling edges		26	33	45	ns
t_{PDLH}	Propagation delay from INx to OUTx rising edges		26	33	45	ns
t_{PWD}	Pulse width distortion $\lvert t_{PDLH} - t_{PDHL} \rvert$				6	ns
t_{DM}	Propagation Delay Matching for Dual Channel Driver	Input Pulse Width = 100ns, 500kHz, T_J = -40°C to -10°C $\lvert t_{PDLHA} - t_{PDLHB} \rvert$, $\lvert t_{PDHLA} - t_{PDHLB} \rvert$			6.5	ns
t_{DM}	Propagation Delay Matching for Dual Channel Driver	Input Pulse Width = 100ns, 500kHz, T_J = -10°C to +150°C $\lvert t_{PDLHA} - t_{PDLHB} \rvert$, $\lvert t_{PDHLA} - t_{PDHLB} \rvert$			5	ns
t_{VCCI+} to OUT	VCCI Power-up Delay Time: UVLO Rise to OUTA, OUTB	INA or INB tied to VCCI			50	µs
t_{VDD+} to OUT	VDDA. VDDB Power-up Delay Time: UVLO Rise to OUTA, OUTB	INA or INB tied to VCCI			10	µs
$\lvert CM_H \rvert$	High-level common-mode transient immunity (See セクション 6.6)	Slew rate of GND versus VSSA/B, INA and INB both are tied to GND or VCCI; V_{CM} = 1500V	125			V/ns
$\lvert CM_L \rvert$	Low-level common-mode transient immunity (See セクション 6.6)	Slew rate of GND versus VSSA/B, INA and INB both are tied to GND or VCCI; V_{CM} = 1500V	125			V/ns

5.11 Insulation Characteristics Curves

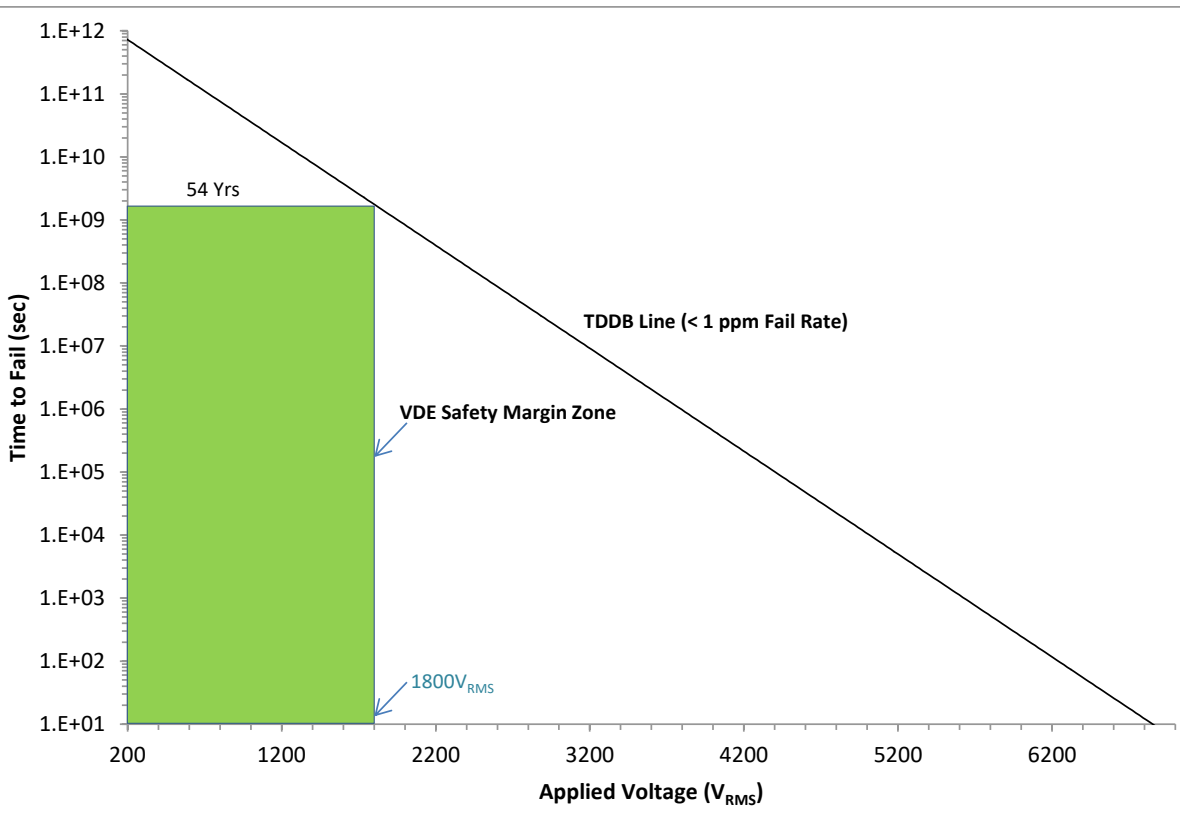


図 5-1. Reinforced Isolation Capacitor Life Time Projection

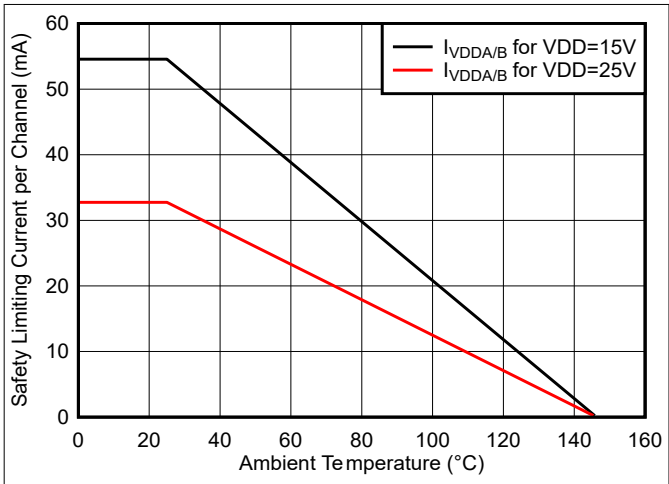


図 5-2. Thermal Derating Curve for Safety-Related Limiting Current (Current in Each Channel with Both Channels Running Simultaneously)

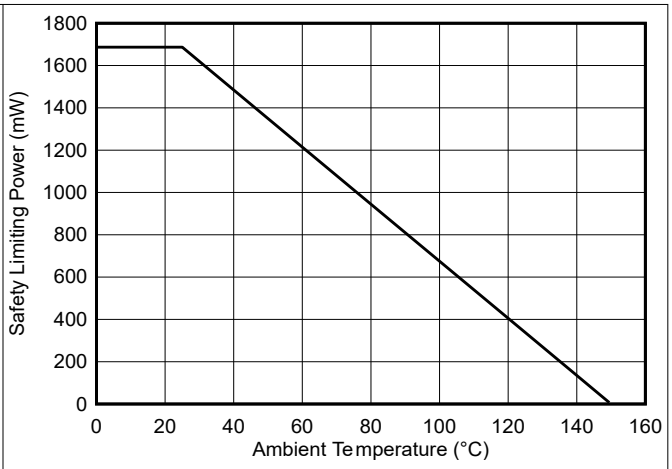


図 5-3. Thermal Derating Curve for Safety-Related Limiting Power

5.12 Typical Characteristics

VDDA = VDDB= 15 V, VCCI = 3.3 V, T_A = 25°C, No load unless otherwise noted.

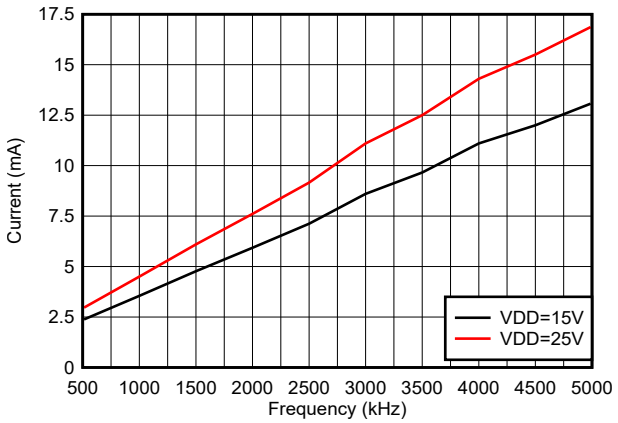


図 5-4. Per Channel Current Consumption vs Frequency (No Load, VDD = 15 V or 25 V)

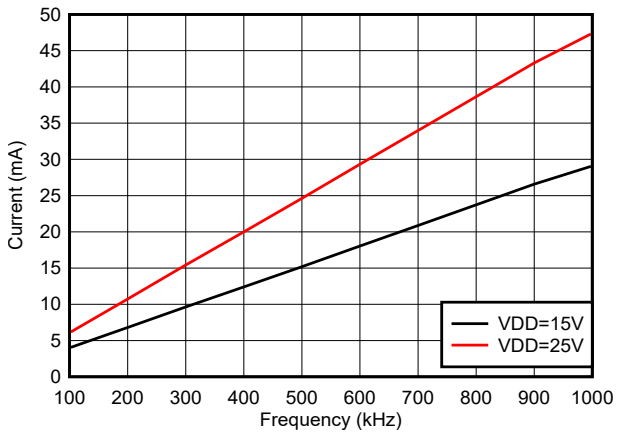


図 5-5. Per Channel Current Consumption ($I_{VDDA/B}$) vs Frequency (1-nF Load, VDD = 15 V or 25 V)

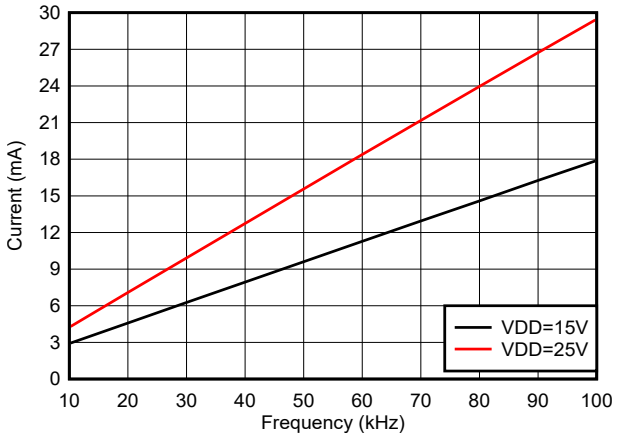


図 5-6. Per Channel Current Consumption ($I_{VDDA/B}$) vs Frequency (10-nF Load, VDD = 15 V or 25 V)

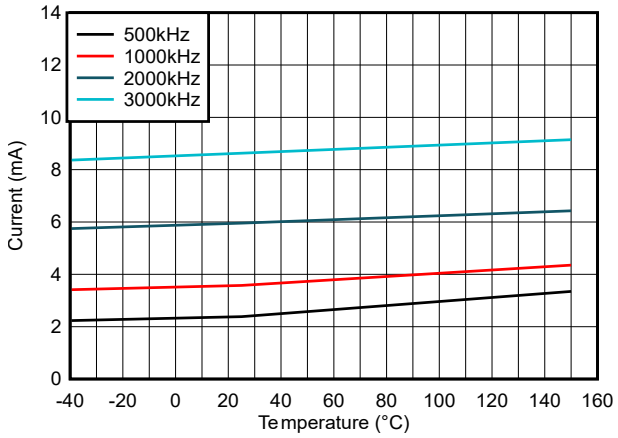


図 5-7. Per Channel ($I_{VDDA/B}$) Supply Current vs Temperature (No Load, Different Switching Frequencies)

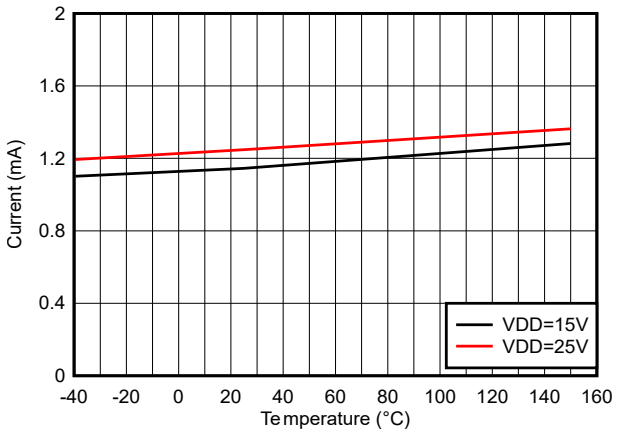


図 5-8. Per Channel ($I_{VDDA/B}$) Quiescent Supply Current vs Temperature (No Load, Input Low, No Switching)

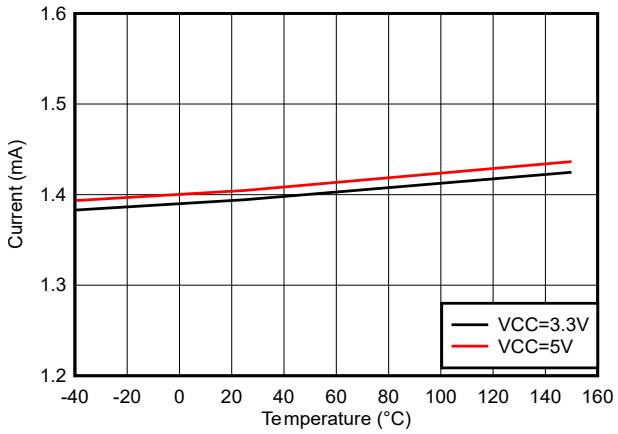


図 5-9. I_{VCCI} Quiescent Supply Current vs Temperature (No Load, Input Low, No Switching)

5.12 Typical Characteristics (continued)

VDDA = VDDB= 15 V, VCCI = 3.3 V, T_A = 25°C, No load unless otherwise noted.

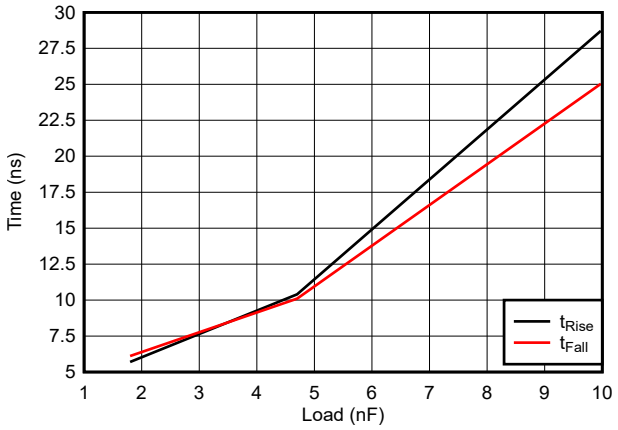


図 5-10. Rising and Falling Times vs Load (VDD = 15 V)

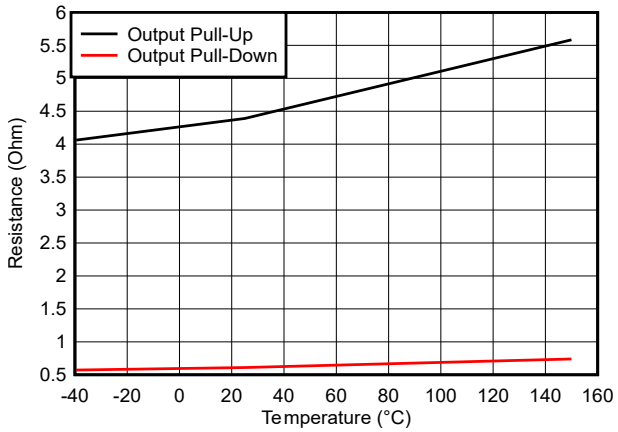


図 5-11. Output Resistance vs Temperature

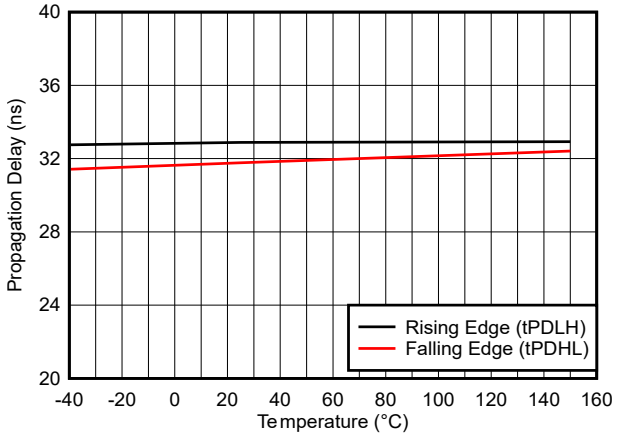


図 5-12. Propagation Delay vs Temperature

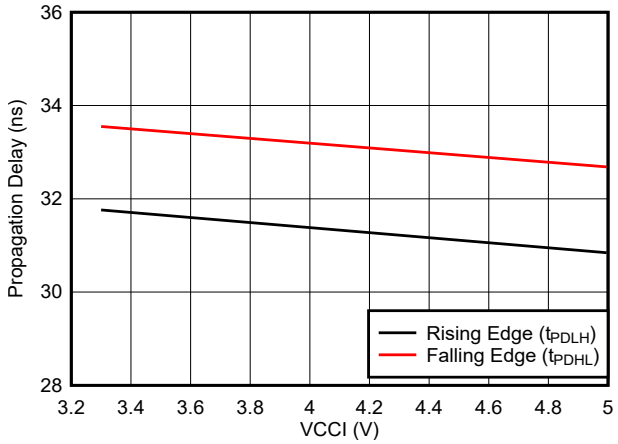


図 5-13. Propagation Delay vs VCCI

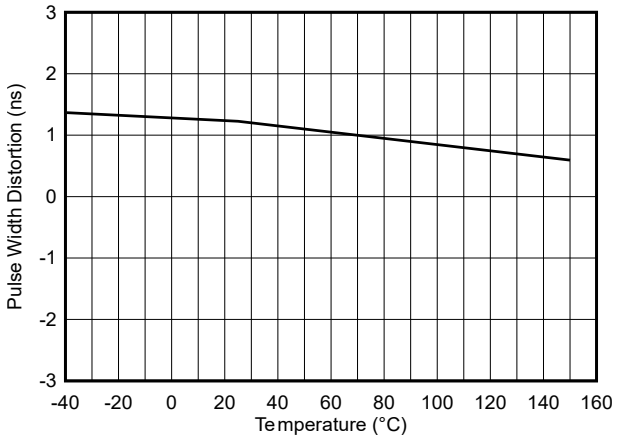


図 5-14. Pulse Width Distortion vs Temperature

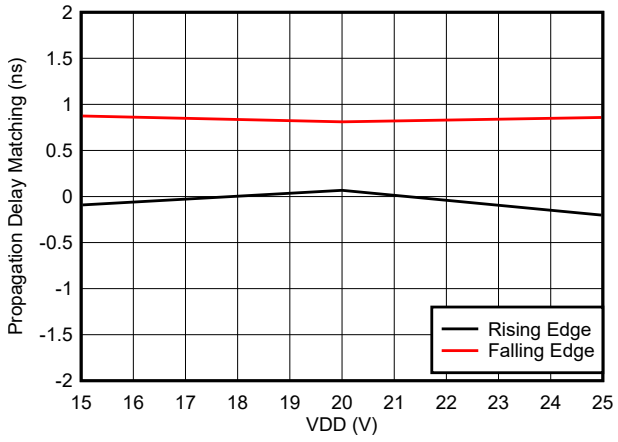


図 5-15. Propagation Delay Matching (t_{DM}) vs VDD

5.12 Typical Characteristics (continued)

VDDA = VDDB= 15 V, VCCI = 3.3 V, T_A = 25°C, No load unless otherwise noted.

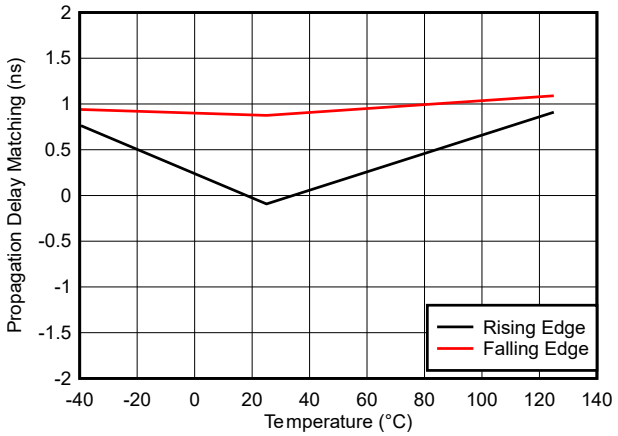


図 5-16. Propagation Delay Matching (t_{DM}) vs Temperature

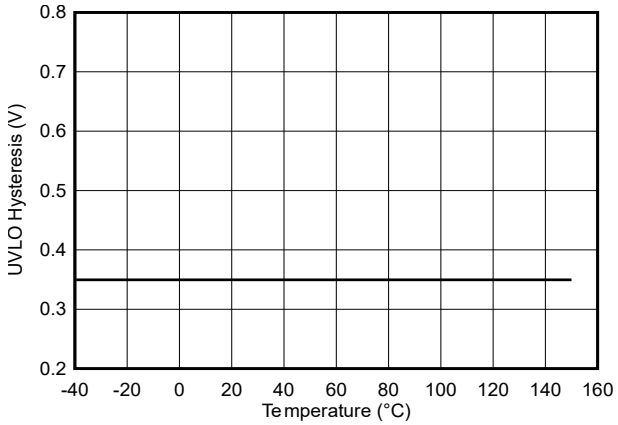


図 5-17. VDD 5-V UVLO Hysteresis vs Temperature

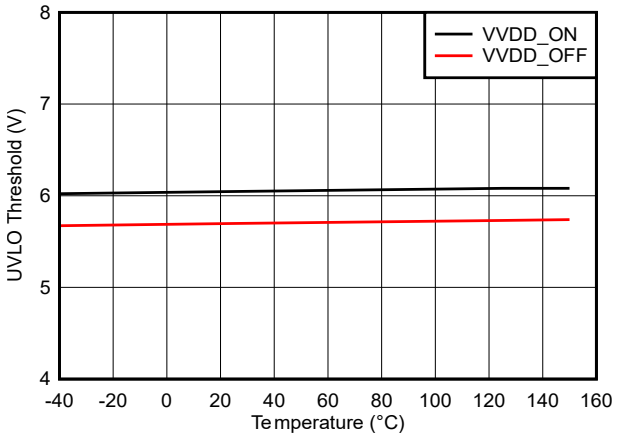


図 5-18. VDD 5-V UVLO Threshold vs Temperature

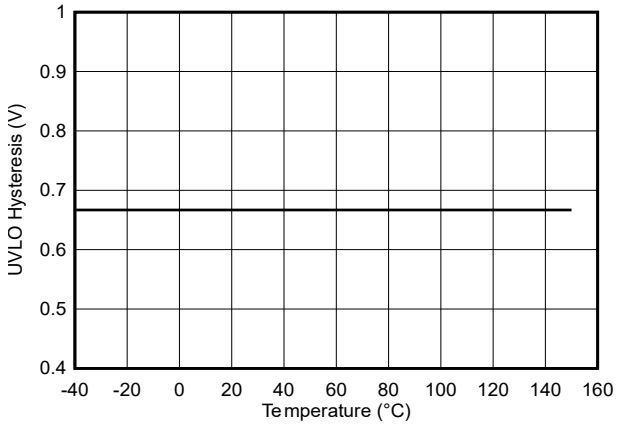


図 5-19. VDD 8-V UVLO Hysteresis vs Temperature

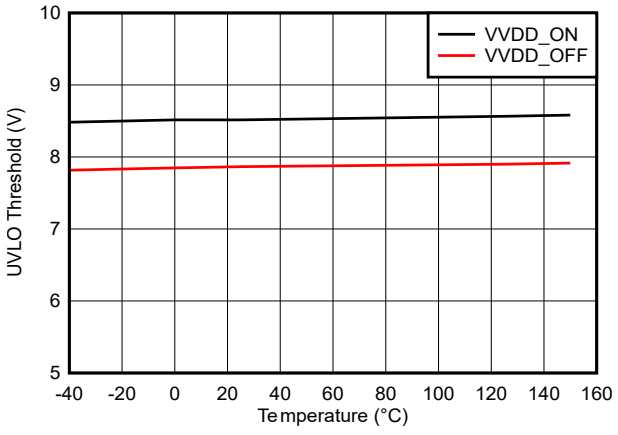


図 5-20. VDD 8-V UVLO Threshold vs Temperature

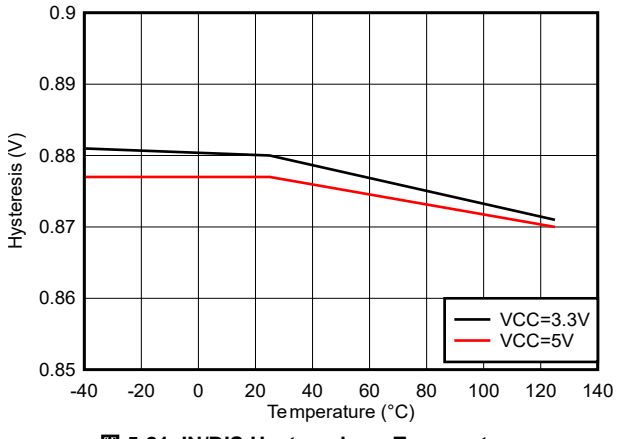


図 5-21. IN/DIS Hysteresis vs Temperature

5.12 Typical Characteristics (continued)

VDDA = VDDB= 15 V, VCCI = 3.3 V, T_A = 25°C, No load unless otherwise noted.

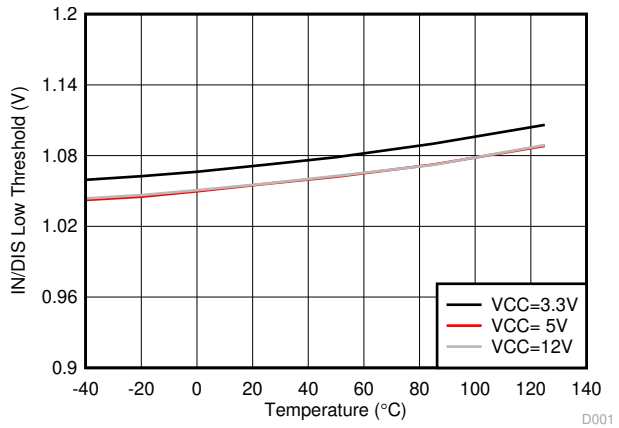


図 5-22. IN/DIS Low Threshold

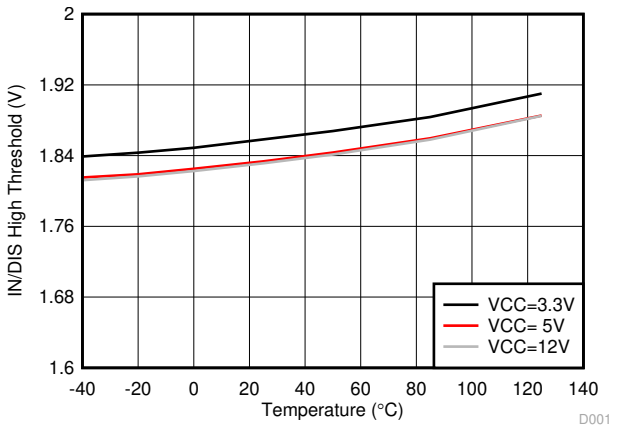


図 5-23. IN/DIS High Threshold

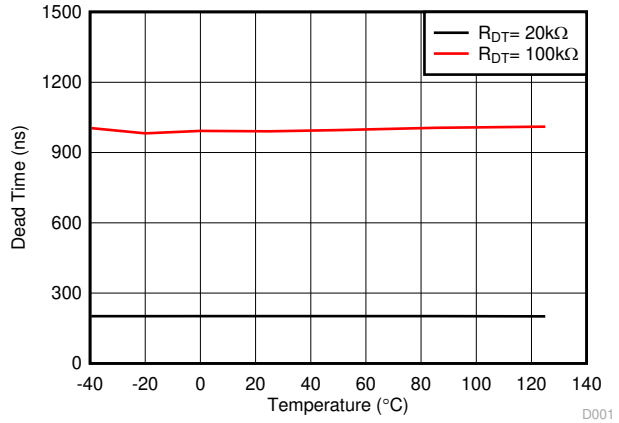


図 5-24. Dead Time vs Temperature (with R_{DT} = 20 kΩ and 100 kΩ)

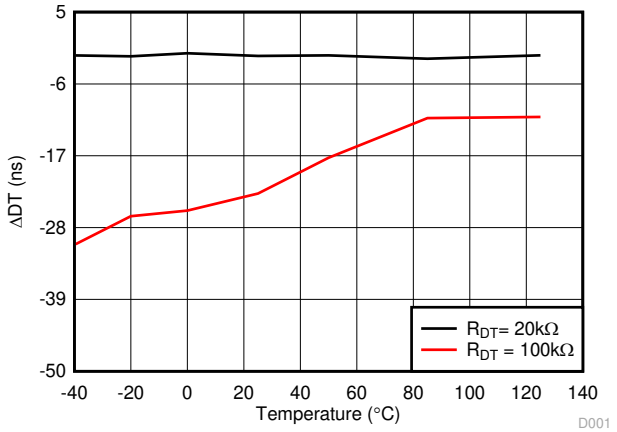


図 5-25. Dead Time Matching vs Temperature (with R_{DT} = 20 kΩ and 100 kΩ)

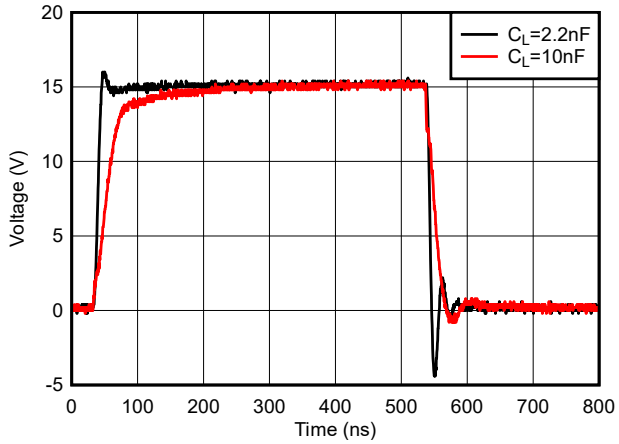


図 5-26. Typical Output Waveforms

6 Parameter Measurement Information

6.1 Propagation Delay and Pulse Width Distortion

図 6-1 shows how one calculates pulse width distortion (t_{PWD}) and delay matching (t_{DM}) from the propagation delays of channels A and B. It can be measured by ensuring that both inputs are in phase and disabling the dead time function by shorting the DT Pin to VCC.

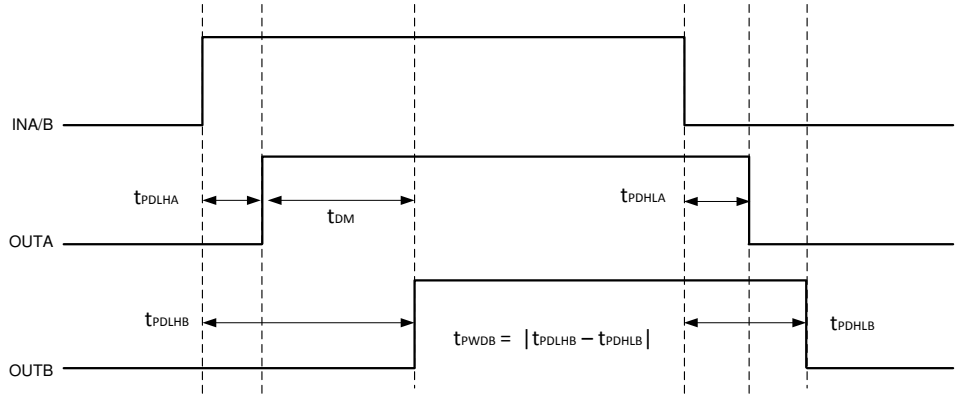


図 6-1. Overlapping Inputs, Dead Time Disabled

6.2 Rising and Falling Time

図 6-2 shows the criteria for measuring rising (t_{RISE}) and falling (t_{FALL}) times. For more information on how short rising and falling times are achieved see セクション 7.3.4.

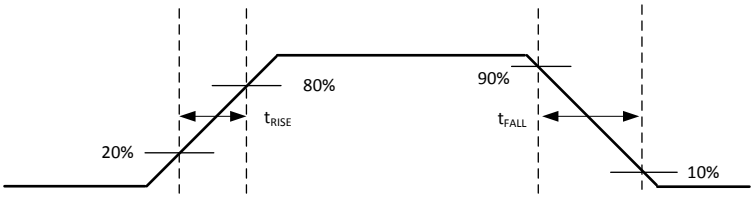


図 6-2. Rising and Falling Time Criteria

6.3 Input and Disable Response Time

図 6-3 shows the response time of the disable function. It is recommended to bypass using a ≈1nF low ESR/ESL capacitor close to DIS pin when connecting DIS pin to a micro controller with distance. For more information, see セクション 7.4.1.

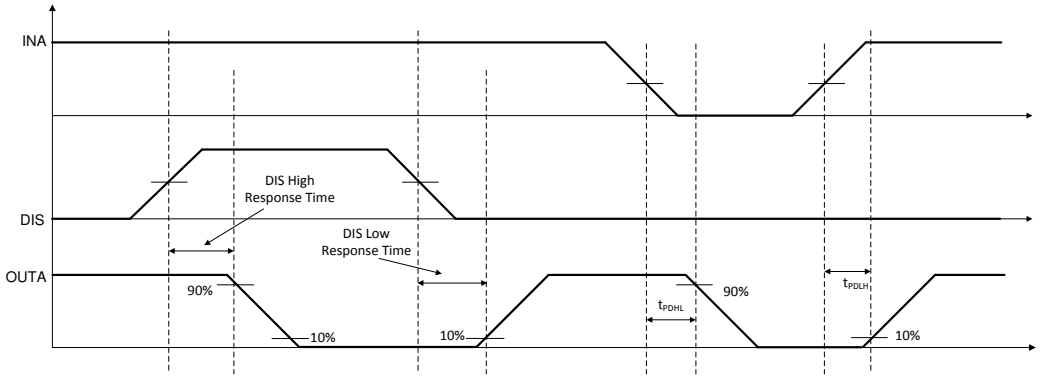


図 6-3. Disable Pin Timing

6.4 Programable Dead Time

Leaving the DT pin open or tying it to GND through an appropriate resistor (R_{DT}) sets a dead-time interval. For more details on dead time, refer to セクション 7.4.2.

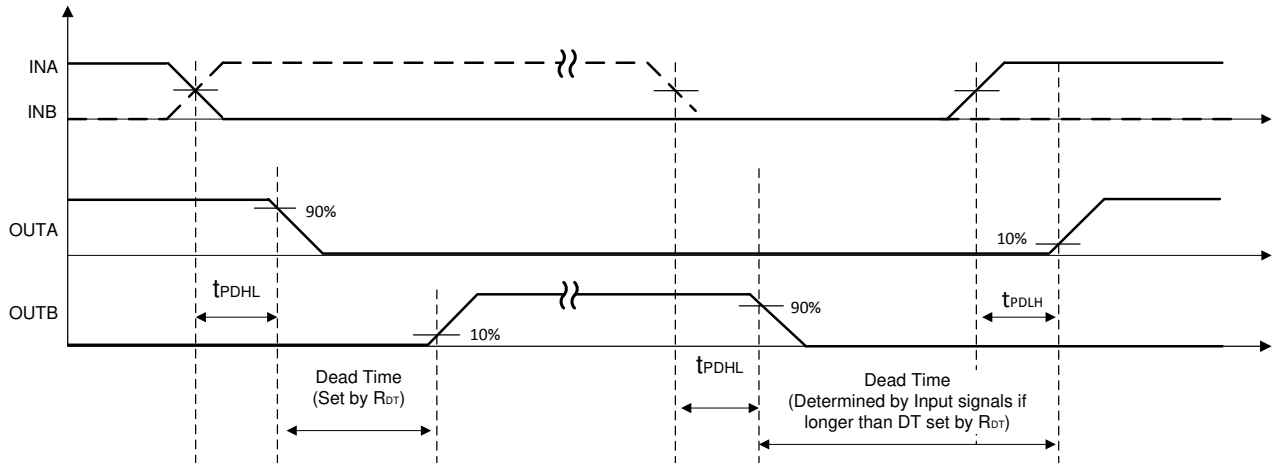


図 6-4. Dead-Time Switching Parameters

6.5 Power-up UVLO Delay to OUTPUT

Before the driver is ready to deliver a proper output state, there is a power-up delay from the UVLO rising edge to output and it is defined as $t_{VCCI+\ to\ OUT}$ for VCCI UVLO (typically 40us) and $t_{VDD+\ to\ OUT}$ for VDD UVLO (Max 10us). It is recommended to consider proper margin before launching PWM signal after the driver's VCCI and VDD bias supply is ready. 図 6-5 and 図 6-6 show the power-up UVLO delay timing diagram for VCCI and VDD.

If INA or INB are active before VCCI or VDD have crossed above their respective on thresholds, the output will not update until $t_{VCCI+\ to\ OUT}$ or $t_{VDD+\ to\ OUT}$ after VCCI or VDD crossing its UVLO rising threshold. However, when either VCCI or VDD receive a voltage less than their respective off thresholds, there is <2µs delay, depending on the voltage slew rate on the supply pins, before the outputs are held low. This asymmetric delay is designed to ensure safe operation during VCCI or VDD brownouts.

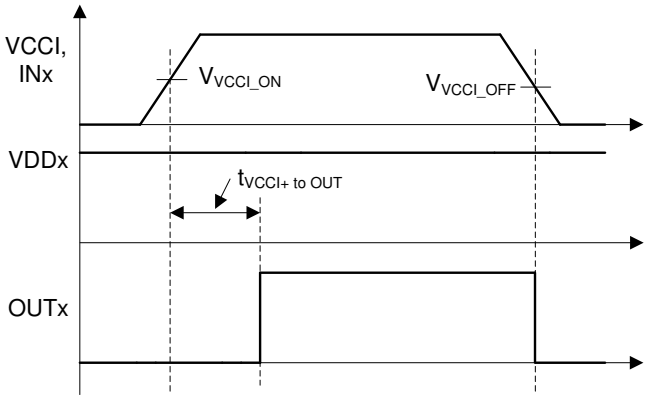


図 6-5. VCCI Power-up UVLO Delay

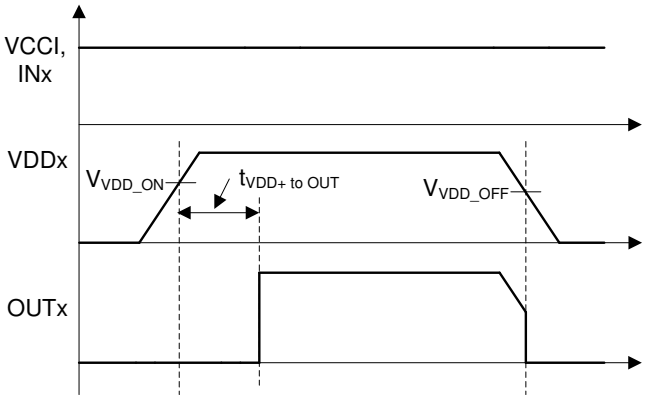


図 6-6. VDDA/B Power-up UVLO Delay

6.6 CMTI Testing

図 6-7 is a simplified diagram of the CMTI testing configuration.

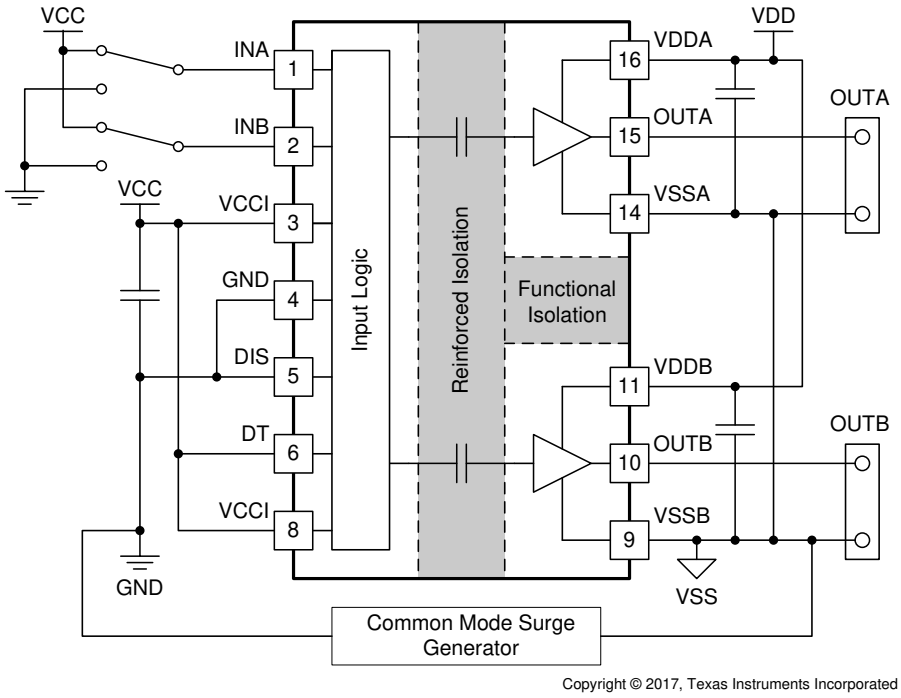


図 6-7. Simplified CMTI Testing Setup

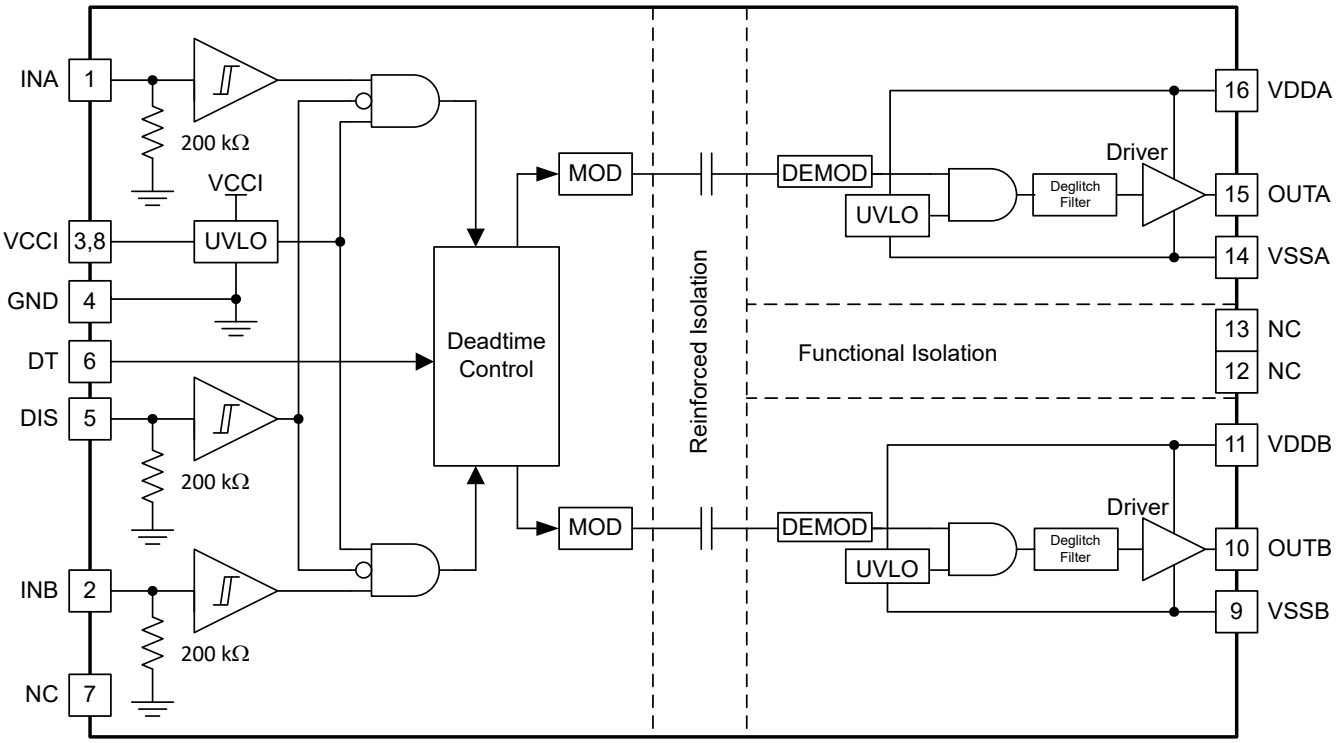
7 Detailed Description

7.1 Overview

In order to switch power transistors rapidly and reduce switching power losses, high-current gate drivers are often placed between the output of control devices and the gates of power transistors. There are several instances where controllers are not capable of delivering sufficient current to drive the gates of power transistors. This is especially the case with digital controllers, since the input signal from the digital controller is often a 3.3-V logic signal capable of only delivering a few mA.

The UCC21520-Q1 is a flexible dual gate driver which can be configured to fit a variety of power supply and motor drive topologies, as well as drive several types of transistors, including SiC MOSFETs. The UCC21520-Q1 has many features that allow it to integrate well with control circuitry and protect the gates it drives such as: resistor-programmable dead time (DT) control, a DISABLE pin, and under voltage lock out (UVLO) for both input and output voltages. The UCC21520-Q1 also holds its outputs low when the inputs are left open or when the input pulse is not wide enough. The driver inputs are CMOS and TTL compatible for interfacing to digital and analog power controllers alike. Each channel is controlled by its respective input pins (INA and INB), allowing full and independent control of each of the outputs.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 VDD, VCCI, and Undervoltage Lock Out (UVLO)

The UCC21520-Q1 has an internal undervoltage lock out (UVLO) protection feature on the supply circuit blocks between the VDD and VSS pins for both outputs. When the VDD bias voltage is lower than V_{VDD_ON} at device start-up or lower than V_{VDD_OFF} after start-up, the VDD UVLO feature holds the effected output low, regardless of the status of the input pins (INA and INB).

When the output stages of the driver are in an unbiased or UVLO condition, the driver outputs are held low by an active clamp circuit that limits the voltage rise on the driver outputs (Illustrated in 図 7-1). In this condition, the upper PMOS is resistively held off by R_{Hi-Z} while the lower NMOS gate is tied to the driver output through R_{CLAMP}. In this configuration, the output is effectively clamped to the threshold voltage of the lower NMOS device, typically around 1.5 V, when no bias power is available.

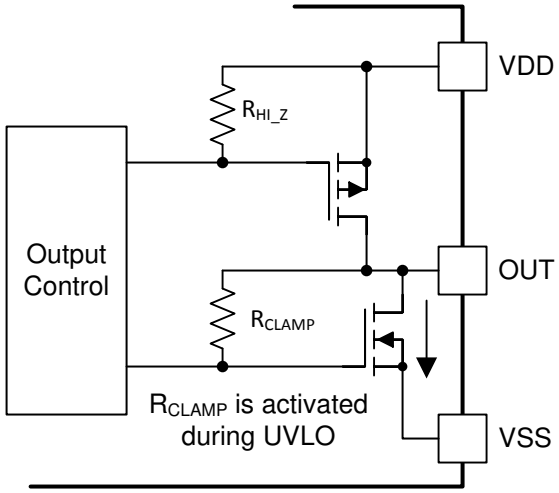


図 7-1. Simplified Representation of Active Pulldown Feature

The VDD UVLO protection has a hysteresis feature (V_{VDD_HYS}). This hysteresis prevents chatter when there is ground noise from the power supply. Also this allows the device to accept small drops in bias voltage, which is bound to happen when the device starts switching and operating current consumption increases suddenly.

The input side of the UCC21520-Q1 also has an internal undervoltage lock out (UVLO) protection feature. The device isn't active unless the voltage, VCCI, is going to exceed V_{VCCI_ON} on start up. And a signal will cease to be delivered when that pin receives a voltage less than V_{VCCI_OFF}. And, just like the UVLO for VDD, there is hysteresis (V_{VCCI_HYS}) to ensure stable operation.

All versions of the UCC21520-Q1 can withstand an absolute maximum of 30 V for VDD, and 20 V for VCCI.

表 7-1. UCC21520-Q1 VCCI UVLO Feature Logic

CONDITION	INPUTS		OUTPUTS	
	INA	INB	OUTA	OUTB
VCCI-GND < V_{VCCI_ON} during device start up	H	L	L	L
VCCI-GND < V_{VCCI_ON} during device start up	L	H	L	L
VCCI-GND < V_{VCCI_ON} during device start up	H	H	L	L
VCCI-GND < V_{VCCI_ON} during device start up	L	L	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	H	L	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	L	H	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	H	H	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	L	L	L	L

表 7-2. UCC21520-Q1 VDD UVLO Feature Logic

CONDITION	INPUTS		OUTPUTS	
	INA	INB	OUTA	OUTB
VDD-VSS < V_{VDD_ON} during device start up	H	L	L	L
VDD-VSS < V_{VDD_ON} during device start up	L	H	L	L
VDD-VSS < V_{VDD_ON} during device start up	H	H	L	L
VDD-VSS < V_{VDD_ON} during device start up	L	L	L	L
VDD-VSS < V_{VDD_OFF} after device start up	H	L	L	L
VDD-VSS < V_{VDD_OFF} after device start up	L	H	L	L
VDD-VSS < V_{VDD_OFF} after device start up	H	H	L	L
VDD-VSS < V_{VDD_OFF} after device start up	L	L	L	L

7.3.2 Input and Output Logic Table

表 7-3. INPUT/OUTPUT Logic Table (1)

Assume VCCI, VDDA, VDDB are powered up. See セクション 7.3.1 for more information on UVLO operation modes.

INPUTS		DISABLE	OUTPUTS		NOTE
INA	INB		OUTA	OUTB	
L	L	L or Left Open	L	L	If Dead Time function is used, output transitions occur after the dead time expires. See セクション 7.4.2
L	H	L or Left Open	L	H	
H	L	L or Left Open	H	L	
H	H	L or Left Open	L	L	DT is left open or programmed with R_{DT}
H	H	L or Left Open	H	H	DT pin pulled to VCCI
Left Open	Left Open	L or Left Open	L	L	-
X	X	H	L	L	-

(1) "X" means L, H or left open.

7.3.3 Input Stage

The input pins (INA, INB, and DIS) of the UCC21520-Q1 are based on a TTL and CMOS compatible input-threshold logic that is totally isolated from the VDD supply voltage. The input pins are easy to drive with logic-level control signals (such as those from 3.3-V micro-controllers), since the UCC21520-Q1 has a typical high threshold (V_{INAH}) of 1.8 V and a typical low threshold of 1 V, which vary little with temperature (see 図 5-22, 図 5-23). A wide hysterisis (V_{INA_HYS}) of 0.8 V makes for good noise immunity and stable operation. If any of the inputs are ever left open, internal pull-down resistors force the pin low. These resistors are typically 200 kΩ (see セクション 7.2). However, it is still recommended to ground an input if it is not being used.

Since the input side of the UCC21520-Q1 is isolated from the output drivers, the input signal amplitude can be larger or smaller than VDD, provided that it doesn't exceed the recommended limit. This allows greater flexibility when integrating with control signal sources, and allows the user to choose the most efficient VDD for their chosen gate. That said, the amplitude of any signal applied to INA or INB must *never* be at a voltage higher than VCCI.

7.3.4 Output Stage

The UCC21520-Q1 output stages feature a pull-up structure which delivers the highest peak-source current when it is most needed, during the Miller plateau region of the power-switch turn on transition (when the power switch drain or collector voltage experiences dV/dt). The output stage pull-up structure features a P-channel MOSFET and an additional *Pull-Up* N-channel MOSFET in parallel. The function of the N-channel MOSFET is to provide a brief boost in the peak-sourcing current, enabling fast turn on. This is accomplished by briefly turning on the N-channel MOSFET during a narrow instant when the output is changing states from low to high. The on-resistance of this N-channel MOSFET (R_{NMOS}) is approximately 1.47 Ω when activated.

The R_{OH} parameter is a DC measurement and it is representative of the on-resistance of the P-channel device only. This is because the *Pull-Up* N-channel device is held in the off state in DC condition and is turned on only for a brief instant when the output is changing states from low to high. Therefore the effective resistance of the UCC21520-Q1 pull-up stage during this brief turn-on phase is much lower than what is represented by the R_{OH} parameter. Therefore, the value of R_{OH} belies the fast nature of the UCC21520-Q1's turn-on time.

The pull-down structure in the UCC21520-Q1 is simply composed of an N-channel MOSFET. The R_{OL} parameter, which is also a DC measurement, is representative of the impedance of the pull-down state in the device. Both outputs of the UCC21520-Q1 are capable of delivering 4-A peak source and 6-A peak sink current pulses. The output voltage swings between VDD and VSS provides rail-to-rail operation, thanks to the MOS-out stage which delivers very low drop-out.

To ensure robust and reliable operation of gate drivers, pay special attention to the minimum pulse width. The minimum pulse width shown in the electrical characteristics table describes the minimum input pulse that would be passed to the output in an unloaded driver. This is dictated by the deglitch filter present in the driver IC. An input ON or OFF pulse width longer than the maximum specification is needed to guarantee an output state change and avoid potential shoot-through. With a loaded driver, extra precaution must be taken to ensure robust operation of the system. During gate switching, if the output state changes before the driver completes each transition, a non-zero current switching event occurs. Combined with layout parasitics, non-zero current switching can cause internal rail overshoot and EOS damage of the gate driver. Thus, a minimum output width is needed for reliable system operation. This minimum output pulse width is dependent on several factors: gate capacitance, VDD supply voltage, gate resistance, and PCB layout parasitics. The minimum pulse width for robust operation might be magnitudes larger than the minimum pulse width shown in the electrical characteristics table. System-level study should be carried out to determine the minimum output pulse width required for each system.

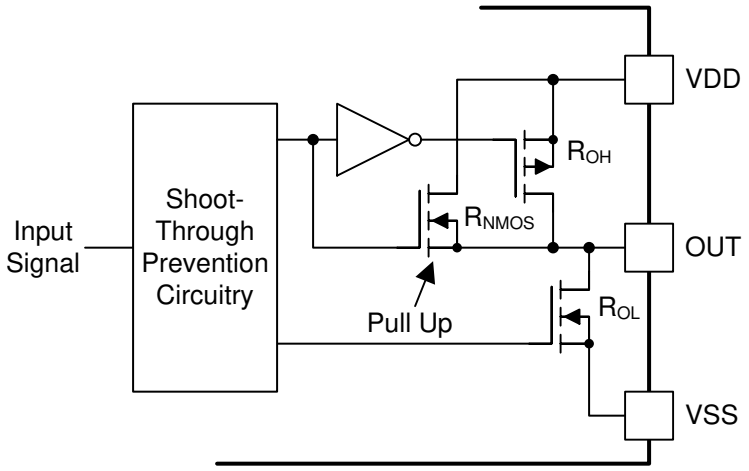


図 7-2. Output Stage

7.3.5 Diode Structure in the UCC21520-Q1

図 7-3 illustrates the multiple diodes involved in the ESD protection components of the UCC21520-Q1. This provides a pictorial representation of the absolute maximum rating for the device.

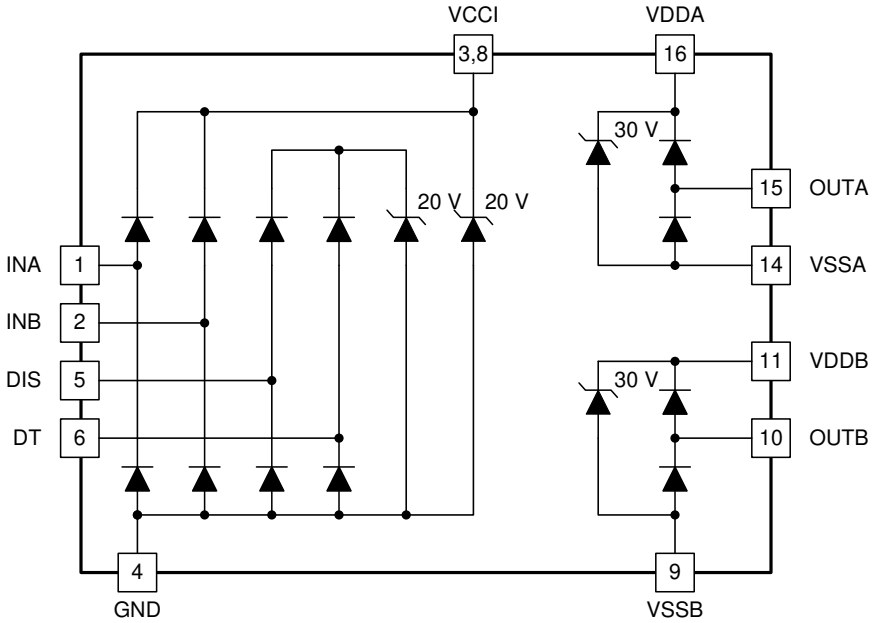


図 7-3. ESD Structure

7.4 Device Functional Modes

7.4.1 Disable Pin

Setting the DISABLE pin high shuts down both outputs simultaneously. Grounding (or left open) the DISABLE pin allows the UCC21520-Q1 to operate normally. The DISABLE response time is in the range of 20 ns and quite responsive, which is as fast as propagation delay. The DISABLE pin is only functional (and necessary) when VCCI stays above the UVLO threshold. It is recommended to tie this pin to ground if the DISABLE pin is not used to achieve better noise immunity, and it is recommended to bypass using a ≈1-nF low ESR/ESL capacitor close to DIS pin when connecting DIS pin to a micro controller with distance.

7.4.2 Programmable Dead-Time (DT) Pin

The UCC21520-Q1 allows the user to adjust dead time (DT) in the following ways:

7.4.2.1 Tying the DT Pin to VCC

Outputs completely match inputs, so no dead time is asserted. This allows outputs to overlap.

7.4.2.2 DT Pin Connected to a Programming Resistor Between DT and GND Pins

One can program t_{DT} by placing a resistor, R_{DT}, between the DT pin and GND. The appropriate R_{DT} value can be determined from 式 1, where R_{DT} is in kΩ and t_{DT} is in ns:

$$t_{DT} \approx 10 \times R_{DT} \quad (1)$$

The steady state voltage at DT pin is around 0.8 V, and the DT pin current will be less than 10uA when R_{DT}=100kΩ. When using R_{DT}> 5kΩ, it is recommended to parallel a ceramic capacitor, <1nF, close to the chip with R_{DT} to achieve better noise immunity and better dead time matching between two channels. It is not recommended to leave the DT pin floating.

An input signal's falling edge activates the programmed dead time for the other signal. The output signals' dead time is always set to the longer of either the driver's programmed dead time or the input signal's own dead time. If both inputs are high simultaneously, both outputs will immediately be set low. This feature is used to prevent shoot-through, and it doesn't affect the programmed dead time setting for normal operation. Various driver dead time logic operating conditions are illustrated and explained in:

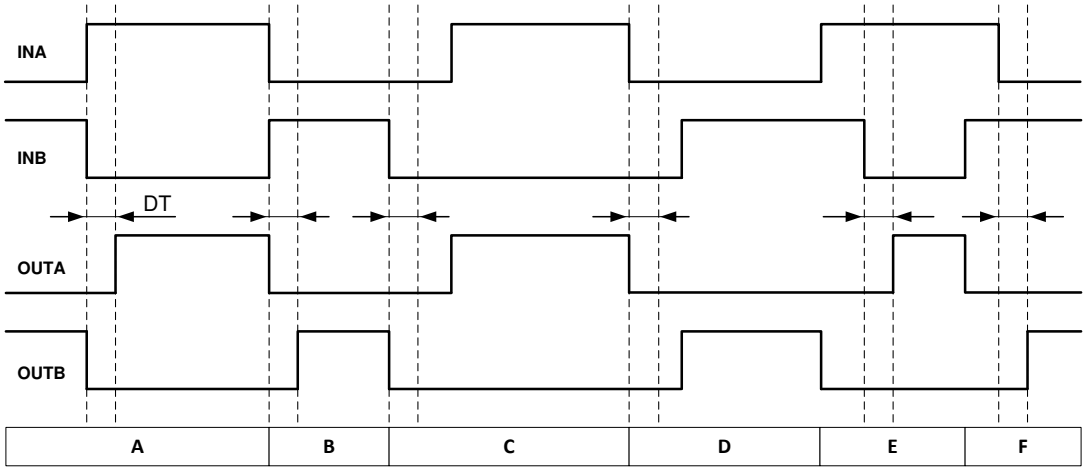


図 7-4. Input and Output Logic Relationship With Input Signals

Condition A: INB goes low, INA goes high. INB sets OUTB low immediately and assigns the programmed dead time to OUTA. OUTA is allowed to go high after the programmed dead time.

Condition B: INB goes high, INA goes low. Now INA sets OUTA low immediately and assigns the programmed dead time to OUTB. OUTB is allowed to go high after the programmed dead time.

Condition C: INB goes low, INA is still low. INB sets OUTB low immediately and assigns the programmed dead time for OUTA. In this case, the input signal's *own* dead time is longer than the programmed dead time. Thus, when INA goes high, it immediately sets OUTA high.

Condition D: INA goes low, INB is still low. INA sets OUTA low immediately and assigns the programmed dead time to OUTB. INB's *own* dead time is longer than the programmed dead time. Thus, when INB goes high, it immediately sets OUTB high.

Condition E: INA goes high, while INB and OUTB are still high. To avoid overshoot, INA immediately pulls OUTB low and keeps OUTA low. After some time OUTB goes low and assigns the programmed dead time to OUTA. OUTB is already low. After the programmed dead time, OUTA is allowed to go high.

Condition F: INB goes high, while INA and OUTA are still high. To avoid overshoot, INB immediately pulls OUTA low and keeps OUTB low. After some time OUTA goes low and assigns the programmed dead time to OUTB. OUTA is already low. After the programmed dead time, OUTB is allowed to go high.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The UCC21520-Q1 effectively combines both isolation and buffer-drive functions. The flexible, universal capability of the UCC21520-Q1 (with up to 18-V VCCI and 25-V VDDA/VDDB) allows the device to be used as a low-side, high-side, high-side/low-side or half-bridge driver for MOSFETs, IGBTs or SiC MOSFETs. With integrated components, advanced protection features (UVLO, dead time, and disable) and optimized switching performance; the UCC21520-Q1 enables designers to build smaller, more robust designs for enterprise, telecom, automotive, and industrial applications with a faster time to market.

8.2 Typical Application

The circuit in 図 8-1 shows a reference design with the UCC21520-Q1 driving a typical half-bridge configuration which could be used in several popular power converter topologies such as synchronous buck, synchronous boost, half-bridge/full bridge isolated topologies, and 3-phase motor drive applications.

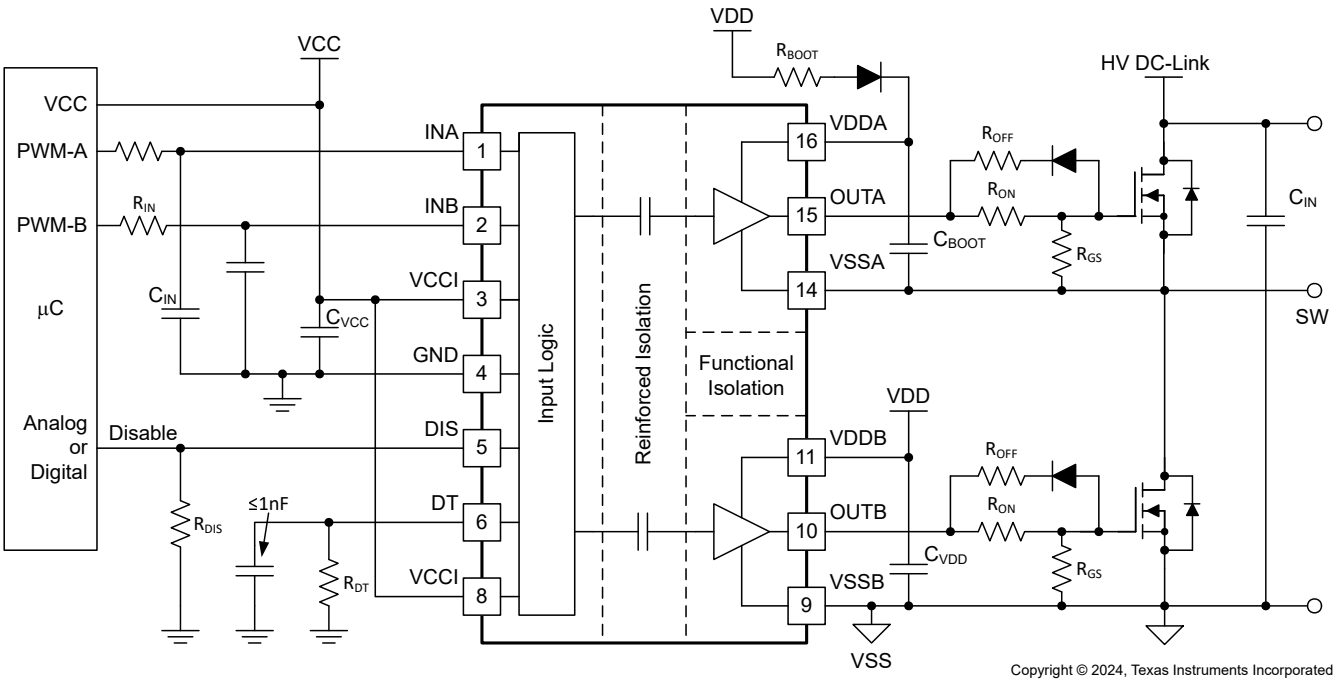


図 8-1. Typical Application Schematic

8.2.1 Design Requirements

表 8-1 lists reference design parameters for the example application: UCC21520-Q1 driving 1200-V SiC-MOSFETs in a high side-low side configuration.

表 8-1. UCC21520-Q1 Design Requirements

PARAMETER	VALUE	UNITS
Power transistor	C2M0080120D	-
VCC	5.0	V
VDD	20	V
Input signal amplitude	3.3	V
Switching frequency (f_s)	100	kHz
DC link voltage	800	V

8.2.2 Detailed Design Procedure

8.2.2.1 Designing INA/INB Input Filter

It is recommended that users avoid shaping the signals to the gate driver in an attempt to slow down (or delay) the signal at the output. However, a small input R_{IN}-C_{IN} filter can be used to filter out the ringing introduced by non-ideal layout or long PCB traces.

Such a filter should use an R_{IN} in the range of 0 Ω to100 Ω and a C_{IN} between 10 pF and 100 pF. In the example, an R_{IN} = 51 Ω and a C_{IN} = 33 pF are selected, with a corner frequency of approximately 100 MHz.

When selecting these components, it is important to pay attention to the trade-off between good noise immunity and propagation delay.

8.2.2.2 Select External Bootstrap Diode and its Series Resistor

The bootstrap capacitor is charged by VDD through an external bootstrap diode every cycle when the low side transistor turns on. Charging the capacitor involves high-peak currents, and therefore transient power dissipation in the bootstrap diode may be significant. Conduction loss also depends on the diode's forward voltage drop. Both the diode conduction losses and reverse recovery losses contribute to the total losses in the gate driver circuit.

When selecting external bootstrap diodes, it is recommended that one chose high voltage, fast recovery diodes or SiC Schottky diodes with a low forward voltage drop and low junction capacitance in order to minimize the loss introduced by reverse recovery and related grounding noise bouncing. In the example, the DC-link voltage is 800 V_{DC}. The voltage rating of the bootstrap diode should be higher than the DC-link voltage with a good margin. Therefore, a 1200-V SiC diode, C4D02120E, is chosen in this example.

When designing a bootstrap supply, it is recommended to use a bootstrap resistor, R_{BOOT}. A bootstrap resistor, is also used to reduce the inrush current in D_{BOOT} and limit the ramp up slew rate of voltage of VDDA-VSSA during each switching cycle.

Failure to limit the voltage to VDDx-VSSx to less than the Absolute Maximum Ratings of the FET and UCC21520 may result in permanent damage to the device in certain cases.

The recommended value for R_{BOOT} is between 1 Ω and 20 Ω depending on the diode used. In the example, a current limiting resistor of 2.2 Ω is selected to limit the inrush current of bootstrap diode. The estimated worst case peak current through D_{Boot} is,

$$I_{DBoot(pk)} = \frac{V_{DD} - V_{BDF}}{R_{Boot}} = \frac{20V - 2.5V}{2.2\Omega} \approx 8A \quad (2)$$

where

- V_{BDF} is the estimated bootstrap diode forward voltage drop at 8 A.

8.2.2.3 Gate Driver Output Resistor

The external gate driver resistors, R_{ON}/R_{OFF}, are used to:

1. Limit ringing caused by parasitic inductances/capacitances.
2. Limit ringing caused by high voltage/current switching dv/dt, di/dt, and body-diode reverse recovery.
3. Fine-tune gate drive strength, i.e. peak sink and source current to optimize the switching loss.
4. Reduce electromagnetic interference (EMI).

As mentioned in セクション 7.3.4, the UCC21520-Q1 has a pull-up structure with a P-channel MOSFET and an additional *pull-up* N-channel MOSFET in parallel. The combined peak source current is 4 A. Therefore, the peak source current can be predicted with:

$$I_{OA+} = \min\left(4A, \frac{V_{DD} - V_{BDF}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET\_Int}}\right) \tag{3}$$

$$I_{OB+} = \min\left(4A, \frac{V_{DD}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET\_Int}}\right) \tag{4}$$

where

- R_{ON}: External turn-on resistance.
- R_{GFET_INT}: Power transistor internal gate resistance, found in the power transistor datasheet.
- I_{O+} = Peak source current – The minimum value between 4 A, the gate driver peak source current, and the calculated value based on the gate drive loop resistance.

In this example:

$$I_{OA+} = \frac{V_{DD} - V_{BDF}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET\_Int}} = \frac{20V - 0.8V}{1.47\Omega \,||\, 5\Omega + 2.2\Omega + 4.6\Omega} \approx 2.4A \tag{5}$$

$$I_{OB+} = \frac{V_{DD}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET\_Int}} = \frac{20V}{1.47\Omega \,||\, 5\Omega + 2.2\Omega + 4.6\Omega} \approx 2.5A \tag{6}$$

Therefore, the high-side and low-side peak source current is 2.4 A and 2.5 A respectively. Similarly, the peak sink current can be calculated with:

$$I_{OA-} = \min\left(6A, \frac{V_{DD} - V_{BDF} - V_{GDF}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET\_Int}}\right) \tag{7}$$

$$I_{OB-} = \min\left(6A, \frac{V_{DD} - V_{GDF}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET\_Int}}\right) \tag{8}$$

where

- R_{OFF}: External turn-off resistance;
- V_{GDF}: The anti-parallel diode forward voltage drop which is in series with R_{OFF}. The diode in this example is an MSS1P4.
- I_{O-}: Peak sink current – the minimum value between 6 A, the gate driver peak sink current, and the calculated value based on the gate drive loop resistance.

In this example,

$$I_{OA-} = \frac{V_{DD} - V_{BDF} - V_{GDF}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET\_Int}} = \frac{20V - 0.8V - 0.75V}{0.55\Omega + 0\Omega + 4.6\Omega} \approx 3.6A \quad (9)$$

$$I_{OB-=} \frac{V_{DD} - V_{GDF}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET\_Int}} = \frac{20V\text{-}0.75V}{0.55\Omega + 0\Omega + 4.6\Omega} \approx 3.7A \quad (10)$$

Therefore, the high-side and low-side peak sink current is 3.6 A and 3.7 A respectively.

Importantly, the estimated peak current is also influenced by PCB layout and load capacitance. Parasitic inductance in the gate driver loop can slow down the peak gate drive current and introduce overshoot and undershoot. Therefore, it is strongly recommended that the gate driver loop should be minimized. On the other hand, the peak source/sink current is dominated by loop parasitics when the load capacitance (C_{ISS}) of the power transistor is very small (typically less than 1 nF), because the rising and falling time is too small and close to the parasitic ringing period.

Failure to control OUTx voltage to less than the Absolute Maximum Ratings in the datasheet (including transients) may result in permanent damage to the device in certain cases. To reduce excessive gate ringing, it is recommended to use a ferrite bead near the gate of the FET. External clamping diodes can also be added in the case of extended overshoot/undershoot, in order to clamp the OUTx voltage to the VDDx and VSSx voltages.

8.2.2.4 Gate to Source Resistor Selection

A gate to source resistor, R_{GS}, is recommended to pull down the gate to the source voltage when the gate driver output is unpowered and in an indeterminate state. This resistor also helps to mitigate the risk of dv/dt induced turn-on due to Miller current before the gate driver is able to turn on and actively pull low. This resistor is typically sized between 5.1kΩ and 20kΩ, depending on the Vth and ratio of C_{GD} to C_{GS} of the power device.

8.2.2.5 Estimate Gate Driver Power Loss

The total loss, P_G, in the gate driver subsystem includes the power losses of the UCC21520-Q1 (P_{GD}) and the power losses in the peripheral circuitry, such as the external gate drive resistor. Bootstrap diode loss is not included in P_G and not discussed in this section.

P_{GD} is the key power loss which determines the thermal safety-related limits of the UCC21520-Q1, and it can be estimated by calculating losses from several components.

The first component is the static power loss, P_{GDQ}, which includes quiescent power loss on the driver as well as driver self-power consumption when operating with a certain switching frequency. P_{GDQ} is measured on the bench with no load connected to OUTA and OUTB at a given VCCI, VDDA/VDDB, switching frequency and ambient temperature. 図 5-4 shows the per output channel current consumption vs operating frequency with no load. In this example, V_{VCCI} = 5 V and V_{VDD} = 20 V. The current on each power supply, with INA/INB switching from 0 V to 3.3 V at 100 kHz is measured to be I_{VCCI} = 2.5 mA, and I_{VDDA} = I_{VDDB} = 1.5 mA. Therefore, the P_{GDQ} can be calculated with

$$P_{GDQ} = V_{VCCI} \times I_{VCCI} + V_{VDDA} \times I_{DDA} + V_{VDDB} \times I_{DDB} \approx 72mW \quad (11)$$

The second component is switching operation loss, P_{GDO}, with a given load capacitance which the driver charges and discharges the load during each switching cycle. Total dynamic loss due to load switching, P_{GSW}, can be estimated with

$$P_{GSW} = 2 \times V_{DD} \times Q_G \times f_{SW} \quad (12)$$

where

- Q_G is the gate charge of the power transistor.

If a split rail is used to turn on and turn off, then VDD is going to be equal to difference between the positive rail to the negative rail.

So, for this example application:

$$P_{GSW} = 2 \times 20V \times 60nC \times 100kHz = 240mW \tag{13}$$

Q_G represents the total gate charge of the power transistor switching 800 V at 20 A, and is subject to change with different testing conditions. The UCC21520-Q1 gate driver loss on the output stage, P_{GDO}, is part of P_{GSW}. P_{GDO} will be equal to P_{GSW} if the external gate driver resistances are zero, and all the gate driver loss is dissipated inside the UCC21520-Q1. If there are external turn-on and turn-off resistances, the total loss will be distributed between the gate driver pull-up/down resistances and external gate resistances. Importantly, the pull-up/down resistance is a linear and fixed resistance if the source/sink current is not saturated to 4 A/6 A, however, it will be non-linear if the source/sink current is saturated. Therefore, P_{GDO} is different in these two scenarios.

Case 1 - Linear Pull-Up/Down Resistor:

$$P_{GDO} = \frac{P_{GSW}}{2} \times \left(\frac{R_{OH} \,||\, R_{NMOS}}{R_{OH} \,||\, R_{NMOS} + R_{ON} + R_{GFET\_Int}} + \frac{R_{OL}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET\_Int}} \right) \tag{14}$$

In this design example, all the predicted source/sink currents are less than 4 A/6 A, therefore, the UCC21520-Q1 gate driver loss can be estimated with:

$$P_{GDO} = \frac{240mW}{2} \times \left(\frac{5\Omega \,||\, 1.47\Omega}{5\Omega \,||\, 1.47\Omega + 2.2\Omega + 4.6\Omega} + \frac{0.55\Omega}{0.55\Omega + 0\Omega + 4.6\Omega} \right) \approx 30mW \tag{15}$$

Case 2 - Nonlinear Pull-Up/Down Resistor:

$$P_{GDO} = 2 \times f_{SW} \times \left[4A \times \int_0^{T_{R\_Sys}} \left(V_{DD} - V_{OUTA/B}(t) \right) dt + 6A \times \int_0^{T_{F\_Sys}} V_{OUTA/B}(t)\, dt \right] \tag{16}$$

where

- $V_{OUTA/B}(t)$ is the gate driver OUTA and OUTB pin voltage during the turn on and off transient, and it can be simplified that a constant current source (4 A at turn-on and 6 A at turn-off) is charging/discharging a load capacitor. Then, the $V_{OUTA/B}(t)$ waveform will be linear and the T_{R_Sys} and T_{F_Sys} can be easily predicted.

For some scenarios, if only one of the pull-up or pull-down circuits is saturated and another one is not, the P_{GDO} will be a combination of Case 1 and Case 2, and the equations can be easily identified for the pull-up and pull-down based on the above discussion. Therefore, total gate driver loss dissipated in the gate driver UCC21520-Q1, P_{GD}, is:

$$P_{GD} = P_{GDQ} + P_{GDO} \tag{17}$$

which is equal to 102 mW in the design example.

8.2.2.6 Estimating Junction Temperature

The junction temperature (T_J) of the UCC21520-Q1 can be estimated with:

$$T_J = T_C + \Psi_{JT} \times P_{GD} \tag{18}$$

where

- T_C is the UCC21520-Q1 case-top temperature measured with a thermocouple or some other instrument, and
- Ψ_{JT} is the Junction-to-top characterization parameter from the Thermal Information table.

Using the junction-to-top characterization parameter (Ψ_{JT}) instead of the junction-to-case thermal resistance ($R_{\Theta JC}$) can greatly improve the accuracy of the junction temperature estimation. The majority of the thermal energy of most ICs is released into the PCB through the package leads, whereas only a small percentage of the total energy is released through the top of the case (where thermocouple measurements are usually conducted). $R_{\Theta JC}$ can only be used effectively when most of the thermal energy is released through the case, such as with metal packages or when a heatsink is applied to an IC package. In all other cases, use of $R_{\Theta JC}$ will inaccurately estimate the true junction temperature. Ψ_{JT} is experimentally derived by assuming that the amount of energy leaving through the top of the IC will be similar in both the testing environment and the application environment. As long as the recommended layout guidelines are observed, junction temperature estimates can be made accurately to within a few degrees Celsius. For more information, see the *Semiconductor and IC Package Thermal Metrics Application Report*.

8.2.2.7 Selecting VCCI, VDDA/B Capacitor

Bypass capacitors for VCCI, VDDA, and VDDB are essential for achieving reliable performance. It is recommended that one choose low ESR and low ESL surface-mount multi-layer ceramic capacitors (MLCC) with sufficient voltage ratings, temperature coefficients and capacitance tolerances. Importantly, DC bias on an MLCC will impact the actual capacitance value. For example, a 25-V, 1-µF X7R capacitor is measured to be only 500 nF when a DC bias of 15 V_{DC} is applied.

8.2.2.7.1 Selecting a VCCI Capacitor

A bypass capacitor connected to VCCI supports the transient current needed for the primary logic and the total current consumption, which is only a few mA. Therefore, a 50-V MLCC with over 100 nF is recommended for this application. If the bias power supply output is a relatively long distance from the VCCI pin, a tantalum or electrolytic capacitor, with a value over 1 µF, should be placed in parallel with the MLCC.

8.2.2.7.2 Selecting a VDDA (Bootstrap) Capacitor

A VDDA capacitor, also referred to as a *bootstrap capacitor* in bootstrap power supply configurations, allows for gate drive current transients up to 6 A, and needs to maintain a stable gate drive voltage for the power transistor.

The total charge needed per switching cycle can be estimated with

$$Q_{Total} = Q_G + \frac{I_{VDD}@100kHz(\text{No Load})}{f_{SW}} = 60nC + \frac{1.5mA}{100kHz} = 75nC \quad (19)$$

where

- Q_{Total}: Total charge needed
- Q_G: Gate charge of the power transistor.
- I_{VDD}: The channel self-current consumption with no load at 100kHz.
- f_{SW}: The switching frequency of the gate driver

Therefore, the absolute minimum C_{Boot} requirement is:

$$C_{Boot} = \frac{Q_{Total}}{\Delta V_{VDDA}} = \frac{75nC}{0.5V} = 150nF \quad (20)$$

where

- ΔV_{VDDA} is the voltage ripple at VDDA, which is 0.5 V in this example.

In practice, the value of C_{Boot} is greater than the calculated value. This allows for the capacitance shift caused by the DC bias voltage and for situations where the power stage would otherwise skip pulses due to load transients. Therefore, it is recommended to include a safety-related margin in the C_{Boot} value and place it as close to the VDD and VSS pins as possible. A 50-V 1-µF capacitor is chosen in this example.

$$C_{Boot} = 1\mu F \tag{21}$$

Care should be taken when selecting the bootstrap capacitor to ensure that the VDD to VSS voltage does not drop below the recommended minimum operating level listed in section 6.3. The value of the bootstrap capacitor should be sized such that it can supply the initial charge to switch the power device, and then continuously supply the gate driver quiescent current for the duration of the high-side on-time.

If the high-side supply voltage drops below the UVLO falling threshold, the high-side gate driver output will turn off and switch the power device off. Uncontrolled hard-switching of power devices can cause high di/dt and high dv/dt transients on the output of the driver and may result in permanent damage to the device.

To further lower the AC impedance for a wide frequency range, it is recommended to have bypass capacitor placed very close to VDDx - VSSx pins with a low ESL/ESR. In this example a 100 nF, X7R ceramic capacitor, is placed in parallel with C_{Boot} to optimize the transient performance.

注

Too large C_{BOOT} is not good. C_{BOOT} may not be charged within the first few cycles and V_{BOOT} could stay below UVLO. As a result, the high-side FET does not follow input signal command. Also during initial C_{BOOT} charging cycles, the bootstrap diode has highest reverse recovery current and losses.

8.2.2.7.3 Select a VDDB Capacitor

Chanel B has the same current requirements as Channel A, Therefore, a VDDB capacitor (Shown as C_{VDD} in 図 8-1) is needed. In this example with a bootstrap configuration, the VDDB capacitor will also supply current for VDDA through the bootstrap diode. A 50-V, 10-µF MLCC and a 50-V, 220-nF MLCC are chosen for C_{VDD}. If the bias power supply output is a relatively long distance from the VDDB pin, a tantalum or electrolytic capacitor, with a value over 10 µF, should be used in parallel with CVDD.

8.2.2.8 Dead Time Setting Guidelines

For power converter topologies utilizing half-bridges, the dead time setting between the top and bottom transistor is important for preventing shoot-through during dynamic switching.

The UCC21520-Q1 dead time specification in the electrical table is defined as the time interval from 90% of one channel's falling edge to 10% of the other channel's rising edge (see 図 6-4). This definition ensures that the dead time setting is independent of the load condition, and guarantees linearity through manufacture testing. However, this dead time setting may not reflect the dead time in the power converter system, since the dead time setting is dependent on the external gate drive turn-on/off resistor, DC-Link switching voltage/current, as well as the input capacitance of the load transistor.

Here is a suggestion on how to select an appropriate dead time for UCC21520-Q1:

$$DT_{Setting} = DT_{Req} + T_{F\_Sys} + T_{R\_Sys} - T_{D(on)} \tag{22}$$

where

- $DT_{setting}$: UCC21520-Q1 dead time setting in ns, $DT_{Setting}$ = 10 × RDT(in kΩ).
- DT_{Req}: System required dead time between the real V_{GS} signal of the top and bottom switch with enough margin, or ZVS requirement.
- T_{F_Sys}: In-system gate turn-off falling time at worst case of load, voltage/current conditions.
- T_{R_Sys}: In-system gate turn-on rising time at worst case of load, voltage/current conditions.
- $T_{D(on)}$: Turn-on delay time, from 10% of the transistor gate signal to power transistor gate threshold.

In the example, $DT_{Setting}$ is set to 250 ns.

It should be noted that the UCC21520-Q1 dead time setting is decided by the DT pin configuration (see セクション 7.4.2), and it cannot automatically fine-tune the dead time based on system conditions. It is recommended to parallel a ceramic capacitor, <1nF, close to the DT pin with R_{DT} to achieve better noise immunity.

8.2.2.9 Application Circuits with Output Stage Negative Bias

When parasitic inductances are introduced by non-ideal PCB layout and long package leads (for example, TO-220 and TO-247 type packages), there could be ringing in the gate-source drive voltage of the power transistor during high di/dt and dv/dt switching. If the ringing is over the threshold voltage, there is the risk of unintended turn-on and even shoot-through. Applying a negative bias on the gate drive is a popular way to keep such ringing below the threshold. Below are a few examples of implementing negative gate drive bias.

図 8-2 shows the first example with negative bias turn-off on the channel-A driver using a Zener diode on the isolated power supply output stage. The negative bias is set by the Zener diode voltage. If the isolated power supply, V_A, is equal to 25 V, the turn-off voltage will be –5.1 V and turn-on voltage will be 25 V – 5.1 V ≈ 20 V. The channel-B driver circuit is the same as channel-A, therefore, this configuration needs two power supplies for a half-bridge configuration, and there will be steady state power consumption from R_Z.

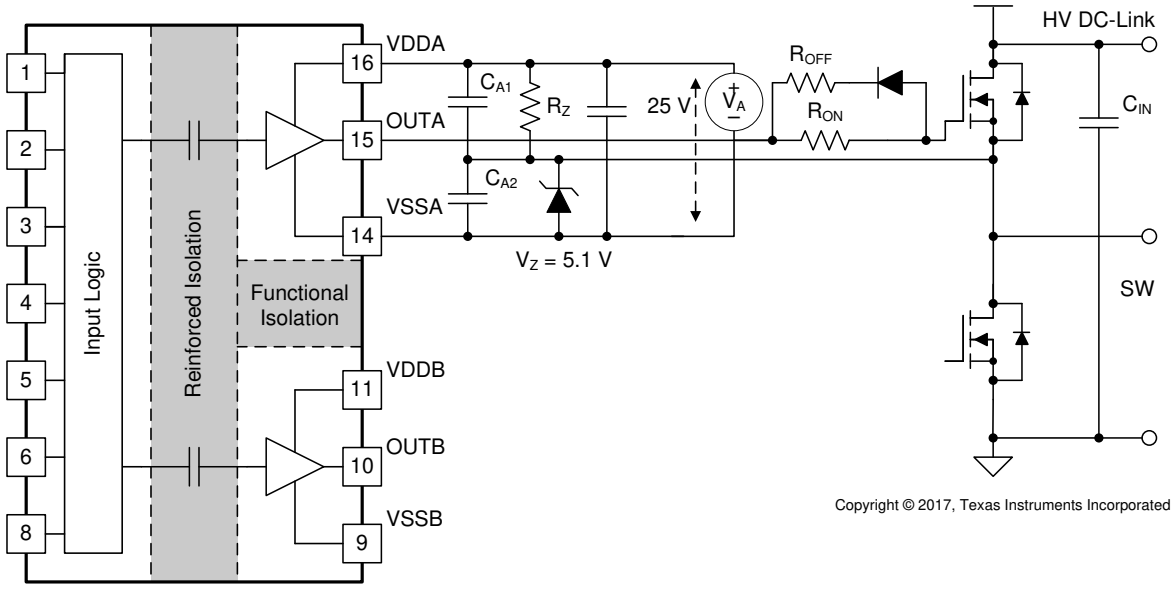


図 8-2. Negative Bias with Zener Diode on Iso-Bias Power Supply Output

図 8-3 shows another example which uses two supplies (or single-input-double-output power supply). Power supply V_{A+} determines the positive drive output voltage and $V_{A–}$ determines the negative turn-off voltage. The configuration for channel B is the same as channel A. This solution requires more power supplies than the first example, however, it provides more flexibility when setting the positive and negative rail voltages.

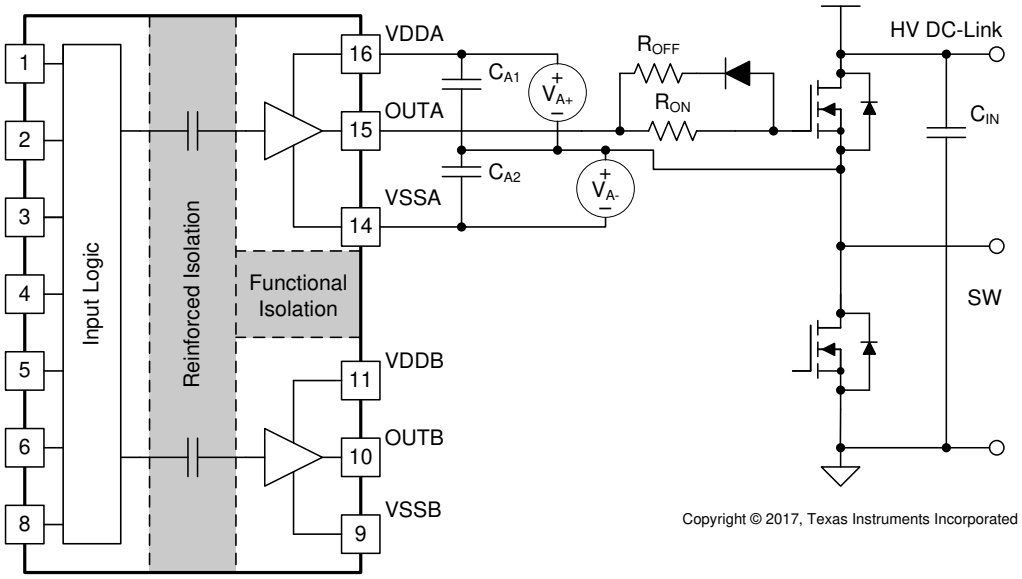


図 8-3. Negative Bias with Two Iso-Bias Power Supplies

The last example, shown in 図 8-4, is a single power supply configuration and generates negative bias through a Zener diode in the gate drive loop. The benefit of this solution is that it only uses one power supply and the bootstrap power supply can be used for the high side drive. This design requires the least cost and design effort among the three solutions. However, this solution has limitations:

1. The negative gate drive bias is not only determined by the Zener diode, but also by the duty cycle, which means the negative bias voltage will change when the duty cycle changes. Therefore, converters with a fixed duty cycle (~50%) such as variable frequency resonant convertors or phase shift convertors favor this solution.
2. The high side VDDA-VSSA must maintain enough voltage to stay in the recommended power supply range, which means the low side switch must turn-on or have free-wheeling current on the body (or anti-parallel) diode for a certain period during each switching cycle to refresh the bootstrap capacitor. Therefore, a 100% duty cycle for the high side is not possible unless there is a dedicated power supply for the high side, like in the other two example circuits.

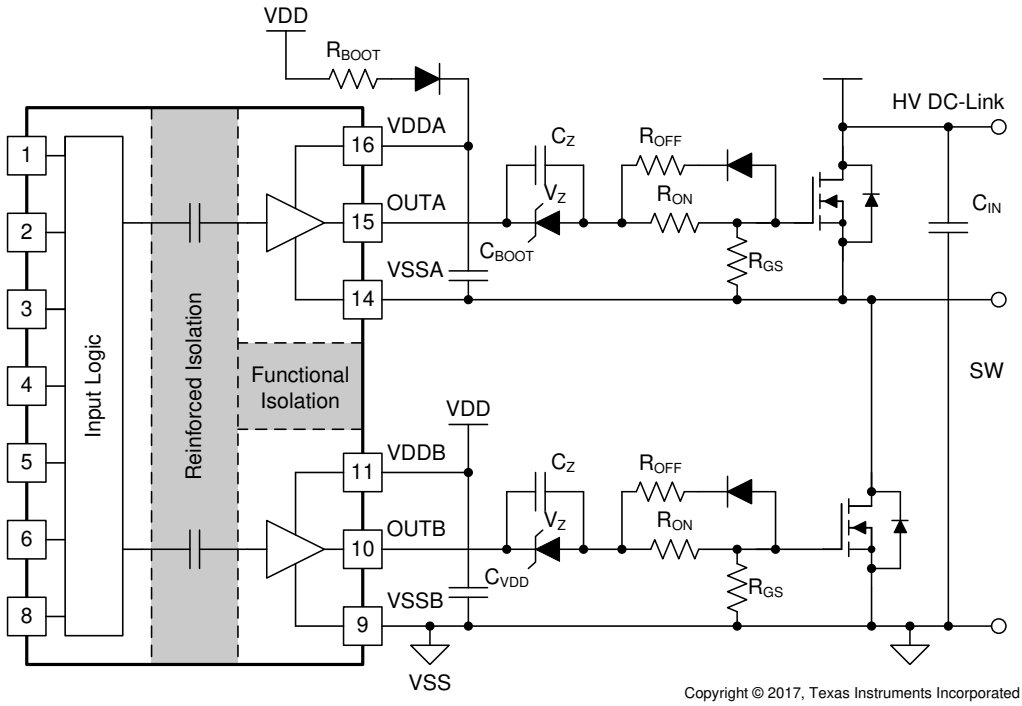


図 8-4. Negative Bias with Single Power Supply and Zener Diode in Gate Drive Path

8.2.3 Application Curves

図 8-5 and 図 8-6 shows the bench test waveforms for the design example shown in 図 8-1 under these conditions: VCC = 5 V, VDD = 20 V, f_{SW} = 100 kHz, $V_{DC\text{-}Link}$ = 0 V.

Channel 1 (Yellow): UCC21520-Q1 INA pin signal.

Channel 2 (Blue): UCC21520-Q1 INB pin signal.

Channel 3 (Pink): Gate-source signal on the high side power transistor.

Channel 4 (Green): Gate-source signal on the low side power transistor.

In 図 8-5, INA and INB are sent complimentary 3.3-V, 50% duty-cycle signals. The gate drive signals on the power transistor have a 250-ns dead time, shown in the measurement section of 図 8-5. The dead-time matching is less than 1 ns with the 250-ns dead-time setting.

図 8-6 shows a zoomed-in version of the waveform of 図 8-5, with measurements for propagation delay and rising/falling time. Cursors are also used to measure dead time. Importantly, the output waveform is measured between the power transistors' gate and source pins, and is not measured directly from the driver OUTA and OUTB pins. Due to the split on and off resistors (R_{on},R_{off}) and different sink and source currents, different rising (16 ns) and falling time (9 ns) are observed in 図 8-6.

図 8-5. Bench Test Waveform for INA/B and OUTA/B

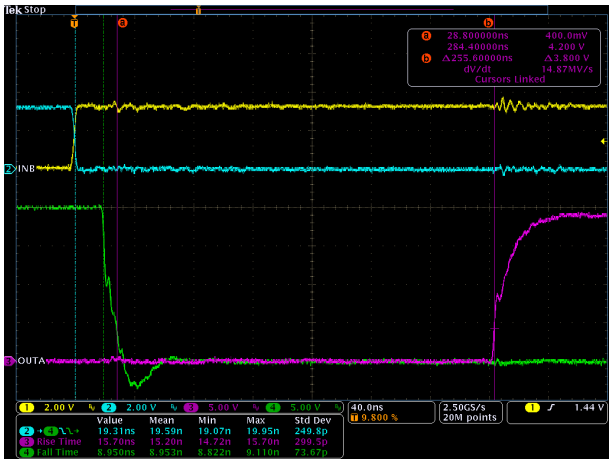


図 8-6. Zoomed-In Bench Test Waveform

9 Power Supply Recommendations

The recommended input supply voltage (VCCI) for the UCC21520-Q1 is between 3 V and 18 V. The output bias supply voltage (VDDA/VDDB) range depends on which version of UCC21520-Q1 one is using. The lower end of this bias supply range is governed by the internal under voltage lockout (UVLO) protection feature of each device. One mustn't let VDD or VCCI fall below their respective UVLO thresholds (For more information on UVLO see セクション 7.3.1). The upper end of the VDDA/VDDB range depends on the maximum gate voltage of the power device being driven by the UCC21520-Q1. The UCC21520-Q1 have a recommended maximum VDDA/VDDB of 25 V.

A local bypass capacitor should be placed between the VDD and VSS pins. This capacitor should be positioned as close to the device as possible. A low ESR, ceramic surface mount capacitor is recommended. It is further suggested that one place two such capacitors: one with a value of ≈10-µF for device biasing, and an additional ≤100-nF capacitor in parallel for high frequency filtering.

Similarly, a bypass capacitor should also be placed between the VCCI and GND pins. Given the small amount of current drawn by the logic circuitry within the input side of the UCC21520-Q1, this bypass capacitor has a minimum recommended value of 100 nF.

10 Layout

10.1 Layout Guidelines

One must pay close attention to PCB layout in order to achieve optimum performance for the UCC21520-Q1. Below are some key points.

Component Placement:

- Low-ESR and low-ESL capacitors must be connected close to the device between the VCCI and GND pins and between the VDD and VSS pins to support high peak currents when turning on the external power transistor.
- To avoid large negative transients on the switch node VSSA (HS) pin, the parasitic inductances between the source of the top transistor and the source of the bottom transistor must be minimized.
- It is recommended to place the dead-time setting resistor, R_{DT}, and its bypassing capacitor close to DT pin of the UCC21520-Q1.
- It is recommended to bypass using a ≈1nF low ESR/ESL capacitor, C_{DIS}, close to DIS pin when connecting to a µC with distance.

Grounding Considerations:

- It is essential to confine the high peak currents that charge and discharge the transistor gates to a minimal physical area. This will decrease the loop inductance and minimize noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.
- Pay attention to high current path that includes the bootstrap capacitor, bootstrap diode, local VSSB-referenced bypass capacitor, and the low-side transistor body/anti-parallel diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode by the VDD bypass capacitor. This recharging occurs in a short time interval and involves a high peak current. Minimizing this loop length and area on the circuit board is important for ensuring reliable operation.

High-Voltage Considerations:

- To ensure isolation performance between the primary and secondary side, one should avoid placing any PCB traces or copper below the driver device. A PCB cutout is recommended in order to prevent contamination that may compromise the UCC21520-Q1's isolation performance.
- For half-bridge, or high-side/low-side configurations, where the channel A and channel B drivers could operate with a DC-link voltage up to 1500 V_{DC}, one should try to increase the creepage distance of the PCB layout between the high and low-side PCB traces.

Thermal Considerations:

- A large amount of power may be dissipated by the UCC21520-Q1 if the driving voltage is high, the load is heavy, or the switching frequency is high (refer to セクション 8.2.2.5 for more details). Proper PCB layout can help dissipate heat from the device to the PCB and minimize junction to board thermal impedance (θ_{JB}).
- Increasing the PCB copper connecting to VDDA, VDDB, VSSA and VSSB pins is recommended, with priority on maximizing the connection to VSSA and VSSB (see 図 10-2 and 図 10-3). However, high voltage PCB considerations mentioned above must be maintained.
- If there are multiple layers in the system, it is also recommended to connect the VDDA, VDDB, VSSA and VSSB pins to internal ground or power planes through multiple vias of adequate size. However, keep in mind that there shouldn't be any traces/coppers from different high voltage planes overlapping.

10.2 Layout Example

図 10-1 shows a 2-layer PCB layout example with the signals and key components labeled.

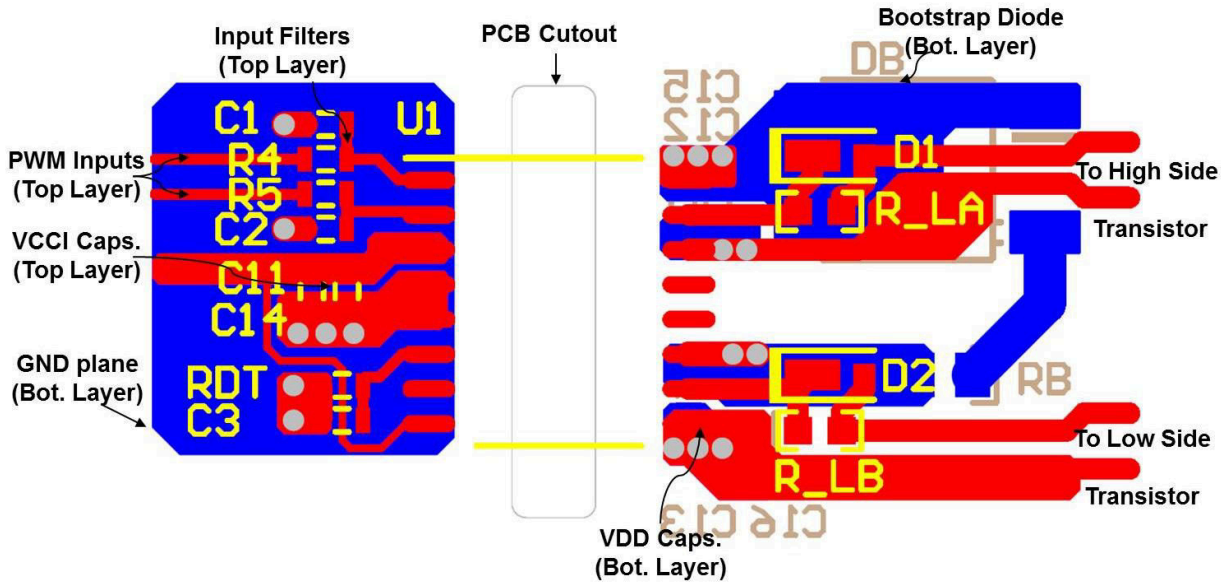


図 10-1. Layout Example

図 10-2 and 図 10-3 shows top and bottom layer traces and copper.

注

There are no PCB traces or copper between the primary and secondary side, which ensures isolation performance.

PCB traces between the high-side and low-side gate drivers in the output stage are increased to maximize the creepage distance for high-voltage operation, which will also minimize cross-talk between the switching node VSSA (SW), where high dv/dt may exist, and the low-side gate drive due to the parasitic capacitance coupling.

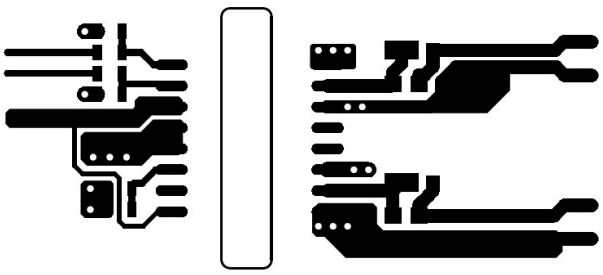


図 10-2. Top Layer Traces and Copper

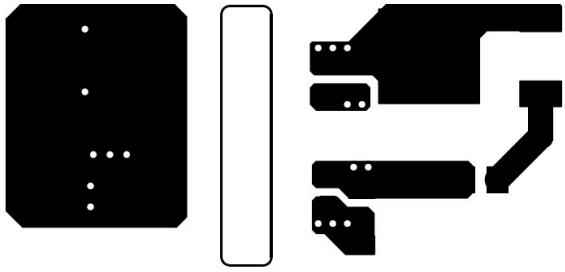


図 10-3. Bottom Layer Traces and Copper

図 10-4 and 図 10-5 are 3D layout pictures with top view and bottom views.

注

The location of the PCB cutout between the primary side and secondary sides, which ensures isolation performance.

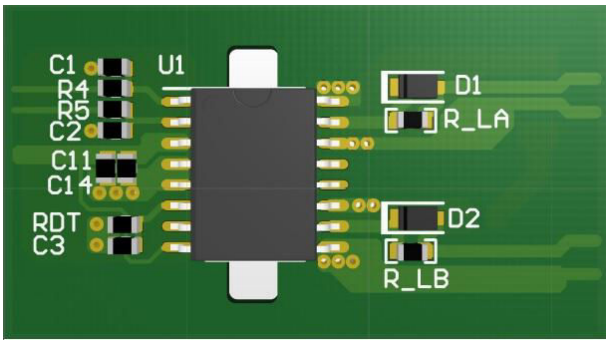


図 10-4. 3-D PCB Top View

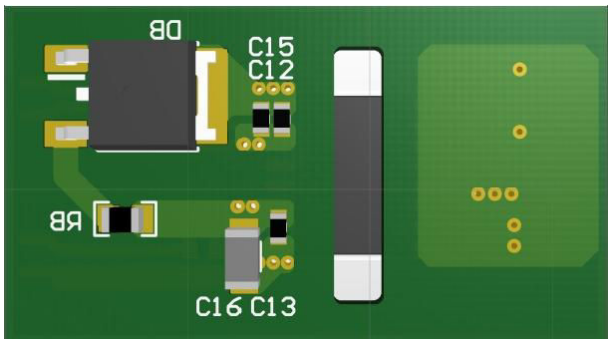


図 10-5. 3-D PCB Bottom View

11 Device and Documentation Support

11.1 サード・パーティ製品に関する免責事項

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11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *Semiconductor and IC Package Thermal Metrics Application Report*
- Isolation Glossary

11.3 Certifications

UL Online Certifications Directory, *"FPPT2.E181974 Nonoptical Isolating Devices - Component"* Certificate Number: 20160516-E181974,

VDE Pruf- und Zertifizierungsinstitut Certification, Certificate of Conformity with Factory Surveillance

CQC Online Certifications Directory, "GB4943.1-2011, Digital Isolator Certificate" Certificate Number:CQC16001155011

CSA Online Certifications Directory, "CSA Certificate of Compliance" Certificate Number:70097761, Master Contract Number:220991

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11.8 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

12 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (June 2020) to Revision E (June 2024) **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新 1
- 「特長」セクションから 5ns の最大遅延マッチングを削除 1
- 伝搬遅延の標準値を 19ns から 33ns に変更 1
- 10ns の最小パルス幅を 20ns に変更 1
- 動作温度範囲を接合部温度範囲に変更 1
- CMTI 仕様を 100V/ns から 125V/ns に変更 1
- サージ耐性の値を 12.8kV から 10kV に変更 1
- 「5ns 未満の入力パルスとノイズ過渡を除去」を削除 1
- 「特長」の HBM および CDM ESD 分類レベルを削除 1
- 安全認証を最新の規格に更新 1
- 新しい仕様値に合わせて「概要」セクションを更新 1
- Updated DT pin description to recommend ≤1nF capacitor on DT pin 2
- Changed DT pin Min resistor recommendations from 500Ω to 2kΩ 2
- Updated ESD spec from HBM = ±4000 and CDM = ±1500 to HBM = ±2000 and CDM = ±1000 to match ESD industry standards 3
- Deleted ambient temperature spec 4
- Changed Max junction temp to 150C 4
- Updated values from RθJA = 67.3°C/W, RθJC(top) = 34.4°C/W, RθJB = 32.1°C/W, ψJT = 18°C/W, ψJB = 31.6°C/W to RθJA = 69.8°C/W, RθJC(top) = 33.1°C/W, RθJB = 36.9°C/W, ψJT = 22.2°C/W, ψJB = 36°C/W 4
- Updated values from PD = 1.05W, PDI = 0.05W, PDA/PDB = 0.5W to PD = 950mW, PDI = 50mW, PDA/PDB = 450mW 4
- Updated values from DTI = >21mm, VIOSM = 8000VPK to DTI = >17mm, VIOSM = 10000VPK and added VIMP = 7692VPK 5
- Deleted safety related certifications section 5
- Updated values from IS = 75mA/36mA, PS = 50mW/900mW/900mW/1850mW to IS = 58mA/34mA, PS = 50mW/870mW/870mW/1790mW 6
- Updated IVDDA/IVDDB quiescent current spec Max value from 1.8mA to 2.5mA 6
- Updated IVCCI operating current Typ value from 2.0mA to 3.0mA and added Max value 3.5mA 6
- Added IVDDA/IVDDB operating current Max = 4.2mA 6
- Updated values from Rising threshold Min = 8.3V, Typ = 8.7V, Max = 9.2V to Min = 7.7V, Typ = 8.5V, Max = 8.9V 6
- Updated values from Falling threshold Min = 7.8V, Typ = 8.2V, Max = 8.7V to Min = 7.2V, Typ = 7.9V, Max = 8.4V 6
- Updated 8-V UVLO hysteresis typ = 0.5V to 0.6V 6
- Updated Input high threshold Min value from 1.6V to 1.2V 6
- Deadtime parameter broken to a its own table and added more parameters 7
- Changed propagation delay TPDHL and TPDLH from Typ = 19ns, Max = 30ns to Typ = 33ns, Max = 45ns and adding Min = 26ns 7
- Changed propagation delay matching from Max = 5ns to Max = 6.5ns from TJ = -40C to -10C and Max = 5ns from TJ = -10C to 150C 7
- Added VCCI power up delay 7
- Updated VDDA/VDDB power-up delay from Max = 100us to 10us 7
- Updated CMTI from Min = 100V/ns to 125V/ns 7
- Updated insulation curves to match updated characteristics 8
- Updated typical characteristics figures 9
- Updated Power-up UVLO Delay to OUTPUT section to match device electrical characteristics 14

- Changed the Functional Block Diagram to add deglitch filter block ... 16
- Added paragraph on minimum pulse width to Output Stage section ... 20
- Updated DT Pin Connected to a Programming Resistor Between DT and GND Pins section to recommend <1nF capacitor on DT pin. ... 22
- Updated typical schematic DT pin capacitor recommendation ... 24
- Updated Dead Time Setting Guidelines section to recommend <1nF capacitor on DT pin. ... 31

Changes from Revision C (March 2020) to Revision D (June 2020) **Page**

- 「特長」の一覧に「機能安全品質管理」を追加 ... 1

Changes from Revision B (July 2018) to Revision C (March 2020) **Page**

- Changed DT pin description ... 2
- Changed DT pin configuration recommendations ... 22
- Added update to bootstrap circuit recommendations ... 25
- Added update to gate resistor selection recommendations ... 26
- Added gate to source resistor recommendation ... 27
- Added update to Cboot selection recommendations ... 29

Changes from Revision A (May 2018) to Revision B (July 2018) **Page**

- UCC21520A-Q1 事前情報のマーケティング ステータスを初期リリースに変更 ... 1
- Added detailed description for DISABLE Pin and DT Pin ... 2
- Added feature descriptions for UVLO delay to OUTPUT ... 14
- Added bullet "It is recommended..." bullet to the component placement in the Layout Guidelines. ... 37

Changes from Revision * (October 2017) to Revision A (May 2018) **Page**

- このデータシートに UCC21520A-Q1 デバイス (5V UVLO オプション) を追加 ... 1
- UCC21520A-Q1 事前情報を追加 ... 1
- Added typical curves of 5-V UVLO hysteresis and ON-OFF thresholds ... 9

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC21520AQDWQ1	LIFEBUY	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCC21520AQ	
UCC21520AQDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCC21520AQ	Samples
UCC21520QDWQ1	LIFEBUY	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCC21520Q	
UCC21520QDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCC21520Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UCC21520-Q1 :

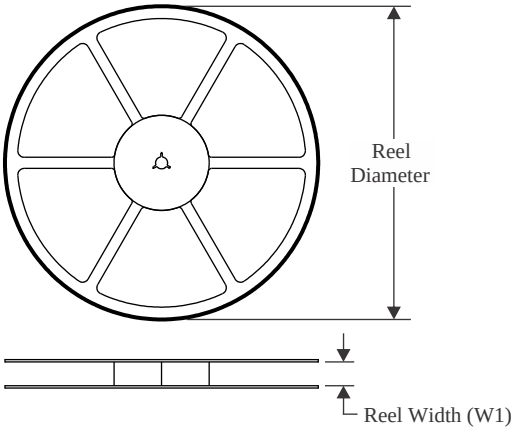
- Catalog : UCC21520

NOTE: Qualified Version Definitions:

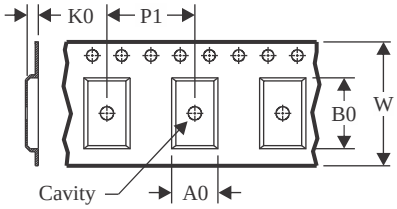
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

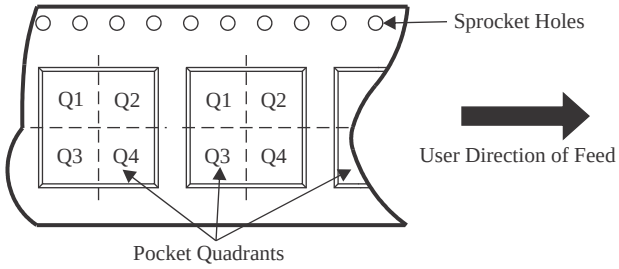


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

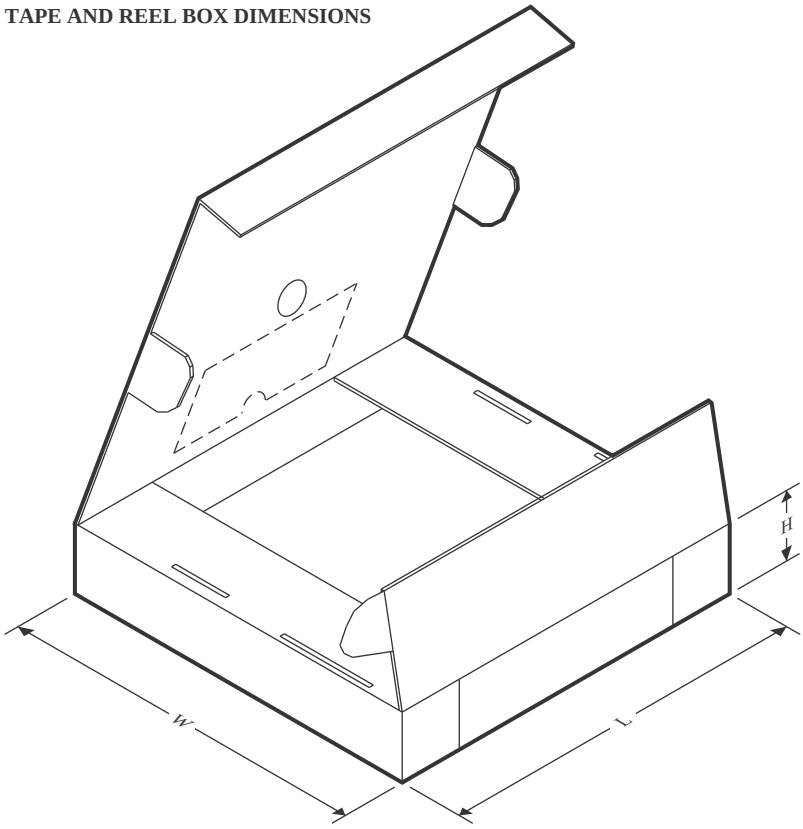
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC21520AQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
UCC21520QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
UCC21520QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

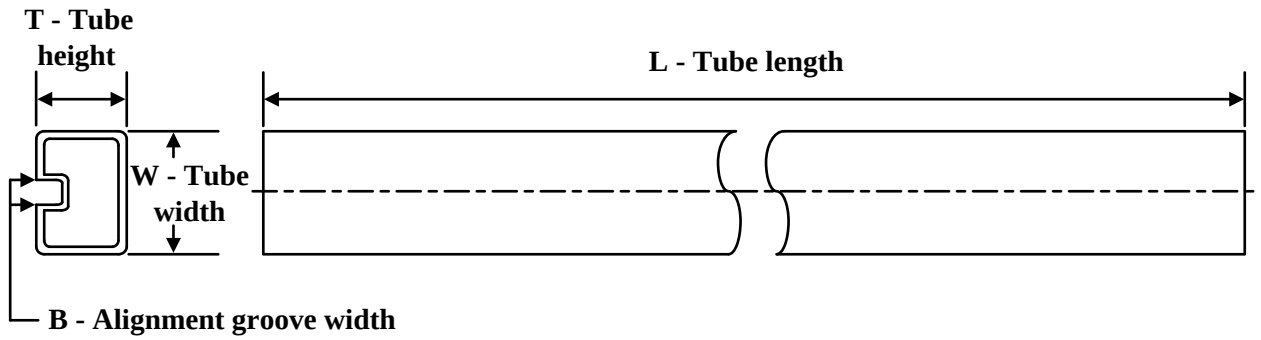
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC21520AQDWRQ1	SOIC	DW	16	2000	356.0	356.0	35.0
UCC21520QDWRQ1	SOIC	DW	16	2000	356.0	356.0	35.0
UCC21520QDWRQ1	SOIC	DW	16	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC21520AQDWQ1	DW	SOIC	16	40	506.98	12.7	4826	6.6
UCC21520AQDWQ1	DW	SOIC	16	40	507	12.83	5080	6.6
UCC21520QDWQ1	DW	SOIC	16	40	507	12.83	5080	6.6
UCC21520QDWQ1	DW	SOIC	16	40	506.98	12.7	4826	6.6

GENERIC PACKAGE VIEW

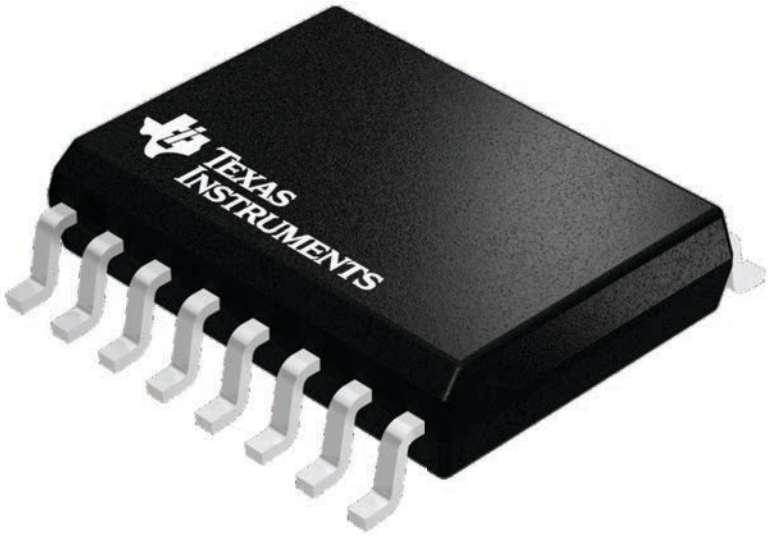
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

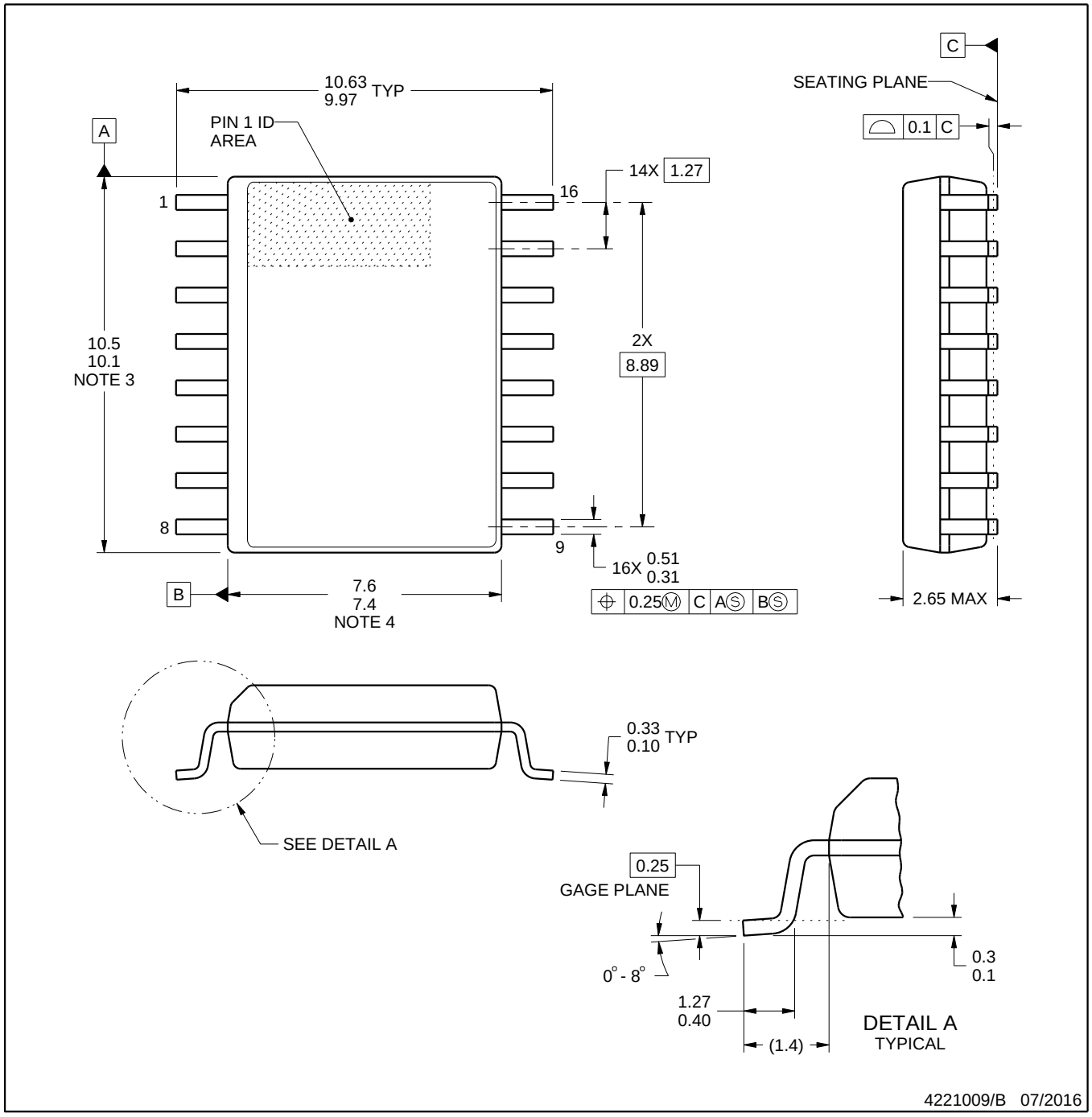
SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



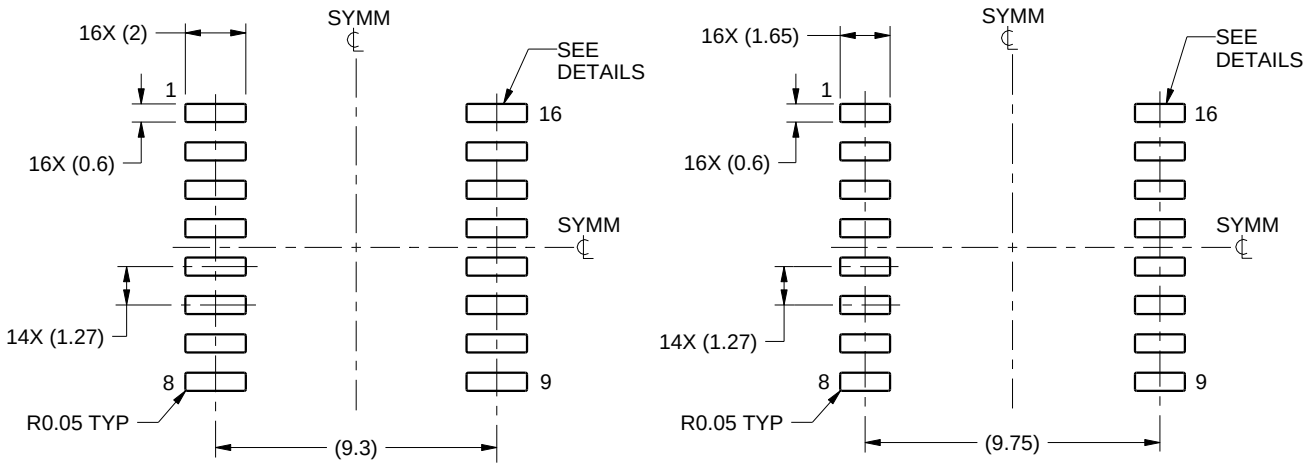
4224780/A

SOIC



NOTES:

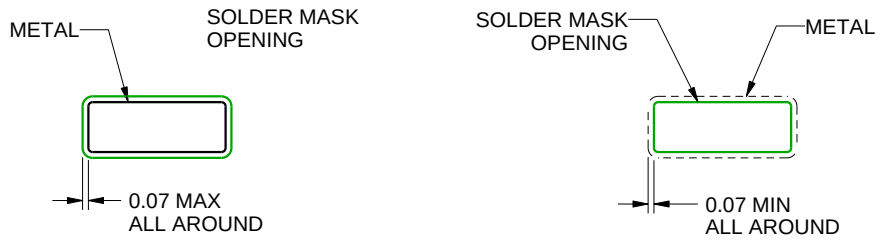
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

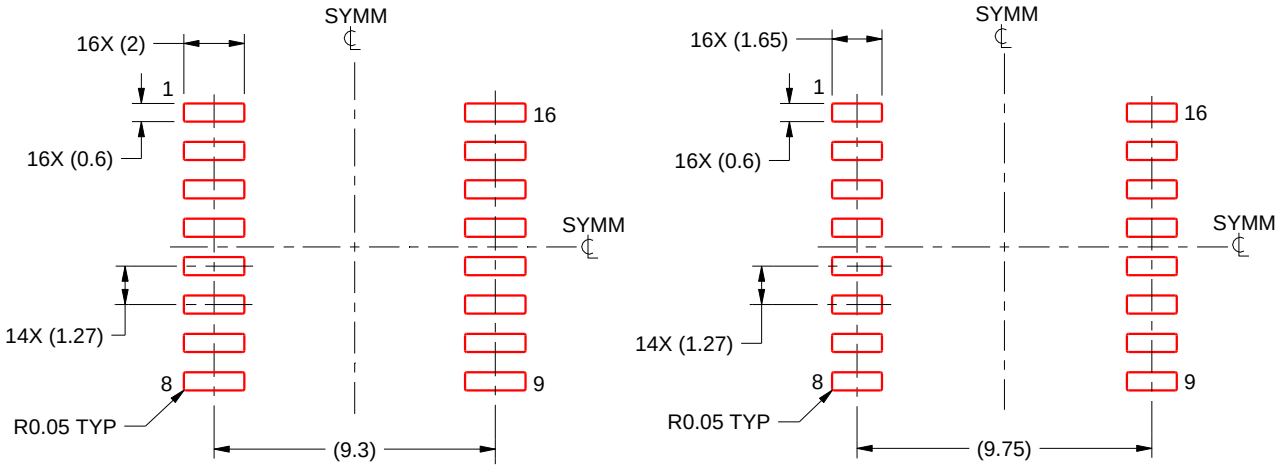
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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