

# DRV110 ソレノイド、リレー、バルブ用の120Vおよび230V AC、 6~48V DC電流コントローラ

## 1 特長

- 高電圧の動作用に、電源ピンにツェナー・ダイオードを内蔵
  - 整流器および $R_S$ 抵抗経由で120Vおよび230V AC電源を使用
  - $R_S$ 抵抗経由で24V、48V、およびより高電圧のDC電源を使用
- PWMにより外付けMOSFETを駆動し、ソレノイド電流を制御
  - 外付けの検出抵抗によりソレノイド電流をレギュレート
- ソレノイド電流の高速なランプ・アップによりアクティブ化を保証
- ホールド・モードでソレノイド電流を低減し、低消費電力と熱放散を実現
- ランプ・ピーク電流、ピーク電流のキープ時間、およびPWMクロック周波数を外部で設定可能。これらは外付け部品なしでも通常の値で動作可能
- 保護
  - サーマル・シャットダウン
  - 低電圧誤動作防止(UVLO)
- オプションのSTATUS出力
- 動作温度範囲:  $-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$
- 8ピンおよび14ピンのTSSOPパッケージ・オプション

## 2 アプリケーション

- 電気機械ドライバ: ソレノイド、バルブ、リレー、接触子、スイッチギア、空気圧
- 白物家電、太陽光、輸送機械、スマート・グリッド、配電

## 3 概要

DRV110デバイスは、ソレノイド用のPWM電流コントローラです。このデバイスは、適切に制御された波形により電流をレギュレートし、消費電力を減らすように設計されています。ソレノイド電流は高速にランプ・アップされ、バルブやリレーが確実に開くようになります。最初のランプの後で、正しい動作を保証するためソレノイド電流はピーク値に維持され、その後で熱による問題を回避し、消費電力を減らすため、電流は低い保持レベルまで引き下げられます。

ピーク電流の期間は、外付けのコンデンサにより設定されます。電流ランプのピークおよび保持レベルと、PWM周波数は、外付けの抵抗で別々に設定できます。外付けの設定抵抗は、対応するパラメータのデフォルト値がアプリケーションに適切なら、省略できます。

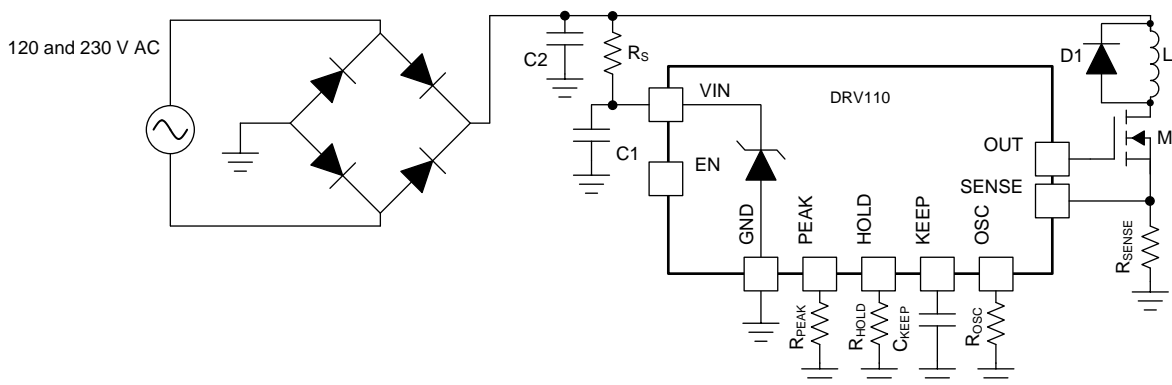
DRV110にはツェナー・ダイオードが内蔵されており、高い電源電圧を必要とするアプリケーションで、VINの電源電圧を $V_{ZENER}$ に制限します。内蔵のツェナーを使用することで、DRV110は整流器と電流制限抵抗を経由して120Vおよび230V AC電源から電力の供給を受けることができます。この方法により、48Vなどの高いDC電圧も使用できます。

### 製品情報<sup>(1)</sup>

型番	パッケージ	本体サイズ(公称)
DRV110	TSSOP (14)	5.00mmx4.40mm
	TSSOP (8)	3.00mmx4.40mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

### 電源ライン電圧によるDRV110への給電



Copyright © 2018, Texas Instruments Incorporated

## 目次

1	特長	1	7.4	Device Functional Modes	13
2	アプリケーション	1	8	<b>Application and Implementation</b>	14
3	概要	1	8.1	Application Information	14
4	改訂履歴	2	8.2	Typical Application	14
5	<b>Pin Configuration and Functions</b>	4	9	<b>Power Supply Recommendations</b>	17
6	<b>Specifications</b>	5	10	<b>Layout</b>	17
6.1	Absolute Maximum Ratings	5	10.1	Layout Guidelines	17
6.2	ESD Ratings	5	10.2	Layout Example	18
6.3	Recommended Operating Conditions	5	11	デバイスおよびドキュメントのサポート	19
6.4	Thermal Information	5	11.1	ドキュメントのサポート	19
6.5	Electrical Characteristics	6	11.2	ドキュメントの更新通知を受け取る方法	19
6.6	Typical Characteristics	7	11.3	コミュニティ・リソース	19
7	<b>Detailed Description</b>	8	11.4	商標	19
7.1	Overview	8	11.5	静電気放電に関する注意事項	19
7.2	Functional Block Diagram	8	11.6	Glossary	19
7.3	Feature Description	9	12	メカニカル、パッケージ、および注文情報	19

## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

### Revision F (March 2017) から Revision G に変更

Page

•	ツェナー・ダイオードにより制限される最大電源電圧を15Vから $V_{ZENER}$ に変更	1
•	Deleted <i>virtual</i> from the operating junction temperature and changed its maximum value from 125°C to 150°C in the <i>Absolute Maximum Ratings</i> table	5
•	Added the temperature range for the parameters in the <i>Recommended Operating Conditions</i> table, add the $V_S$ parameter, and updated the $V_{IN}$ and $I_Q$ parameters	5
•	Deleted the solenoid inductance parameter from the <i>Recommended Operating Conditions</i> table	5
•	Deleted the $I_{VIN}$ test condition from the gate drive voltage parameter in the <i>Electrical Characteristics</i> table	6
•	Changed the parameter names for $V_{PEAK}$ and $V_{HOLD}$ in the <i>Electrical Characteristics</i> table	6
•	Added the input pulldown resistance parameter in the <i>Electrical Characteristics</i> table	6
•	Added the <i>DRV110 Current Control with Varying OUT Duty Cycle</i> image to the <i>PWM Current Control</i> section	10
•	Changed the $R_{PEAK}$ value for $I_{PEAK} = 450$ mA from 50 k $\Omega$ to 55 k $\Omega$ in the <i>Configuring Peak and Hold Currents</i> section	10
•	Changed the <i>Configuring Peak and Hold Currents</i> section and <i>PEAK and HOLD Mode <math>V_{REF}</math> Settings</i> image (which is now named <i><math>I_{PEAK}</math> and <math>I_{HOLD}</math> settings for <math>R_{SENSE} = 1 \Omega</math></i> )	11
•	Changed the <i>Voltage Supply and Integrated Zener Diode</i> section. Added the <i><math>V_{ZENER}</math> Value</i> table and changed the $R_S$ equation to specify calculations for $R_{S,max}$ and $R_{S,min}$	12
•	Deleted the <i>Default Configuration</i> schematic	14
•	Added the <i>Current Limiting Resistor Selection</i> and <i>Passives Selection</i> sections in the <i>Detailed Design Procedure</i>	15
•	Changed the value of $R_{PEAK}$ from 303 k $\Omega$ to 400 k $\Omega$ in the <i>Application Curve</i>	17

### Revision E (November 2016) から Revision F に変更

Page

•	Changed the <i>Functional Block Diagram</i>	8
•	Changed the $I_{HOLD}$ equation	11
•	Changed the <i>Shutdown</i> section to provide a description of the STATUS pin.	13

---

**Revision D (June 2016) から Revision E に変更** **Page**


---

- ドキュメントのタイトルにV ACおよびV DCの値を含めて 変更 ..... 1
  - 「特長」および「アプリケーション」の一覧を修正 ..... 1
  - 表紙のグラフィックを回路図に 変更 ..... 1
  - Revised table notes for *Recommended Operating Conditions* table..... 5
- 

**Revision C (April 2016) から Revision D に変更** **Page**


---

- ドキュメントのタイトル 変更..... 1
  - Changed 160 kΩ in the  $f_{PWM}$  equation to 66.67 kΩ ..... 11
  - 追加「ドキュメントの更新通知を受け取る方法」セクション ..... 19
- 

**Revision B (July 2015) から Revision C に変更** **Page**


---

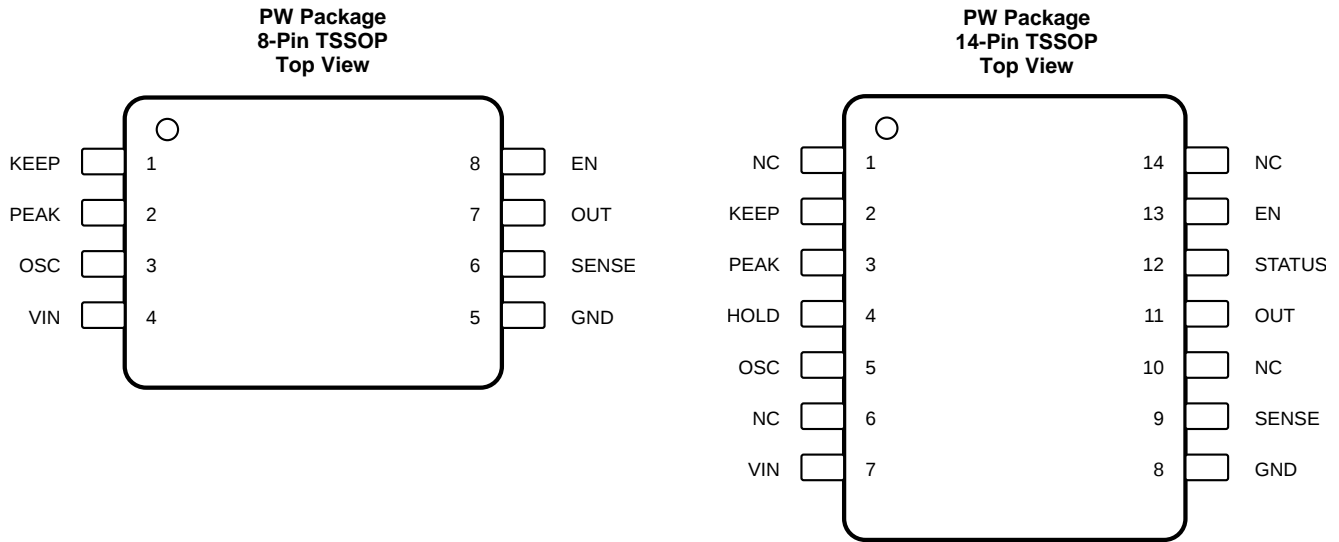
- Changed one test condition ( $R_{OSC} = 50\text{ k}\Omega$  to 160 kΩ) and the maximum value for the Externally set PWM clock frequency (60 to 25) in the *Electrical Characteristics* table ..... 6
  - Changed the *PWM Clock Frequency Setting* graph..... 11
- 

**Revision A (January 2013) から Revision B に変更** **Page**


---

- 「ESD定格」の表、「機能説明」セクション、「デバイスの機能モード」、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスとドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクション 追加 ..... 1
-

## 5 Pin Configuration and Functions



### Pin Functions

NAME	PIN NO.		I/O	DESCRIPTION
	8 PINS	14 PINS		
EN	8	13	I	Enable
GND	5	8	—	Ground
HOLD	—	4	I	Hold current set <sup>(1)</sup>
KEEP	1	2	I	Keep time set
NC	—	1	—	No connect
NC	—	6	—	No connect
NC	—	10	—	No connect
NC	—	14	—	No connect
OSC	3	5	I	PWM frequency set
OUT	7	11	O	Solenoid switch gate drive
PEAK	2	3	I	Peak current set
SENSE	6	9	I	Solenoid current sense
STATUS	—	12	O	Open drain status indicator
VIN	4	7	I	6-V to 15-V supply

(1) In the 8-pin package, the HOLD pin is not bonded out. For this package, the HOLD mode is configured to default (internal) settings.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

See <sup>(1)</sup> and <sup>(2)</sup>

		MIN	MAX	UNIT
V <sub>IN</sub>	Input voltage	-0.3	20	V
	Voltage on EN, STATUS, PEAK, HOLD, OSC, SENSE, KEEP	-0.3	7	V
	Voltage on OUT	-0.3	20	V
T <sub>J</sub>	Operating junction temperature	-40	150	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge		
	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

-40°C ≤ T<sub>A</sub> ≤ 125°C (unless otherwise noted)

		MIN	NOM	MAX	UNIT
I <sub>Q</sub>	Supply current (the device sinks additional current when V <sub>IN</sub> > V <sub>ZENER</sub> <sup>(1)</sup> )	1	1.5	3	mA
V <sub>IN</sub>	Voltage at the VIN pin <sup>(2)(3)</sup> (see <a href="#">Detailed Description</a> )	6			V
V <sub>S</sub>	Voltage directly from the supply before clamped by the Zener diode	6		330	V
C <sub>IN</sub>	Input capacitor between VIN and GND <sup>(4)</sup>	1	4.7		μF
T <sub>A</sub>	Operating ambient temperature	-40		125	°C

- (1) The device regulates the supply with an internal Zener diode. The device sinks up to 3 mA with the added supply current. See [Equation 5](#) to find appropriate value for the R<sub>S</sub> resistor.
- (2) The maximum input voltage of the device depends on the clamping voltage of the internal Zener diode, which changes over temperature. A current-limiting resistor is required to limit current to the Zener diode if the input voltage (V<sub>IN</sub>) is greater than V<sub>ZENER</sub>. For more information on resistor sizing see the [Detailed Description](#) section and [Application and Implementation](#) section.
- (3) For V<sub>S</sub> voltages less than V<sub>ZENER</sub>, V<sub>IN</sub> = V<sub>S</sub>. For V<sub>S</sub> voltages greater than V<sub>ZENER</sub>, V<sub>IN</sub> = V<sub>ZENER</sub>.
- (4) 4.7-μF input capacitor and full wave rectified 230-Vrms AC supply results in approximately 500-mV supply ripple.

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	DRV110		UNIT	
	PW (TSSOP)			
	8 PINS	14 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	183.8	122.6	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	69.2	51.2	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	112.6	64.3	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	10.4	6.5	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	110.9	63.7	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

## 6.5 Electrical Characteristics

 $V_{IN} = 14\text{ V}$ ,  $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ , over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY</b>						
$I_Q$	Standby current	EN = 0, $V_{IN} = 14\text{ V}$ , bypass deactivated		200	250	$\mu\text{A}$
	Quiescent current	EN = 1, $V_{IN} = 14\text{ V}$ , bypass deactivated		360	570	
	Internally regulated supply	EN = 0, $I_{VIN} = 2\text{ mA}$ , bypass activated	10.5	15	19	V
		EN = 1, $I_{VIN} = 2\text{ mA}$ , bypass activated	14.5	15	15.5	
<b>GATE DRIVER</b>						
$V_{DRV}$	Gate drive voltage	Supply voltage in regulation		$V_{IN}$		V
$I_{DRV\_SINK}$	Gate drive sink current	$V_{OUT} = 15\text{ V}$ ; $V_{IN} = 15\text{ V}$	8	15		mA
$I_{DRV\_SOURCE}$	Gate drive source current	$V_{OUT} = \text{GND}$ ; $V_{IN} = 15\text{ V}$		-15	-10	mA
$f_{PWM}$	PWM clock frequency	OSC = GND	15	20	27	kHz
$D_{MAX}$	Maximum PWM duty cycle			100%		
$D_{MIN}$	Minimum PWM duty cycle			7.5%		
$t_D$	Start-up delay	Delay between EN going high until gate driver starts switching, $f_{PWM} = 20\text{ kHz}$			50	$\mu\text{s}$
<b>CURRENT CONTROLLER, INTERNAL SETTINGS</b>						
$I_{PEAK}$	Peak current	$R_{SENSE} = 1\ \Omega$ , PEAK = GND	270	300	330	mA
$I_{HOLD}$	Hold current	$R_{SENSE} = 1\ \Omega$ , HOLD = GND	40	50	65	mA
<b>CURRENT CONTROLLER, EXTERNAL SETTINGS</b>						
$t_{KEEP}$	Externally set keep time at peak current	$C_{KEEP} = 1\ \mu\text{F}$		100		ms
$V_{PEAK}$	Voltage of internal reference to which the SENSE pin voltage is compared to for $I_{PEAK}$	$R_{PEAK} = 50\text{ k}\Omega$		900		mV
		$R_{PEAK} = 200\text{ k}\Omega$		300		
$V_{HOLD}$	Voltage of internal reference to which the SENSE pin voltage is compared to for $I_{HOLD}$	$R_{HOLD} = 50\text{ k}\Omega$		150		mV
		$R_{HOLD} = 200\text{ k}\Omega$		50		
$f_{PWM}$	Externally set PWM clock frequency	$R_{OSC} = 160\text{ k}\Omega$		25		kHz
		$R_{OSC} = 200\text{ k}\Omega$		20		
<b>LOGIC INPUT LEVELS (EN)</b>						
$V_{IL}$	Input low level				1.3	V
$V_{IH}$	Input high level		1.65			V
$R_{EN}$	Input pullup resistance		350	500		$\text{k}\Omega$
	Input pulldown resistance			250		$\text{k}\Omega$
<b>LOGIC OUTPUT LEVELS (STATUS)</b>						
$V_{OL}$	Output low level	Pulldown activated, $I_{STATUS} = 2\text{ mA}$			0.3	V
$I_{IL}$	Output leakage current	Pulldown deactivated, $V(\text{STATUS}) = 5\text{ V}$			2	$\mu\text{A}$
<b>UNDERVOLTAGE LOCKOUT</b>						
$V_{UVLO}$	Undervoltage lockout threshold			4.6		V
<b>THERMAL SHUTDOWN</b>						
$T_{TSU}$	Junction temperature start-up threshold			140		$^{\circ}\text{C}$
$T_{TSD}$	Junction temperature shutdown threshold			160		$^{\circ}\text{C}$

## 6.6 Typical Characteristics

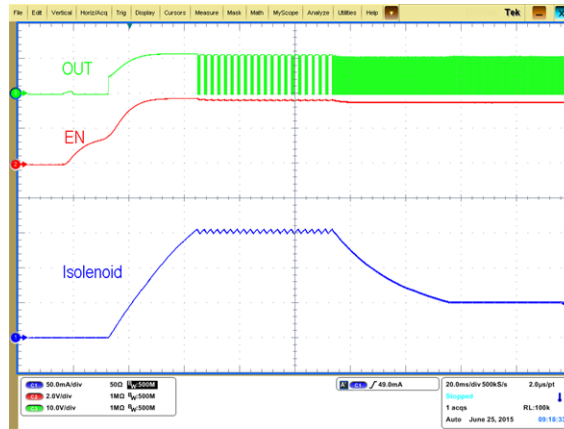


Figure 1. Solenoid Current, EN, and PWM vs Time

## 7 Detailed Description

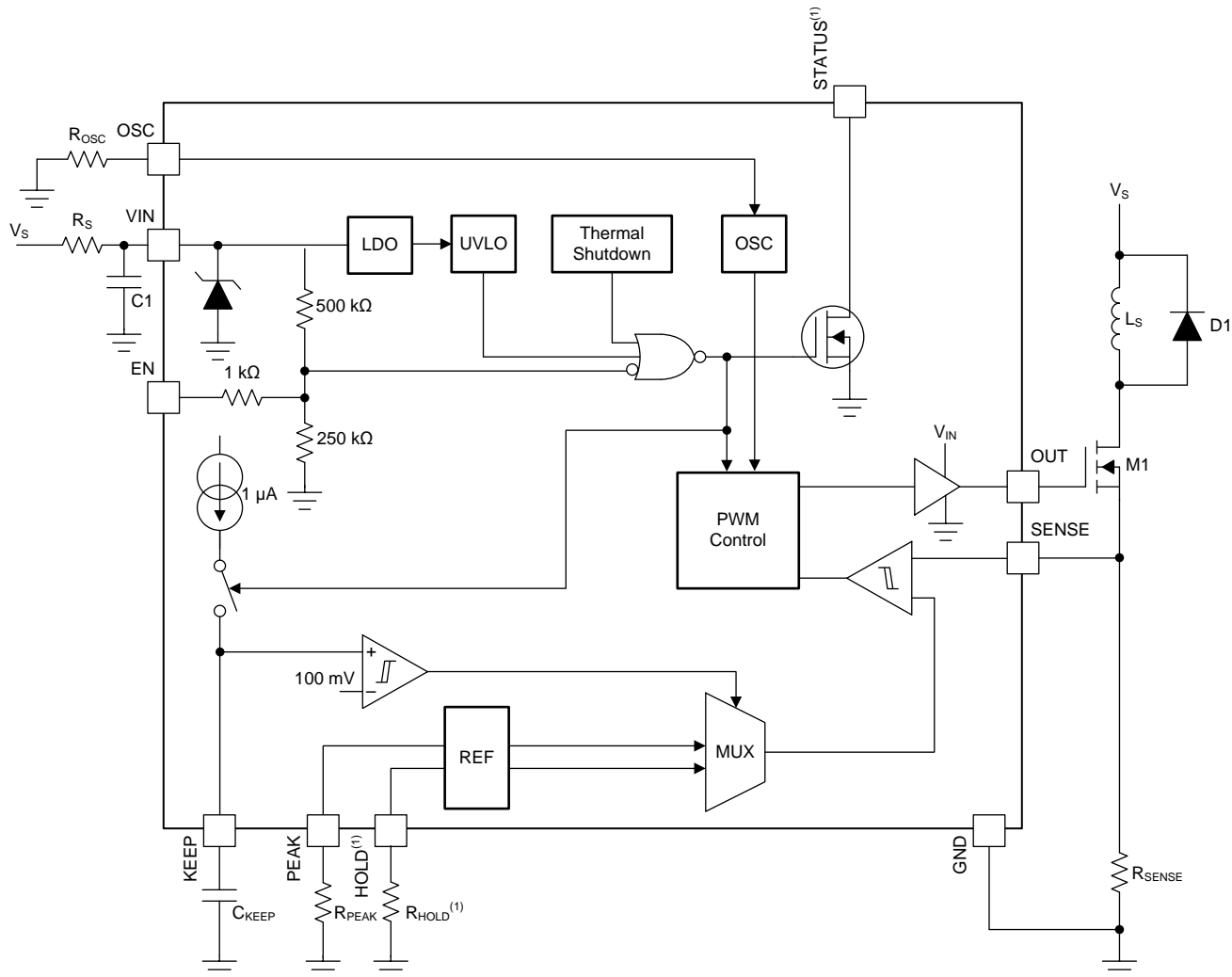
### 7.1 Overview

The DRV110 device provides a PWM current controller for use with solenoids. The device provides a quick ramp to a high peak current value in order to ensure opening of the valve or relay. The current is held for a programmable time and then lowered to the hold current value to maintain the open state of the valve or relay while reducing the total current consumption. Peak current duration, peak current amount, hold current amount (in the 14-pin package), and PWM frequency can all be controlled by external components or used at default levels by omitting these components (except peak current duration).

Enable and disable of the switch is controlled by the EN pin. The EN pin contains an internal resistor network to set the pin to logic HIGH when the EN pin is floating. This feature can be used for situations where a control signal is not required and the solenoid is only energized when a supply voltage is present. Such applications could be valves or contactors.

The DRV110 also features a wide VIN range with an internal bypass regulator to maintain VIN at an acceptable level. Finally, the 14-pin package features an open-drain pull-down path on the STATUS pin which is enabled as long as undervoltage lockout or thermal shutdown has not triggered.

### 7.2 Functional Block Diagram



Copyright © 2017, Texas Instruments Incorporated

(1) Available only in the 14-pin package.



### 7.3 Feature Description

The DRV110 controls the current through the solenoid as shown in [Figure 2](#). Activation starts when EN pin voltage is pulled high either by an external driver or internal pullup. In the beginning of activation, DRV110 allows the solenoid current to ramp up to the peak value  $I_{PEAK}$  and it regulates it at the peak value for the time,  $t_{KEEP}$ , before reducing it to  $I_{HOLD}$ . The solenoid current is regulated at the hold value as long as the EN pin is kept high. The initial current ramp-up time depends on the inductance and resistance of the solenoid. Once EN pin is driven to GND, DRV110 allows the solenoid current to decay to zero.

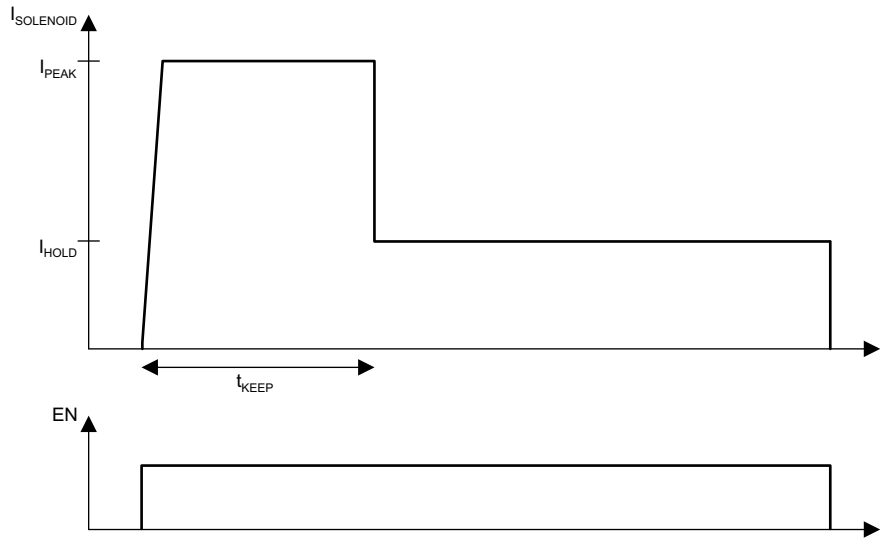


Figure 2. Typical Current Waveform Through the Solenoid

#### 7.3.1 Keep Time

The keep time,  $t_{KEEP}$ , is set externally by connecting a capacitor to the KEEP pin. A constant current is sourced from the KEEP pin that is driven into an external capacitor resulting in a linear voltage ramp. When the KEEP pin voltage reaches 100 mV, the current regulation reference voltage,  $V_{REF}$ , is switched from  $V_{PEAK}$  to  $V_{HOLD}$ . The internal current source is switched off, and the capacitor is grounded for discharge. The dependency of  $t_{KEEP}$  from the external capacitor size can be calculated with [Equation 1](#).

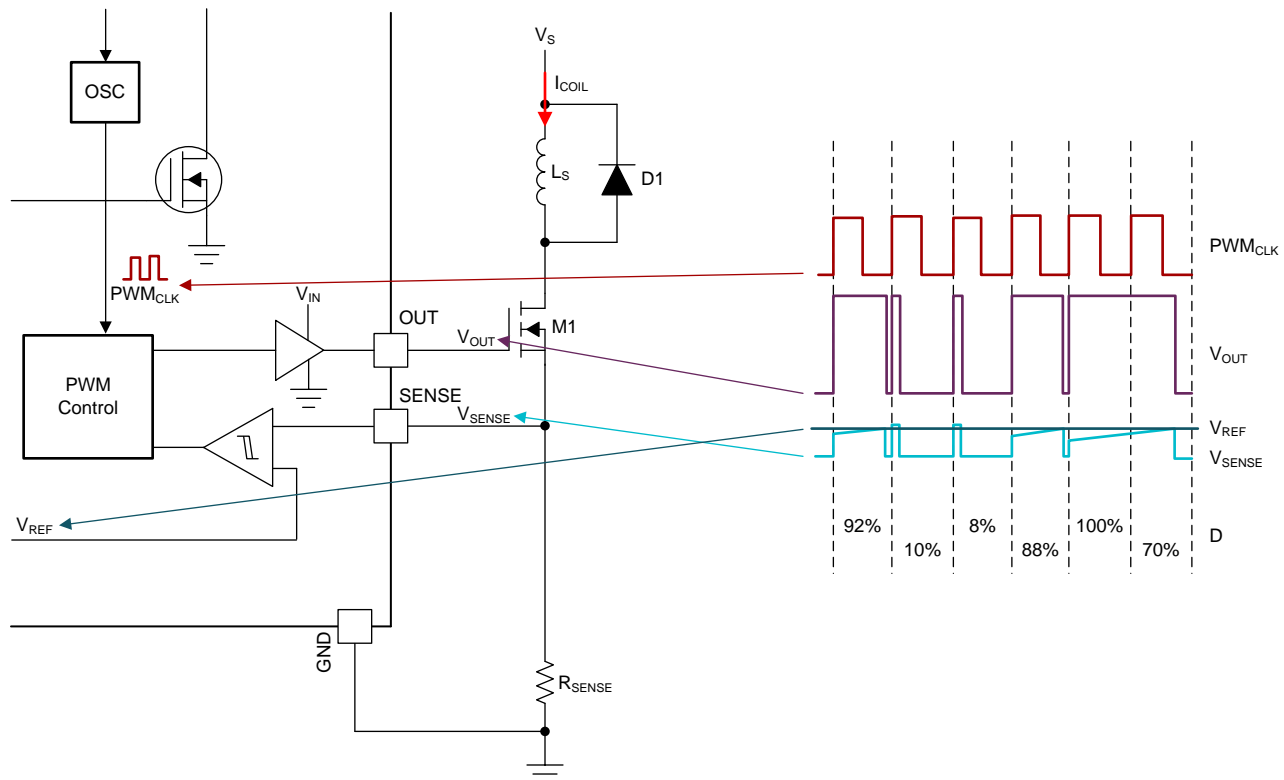
$$t_{KEEP} [s] = C_{KEEP} [F] \cdot 10^5 \left[ \frac{s}{F} \right] \quad (1)$$

#### 7.3.2 PWM Current Control

The current control loop regulates, cycle-by-cycle, the solenoid current by sensing voltage at the SENSE pin and controlling the external switching device gate through the OUT pin. During the ON-cycle, the OUT pin voltage is driven and kept high (equal to  $V_{IN}$  voltage) allowing current to flow through the external switch as long as the voltage at the SENSE pin is less than  $V_{REF}$ . As soon as the voltage at the SENSE pin is above  $V_{REF}$ , the OUT pin voltage is immediately driven low and kept low until the next ON-cycle is triggered by the internal PWM clock signal. In the beginning of each ON-cycle, the OUT pin voltage is driven high and kept high for at least the time determined by the minimum PWM signal duty cycle,  $D_{MIN}$ .

Because the current sense is done by comparing the voltage at the SENSE pin to a reference voltage, the DRV110 device acts like a hysteresis controller. When the device acts like a hysteresis controller, it can make the PWM frequency and duty cycle appear uneven for some solenoids (see [Figure 3](#)).

Feature Description (continued)



- (1) The DRV110 device measures the voltage at the SENSE node ( $V_{SENSE}$ ). This voltage is compared against the reference voltage ( $V_{REF}$ ) each clock cycle. The voltage at the output node ( $V_{OUT}$ ) becomes low when  $V_{SENSE} \geq V_{REF}$ . The duty cycle (D) of the output voltage varies from 8% to 100%. In summary, the SENSE voltage is sampled after each rising edge of the PWM CLK signal ( $PWM_{CLK}$ ) and goes low when  $V_{SENSE} \geq V_{REF}$  at a minimum duty cycle of 8%.

Figure 3. DRV110 Current Control with Varying OUT Duty Cycle

7.3.3 Configuring Peak and Hold Currents

$I_{PEAK}$  and  $I_{HOLD}$  depend on fixed resistance values  $R_{PEAK}$  and  $R_{HOLD}$  as shown in Figure 4. If the PEAK pin or HOLD pin is connected to ground or  $R_{PEAK}$  or  $R_{HOLD}$  is less than 43.33 k $\Omega$  (typical), then  $I_{PEAK}$  is at its default value of 300 mA for  $I_{PEAK}$  and 50 mA for  $I_{HOLD}$ .

The  $I_{PEAK}$  value can alternatively be set by connecting an external resistor to ground from the PEAK pin. For example, if a 60-k $\Omega$  ( $= R_{PEAK}$ ) resistor is connected between PEAK and GND, and  $R_{SENSE} = 1 \Omega$ , then the externally set  $I_{PEAK}$  level will be 900 mA. If  $R_{PEAK} = 200 \text{ k}\Omega$  and  $R_{SENSE} = 1 \Omega$ , then the externally set  $I_{PEAK}$  level will be 300 mA. TI does not recommend using a resistor from 30 k $\Omega$  and 55 k $\Omega$  to avoid the  $I_{PEAK}$  or  $I_{HOLD}$  current slipping from the maximum current setting to the default setting.

In case  $R_{SENSE} = 2 \Omega$  instead of 1  $\Omega$ , then  $I_{PEAK} = 450 \text{ mA}$  (when  $R_{PEAK} = 55 \text{ k}\Omega$ ) and  $I_{PEAK} = 150 \text{ mA}$  (when  $R_{PEAK} = 200 \text{ k}\Omega$ ). In the 8-pin package, the HOLD reference uses the internal  $V_{REF}$  setting of 50 mV. In the 14-pin package, external setting of the HOLD current,  $I_{HOLD}$ , works in the same way as the external setting for  $I_{PEAK}$  but the current levels are 1/6 of the  $I_{PEAK}$  levels for the same resistor setting.

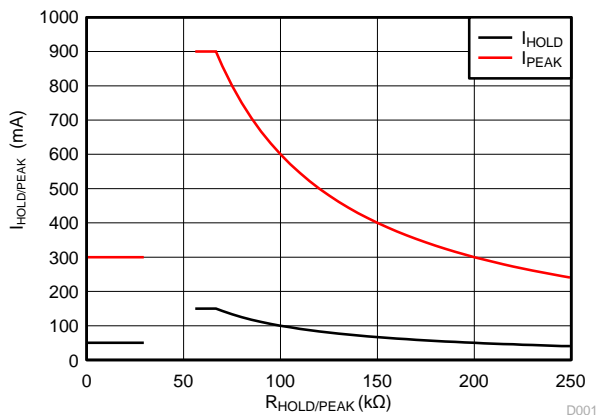
External settings for  $I_{PEAK}$  and  $I_{HOLD}$  are independent of each other. If  $R_{PEAK}$  or  $R_{HOLD}$  is decreased below 33.33 k $\Omega$  (typical value), then the reference is clamped to the internal setting of 300 mV for PEAK and 50 mV for HOLD. Use Equation 2 and Equation 3 to calculate the values for  $I_{PEAK}$  and  $I_{HOLD}$  respectively.

The currents and resistor values should be chosen such that the voltage across the sense resistor is more than 30 mV.

**Feature Description (continued)**

$$I_{PEAK} = \frac{V_{REF}}{R_{SENSE}} = \frac{1 \Omega \times 900 \text{ mA} \times 66.67 \text{ k}\Omega}{R_{PEAK}} \times \frac{1}{R_{SENSE}}; 66.67 \text{ k}\Omega < R_{PEAK} < 2 \text{ M}\Omega \tag{2}$$

$$I_{HOLD} = \frac{V_{REF}}{R_{SENSE}} = \frac{1 \Omega \times 150 \text{ mA} \times 66.67 \text{ k}\Omega}{R_{HOLD}} \times \frac{1}{R_{SENSE}}; 66.67 \text{ k}\Omega < R_{HOLD} < 333 \text{ k}\Omega \tag{3}$$

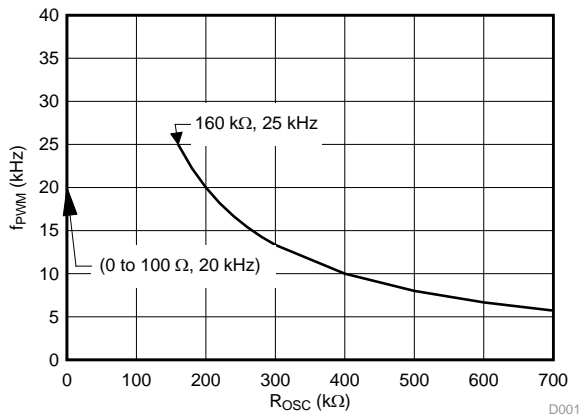


**Figure 4. I<sub>PEAK</sub> and I<sub>HOLD</sub> settings for R<sub>SENSE</sub> = 1 Ω**

**7.3.4 Configuring the PWM Frequency**

Frequency of the internal PWM clock signal, PWM<sub>CLK</sub>, that triggers each OUT pin ON-cycle can be adjusted by external resistor, R<sub>OSC</sub>, connected between OSC and GND. Frequency as a function of resistor value is shown in Figure 5. Default frequency is used when OSC is connected to GND directly. Use Equation 4 to calculate the PWM frequency as a function of the external fixed adjustment resistor value (greater than 160 kΩ).

$$f_{PWM} = \frac{60 \text{ kHz}}{R_{OSC}} \times 66.67 \text{ k}\Omega; 160 \text{ k}\Omega < R_{OSC} < 2 \text{ M}\Omega \tag{4}$$



**Figure 5. PWM Clock Frequency Setting**

**7.3.5 Voltage Supply and Integrated Zener Diode**

Voltage at the OUT pin, that is the gate voltage of an external switching device, is equal to VIN voltage during the ON-cycle. The voltage is driven to ground during the OFF-cycle. VIN voltages below V<sub>ZENER</sub> can be supplied directly from an external voltage source. Supply voltages of at least 6 V are supported.

**Feature Description (continued)**

The DRV110 is able to regulate VIN voltage from a higher external supply voltage,  $V_S$ , by an internal bypass regulator that replicates the function of an ideal Zener diode. This requires that the supply current is sufficiently limited by an external resistor between  $V_S$  and the VIN pin. An external capacitor connected to the VIN pin is used to store enough energy to charge the external switch gate capacitance at the OUT pin. A range of current limiting resistor sizes ( $R_{S,min}$  and  $R_{S,max}$ ) can be calculated with [Equation 5](#) and [Equation 6](#). This range keeps the VIN current within the recommended operating conditions.

$$R_{S,max} = \frac{V_{S,minDC} - V_{ZENER}}{1 \text{ mA} + I_{Gate,AVE}}$$

where

- $I_{Gate,AVE}$  is the current flowing to the external switch. For a MOSFET,  $I_{Gate,AVE}$  is equal to the external FET gate charge multiplied by  $f_{PWM}$ . (5)

$$R_{S,min} = \frac{V_{S,maxDC} - V_{ZENER}}{3 \text{ mA} + I_{Gate,AVE}} \quad (6)$$

Ideally, the DRV110 device clamps the input voltage to 15 V. For configurations that do not use the EN pin (force the pin high or leave it floating), the DRV110 device clamps at 15 V ( $V_{ZENER} = 15 \text{ V}$ ) across the temperature range of the device. If the EN pin is set to 0, then refer to the values in [Table 1](#) to find the  $V_{ZENER}$  used when calculating the value of  $R_S$ , based on the temperature range of the application. Because the  $V_{ZENER}$  changes when the EN state changes, select a value for  $R_S$  that meets the current requirements at both  $V_{ZENER}$  voltages.

**Table 1.  $V_{ZENER}$  Value**

TEMPERATURE RANGE	ENABLE STATE	$V_{ZENER}$
$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	1	15 V
$-40^\circ\text{C} \leq T_A \leq 35^\circ\text{C}$	0	15 V
$-40^\circ\text{C} \leq T_A \leq 45^\circ\text{C}$	0	14.2 V
$-40^\circ\text{C} \leq T_A \leq 55^\circ\text{C}$	0	13.9 V
$-40^\circ\text{C} \leq T_A \leq 65^\circ\text{C}$	0	13.5 V
$-40^\circ\text{C} \leq T_A \leq 75^\circ\text{C}$	0	13.1 V
$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	0	12.7 V
$-40^\circ\text{C} \leq T_A \leq 95^\circ\text{C}$	0	12.3 V
$-40^\circ\text{C} \leq T_A \leq 105^\circ\text{C}$	0	12 V
$-40^\circ\text{C} \leq T_A \leq 115^\circ\text{C}$	0	11.4 V
$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	0	11 V

The open-drain pulldown path at the STATUS pin is deactivated if the undervoltage lockout or thermal shutdown blocks have triggered or if the EN pin is low.

## 7.4 Device Functional Modes

### 7.4.1 Normal Mode

The DRV110 transitions through three different states in normal mode:

**OFF state** In the OFF state, the EN pin is low and the PWM output is off.

**PEAK state** The PEAK state begins when the EN pin is set high, and ends when the  $t_{KEEP}$  time has been reached. During this state, the PWM operates to reach the  $I_{PEAK}$  current set by the  $R_{PEAK}$  resistor.

**HOLD state** In the HOLD state, the  $t_{KEEP}$  time has been reached, and the PWM continues to operate but at the  $I_{HOLD}$  level. This continues until the EN pin is set low again and the PWM turns off.

### 7.4.2 Shutdown

The DRV110 turns off the gate driver in undervoltage lockout ( $V_{IN} < 4.6\text{ V}$ ) or thermal shutdown ( $T_J > 160^\circ\text{C}$ ). If temperature shutdown is activated, the DRV110 resumes operation when the junction temperature is below  $140^\circ\text{C}$ . The shutdown conditions are expressed by the STATUS pin going to the high-impedance state. A pullup resistor can be connected to the STATUS pin so these conditions may be observed by a microcontroller. [Table 2](#) provides an explanation of this operation.

**Table 2. Shutdown Operation**

CONDITIONS			OUTPUT PINS	
EN	UVLO	TSD	STATUS	OUT
0	X	X	Hi-Z	LOW
1	0	0	Pulled down	HIGH or PWM
1	X	1	Hi-Z	LOW
1	1	X	Hi-Z	LOW

## 8 Application and Implementation

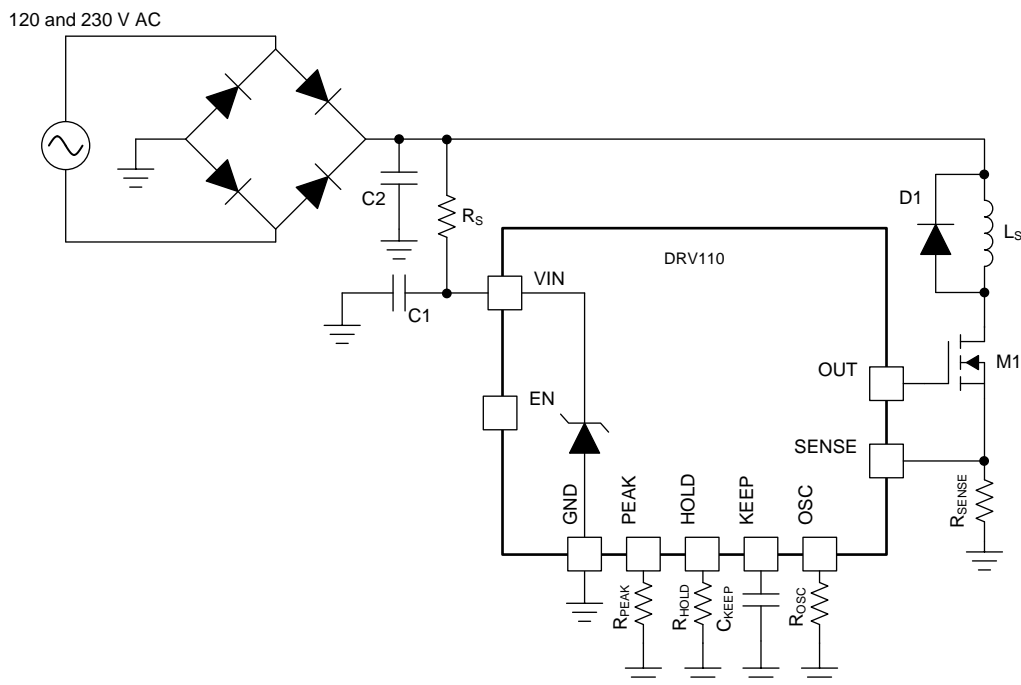
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The DRV110 device is designed to operate a solenoid valve or relay. For detailed information on using the DRV110 with 230 V AC solenoids, see [Current Controlled Driver for 230V AC Solenoids Reference Design](#). A typical DC input design will be outlined in [Typical Application](#). Approximate resistor and capacitor values for the peak current, hold current, sense, and keep time will be derived for a sample application.

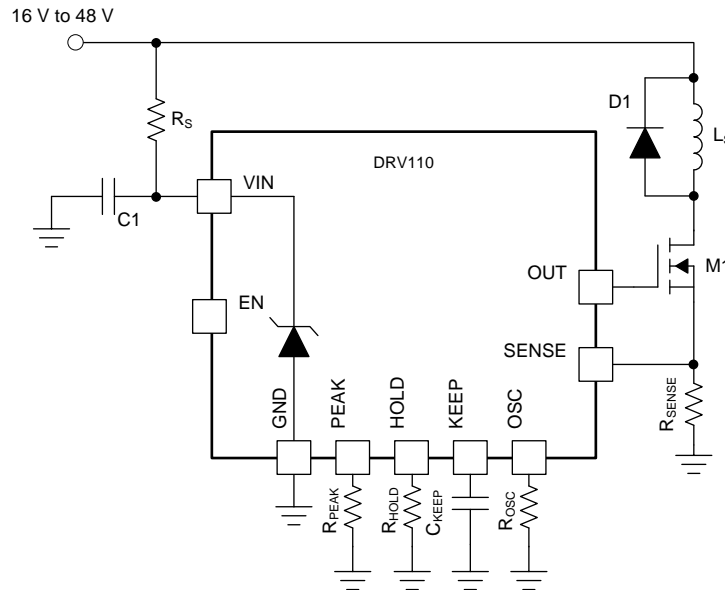
### 8.2 Typical Application



Copyright © 2016, Texas Instruments Incorporated

Figure 6. DRV110 Powered by a Rectified AC Power Source

## Typical Application (continued)



Copyright © 2016, Texas Instruments Incorporated

Figure 7. DRV110 Powered by a DC Power Source Greater than 15 V

### 8.2.1 Design Requirements

The key elements to identify here are the system input voltage, peak current, hold current, and peak keep time values required for the solenoid or relay being used. With these values, approximate  $R_S$ ,  $R_{PEAK}$ ,  $R_{HOLD}$  (for 14-pin package),  $C_{KEEP}$ , and  $R_{SENSE}$  values can be determined and the proper FET and diode can be identified.  $R_{OSC}$  can be varied in order to tune the circuit to the chosen solenoid or relay.

### 8.2.2 Detailed Design Procedure

#### 8.2.2.1 Current Limiting Resistor Selection

The temperature range, input voltage, and enable state must be considered when selecting the current limiting resistor. These values must be considered because the Zener clamping voltage of the DRV110 device starts dropping from its ideal 15 V at temperatures greater than 45°C when the EN pin is pulled low. Applications that leave the EN pin floating or pulled high at all times only require a current-limiting resistor when the input voltage is greater than 15 V across all temperature.

While using a current-limiting resistor is not required when the supply voltage ( $V_S$ ) is less than the Zener clamping voltage,  $V_{ZENER}$ , TI recommends populating a small resistor in case of possible input voltage transients during operation. At the very least, TI recommends placing a resistor footprint jumped by a 0-Ω resistor. Table 3 lists recommended resistor values for voltages close to  $V_{ZENER}$  and common voltages greater than  $V_{ZENER}$  for different enable states.

**Table 3. Recommended Resistor Values**  
 $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ 

SUPPLY VOLTAGE	RECOMMENDED CURRENT-LIMITING RESISTOR
<b>EN Pulled High or Floating</b>	
< 15 V	500 $\Omega$
24 V	9 k $\Omega$
48 V	33 k $\Omega$
110 V to 120 V	100 k $\Omega$
220 V to 240 V	200 k $\Omega$
<b>EN Toggled Between 0 and 1</b>	
10 V	510 $\Omega$
11 V	510 $\Omega$
12 V	1 k $\Omega$
13 V	2 k $\Omega$
14 V	3 k $\Omega$
15 V	3.9 k $\Omega$
24 V	13 k $\Omega$
48 V	36 k $\Omega$
110 V to 120 V	100 k $\Omega$
220 V to 240 V	200 k $\Omega$

### 8.2.2.2 Passive Component Selection

With the selected peak current, hold current, and peak keep time values, the values of  $R_{\text{PEAK}}$ ,  $R_{\text{HOLD}}$  (for 14-pin package),  $C_{\text{KEEP}}$ , and  $R_{\text{SENSE}}$  can be determined. [Table 4](#) lists the example values and results from calculation.

**Table 4. Example Application Values When  $R_{\text{SENSE}} = 1 \Omega$** 

VARIABLE	VALUE	14-PIN VALUES	8-PIN VALUES	CALCULATED FROM
Peak current	150 mA	$R_{\text{PEAK}} = 400 \text{ k}\Omega$	$R_{\text{PEAK}} = 400 \text{ k}\Omega$	<a href="#">Equation 2</a>
Hold current	50 mA	$R_{\text{HOLD}} = 200 \text{ k}\Omega$ or connect HOLD to ground	Default	<a href="#">Equation 3</a>
Keep time	100 ms	$C_{\text{KEEP}} = 1 \mu\text{F}$	$C_{\text{KEEP}} = 1 \mu\text{F}$	<a href="#">Equation 1</a>
PWM frequency	20 kHz	$R_{\text{OSC}} = \text{Shorted to ground}$	$R_{\text{OSC}} = \text{Shorted to ground}$	<a href="#">Equation 4</a>

Use [Equation 2](#) and [Equation 3](#) to calculate the values of the  $R_{\text{PEAK}}$  resistor and  $R_{\text{HOLD}}$  (if applicable) resistor. For the sample values, the  $R_{\text{PEAK}}$  resistor is set to 400 k $\Omega$  and the  $R_{\text{HOLD}}$  resistor is shorted to GND. TI recommends using a 0- $\Omega$  resistor for prototyping in case changes to this value are desired.

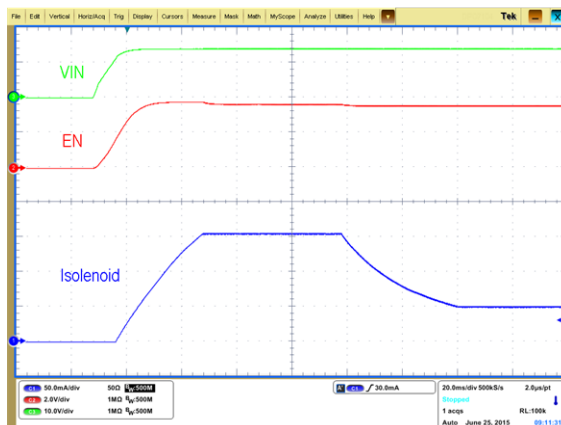
Next, select the value of the  $C_{\text{KEEP}}$  capacitor based on [Equation 1](#). For the sample value, the  $C_{\text{KEEP}}$  capacitor is set to 1  $\mu\text{F}$ . The  $R_{\text{OSC}}$  resistor is initially be shorted to GND, but a 0- $\Omega$  resistor is also recommended for prototyping. Additionally, a low-pass filter on the SENSE line can be added in a high-noise environment and is recommended for prototyping. The typical value for the low pass filter resistor is 1 k $\Omega$  and the typical value for the filter capacitor is 100 pF.

The value of sense resistor can be selected based on the preference of the designer. The only restriction is that the voltage across the sense resistor (found by the  $R_{\text{SENSE}}$  resistance times the  $I_{\text{HOLD}}$  current) must be greater than 30 mV for reliable operation.

The external FET and current recirculation diode must be selected based on the current values defined in [Table 4](#) and the supply voltage. The current recirculation diode should be a fast recovery diode.



### 8.2.3 Application Curve



$$\begin{array}{lll}
 R_{OSC} = 0 \Omega & R_{PEAK} = 400 \text{ k}\Omega & R_{HOLD} = 0 \Omega \\
 R_{SENSE} = 1 \Omega & C_{KEEP} = 1 \mu\text{F} & L_{ind} = 1 \text{ H} \\
 R_{ind} = 50 \Omega & \text{Measured on the EVM} & 
 \end{array}$$

Figure 8.  $I_{SOLENOID}$ , EN, and  $V_{IN}$  vs Time

## 9 Power Supply Recommendations

The input supply range must be at least 6 V, and needs a current-limiting resistor above  $V_{ZENER}$ . An input capacitor of 4.7  $\mu\text{F}$  (typical) is required as well.  $I_Q$  max is 3 mA, but additional current will be required to operate the solenoid or relay.

## 10 Layout

### 10.1 Layout Guidelines

Routing for the SENSE pin should be careful to avoid noise sources. Routing for the output node and sense node should be minimized. The trace for the solenoid or relay current should be wide in order to prevent any unexpected voltage drop.

## 10.2 Layout Example

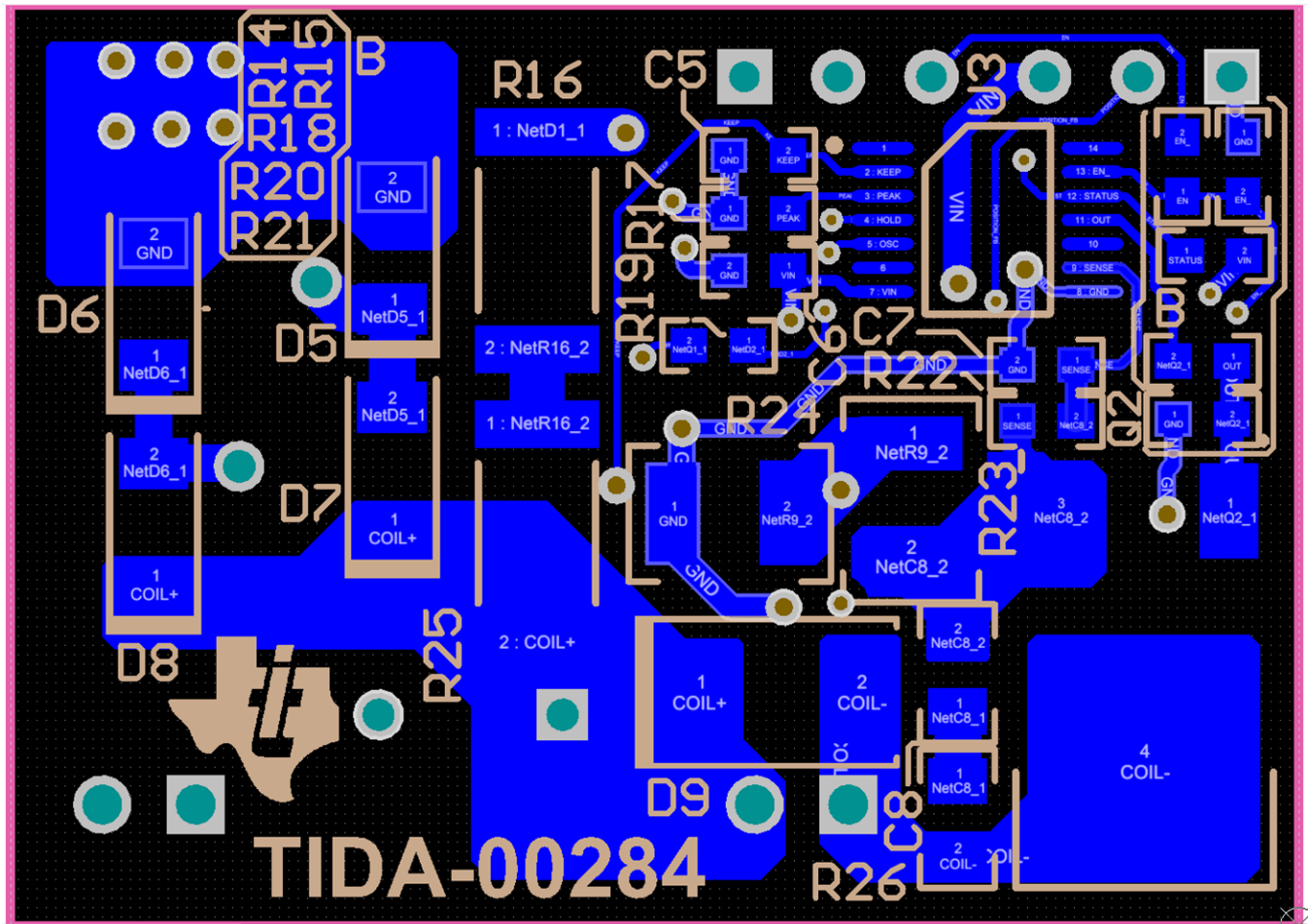


Figure 9. Layout Schematic

## 11 デバイスおよびドキュメントのサポート

### 11.1 ドキュメントのサポート

#### 11.1.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、『[プランジャー・フォルト検出機能を持つ、24V DCソレノイド用の電流制御ドライバ](#)』リファレンス・デザイン
- テキサス・インスツルメンツ、『[230V ACソレノイド用の電流制御ドライバ](#)』リファレンス・デザイン
- テキサス・インスツルメンツ、『[DRV110およびDRV120評価モジュール\(EVM\)](#)』ユーザー・ガイド

### 11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com)のデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™オンライン・コミュニティ** *TIのE2E (Engineer-to-Engineer) コミュニティ*。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイデアを検討して、問題解決に役立てることができます。

**設計サポート** *TIの設計サポート* 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

### 11.4 商標

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 11.5 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

### 11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV110APWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	110A	<a href="#">Samples</a>
DRV110PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	110	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV110APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DRV110PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV110APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
DRV110PWR	TSSOP	PW	8	2000	356.0	356.0	35.0

PW0014A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



# EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW0008A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153, variation AA.

# EXAMPLE BOARD LAYOUT

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## 重要なお知らせと免責事項

TI は、技術データと信頼性データ(データシートを含みます)、設計リソース(リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](#) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所 : Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024, Texas Instruments Incorporated