ADS1119 4チャネル、1kSPS、16ビット、I²Cインターフェイス搭載デルタ・シグマADC

1 特長

- 設定するレジスタが1つだけで使いやすい
- 消費電流はわずか315µA (標準値)
- 広い電源電圧範囲: 2.3V～5.5V
- レール・ツー・レール入力バッファにより高い入力インピーダンスを実現
- プログラマブル・ゲイン: 1、4
- プログラマブル・データレート: 最高1kSPS
- 16ビットのノイズ・フリー分解能(20SPS)
- シングルサイクル安定化デジタル・フィルタにより20SPSで50Hzおよび60Hzの同時除去
- 2つの差動入力または4つのシングルエンド入力
- 内部リファレンス：2.048V、ドリフト(標準値)：5ppm/℃
- 精度2%の内部発振器
- I²C互換インターフェイス
- サポートされるI²Cバス速度モード:
  Standard-Mode、Fast-Mode、Fast-Mode Plus
- 16のI²Cアドレスをピンで設定可能
- パッケージ：3.0mm × 3.0mm × 0.75mm WQFN

2 アプリケーション

- バッテリ・テスト機器
- ガス検出器
- 熱メータ
- 光モジュール
- ウェアラブル・フィットネスおよびアクティビティ・トラッカー

3 概要

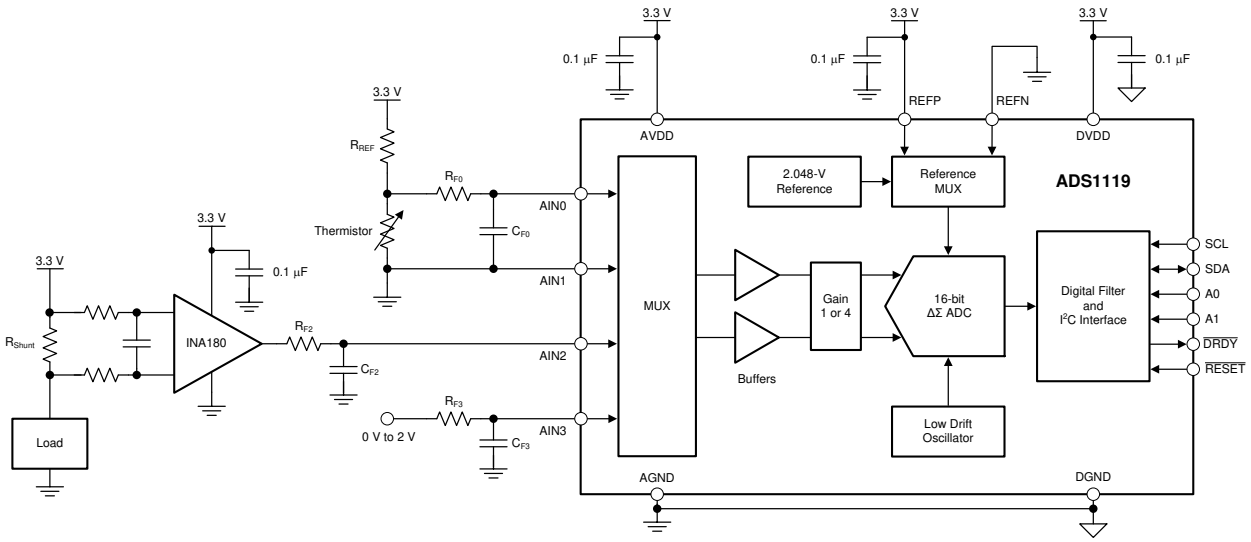
ADS1119は高精度の16ビット、アナログ/デジタル・コンバータ(ADC)で、電源電圧、電流、および温度監視など、最も一般的なシステム監視機能の実装に必要な機能をすべて搭載しています。柔軟な入力マルチプレクサ(MUX)を介した2つの差動入力または4つのシングルエンド入力を特長とし、レール・ツー・レール入力バッファ、プログラマブル・ゲイン段、基準電圧、発振器を備えています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
ADS1119	WQFN (16)	3.00mm×3.00mm
	TSSOP (16)	5.00mm×4.40mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

電圧、電流、および温度監視アプリケーション



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目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2018年8月発行のものから更新 **Page**

- Changed Internal Voltage Reference, *Accuracy* parameter: added *TSSOP package* to test conditions of first row and added second row to Internal Voltage Reference, *Accuracy* parameter ... 6
- 追加 *TSSOP package* to conditions of *Internal Reference Voltage Histogram* figure ... 12

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5 概要（続き）

バッファを搭載しているため、高インピーダンス・ソースを直接接続できます。ゲイン段はバッファに追従し、1および4のゲインを選択可能です。ADS1119はシングルサイクル安定化により、最高1000サンプル/秒(SPS)のデータレートで変換を実行できます。雑音の多い産業用途では、20SPSで、デジタル・フィルタにより50Hzおよび60Hzの同時除去を実現します。

ADS1119は2線式のI^2C互換インターフェイスを搭載しており、最高1MbpsのI^2Cバス速度に対応します。2本のアドレス・ピンを介して、16種類のI^2Cアドレスを選択することが可能です。

ADS1119は、16ピンのリードレスWQFNパッケージ、または16ピンTSSOPパッケージで供給され、-40℃ ～ +125℃の温度範囲で動作が規定されています。

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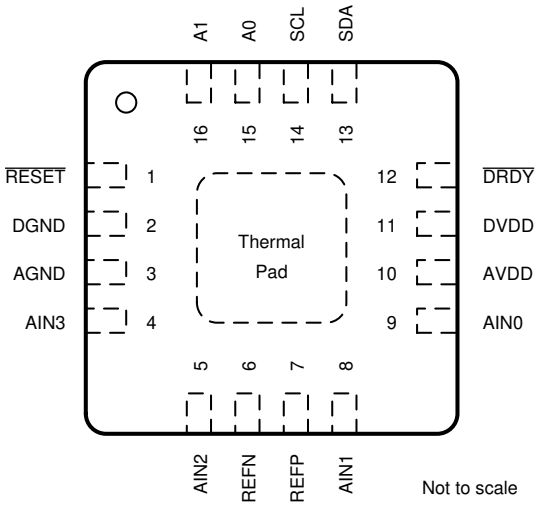
6 Pin Configuration and Functions

RTE Package
16-Pin WQFN
Top View



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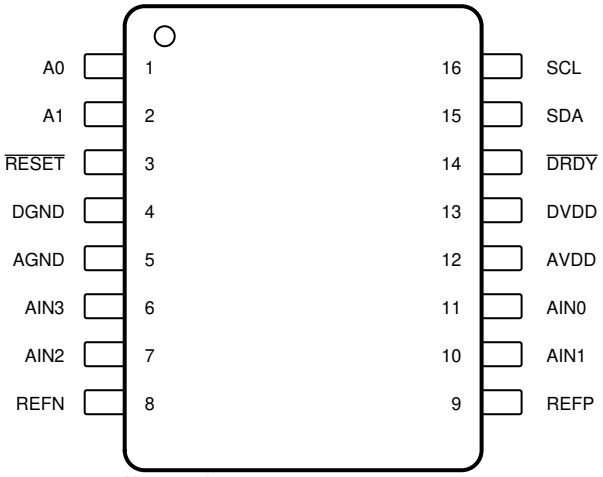
PW Package
16-Pin TSSOP
Top View



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Pin Functions

PIN			ANALOG OR DIGITAL INPUT/OUTPUT	DESCRIPTION[1]
NAME	NO. RTE	NO. PW		
A0	15	1	Digital input	I^2C slave address select pin 0. See the *I2C Address* section for details.
A1	16	2	Digital input	I^2C slave address select pin 1. See the *I2C Address* section for details.
AIN0	9	11	Analog input	Analog input 0
AIN1	8	10	Analog input	Analog input 1
AIN2	5	7	Analog input	Analog input 2
AIN3	4	6	Analog input	Analog input 3
AGND	3	5	Analog supply	Negative analog power supply
AVDD	10	12	Analog supply	Positive analog power supply. Connect a 100-nF (or larger) capacitor to AGND.
DGND	2	4	Digital supply	Digital ground
$\overline{\text{DRDY}}$	12	14	Digital output	Data ready, active low. Connect to DVDD using a pullup resistor.
DVDD	11	13	Digital supply	Positive digital power supply. Connect a 100-nF (or larger) capacitor to DGND.
REFN	6	8	Analog input	Negative reference input
REFP	7	9	Analog input	Positive reference input
$\overline{\text{RESET}}$	1	3	Digital input	Reset, active low
SCL	14	16	Digital input	Serial clock input. Connect to DVDD using a pullup resistor.
SDA	13	15	Digital input/output	Serial data input and output. Connect to DVDD using a pullup resistor.
Thermal pad	Pad	—	—	Thermal power pad. Connect to AGND.

(1) See the *Unused Inputs and Outputs* section for details on how to connect unused pins.

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7 Specifications

7.1 Absolute Maximum Ratings

see (1)

		MIN	MAX	UNIT
Power-supply voltage	AVDD to AGND	–0.3	7	V
	DVDD to DGND	–0.3	7	
	AGND to DGND	–2.8	0.3	
Analog input voltage	AIN0, AIN1, AIN2, AIN3, REFP, REFN	AGND – 0.3	AVDD + 0.3	V
Digital input voltage	SCL, SDA, A0, A1, $\overline{DRDY}$, $\overline{RESET}$	DGND – 0.3	7	V
Input current	Continuous, any pin except power-supply pins	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–60	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	Analog power supply	AVDD to AGND	2.3		5.5	V
		AGND to DGND	–0.1	0	0.1	
	Digital power supply	DVDD to DGND	2.3		5.5	V
ANALOG INPUTS (1)						
$V_{(AINx)}$	Absolute input voltage	Gain = 1 and 4	AGND – 0.1		AVDD + 0.1	V
V_{IN}	Differential input voltage	$V_{IN} = V_{AINP} – V_{AINN}$ (2)	$–V_{REF}$ / Gain		V_{REF} / Gain	V
VOLTAGE REFERENCE INPUTS						
V_{REF}	Differential reference input voltage	$V_{REF} = V_{(REFP)} – V_{(REFN)}$	0.75	2.5	AVDD	V
$V_{(REFN)}$	Absolute negative reference voltage		AGND – 0.1		$V_{(REFP)}$ – 0.75	V
$V_{(REFP)}$	Absolute positive reference voltage		$V_{(REFN)}$ + 0.75		AVDD + 0.1	V
DIGITAL INPUTS						
	Input voltage	SCL, SDA, A0, A1, $\overline{DRDY}$, 2.3 V ≤ DVDD < 3.0 V	DGND		DVDD + 0.5	V
		SCL, SDA, A0, A1, $\overline{DRDY}$, 3.0 V ≤ DVDD ≤ 5.5 V	DGND		5.5	
		$\overline{RESET}$	DGND		DVDD	
TEMPERATURE RANGE						
T_A	Operating ambient temperature		–40		125	°C

(1) AINx denotes one of the four available analog inputs. AIN_P and AIN_N denote the positive and negative inputs selected by the MUX.
(2) Excluding the effects of offset and gain error.

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7.4 Thermal Information

THERMAL METRIC[1]		ADS1119		UNIT
		WQFN (RTE)	TSSOP (PW)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	57.7	90.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.0	31.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.9	41.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	1.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19.8	41.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	11.8	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD = 2.3 V to 5.5 V, DVDD = 3.3 V, all data rates, all gains, and internal reference enabled (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
	Absolute input current	V_{IN} = 0 V		±5		nA
	Absolute input current drift	V_{IN} = 0 V		10		pA/°C
	Differential input current	V_{CM} = AVDD / 2, $-V_{REF}$ / Gain ≤ V_{IN} ≤ V_{REF} / Gain		±5		nA
	Differential input current drift	V_{CM} = AVDD / 2, $-V_{REF}$ / Gain ≤ V_{IN} ≤ V_{REF} / Gain		10		pA/°C
SYSTEM PERFORMANCE						
	Resolution (no missing codes)		16			Bits
DR	Data rate			20, 90, 330, 1000		SPS
	Noise (input-referred)[1]	Gain = 1, DR = 20 SPS		62.5		μV_{RMS}
INL	Integral nonlinearity	AVDD = 3.3 V, V_{CM} = AVDD / 2, best fit	–15	4	15	ppm_{FSR}
V_{IO}	Input offset voltage	Differential inputs		±4		µV
	Offset drift vs temperature			0.02	0.1	µV/°C
	Gain error[2]			±0.01%		
	Gain drift vs temperature[2]			0.3	2	ppm/°C
NMRR	Normal-mode rejection ratio	50 Hz ±1 Hz, DR = 20 SPS	78	88		dB
		60 Hz ±1 Hz, DR = 20 SPS	80	88		
CMRR	Common-mode rejection ratio	At dc, gain = 1, AVDD = 3.3 V	90	105		dB
		f_{CM} = 50 Hz or 60 Hz, DR = 20 SPS, AVDD = 3.3 V	105	115		
PSRR	Power-supply rejection ratio	AVDD at dc, V_{CM} = AVDD / 2	85	105		dB
		DVDD at dc, V_{CM} = AVDD / 2	95	115		
INTERNAL VOLTAGE REFERENCE						
V_{REF}	Reference voltage			2.048		V
	Accuracy	T_A = 25°C, TSSOP package	–0.15%	±0.01%	0.15%	
		T_A = 25°C, WQFN package	–0.25%	±0.04%	0.25%	
	Temperature drift			5	30	ppm/°C
	Long-term drift	1000 hours		110		ppm
VOLTAGE REFERENCE INPUTS						
	Reference input current	REFP = V_{REF}, REFN = AGND, AVDD = 3.3 V		±10		nA
INTERNAL OSCILLATOR						
f_{CLK}	Frequency			1.024		MHz
	Accuracy		–2%	±1%	2%	

(1) See the *Noise Performance* section for more information.
(2) Excluding error of voltage reference.

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Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD = 2.3 V to 5.5 V, DVDD = 3.3 V, all data rates, all gains, and internal reference enabled (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS/OUTPUTS						
V_{IL}	Logic input level, low		DGND		0.3 DVDD	V
V_{IH}	Logic input level, high	2.3 V ≤ DVDD < 3.0 V, SCL, SDA, A0, A1, $\overline{DRDY}$	0.7 DVDD		DVDD + 0.5	V
		3.0 V ≤ DVDD ≤ 5.5 V, SCL, SDA, A0, A1, $\overline{DRDY}$	0.7 DVDD		5.5	
		$\overline{RESET}$	0.7 DVDD		DVDD	
V_{hys}	Hysteresis of Schmitt-trigger inputs	Fast-mode, fast-mode plus	0.05 DVDD			V
V_{OL}	Logic output level, low	I_{OL} = 3 mA	DGND	0.15	0.4	V
I_{OL}	Low-level output current	V_{OL} = 0.4 V, standard-mode, fast-mode	3			mA
		V_{OL} = 0.4 V, fast-mode plus	20			
		V_{OL} = 0.6 V, fast-mode	6			
I_i	Input current	DGND + 0.1 V < $V_{Digital\ Input}$ < DVDD – 0.1 V	–10		10	µA
C_i	Capacitance	Each pin			10	pF
ANALOG SUPPLY CURRENT (AVDD = 3.3 V, V_{IN} = 0 V)						
I_{AVDD}	Analog supply current	Power-down mode		0.1	3	µA
		Conversion mode, internal reference selected		250		
		Conversion mode, external reference selected		310		
DIGITAL SUPPLY CURRENT (DVDD = 3.3 V, All Data Rates, I^2C Not Active)						
I_{DVDD}	Digital supply current	Power-down mode		0.3	5	µA
		Conversion mode		65	100	
POWER DISSIPATION (AVDD = DVDD = 3.3 V, All Data Rates, V_{IN} = 0 V, I^2C Not Active)						
P_D	Power dissipation	Conversion mode, internal reference selected		1.04		mW

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7.6 I²C Timing Requirements

over operating ambient temperature range and DVDD = 2.3 V to 5.5 V, bus capacitance = 10 pF to 400 pF, and pullup resistor = 1 kΩ (unless otherwise noted)

			MIN	MAX	UNIT
STANDARD-MODE					
f_{SCL}	SCL clock frequency		0	100	kHz
$t_{HD;STA}$	Hold time, (repeated) START condition. After this period, the first clock pulse is generated.		4		µs
t_{LOW}	Pulse duration, SCL low		4.7		µs
t_{HIGH}	Pulse duration, SCL high		4.0		µs
$t_{SU;STA}$	Setup time, repeated START condition		4.7		µs
$t_{HD;DAT}$	Hold time, data		0		µs
$t_{SU;DAT}$	Setup time, data		250		ns
t_r	Rise time, SCL, SDA			1000	ns
t_f	Fall time, SCL, SDA			250	ns
$t_{SU;STO}$	Setup time, STOP condition		4.0		µs
t_{BUF}	Bus free time, between STOP and START condition		4.7		µs
$t_{VD;DAT}$	Valid time, data			3.45	µs
$t_{VD;ACK}$	Valid time, acknowledge			3.45	µs
FAST-MODE					
f_{SCL}	SCL clock frequency		0	400	kHz
$t_{HD;STA}$	Hold time, (repeated) START condition. After this period, the first clock pulse is generated.		0.6		µs
t_{LOW}	Pulse duration, SCL low		1.3		µs
t_{HIGH}	Pulse duration, SCL high		0.6		µs
$t_{SU;STA}$	Setup time, repeated START condition		0.6		µs
$t_{HD;DAT}$	Hold time, data		0		µs
$t_{SU;DAT}$	Setup time, data		100		ns
t_r	Rise time, SCL, SDA		20	300	ns
t_f	Fall time, SCL, SDA		20 · (DVDD / 5.5 V)	250	ns
$t_{SU;STO}$	Setup time, STOP condition		0.6		µs
t_{BUF}	Bus free time, between STOP and START condition		1.3		µs
$t_{VD;DAT}$	Valid time, data			0.9	µs
$t_{VD;ACK}$	Valid time, acknowledge			0.9	µs
t_{SP}	Pulse width of spikes that must be suppressed by the input filter		0	50	ns
FAST-MODE PLUS					
f_{SCL}	SCL clock frequency		0	1000	kHz
$t_{HD;STA}$	Hold time, (repeated) START condition. After this period, the first clock pulse is generated.		0.26		µs
t_{LOW}	Pulse duration, SCL low		0.5		µs
t_{HIGH}	Pulse duration, SCL high		0.26		µs
$t_{SU;STA}$	Setup time, repeated START condition		0.26		µs
$t_{HD;DAT}$	Hold time, data		0		µs
$t_{SU;DAT}$	Setup time, data		50		ns
t_r	Rise time, SCL, SDA			120	ns
t_f	Fall time, SCL, SDA	Pullup resistor = 350 Ω	20 · (DVDD / 5.5 V)	120	ns
$t_{SU;STO}$	Setup time, STOP condition		0.26		µs
t_{BUF}	Bus free time, between STOP and START condition		0.5		µs
$t_{VD;DAT}$	Valid time, data			0.45	µs
$t_{VD;ACK}$	Valid time, acknowledge			0.45	µs
t_{SP}	Pulse duration of spikes that must be suppressed by the input filter		0	50	ns

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I²C Timing Requirements (continued)

over operating ambient temperature range and DVDD = 2.3 V to 5.5 V, bus capacitance = 10 pF to 400 pF, and pullup resistor = 1 kΩ (unless otherwise noted)

		MIN	MAX	UNIT
$\overline{\text{RESET}}$ PIN				
$t_{w(RSL)}$	Pulse duration, $\overline{\text{RESET}}$ low	250		ns
$t_{d(RSSTA)}$	Delay time, START condition after $\overline{\text{RESET}}$ rising edge(1)	100		ns
$\overline{\text{DRDY}}$ PIN				
$t_{d(DRSTA)}$	Delay time, START condition after $\overline{\text{DRDY}}$ falling edge	0		ns
TIMEOUT				
	Timeout(2)		14000	t_{MOD}

(1) No delay time is required when using the RESET command as long as all I²C timing requirements for the (repeated) START and STOP conditions are met.
(2) See the *Timeout* section for more information.
t_{MOD} = 1 / f_{MOD}. Modulator frequency f_{MOD} = 256 kHz.

7.7 I²C Switching Characteristics

over operating ambient temperature range, DVDD = 2.3 V to 5.5 V, bus capacitance = 10 pF to 400 pF, and pullup resistor = 1 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{w(DRH)}$	Pulse duration, $\overline{\text{DRDY}}$ high(1)		2			t_{MOD}
$t_{p(RDDR)}$	Propagation delay time, RDATA command latched to $\overline{\text{DRDY}}$ rising edge			2		t_{MOD}

(1) t_{MOD} = 1 / f_{MOD}. Modulator frequency f_{MOD} = 256 kHz.

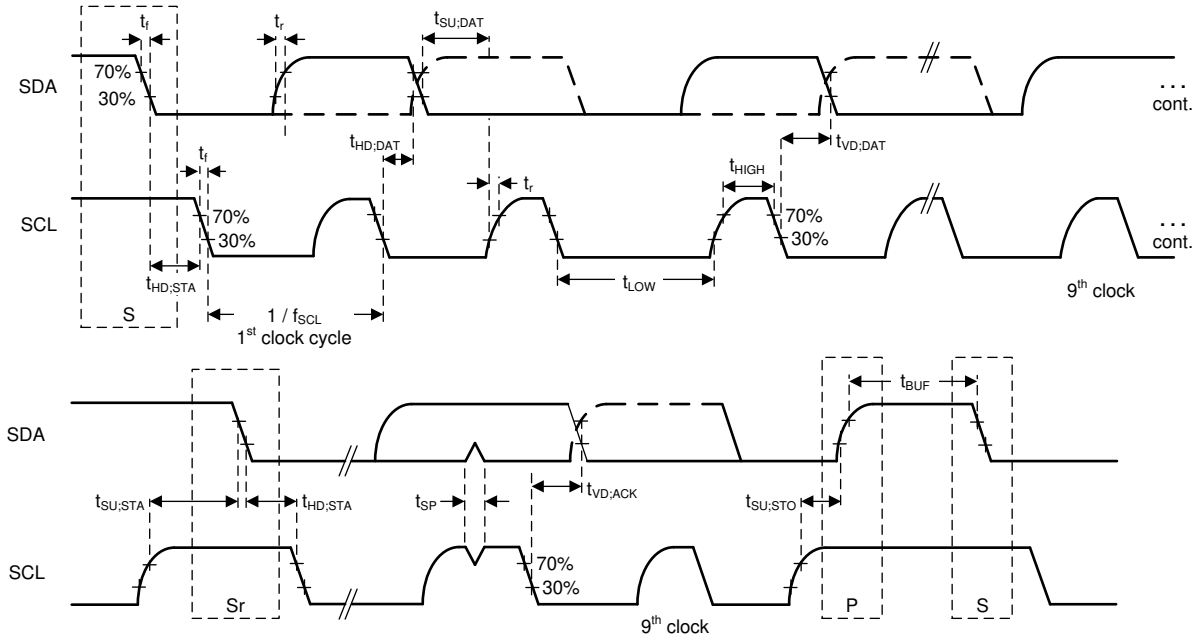

図 1. I²C Timing Requirements

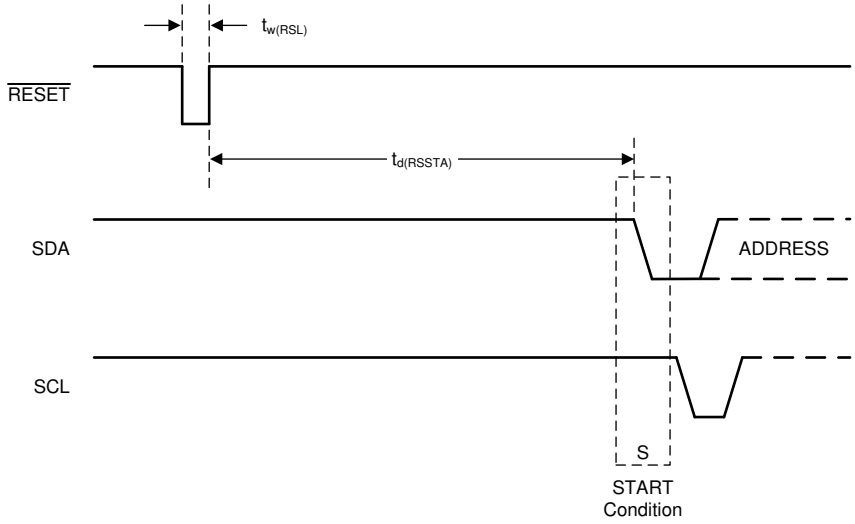

図 2. RESET Pin Timing Requirements

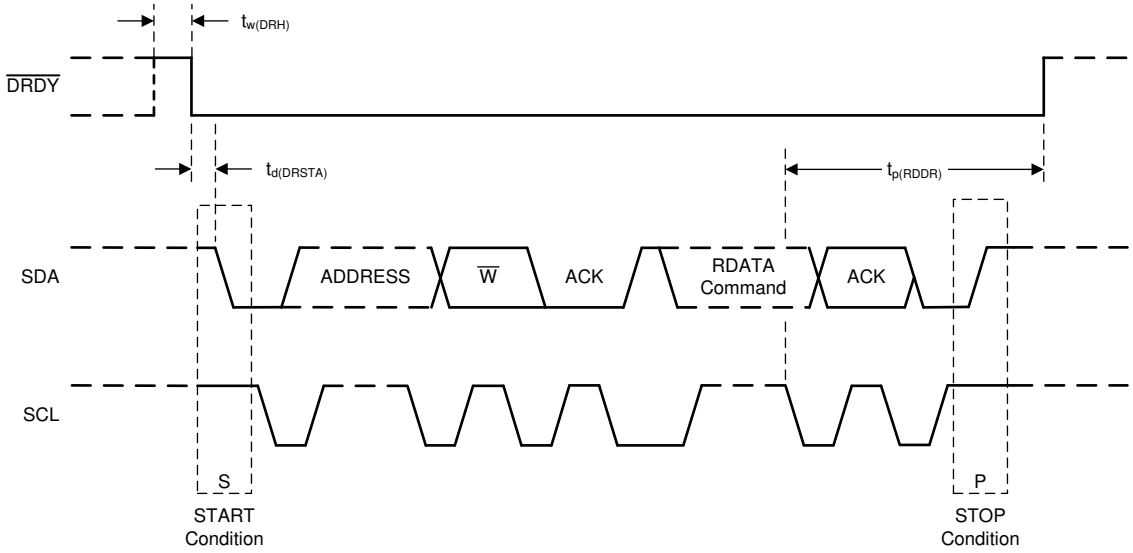

図 3. DRDY Pin Timing Requirements and Switching Characteristics

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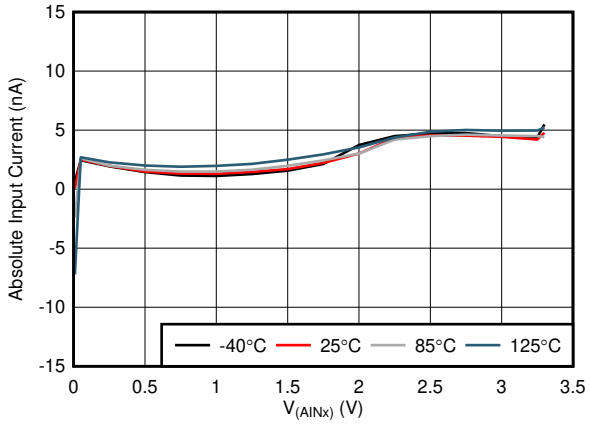
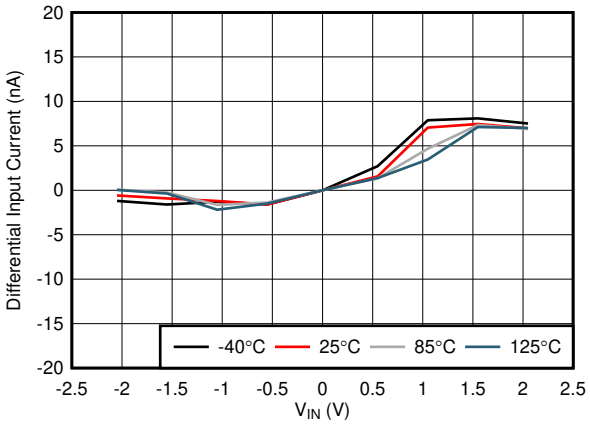
7.8 Typical Characteristics

at T_A = 25°C, AVDD = 3.3 V, and using internal V_{REF} = 2.048 V (unless otherwise noted)



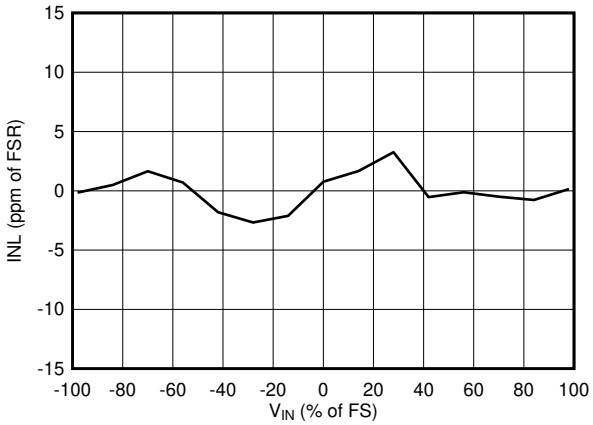
V_{IN} = 0 V

図 4. Absolute Input current vs Absolute Input Voltage



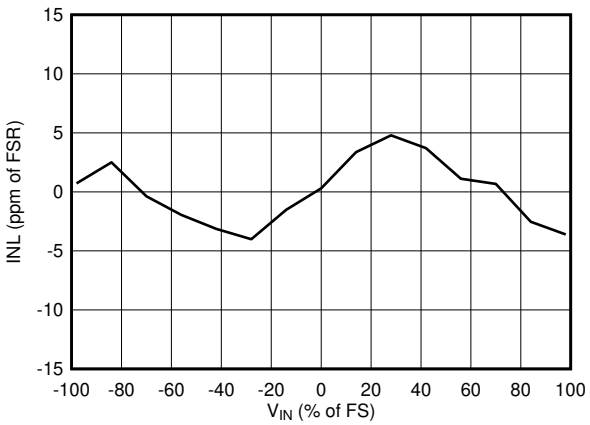
V_{CM} = 1.65 V

図 5. Differential Input Current vs Differential Input Voltage



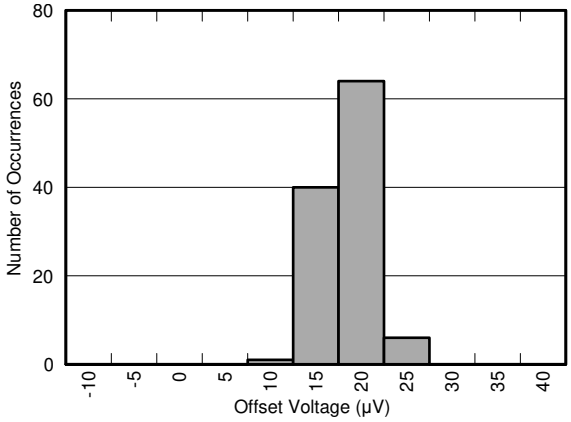
External reference, best fit

図 6. INL vs Differential Input Voltage



Internal reference, best fit

図 7. INL vs Differential Input Voltage



AVDD = 5 V, gain = 1, 110 samples

図 8. Offset Voltage Histogram

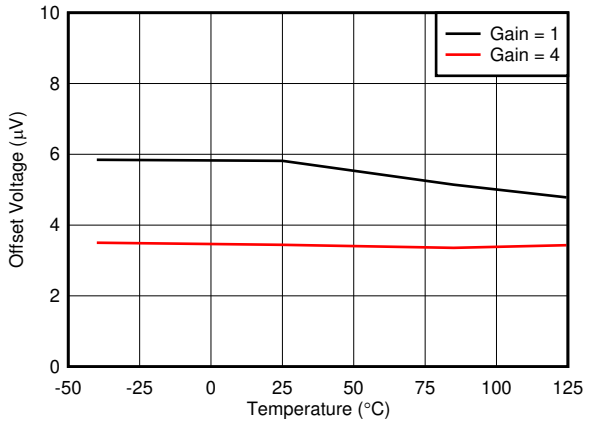


図 9. Input Offset Voltage vs Temperature

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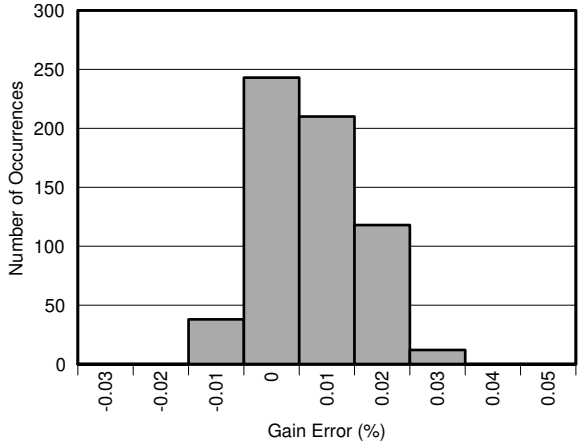
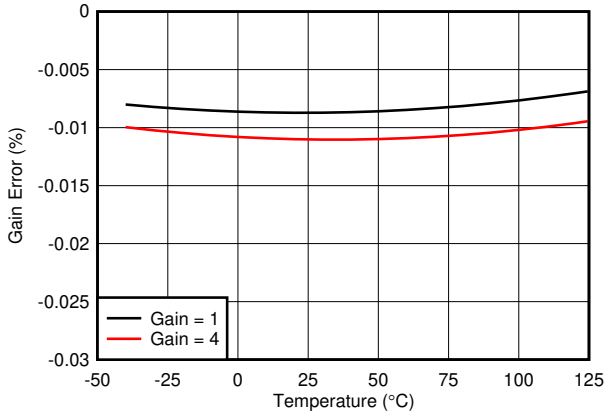
Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, and using internal V_{REF} = 2.048 V (unless otherwise noted)



Gain = 1, 620 samples,
excluding error of voltage reference

図 10. Gain Error Histogram



Excluding error of voltage reference

図 11. Gain Error vs Temperature

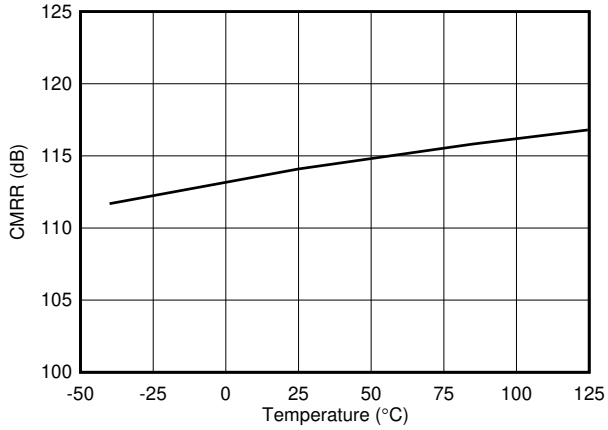
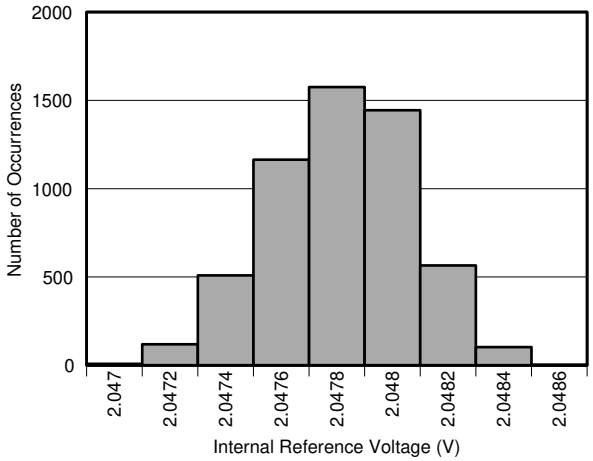


図 12. DC CMRR vs Temperature



5940 samples, TSSOP package

図 13. Internal Reference Voltage Histogram

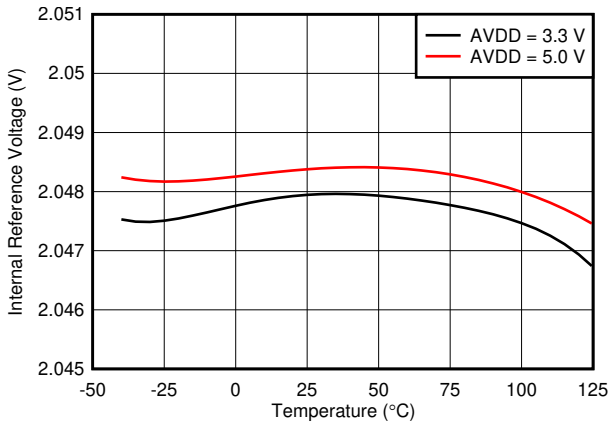


図 14. Internal Reference Voltage vs Temperature

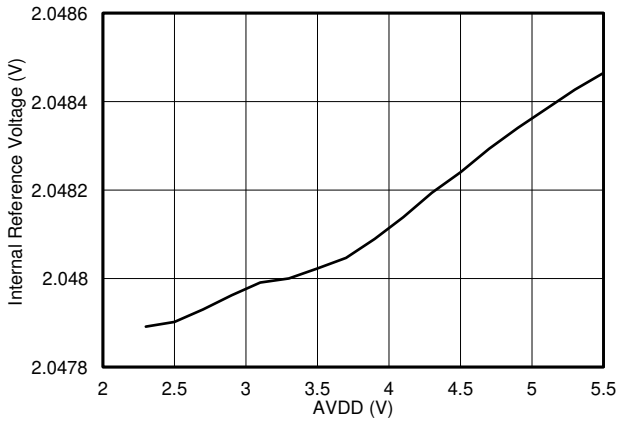


図 15. Internal Reference Voltage vs AVDD

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Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, and using internal V_{REF} = 2.048 V (unless otherwise noted)

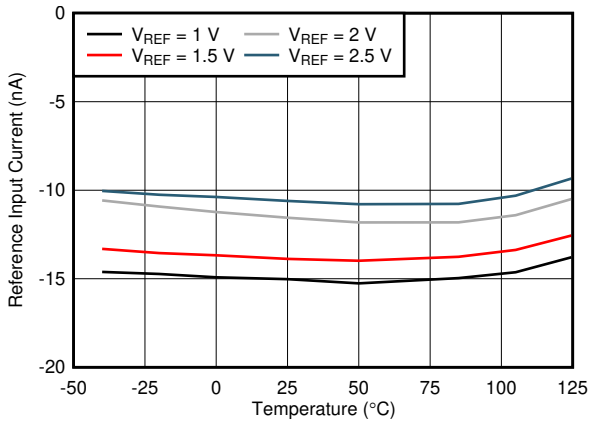

図 16. External Reference Input Current vs Temperature

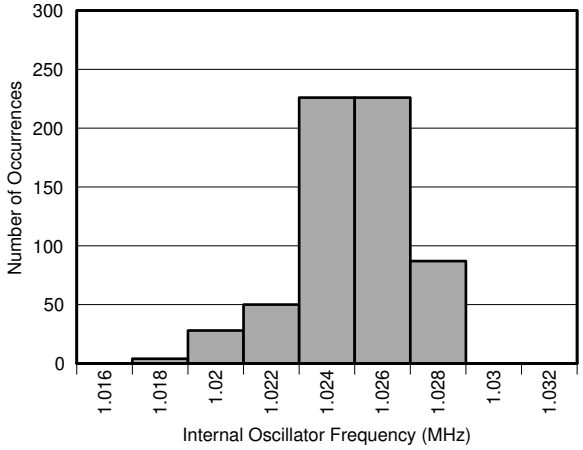

図 17. Internal Oscillator Frequency Histogram

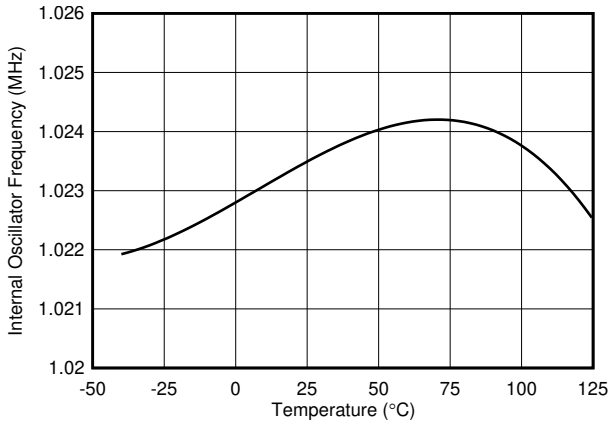

図 18. Internal Oscillator Frequency vs Temperature

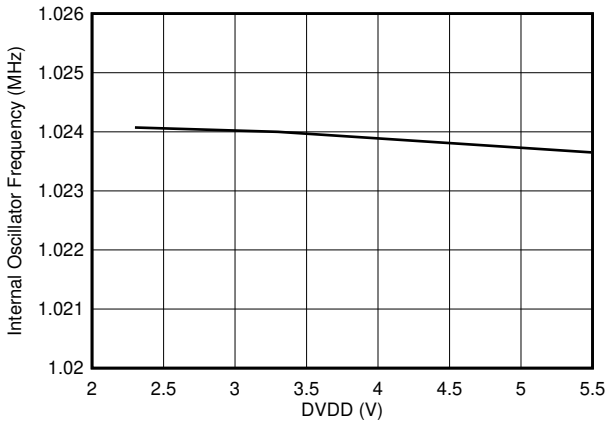

図 19. Internal Oscillator Frequency vs DVDD

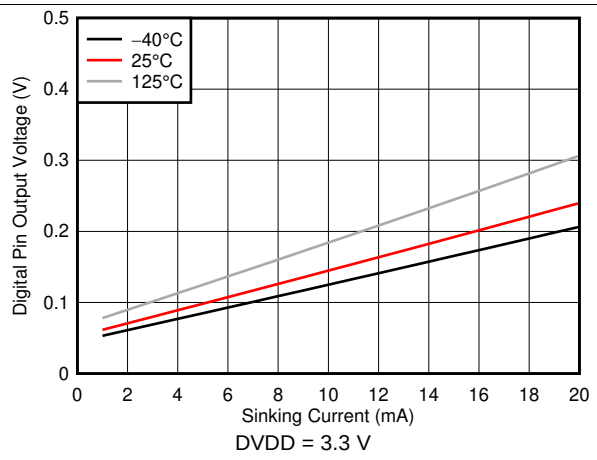

図 20. Digital Pin Output Voltage vs Sinking Current

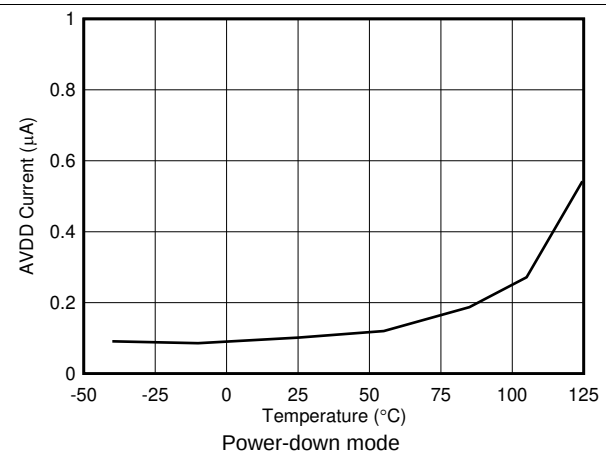

図 21. Analog Supply Current vs Temperature

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Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, and using internal V_{REF} = 2.048 V (unless otherwise noted)

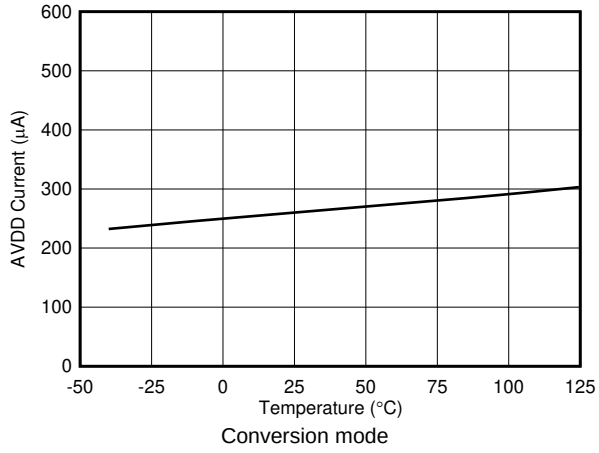

図 22. Analog Supply Current vs Temperature

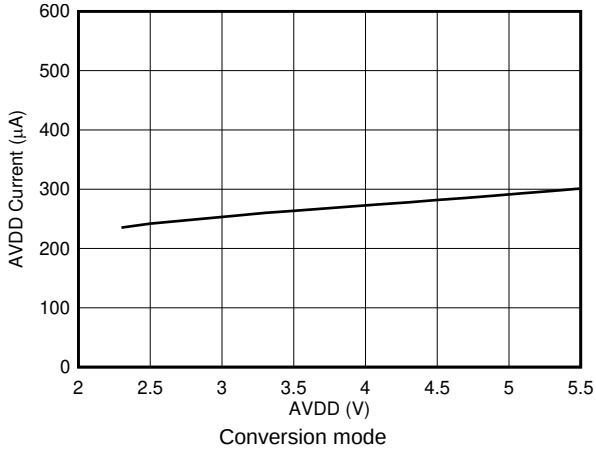

図 23. Analog Supply Current vs AVDD

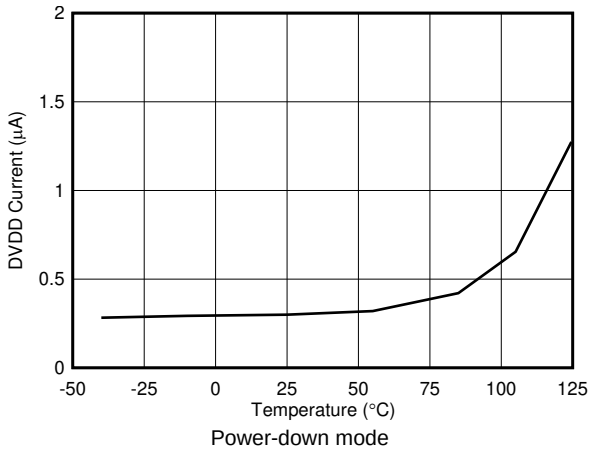

図 24. Digital Supply Current vs Temperature

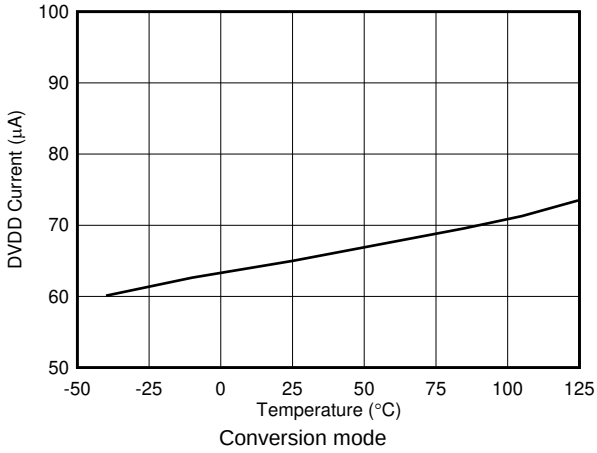

図 25. Digital Supply Current vs Temperature

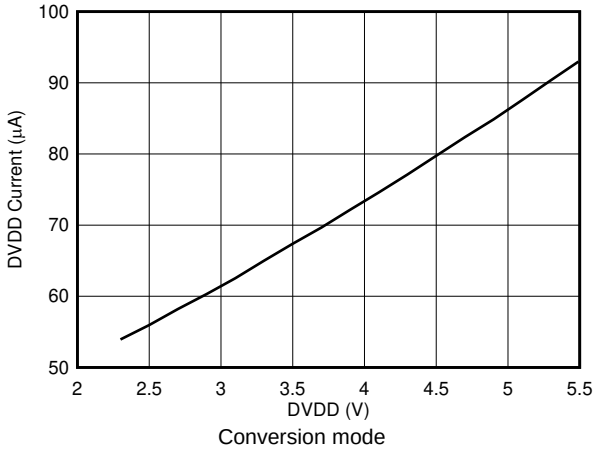

図 26. Digital Supply Current vs DVDD

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8 Parameter Measurement Information

8.1 Noise Performance

Delta-sigma (ΔΣ) analog-to-digital converters (ADCs) are based on the principle of oversampling. The input signal of a ΔΣ ADC is sampled at a high frequency (modulator frequency) and subsequently filtered and decimated in the digital domain to yield a conversion result at the respective output data rate. The ratio between modulator frequency and output data rate is called *oversampling ratio* (OSR). By increasing the OSR, and thus reducing the output data rate, the noise performance of the ADC can be optimized. In other words, the input-referred noise drops when reducing the output data rate because more samples of the internal modulator are averaged to yield one conversion result. Increasing the gain also reduces the input-referred noise, which is particularly useful when measuring low-level signals.

表 1 and 表 2 summarize the device noise performance. Data are representative of typical noise performance at T_A = 25°C using the internal 2.048-V reference. Data shown are the result of averaging readings from a single device over a time period of approximately 0.75 seconds and are measured with the inputs internally shorted together. 表 1 lists the input-referred noise in units of μV_{RMS} for the conditions shown. Values in μV_{PP} are shown in parenthesis. 表 2 lists the corresponding data in effective resolution calculated from μV_{RMS} values using 式 1. Noise-free resolution calculated from peak-to-peak noise values using 式 2 are shown in parenthesis.

The input-referred noise only changes marginally when using an external low-noise reference, such as the REF5020. Use 式 1 and 式 2 to calculate effective resolution numbers and noise-free resolution when using a reference voltage other than 2.048 V:

$$\text{Effective Resolution} = \ln [2 \cdot V_{REF} / (\text{Gain} \cdot V_{RMS\text{-Noise}})] / \ln(2) \quad (1)$$

$$\text{Noise-Free Resolution} = \ln [2 \cdot V_{REF} / (\text{Gain} \cdot V_{PP\text{-Noise}})] / \ln(2) \quad (2)$$

表 1. Noise in μV_{RMS} (μV_{PP}) at AVDD = 3.3 V and Internal V_{REF} = 2.048 V

DATA RATE (SPS)	GAIN	
	1	4
20	62.50 (62.50)	15.63 (15.63)
90	62.50 (62.50)	15.63 (15.63)
330	62.50 (106.06)	15.63 (26.30)
1000	62.50 (221.61)	15.63 (55.07)

表 2. Effective Resolution From RMS Noise (Noise-Free Resolution From Peak-to-Peak Noise) at AVDD = 3.3 V and Internal V_{REF} = 2.048 V

DATA RATE (SPS)	GAIN	
	1	4
20	16 (16)	16 (16)
90	16 (16)	16 (16)
330	16 (15.24)	16 (15.25)
1000	16 (14.17)	16 (14.18)

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9 Detailed Description

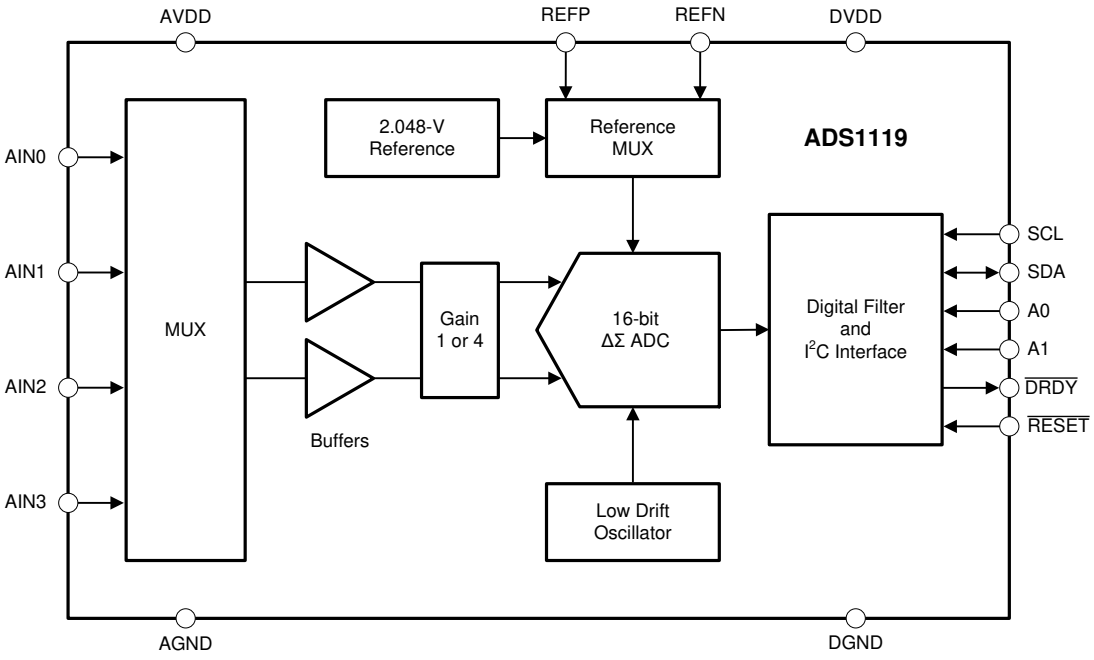
9.1 Overview

The ADS1119 is a small, low-power, 16-bit, ΔΣ ADC. In addition to the ΔΣ ADC core and single-cycle settling digital filter, the device offers a multiplexer (MUX), rail-to-rail input buffers, a programmable gain stage, an internal 2.048-V voltage reference, and a clock oscillator. All of these features are intended to reduce the required external circuitry in typical voltage, current, and temperature monitoring applications. The device is fully configured through a single register and controlled by six commands through an I^2C-compatible interface. The *Functional Block Diagram* section shows the device functional block diagram.

The MUX selects the positive (AIN_P) and negative (AIN_N) signals that feed into the rail-to-rail input buffers. A gain stage with selectable gains of 1 and 4 follows the input buffers. The 16-bit ADC measures the differential signal provided after the gain stage. The converter core consists of a differential, switched-capacitor, ΔΣ modulator followed by a digital filter. The digital filter receives a high-speed bitstream from the modulator and outputs a code proportional to the input voltage. This architecture results in a very strong attenuation of any common-mode signal.

The device has two available conversion modes: single-shot conversion and continuous conversion mode. In single-shot conversion mode, the ADC performs one conversion of the input signal upon request and stores the value in an internal data buffer. The device then enters a low-power state to save power. Single-shot conversion mode is intended to provide significant power savings in systems that require only periodic conversions, or when there are long idle periods between conversions. In continuous conversion mode, the ADC automatically begins a conversion of the input signal as soon as the previous conversion is completed. New data are available at the programmed data rate. Data can be read at any time without concern of data corruption and always reflect the most recently completed conversion.

9.2 Functional Block Diagram



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9.3 Feature Description

9.3.1 Multiplexer

図 27 shows the flexible input multiplexer of the device. Either four single-ended signals, two differential signals, or a combination of two single-ended signals and one differential signal can be measured. The positive (AIN_P) and negative (AIN_N) inputs selected for measurement are configured by three bits (MUX[2:0]) in the configuration register. When single-ended signals need to be measured, the negative ADC input (AIN_N) can internally be connected to AGND by a switch within the multiplexer.

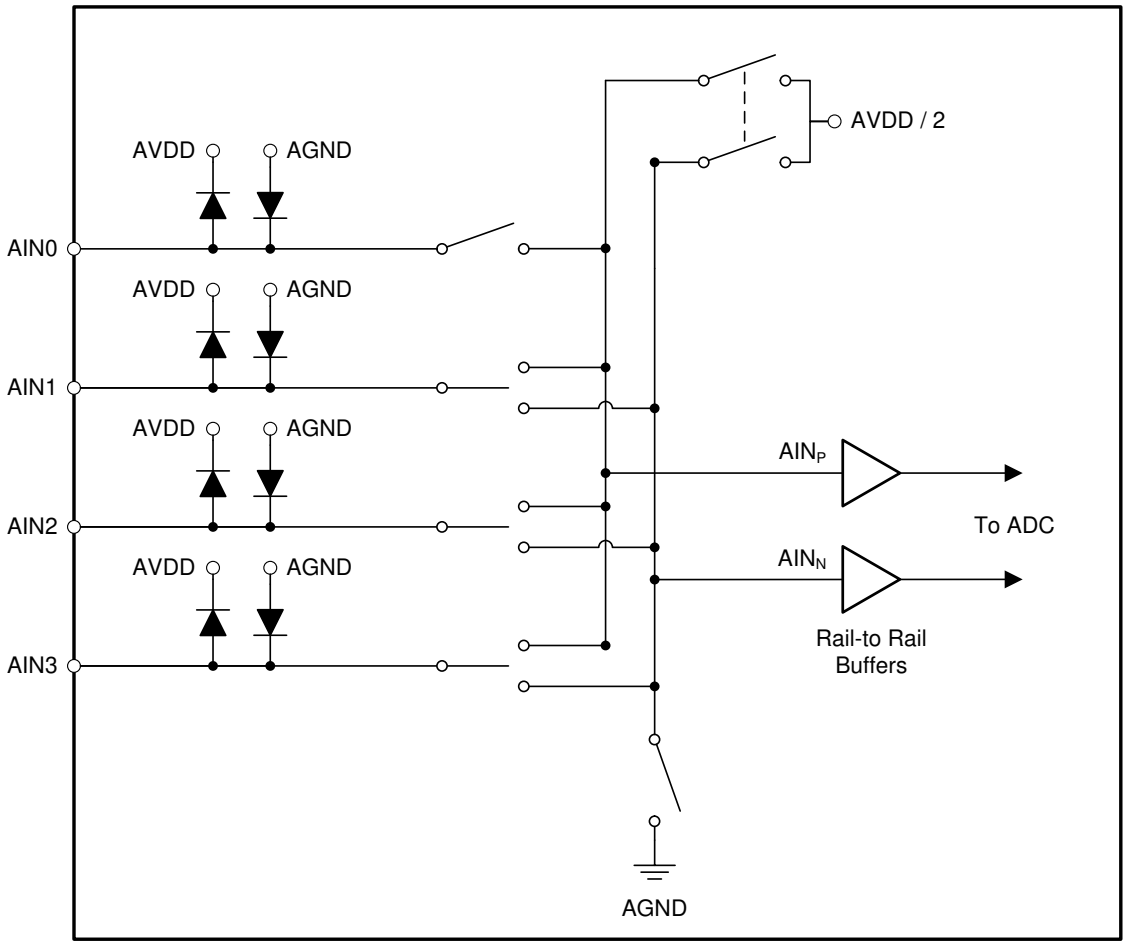

図 27. Analog Input Multiplexer

Electrostatic discharge (ESD) diodes to AVDD and AGND protect the inputs. The absolute voltage on any input must stay within the range provided by 式 3 to prevent the ESD diodes from turning on:

$$AGND - 0.3\ V < V_{(AINx)} < AVDD + 0.3\ V \quad (3)$$

If the voltages on the input pins have any potential to violate these conditions, external Schottky clamp diodes or series resistors may be required to limit the input current to safe values (see the *Absolute Maximum Ratings* table). Overdriving an unused input on the device can affect conversions taking place on other input pins.

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Feature Description (continued)

9.3.2 Rail-to-Rail Input Buffers and Programmable Gain Stage

The ADS1119 integrates two rail-to-rail input buffers to ensure that the effect on the input loading resulting from the capacitor charging and discharging of the ΔΣ ADC is minimal. The buffers therefore help to increase the input impedance of the device. See the *Electrical Characteristics* table for the typical values of absolute input currents (current flowing into or out of each input) and differential input currents (difference in absolute current between the positive and negative input).

The usable absolute input voltage range of the buffers is (AGND – 0.1 V ≤ V_{AINP}, V_{AINN} ≤ AVDD + 0.1 V). V_{IN} denotes the differential input voltage $V_{IN} = V_{AINP} – V_{AINN}$ between the buffer inputs.

A programmable gain stage follows the buffers. The GAIN bit in the configuration register is used to configure the gain to either 1 or 4.

式 4 shows that the differential full-scale input voltage range (FSR) of the device is defined by the gain setting and the reference voltage used:

$$FSR = \pm V_{REF} / Gain \quad (4)$$

表 3 shows the corresponding full-scale ranges and least significant bit (LSB) sizes when using the internal 2.048-V reference.

表 3. Full-Scale Range and LSB Size

GAIN SETTING	FSR	LSB SIZE
1	±2.048 V	62.50 µV
4	±0.512 V	15.63 µV

In order to measure single-ended signals that are referenced to AGND ($AIN_P = V_{IN}$, AIN_N = AGND), connect one of the analog inputs to AGND externally or use the internal AGND connection of the multiplexer (MUX[2:0] settings 011 through 110). The device only uses the code range that represents positive differential voltages when measuring single-ended signals. See the *Data Format* section for more details.

For signal sources with high output impedance, external buffering may still be necessary. Active buffers can introduce noise as well as offset and gain errors. Consider all of these factors in high-accuracy applications.

9.3.3 Voltage Reference

The device offers an integrated, low-drift, 2.048-V reference. For applications that require a different reference voltage value or a ratiometric measurement approach, the device offers a differential reference input pair (REFP and REFN).

The reference source is selected by the VREF bit in the configuration register. By default, the internal reference is selected. The internal voltage reference requires less than 25 µs to fully settle after power-up, when coming out of power-down mode, or when switching from the external reference source to the internal reference.

The differential reference input allows freedom in the reference common-mode voltage. The reference inputs are internally buffered to increase input impedance. Therefore, additional reference buffers are usually not required when using an external reference. When used in ratiometric applications, the reference inputs do not load the external circuitry; however, the analog supply current increases when using an external reference because the reference buffers are enabled.

In most cases the conversion result is directly proportional to the stability of the reference source. Any noise and drift of the voltage reference is reflected in the conversion result.

9.3.4 Modulator and Internal Oscillator

A ΔΣ modulator is used in the ADS1119 to convert the differential signal provided by the gain stage into a pulse code modulated (PCM) data stream. The modulator runs at a modulator clock frequency of $f_{MOD} = f_{CLK} / 4$ = 256 kHz, where f_{CLK} is provided by the internal 1.024-MHz oscillator.

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9.3.5 Digital Filter

The device uses a linear-phase finite impulse response (FIR) digital filter that performs both filtering and decimation of the digital data stream coming from the modulator. The digital filter is automatically adjusted for the different data rates and always settles within a single cycle. The frequency responses of the digital filter are shown in 図 28 to 図 32 for different output data rates. The filter notches and output data rate scale proportionally with the clock frequency. The internal oscillator can vary over temperature as specified in the *Electrical Characteristics* table. The data rate or conversion time, respectively, and consequently also the filter notches vary proportionally.

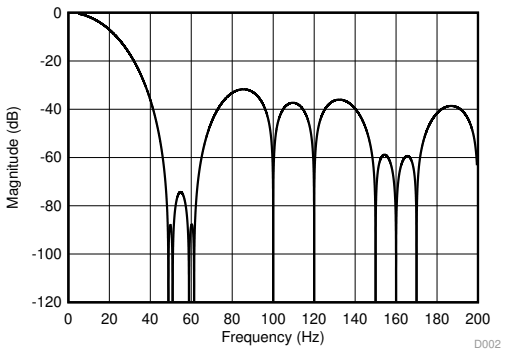

図 28. Filter Response (DR = 20 SPS)

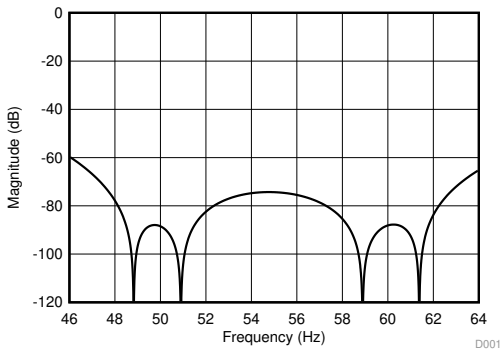

図 29. Detailed View of the Filter Response (DR = 20 SPS)

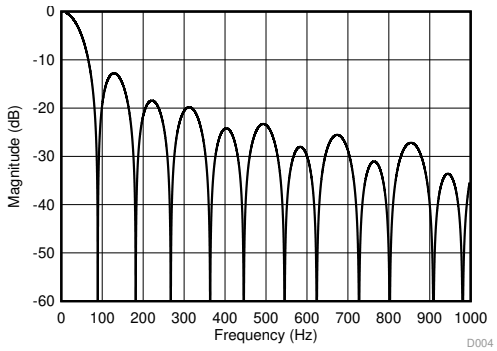

図 30. Filter Response (DR = 90 SPS)

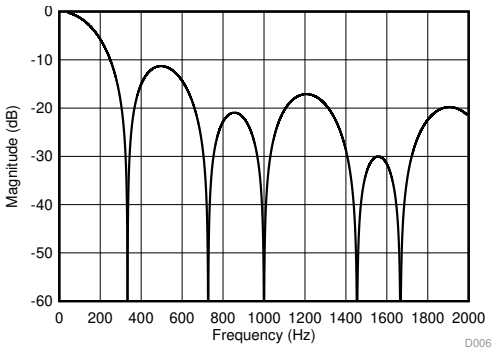

図 31. Filter Response (DR = 330 SPS)

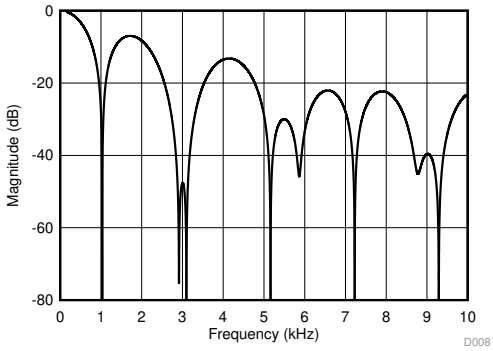

図 32. Filter Response (DR = 1 kSPS)

9.3.6 Conversion Times

表 4 shows the actual conversion times for each data rate setting. The values provided are in terms of t_{CLK} cycles and in milliseconds.

Continuous conversion mode data rates are timed from one $\overline{DRDY}$ falling edge to the next $\overline{DRDY}$ falling edge. The first conversion starts 28.5 · t_{CLK} after the START/SYNC command is latched.

Single-shot conversion mode data rates are timed from when the START/SYNC command is latched to the $\overline{DRDY}$ falling edge and rounded to the next t_{CLK}.

Commands are latched on the eighth falling edge of SCL in the command byte.

表 4. Conversion Times

NOMINAL DATA RATE (SPS)	–3-dB BANDWIDTH (Hz)	CONTINUOUS CONVERSION MODE(1)		SINGLE-SHOT CONVERSION MODE	
		ACTUAL CONVERSION TIME (t_{CLK})(2)	ACTUAL CONVERSION TIME (ms)	ACTUAL CONVERSION TIME (t_{CLK})(2)	ACTUAL CONVERSION TIME (ms)
20	13.1	51192	49.99	51213	50.01
90	39.6	11532	11.26	11557	11.29
330	150.1	3116	3.04	3141	3.07
1000	483.8	1036	1.01	1061	1.04

(1) The first conversion starts 28.5 · t_{CLK} after the START/SYNC command is latched. The times listed in this table do not include that time.
(2) t_{CLK} = 1 / f_{CLK}. f_{CLK} = 1.024 MHz.

Although the conversion time at the 20-SPS setting is not exactly 1 / 20 Hz = 50 ms, this discrepancy does not affect the 50-Hz or 60-Hz rejection. The conversion time and filter notches vary by the amount specified in the *Electrical Characteristics* table for oscillator accuracy.

9.3.7 Offset Calibration

The ADS1119 does not offer any self-calibration options. However the internal multiplexer offers the option to short both inputs (AIN_P and AIN_N) to mid-supply AVDD / 2. This option can be used to measure and calibrate the device offset voltage by storing the result of the shorted input voltage reading in a microcontroller and consequently subtracting the result from each following reading. Take multiple readings with the inputs shorted and average the result to reduce the effect of noise.

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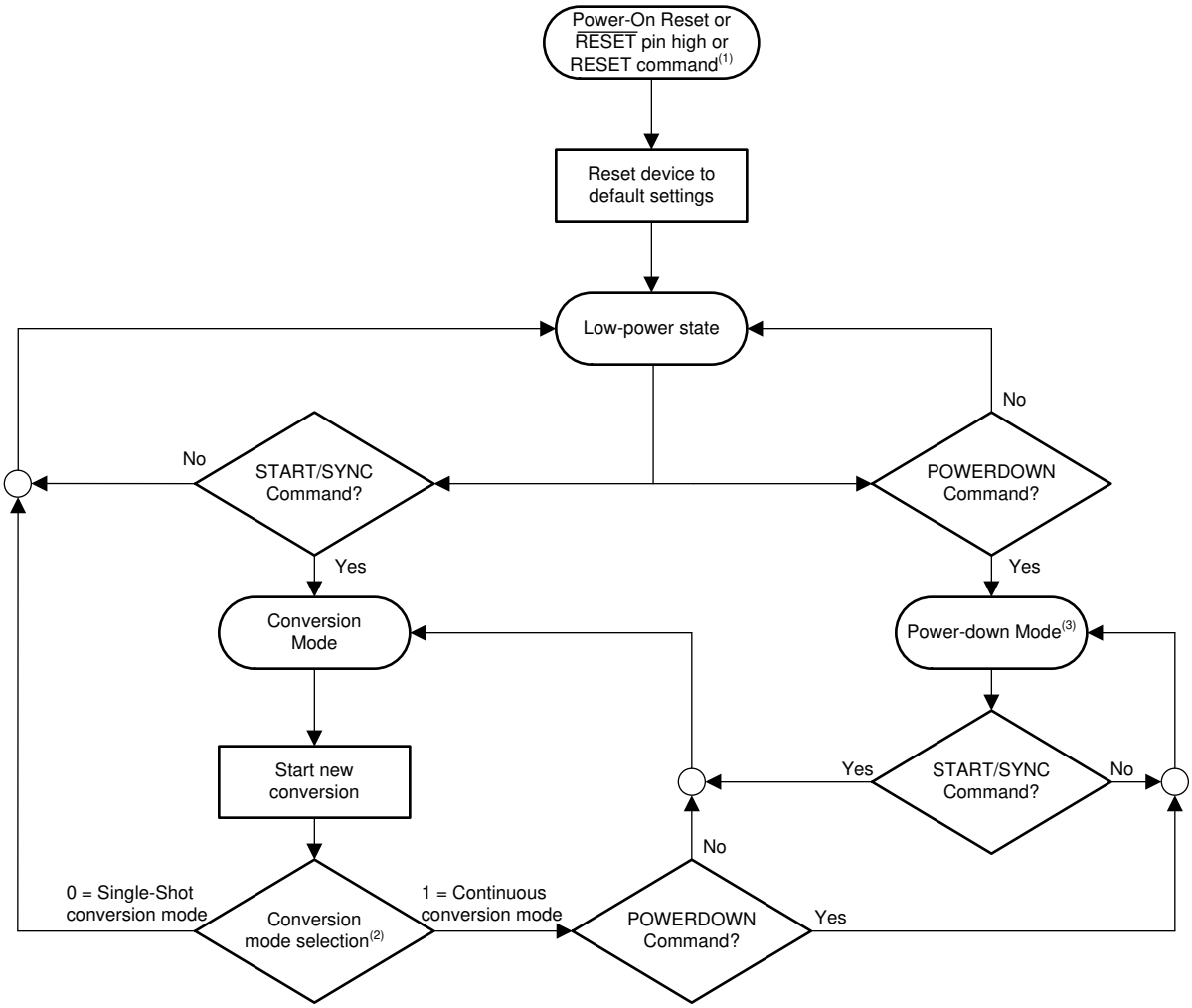
9.4 Device Functional Modes

図 33 shows a flow chart of the different operating modes and how the device transitions from one mode to another.



(1) Any reset (power-on, command, or pin) immediately resets the device.

(2) The conversion mode is selected with the CM bit in the configuration register.

(3) The POWERDOWN command allows any ongoing conversion to complete before placing the device in power-down mode.

図 33. Operating Flow Chart

9.4.1 Power-Up and Reset

The ADS1119 is reset in one of three ways: either by a power-on reset, by the $\overline{\text{RESET}}$ pin, or by a RESET command.

When a reset occurs, the configuration register resets to the default values and the device enters a low-power state. The device then waits for the START/SYNC command to enter conversion mode; see the *I^2C Timing Requirements* table for reset timing information.

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Device Functional Modes (continued)

9.4.1.1 Power-On Reset

During power up, the device is held in reset. The power-on reset releases approximately 500 µs after both supplies have exceeded their respective power-up reset thresholds. After this time all internal circuitry (including the voltage reference) are stable and communication with the device is possible. As part of the power-on reset process, the device sets all bits in the configuration register to the respective default settings. After power-up, the device enters a low-power state. This power-up behavior is intended to prevent systems with tight power-supply requirements from encountering a current surge during power-up.

9.4.1.2 $\overline{\text{RESET}}$ Pin

Reset the ADC by taking the $\overline{\text{RESET}}$ pin low for a minimum of $t_{w(RSL)}$ and then returning the pin high. After the rising edge of the $\overline{\text{RESET}}$ pin, a delay time of $t_{d(RSSTA)}$ is required before communicating with the device; see the *I^2C Timing Requirements* table for reset timing information.

9.4.1.3 Reset by Command

Reset the ADC by using the RESET command (06h or 07h). No delay time is required after the RESET command is latched before starting to communicate with the device as long as the timing requirements (see the *I^2C Timing Requirements* table) for the (repeated) START and STOP conditions are met. Alternatively, the device also responds to the I^2C general-call software reset.

9.4.2 Conversion Modes

The device operates in one of two conversion modes that are selected by the CM bit in the configuration register. These conversion modes are single-shot conversion and continuous conversion mode. A START/SYNC command must be issued each time the CM bit is changed.

9.4.2.1 Single-Shot Conversion Mode

In single-shot conversion mode, the device only performs a conversion when a START/SYNC command is issued. The device consequently performs one single conversion and returns to a low-power state afterwards. The internal oscillator and all analog circuitry are turned off while the device waits in this low-power state until the next conversion is started. Writing to the configuration register when a conversion is ongoing functions as a new START/SYNC command that stops the current conversion and restarts a single new conversion. Each conversion is fully settled (assuming the analog input signal settles to the final value before the conversion starts) because the device digital filter settles within a single cycle.

9.4.2.2 Continuous Conversion Mode

In continuous conversion mode, the device continuously performs conversions. When a conversion completes, the device places the result in the output buffer and immediately begins another conversion.

In order to start continuous conversion mode, the CM bit must be set to 1 followed by a START/SYNC command. The first conversion starts $28.5 \cdot t_{CLK}$ after the START/SYNC command is latched. Writing to the configuration register during an ongoing conversion restarts the current conversion. Send a START/SYNC command immediately after the CM bit is set to 1.

Stop continuous conversions by sending the POWERDOWN command.

9.4.3 Power-Down Mode

When the POWERDOWN command is issued, the device enters power-down mode after completing the current conversion. In this mode, all analog circuitry (including the voltage reference) are powered down and the device typically only uses 400 nA of current. When in power-down mode, the device holds the configuration register settings and responds to commands, but does not perform any data conversions.

Issuing a START/SYNC command wakes up the device and either starts a single conversion or starts continuous conversion mode, depending on the conversion mode selected by the CM bit.

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9.5 Programming

9.5.1 I²C Interface

The ADS1119 uses an I²C-compatible (inter-integrated circuit) interface for serial communication. I²C is a 2-wire communication interface that allows communication of a master device with multiple slave devices on the same bus through the use of device addressing. Each slave device on an I²C bus must have a unique address. Communication on the I²C bus always takes place between two devices: one acting as the master and the other as the slave. Both the master and slave can receive and transmit data, but the slave can only read or write under the direction of the master. The ADS1119 always acts as an I²C slave device.

An I²C bus consists of two lines: SDA and SCL. SDA carries data and SCL provides the clock. Devices on the I²C bus drive the bus lines low by connecting the lines to ground; the devices never drive the bus lines high. Instead, the bus wires are pulled high by pullup resistors; thus, the bus wires are always high when a device is not driving the lines low. As a result of this configuration, two devices do not conflict. If two devices drive the bus simultaneously, there is no driver contention.

See the *I²C-Bus Specification and User Manual* from NXP Semiconductors™ for more details.

9.5.1.1 I²C Address

The ADS1119 has two address pins: A0 and A1. Each address pin can be tied to either DGND, DVDD, SDA, or SCL, providing 16 possible unique addresses. This configuration allows up to 16 different ADS1119 devices to be present on the same I²C bus. 表 5 shows the truth table for the I²C addresses for the possible address pin connections.

At the start of every transaction, that is between the START condition (first falling edge of SDA) and the first falling SCL edge of the address byte, the ADS1119 decodes its address configuration again.

表 5. I²C Address Truth Table

A1	A0	I²C ADDRESS
DGND	DGND	100 0000
DGND	DVDD	100 0001
DGND	SDA	100 0010
DGND	SCL	100 0011
DVDD	DGND	100 0100
DVDD	DVDD	100 0101
DVDD	SDA	100 0110
DVDD	SCL	100 0111
SDA	DGND	100 1000
SDA	DVDD	100 1001
SDA	SDA	100 1010
SDA	SCL	100 1011
SCL	DGND	100 1100
SCL	DVDD	100 1101
SCL	SDA	100 1110
SCL	SCL	100 1111

9.5.1.2 Serial Clock (SCL) and Serial Data (SDA)

The serial clock (SCL) line is used to clock data in and out of the device. The master always drives the clock line. The ADS1119 cannot act as a master and as a result can never drive SCL.

The serial data (SDA) line allows for bidirectional communication between the host (the master) and the ADS1119 (the slave). When the master reads from a ADS1119, the ADS1119 drives the data line; when the master writes to a ADS1119, the master drives the data line.

Data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the SCL line is low. One clock pulse is generated for each data bit transferred. When in an idle state, the master should hold SCL high.

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9.5.1.3 Data Ready (DRDY)

DRDY is an open-drain output pin that indicates when a new conversion result is ready for retrieval. When DRDY falls low, new conversion data are ready. DRDY transitions back high when the conversion result is latched for output transmission. In case a conversion result in continuous conversion mode is not read, DRDY releases high for $t_{w(DRH)}$ before the next conversion completes. See the *I²C Timing Requirements* table for more details.

9.5.1.4 Interface Speed

The ADS1119 supports I²C interface speeds up to 1 Mbps. Standard-mode (Sm) with bit rates up to 100 kbps, fast-mode (Fm) with bit rates up to 400 kbps, and fast-mode plus (Fm+) with bit rates up to 1 Mbps are supported. High-speed mode (Hs-mode) is not supported.

9.5.1.5 Data Transfer Protocol

図 34 shows the format of the data transfer. The master initiates all transactions with the ADS1119 by generating a START (S) condition. A high-to-low transition on the SDA line while SCL is high defines a START condition. The bus is considered to be busy after the START condition.

Following the START condition, the master sends the 7-bit slave address corresponding to the address of the ADS1119 that the master wants to communicate with. The master then sends an eighth bit that is a data direction bit (R/W). An R/W bit of 0 indicates a write operation, and an R/W bit of 1 indicates a read operation. After the R/W bit, the master generates a ninth SCLK pulse and releases the SDA line to allow the ADS1119 to acknowledge (ACK) the reception of the slave address by pulling SDA low. In case the device does not recognize the slave address, the ADS1119 holds SDA high to indicate a not acknowledge (NACK) signal.

Next follows the data transmission. If the transaction is a read (R/W = 1), the ADS1119 outputs data on SDA. If the transaction is a write (R/W = 0), the host outputs data on SDA. Data are transferred byte-wise, most significant bit (MSB) first. The number of bytes that can be transmitted per transfer is unrestricted. Each byte must be acknowledged (via the ACK bit) by the receiver. If the transaction is a read, the master issues the ACK. If the transaction is a write, the ADS1119 issues the ACK.

The master terminates all transactions by generating a STOP (P) condition. A low-to-high transition on the SDA line while SCL is high defines a STOP condition. The bus is considered free again t_{BUF} (bus-free time) after the STOP condition.

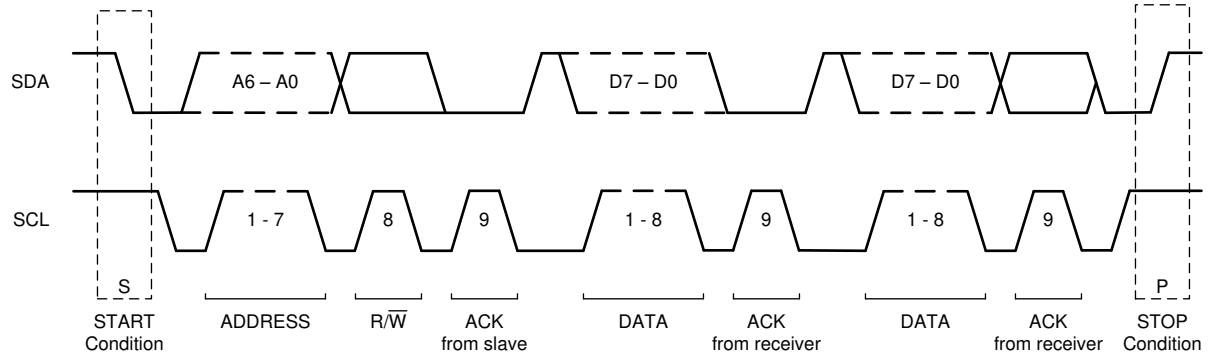

図 34. I²C Data Transfer Format

9.5.1.6 I²C General Call (Software Reset)

The ADS1119 responds to the I²C general-call address (0000 000) if the R/W bit is 0. The device acknowledges the general-call address and, if the next byte is 06h, performs a reset. The general-call software reset has the same effect as the RESET command.

9.5.1.7 Timeout

The ADS1119 offers a I²C timeout feature that can be used to recover communication when a serial interface transmission is interrupted. If the host initiates contact with the ADS1119 but subsequently remains idle for $14000 \cdot t_{MOD}$ before completing a command, the ADS1119 interface is reset. If the ADS1119 interface resets because of a timeout condition, the host must abort the transaction and restart the communication again by issuing a new START condition.

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9.5.2 Data Format

The device provides 16 bits of data in binary two's complement format. Use 式 5 to calculate the size of one code (LSB).

$$1\ \text{LSB} = (2 \cdot V_{REF} / \text{Gain}) / 2^{16} = +\text{FS} / 2^{15} \quad (5)$$

A positive full-scale input [$V_{IN} \geq (+\text{FS} - 1\ \text{LSB}) = (V_{REF} / \text{Gain} - 1\ \text{LSB})$] produces an output code of 7FFFh and a negative full-scale input ($V_{IN} \leq -\text{FS} = -V_{REF} / \text{Gain}$) produces an output code of 8000h. The output clips at these codes for signals that exceed full-scale.

表 6 summarizes the ideal output codes for different input signals.

表 6. Ideal Output Code versus Input Signal

INPUT SIGNAL, $V_{IN} = V_{AINP} - V_{AINN}$	IDEAL OUTPUT CODE(1)
≥ FS ($2^{15} - 1$) / 2^{15}	7FFFh
FS / 2^{15}	0001h
0	0000h
–FS / 2^{15}	FFFFh
≤ –FS	8000h

(1) Excludes the effects of noise, INL, offset, and gain errors.

図 35 shows the mapping of the analog input signal to the output codes.

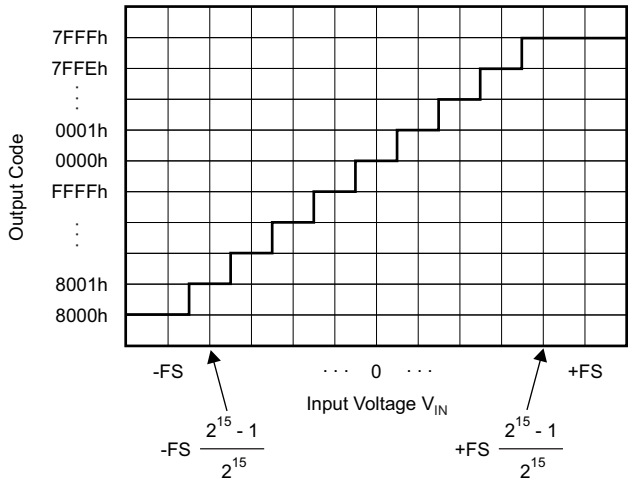

図 35. Code Transition Diagram

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Single-ended signal measurements, where V_{AINN} = 0 V and V_{AINP} = 0 V to +FS, only use the positive code range from 0000h to 7FFFh. However, because of device offset, the ADS1119 can still output negative codes when V_{AINP} is close to 0 V.

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9.5.3 Commands

As 表 7 shows, the device offers six different commands to control device operation. Four commands are stand-alone instructions (RESET, START/SYNC, POWERDOWN, and RDATA). The commands to read (RREG) and write (WREG) register data from and to the device require additional information as part of the instruction.

表 7. Command Definitions

COMMAND	DESCRIPTION	COMMAND BYTE(1)
RESET	Reset the device	0000 011x
START/SYNC	Start or restart conversions	0000 100x
POWERDOWN	Enter power-down mode	0000 001x
RDATA	Read data by command	0001 xxxx
RREG	Read register at address *r*	0010 0rxx
WREG	Write configuration register	0100 00xx

(1) Operands: r = register address (0 or 1), x = don't care.

9.5.3.1 Command Latching

Commands are not processed until latched by the ADS1119. Commands are latched on the eighth falling edge of SCL in the command byte.

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The legend for 図 36 to 図 40:

From master to slave

From slave to master

S = START condition
Sr = Repeated START condition
P = STOP condition
A = acknowledge (SDA low)
$\overline{A}$ = not acknowledge (SDA high)

9.5.3.2 RESET (0000 011x)

This command resets the device to the default states. No delay time is required after the RESET command is latched before starting to communicate with the device as long as the timing requirements (see the *I^2C Timing Requirements* table) for the (repeated) START and STOP conditions are met.

9.5.3.3 START/SYNC (0000 100x)

In single-shot conversion mode, the START/SYNC command is used to start a single conversion, or (when sent during an ongoing conversion) to reset the digital filter and then restart a single new conversion. When the device is set to continuous conversion mode, the START/SYNC command must be issued one time to start converting continuously. Sending the START/SYNC command when converting in continuous conversion mode resets the digital filter and restarts continuous conversions.

9.5.3.4 POWERDOWN (0000 001x)

The POWERDOWN command places the device into power-down mode. This command shuts down all internal analog components, but holds all register values. In case the POWERDOWN command is issued when a conversion is ongoing, the conversion completes before the ADS1119 enters power-down mode. As soon as a START/SYNC command is issued, all analog components return to their previous states.

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9.5.3.5 RDATA (0001 xxxx)

The RDATA command loads the output shift register with the most recent conversion result. Reading conversion data must be performed as shown in 図 36 by using two I²C communication frames. The first frame is an I²C write operation where the R/W bit at the end of the address byte is 0 to indicate a write. In this frame, the host sends the RDATA command to the ADS1119. The second frame is an I²C read operation where the R/W bit at the end of the address byte is 1 to indicate a read. The ADS1119 reports the latest ADC conversion data in this second I²C frame. If a conversion finishes in the middle of the RDATA command byte, the state of the DRDY pin at the end of the read operation signals whether the old or the new result is loaded. If the old result is loaded, DRDY stays low, indicating that the new result is not read out. The new conversion result loads when DRDY is high.

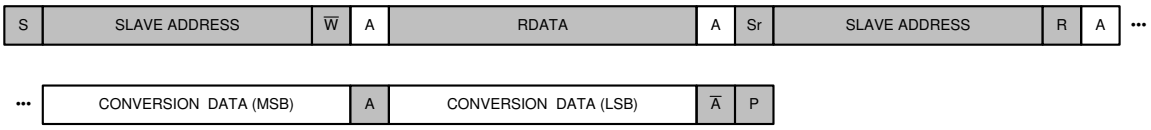

図 36. Read Conversion Data Sequence

9.5.3.6 RREG (0010 0rxx)

The RREG command reads the value of the register at address r. Reading a register must be performed as shown in 図 37 by using two I²C communication frames. The first frame is an I²C write operation where the R/W bit at the end of the address byte is 0 to indicate a write. In this frame, the host sends the RREG command including the register address to the ADS1119. The second frame is an I²C read operation where the R/W bit at the end of the address byte is 1 to indicate a read. The ADS1119 reports the contents of the requested register in this second I²C frame.

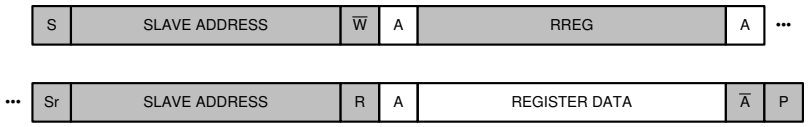

図 37. Read Register Sequence

9.5.3.7 WREG (0100 00xx dddd dddd)

The WREG command writes dddd dddd to the configuration register. 図 38 shows the sequence for writing the configuration register. The R/W bit at the end of the address byte is 0 to indicate a write. The WREG command forces the digital filter to reset and any ongoing ADC conversion to restart.

図 38. Write Register Sequence

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9.5.4 Reading Data and Monitoring for New Conversion Results

Conversion data are read by issuing the RDATA command. The ADS1119 responds to the RDATA command with the latest conversion result. There are two ways to monitor for new conversion data.

One way is to monitor for the falling edge of the $\overline{\text{DRDY}}$ signal. When $\overline{\text{DRDY}}$ falls low, a new conversion result is available for retrieval using the RDATA command. 図 39 shows the timing diagram for collecting data using the $\overline{\text{DRDY}}$ signal to indicate new data.

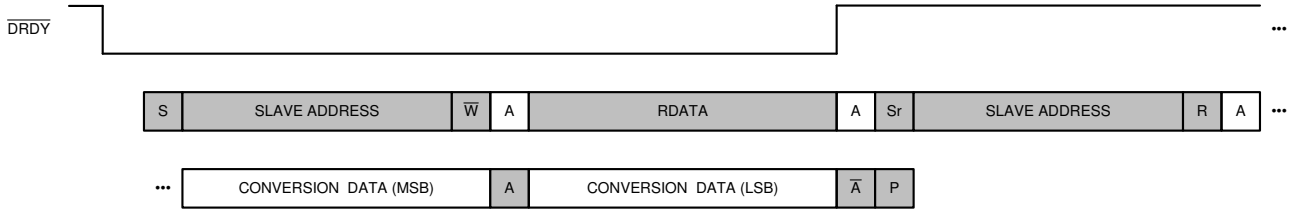

図 39. Using the $\overline{\text{DRDY}}$ Pin to Check for New Conversion Data

Another way to monitor for a new conversion result is to periodically read the DRDY bit in the status register. If set, the DRDY bit indicates that a new conversion result is ready for retrieval. The host can subsequently issue an RDATA command to retrieve the data. The rate at which the host polls the ADS1119 for new data must be at least as fast as the data rate in continuous conversion mode to prevent the host from missing a conversion result.

If a new conversion result becomes ready during an I^2C transmission, the transmission is not corrupted. The new data are loaded into the output shift register upon the following RDATA command.

図 40 shows the timing diagram for collecting data using the DRDY bit in the status register to indicate new data.

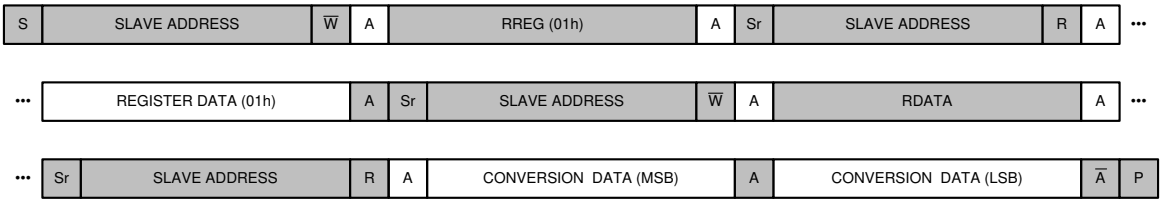

図 40. Using the DRDY Bit to Check for New Conversion Data

9.6 Register Map

9.6.1 Configuration and Status Registers

The device has two 8-bit registers (configuration and status) that are accessible through the I^2C interface using the RREG and WREG commands. After power-up or reset, both registers are set to the default values (which are all 0). All register values are retained during power-down mode. 表 8 shows the register map of the two registers.

表 8. Register Map

REGISTER (Hex)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0h	MUX[2:0]			GAIN	DR[1:0]		CM	VREF
1h	DRDY	ID[6:0]						

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9.6.2 Register Descriptions

表 9 lists the access codes for the ADS1119 registers.

表 9. Register Access Type Codes

Access Type	Code	Description
R	R	Read
R/W	R/W	Read-Write
-n		Value after reset or the default value

9.6.2.1 Configuration Register (address = 0h) [reset = 00h]

図 41. Configuration Register

7	6	5	4	3	2	1	0
MUX[2:0]			GAIN	DR[1:0]		CM	VREF
R/W-0h			R/W-0h	R/W-0h		R/W-0h	R/W-0h

表 10. Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	MUX[2:0]	R/W	0h	**Input multiplexer configuration** These bits configure the input multiplexer. 000 : AIN_P = AIN0, AIN_N = AIN1 (default) 001 : AIN_P = AIN2, AIN_N = AIN3 010 : AIN_P = AIN1, AIN_N = AIN2 011 : AIN_P = AIN0, AIN_N = AGND 100 : AIN_P = AIN1, AIN_N = AGND 101 : AIN_P = AIN2, AIN_N = AGND 110 : AIN_P = AIN3, AIN_N = AGND 111 : AIN_P and AIN_N shorted to AVDD / 2
4	GAIN	R/W	0h	**Gain configuration** This bit configures the device gain. 0 : Gain = 1 (default) 1 : Gain = 4
3:2	DR[1:0]	R/W	0h	**Data rate** These bits control the data rate setting. 00 : 20 SPS (default) 01 : 90 SPS 10 : 330 SPS 11 : 1000 SPS
1	CM	R/W	0h	**Conversion mode** This bit sets the conversion mode for the device. 0 : Single-shot conversion mode (default) 1 : Continuous conversion mode
0	VREF	R/W	0h	**Voltage reference selection** This bit selects the voltage reference source that is used for the conversion. 0 : Internal 2.048-V reference selected (default) 1 : External reference selected using the REFP and REFN inputs

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9.6.2.2 Status Register (address = 1h) [reset = 00h]

図 42. Status Register

7	6	5	4	3	2	1	0
DRDY	RESERVED						
R-0h	R-xxh						

表 11. Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DRDY	R	0h	**Conversion result ready flag** This bit flags if a new conversion result is ready. This bit is reset when conversion data are read. 0 : No new conversion result available (default) 1 : New conversion result ready
6:0	RESERVED	R	xxh	**Reserved** Values are subject to change without notice.

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10 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The ADS1119 is a precision, 16-bit, delta-sigma (ΔΣ), analog-to-digital converter (ADC) that integrates all features required to implement the most common system monitoring functions, such as supply voltage, current, and temperature monitoring. Primary considerations when designing an application with the ADS1119 include analog input filtering, and establishing an appropriate external reference for ratiometric measurements. Connecting and configuring the interface appropriately is another concern. These considerations are discussed in the following sections.

10.1.1 Interface Connections

図 43 shows the principle interface connections for the ADS1119.

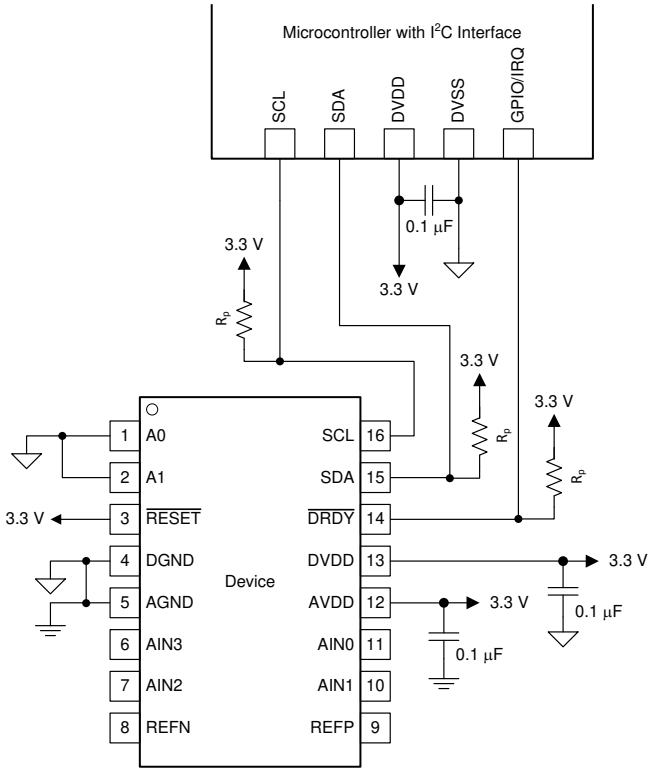

図 43. Interface Connections

The ADS1119 interfaces directly to standard-mode, fast-mode, or fast-mode plus I^2C controllers. Any microcontroller I^2C peripheral, including master-only and single-master I^2C peripherals, operates with the ADS1119. Details of the I^2C communication protocol of the device can be found in the *Programming* section. The ADS1119 does not perform clock-stretching (that is, the device never pulls the clock line low), so this function does not need to be provided for unless other clock-stretching devices are present on the same I^2C bus.

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Application Information (continued)

Pullup resistors are required on both the SDA and SCL lines, as well as on the open-drain $\overline{\text{DRDY}}$ output. The size of these resistors depends on the bus operating speed and capacitance of the bus lines. Higher-value resistors yield lower power consumption when the bus lines are pulled low, but increase the transition times on the bus, which limits the bus speed. Lower-value resistors allow higher interface speeds, but at the expense of higher power consumption when the bus lines are pulled low. Long bus lines have higher capacitance and require smaller pullup resistors to compensate. Do not use resistors that are too small because the bus drivers may be unable to pull the bus lines low. See the *I²C-Bus Specification and User Manual* for details on pullup resistor sizing.

10.1.2 Connecting Multiple Devices on the Same I²C Bus

Up to 16 ADS1119 devices can be connected to a single I²C bus by using different address pin configurations for each device. Use the address pins, A0 and A1, to set the ADS1119 to one of 16 different I²C addresses. 図 44 shows an example with three ADS1119 devices on the same I²C bus. One set of pullup resistors is required per bus line. If needed, decrease the pullup resistor values to compensate for the additional bus capacitance presented by multiple devices and increased line length.

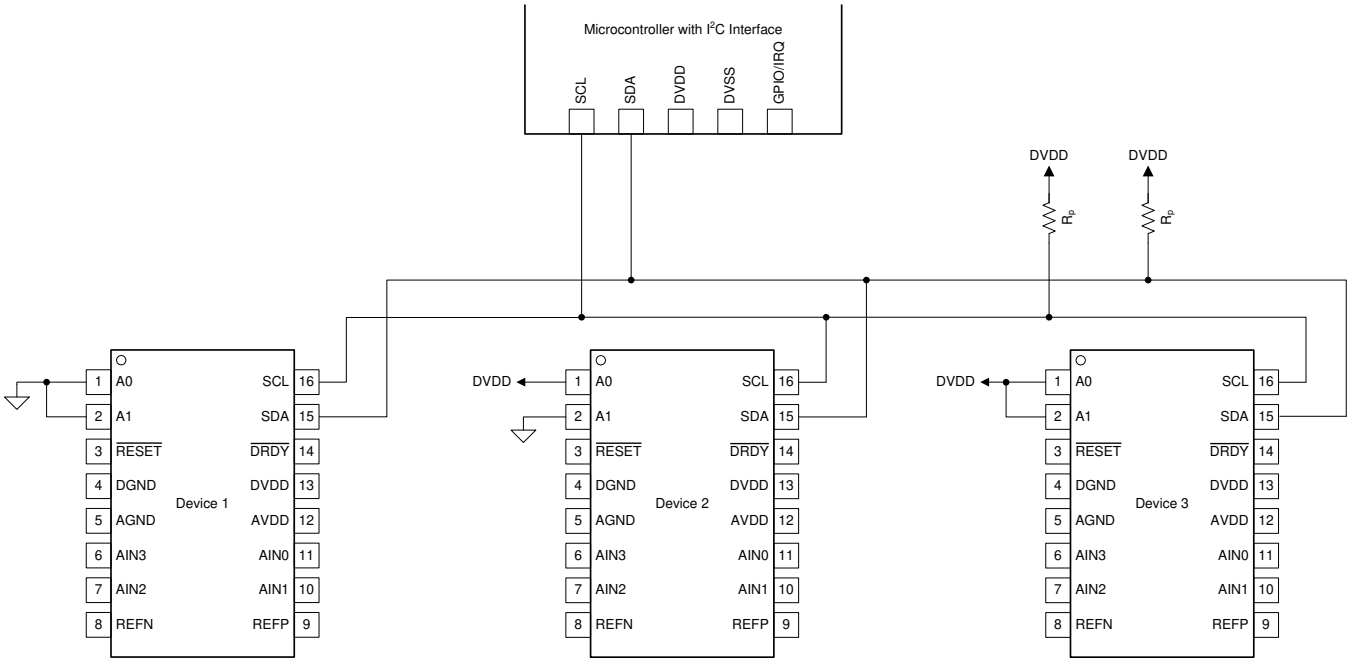

図 44. Connecting Multiple ADS1119 Devices on the Same I²C Bus

10.1.3 Unused Inputs and Outputs

To minimize leakage currents on the analog inputs, leave unused analog and reference inputs floating, or connect the inputs to mid-supply or to AVDD. Connecting unused analog or reference inputs to AGND is possible as well, but can yield higher leakage currents on other analog inputs than the previously mentioned options.

Do not float unused digital inputs; excessive power-supply leakage current can result. Tie all unused digital inputs to the appropriate levels, DVDD or DGND, even when in power-down mode. Connections for unused digital pins are:

- Tie the $\overline{\text{RESET}}$ pin to DVDD if the $\overline{\text{RESET}}$ pin is not used
- If the $\overline{\text{DRDY}}$ output is not used, leave the $\overline{\text{DRDY}}$ pin unconnected or tie the $\overline{\text{DRDY}}$ pin to DVDD using a weak pullup resistor

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Application Information (continued)

10.1.4 Analog Input Filtering

Analog input filtering serves two purposes:

- Limits the effect of aliasing during the ADC sampling process
- Attenuates unwanted noise components outside the bandwidth of interest

In most cases, a first-order resistor capacitor (RC) filter is sufficient to completely eliminate aliasing or to reduce the effect of aliasing to a level within the noise floor of the sensor. A good starting point for a system design with the ADS1119 is to use a differential RC filter with a cutoff frequency set somewhere between the selected output data rate and 25 kHz. Make the series resistor values as small as possible to reduce voltage drops across the resistors caused by the device input currents to a minimum. However, the resistors should be large enough to limit the current into the analog inputs to less than 10 mA in the event of an overvoltage. Then choose the differential capacitor value to achieve the target filter cutoff frequency. Common-mode filter capacitors to GND can be added as well, but should always be at least ten times smaller than the differential filter capacitor.

Internal to the device, prior to the buffer inputs, is an EMI filter. The cutoff frequency of this filter is approximately 31.8 MHz, which helps reject high-frequency interferences.

10.1.5 External Reference and Ratiometric Measurements

The full-scale range (FSR) of the ADS1119 is defined by the reference voltage and the gain setting (FSR = $\pm V_{REF}$ / Gain). An external reference can be used instead of the integrated 2.048-V reference to adapt the FSR to the specific system needs. An external reference must be used if V_{IN} is greater than 2.048 V. For example, an external 5-V reference and an AVDD = 5 V are required in order to measure a single-ended signal that can swing between 0 V and 5 V.

The reference inputs of the device also allow the implementation of ratiometric measurements. In a ratiometric measurement the same excitation source that is used to excite the sensor is also used to establish the reference for the ADC. As an example, a simple form of a ratiometric measurement uses the same current source to excite both the resistive sensor element (such as an RTD) and another resistive reference element that is in series with the element being measured. The voltage that develops across the reference element is used as the reference source for the ADC. These components cancel out in the ADC transfer function because current noise and drift are common to both the sensor measurement and the reference. The output code is only a ratio of the sensor element and the value of the reference resistor. The value of the excitation current source itself is not part of the ADC transfer function.

10.1.6 Establishing Proper Limits on the Absolute Input Voltage

The ADS1119 can be used to measure various types of input signal configurations: single-ended, pseudo-differential, and fully differential signals. However, configuring the device properly for the respective signal type is important.

Signals where the negative analog input is fixed and referenced to analog ground (V_{AINN} = 0 V) are commonly called *single-ended signals*. The absolute input voltages of the ADS1119 can be as low as 100 mV below AGND and as large as 100 mV above AVDD. Using the gain of 4 is still possible in this configuration. Measuring a 0-mA to 20-mA or 4-mA to 20-mA signal across a load resistor of 100 Ω referenced to GND is a typical example. The ADS1119 can directly measure the signal across the load resistor using the internal 2.048-V reference and gain = 1.

Signals where the negative analog input (AIN_N) is fixed at a voltage other the 0 V are referred to as *pseudo-differential signals*.

Fully differential signals in contrast are defined as signals having a constant common-mode voltage where the positive and negative analog inputs swing 180° out-of-phase but have the same amplitude.

The ADS1119 can measure pseudo-differential and fully differential signals.

Signals where both the positive and negative inputs are always ≥ 0 V are called *unipolar signals*. These signals can in general be measured with the ADS1119. A signal is called *bipolar* when either the positive or negative input can swing below 0 V. Bipolar signals cannot be measured with the ADS1119.

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Application Information (continued)

10.1.7 Pseudo Code Example

The following list shows a pseudo code sequence with the required steps to set up the device and the microcontroller that interfaces to the ADC in order to take subsequent readings from the ADS1119 in continuous conversion mode. The $\overline{\text{DRDY}}$ pin is used to indicate availability of new conversion data. The default configuration register settings are changed to gain = 4 and continuous conversion mode.

```
Power-up;
Delay to allow power supplies to settle and power-on reset to complete; minimum of 500 µs;
Configure the I2C interface of the microcontroller;
Configure the microcontroller GPIO connected to the DRDY pin as a falling edge triggered interrupt
input;

Send the RESET command (06h) to make sure the device is properly reset after power-up;


Write the respective register configuration with the WREG command (40h, 12h);
As an optional sanity check, read back the configuration register with the RREG command (20h);

Send the START/SYNC command (08h) to start converting in continuous conversion mode;

Loop
{
    Wait for DRDY to transition low;
    Send the RDATA command (10h) to read 2 bytes of conversion data;
}

Send the POWERDOWN command (02h) to stop conversions and put the device in power-down mode;
```

TI recommends running an offset calibration before performing any measurements or when changing the gain or MUX settings. The internal offset of the device can, for example, be measured by shorting the inputs to mid-supply (MUX[2:0] = 111). The microcontroller then takes multiple readings from the device with the inputs shorted and stores the average value in the microcontroller memory. When measuring the sensor signal, the microcontroller then subtracts the stored offset value from each device reading to obtain an offset compensated result; the offset can be either positive or negative in value.

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10.2 Typical Application

This application example describes how to use the ADS1119 for the most common system monitoring functions (such as voltage measurement, high-side current measurement using a current sense amplifier, and temperature measurement using a thermistor or 2-wire RTD). 図 45 shows a typical circuit implementation.

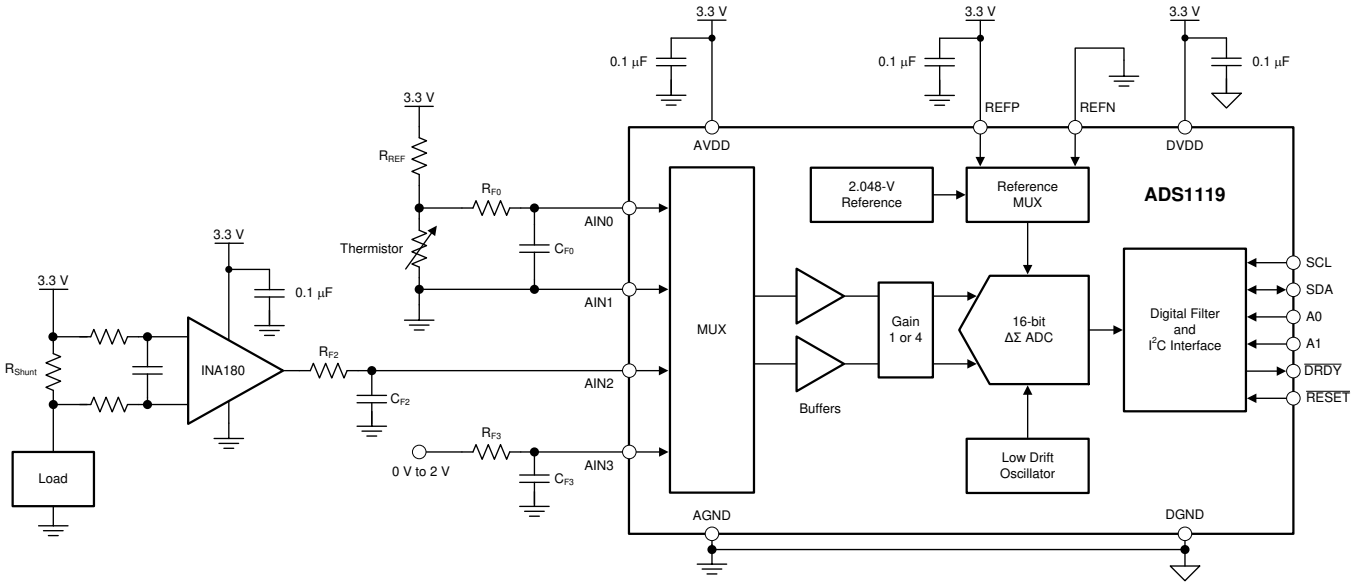

図 45. Typical System Monitoring Example Using the ADS1119

10.2.1 Design Requirements

表 12 lists the design requirements for this application.

表 12. Design Requirements

DESIGN PARAMETER	VALUE
Supply voltage	3.3 V
Voltage measurement range	0 V to 2 V
Voltage measurement accuracy(1)	±0.5 mV
Current measurement range (unidirectonal)	0.5 A to 10 A
Maximum voltage drop across shunt resistor	20 mV
Current measurement accuracy(1)	±5 mA
Thermistor type	NTC
Thermistor nominal resistance	10 kΩ
Thermistor temperature range	–40°C to +125°C
Thermistor temperature measurement accuracy(1)	±0.1°C
Update rate	100 ms

(1) After offset and gain calibration at T_A = 25°C.

10.2.2 Detailed Design Procedure

In order to take one reading from each of the three input signals within 100 ms, the ADS1119 must use a data rate of 90 SPS or faster. When using a data rate setting of 90 SPS, every conversion takes approximately 11.3 ms according to 表 4. Consequently, all three signals can be measured within approximately 34 ms when also accounting for the time to read conversion results and to write new configuration register settings between conversions.

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All three signal measurements use a single-ended measurement implementation. The voltage and current measurements use the GND connection within the MUX, whereas the thermistor measurement uses an external GND connection through AIN1 to showcase the two different options for implementing a single-ended measurement.

RC filters are provided on all three analog inputs of the device, which act as antialiasing filters and to limit the current into the analog inputs in case of overvoltage events. The filter component values are chosen according to the guidelines in the *Analog Input Filtering* section as R_F = 1 kΩ and C_F = 100 nF to create a filter corner frequency of $f_C = 1 / (2\pi \cdot R_F \cdot C_F)$ = 1.6 kHz.

10.2.2.1 Voltage Monitoring

The ADS1119 can measure single-ended signals ranging from AGND to V_{REF} / Gain. In order to monitor voltages up to 2 V, the device is configured to use the internal 2.048-V reference and gain = 1.

式 6 details the relationship between output codes of the ADS1119 and the input voltage on AIN3.

$$V_{AIN3} = (V_{REF} / \text{Gain}) \cdot (\text{Code} / 2^{15}) = 2.048\ \text{V} \cdot \text{Code} / 2^{15} \quad (6)$$

An external voltage reference must be provided on the external reference inputs of the device in case larger voltages than 2.048 V are to be monitored. The device can measure input signals up to the positive analog supply voltage in case AVDD is used as the positive reference input (REFP) and AGND as the negative reference input (REFN). However the ADS1119 cannot monitor its own supply voltage in that case. As described in 式 6, when using V_{AIN3} = AVDD and V_{REF} = AVDD, the device will always output a positive full-scale code irrespective of the value of AVDD. To monitor the supply of the ADC, use a resistor divider instead to divide the supply voltage down to below 2.048 V and measure the voltage using the internal reference.

The input-referred peak-to-peak noise of the ADC is ideally a factor smaller than the required measurement accuracy of ±0.5 mV. At 90 SPS using gain = 1 the ADS1119 offers an input-referred noise of 62.5 μV_{PP}, which meets this requirement.

10.2.2.2 High-Side Current Measurement

The unidirectional, high-side load current measurement is implemented using a shunt resistor, R_{Shunt}, and a current-sense amplifier, INA180, with a gain of 100. To meet the requirement of a maximum voltage drop across R_{Shunt} of 20 mV at the maximum current of 10 A, the shunt resistor must be $R_{Shunt} \le 20\ \text{mV} / 10\ \text{A} = 2\ \text{m}\Omega$. The output signal of the INA180 is fed single-endedly to input AIN2 of the ADS1119. Consequently, the voltage at AIN2 ranges from 0 V to (2 mΩ · 10 A · 100) = 2 V, which can be measured using the internal 2.048-V reference and gain = 1 of the ADC.

式 7 through 式 9 describe the relationship between output codes of the ADS1119 and the current across the shunt resistor.

$$V_{AIN2} = (V_{REF} / \text{Gain}_{ADC}) \cdot (\text{Code} / 2^{15}) = 2.048\ \text{V} \cdot \text{Code} / 2^{15} \quad (7)$$

$$V_{Shunt} = V_{AIN2} / \text{Gain}_{INA} = V_{AIN2} / 100 \quad (8)$$

$$I_{Shunt} = V_{Shunt} / R_{Shunt} = (V_{REF} \cdot \text{Code}) / (\text{Gain}_{ADC} \cdot \text{Gain}_{INA} \cdot R_{Shunt} \cdot 2^{15}) = (2.048\ \text{V} \cdot \text{Code}) / (100 \cdot 2\ \text{m}\Omega \cdot 2^{15}) \quad (9)$$

10.2.2.3 Thermistor Measurement

The temperature measurement using a 10-kΩ thermistor is implemented using a ratiometric measurement approach to achieve best accuracy. The analog supply voltage, AVDD, is used as the excitation voltage for the thermistor in a resistor divider configuration, as well as the external reference voltage, V_{REF}, for the ADS1119.

The relationship between output codes of the ADS1119 and the thermistor resistance, $R_{Thermistor}$, is derived using the following equations. 式 10 expresses the input voltage at input AIN0 as the voltage across $R_{Thermistor}$, whereas 式 11 shows how the ADC converts the voltage at AIN0 into corresponding digital codes.

$$V_{AIN0} = R_{Thermistor} / (R_{Thermistor} + R_{REF}) \cdot V_{REF} \quad (10)$$

$$V_{AIN0} = (V_{REF} / \text{Gain}) \cdot (\text{Code} / 2^{15}) \quad (11)$$

Setting 式 10 equal to 式 11 and solving for $R_{Thermistor}$ yields the relationship between thermistor resistance and ADC code.

$$R_{Thermistor} / (R_{Thermistor} + R_{REF}) = \text{Gain} \cdot (\text{Code} / 2^{15}) \quad (12)$$

$$R_{Thermistor} = R_{REF} \cdot \text{Gain} \cdot (\text{Code} / 2^{15}) / [1 - \text{Gain} \cdot (\text{Code} / 2^{15})] \quad (13)$$

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式 13 proves that the output code and thus the accuracy of the thermistor measurement is independent of the excitation voltage. The accuracy of the reference resistor, R_{REF}, is typically dominating the measurement accuracy in such a ratiometric circuit implementation. A high-precision, low-drift resistor is therefore required for R_{REF}. For best performance, the value of R_{REF} is chosen such that the ratio between R_{REF} and $R_{Thermistor\_Max}$ equals the ratio between $R_{Thermistor\_Min}$ and R_{REF}. 式 14 is therefore used to calculate R_{REF}.

$$R_{REF}^2 = R_{Thermistor\_Min} \cdot R_{Thermistor\_Max} \quad (14)$$

At the two temperature measurement extremes, –40°C and +125°C, a typical 10-kΩ NTC exhibits a resistance of $R_{Thermistor\_Max}$ = 239.8 kΩ and $R_{Thermistor\_Min}$ = 425.3 Ω, respectively. Using 式 14, R_{REF} calculates to 10.1 kΩ. A 10-kΩ resistor is chosen for this example. Consequently, when using 式 10, the voltage at the ADC input ranges from 0.13 V to 3.17 V. Thus, an ADC gain = 1 must be used for the measurement.

The microcontroller interfacing to the ADS1119 converts $R_{Thermistor}$ into a corresponding thermistor temperature by either solving the Steinhart-Hart equation or leveraging a look-up table.

10.2.2.4 Register Settings

表 13 summarizes the configuration register bit settings used for the different measurements in this example.

表 13. Configuration Register Settings

MEASUREMENT	BIT SETTINGS	DESCRIPTION
Voltage	1100 0100	AIN3:AGND, gain = 1, DR = 90 SPS, single-shot conversion mode, internal VREF
Current	1010 0100	AIN2:AGND, gain = 1, DR = 90 SPS, single-shot conversion mode, internal VREF
Thermistor	0000 0101	AIN0:AIN1, gain = 1, DR = 90 SPS, single-shot conversion mode, external VREF

10.2.3 Application Curve

図 46 shows the measurement results for the voltage measurement on AIN3. The measurements are taken at T_A = 25°C. The black curve shows the measurement error in mV without any offset and gain calibration. The red curve shows the measurement error after offset and gain calibration. The gain calibration removes both the gain error and the error introduced by the initial inaccuracy of the internal voltage reference.

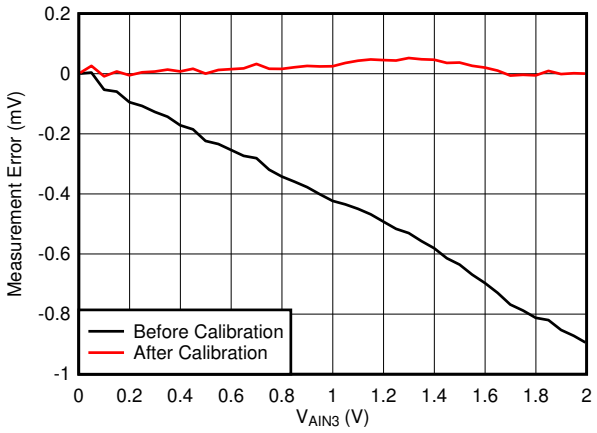

図 46. Measurement Error of Voltage Measurement

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11 Power Supply Recommendations

The device requires two power supplies: analog (AVDD, AGND) and digital (DVDD, DGND). The analog power supply is independent of the digital power supply. The digital supply sets the digital I/O levels.

11.1 Power-Supply Sequencing

The power supplies can be sequenced in any order, but in no case must any analog or digital inputs exceed the respective analog or digital power-supply voltage and current limits. Wait approximately 500 µs after all power supplies are stabilized before communicating with the device to allow the power-on reset process to complete.

11.2 Power-Supply Decoupling

Good power-supply decoupling is important to achieve optimum performance. As shown in 図 47, AVDD and DVDD must be decoupled with at least a 0.1-µF capacitor. Place the bypass capacitors as close to the power-supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes. Connect analog and digital grounds together as close to the device as possible.

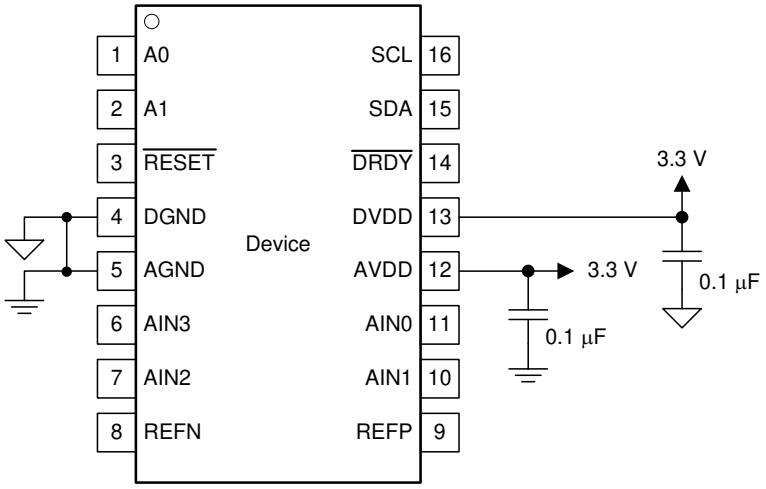

図 47. Power-Supply Decoupling

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12 Layout

12.1 Layout Guidelines

Employing best design practices is recommended when laying out a printed-circuit board (PCB) for both analog and digital components. This recommendation generally means that the layout separates analog components [such as ADCs, amplifiers, references, digital-to-analog converters (DACs), and analog MUXs] from digital components [such as microcontrollers, complex programmable logic devices (CPLDs), field-programmable gate arrays (FPGAs), radio frequency (RF) transceivers, universal serial bus (USB) transceivers, and switching regulators].

The following basic recommendations for layout of the ADS1119 help achieve the best possible performance of the ADC. A good design can be ruined with a bad circuit layout.

- Separate analog and digital signals. To start, partition the board into analog and digital sections where the layout permits. Routing digital lines away from analog lines prevents digital noise from coupling back into analog signals.
- The ground plane can be split into an analog plane (AGND) and digital plane (DGND), but is not necessary. Place digital signals over the digital plane, and analog signals over the analog plane. As a final step in the layout, the split between the analog and digital grounds must be connected together at the ADC.
- Fill void areas on signal layers with ground fill.
- Provide good ground return paths. Signal return currents flow on the path of least impedance. If the ground plane is cut or has other traces that block the current from flowing right next to the signal trace, another path must be found to return to the source and complete the circuit. If forced into a larger path, the chance that the signal radiates increases. Sensitive signals are more susceptible to EMI interference.
- Use bypass capacitors on supplies to reduce high-frequency noise. Do not place vias between bypass capacitors and the active device. Placing the bypass capacitors on the same layer as close to the active device yields the best results.
- Consider the resistance and inductance of the routing. Often, traces for the inputs have resistances that react with the input bias current and cause an added error voltage. Reducing the loop area enclosed by the source signal and the return current reduces the inductance in the path. Reducing the inductance reduces the EMI pickup and reduces the high-frequency impedance at the input of the device.
- Watch for parasitic thermocouples in the layout. Dissimilar metals going from each analog input to the sensor can create a parasitic thermocouple that can add an offset to the measurement. Differential inputs must be matched for both the inputs going to the measurement source.
- Analog inputs with differential connections must have a capacitor placed differentially across the inputs. Best input combinations for differential measurements use adjacent analog input lines (such as AIN0, AIN1 and AIN2, AIN3). The differential capacitors must be of high quality. The best ceramic chip capacitors are C0G (NPO) that have stable properties and low noise characteristics.

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12.2 Layout Example

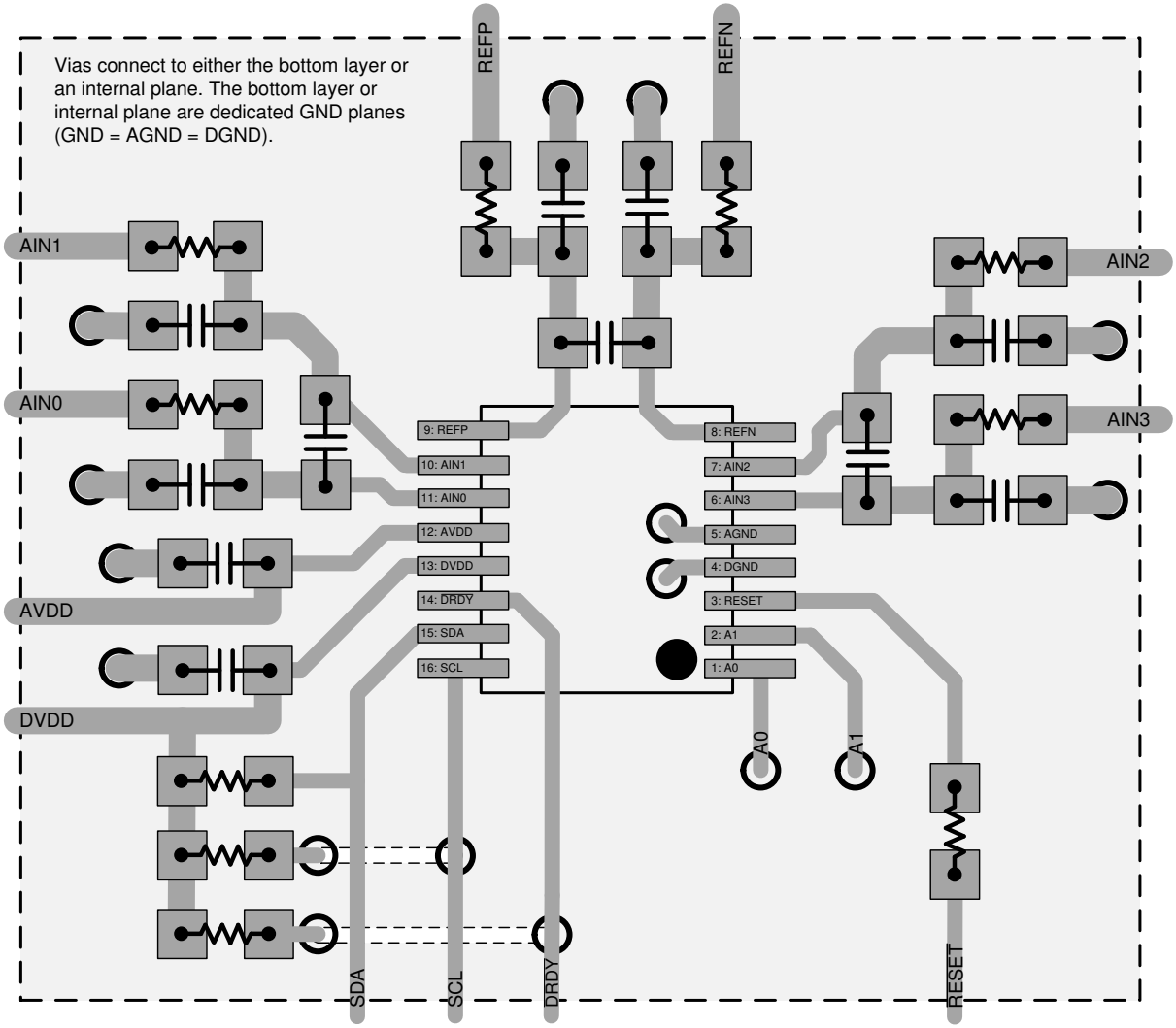

図 48. Layout Example

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13 デバイスおよびドキュメントのサポート

13.1 デバイス・サポート

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13.2 ドキュメントのサポート

13.2.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、*『REF50xx 低ノイズ、超低ドリフト、高精度基準電圧』データシート*
- テキサス・インスツルメンツ、*『INAx180 ローサイドおよびハイサイド電圧出力、電流センス・アンプ』データシート*

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13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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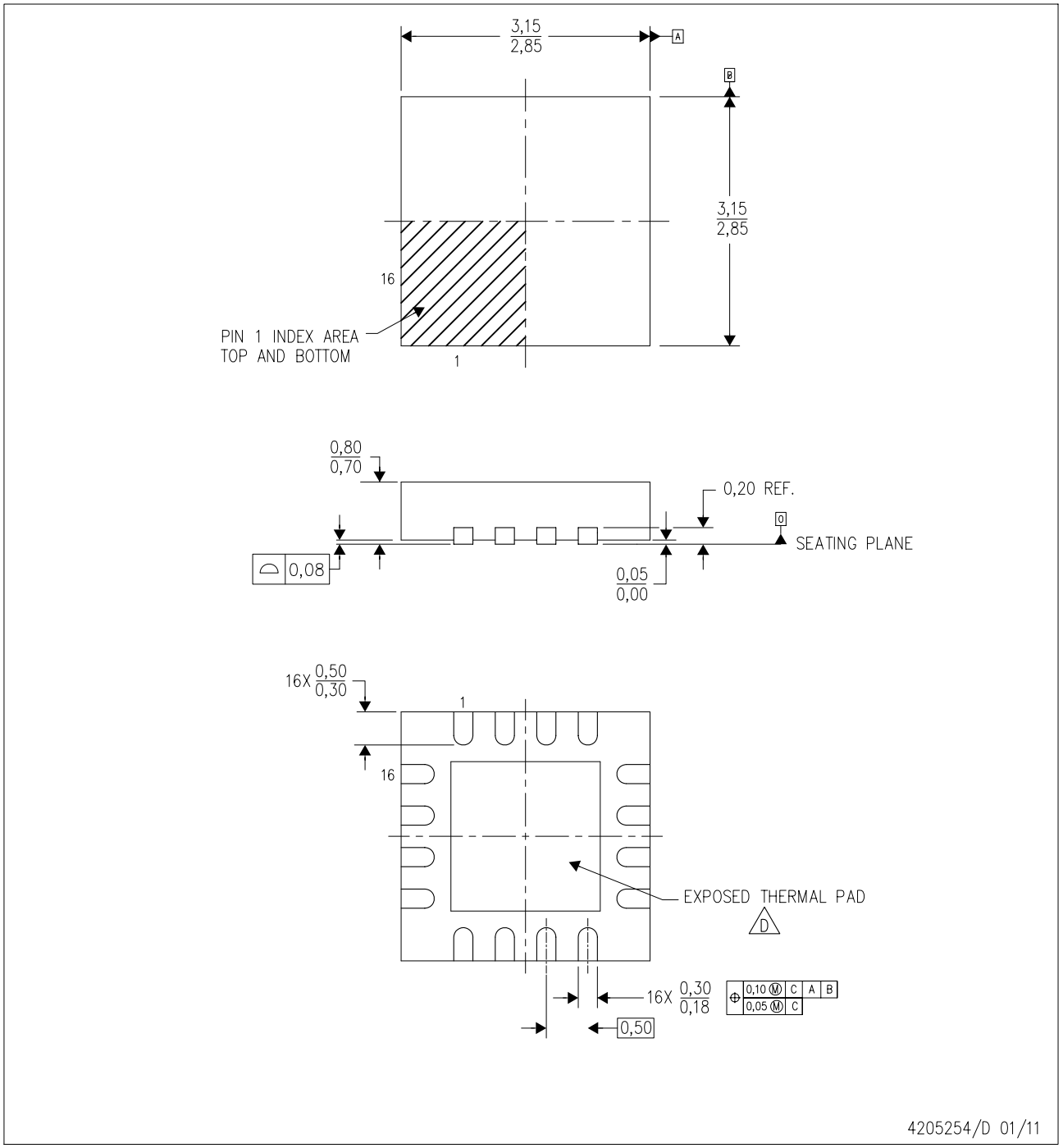
MECHANICAL DATA

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

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THERMAL PAD MECHANICAL DATA

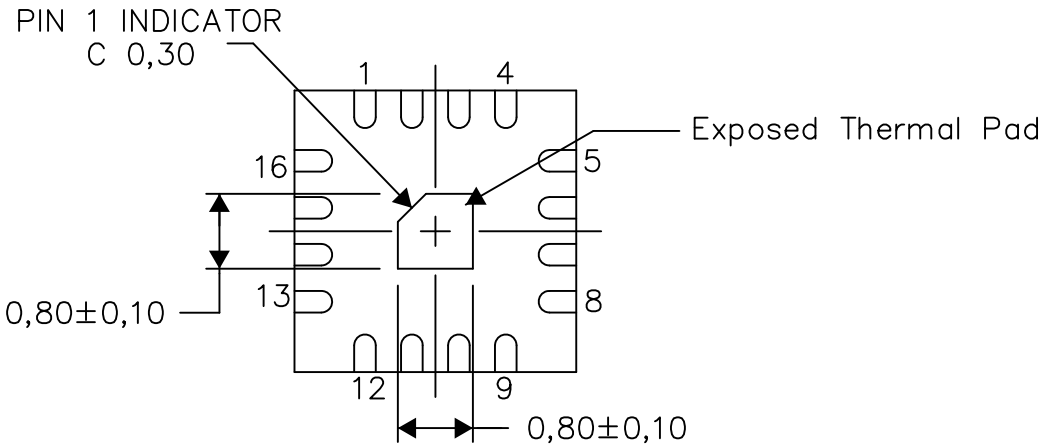
RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206446–5/U 08/15

NOTE: A. All linear dimensions are in millimeters

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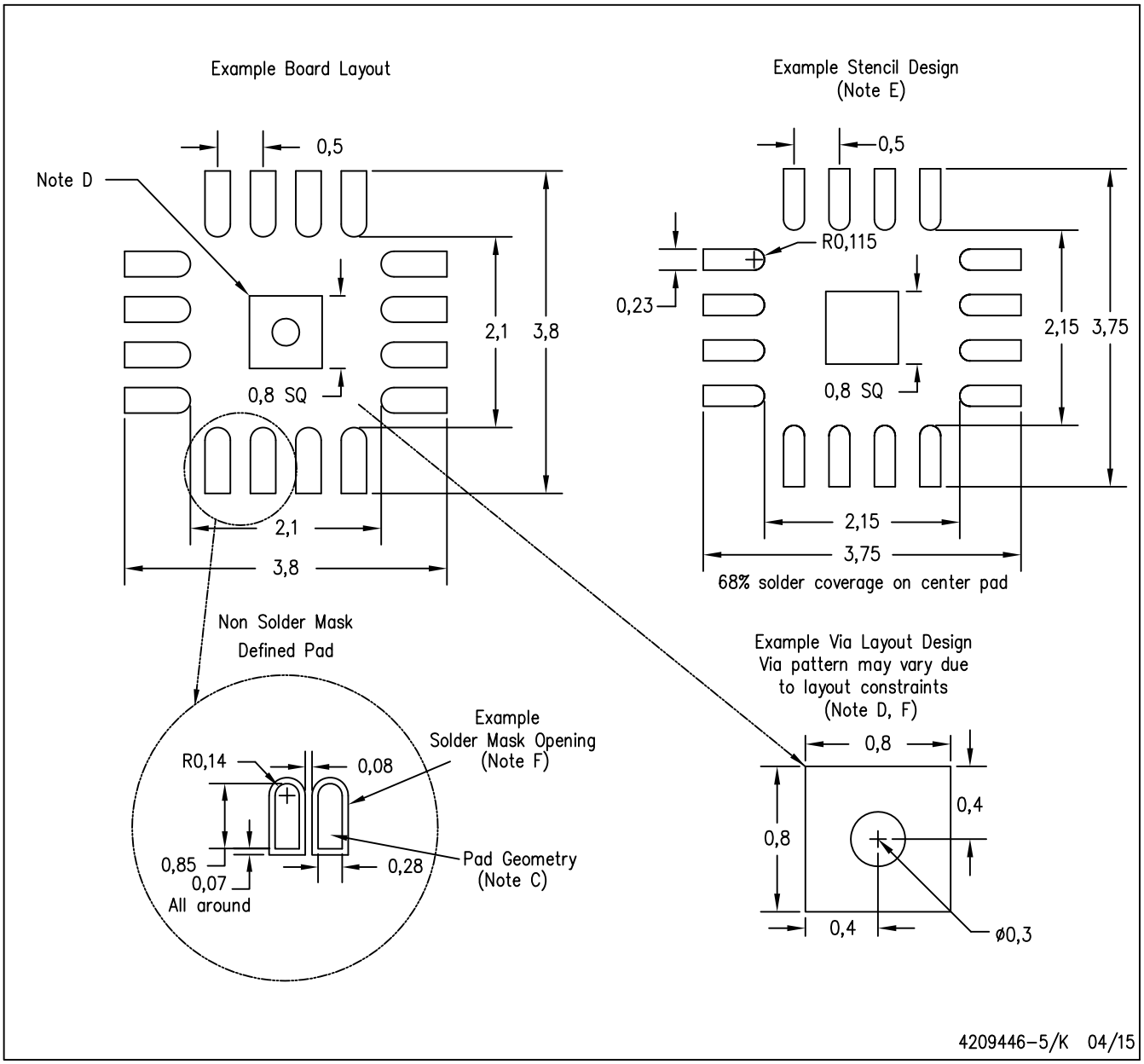
LAND PATTERN DATA

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1119IPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS1119	Samples
ADS1119IPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS1119	Samples
ADS1119IPWT	ACTIVE	TSSOP	PW	16	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS1119	Samples
ADS1119IRTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1119	Samples
ADS1119IRTET	ACTIVE	WQFN	RTE	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1119	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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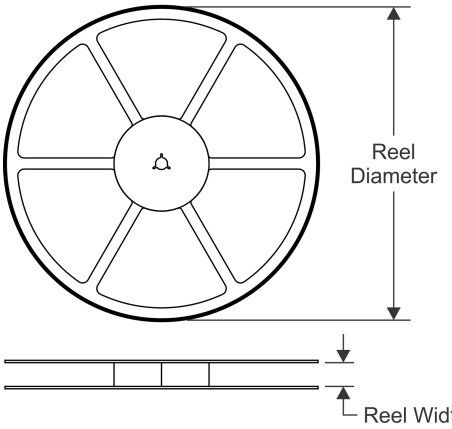
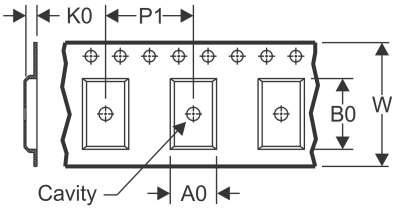
TAPE AND REEL INFORMATION

REEL DIMENSIONS

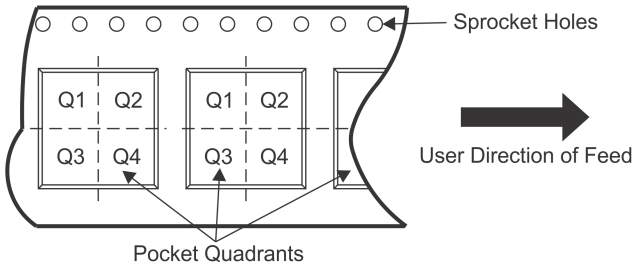


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

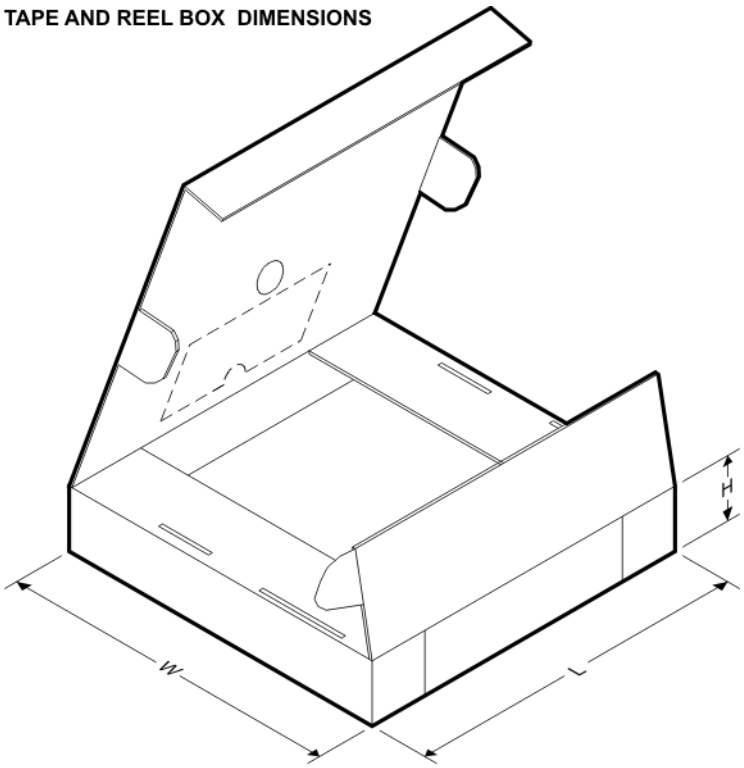
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1119IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
ADS1119IPWT	TSSOP	PW	16	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
ADS1119IRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
ADS1119IRTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2

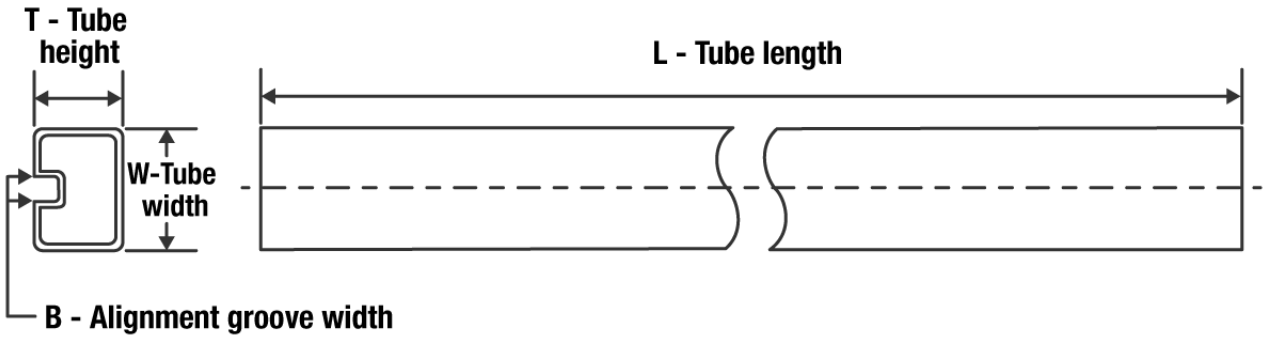
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1119IPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
ADS1119IPWT	TSSOP	PW	16	250	210.0	185.0	35.0
ADS1119IRTER	WQFN	RTE	16	3000	367.0	367.0	38.0
ADS1119IRTET	WQFN	RTE	16	250	213.0	191.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ADS1119IPW	PW	TSSOP	16	90	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

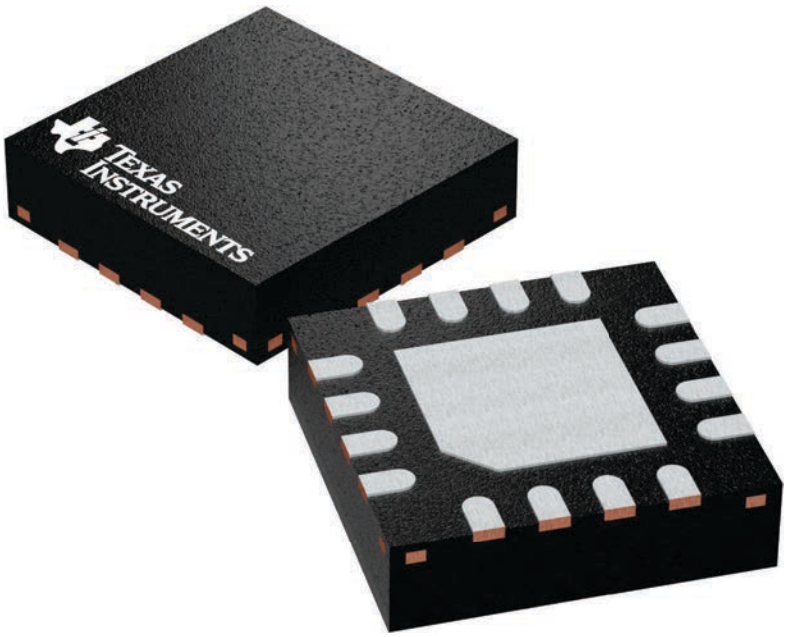
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

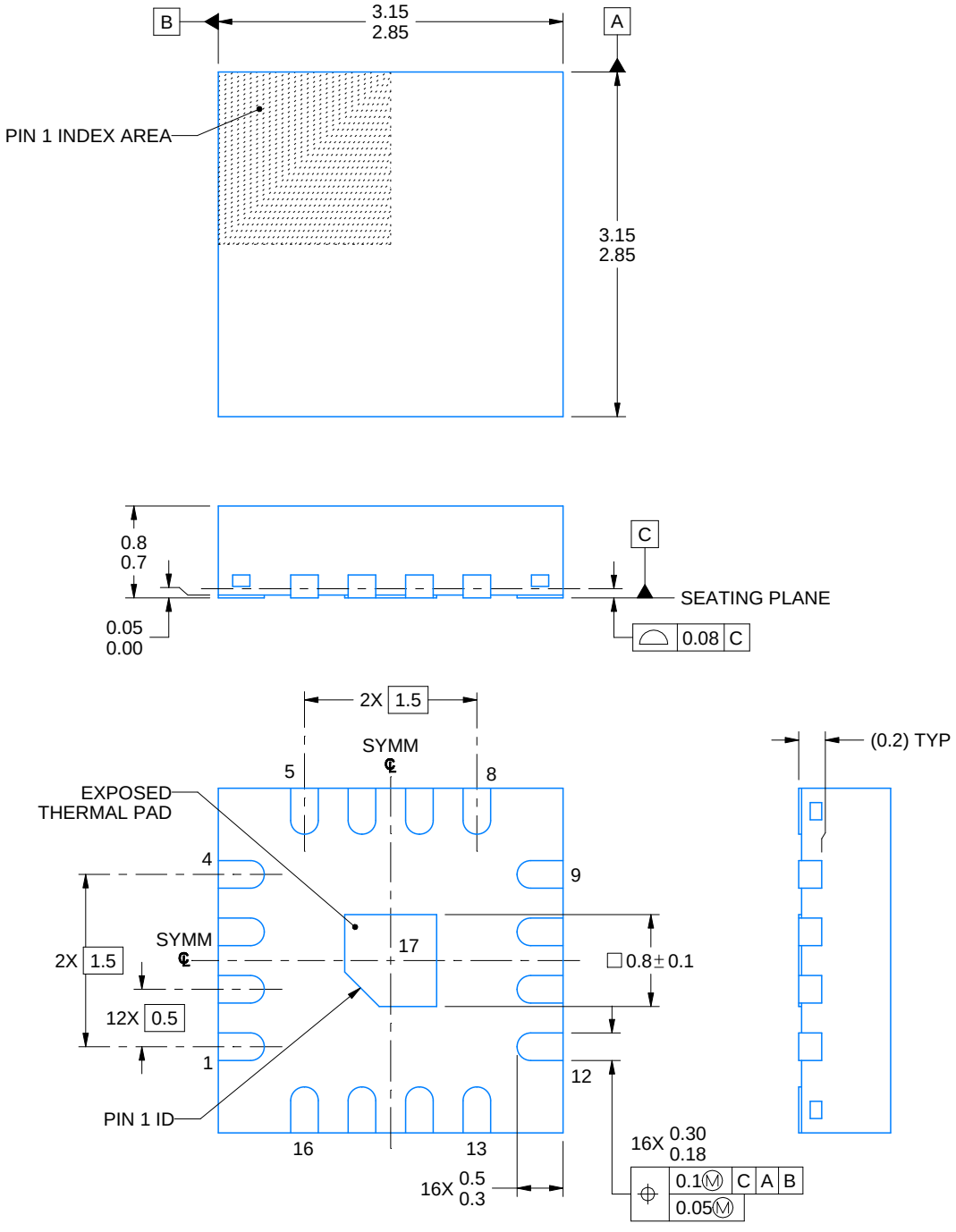


PACKAGE OUTLINE

RTE0016D

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

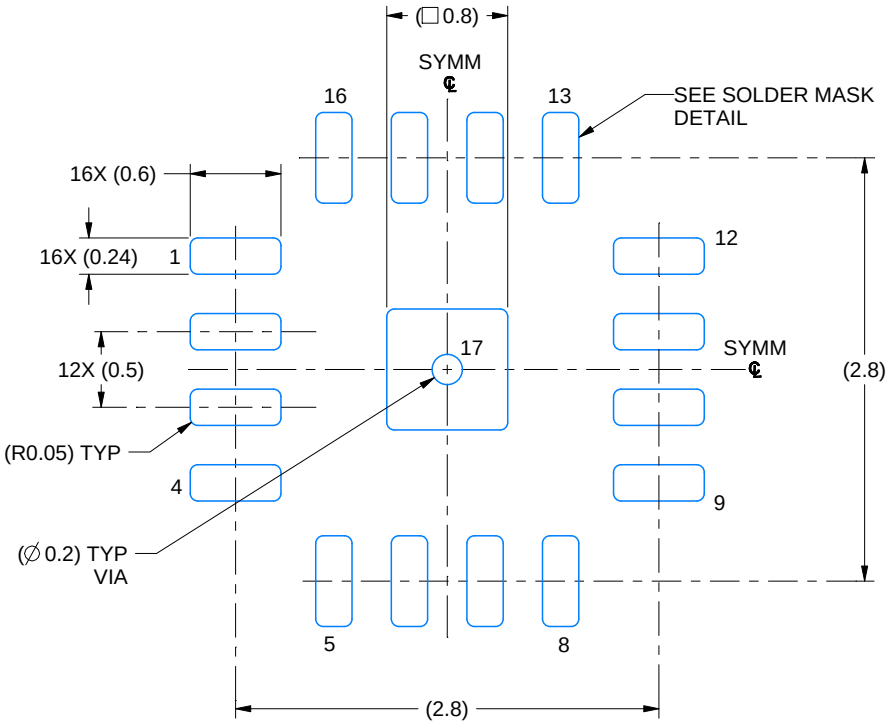
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

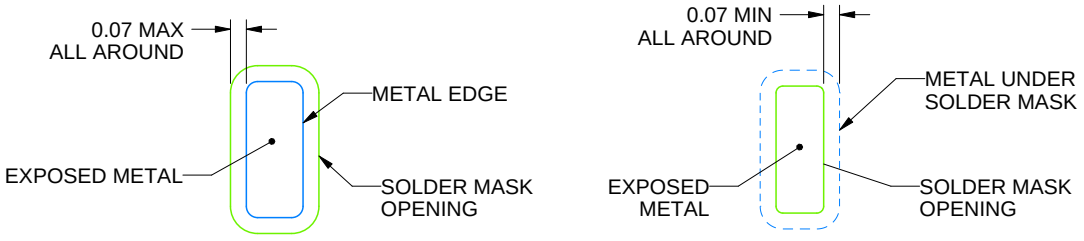
RTE0016D

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

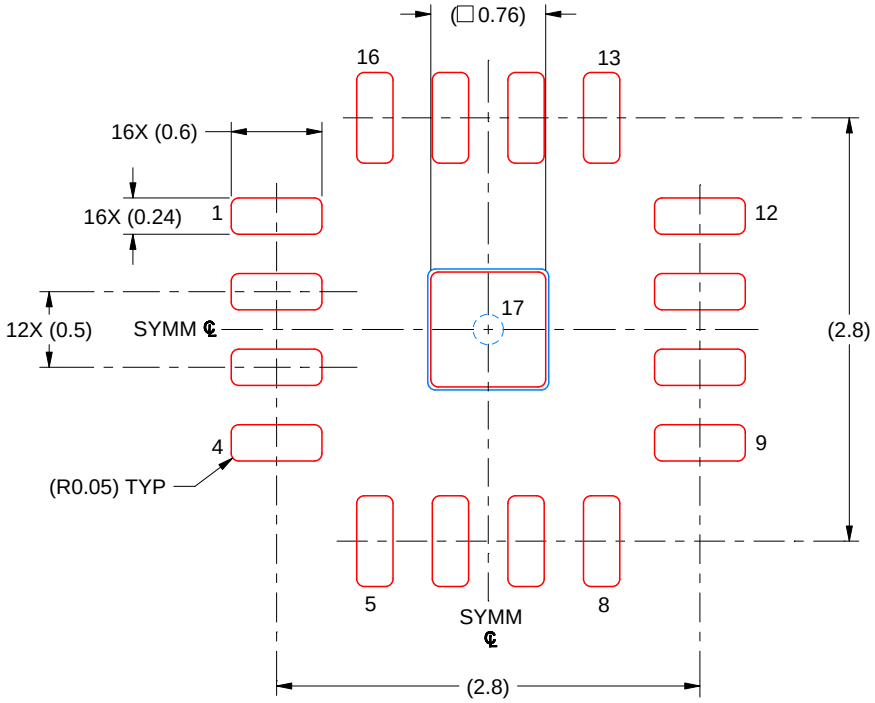


SOLDER MASK DETAILS

4219118/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219118/A 11/2018

NOTES: (continued)

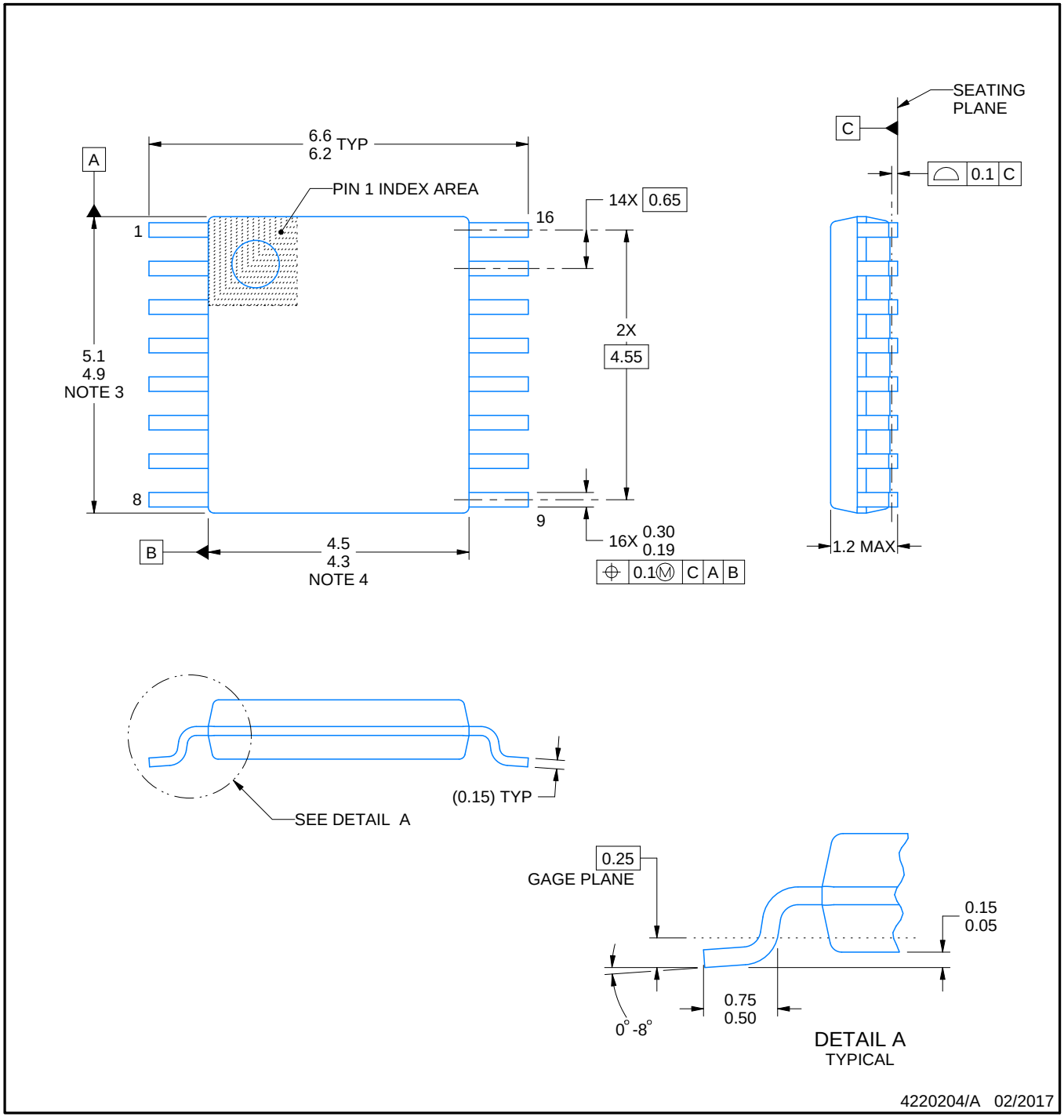
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0016A

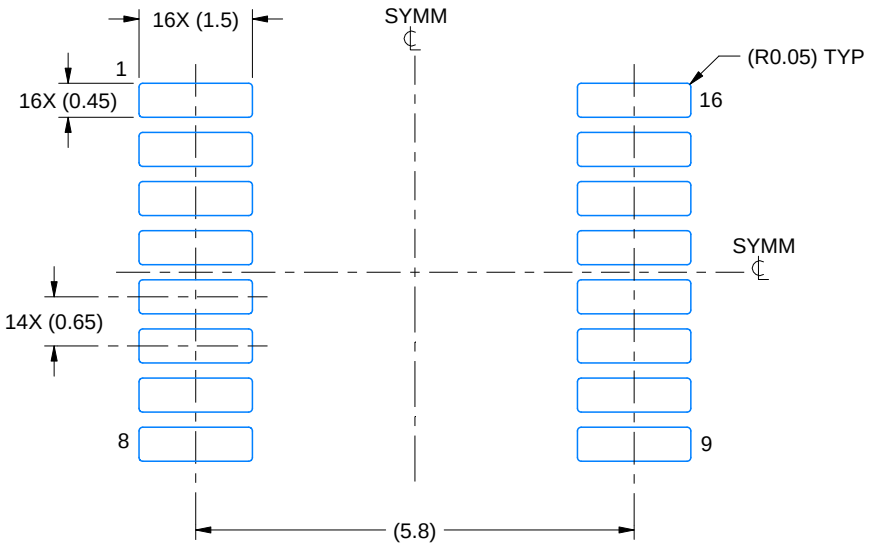
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

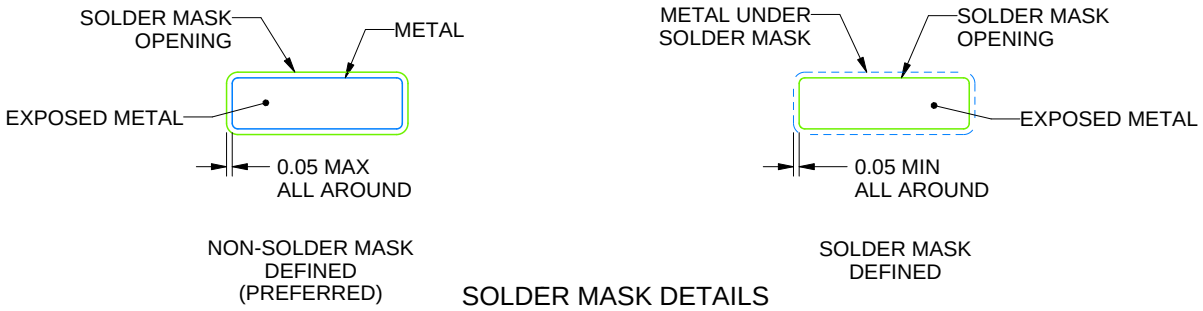


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

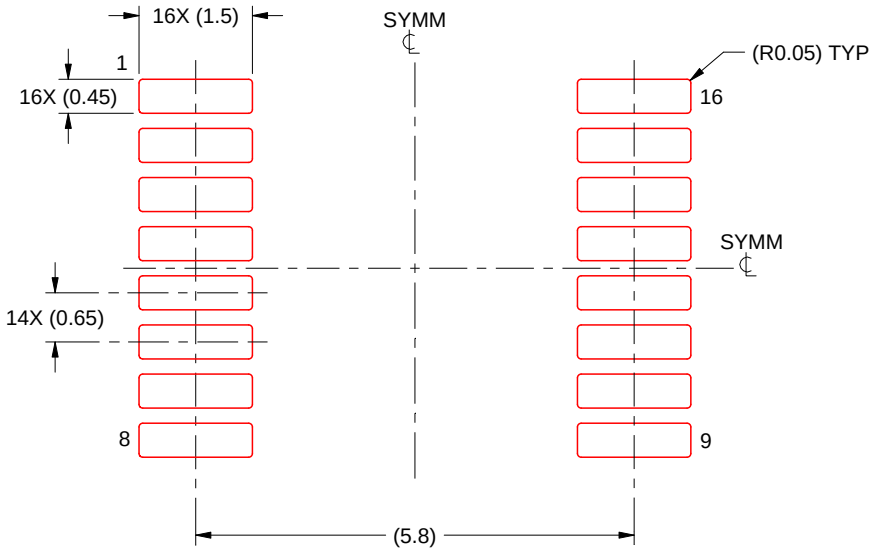


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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