参考資料

JAJU205

TI Designs

絶縁型シャント・センサによる多相エネルギー測定

TI Designs

TI Designsは、システムをすばやく評価してカスタマイズするために必要な、手法、テスト、デザイン・ファイルなどの基盤を提供し、開発期間の短縮に役立ちます。

デザイン・リソース

TIDA-00601	デザイン・ファイルを含むツール・フォルダ
AMC1304M05	製品フォルダ
MSP430F67641	製品フォルダ
SN6501	製品フォルダ
TRS3232	製品フォルダ
ISO7321	製品フォルダ
TPS76333	製品フォルダ
ISO7320	製品フォルダ

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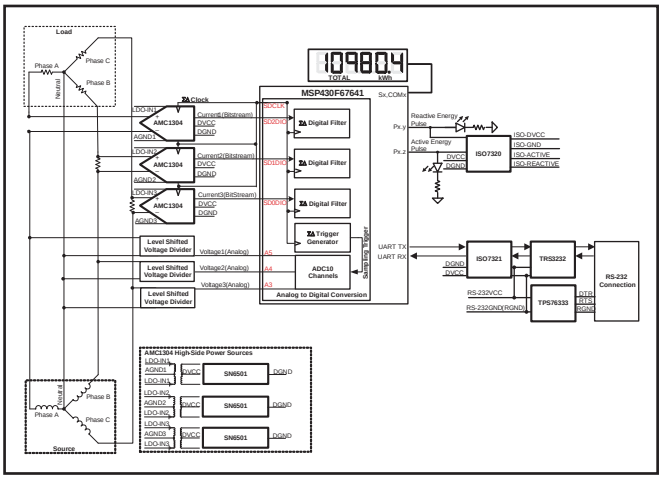
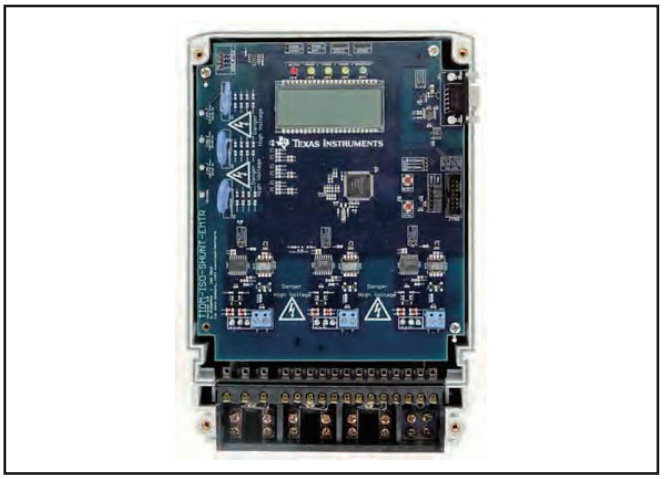
デザインの特長

- 絶縁型シャント電流センサによるクラス0.5%の三相測定
- 最大1kV AC(動作電圧)および7kV(ピーク電圧)の絶縁性能
- TIのEnergy Libraryファームウェアによって、アクティブおよびリアクティブな電力とエネルギー、RMS(2乗平均平方根)電流および電圧、力率、ライン周波数など、すべてのエネルギー測定パラメータを計算
- 3kV$_{RMS}$の動作絶縁境界を備えた絶縁型RS-232によって、PCのグラフィカル・ユーザー・インターフェイス(GUI)と通信
- 内蔵の160セグメント・ディスプレイによって測定パラメータを表示

主なアプリケーション

- 計測
- グリッド監視
- 街路照明





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TIDU845A　翻訳版

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1 システム説明

このデザインは、絶縁型シャント・センサを使用したクラス0.5の三相エネルギー測定システムを実装します。絶縁は、出力回路がコンデンサを介して入力回路と分離されている、絶縁型デルタ・シグマ変調器を使用して実現されています。エネルギー測定用のSoC (System on Chip)が絶縁型変調器からビットストリームを取得し、オンボード・デジタル・フィルタを使用してADCサンプル値を生成します。また、このエネルギー測定用SoCは、電圧のセンシング、測定パラメータ値の計算、基板上の液晶ディスプレイ(LCD)の駆動、および基板上の絶縁型RS-232回路を通したPC GUIとの通信にも使用されます。

測定に関しては、ソフトウェア・エネルギー・ライブラリにより、最大で3つの相のエネルギーを測定するための各種パラメータの計算をサポートします。エネルギー測定中に計算される主なパラメータは、RMS電流および電圧、アクティブ/リアクティブの電力およびエネルギー、力率、周波数です。これらのパラメータは、校正用GUIまたはLCDに表示できます。このデザイン・ガイドでは、測定用ソース・コードの全体を、ダウンロード可能なzipファイルとして提供しています。

1.1 MSP430F67641

測定パラメータのセンシングと計算には、エネルギー測定用SoCデバイスであるMSP430F67641を使用します。このデバイスは、MSP430F67xxファミリに属する最新の計測用SoCです。このデバイス・ファミリは、強力な16ビットMSP430F6xxプラットフォームをベースとし、多くの新機能により堅牢な多相測定ソリューションを柔軟にサポートします。これらのチップは、エネルギー測定アプリケーション向けに開発され、それをサポートするために必要なアーキテクチャを搭載しています。

MSP430F67xxデバイスには、内部または外部の変調器を使用できるデルタ・シグマADCモジュール(SD24_B)が搭載されています。このデザインでは外部変調器オプションを使用し、電流を測定する絶縁型デルタ・シグマ変調器とともにMSP430F67641のデジタル・フィルタを利用できます。図1に、SD24_Bコンバータのブロック図を示します。外部変調オプションの選択時には、図1で赤色に塗られた部分が使用され、それ以外の部分はバイパスされます。

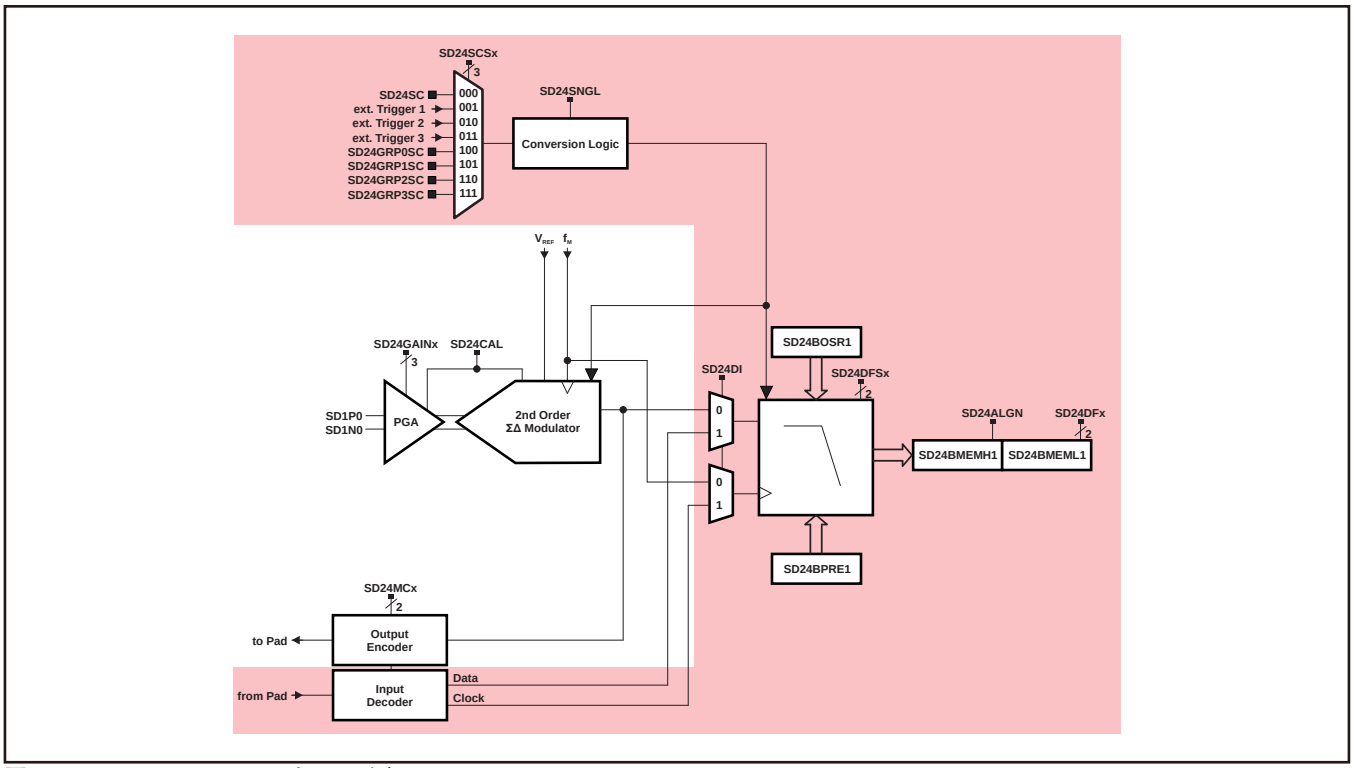

図 1. SD24_Bコンバータのブロック図

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デザインで使用する絶縁型デルタ-シグマ変調器の個数を最小限に抑えるために、これらの変調器は電流の測定のみに使用されます。これらの変調器を使用した結果、SD24_Bモジュール内で使用される変調クロック周波数は、現時点で外部変調器に接続されていない追加のSD24_B ADCの内部変調器に対して使用するには高すぎます。この制約により、相電圧のセンシングには、MSP430F67641の内蔵10ビットSAR ADCを使用しています（デザインTIDM-THREEPHASEMETER-F67641を参照）。

これらのSAR ADCをSD24_Bと同期させるために、すべてのMSP430F67xx多相デバイスにはトリガ-ジェネレータが搭載され、ADC10とSD24_Bモジュール間のタイミングが確実にグループ化されて同期されるように、ADC10をトリガします。図2に、トリガ-ジェネレータのブロック図を示します。

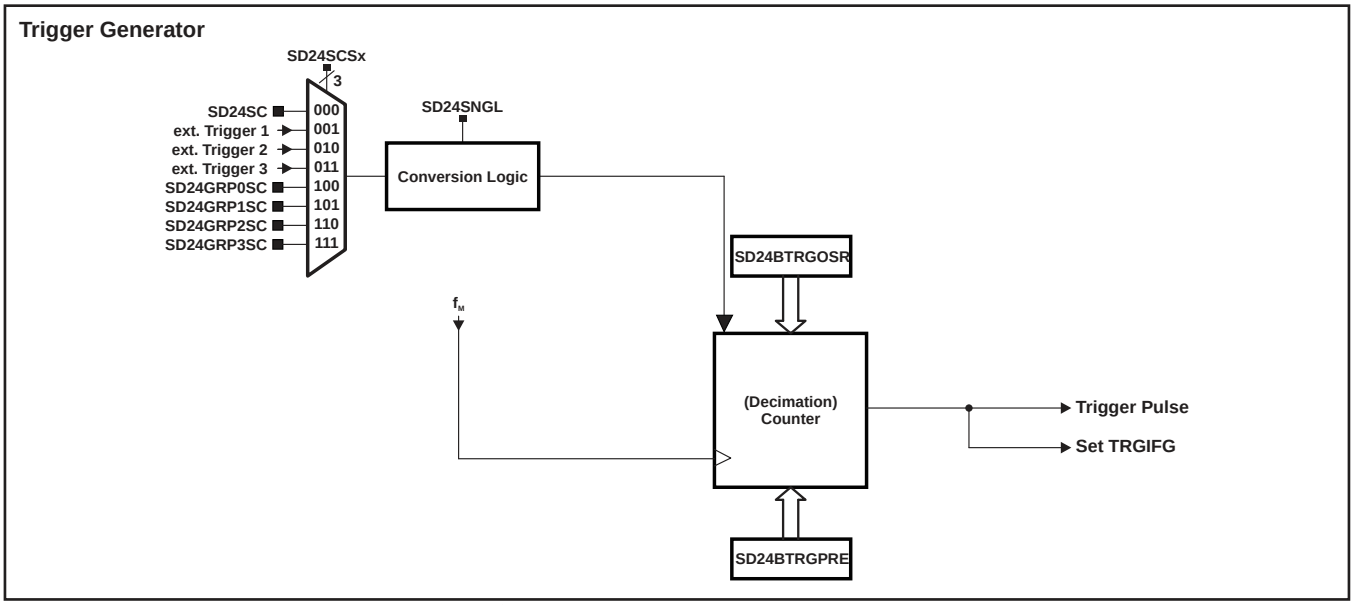

図 2. SD24_Bトリガ・ジェネレータのブロック図

1.2 AMC1304M05

AMC1304は、デザインのシャント電流センサに対して、絶縁された状態で電流測定を行うために使用されます。この電流測定のために、AMC1304が提供する変調ビットストリーム出力は、シャントからAMC1304に供給されるアナログ信号から容量性絶縁されています（図3を参照）。

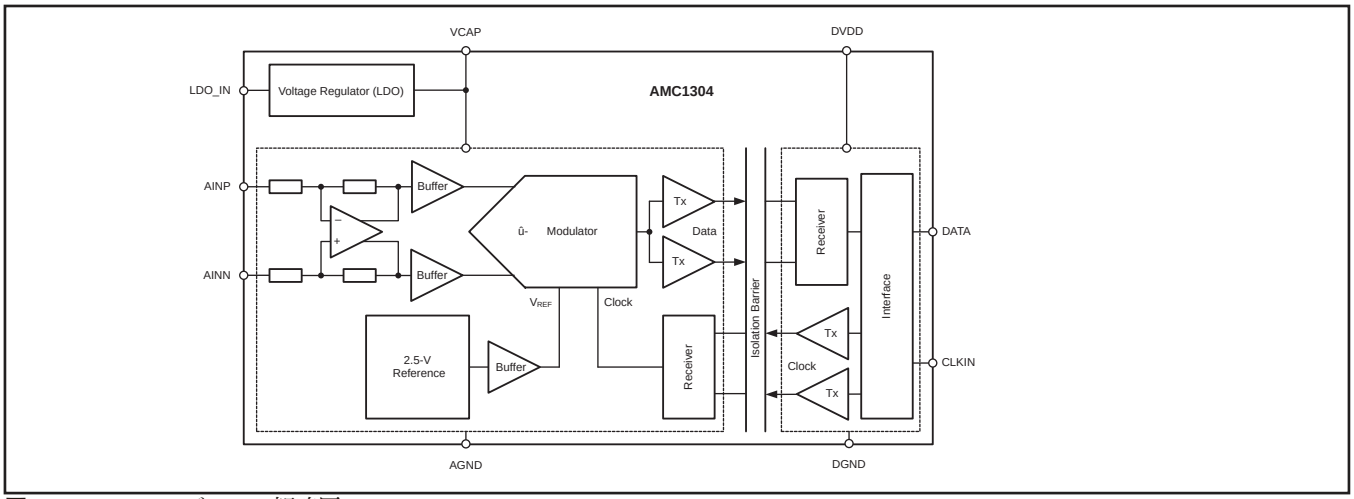

図 3. AMC1304のブロック概略図

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図3では、AMC1304のAINP端子とAINN端子の間でシャント電流を測定しています。シャントの第3の端子は、AMC1304のAGNDに接続します。測定を行うには、LDO_INとAGNDの間に4V～18Vを供給する必要があります。AMC1304では、内蔵の低ドロップアウト（LDO）レギュレータを使用して、変調器を搭載するチップのハイサイドに電源を供給します。

コントローラ側への電源を適切に供給するために、AMC1304のDVDDピンおよびDGNDピンをMSP430F67641のDVCCおよびDGNDに接続する必要があります。さらに、MSP430F67641のSD24_Bデジタル・フィルタで使用される変調クロックを、CLKINに接続する必要があります。AMC1304が適切に動作するには、この変調クロックを5MHz～20MHzにする必要があり、これはMSP430のSD24_Bモジュールのクロック出力から生成するか、またはMSP430F67641のSD24_BとAMC1304の両方に供給される外部クロック・ジェネレータから生成できます。CLKINに適切なクロックが供給されると、AMC1304のDATAピンからビットストリームが出力されます。このDATAピンは、MSP430F67641のデジタル・ビットストリーム入力に接続する必要があります。

AMC1304チップの選択については、4種類のデバイスがあります。そのうち2つはCMOSデジタル・インターフェイス・オプション（品名に“M”を含む）に対応し、残りの2つは低電圧差動シグナリング（LVDS）デジタル・インターフェイス・オプション（品名に“L”を含む）に対応しています。MSP430F67641に対して適切にインターフェイスするには、CMOSオプションを選択します。CMOSオプションには、±50mVの入力範囲を持つオプション（品名に“05”を含む）と、±250mVの入力範囲を持つオプション（品名に“25”を含む）があります。Eメーター・アプリケーションに対しては、一般に、シャントの消費電力を減らすために抵抗の小さいシャントが使用されます。したがって、AMC1304の入力範囲全体を使用するには、±250mVの入力範囲ではなく、±50mVの入力範囲を使用する必要があります。その結果、このデザインに最も適しているAMC1304デバイスは、AMC1304M05です。

AMC1304M05デバイスでは、入力電圧値が±50mVを超えた場合、測定値の精度が低下します。また、特定の差動入力電圧（フルスケール電圧以上ではないと仮定）を印加した場合の“1”の割合を求めるには、式（1）を使用します。

$$\%_{HIGH} = 100 \times \left(\frac{V_{input} + 0.625}{1.25} \right) \quad (1)$$

この式から、0Vの差動電圧は、“1”と“0”が全体の50%の時間Highであるようなビットストリームに関連付けられます。また、50mVの差動電圧は、“1”と“0”が全体の90%の時間Highであるようなビットストリームを生成し、-50mVの差動電圧は、“1”と“0”が全体の10%の時間Highであるようなビットストリームを生成します。

1.3 SN6501

各AMC1304では、チップのハイサイドに電源を供給するために、LDO_INピンに4V～18Vを供給する必要があります。このデザインでは、この電圧はオンボードの絶縁型電源から得られます。この絶縁型電源では、電圧入力としてのDVCC、およびトランスとトランス・ドライバを使用して、LDO_INに供給する必要な絶縁電圧を生成します。トランス・ドライバ機能は、SN6501を使用して実現されます。

1.4 TRS3232

RS-232標準に対して適切にインターフェイスするために、電圧変換システムを使用して、基板上の3.3Vドメインとポート上の12Vとの間で変換を行う必要があります。この変換を容易にするために、デザインではTRS3232デバイスを使用しています。TRS3232デバイスは、チャージ・ポンプ・システムを通して、3.3VのDVCCのみから、より高い電圧信号をRS-232ポート上で駆動できます。

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1.5 ISO7321

PCへのRS-232接続に絶縁を追加するために、このデザインの絶縁型RS-232回路では、オプトアイソレータよりも本質的に耐用年数が優れた、容量性ガルバニック絶縁を使用しています。特に、産業用デバイスは通常、民生用電子機器よりもずっと長い期間にわたって使用されるため、15年以上にわたって有効な絶縁を維持することが重要です。

TIのISO7321デバイスは、3.3Vまたは5Vで動作できる単純なデュアル・チャネル・アイソレータであり、インターフェイスのDCE（データ回線終端装置）側に幅広い範囲のデバイスの接続を可能にします。ISO7321デバイスは、UART（Universal Asynchoronous Receiver/Transmitter）信号パス上に単純に挿入し、各側に適切な電源を配置することで、動作できます。また、ISO7321デバイスは、UL（Underwriters Laboratories）の認定レベルを満たすために3kVの絶縁を維持します。

ISO7321デバイスには、ISO7321CとISO7321FCの2種類があり、デフォルト・オプションがHighかLowかが異なります。このデザインではどちらの種類も使用可能ですが、ISO7321Cデバイスを使用しています。また、代替手段として、ISO7321とピン・コンパチブルであるISO7421などのアイソレータも使用できます。

1.6 TPS76333

絶縁境界のDCE（データ回線終端装置）側およびRS-232チャージ・ポンプに電源を供給するには、2つの選択肢があります。インターフェイスでは、絶縁型電源を実装するか、またはRS-232ラインから電源を得ることができます。電源を搭載するとコストおよび複雑性が増すため、低コストのセンシング・アプリケーションでは適切ではありません。

第2のオプションである、RS-232ポート自体からの給電を実装するために、このデザインでは、ほとんどの組み込みアプリケーションでは無視されるフロー制御ラインを利用しています。RS-232仕様（ホスト・コンピュータまたはアダプタ・ケーブルで適切に実装された場合）では、ポートがアクティブのときにRTS（Request to send）ラインとDTR（Data terminal ready）ラインがHighに維持されます。ホストでCOMポートが開いている間、この2本のラインには電圧がかかっています。この電圧は、ドライバの実装に応じて、5V～12Vの範囲で異なります。5V～12Vの電圧は、このデザインでの使用要件に対して十分な値です。

この電圧は、信号がピンに逆流するのを防ぐため、ダイオード回路を通して供給されます。この電圧はコンデンサを充電してエネルギーを蓄積します。バリアとチャージ・ポンプに、瞬間的に許容される値を超える電流が流れた場合には、このコンデンサのエネルギーが解放されます。TPS76333は、このライン電圧を、チャージ・ポンプおよび絶縁デバイスの動作電圧へと下げるために使用されます。

1.7 ISO7320

メーターのアクティブ・エネルギーおよびリアクティブ・エネルギーの精度をテストするために、消費されたエネルギーの大きさに比例するレートでパルスが出力されます。次に、リファレンス・メーターを使用して、これらのパルスおよびメーターへのエネルギー供給量に基づいて誤差を計算することで、メーターの精度を決定します。このデザインでは、アクティブ・エネルギーとリアクティブ・エネルギーの累積的な消費に対して、ヘッダを通してパルスが出力されます。これらのヘッダの絶縁型バージョンであるISO7320を使用することで、非絶縁機器への接続が可能になります。これらの絶縁型アクティブ/リアクティブ信号は、最大電圧出力を3.3Vまたは5Vに設定できます。そのためには、絶縁側VCC（ISO_VCC）と絶縁側GND（ISO_GND）の間に、選択した最大電圧出力を印加します。

ISO7320デバイスには、ISO7320CとISO7320FCの2種類があり、デフォルト・オプションがHighかLowかが異なります。このデザインではどちらの種類も使用可能ですが、ISO7320Cデバイスを使用しています。また、代替手段として、ISO7320とピン・コンパチブルであるISO7420などのアイソレータも使用できます

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2 ブロック図

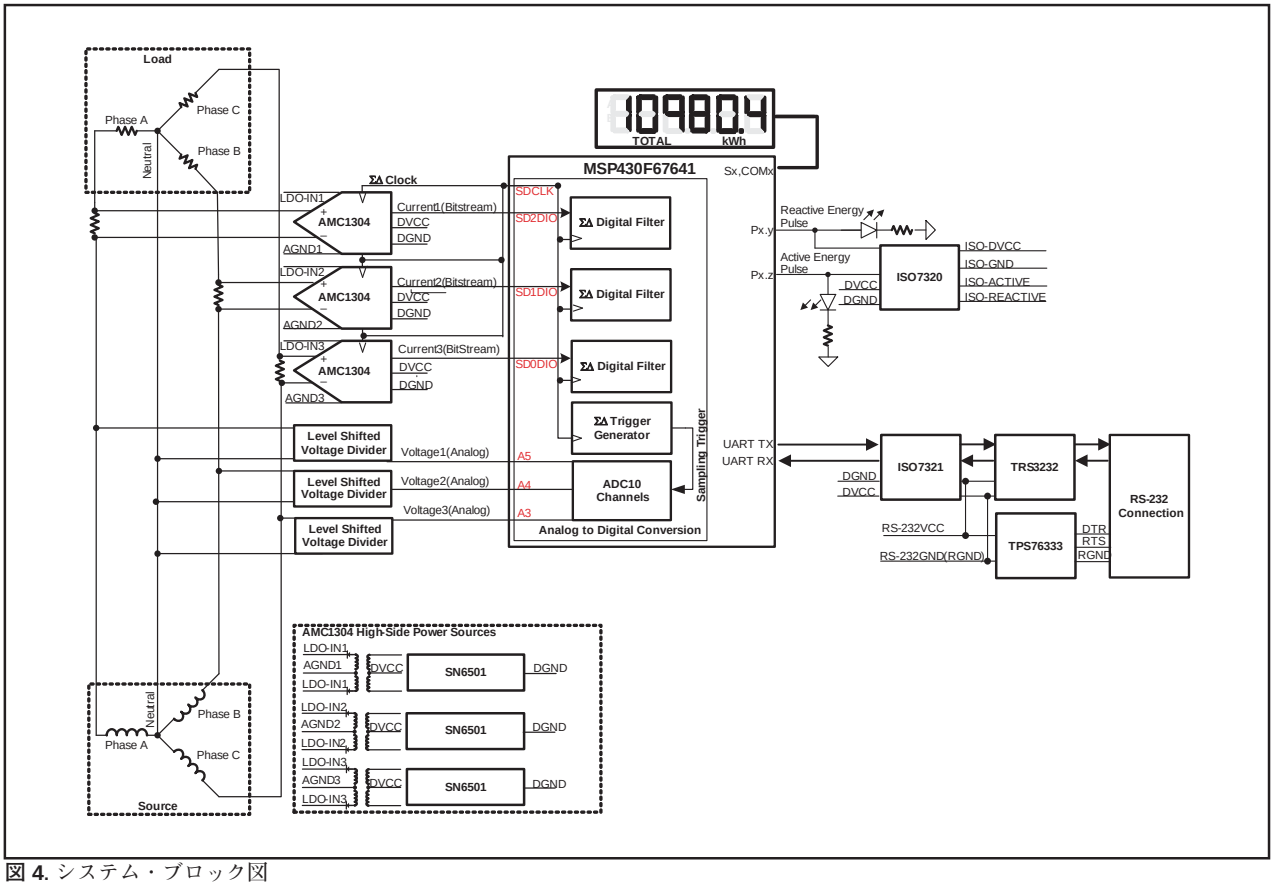

図 4. システム・ブロック図

図4のブロック図は、絶縁型シャントを備えたMSP430F67641ベースの三相エネルギー測定アプリケーションに対して使用されるインターフェイスの概要を示しています。図4は、このデザインでの商用AC電源に対する三相4線式スター接続を示しています。このデザインでは、各相ごとにシャント電流センサとAMC1304デバイスが接続され、シャント電流センサにかかる電圧を測定します。シャントの抵抗は、エネルギー測定に必要な電流範囲に基づき、シャントの最大消費電力が最小限に抑えられるよう選択されています。

AMC1304のハイサイドへの電源供給のために、各AMC1304には外部に絶縁型電源が接続されています。AMC1304の各ハイサイドはそれぞれ異なるライン電圧を基準とする必要があるため、3つの絶縁型電源が使用されていることに注意してください。実装されている各電源は、DVCC、トランス、およびSN6501トランス・ドライバを使用して、対応するAMC1304に電源を供給します。対照的に、AMC1304チップのコントローラ側の電源供給については、すべてのAMC1304が、MSP430F67641デバイスと同じソースから給電される必要があります。

変換を実行するために、すべてのAMC1304チップに同じ外部クロックを供給する必要があります。このデザインでは、SD24_Bモジュールによって、MSP430F67641内部で生成される変調クロックが出力され、この変調クロックをすべてのAMC1304チップに供給します。それにより、AMC1304チップはそれぞれ対応するビットストリームを出力します。これらのビットストリームは、チップのハイサイド側からは絶縁されています。これらの各ビットストリームは、それぞれ異なるMSP430F67641コンバータのビットストリーム入力に供給されます。

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電圧センサに対しては、分圧回路とレベル・シフタを組み合わせることで、ADCへの入力電圧がシングルエンド動作電圧範囲内に収まるようにしています。動作範囲は、SAR ADCに対して選択された基準電圧ソースによって決まります。電圧チャネルに対する分圧抵抗は、選択された基準電圧に基づいて、商用電源電圧がSAR ADCの有効な通常入力範囲へと分圧されるように選択します。これらのSAR ADCをSD24_Bモジュールと同期させるために、SD24_B内のトリガ・ジェネレータによって、ADC10とSD24_Bモジュール間のタイミングが確実にグループ化されて同期されるように、ADC10をトリガします。

図4の中で他に注意すべき信号は、精度測定と校正のために使用されるアクティブおよびリアクティブ・エネルギー・パルスです。ISO7320は、非絶縁機器への接続用に、これらのパルスに対する絶縁接続を提供します。絶縁されたパルスに加えて、このデザインは、TPS76333、ISO7321、およびTRS3232デバイスの使用により絶縁型RS-232通信をサポートしています。デザインの絶縁型RS-232回路の詳細については、TIDA-00163のリソースを参照してください。

2.1 使用製品

2.1.1 MSP430F67641

MSP430F67641多相計測SoCは、強力な高集積エネルギー測定ソリューションであり、わずかな外部部品で高い精度と低いシステム・コストを実現します。F67641は、低消費電力のMSP430 CPUを32ビット乗算器とともに使用し、すべてのエネルギー計算や、料率管理などの計測アプリケーション、および自動検針（AMR）または高度計量インフラ（AMI）モジュールとの通信を実行します。このチップには、最大320セグメントをサポートするLCDコントローラ、オフセットおよび温度校正を内蔵したリアルタイム・クロック（RTC）モジュール、およびチップ内の他の部分から独立してRTCに給電できる個別の補助電源が搭載されています。図5に、これらを含めたMSP430F67641 SoCの各種機能を示します。

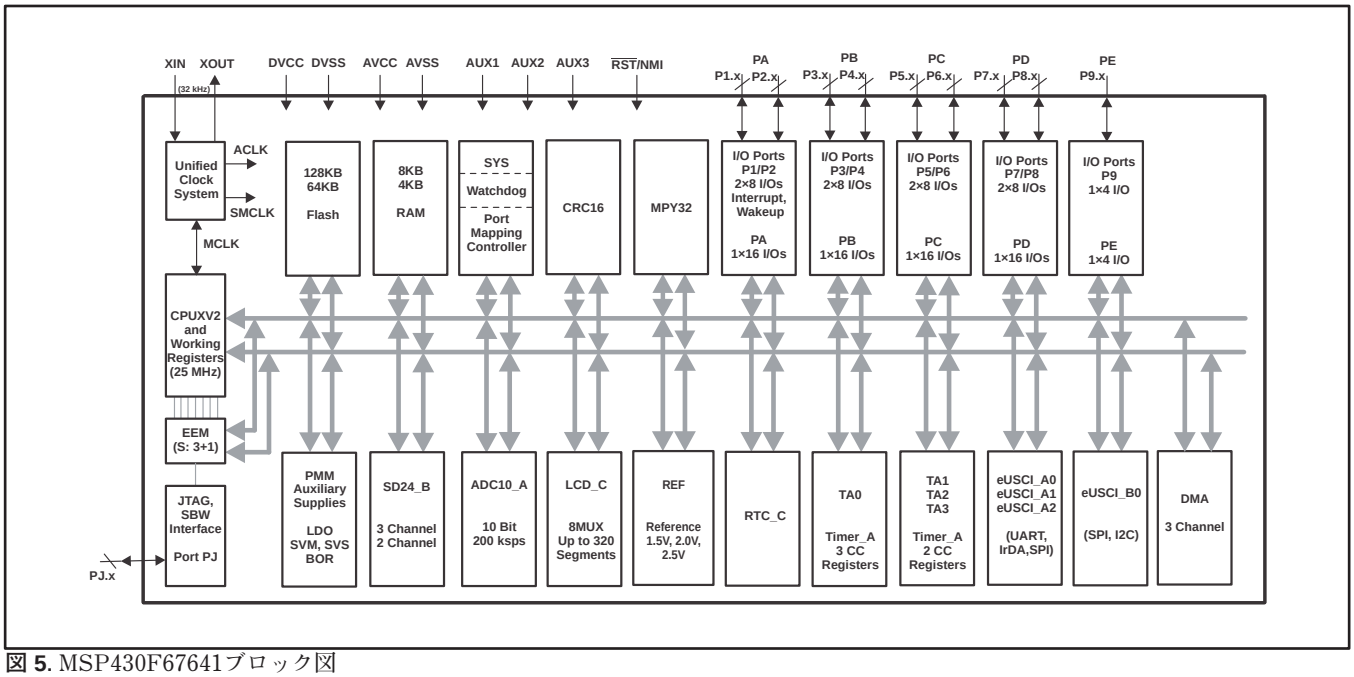

図 5. MSP430F67641ブロック図

2.1.2 AMC1304M05

AMC1304デバイスは、高精度のデルタ・シグマ（ΔΣ）変調器であり、磁気干渉に対して高い耐性を持つ容量性絶縁バリアによって、出力が入力回路から分離されています。このバリアは、UL 1577規格、VDE V-0884-10規格に従って最大7000V_{PEAK}の強化された絶縁を提供し、デバイスの寿命全体にわたって最大1.0-$kV_{AC,RMS}$の動作絶縁電圧を提供できることが認定されています。AMC1304のハイサイドでは、内蔵LDOレギュレータによって電源が供給され、これにより、4V～18Vの非レギュレーション電圧を使用してチップのハイサイドに給電が可能です。

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2.1.3 SN6501

SN6501は、絶縁型インターフェイス・アプリケーションで使用される小型の絶縁型電源向けに設計された、モノリシックな発振器/電源ドライバです。3.3Vまたは5VのDC電源から、低背のセンター・タップ付きトランスの1次側を駆動します。2次側は、トランスの巻数比に基づいて任意の絶縁電圧に設定できます。

SN6501は、発振回路に続いて、グランド基準のNチャネル電源スイッチを駆動するための相補型出力信号を供給するゲート駆動回路を搭載しています。内部ロジックにより、2つのスイッチ間でBreak-Before-Make動作が保証されます。

2.1.4 TRS3232

TRS3232デバイスは、2つのライン・ドライバと2つのライン・レシーバ、およびピン間（シリアル・ポート接続ピン、GNDを含む）に±15kVの静電気放電（ESD）保護を備えたデュアル・チャージ・ポンプ回路から構成されています。このデバイスは、Telecommunications Industry AssociationおよびElectronic Industries AllianceのTIA/EIA-232-F要件に準拠し、非同期通信コントローラとシリアル・ポート・コネクタとの間に電気的インターフェイスを提供します。チャージ・ポンプと4個の小さな外部コンデンサにより、3V～5.5Vのシングル電源で動作できます。最大250kbit/sのデータ・シグナリング・レート、および最大30V/μsのドライバ出力スルー・レートで動作します。

2.1.5 ISO7321

ISO7321は、ULに準拠した最大3kVRMSのガルバニック絶縁（1分間）を提供します。このデジタル・アイソレータには2つの絶縁されたチャネルがあり、1つは順方向チャネル、もう1つは逆方向チャネルです。各絶縁チャネルでは、ロジック入力バッファとロジック出力バッファが、二酸化ケイ素（SiO2）絶縁バリアによって分離されています。このチップは、25Mbpsのシグナリング・レートをサポートします。このチップは、3.3Vおよび5Vの電源およびロジック・レベルで動作できます。定格電圧において、ISO7321は25年以上にわたる絶縁完全性を備えています。

2.1.6 TPS76333

TPS763xxファミリのLDO電圧レギュレータは、低ドロップアウト電圧、低電力動作、および小型パッケージという利点を備えています。これらのレギュレータは、従来のLDOレギュレータと比較して、低いドロップアウト電圧および静止電流を特長とします。新しい回路設計とプロセスの革新によって、通常のPNPパス・トランジスタをPMOSパス素子で置き換えることが可能になりました。PMOSパス素子は値の小さな抵抗として機能するため、ドロップアウト電圧は非常に低く（負荷電流150mAで標準300mV、TPS76333の場合）、負荷電流に直接比例します。PMOSパス素子は電圧駆動デバイスであるため、静止電流は非常に低く（最大140 μA）、出力負荷電流の範囲全体（0mA～150mA）にわたって安定して動作します。また、TPS763xxは、レギュレータをシャットダウンするために、ロジック制御のスリープ・モードを備え、T_J = 25°Cで静止電流を最大1μAまで低減します。

2.1.7 ISO7320

ISO7320は、ULに準拠した最大3kV_{RMS}のガルバニック絶縁（1分間）を提供します。このデジタル・アイソレータは、2つの絶縁された順方向チャネルを備えています。各絶縁チャネルでは、ロジック入力バッファとロジック出力バッファが、二酸化ケイ素（SiO2）絶縁バリアによって分離されています。このチップは、25Mbpsのシグナリング・レートをサポートします。このチップは、3.3Vおよび5Vの電源およびロジック・レベルで動作できます。定格電圧において、ISO7320は25年以上にわたる絶縁完全性を備えています。

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3 System Design Theory

3.1 Design Hardware Implementation

3.1.1 Analog Inputs

The design of the front end consists of the three AMC1304 chips used for measuring current, the MSP430F67641s three digital filters that are connected to each AMC1304, a 10-bit SAR ADC (ADC10_A), and a mechanism to synchronize the digital filters with the SAR ADC.

For maximum accuracy, the AMC1304 requires that the input analog signal voltage does not exceed ±50 mV. In addition, the AMC1304 has differential inputs; therefore, the AC current signal from mains can be directly interfaced without the requirement for level shifters.

In contrast, the ADC10_A module has single-ended inputs. Therefore the ADC10_A requires that the sensed voltage is between 0-V_{REF} Volts, with the option to select the V_{REF} source and voltage in the software. As a result, after the mains voltage is divided down for sensing, the voltage front-end circuitry requires a level shifter to properly interface to the ADC10_A module.

3.1.1.1 Voltage Analog Front-End

The voltage from the mains is usually 230 V or 120 V and must be brought down to within V_{REF} Volts. The analog front-end for voltage consists of spike protection varistors followed by a voltage divider and shifter network, and a RC low-pass filter that functions like an anti-alias filter.

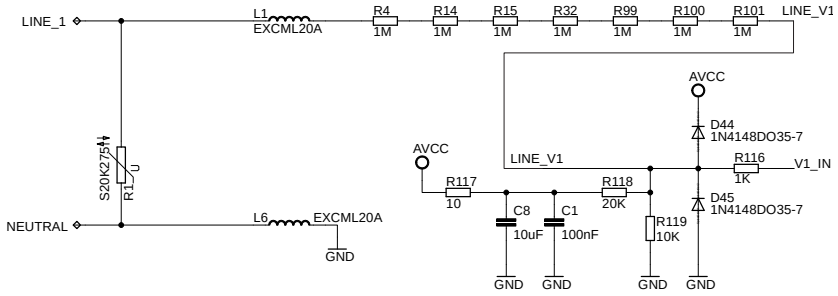

Figure 6. Analog Front-End for Voltage Inputs

Figure 6 shows the analog front-end for the voltage inputs for a mains voltage of 230 V. The voltage is brought down to a range within V_{REF} volts, where V_{REF} is selected to be the 2.0-V reference produced by the chips reference module. The maximum voltage that is fed to the ADC is usually a certain margin below the maximum V_{REF} voltage. As an example, when the 2.0-V reference is selected, the front end may be built to produce a maximum voltage of 1.4 V to 1.6 V when the maximum mains voltage is applied. This margin helps prevent ADC clipping when the system is exposed to harmonics or an over-voltage condition.

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3.1.1.2 Current Front-End

3.1.1.2.1 AMC1304 High-Side Power Supply

To sense the voltage across the shunt, the high-side of each AMC1304 device must be powered. Because each AMC1304 should be referenced from a different line voltage, a different power supply is required for each AMC1304. Figure 7 shows the designs different power options for the AMC1304.

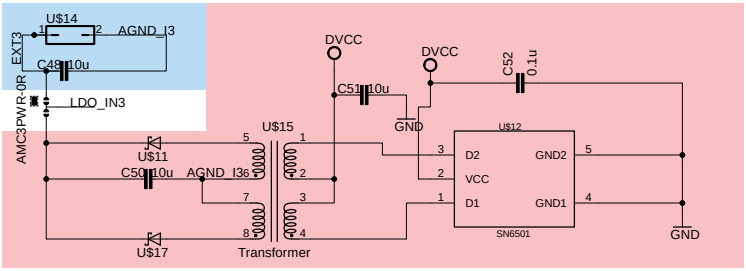

Figure 7. AMC1304 High-Side Power Options

In Figure 7, LDO_IN3 is fed directly into the AMC1304 to provide power to it. Because the AMC1304 has an integrated LDO, LDO_IN3 can be unregulated as long as the voltage fed into LDO_IN of the AMC1304 is within the 4- to 18-V operating range.

In this design, there are two options for powering the high side of the AMC1304. The first option (shaded blue in Figure 7), is to provide the necessary 4- to 18-V from an external isolated voltage supply to its associated terminal block (U$14 in Figure 7). The second option (shaded red in Figure 7), is to use the on-board isolated power supply that uses DVCC as a voltage input, a transformer, and the SN6501 transformer driver to provide an unregulated voltage into the AMC1304s integrated LDO input. In this design, a ferromagnetic core transformer is used; however, the SN6501 can also be used with an air-core transformer instead.

For further details on this power supply implementation, please refer to Section 3.6 of the *Isolated, Shunt-Based Current Sensing Reference Design* (TIDU384).

3.1.1.2.2 Current Sensing

The analog front-end for current inputs is different from the analog front-end for the voltage inputs. Figure 8 shows the analog front-end used for a current channel.

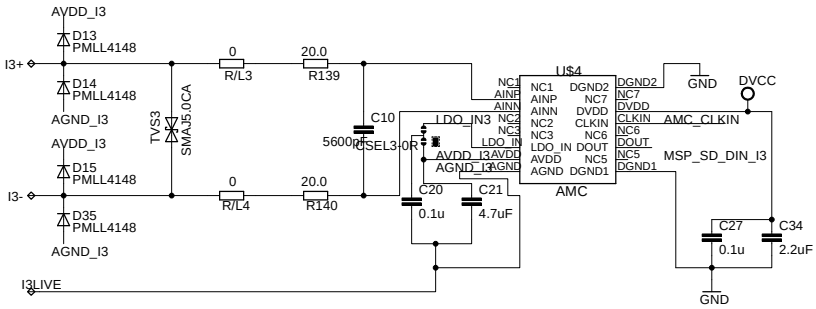

Figure 8. Analog Front-End for Current Inputs

The analog front-end for current consists of diodes and transorbs for any additional transient voltage suppression, footprints (R/L3 and R/L4) that could be replaced with inductors for EMI suppression (these footprints are populated with 0-Ω resistors by default), an anti-alias filter (R139, R140, and C10), and the AMC1304 isolated delta-sigma modulator.

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In Figure 8, the three-terminal shunt used for current measurement is to be connected at I3+, I3−, and I3Live. The value of this shunt is selected based on balancing maximizing the peak analog voltage input into the AMC1304 with minimizing the power dissipation of the shunt. In particular, for optimal accuracy, the peak DC voltage fed into the AMC1304 must be as close as possible to 50 mV without surpassing this voltage. This peak voltage is dependent on the rated maximum current of the system and the resistance of the selected shunt. For example, this design uses 400-µΩ shunts (utilized shunts are shown here: http://www.vishay.com/docs/30173/wsms3124.pdf). With these 400-µΩ shunts and a maximum RMS current of 90 A, the maximum DC voltage fed into the AMC1304 is $90 \times \sqrt{2} \times (400 \times 10^{-6}) \approx 50$ mV. To minimize the power dissipation in the shunt, a smaller value shunt can also be used. In this design, 200-µΩ shunts are also used. However, by using smaller value shunts, the voltage fed into the AMC1304 is also reduced. As a result, there is a tradeoff in accuracy. Based on the requirements of the system, the tradeoff in accuracy from using a shunt with a small resistance and the reduced power dissipation from choosing the smaller shunt must be taken into account when selecting the proper shunt value.

3.2 Metrology Software Implementation

This section discusses the software for the implementation of three-phase metrology. The first subsection discusses the setup of various peripherals of the metrology and application processors. Subsequently, the metrology software is described as two major processes: the foreground process and background process.

3.2.1 Peripherals Setup

3.2.1.1 SD24_B Setup

The MSP430F67641 has three delta-sigma data converters, with each of them having the ability to bypass its internal modulator and accept an external bit-stream to be used with its associated digital filters. This feature is used to obtain ADC samples using the bit-stream input that is output from the AMC1304.

In addition, the SD24_B has a trigger generator module that is used to trigger the ADC10, which in turn is used to sense the corresponding three voltages of the three-phase system. In this application, all of the digital filters for the SD24_B ADCs and the trigger generator are grouped together for synchronization.

The modulation clock (fM) to the trigger generator and the digital filters of the SD24_B ADCs is derived from system clock, which is configured to run at 19,798,016 Hz. Because the AMC1304 can support a clock from 5 MHz to 20 MHz, this clock can be used as the modulation clock for the AMC1304 without being further divided down. Similarly, the digital filters of the MSP430F67641s SD24_B ADC can also operate at this 20-MHz modulation clock frequency (unlike the internal modulators of the SD24_B ADC, which are bypassed in this application). In this design, the modulation clock used in the SD24_B is derived internally and output from the SD24_B module to the AMC1304 device.

To reduce the central processing unit (CPU) utilization, the effective sample rate is divided down to 4833.5 samples per second for the digital filters. This reduction is first accomplished by choosing the highest oversampling ratio (OSR) setting for the digital filters and trigger generator, which is 1024. Because the sampling frequency is defined as F_s = fM / OSR, this results in a sampling frequency of 19334. To further divide this sample rate, the software skips the ADC samples produced from the digital filter. In this design, three samples are skipped for every four samples, which results in an effective sample rate of 4833.5 samples per second for the ADC samples produced from the digital filter. For every sample that is not skipped, it is used for performing metrology calculations.

In contrast, because the trigger generator is used to keep track of when to skip samples, the trigger generator still has a triggering frequency of 19334 samples per second. Despite having a trigger frequency of 19334 , the sample rate for the voltage samples is still 4833.5 because the ADC10_A used for sensing voltages is only re-enabled for conversions one time every four samples.

In the application, the following SD24_B channels associations are used:

SD0DIO (Converter 0 digital filter) → Current I1 (Current I_A)

SD1DIO (Converter 1 digital filter) → Current I2 (Current I_B)

SD2DIO (Converter 2 digital filter) → Current I3 (Current I_C)

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3.2.1.2 ADC10_A Setup

The ADC10 is used to sample the three mains voltages and is triggered by the SD24_Bs trigger generator once every four samples. When triggered by the ΣΔ, the ADC10 enters autoscan mode and samples 6 of its channels once. In the software, the clock to the ADC10 is set to 4 MHz. The sample and hold time for each converter is 8 cycles and the conversion time is 12 cycles, which results in an approximate 20-cycle (approximately 5 µs) delay between conversion results of adjacent converters. In addition, the ADC10_A uses the 2.0-V reference from the REF module and is configured to output 10-bit results that are scaled to 16-bit twos complement numbers (ADC10DF = 1). This configuration allows the ADC results from the ADC10 to be treated as a 16-bit signed number when performing mathematical operations.

In this application, the following are the relevant ADC10 channel associations:

A10 (internal channel) → Temperature sensor

A5 → Voltage V1

A4 → Voltage V2

A3 → Voltage V3

3.2.1.3 Real Time Clock (RTC_C)

The RTC_C is a real-time clock module that is configured to give precise one second interrupts. Based off of these one second interrupts, the time and date are updated in software, as necessary.

3.2.1.4 LCD Controller (LCD_C)

The LCD controller on the MSP430F67641 can support up to 8-mux displays and 320 segments. The LCD controller is also equipped with an internal charge pump that can be used for good contrast. In the current design, the LCD controller is configured to work in 4-mux mode using 160 segments with a refresh rate set to ACLK/64, which is 512 Hz.

3.2.1.5 Port Map

The MSP430F67641 has a port mapping controller that allows a flexible mapping of digital functions to port pins. The set of digital functions that can be ported to other pins is dependent on the device. For the MSP430F67641 device in particular, the digital bit-stream inputs for the three SD24_B converters and the delta-sigma modulation clock output are all available options to port to ports P1, P2, and P3. In this design, this port mapping feature is used for providing flexibility in the PCB layout.

Using the port mapping controller, the following mappings are used:

SDCLK (SD24_B modulation clock output) → Port P2.6

SD0DIO (SD24_B Converter 0 digital filter input) → Port P3.1

SD1DIO (SD24_B Converter 1 digital filter input) → Port P3.0

SD2DIO (SD24_B Converter 2 digital filter input) → Port P2.7

3.2.1.6 DMA

The direct memory access (DMA) module is used to transfer all of the ADC10 conversion results automatically from the ADC10 to memory. Each time all of the six sampled ADC channels are converted and placed into memory, the DMAIFG flag is set; as a result, this flag can be used to determine the completion of each ADC10 autoscan sequence.

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3.2.2 Foreground Process

The foreground process includes the initial setup of the MSP430 hardware and software immediately after a device RESET. Figure 9 shows the flowchart for this process.

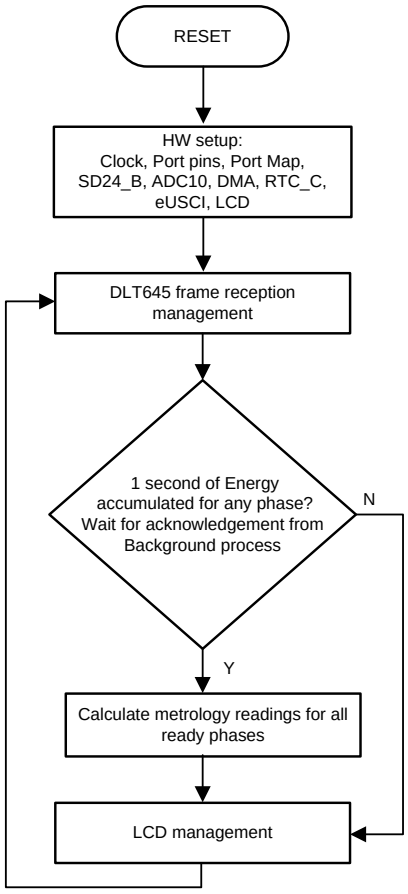

Figure 9. Foreground Process

The initialization routines involve the setup of the SD24_B module; ADC10_A module; DMA; clock system; general purpose input/output (GPIO) port pins and associated port map controller; RTC module for clock functionality; LCD; and the USCI_A0 for UART functionality.

After the hardware is setup, any received frames from the GUI are processed. Subsequently, the foreground process checks whether the background process has notified the foreground process to calculate new metering parameters. This notification is accomplished through the assertion of the “PHASE_STATUS_NEW_LOG” status flag whenever a frame of data is available for processing. The data frame consists of the processed dot products that were accumulated for one second in the background process. This is equivalent to an accumulation of 50 or 60 cycles of data synchronized to the incoming voltage signal. In addition, a sample counter keeps track of how many samples accumulate over this frame period. This count can vary as the software synchronizes with the incoming mains frequency.

The processed dot products include the V_{RMS}, I_{RMS}, active power, and reactive power. These dot products are used by the foreground process to calculate the corresponding metrology readings in real-world units. Processed voltage dot products are accumulated in 48-bit registers. In contrast, processed current dot products, active energy dot products, and reactive energy dot products are accumulated in separate 64-bit registers to further process and obtain the RMS and mean values. Using the foreground's calculated values of active and reactive power, the apparent power is calculated. The frequency (in Hz) and power factor are also calculated using parameters calculated by the background process using the formulas in Section 3.2.2.1.

The foreground process also updates the LCD. The LCD display item is changed every two seconds. Refer to Section 7.1 for more information about the different items displayed on the LCD.

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3.2.2.1 Formulae

This section briefly describes the formulas used for the voltage, current, energy, and temperature calculations.

As previous sections describe, voltage and current samples are obtained at a sampling rate of 4833.5 Hz. All of the samples that are taken in one second are kept and used to obtain the RMS values for voltage and current for each phase. The RMS values are obtained by the following formulas:

$$V_{RMS,ph} = K_{v,ph} \times \sqrt{\frac{\sum_{n=1}^{\text{Sample count}} v_{ph}(n) \times v_{ph}(n)}{\text{Sample count}}} - v_{offset,ph} \quad (2)$$

$$I_{RMS,ph} = K_{i,ph} \times \sqrt{\frac{\sum_{n=1}^{\text{Sample count}} i_{ph}(n) \times i_{ph}(n)}{\text{Sample count}}} - i_{offset,ph}$$

where

- ph = Phase parameters that are being calculated [that is, Phase A(=1), B(=2), or C(=3)]
- $V_{ph}(n)$ = Voltage sample at a sample instant n
- $V_{offset,ph}$ = Offset used to subtract effects of the additive white Gaussian noise from the voltage converter
- $I_{ph}(n)$ = Each current sample at a sample instant n
- $I_{offset,ph}$= Offset used to subtract effects of the additive white Gaussian noise from the current converter
- Sample count = Number of samples in one second
- $K_{v,ph}$ = Scaling factor for voltage
- $K_{i,ph}$ = Scaling factor for each current (3)

Power and energy are calculated for a frames worth of active and reactive energy samples. These samples are phase corrected and passed on to the foreground process, which uses the number of samples (sample count) to calculate phase active and reactive powers through the following formulas:

$$P_{ACT,ph} = K_{ACT,ph} \frac{\sum_{n=1}^{\text{Sample count}} v(n) \times i_{ph}(n)}{\text{Sample count}} \quad (4)$$

$$P_{REACT,ph} = K_{REACT,ph} \frac{\sum_{n=1}^{\text{Sample count}} v_{90}(n) \times i_{ph}(n)}{\text{Sample count}} \quad (5)$$

$$P_{APP,ph}{}^2 = \sqrt{P_{ACT,ph}{}^2 + P_{REACT,ph}{}^2}$$

where

- $V_{90}(n)$ = Voltage sample at a sample instant ‘n’ shifted by 90°
- $K_{ACT,ph}$ = Scaling factor for active power
- $K_{REACT,ph}$ = Scaling factor for reactive power (6)

Please note that for reactive energy, the 90° phase shift approach is used for two reasons:

1. This approach allows accurate measurement of the reactive power for very small currents.
2. This approach conforms to the measurement method specified by IEC and ANSI standards.

The calculated mains frequency is used to calculate the 90 degrees-shifted voltage sample. Because the frequency of the mains varies, it is important to first measure the mains frequency accurately to phase shift the voltage samples accordingly (see Section 3.2.3.1.2 for details).

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To get an exact 90° phase shift, interpolation is used between two samples. For these two samples, a voltage sample slightly more than 90 degrees before the current sample and a voltage sample slightly less than 90 degrees before the current sample are used. The application's phase shift implementation consists of an integer part and a fractional part. The integer part is realized by providing an N samples delay. The fractional part is realized by a one-tap FIR filter. In the software, a lookup table provides the filter coefficients that are used to create the fractional delays.

In addition to calculating the per-phase active and reactive powers, the cumulative sum of these parameters are also calculated by the following Equation 7, Equation 8, and Equation 9:

$$P_{ACT,Cumulative} = \sum_{ph=1}^{3} P_{ACT,ph} \quad (7)$$

$$P_{REACT,Cumulative} = \sum_{ph=1}^{3} P_{REACT,ph} \quad (8)$$

$$P_{APP,Cumulative} = \sum_{ph=1}^{3} P_{APP,ph} \quad (9)$$

Using the calculated powers, energies are calculated by the following formulas in Equation 10:

$$E_{ACT,ph} = P_{ACT,ph} \times Samplecount$$
$$E_{REACT,ph} = P_{REACT,ph} \times Samplecount$$
$$E_{APP,ph} = P_{APP,ph} \times Samplecount \quad (10)$$

From there, the energies are also accumulated to calculate the cumulative energies, by the following Equation 11, Equation 12, and Equation 13:

$$E_{ACT,Cumulative} = \sum_{ph=1}^{3} E_{ACT,ph} \quad (11)$$

$$E_{REACT,Cumulative} = \sum_{ph=1}^{3} E_{REACT,ph} \quad (12)$$

$$E_{APP,Cumulative} = \sum_{ph=1}^{3} E_{APP,ph} \quad (13)$$

The calculated energies are then accumulated into buffers that store the total amount of energy consumed since system reset. Please note that these energies are different from the working variables used to accumulate energy for outputting energy pulses. There are four sets of buffers that are available: one for each phase and one for the cumulative of the phases. Within each set of buffers, the following energies are accumulated:

1. Active import energy (active energy when active energy ≥ 0)
2. Active export energy (active energy when active energy < 0)
3. React. Quad I energy (reactive energy when reactive energy ≥ 0 and active power ≥ 0; inductive load)
4. React. Quad II energy (reactive energy when reactive energy ≥ 0 and active power < 0; capacitive generator)
5. React. Quad III energy (reactive energy when reactive energy < 0 and active power < 0; inductive generator)
6. React. Quad IV energy (reactive energy when reactive energy < 0 and active power ≥ 0; capacitive load)
7. App. import energy (apparent energy when active energy ≥ 0)
8. App. export energy (apparent energy when active energy < 0)

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The background process also calculates the frequency in terms of samples per mains cycle. The foreground process then converts this samples per mains cycle to Hertz by the following formula:

$$\text{Frequency (Hz)} = \frac{\text{Sample Rate (samples / second)}}{\text{Frequency (samples / cycle)}} \tag{14}$$

After the active power and apparent power have been calculated, the absolute value of the power factor is calculated. In the system's internal representation of power factor, a positive power factor corresponds to a capacitive load; a negative power factor corresponds to an inductive load. The sign of the internal representation of power factor is determined by whether the current leads or lags voltage, which is determined in the background process. Therefore, the internal representation of power factor is calculated by the following formula:

$$\text{Internal Representation of Power Factor} = \begin{cases} \dfrac{P_{Act}}{P_{Apparent}}, \text{ if capacitive load} \\ -\dfrac{P_{Act}}{P_{Apparent}}, \text{ if inductive load} \end{cases} \tag{15}$$

In addition, temperature is also calculated in the software. Temperature is calculated using the TLV entries on the MSP430F67641 and is calculated in units of Celsius. The measured values for 30°C ±3°C and 85°C ±3°C for the 2.0-V reference are used for calculating temperature. The following Equation 16 shows the exact formula that is used to calculate temperature:

$$\text{Temp} = \left(\text{ADC(raw)} - \text{CAL\_ADC\_20T30}\right) \times \left(\frac{85 - 30}{\text{CAL\_ADC\_20T85} - \text{CAL\_ADC\_20T30}}\right) \tag{16}$$

3.2.3 Background Process

Figure 10 shows the background process, which mainly deals with timing critical events in software. The background process uses the SD24_B trigger generation to collect voltage and current samples. The SD24_B provides a trigger 19334 times per second. For a certain number of these triggers, sample processing is done on the previously obtained voltage and current samples. This sample processing is done by the "per_sample_dsp ()" function. After sample processing, the background process uses the "per_sample_energy_pulse_processing ()" for the calculation and output of energy-proportional pulses. In the software, the "SAMPLES_SKIPPED" macro determines how many triggers to skip between successive calculations. Because the default value of this macro is 3, sample processing and energy pulse processing is done once every four SD24_B triggers. As a result, three out of four current samples are skipped and not used for calculations, which leads to an effective sample rate of 4833.5 samples per second for the current channels.

To keep track of when to skip samples, the "sample_number" variable is used to keep track of how many trigger pulses have been produced since the last time sample and energy pulse processing has occurred. Due to the high frequency of triggers, triggers may occur in the middle of sample processing within the SD24_B ISR. Because interrupts are disabled within the ISR, the trigger pulse flag (SD24TRGIFG) is checked in various places within the ISR code to keep track of triggers that occur during the SD24_B interrupt. These checks are done by calling the "update_sample_count ()" function (Figure 11). The places where the update_sample_count is called are set so that the time between checks is less than the period of the triggers.

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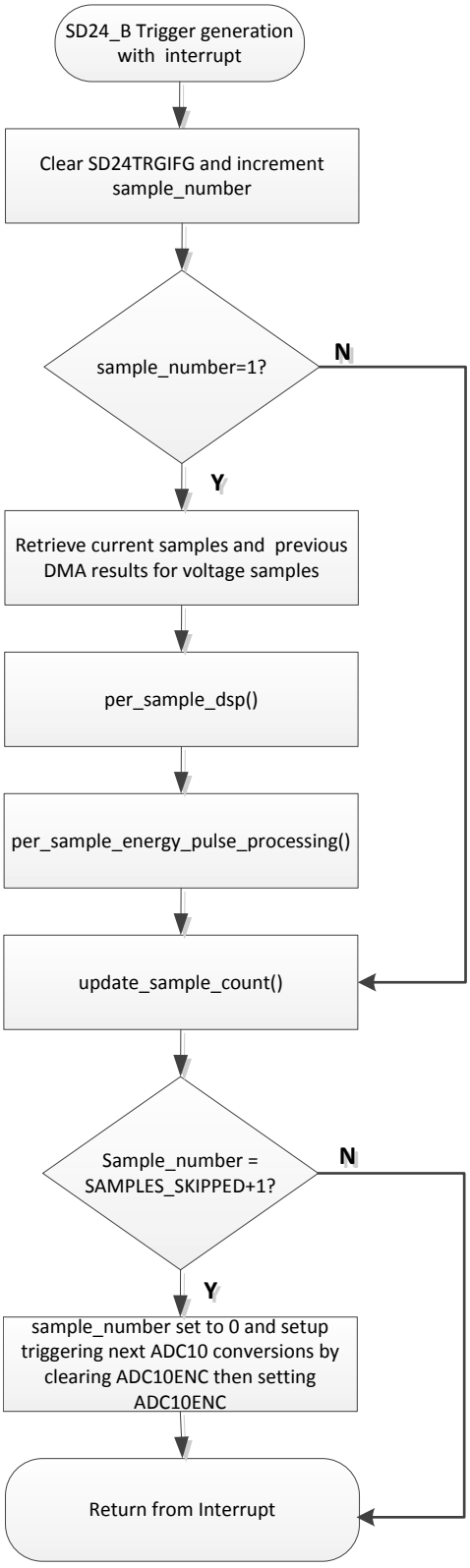

Figure 10. Background Process

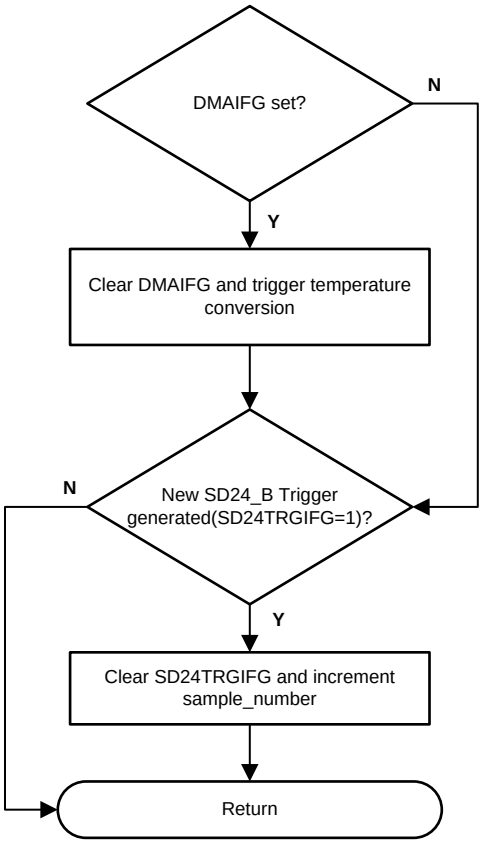

Figure 11. update_sample_count ()

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Similar to the current samples, the sample rate for voltage samples is also 4833.5 samples per second; however, unlike the current samples, this sample rate is not achieved by skipping samples. Instead, the sample rate is caused by only re-enabling the ADC10 for conversions to measure the phase voltage channels only once every SAMPLES_SKIPPED + 1 samples. Re-enabling the ADC10 for conversions is accomplished by clearing and then setting the ADC10ENC bit. As Figure 10 shows, this clearing and setting is done when the sample_number = (SAMPLES_SKIPPED + 1). As a result, the ADC10 converts the voltage samples in parallel to the sample processing done in the background process. Figure 12 shows this parallel activity. In Figure 12, the gray containers represent items that are automatically done by the configuration of the ADC10, DMA, and ΣΔ modules. For these gray items, CPU intervention is not required.

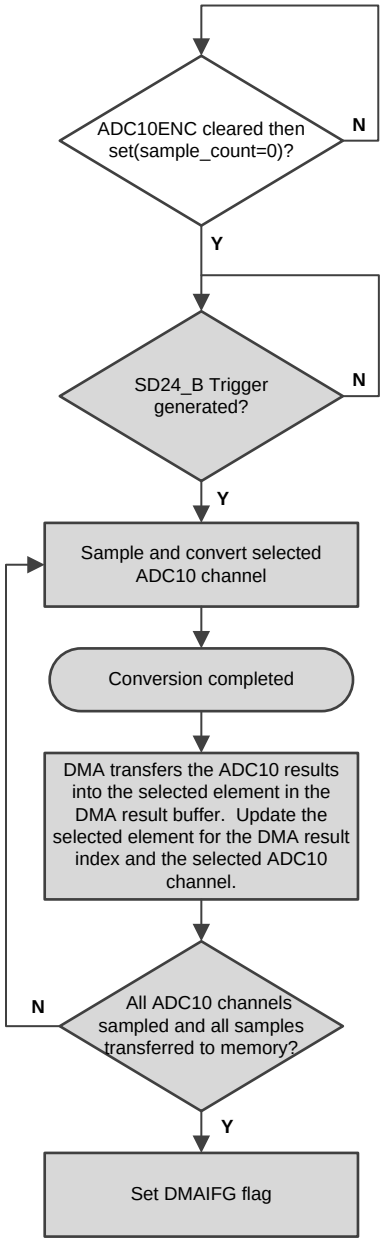

Figure 12. ADC10 Triggering Process

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As Figure 12 represents, whenever the ADC10 is triggered, the ADC10 enters autoscan mode and samples six ADC channels once. After each channel has a conversion result, the DMA automatically places these results in memory and the next channel's conversion is automatically started. For each converter, there is a memory location that stores the conversion results for that particular converter. The procedure of sampling a converter and storing the results in memory is repeated until the last converter (ADC10INCH = 0) is sampled. Because the clock to the ADC10 is set to 4 MHz, the sample and hold time for each converter is 8 cycles, and the conversion time is 12 cycles, there is an approximate 20-cycle (approximately 5-µs) delay between the conversion results of adjacent converters.

Once all of the ADC10 channels are sampled and the samples are transferred to memory, the DMAIFG flag is set to indicate that the ADC10 has completed its operation and may be used for other conversions.

To sense the internal temperature sensor using the ADC10, a recommended sample period of at least 30 µs must be used. As a result, the autoscan mode that is used to measure the phase voltages cannot be extended to also measure the temperature channel. To prevent this loss of temperature channel measurement, a single conversion of the ADC10 temperature channel is triggered (see Figure 13). The temperature conversion is triggered when the DMAIFG flag is asserted (see Figure 12) to indicate that the phase voltages have just been completely converted and transferred to memory so that other conversions can be started. The check for the completion of the phase voltage sampling is done within the update_sample_count function (see Figure 11). Because the update_sample_count function is called multiple times within the SD24_B interrupt, this ensures that the temperature conversion can be started relatively quickly. After a temperature reading has been received and its associated ISR has been called, temperature reading is stored in memory and the ADC10 settings are then reset to support autoscan mode for the next conversion.

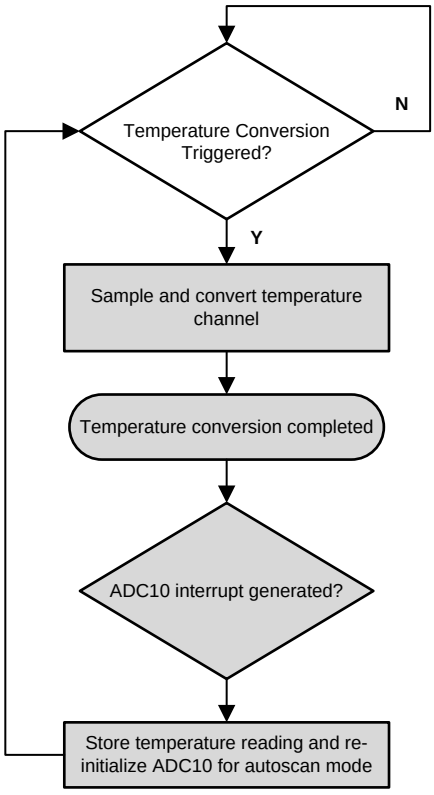

Figure 13. Temperature Triggering Mechanism

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3.2.3.1 per_sample_dsp ()

Figure 14 shows the flowchart for the per_sample_dsp () function. The per_sample_dsp function() is used to calculate intermediate dot product results that are fed into the foreground process for the calculation of metrology readings. The ADC10 is configured to represent the 10-bit voltage results as a 16-bit signed result. Because 16-bit voltage samples are used, the voltage samples are further processed and accumulated in dedicated 48-bit registers. In contrast, as a result of using an oversampling ratio of 1024, current samples have more bits. Because many of these bits are unnecessary, they are shifted out so that 24-bit current samples are used. As a result, the current samples are processed and accumulated in dedicated 64-bit registers. Per-phase active power and reactive power are also accumulated in 64-bit registers.

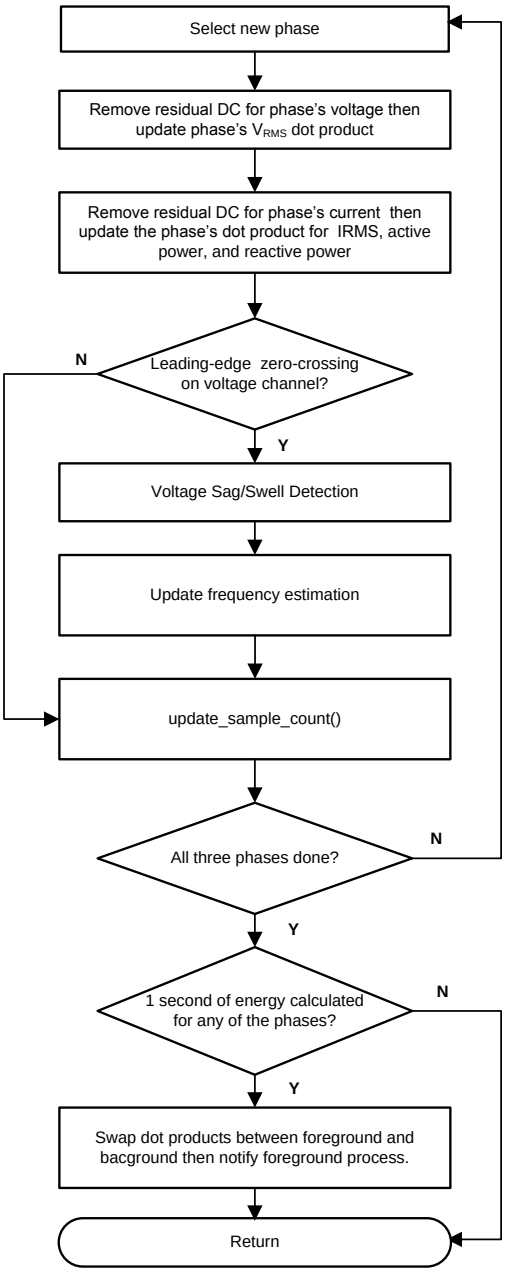

Figure 14. per_sample_dsp ()

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After sufficient samples (approximately one seconds worth) have been accumulated, then the foreground function is triggered to calculate the final values of V_{RMS}; I_{RMS}; active, reactive, and apparent powers; active, reactive, and apparent energy; and frequency, temperature, and power factor. In the software, there are two sets of dot products: at any given time, one is used by the foreground for calculation and the other used as the working set by the background. After the background process has sufficient samples, it swaps the two dot products so that the foreground uses the newly acquired dot products just calculated by the background process and the background process uses a new empty set to calculate the next set of dot products.

Whenever there is a leading-edge zero-crossing (− to + voltage transition) on a voltage channel, the per_sample_dsp function () is also responsible for updating the corresponding phases frequency (in samples per cycle) and voltage sag and swell conditions. For the sag conditions, whenever the RMS voltage is below a certain user-defined threshold percentage, the number of mains cycles where this condition persists is logged as the sag duration. The number of periods in time where there was a sag condition is logged as the sag events count. Please note that the sag duration corresponds to the total number of cycles in a sag condition since being reset, and is therefore, not cleared for every sag event. Also, when the RMS voltage is above a certain threshold percentage, swell events and duration are logged in a similar way.

3.2.3.1.1 Voltage and Current Signals

The output of each SD24_B digital filter and ADC10 converter is a signed integer and any stray DC or offset value on these converters are removed using a DC tracking filter. Separate DC estimates for all voltages and currents are obtained using the filter and voltage and current samples, respectively. These estimates are then subtracted from each voltage and current sample. The resulting instantaneous voltage and current samples are used to generate the following intermediate dot product results:

- Accumulated squared values of voltages and currents, which is used for V_{RMS} and I_{RMS} calculations, respectively.
- Accumulated energy samples to calculate active energies.
- Accumulated energy samples using current and 90° phase shifted voltage to calculate reactive energies.

These accumulated values are processed by the foreground process.

3.2.3.1.2 Frequency Measurement and Cycle Tracking

The instantaneous voltage of each phase is accumulated in 48-bit registers. In contrast, the instantaneous current, active power, and reactive power are accumulated in 64-bit registers. A cycle tracking counter and sample counter keep track of the number of samples accumulated. When approximately one seconds worth of samples has been accumulated, the background process switches the foreground and background and then notifies the foreground process to produce the average results such as RMS and power values. Cycle boundaries are used to trigger the foreground averaging process because this process produces very stable results.

For frequency measurements, a straight-line interpolation is used between the zero-crossing voltage samples. Figure 15 shows the samples near a zero cross and the process of linear interpolation.

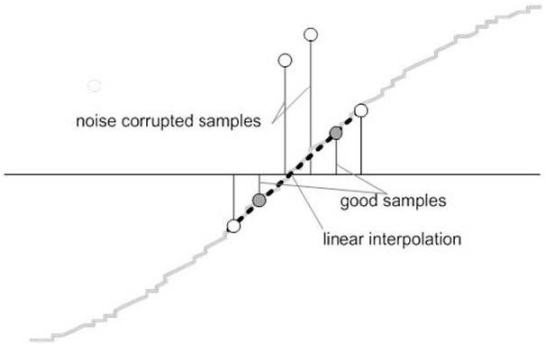

Figure 15. Frequency Measurement

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Because noise spikes can also cause errors, the application uses a rate of change check to filter out the possible erroneous signals and make sure that the two points that are interpolated are from genuine zero crossing points. For example, with two negative samples, a noise spike can make one of the samples positive, thereby making the negative and positive pair look as if there is a zero crossing.

The resultant cycle-to-cycle timing goes through a weak low-pass filter to further smooth out cycle-to-cycle variations. This filtering results in a stable and accurate frequency measurement that is tolerant of noise.

3.2.3.2 LED Pulse Generation (per_sample_energy_pulse_processing)

In electricity meters, the active energy consumed is normally measured in a fraction of kilowatt-hour (kWh) pulses. This information can be used to calibrate any meter for accurate measurement. Typically, the measuring element (the MSP430 microcontroller) is responsible for generating pulses proportional to the energy consumed. To serve both these tasks efficiently, pulse generation must be accurate with relatively little jitter. Although time jitters are not an indication of bad accuracy, they give a negative indication of the overall accuracy of the meter, which is why the jitter is averaged out.

This application uses average power to generate these energy pulses. The average power (calculated by the foreground process) accumulates every time the per_sample_energy_pulse_processing is called, thereby spreading the accumulated energy from the previous one second time frame evenly for each interrupt in the current one second time frame. This process is equivalent to converting it to energy. When the accumulated energy crosses a threshold, a pulse is generated. The amount of energy above this threshold is kept and a new energy value is added on top of the energy above the threshold in the next interrupt cycle. Because the average power tends to be a stable value, this way of generating energy pulses is very steady and free of jitter.

The threshold determines the energy "tick" specified by meter manufacturers and is a constant. The “tick” is usually defined in pulses per kWh or just in kWh. One pulse is generated for every energy "tick". For example, in this application, the number of pulses generated per kWh is set to 6400 for active and reactive energies. The energy "tick" in this case is 1 kWh/6400. Energy pulses are generated and available on a header and also through light-emitting diodes (LEDs) on the board. GPIO (port) pins are used to produce the pulses.

In the EVM, the LEDs that are labeled “Phase 1”, “Phase 2”, “Phase 3”, and “Active” correspond to the active energy consumption for phase A, phase B, phase C, and the cumulative three-phase sum, respectively. “Reactive” corresponds to the cumulative three-phase reactive energy sum. The number of pulses per kWh and each pulse duration can be configured in software. Figure 16 shows the flow diagram for pulse generation. This flow diagram is valid for pulse generation of individual or accumulative phase active, reactive, and apparent energy.

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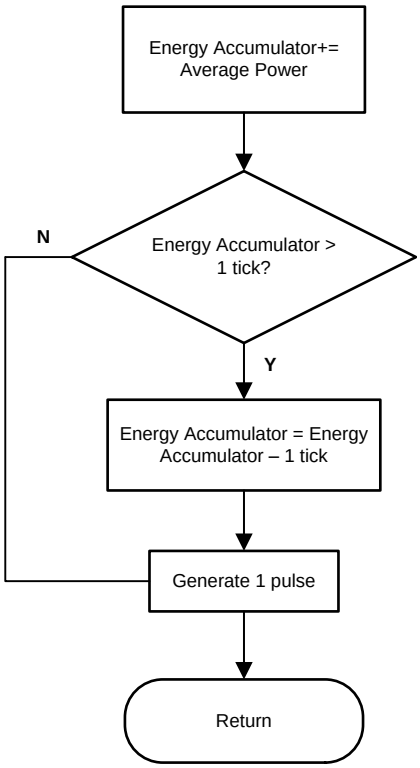

Figure 16. Pulse Generation for Energy Indication

The average power is in units of 0.001 W and the 1-kWh threshold is defined as:

1 kWh threshold = (1 / 0.001) × 1 kW × (number of interrupts per second) × (number of seconds in one hour) = 1000000 × 4833.5 × 3600 = 0xFD36494F600

3.2.3.3 Phase Compensation

In order to ensure accurate measurements, the relative phase shift between voltage and current samples must be compensated. This phase shift may be caused by the passive components of the voltage and current input circuit or even the sequential sampling on the voltage channel.

The implementation of the phase shift compensation consists of an integer part and a fractional part. The integer part is realized by providing an N samples delay. The fractional part is realized by a one-tap finite impulse response (FIR) filter that interpolates between two samples, similar to the FIR filter used for providing 90°-shifted voltage samples for reactive energy measurements. In the software, a lookup table provides the filter coefficients that are used to create the fractional delays. The lookup table provides fractional phase shifts as small as 1/256th of a sample. The 4833.5 sample rate used in this application corresponds to a 0.0145° degree resolution at 50 Hz. In addition to the filter coefficients, the lookup table also has an associated gain variable for each set of filter coefficients. This gain variable is used to cancel out the resulting gain from using a certain set of filter coefficients.

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4 Getting Started Hardware

The following figures of the EVM best describe the hardware: Figure 17 is the top view of the energy measurement system and Figure 18 shows the location of various pieces of the EVM based on functionality.

Figure 17. Top View TIDA-00601 Design

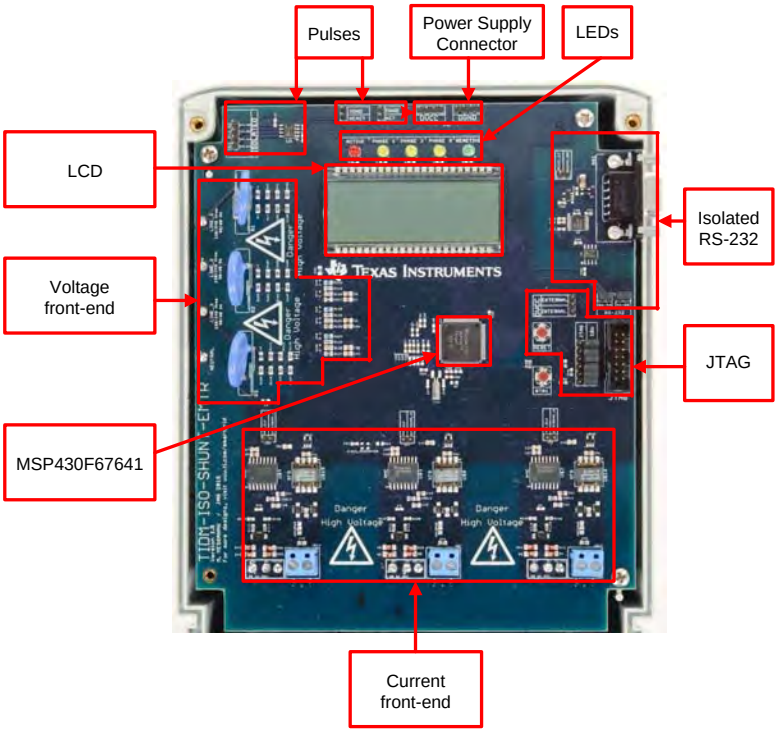

Figure 18. Top View of TIDA-00601 Design With Components Highlighted

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4.1 Connections to the Test Setup for AC Voltages

AC voltages can be applied to the board for testing purposes at these points:

- Pad “LINE1” corresponds to the line connection for phase A.
- Pad “LINE2” corresponds to the line connection for phase B.
- Pad “LINE3” corresponds to the line connection for phase C.
- Pad “Neutral” corresponds to the neutral voltage. The voltage between any of the three line connections to the neutral connection must not exceed 230-V AC at 50/60 Hz.
- I1+, I1−, and I1Live are connected to the output terminals of the shunt that is used for measuring the current for Phase A. When a shunt is selected, the differential voltage that is output across I1+ and I1− must not exceed 50 mV.
- I2+, I2−, and I2Live are connected to the output terminals of the shunt that is used for measuring the current for Phase B. When a shunt is selected, the differential voltage that is output across I2+ and I2− must not exceed 50 mV.
- I3+, I3−, and I3Live are connected to the output terminals of the shunt that is used for measuring the current for Phase C. When a shunt is selected, the differential voltage that is output across I3+ and I3− must not exceed 50 mV.

Figure 19 and Figure 20 show the various connections that must be made to the test setup for proper functionality of the EVM. When a test AC source must be connected, the connections have to be made according to the EVM design. Figure 19 shows the connections from the top view. VA+, VB+, and VC+ correspond to the line voltages for phases A, B, and C, respectively. VN corresponds to the neutral voltage from the test AC source.

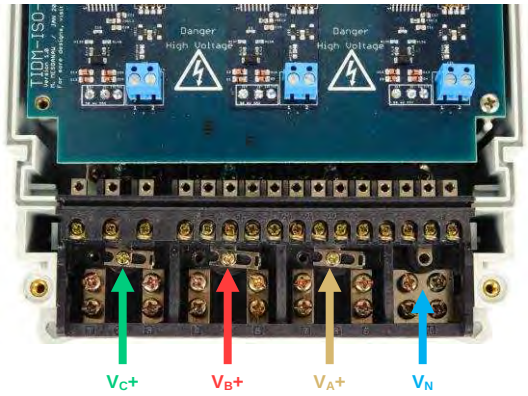

Figure 19. Top View of EVM With Test Setup Connections

Figure 20 shows the connections from the front view. IA+ and IA− correspond to the current inputs for phase A, IB+, and IB− correspond to the current inputs for phase B; IC+ and IC− correspond to the current inputs for phase C. VN corresponds to the neutral voltage from the test setup.

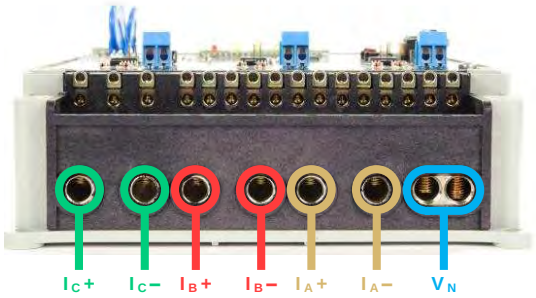

Figure 20. Front View of EVM With Test Setup Connections

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4.2 Power Supply Options and Jumper Settings

The entire board is powered by a single DC voltage rail (DVCC), which can be derived either by JTAG or external power. Various jumper headers and jumper settings are present to add to the flexibility to the board. Some of these headers require that jumpers be placed appropriately for the board to correctly function. Table 1 indicates the functionality of each jumper on the board.

Table 1. Header Names and Jumper Settings

HEADER/HEADER OPTION NAME	TYPE	MAIN FUNCTIONALITY	VALID USE-CASE	COMMENTS
ACT (Not isolated, do not probe)	1-pin header	Active energy pulses (WARNING)	Probe between here and ground for cumulative three-phase active energy pulses.	This header is not isolated from AC voltage, so do not connect measuring equipment unless isolators external to the EVM are available. See Isolated ACT instead.
AMC1PWR	3-pad jumper resistor footprint	Selection for the AMC1304 high-side power supply for Phase A	This header is used to select the power source for the AMC1304 associated with Phase A.	To enable powering the high-side using the on-board isolated power supply, place a 0-Ω resistor on the two top-most terminals (when the board is oriented as Figure 17 shows). To enable powering the high side by providing 4 V to 18 V directly to the U$16-terminal block , place a 0-Ω resistor on the two bottom-most terminals (when the board is oriented as Figure 17 shows).
AMC2PWR	3-pad jumper resistor footprint	Selection for the AMC1304 high-side power supply for Phase B	This header is used to select the power source for the AMC1304 associated with Phase B.	To enable powering the high side using the on-board isolated power supply, place a 0-Ω resistor on the two top-most terminals (when the board is oriented as Figure 17 shows). To enable powering the high side by providing 4 V to 18 V directly to the U$8-terminal block , place a 0-Ω resistor on the two bottom-most terminals (when the board is oriented as Figure 17 shows).
AMC3PWR	3-pad jumper resistor footprint	Selection for the AMC1304 high-side power supply for Phase C	This header is used to select the power source for the AMC1304 associated with Phase C.	To enable powering the high side using the on-board isolated power supply, place a 0-Ω resistor on the two top-most terminals (when the board is oriented as Figure 17 shows). To enable powering the high side by providing 4 V to 18 V directly to the U$15-terminal block , place a 0-Ω resistor on the two bottom-most terminals (when the board is oriented as Figure 17 shows).

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Table 1. Header Names and Jumper Settings (continued)

HEADER/HEADER OPTION NAME	TYPE	MAIN FUNCTIONALITY	VALID USE-CASE	COMMENTS
AMC_CLK (Not isolated, do not probe)	1-pin header	Modulation clock fed into the AMC1304	Probe between here and ground for the clock fed into the AMC1304 chips. An external clock can also be fed into this header to be used as the modulation clock; however, the software must be changed to accept a modulation clock input instead of providing one from the SD24_B.	Each AMC1304 has its own associated AMC_CLK header. However, all AMC_CLK headers are connected to each other.
BIT-STREAM_I1 (Not isolated, do not probe without isolated equipment)	1-pin header	Bit-stream output for the AMC associated with Phase A.	Probe between here and ground for the bit-stream output from the AMC1304 chip associated with Phase A.	
BIT-STREAM_I2 (Not isolated, do not probe without isolated equipment)	1-pin header	Bit-stream output for the AMC associated with Phase B.	Probe between here and ground for the bit-stream output from the AMC1304 chip associated with Phase B.	
BIT-STREAM_I3 (Not isolated, do not probe without isolated equipment)	1-pin header	Bit-stream output for the AMC associated with Phase C.	Probe between here and ground for the bit-stream output from the AMC1304 chip associated with Phase C.	
CSEL1	3-pad jumper resistor footprint	Capacitor Connection Select for the AMC1304 for Phase A	For this design, place a 0-Ω resistor on the two left-most terminals (when the board is oriented as Figure 17 shows).	
CSEL2	3-pad jumper resistor footprint	Capacitor Connection Select for the AMC1304 for Phase B	For this design, place a 0-Ω resistor on the two left-most terminals(when the board is oriented as Figure 17 shows).	
CSEL3	3-pad jumper resistor footprint	Capacitor Connection Select for the AMC1304 for Phase C	For this design, place a 0-Ω resistor on the two left-most terminals(when the board is oriented as Figure 17 shows).	
DGND (Not isolated, do not probe)	Header	Ground voltage header (WARNING)	Not a jumper header, probe here for GND voltage. Connect negative terminal of bench or external power supply when powering the board externally.	Do not probe if AC mains is not isolated.
DVCC (Not isolated, do not probe)	Header	VCC voltage header (WARNING)	Not a jumper header, probe here for VCC voltage. Connect positive terminal of bench or external power supply when powering the board externally.	Do not probe if AC mains is not isolated.
DVCC EXTERNAL (Do not connect JTAG if AC mains is not isolated)	Jumper header option	JTAG external power selection option (WARNING)	Place a jumper at this header option to select external voltage for JTAG programming.	This jumper option and the DVCC INTERNAL jumper option comprise one three-pin header used to select the voltage source for JTAG programming.

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Table 1. Header Names and Jumper Settings (continued)

HEADER/HEADER OPTION NAME	TYPE	MAIN FUNCTIONALITY	VALID USE-CASE	COMMENTS
DVCC INTERNAL (Do not connect JTAG if AC mains is not isolated; isolated JTAG is fine)	Jumper header option	JTAG internal power selection option (WARNING)	Place a jumper at this header option to power the board using JTAG and to select the voltage from the USB FET for JTAG programming.	This jumper option and the DVCC EXTERNAL jumper option comprise one three-pin header used to select the voltage source for JTAG programming.
ISO_ACT	1-pin header	Isolated active energy pulses	Probe between here and ground for cumulative three-phase active energy pulses.	This header is isolated from AC voltage so it is safe to connect to scope or other measuring equipment because isolators are already present. However, either 3.3 V or 5 V must be applied between ISO_GND and ISO_VCC to produce pulses on this pin. The produced pulses have a logical high voltage that is equal to the voltage applied between ISO_GND and ISO_VCC.
ISO_GND	1-pin header	Isolated ground For energy pulses	Ground connection for the isolated active and reactive energy pulses.	
ISO_REACT	1-pin header	Isolate reactive energy pulses	Probe between here and ground for cumulative three-phase reactive energy pulses.	This header is isolated from AC voltage so it is safe to connect to scope or other measuring equipment since isolators are already present. However, either 3.3 V or 5 V must be applied between ISO_GND and ISO_VCC to produce pulses on this pin. The produced pulses have a logical high voltage that is equal to the voltage applied between ISO_GND and ISO_VCC.
ISO_VCC	1-pin header	Isolated VCC for energy pulses	VCC connection for the isolated active and reactive energy pulses.	Either 3.3 V or 5 V must be applied between ISO_GND and ISO_VCC to produce isolated active and reactive pulses on the respective isolated ISO_ACT and ISO_REACT pins. The produced pulses have a logical high voltage that is equal to the voltage applied between ISO_GND and ISO_VCC.
JTAG (Do not connect JTAG if AC mains is not isolated)	Jumper header option	4-wire JTAG programming option (WARNING)	Place jumpers at the JTAG header options of all of the six JTAG communication headers to select 4-wire JTAG.	There are six headers that jumpers must be placed at to select a JTAG communication option. Each of these six headers has a JTAG option and an SBW option to select either 4-wire JTAG or SBW. To enable 4-wire JTAG, all of these headers must be configured for the JTAG option. To enable SBW, all of the headers must be configured for the SBW option.

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Table 1. Header Names and Jumper Settings (continued)

HEADER/HEADER OPTION NAME	TYPE	MAIN FUNCTIONALITY	VALID USE-CASE	COMMENTS
R16 Resistor	2-pad jumper resistor footprint	External clock generation selection	This design has a footprint that allows placing a clock generator (footprint is labeled CLOCK_GENERATOR on PCB) on the board so that it can be used for the modulation clock. When using this option, populating the clock generator footprint (not populated by default) and placing a 0-Ω resistor at R16 (also not populated by default) connects the clock generator to the AMC1304 and MSP430F67641.	If the external clock generator is used as the modulation clock of the AMC1304 and MSP430F67641, the software must be changed for the SD24_B to use an external clock and to prevent outputting the SD24_B clock.
REACT (Not isolated, do not probe)	1-pin header	Reactive energy pulses (WARNING)	Probe between here and ground for cumulative three-phase reactive energy pulses.	This header is not isolated from AC voltage so do not connect measuring equipment unless isolators external to the EVM are available. See isolated REACT instead.
RS232_3.3	1-pin header	Voltage source harvested from RS-232 line	Voltage source that is used to power the TRS3232 and ISO7321 for isolated RS-232 communication. This voltage source is harvested from the RS-232 line.	
RS232_GND	1-pin header	Ground connection for the isolated RS-232	Ground connection for the isolated RS-232 circuitry.	
RX_EN	Jumper header	RS-232 receive enable	Place a jumper here to enable receiving characters using RS-232.	
SBW (Do not connect JTAG if AC mains is not isolated)	Jumper header option	SBW JTAG programming option (WARNING)	Place jumpers at the SBW header options of all of the six JTAG communication headers to select SBW.	There are six headers that jumpers must be placed at to select a JTAG communication. Each of these six headers that have a JTAG option and a SBW option to select either 4-wire JTAG or SBW. To enable 4-wire JTAG, all of these headers must be configured for the JTAG option. To enable SBW, all of the headers must be configured for the SBW option.
TX_EN	Jumper header	RS-232 transmit enable	Place a jumper here to enable RS-232 transmissions.	

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5 Getting Started Firmware

The source code is developed in the IAR™ environment using IAR compiler version 6.x. Earlier versions of IAR cannot open the project files. When the project is loaded in IAR version 6.x or later, the integrated development environment (IDE) prompts the user to create a backup. Click "YES" to proceed. There are four main parts to the energy metrology software:

- The toolkit that contains a library of mostly mathematics routines
- The metrology code that is used for calculating metrology parameters
- The application code that is used for the host-processor functionality of the system (that is, communication, LCD display, RTC setup, and so forth)
- The GUI that is used for calibration

Figure 21 shows the contents of the source folder.

Figure 21. Source Folder Structure

Within the *emeter-app-67641* folder in the *emeter-app* folder, the *emeter-app-67641.ewp* project corresponds to the application code. Similarly, within the *emeter-metrology-67641* folder in the *emeter-metrology* folder, the *emeter-metrology-67641.ewp* project corresponds to the portion of the code for metrology. Additionally, the folder *emeter-toolkit-67641* within the *emeter-toolkit* has the corresponding toolkit project file *emeter-toolkit-67641.ewp*. For first-time use, TI recommends that all three projects be completely rebuild by performing the following steps:

1. Open the IAR IDE.
2. Open the F67641 workspace, which is located in the *Source* folder.
3. Within IARs workspace window, click the *Overview* tab to have a list view of all the projects.
4. Right-click the *emeter-toolkit-67641* option in the workspace window and select *Rebuild All*, as Figure 22 shows.
5. Right-click the *emeter-metrology-67641* option in the workspace window and select *Rebuild All*, as Figure 23 shows.
6. Within IARs workspace window, click the *emeter-app-67641* tab.
7. Within the workspace window, select *emeter-app-67641*, click *Rebuild All* as Figure 24 shows, and then download this project onto the MSP430F67641 device.

Please note that if any changes are made to any of the files in the toolkit project and the project is compiled, the metrology project must be recompiled. After recompiling the metrology project, the application project must then be recompiled. Similarly, if any changes are made to any of the files in the metrology project and the project is compiled, the application project must then be recompiled.

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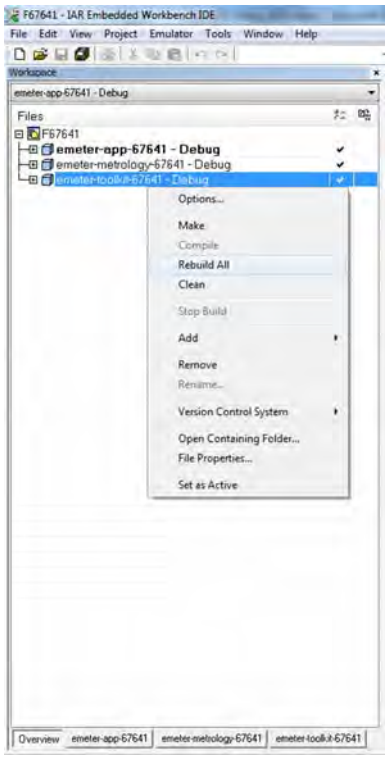

Figure 22. Toolkit Project Compilation

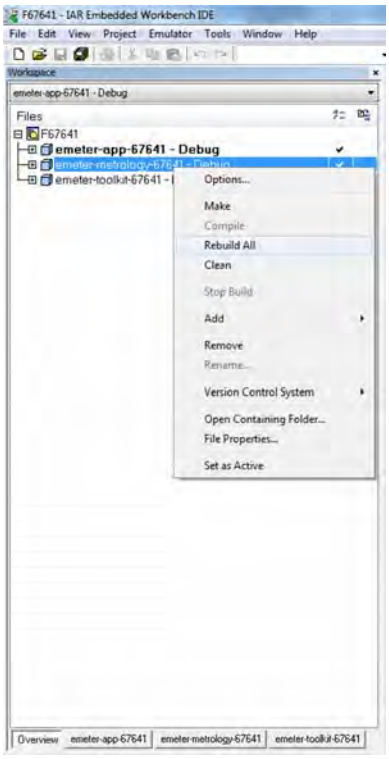

Figure 23. Metrology Project Compilation

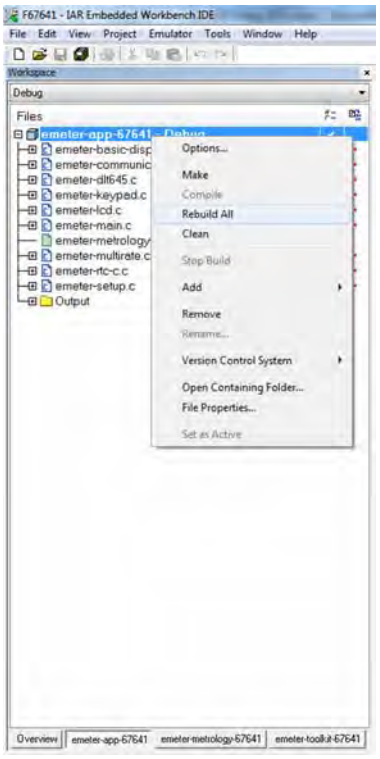

Figure 24. Application Project Compilation

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6 Test Setup

For performing metrology testing, a source generator was used to provide the voltages and currents to the system at the proper locations mentioned in Section 4.1. In the tests, the voltage and current sources were disconnected from each other. Additionally, a nominal voltage of 230 V, calibration current of 10 A, and nominal frequency of 50 Hz were used for each phase.

When the voltages and currents are applied to the system , the system outputs the cumulative active energy pulses and cumulative reactive energy pulses at a rate of 6400 pulses/kWh. This pulse output is fed into a reference meter (in the test equipment for this design, this pulse output is integrated in the same equipment used for the source generator) that determines the active energy % error based on the actual energy provided to the system and the measured energy as determined by the system's active and reactive energy output pulse. In this design, cumulative active energy error testing, cumulative reactive energy error testing, voltage variation testing, and frequency variation testing were performed.

For cumulative active energy error and cumulative reactive energy error testing, current was varied from 100 mA to 90 A simultaneously at each phase. For cumulative active energy error testing, a phase shift of 0°, 60°, and −60° is applied between the voltage and current channels. Based on the error from the active energy output pulse, a plot of active energy % error versus current is created for 0°, 60°, and –60° phase shifts, as Section 8 shows. For cumulative reactive energy error testing, a similar process is followed except that 30°, 60°, –30°, and –60° phase shifts are used and cumulative reactive energy error is plotted instead of cumulative active energy error. Also, cumulative active energy error testing is performed with a 200-µΩ shunt in addition to the 400-µΩ shunts that were used for the rest of the metrology tests.

In performing metrology tests, two sets of voltage tests were also performed. In the first test, the 230-V nominal voltage was varied by ±10% at different currents and power factors. The resulting active energy error at each test point was then logged. For the second test, the active energy error was plotted when voltage was varied over a larger voltage range at unity power factor. Specifically, voltage was varied from 57.5 V to 270 V. Testing beyond 270 V can also be done; however, this requires the 275-V varistors to be removed from the design and replaced with varistors that are rated for a higher voltage.

Another set of tests that were performed were frequency variation tests. For this test, the frequency is varied by ±2 Hertz from its 50-Hz nominal frequency. This test was conducted at 1.5 Amp and 15 Amps at phase shifts of 0°, 60°, and −60°. The resulting active energy error was logged.

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7 Viewing Metrology Readings and Calibration

7.1 Viewing Results from LCD

The LCD display scrolls between metering parameters every two seconds. For each metering parameter that is displayed on the LCD, three items are usually displayed on the screen: a symbol used to denote the phase of the parameter, text to denote which parameter is being displayed, and the actual value of the parameter. The phase symbol is displayed at the top of the LCD and denoted by a triangle shape. The orientation of the symbol determines the corresponding phase. Figure 25, Figure 26, and Figure 27 show the mapping between the different orientations of the triangle and the phase descriptor:

Figure 25. Symbol for Phase A

Figure 26. Symbol for Phase B

Figure 27. Symbol for Phase C

Aggregate results (such as cumulative active and reactive power) and parameters that are independent of phase (such as time and date) are denoted by clearing all of the phase symbols on the LCD.

The bottom line of the LCD is used to denote the value of the parameter being displayed. The text to denote the parameter being shown displays on the top line of the LCD. Table 2 shows the different metering parameters that are displayed on the LCD and the associated units in which they are displayed. The designation column shows which characters correspond to which metering parameter.

Table 2. Displayed Parameters

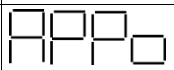
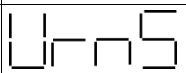
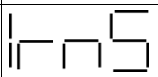
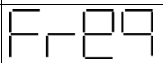
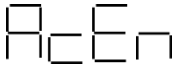
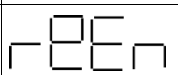
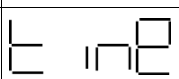
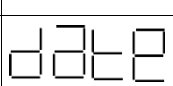
PARAMETER NAME	DESIGNATION	UNITS	COMMENTS
Active power		Watt (W)	This parameter is displayed for each phase. The aggregate active power is also displayed.
Reactive power		Volt-Ampere Reactive (var)	This parameter is displayed for each phase. The aggregate reactive power is also displayed.
Apparent power		Volt-Ampere (VA)	This parameter is displayed for each phase.
Power factor		Constant between 0 and 1	This parameter is displayed for each phase.
Voltage		Volts (V)	This parameter is displayed for each phase.
Current		Amps (A)	This parameter is displayed for each phase.
Frequency		Hertz (Hz)	This parameter is displayed for each phase.
Total consumed active energy		kWh	This parameter is displayed for each phase.
Total consumed reactive energy		kVarh	This parameter is displayed for each phase. This displays the sum of the reactive energy in quadrant 1 and quadrant 4.
Time		Hour:minute:second	This parameter is only displayed when the sequence of aggregate readings are displayed. This parameter is not displayed once per phase.
Date		Year:month:day	This parameter is only displayed when the aggregate readings are displayed. This parameter is not displayed once per phase.

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Figure 28 shows an example of phase Bs measured frequency of 49.99 Hz displayed on the LCD.

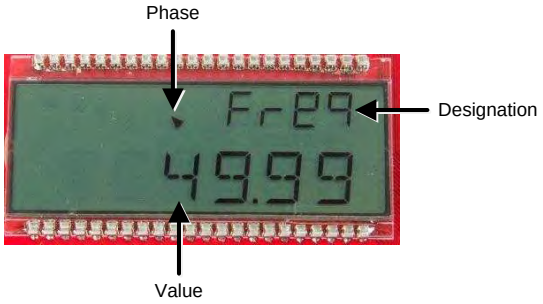

Figure 28. LCD Display

7.2 Calibrating and Viewing Results from PC

7.2.1 Viewing Results

To view the metrology parameter values from the GUI, perform the following steps:

1. Connect the EVM to a PC using an RS-232 cable.
2. Open the GUI folder and open *calibration-config.xml* in a text editor.
3. Change the *port name* field within the *meter* tag to the COM port connected to the system. As Figure 29 shows, this field is changed to *COM7*.

```
260      </correction>
261    </phase>
262    <temperature/>
263    <rtc/>
264  </cal-defaults>
265  <meter position="1">
266    <port name="com7" speed="9600"/>
267  </meter>
268  <reference-meter>
269    <port name="USB0::0x0A69::0x0835::A66200101281::INSTR"/>
270    <type id="chroma-66202"/>
271    <log requests="on" responses="on"/>
272    <scaling voltage="1.0" current="1.0"/>
273  </reference-meter>
```

Figure 29. GUI Configuration File Changed to Communicate With Energy Measurement System

4. Run the *calibrator.exe* file, which is located in the GUI folder. If the COM port in the *calibration-config.xml* was changed in the previous step to the COM port connected to the EVM, the GUI opens (see Figure 30). If the GUI connects properly to the EVM, the top-left button is green. If there are problems with connections or if the code is not configured correctly, the button is red. Click the green button to view the results.

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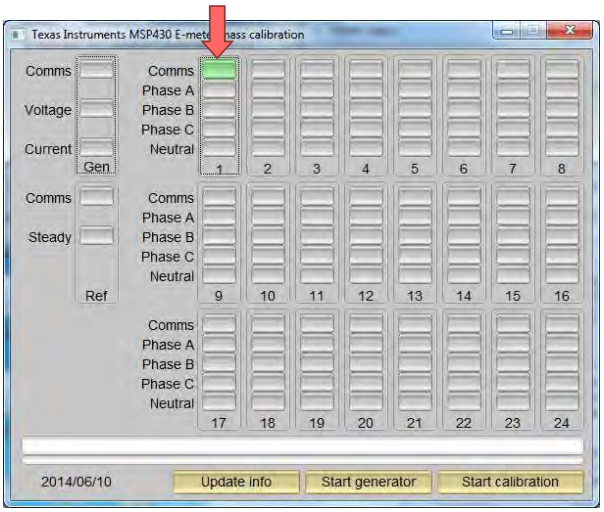

Figure 30. GUI Startup Window

Upon clicking on the green button, the results window opens (see Figure 31). In the figure, there is a trailing "L" or "C" on the *Power factor* values to indicate an inductive or capacitive load, respectively.

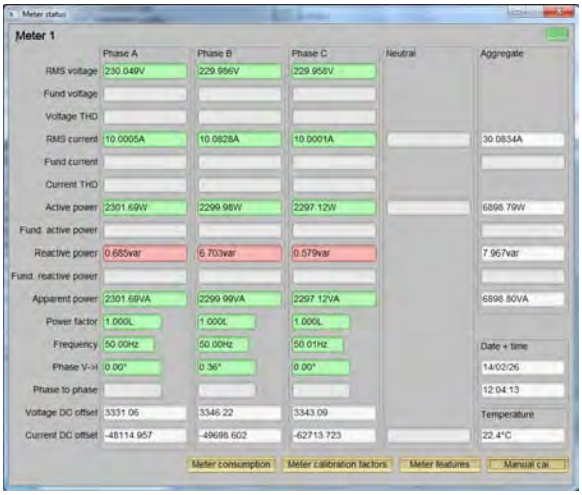

Figure 31. GUI Results Window

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From the results window, the total-energy consumption readings and sag/swell logs can be viewed by clicking the *Meter Consumption* button. After the user clicks this button, the *Meter events and consumption* window pops up, as Figure 32 shows.

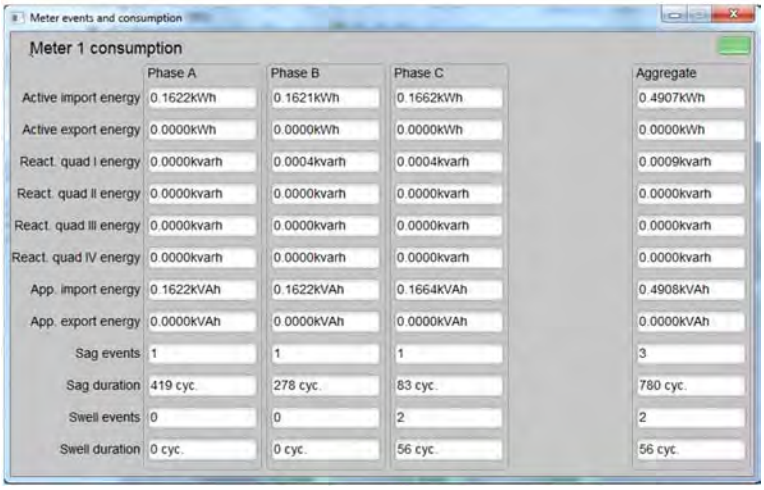

Figure 32. Meter Events and Consumption Window

From this *Meter events and consumption* window, the user can view the meter settings by clicking the *Meter features* button, view the system calibration factors by clicking the *Meter calibration factors* button, or open the window used for calibrating the system by clicking the *Manual cal.* button.

7.2.2 Calibration

Calibration is key to any meter performance and it is absolutely necessary for every meter to go through this process. Initially, every meter exhibits different accuracies due to silicon-to-silicon differences, sensor accuracies, and other passive tolerances. To nullify their effects, every meter must be calibrated. To perform calibration accurately there should be an accurate AC test source and a reference meter available. The source must be able to generate any desired voltage, current, and phase shifts (between V and I). To calculate errors in measurement, the reference meter acts as an interface between the source and the meter being calibrated. This section discusses a simple and effective method of calibration of this three-phase EVM.

The GUI used for viewing results can easily be used to calibrate the EVM. During calibration, parameters called calibration factors are modified in software to give the least error in measurement. For this meter, there are six main calibration factors for each phase: voltage scaling factor, voltage AC offset, current scaling factor, current AC offset, power scaling factor, and the phase compensation factor. The voltage, current, and power scaling factors translate measured quantities in metrology software to real-world values represented in volts, amps, and watts, respectively. The voltage AC offset and current AC offset are used to eliminate the effect of additive white Gaussian noise (AWGN) associated with each channel. This noise is orthogonal to everything except itself; as a result, this noise is only present when calculating RMS voltages and currents. The last calibration factor is the phase compensation factor, which is used to compensate any phase shifts introduced by the current sensors and other passives. Please note that the voltage, current, and power calibration factors are independent of each other. Therefore, calibrating voltage does not affect the readings for RMS current or power.

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When the meter SW is flashed with the code (available in the **.zip* file), default calibration factors are loaded into these calibration factors. These values are to be modified through the GUI during calibration. The calibration factors are stored in INFO_MEM, and therefore, remain the same if the meter is restarted. However, if the code is re-flashed during debugging, the calibration factors are replaced and the meter has to be recalibrated. One way to save the calibration values is by clicking on the *Meter calibration factors* button (see Figure 31). The *Meter calibration factors* window (see Figure 33) displays the latest values, which can be used to restore calibration values.

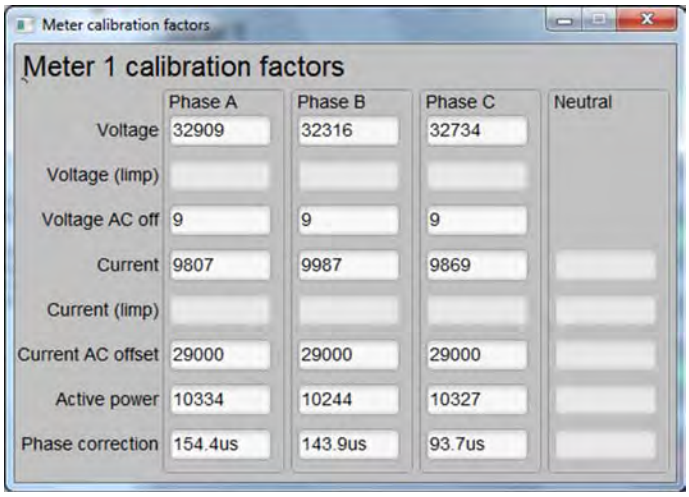

Figure 33. Calibration Factors Window

Calibrating any of the scaling factors is referred to as gain correction. Calibrating the phase compensation factors is referred to as phase correction. For the entire calibration process, the AC test source must be ON, meter connections consistent with Section 4.1, and the energy pulses connected to the reference meter.

7.2.2.1 Gain Calibration

Usually gain correction for voltage and current can be done simultaneously for all phases. However, energy accuracy (%) from the reference meter for each individual phase is required for gain correction for active power. Also, when performing active power calibration for any given phase, the other two phases must be turned OFF. Typically, switching only the currents OFF is good enough for disabling a phase.

7.2.2.1.1 Voltage and Current Gain Calibration

To calibrate the voltage and current readings, perform the following steps:

1. Connect the GUI to view results for voltage, current, active power, and the other metering parameters.
2. Configure the test source to supply desired voltage and current for all phases. Ensure that these are the voltage and current calibration points with a zero-degree phase shift between each phase voltage and current. For example, for 230 V, 10 A, 0º (PF = 1). Typically, these values are the same for every phase.
3. Click on the *Manual cal.* button that Figure 31 shows. The following screen pops up from Figure 34:

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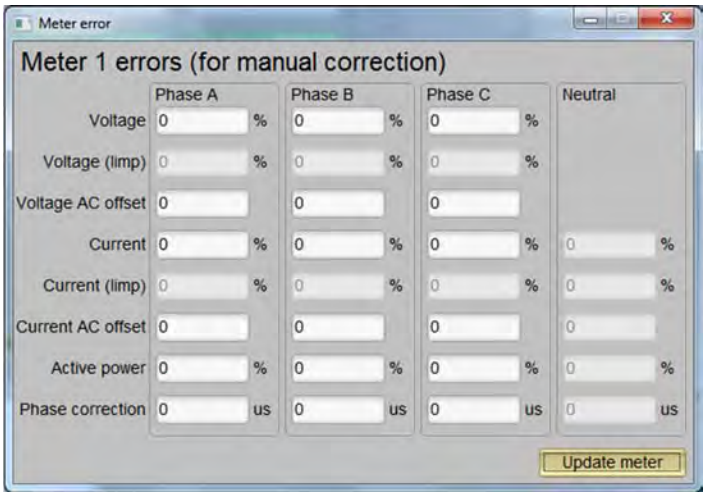

Figure 34. Manual Calibration Window

4. Calculate the correction values for each voltage and current. The correction values that must be entered for the voltage and current fields are calculated by:

$$\text{Correction (\%)} = \left(\frac{\text{value}_{\text{observed}}}{\text{value}_{\text{desired}}} - 1 \right) \times 100 \quad (17)$$

where

- $\text{value}_{\text{observed}}$ is the value measured by the TI meter
- $\text{value}_{\text{desired}}$ is the calibration point configured in the AC test source.

5. After calculating for all voltages and currents, input these values as is (±) for the fields *Voltage and Current* for the corresponding phases.
6. Click on the *Update meter* button and the observed values for the voltages and currents on the GUI settle immediately to the desired voltages and currents.

7.2.2.1.2 Active Power Gain Calibration

Note that this example is for one phase. Repeat these steps for other phases.

After performing gain correction for voltage and current, gain correction for active power must be done. Gain correction for active power is done differently in comparison to voltage and current. Although, conceptually, calculating using Step 4 with active power readings (displayed on the AC test source) can be done, this method is not the most accurate and should be avoided.

The best option to get the *Correction (%)* is directly from the reference meters measurement error of the active power. This error is obtained by feeding energy pulses to the reference meter. To perform active power calibration, perform the following steps.

1. Turn off the system and connect the energy pulse output of the system to the reference meter. Configure the reference meter to measure the active power error based on these pulse inputs.
2. Turn on the AC test source
3. Repeat Steps 1 to Steps 3 from the previous Section 7.2.2.1.1 with the identical voltages, currents, and 0º phase shift that were used in the same section.
4. Obtain the % error in measurement from the reference meter. Note that this value may be negative.
5. Enter the error obtained in the previous Step 4 into the *Active Power* field under the corresponding phase in the GUI window. This error is already the value and does not require calculation.
6. Click the *Update meter* button and the error values on the reference meter immediately settle to a value close to zero.

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7.2.2.2 Phase Correction

After performing power gain correction, phase calibration must be performed. Similar to active power gain calibration, to perform phase correction on one phase, the other phases must be disabled. To perform phase correction calibration, perform the following steps:

1. If the AC test source has been turned OFF or reconfigured, perform Steps 1–3 from Section 7.2.2.1.1 using the identical voltages and currents used in that section.
2. Disable all other phases that are not currently being calibrated by setting the current of these phases to 0 A.
3. Modify only the phase-shift to a non-zero value; typically, +60º is chosen. The reference meter now displays a different % error for active power measurement. Note that this value may be negative.
4. If this error from the previous Step 3 is not close to zero, or is unacceptable, perform phase correction by following these steps:
   (a) Enter a value as an update for the *Phase Correction* field for the phase that is being calibrated. Usually, a small ± integer must be entered to bring the error closer to zero. Additionally, for a phase shift greater than 0 (for example: +60º), a positive (negative) error would require a positive (negative) number as correction.
   (b) Click on the *Update meter* button and monitor the error values on the reference meter.
   (c) If this measurement error (%) is not accurate enough, fine-tune by incrementing or decrementing by a value of 1 based on the previous Step 4a and Step 4b. Please note that after a certain point, the fine-tuning only results in the error oscillating on either side of zero. The value that has the smallest absolute error must be selected.
   (d) Change the phase now to −60° and check if this error is still acceptable. Ideally, errors should be symmetric for same phase shift on lag and lead conditions.

After performing phase correction, calibration is complete for one phase. Please note that the gain calibration and phase calibration are completed in sequence for each phase before moving on to other phases. These two procedures must be repeated for each phase, unlike voltage and current calibration.

This completes calibration of voltage, current, and power for all three phases. View the new calibration factors (see Figure 35) by clicking the *Meter calibration factors* button of the GUI metering results window in Figure 31.

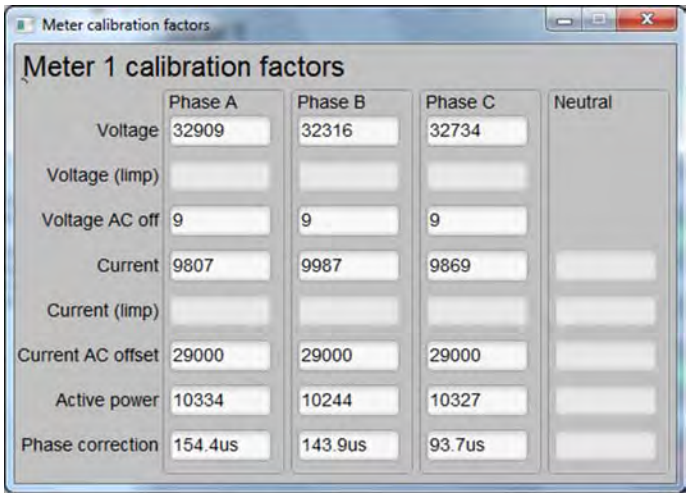

Figure 35. Calibration Factors Window

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Also view the configuration of the system by clicking on the *Meter features* button in Figure 31 to get to the window that Figure 36 shows.

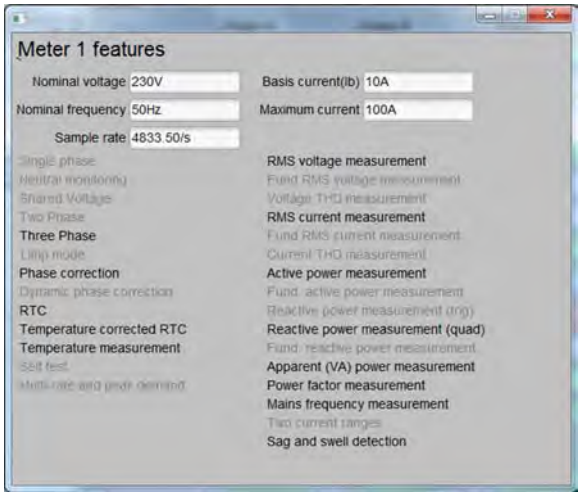

Figure 36. Meter Features Window

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8 Test Data

Table 3. Cumulative Active Energy % Error Versus Current, 400-µΩ Shunts

CURRENT	0°	60°	–60°
0.1	–0.093	–0.059	–0.119
0.25	–0.0343	–0.0475	–0.033
0.5	–0.0255	–0.0287	–0.0345
1	–0.0175	–0.023	–0.032
2	–0.031	–0.0175	–0.034
5	–0.009	–0.03	–0.014
10	–0.0117	–0.009	–0.0073
20	0.001	0	–0.015
30	0.0093	0.021	0.002
40	0.0253	0.043	0.029
50	0.044	0.035	0.0427
60	0.0555	0.054	0.0625
70	0.0755	0.072	0.0795
80	0.094	0.102	0.102
90	0.131	0.132	0.148

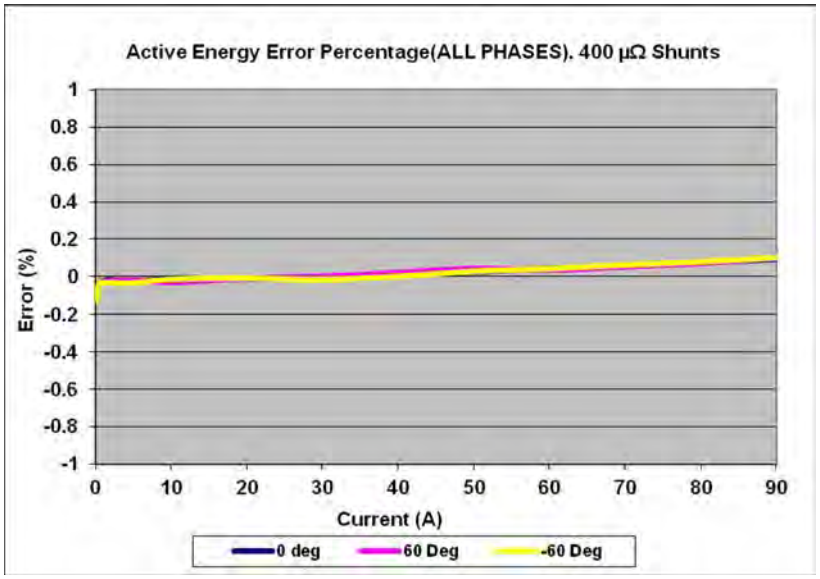

Figure 37. Cumulative Active Energy % Error Versus Current, 200-µΩ Shunts

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Table 4. Cumulative Active Energy % Error Versus Current, 200-µΩ Shunts

CURRENT	0°	60°	–60°
0.1	–0.35	–0.405	–0.3855
0.25	–0.075	–0.055	–0.0765
0.5	–0.031	–0.032	–0.042
1	–0.0147	–0.018	–0.009
2	–0.0187	0.012	–0.022
5	–0.008	–0.0145	0.001
10	–0.0017	–0.003	0.0033
20	0.0007	0.013	–0.0125
30	0.0107	0.021	0
40	0.0097	0.023	0.006
50	–0.006	0.01	0.008
60	0.0043	0.0117	–0.004
70	–0.0015	–0.001	–0.015
80	–0.0173	–0.026	–0.03
90	–0.0345	–0.035	–0.054

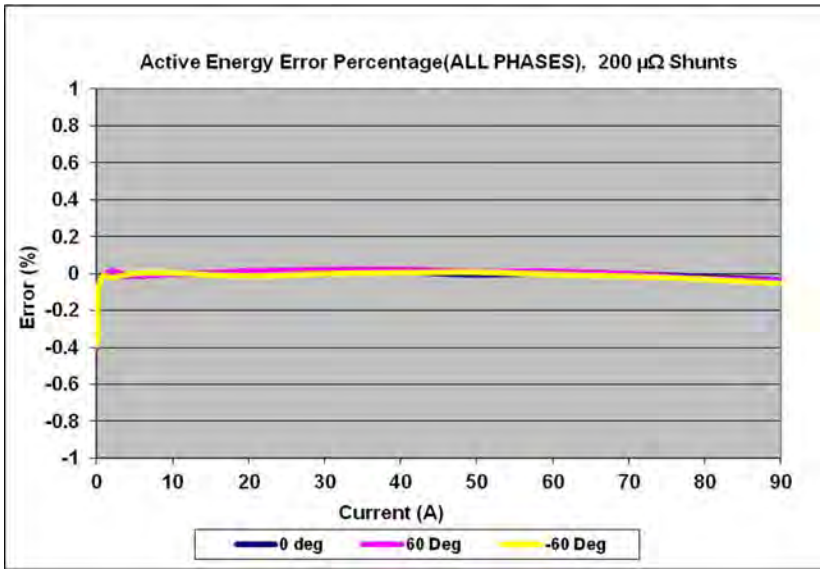

Figure 38. Cumulative Active Energy % Error Versus Current, 200-µΩ Shunts

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Table 5. Cumulative Reactive Energy % Error Versus Current

CURRENT	30°	60°	–30°	–60°
0.1	0.014	–0.066	–0.15	–0.09
0.25	–0.009	–0.018	–0.067	–0.045
0.5	0.0173	–0.057	–0.08	–0.047
1	0.026	–0.013	–0.0757	–0.0375
2	0	–0.005	–0.068	–0.0335
5	0.027	0.006	–0.0603	–0.042
10	0.046	0.009	–0.066	–0.013
20	0.038	0.005	–0.045	–0.0205
30	0.047	0.026	–0.0157	0.029
40	0.072	0.0367	–0.014	0.011
50	0.09	0.05	–0.021	0.011
60	0.1055	0.0663	0.005	0.035
70	0.139	0.0927	0.032	0.0547
80	0.176	0.129	0.053	0.083
90	0.2	0.17	0.1023	0.135

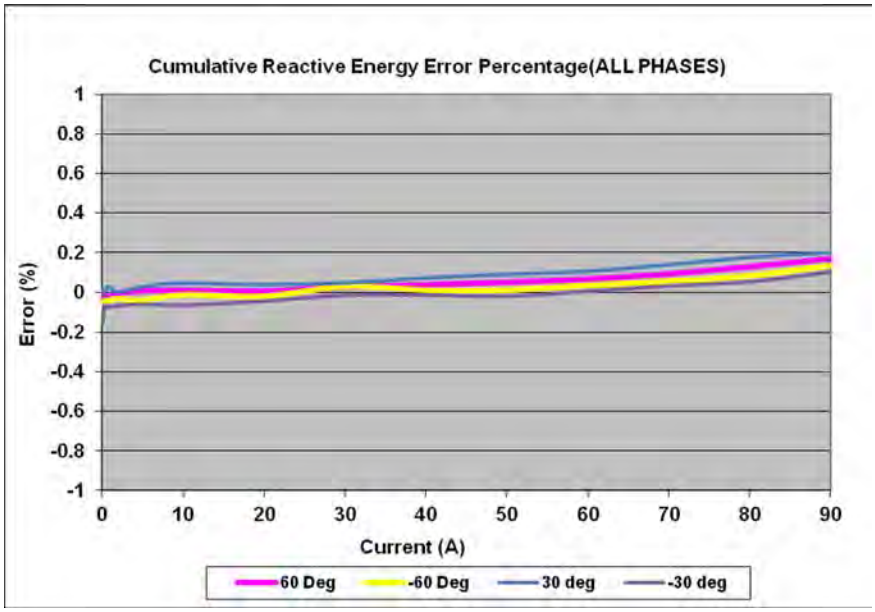

Figure 39. Cumulative Reactive Energy % Error Versus Current

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Table 6. Cumulative Active Energy Measurement Error Versus Voltage, 57.5 V to 270 V

VOLTAGE	%ERROR
57.5	–0.1285
100	–0.052
110	–0.013
120	0.012
150	0.0185
180	0.025
210	0.005
220	–0.003
230	0.009
240	–0.0067
250	–0.0147
260	–0.012
265	0.0057
270	0.003

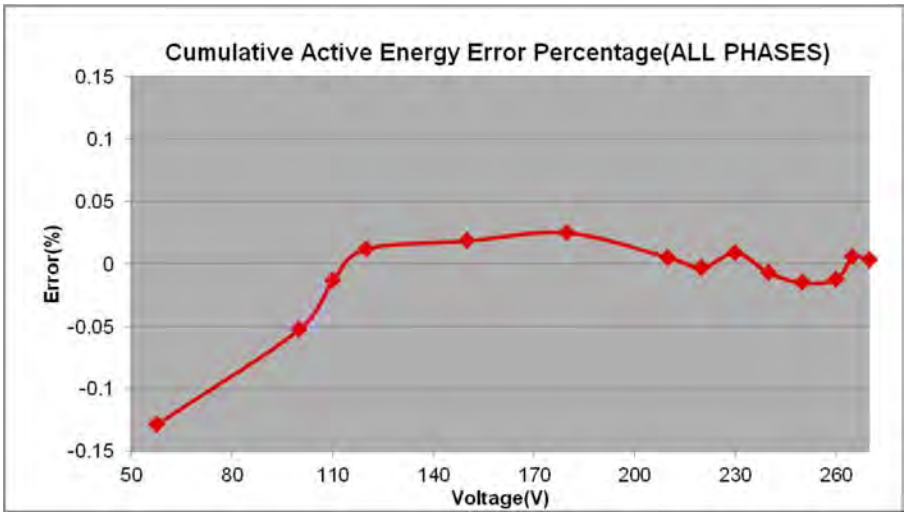

Figure 40. Cumulative Active Energy Measurement Error Versus Voltage, 57.5 V to 270 V

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Table 7. Cumulative Active Energy Measurement Error Versus Voltage, ±10% Nominal Voltage

VOLTAGE	0°, 15 A	60°, 15 A	300°, 15 A	0°, 1.5 A	60°, 1.5 A	300°, 1.5 A
207	0.0225	0.027	0.007	–0.009	–0.007	–0.021
230	0.002	0.016	–0.005	–0.02	0.004	–0.0235
253	–0.0137	0.018	–0.018	–0.0293	–0.011	–0.04

Table 8. Cumulative Active Energy Measurement Error Versus Frequency, ±2 Hz From Nominal Frequency

CONDITIONS	48 Hz	50 Hz	52 Hz
1.5 A, 0	–0.0163	–0.0193	–0.0203
1.5 A, 60	–0.008	0	–0.008
1.5 A, 300	–0.025	–0.037	–0.0333
15 A, 0	0.0013	0.008	–0.016
15 A, 60	0.012	0.009	0.0245
15 A, 300	–0.005	–0.008	–0.014

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9 Design Files

9.1 Schematics

To download the schematic, see the design files at TIDA-00601.

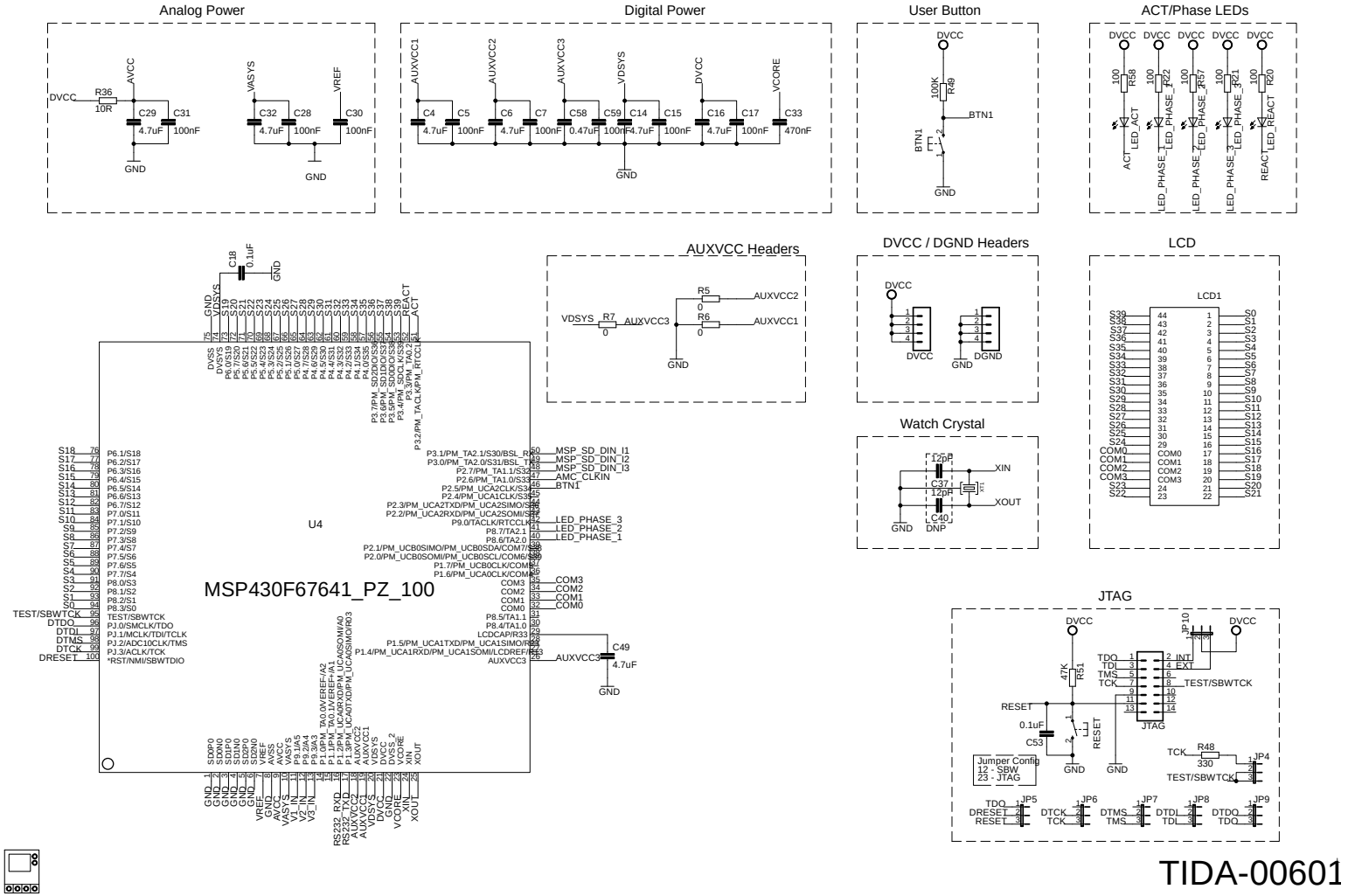

Figure 41. TIDA-00601 Schematic Page 1

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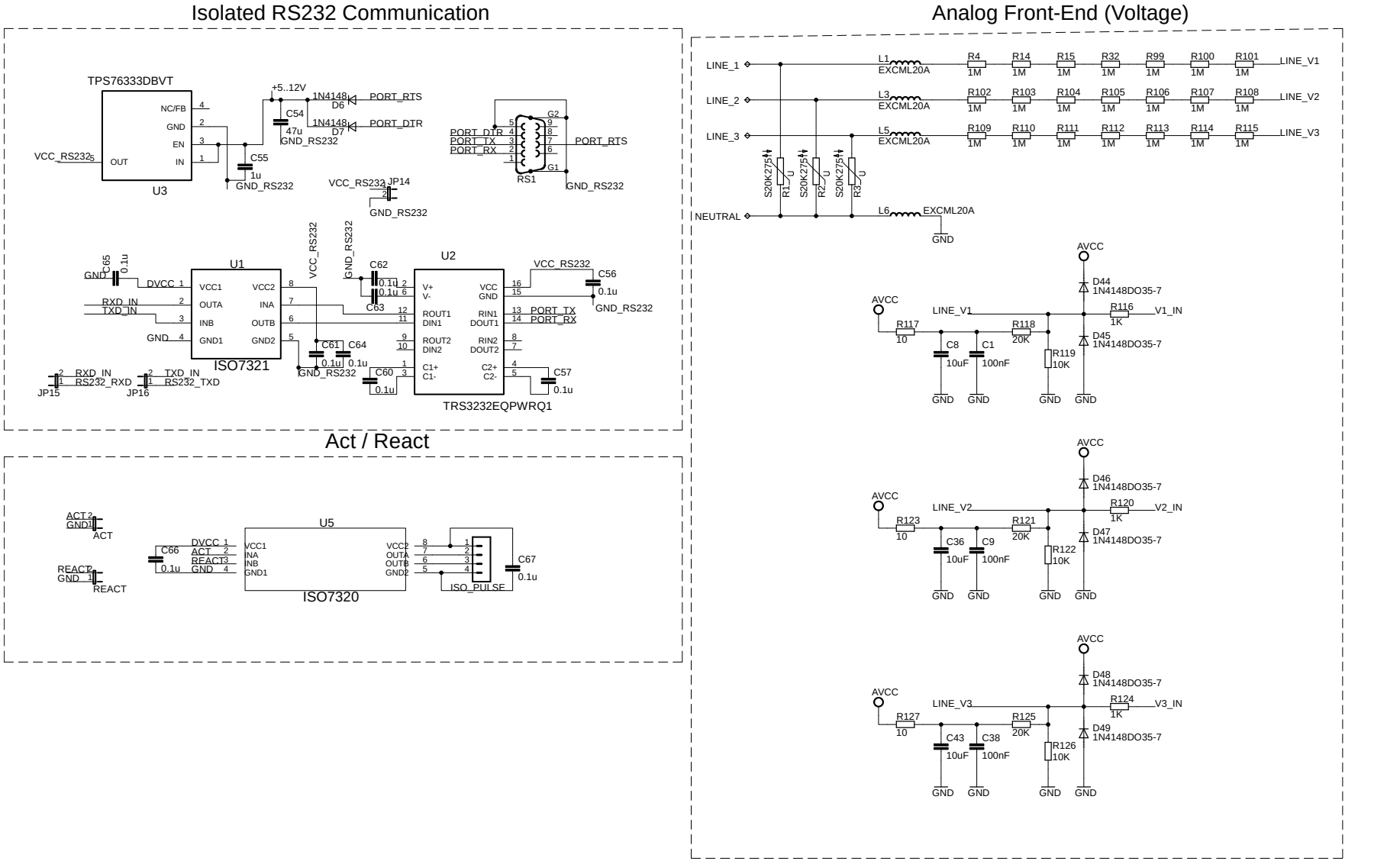

Figure 42. TIDA-00601 Schematic Page 2

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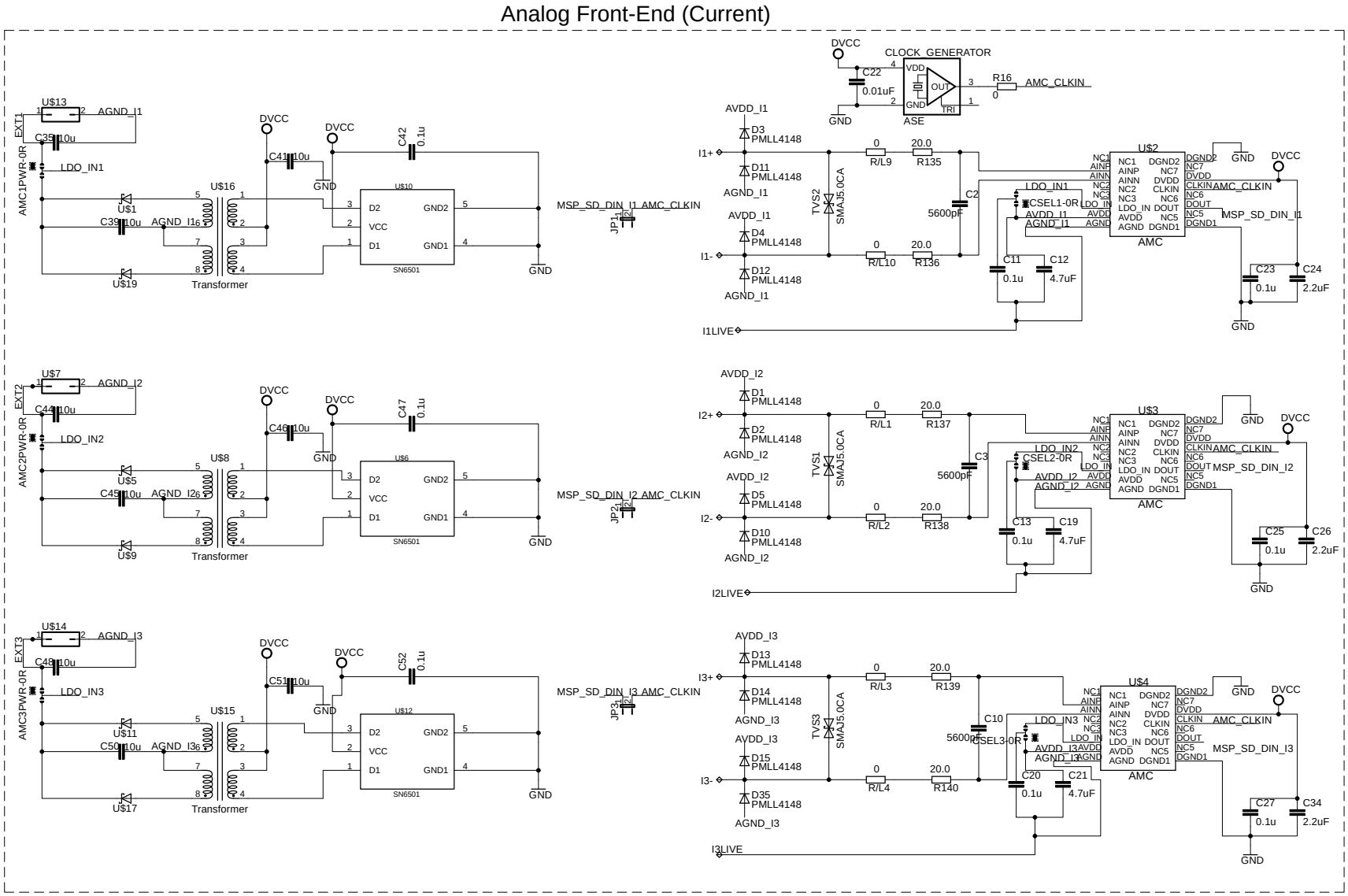

TIDA-00601

Figure 43. TIDA-00601 Schematic Page 3

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9.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00601.

9.3 PCB Layout Recommendations

For this design, the following general guidelines must be followed:

- Place decoupling capacitors close to their associated pins.
- Use ground planes instead of ground traces and minimize the cuts in the ground plane, especially for the ground planes of the high side of each AMC1304. In this design, there is a ground plane on both the top and bottom layer; for this situation, ensure that there is good stitching between the planes through the liberal use of vias.
- Each AMC1304 should have its own set of ground planes that are used for the high side of each AMC1304. Each of these ground planes is actually referenced from a different line voltage because each AMC1304 must be connected to a different line voltage.
- A different ground plane is used for the isolated RS-232. This other ground plane is at the potential of the RS-232 ground and not DGND.
- Be careful to avoid crosstalk from the delta-sigma modulation clock traces or the AMC1304 bit-stream traces.
- Minimize the length of the traces used to connect the crystal to the microcontroller. Place guard rings around the leads of the crystal and ground the crystal housing. In addition, there must be clean ground underneath the crystal and placing any traces underneath the crystal must be avoided. Also, keep high frequency signals away from the crystal.
- Use wide traces for power supply connections.
- Maintain at least an 8.1-mm spacing between the ground planes of the high side of each AMC1304 device and the ground plane on the controller side. This spacing maintains the recommended clearance for the AMC1304 isolation rating. In addition, ensure that the recommended clearance and creepage spacing for other isolation devices (such as the ISO7320 and ISO7321) is also followed.
- Keep the traces of the analog input pin symmetrical and as close as possible to each other.

9.4 Layer Plots

To download the layer plots, see the design files at TIDA-00601.

9.5 CAD Project

To download the CAD project files, see the design files at TIDA-00601.

9.6 Gerber Files

To download the Gerber files for each board, see the design files at TIDA-00601.

10 Software Files

To download the software files for this reference design, please see the software at TIDA-00601.

11 References

1. Texas Instruments, *Isolated, Shunt-Based Current Sensing Reference Design*, User's Guide, (TIDU384)
2. Texas Instruments, *Self-Powered Isolated RS-232 to UART Interface*, User's Guide, (TIDU298)
3. Texas Instruments, *Implementation of a Low-Cost Three-Phase Electronic Watt-Hour Meter Using the MSP430F67641*, Application Report, (SLAA621)

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12 About the Author

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Revision History A

Changes from Original (May 2015) to A Revision	Page
• Changed ISO7421 to ISO7321 and changed ISO7420 to ISO7320	1
• Changed block diagram image	1
• Changed ISO7421 to ISO7321 and added third paragraph to Section 1.5	5
• Changed value of 2.5 kV to 3 kV in Section 1.5	5
• Changed ISO7420 to ISO7320 and added second paragraph to Section 1.7	5
• Changed all instances of ISO7420 to ISO7320 and all instances of ISO7421 to ISO7321	6
• Changed 2.5 kV to 3 kV and changed 1 Mbps to 25 Mbps in Section 2.1.5	8
• Changed 2.5 kV to 3 kV and changed 1 Mbps to 25 Mbps in Section 2.1.7	8

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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