参考資料

デザイン・ガイド：TIDA-00834
測定範囲 ±10V の 14/16/18 ビット SAR ADC を使用した高精度アナログ・フロント・エンドのリファレンス・デザイン

概要

このリファレンス・デザインは、同時サンプル、14/16/18 ビット、±10V のバイポーラ入力 SAR アナログ/デジタル・コンバータ (ADC) を使用して、電圧および電流入力を正確に測定します。アナログ・フロント・エンド (AFE) には、計測アンプまたは高精度オペアンプを使った信号コンディショニングが含まれており、最大 125A の電流を測定できます。また、絶縁アンプまたはオペアンプを使った AFE により、最大 300V の電圧を測定できます。ゲイン・アンプはセンサの出力を ADC の範囲にスケーリングします。コンパレータと FPGA (field-programmable gate array) により、アナログ入力信号のコヒーレントなサンプリングを実装します。AFE に必要な電源は、+5V を使用して生成されます。

リソース

TIDA-00834	デザイン・フォルダ
ADS8588S、ADS8598H、ADS8588H、ADS8598S	プロダクト・フォルダ
ADS8586S、ADS8584S、ADS8578S、INA188	プロダクト・フォルダ
INA821、ISO224A、ISO224B、ISO7741	プロダクト・フォルダ
OPA2188、OPA2180、LM2903	プロダクト・フォルダ
OPA2277、AMC1200、TPS7A39	プロダクト・フォルダ
AMC1301、AMC1300、AMC1300B	プロダクト・フォルダ
LM5017、LM5160、TPS65131、ISOW7841	プロダクト・フォルダ
SN6505B、SN6501、TPS7A30、TVS1400	プロダクト・フォルダ
REF5025、TLV1117、LM27762、TVS1401	プロダクト・フォルダ

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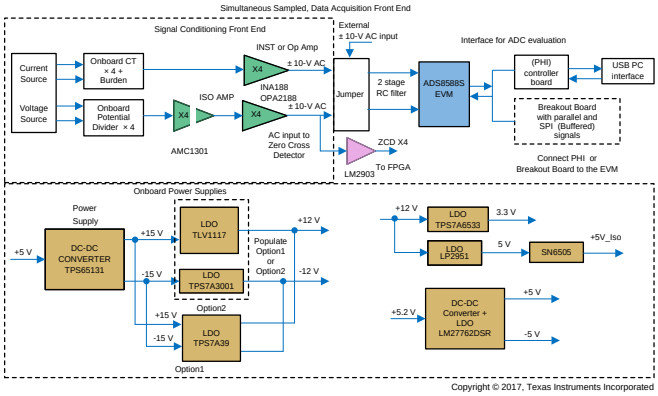
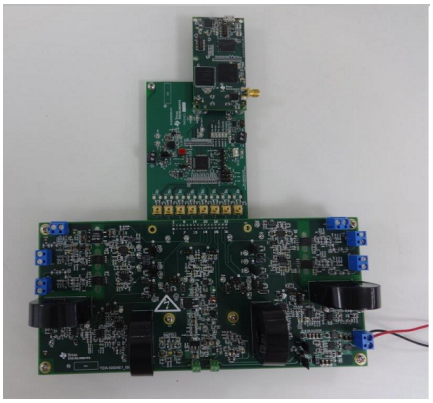
特長

- 4、6、8 チャネル ADC を使用したデータ収集 AFE
  - 測定精度は 18 ビットで ±0.1%、16 ビットで ±0.3%、14 ビットで ±1% 以内、ダイナミック・レンジ 1000:1 以上
- 16 ビット ADC のオーバーサンプリングにより、SNR が 91.72 から 93.95dB に向上
- 高精度アンプまたは計測アンプを使用して最大 125A の電流を測定し、保護および測定アプリケーションに対応
- ±250mV または ±12V 入力の強化絶縁アンプと、固定ゲイン・アンプにより、300V までの電圧を測定
- EFT および AC または DC 入力過負荷を含む信頼性テストで、観測される性能の変動は最小限
- オンボードの DC-DC コンバータと、デュアル 150mA LDO を含む LDO により、5V 単一入力から ±12V、±15V、5V、3.3V、絶縁 5V を生成

アプリケーション

- 保護リレー、マージング・ユニット
- 電力アナライザ、3 相インバータ





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1 System Description

Protection relays used in grid infrastructure applications protect personnel and equipment. These protection relays detect and locate faults by measuring electrical quantities in the power system which vary during normal and faulty conditions. They are installed in generation, transmission, and distribution and at consumer locations for protecting primary equipment like transformers, breakers, and customer loads (motors, busbar). Protection relays are tasked to minimize the damage and expense caused by insulation breakdowns. These faults occur as a result of insulation deterioration or result from unforeseen events such as lightning strikes or power trips caused by contact with trees and foliage. Protection relays constantly monitor the line during normal operation and must immediately activate to handle intolerable system conditions. A relay system must be capable of responding to an infinite number of abnormalities that may occur within the network. These relays are intelligent electronic devices (IEDs) that measure signals from the secondary side of current transformers (CTs) and voltage transformers (VTs). The relays detect whether or not a protected unit is in a stressed condition. A trip signal is sent by protective relays to the circuit breakers to disconnect the faulty components from the power system, if necessary. Protective relays are categorized based on the type of equipment protected such as generators, transmission lines, transformers, and loads.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS	COMMENTS
ADC for measurement of analog inputs (type, resolution)	Simultaneous sampling 18-bit, 16-bit, or 14-bit SAR ADC	Measurement accuracy ±0.1% for 18-bit, ±0.3% for 16-bit, and ±1% for 14-bit
Number of analog inputs	4, 6, or 8 (based on the ADC interfaced)	Interfaced to ADS8588SEVM-PDK
Voltage input range	5 V to 300 V with resistor divider and fixed-gain precision amplifier	Measurement accuracy ±0.3% of 16-bit
Isolated voltage input range	5 V to 300 V with resistor divider, fixed-gain precision amplifier, and isolation amplifier with reinforced isolation	AMC1301 isolation amplifier used
Current input range	0.1 A to 120 A with current transformer and fixed-gain instrumentation amplifier	Measurement accuracy tested with instrumentation amplifier INA188
Current input range	0.1 A to 120 A with current transformer and fixed-gain precision amplifier	Measurement accuracy tested using OPA2188, OPA2180, or OPA2171 op amp
Reference	Internal VREF 2.5-V DC, V(REFCAP) 4-V DC	—
ADC interface	Serial or parallel	—
Power supply for ADC	DVDD digital: +3.3 V; AVDD analog: +5 V	Analog input voltage: VAVDD to VAVSS; using +5 V
Power supply for signal-conditioning amplifier	±13 V (using dual-output LDO or individual LDOs)	Generated using single +5-V DC input
Isolated power	Analog: +5 V	—
Interface to MCU for processing	AM3352 and XC6SLX16 using precision host interface (PHI) controller board	See 3.1 for connection details
Coherent sampling	Using LM2903 comparator and FPGA for digital PLL implementation	
Current and voltage inputs	Onboard CT and resistor divider	—

2 System Overview

2.1 Introduction to Subsystems Using ADC for Grid Applications

The subsystems that use analog-to-digital conversion (ADC) in grid infrastructure applications include the following:

- **AC measurement inputs:**
  - Nominal frequency (FNOM): 50 Hz or 60 Hz and operating range: 45 Hz to 66 Hz
- **CT measurement inputs:**
  - Nominal current: 1 A or 5 A (I_N)
- **VT measurement inputs:**
  - VT measurement inputs
- **DC analog input range (independently configurable):**
  - ±1.25 mA, ±2.5 mA, ±5 mA, and ±10 V;
  - or ±1 mA, ±5 mA, ±10 mA, and ±20 mA

2.2 Voltage and Current Measurement Front End

Power-monitoring systems rely on the measurement of instantaneous current and voltage using CTs and the output of voltage transformers (termed PT, for potential transformers) converted by high-speed ADCs. A processor uses these measurements to calculate the key characteristics including instantaneous values and harmonics.

The data acquisition (DAQ) front end consists of:

- Voltage input measurement with the following options:
  - Potential divider (PD) and signal-conditioning circuit based on precision op amp to scale the sensor output to the ADC input range
  - Isolated voltage measurement using PD, *isolation amplifier*, and differential amplifier based on precision op amp to scale the isolation amplifier output to the ADC input range
- Comparator for zero-cross detection of voltage inputs for implementation of *coherent sampling*
- Onboard high-accuracy CT with burden to connect AC input directly to the DAQ front end
- Current input signal-conditioning circuit based on instrumentation amplifier or precision op amp to scale the CT output to the ADC input range
- Interface connector to connect the DAQ front end to a 16-bit, 18-bit, or 14-bit *simultaneous-sampling* ADC ADS8588S, ADS8588H, ADS8598S, and ADS8578S based EVM with a precision host interface (PHI) controller board for a user interface with *oversampling* up to 64 times
- Option to capture required number of cycles to compute and display root mean square (RMS) value, histogram analysis, and DC offset subtraction to improve the measurement accuracy at a lower current and measure wider current
- Isolated power using transformer driver and low-dropout (LDO) regulator, DC-DC converter, and LDOs to generate ±13 V, 3.3 V, and 5 V from a single +5-V input.

2.3 Isolation of Voltage and Current Inputs

In applications that use a PD for voltage measurement and a shunt for current measurement, the isolation required for the system can be provided using an isolation amplifier. The isolation requirement can be a basic or reinforced type.

2.4 Coherent Sampling

ADC sampling is controlled by a phase-locked loop (PLL) circuit that is referenced to one of the voltage channels. A PLL automatically adjusts the sampling rate to the power line frequency to ensure an evenly-spaced distribution of samples per cycle for every ADC channel that is acquired. The PLL system generates the frequency, which is a multiple of the reference frequency necessary for clocking the ADC. The necessity to use the PLL system results from the requirements of the IEC 61000-4-7, which describes the methodology and admissible errors which occur when measuring harmonic components. The standard requires that the measuring window, which is the basis for a single measurement and evaluation of harmonics content, be equal to the duration of 10 periods in 50-Hz mains systems and 12 periods in 60-Hz systems corresponding to 200 ms. The window duration may not equal exactly 200 ms because the mains frequency can be subject to periodical changes and fluctuations. The standard also recommends that the data not be subject to windowing operation before the Fourier transform (to separate the spectral components). The absence of frequency synchronization and allowing the situation where the fast-Fourier transform (FFT) is performed on the samples from non-integer number of periods can lead to spectral leakage. This phenomenon causes the spectral line of harmonic blurs to some additional few, neighboring interharmonic spectral lines, which may lead to loss of data concerning the actual level and power of the tested spectral line.

2.5 ADC Architecture

ADC sampling can be implemented by simultaneous sampling or multiplexed sampling.

Simultaneous-sampling systems use an individual ADC for each channel and offer the following advantages:

- Eliminates time skew between channels and simplifies both time- and frequency-based analysis techniques
- Results in increased signal bandwidth and provides higher accuracy at high speed
- Simultaneous sampling of all inputs with a single conversion start to acquire all channels
- Eliminates several sources of error including settling time and channel-to-channel crosstalk

The ADS8588S device simultaneously samples eight channels of the ADC. The sampling is gapless, which means each voltage and current cycle is continuously sampled without gaps between cycles and samples. *For the correct measurement of phase shift between the voltage harmonics in relation to current harmonics and power of these harmonics, the important factor is not absolute phase shift in relation to the basic frequency, but the phase coincidence of voltage and current circuits. A phasor measurement unit (PMU) uses a simultaneous-sampling ADC to measure the phase shift between different phase voltages with minimum error.*

2.6 Oversampling

Oversampling is a popular method used for improving ADC resolution and increasing dynamic range. In applications that require higher accuracy, special signal-processing techniques can be used to improve the resolution of a measurement. A higher resolution can be achieved by using a method called *oversampling and decimation*. Oversampling is a cost-effective process of sampling the input signal at a much higher rate than the Nyquist frequency to increase the signal-to-noise ratio (SNR) and resolution (ENOB), which also simplifies the requirements on the antialiasing filter. As a guideline, oversampling the ADC by a factor of four provides one additional bit of resolution, or a 6-dB increase in dynamic range (DR). Increasing the oversampling ratio (OSR) results in reduced noise and the DR improvement due to

oversampling is ΔDR = 10 × log10(OSR) in dB. Oversampling a high-throughput, successive-approximation register (SAR) ADC can improve antialiasing and reduce overall noise. To get the best possible representation of an analog input signal, oversampling the signal is necessary because a larger amount of samples provide a better representation of the input signal when averaged. The ADS8588S device can be configured to perform oversampling by a factor of 64.

2.7 Block Diagram

The high-performance AC DAQ AFE shown in 図 1 implements an ADS8588S ADC EVM that is interfaced to a signal-conditioning circuit with a provision for four voltages and four current inputs. Resistor dividers have been provided to directly connect the AC voltage up to 300 V. An optional isolation amplifier has been provided for the purpose of isolating the voltage inputs for applications that require input-to-output isolation. Onboard CTs are used to measure the current inputs up to 120 A and a CT provides the required isolation for the current inputs. The CT output is scaled to the ADC input range of ±10 V using instrumentation and a precision op amp-based amplifier. Jumpers have been provided to select one of the two outputs. The voltage inputs are scaled to the ADC range using a precision op-amp-based amplifier. An isolation amplifier is used to provide the required isolation between the input and output for the voltage inputs. The voltage outputs are connected to a zero-cross detector to implement coherent sampling. The comparator output is connected to a PHI controller board and the coherent sampling is implemented digitally. ±13-V, +5-V, and +3.3-V power supplies are generated using a DC-DC converter and LDO regulators.

The TIDA-00834 design comprises two different types of boards:

1. The first board offers a potential divider ≥ 1-MΩ impedance and CTs.
2. The second board offers a potential divider ≥ 1-MΩ impedance, isolation amplifier, and CTs.

The current measurement circuit and the ADC interface is the same for both type of boards.

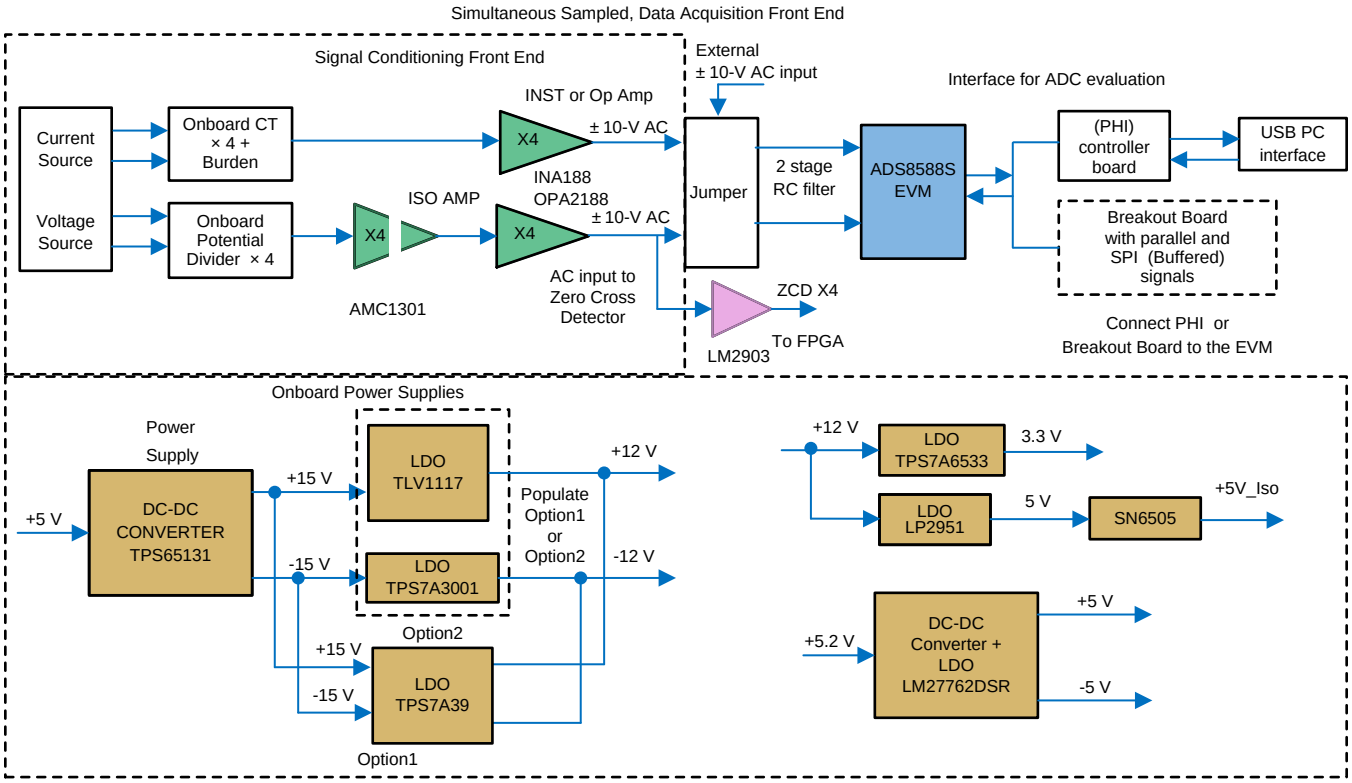


図 1. Block Diagram of DAQ Front End With Isolation and Dual LDO

The block diagram consists of the following functional blocks in 2.7.1.

2.7.1 ADS8588SEVM-PDK Interface to DAQ System

The AC current and voltage input is interfaced to the ADS8588S EVM using an interface connector.

2.7.1.1 DAQ Front-End Interface to ADS8588S ADC EVM Interface Connector

The JP1, 32-pin, TSM-116-01-T-DV-P connector has been provided to facilitate an interface to the DAQ system. The eight ADC inputs are connected to the ADC through the interface connector.

2.7.1.2 ADC EVM Including PHI Controller Board

The ADS8588SEVM-PDK is a platform for evaluating the performance of the ADS8588S SAR ADC. The evaluation kit includes the ADS8588EVM board, PHI controller board, and accompanying computer software which enables a user to communicate with the ADC over a universal serial bus (USB), capture data, and perform data analysis.

Features:

- Includes hardware and software required for diagnostic testing and performance evaluation of the ADS8588 ADC
- Ships with PHI EVM controller which provides a convenient interface to the EVM over USB 2.0 (or higher) for power delivery as well as digital input and output
- Contains easy-to-use evaluation software for Microsoft® Windows 7® and Microsoft Windows 8® 64-bit operating systems
- Contains software suite which includes graphical tools for data capture, output code histogram generation, and linearity analysis, as well as a provision for exporting data to a text file for post-processing

2.7.1.3 Selection of Internal or External Reference for ADC

A jumper provision has been provided for configuring an onboard voltage reference or ADS8588S internal reference.

2.7.1.4 Selection Between AFE Output and External Output for Sampling

A jumper provision has been provided to select the inputs to the ADC on the DAQ board. The output cab be selected between the amplifier output, sensor output, and ±10-V external output for current or voltage inputs.

2.7.2 Current Input Signal Conditioning

The current signal-conditioning circuit includes a CT with a burden that can be configured, an instrumentation amplifier or precision amplifier to scale the CT output to the ADC range, and a jumper to choose between instrumentation or precision amplifier output. An option to connect the output of a shunt-based, isolation amplifier add-on board has also been provided. An option to choose between the amplifier output, the output of a CT with a higher burden, and an external sensor input has been provided.

2.7.3 Voltage Input Signal Conditioning

The voltage signal-conditioning circuit includes a PD whose output can be configured by selection of the resistor values, precision amplifier to scale the PD output to the ADC range, and jumper to choose between a precision amplifier output, PD output, and external sensor input. The precision amplifier output is also connected to a zero-cross detector (ZCD) to generate the square wave for calculating the time period used to generate a conversion start pulse.

2.7.4 Power Supply

The power supply required for the operation of the ADC and the signal-conditioning circuit is generated from a single 5-V input. A DC-DC converter is used to generate ±15 V, which is connected to the dual LDOs or positive or negative LDOs to generate ±13 V, 5 V, and 3 V. In an application where the input range is limited to ±5 V, the design can be simplified by using a DC-DC converter with an integrated LDO to generate a +5-V and –5-V output.

2.7.5 Isolated Power for Voltage Measurement Isolation Amplifier

The isolated power required to operate the isolation amplifier used to measure the voltage inputs with a PD is generated using the SN6505B transformer driver and 5-V LDO.

2.7.6 ADC Reference

The ADC has an internal reference that can be used to simplify the system design. In applications that require a good accuracy performance over a wide range, an external reference can be considered for the ADC. Two reference options are available: one is specified for high performance and the other is a cost-optimized reference. The output of the reference is buffered before connecting to the signal-conditioning circuit. A jumper provision is provided to select the required reference levels, which can be used in situations where the DAQ front end is used with a single-ended ADC.

2.8 Highlighted Products—System Design

2.8.1 ADS8588S EVM Interface

2.8.1.1 AFE-to-ADC EVM Interface Connector JP5

The following 表 2 provides the interface connection details for all eight ADC channels from the DAQ AFE to the ADS8588S EVM.

表 2. JP5 Socket Interface Connections

SOCKET PIN NUMBER	SIGNAL	DESCRIPTION
JP5.2	AIN_1P	Positive analog input for channel AIN1
JP5.4	AIN_1GND	Negative analog input for channel AIN1
JP5.6	AIN_2P	Positive analog input for channel AIN2
JP5.8	AIN_2GND	Negative analog input for channel AIN2
JP5.10	AIN_3P	Positive analog input for channel AIN3
JP5.12	AIN_3GND	Negative analog input for channel AIN3
JP5.14	AIN_4P	Positive analog input for channel AIN4
JP5.16	AIN_4GND	Negative analog input for channel AIN4
JP5.18	AIN_5P	Positive analog input for channel AIN5
JP5.20	AIN_5GND	Negative analog input for channel AIN5
JP5.22	AIN_6P	Positive analog input for channel AIN6

表 2. JP5 Socket Interface Connections (continued)

SOCKET PIN NUMBER	SIGNAL	DESCRIPTION
JP5.24	AIN_6GND	Negative analog input for channel AIN6
JP5.26	AIN_7P	Positive analog input for channel AIN7
JP5.28	AIN_7GND	Negative analog input for channel AIN7
JP5.30	AIN_8P	Positive analog input for channel AIN8
JP5.32	AIN_8GND	Negative analog input for channel AIN8

2.8.1.2 ADC EVM Including PHI Controller Board

The ADS8588SEVM-PDK is a platform for evaluating the performance of the ADS8588S SAR ADC, which is an eight-channel, 16-bit, ±10-V, simultaneous-sampling ADC device. The evaluation kit includes the ADS8588SEVM board and the PHI controller board, which enables the accompanying computer software to communicate with the ADC over USB for data capture and analysis.

Refer to the ADS8588S EVM user's guide for more details: http://www.ti.com/tool/ADS8588SEVM-PDK.

The following list accounts for the major components of the PHI card.

- TPS65217BRSLT, TPS79133DBVT
- REG71055DDCT
- AM3352-ZCZ
- MT47H128M16RT-25E:C
- XC6SLX16-CSG225

2.8.1.3 Selection of Internal or External Reference for ADC

The selection between the internal and external reference is done using J2 on the ADS8588S EVM open-selects internal reference and closed-selects external reference. Use J5 to select the external reference, which is open when using the internal reference and closed when using the external reference. Refer to the jumper setting on the ADS8588S EVM for more details.

2.8.1.4 Selection Between AFE Output and External Output for Sampling

Jumpers are used to configure the DAQ AFE for different sensor output sources. When the external input has been configured, a 100K impedance is enabled. A one-stage resistor-capacitor (RC) filter is provided before connecting the inputs to the ADC. The ADC has another stage of RC filter. Refer to *page 11* of the schematics for more details.

2.8.1.5 GUI for Performance Evaluation

The graphical user interface (GUI) used for performance evaluation provides the following functionalities:

- Input range selection between ±5 V and ±10 V
- ADC interface configuration – serial or parallel
- RMS value display
- Waveform display
- Option for coherent sampling

Refer to the following tool folder and the available user's guide for more information: http://www.ti.com/tool/ADS8588SEVM-PDK.

2.8.1.6 Additional GUI Features

The GUI has some additional features for the purpose of testing the ADS8588S ADC performance for measurement applications:

- Coherent sampling including the capability to adjust the samples per cycle and number of cycles to capture
- Provision to subtract the DC offset from the ADC inputs

These features are not available on the standard GUI. Consult the TI industrial systems team for more information.

2.8.1.7 Coherent Sampling and Frequency Calculation

The coherent sampling is calculated by the GUI as follows:

The zero-crossing detector circuit provides a digital square output signal, which is used to find the frequency of the input analog signal. Coherent sampling begins when the option to "enable frequency track" has been checked and the "capture" button has been pressed in the GUI.

Field-programmable gate array (FPGA) counter:

1. The FPGA counts five consecutive clock cycles of the digital square signal (rising to rising edge), which is counted using a 50-MHz counter and stores the number of ticks for each cycle.

IP signal frequency computation:

1. Five-cycle tick counts are retrieved from the FPGA and the average of tick counts is calculated.
2. The average tick count is converted into frequency by the following formula:
   IP signal frequency (Hz) = 50 MHz / average tick count (50-MHz FPGA counter).
3. The computed IP signal frequency is checked for in the range of 45 Hz to 66 Hz. If not in range, the 50-Hz default value is considered as the signal frequency.

Sampling rate computation:

1. The sampling rate is computed by using the following formula:
   Sampling rate (Hz) = IP signal frequency × number of samples per cycle.
2. The FPGA is configured to generate convert-start pulses at the calculated sampling rate.
3. A custom pattern generator is used to generate the convert-start pulses.

2.8.2 Current Input Signal Conditioning

The current input signal-conditioning circuit has been implemented using an instrumentation amplifier or precision op-amp-based differential amplifier (see 図 2).

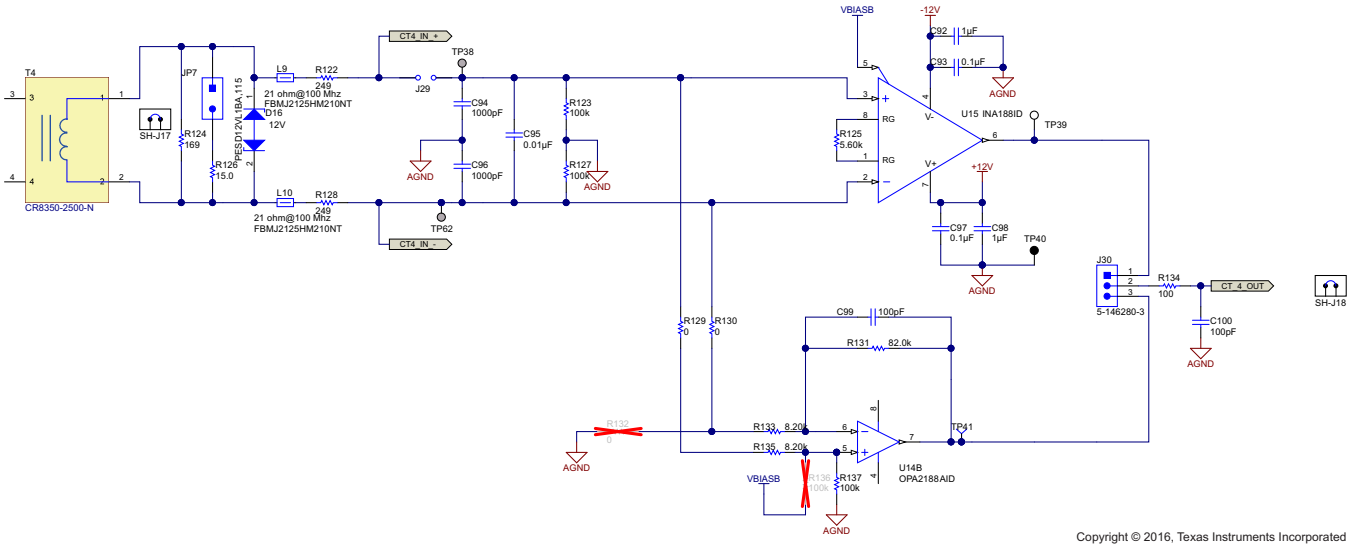


図 2. Current Input Scaling Using Amplifier

2.8.2.1 Measurement With Instrumentation Amplifier INA188

One way to accurately measure a low-voltage output current sensor is to use an instrumentation amplifier, which simplifies the gain adjustment and also improves accuracy. In applications where protection and measurement features are implemented, instrumentation amplifiers are used for measurement because the sensor inputs are expected to be amplified by a gain of 20 or more. In the TIDA-00834 design, the output is configured for a gain of 10. INA188 is a precision instrumentation amplifier that uses TI proprietary auto-zeroing techniques to achieve a near-zero offset and gain drift and excellent linearity.

For more details on the INA188 36-V, zero-drift, rail-to-rail-out instrumentation amplifier, refer to the tool folder at http://www.ti.com/product/INA188.

2.8.2.2 Measurement With Precision Op Amp OPA2188 or OPA2180

An alternative approach for measuring the low-voltage output of the current sensor is to use precision op amps. The op amps are used in differential amplifier mode to achieve maximum accuracy. The OPA2188 operational amplifier provides a low offset voltage (25 µV, maximum) and near zero-drift over time and temperature. This high-precision, low-quiescent current amplifier offers high-input impedance and a rail-to-rail output swing within 15 mV of the rails. The input common-mode range includes the negative rail. Either single or dual supplies can be used in the range of 4 V to 36 V (±2 V to ±18 V). A gain of 10 has been set for scaling the sensor output to the ADC input range. Op amp selection is based on the system performance requirement and applications.

For more details on the 0.03-µV/°C, 6-µV V_{OS}, low-noise, rail-to-rail output, 36-V zero-drift OPA2188 op amp refer to the product folder: http://www.ti.com/product/OPA2188. For more details on the 0.1-uV/°C drift, low-noise, rail-to-rail output, 36-V zero-drift OPA2180 op amp refer to the product folder: http://www.ti.com/product/OPA2180.

Alternatively, for cost-sensitive applications, the OPA2171 can be used. The OPA2171 is a 36-V, single-supply, low-noise operational amplifier with the ability to operate on supplies ranging from 2.7 V (±1.35 V) to 36 V (±18 V). This device offers low offset, drift, and bandwidth with low quiescent current. Unlike most operational amplifiers, which are specified at only one supply voltage, the OPA2171 family is specified from 2.7 to 36 V. Input signals beyond the supply rails do not cause phase reversal. The input can operate 100 mV below the negative rail and within 2 V of the top rail during normal operation. For more details on the OPA2171, refer to the product folder at http://www.ti.com/product/OPA2171.

2.8.2.3 Current Transformer

The current transformer used in this design is the CR8350-2500-N, which is a 100-A, 1:2500 current-sense-transformer, 57-Ω through-hole, solid-core-type transformer with a ±0.2% accuracy. Refer to the following product page for more details: http://www.digikey.com/product-detail/en/cr-magnetics-inc/CR8350-2500-N/582-1015-ND/1045171. Consult CR Magnetics Inc. for more details on the current transformer.

2.8.2.4 Connecting Output of Isolation Amplifier

A provision has been provided in the design to disable the CT output and connect the output from an isolation amplifier such as AMC1200, AMC1100, or AMC1301 to the differential amplifier input for measuring the current with a shunt.

2.8.2.5 Selection Between Instrumentation and Op Amp

A provision has been provided to select the output of an instrumentation amplifier or precision amplifier for current input measurement. 3.1 provides more details on the jumper.

2.8.2.6 Current Input Range Calculation

表 3 provides the calculation for the maximum current input range that can be measured by the DAQ AFE.

表 3. Current Input Measurement Range Calculation

PARAMETERS	SPECIFICATION
Burden (Ω)	13.7780
Max input (V_{RMS})	7.0700
Instrumentation amp gain (A)	9.9200
Max amplifier input (V_{RMS})	0.7127
Max Secondary current (mA_{RMS})	51.7275
Primary current (A_{RMS})	129.3180

2.8.3 Voltage Input Signal Conditioning

2.8.3.1 Measurement With Potential Divider and OPA2188 or OPA2180 Op Amp

The approach to measure the low-voltage output of a potential divider is to use precision op amps. The op amps are used in differential amplifier mode to achieve maximum accuracy. The OPA2188 operational provides a low-offset voltage (25 µV, maximum) and near zero-drift over time and temperature. This high-precision, low-quiescent current amplifier offers a high input impedance and rail-to-rail output swing within 15 mV of the rails (see 図 3). The input common-mode range includes the negative rail. Either single- or dual-supplies can be used in the range of 4 V to 36 V (±2 V to ±18 V). A gain of 5.6 has been set for scaling the sensor output to the ADC input range. The op-amp selection is based on system performance requirement and applications.

For more details on the OPA2188 or OPA2180 refer to the product folders at http://www.ti.com/product/OPA2188 or http://www.ti.com/product/OPA2180.

The input impedance of the potential divider is selected to be ≈1 MΩ, which is the typical input impedance specified for voltage measurement. The potential divider values can be scaled to higher values maintaining the ratios in applications that require higher impedance.

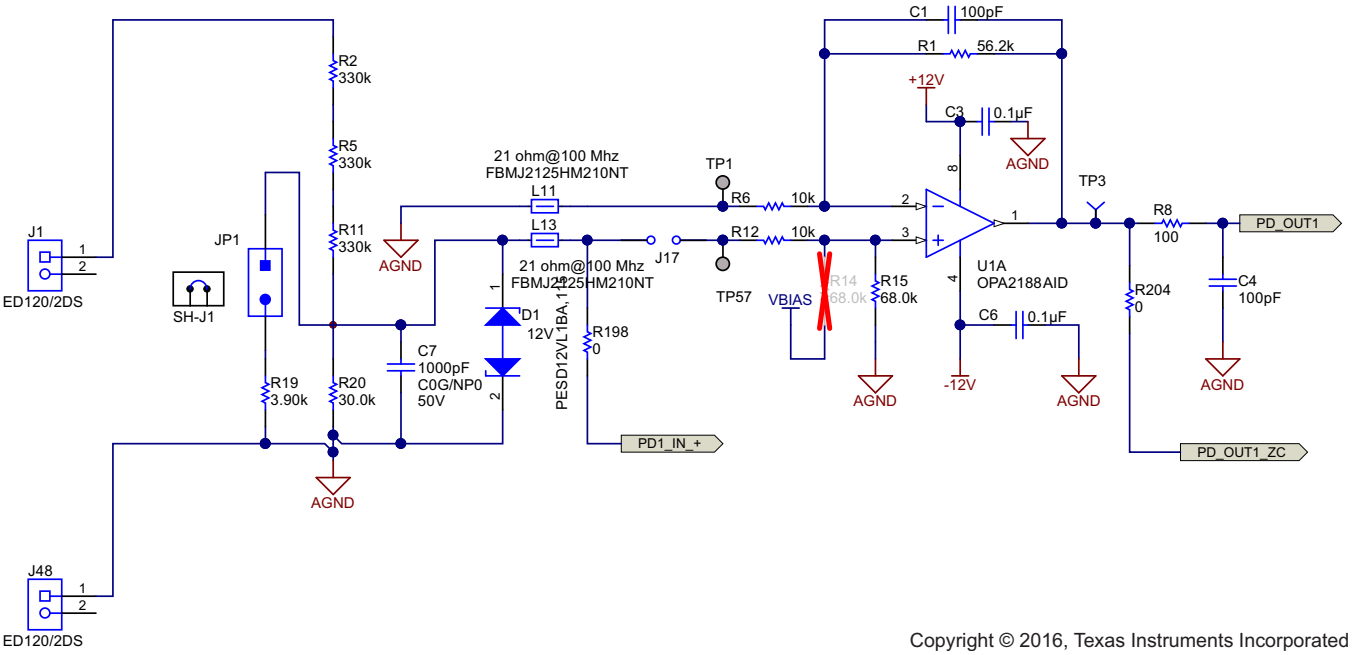


図 3. Voltage Signal Conditioning With Precision Amplifier

2.8.3.2 Measurement With Precision Op Amp OPA2188 and Isolation Amplifier AMC1301 or ISO224

The conventional approach to voltage measurement is to use potential transformers. Potential transformers provide isolation and sufficient measurement accuracy. These transformers are expensive and bulky. One alternative is to use a resistor divider for voltage measurement with the limitation being that the resistor divider does not provide isolation. Using isolation amplifiers is one approach to provide isolation while using a resistor divider.

Isolation amplifiers with basic or reinforced isolation can be used in this application. Isolation amplifiers have a ±250-mV input voltage range, a fixed gain of 8 (0.5% accuracy), and an output signal with DC common-mode voltage.

Precision op amps are used to scale the output of the isolation amplifier to the ADC range. The op amps are used in differential amplifier mode to achieve maximum accuracy and remove the common-mode DC output.

The OPA2188 operational amplifier provides a low-offset voltage (25 µV, maximum), and near zero-drift over time and temperature. This high-precision, low-quiescent current amplifier offers a high input impedance and rail-to-rail output swing within 15 mV of the rails. The input common-mode range includes the negative rail. Either single- or dual-supplies can be used in the range of 4 V to 36 V (±2 V to ±18 V).

For more details on the OPA2188, OPA2180, AMC1301, or AMC1100, refer to the relevant product folders at http://www.ti.com/product/OPA2188, http://www.ti.com/product/OPA2180, http://www.ti.com/product/AMC1301, and http://www.ti.com/product/AMC1100.

For applications where the sensor output is ±10 V and is to be measured with isolation, the ISO224 can be considered. The ISO224 is a precision isolated amplifier with an output separated from the input circuitry by an isolation barrier with high immunity to magnetic interference. The input of the ISO224 is optimized for accurate sensing of ±10-V signals that are widely used in grid applications. The device operates off a single supply on the high-side. The integrated high-side supply voltage detection feature simplifies system level diagnostics. The ±4-V output of the ISO224 allows lower-cost analog-to-digital converters (ADCs) to be used. The differential structure of the output supports high immunity to noise. For more details on the ISO224, refer to the product folder at http://www.ti.com/product/ISO224.

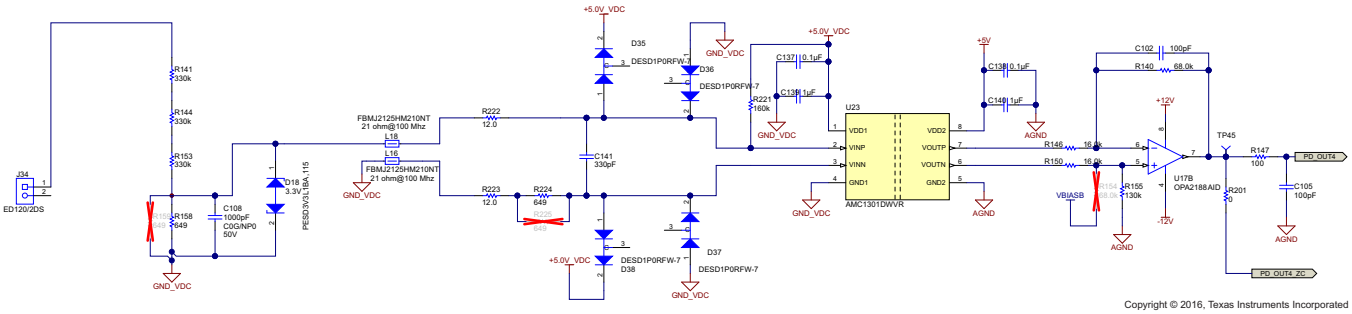


図 4. Voltage Measurement With Isolation Amplifier and Precision Differential Amplifier

注: Concerning offset adjustment: The differential, output common-mode DC voltage of the isolation amplifier can vary and this results in a DC offset at the output of the differential amplifier. The differential stage resistor can be adjusted to reduce the DC offset output to zero.

The input impedance of the potential divider is selected to be ≈1 MΩ, which is the typical input impedance specified for voltage measurement. The potential divider values can be scaled to higher values maintaining the ratios in applications that require higher impedance

2.8.3.3 Potential Transformer

The DAQ AFE has also been tested with a laminated-core-type potential transformer PT120CF or PT120PC which provides a voltage isolation of 4000 V_{RMS}. The dimensions are:
52.40 mm × 27.94 mm × 31.75 mm. The potential transformer has a nominal input of 110 V.

2.8.3.4 Comparator LM2903 for Zero-Cross Detection to Implement Coherent Sampling

Implementation of coherent sampling improves measurement accuracy and system performance when considering the importance of IEC 61000-4-7, IEC61000-4-30, and EN50160 standards. This implementation improves performance when considering true, single-cycle RMS measurements. Coherent sampling can be implemented using an analog or digital PLL. The input to the PLL is a zero-cross detector output of the input voltages. A comparator with a configurable threshold is used to generate the zero-cross output. Any of the phase inputs can be selected for synchronization.

LM2903 devices consist of two independent voltage comparators that are designed to operate from a single power supply over a wide range of voltages. The VCC input must be least 1.5 V more positive than the input common-mode voltage. The outputs can be connected to other open-collector outputs to achieve wired-AND relationships.

注: Note that the signal for frequency measurement (square-wave output of zero-crossing detector) must be given at pin 15 of the QSH-QTH connector on the ADS8588S EVM.

For more details on the LM2903, refer to the product folder at http://www.ti.com/product/LM2903.

2.8.3.5 Voltage Input Range Calculation for Potential Divider

The calculation for the maximum voltage input range measurable by the DAQ AFE has been provided in the following 表 4.

表 4. Voltage Input Measurement Range Calculation

PARAMETERS	SPECIFICATION
Max input (V_{RMS})	7.0700
Precision amplifier gain factor	1:5.62
Max amplifier input (V_{RMS})	1.2580
Potential divider ratio	1:288
Max input voltage (V_{RMS})	362.3060

2.8.4 Power Supply

This section provides details on the different options that are used to generate the power supplies for the DAQ front end.

2.8.4.1 DC-DC Converter for ±15-V TPS65131

The power supply required for operation of the DAQ AFE is generated using a single 5-V input. The TP65131 device is used to generate positive and negative rails from a single input. The TPS65131 is dual-output DC-DC converter which generates a positive output voltage up to 15 V and a negative output voltage down to –15 V, with output currents in a 200-mA range in typical applications depending on the input voltage to output voltage ratio (see 図 5). The converter operates with a fixed-frequency PWM control topology and uses a pulse-skipping mode at light-load currents if the power-save mode has been enabled. The converter operates with only 500-µA device quiescent current. Independent enable pins allow power-up sequencing and power-down sequencing for both outputs. The device has an internal, current-limit overvoltage protection and a thermal shutdown to ensure the highest reliability under fault conditions.

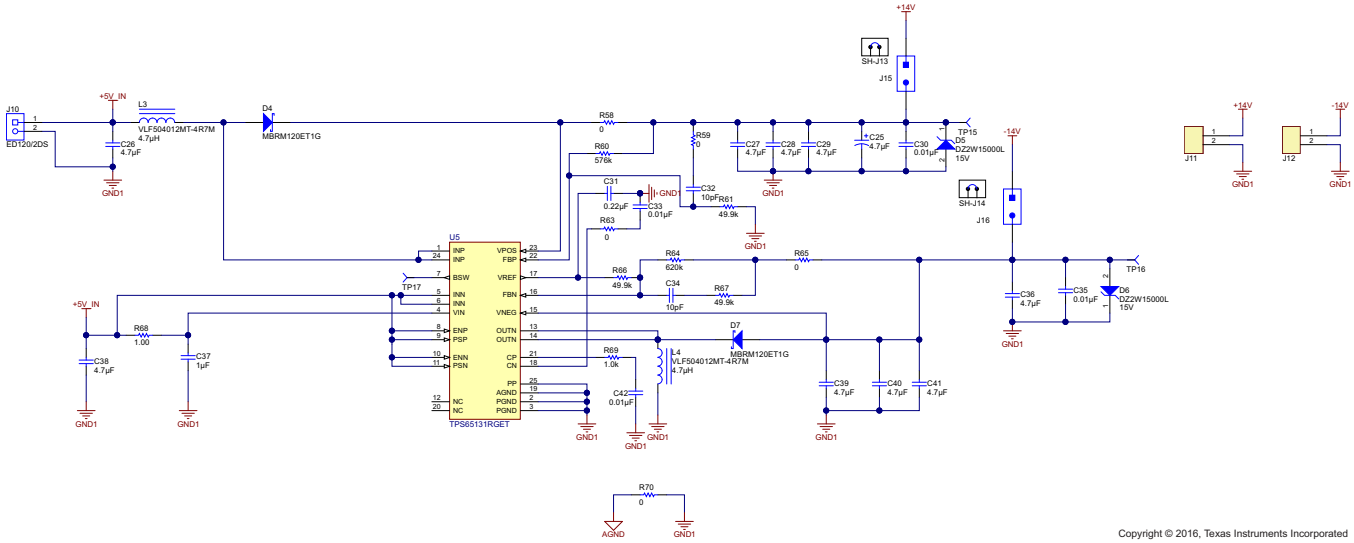


図 5. TPS65131 DC-DC Converter Configuration for Bipolar DC Output

For more details on the TPS65131, refer to the product folder at http://www.ti.com/product/TPS65131.

Alternatively, transformer drivers SN6501 or SN6505B can be used to generate dual supplies. The power requirements are < 60 mA for a ±15-V output.

2.8.4.2 Inverter and LDO for ±5-V Using LM27762

In applications where the ADC has been configured for a ±5-V input, the LM27762 can be considered as a viable option because it simplifies the overall system design. The LM27762 device delivers very-low-noise positive outputs and negative outputs that are adjustable between ±1.5 V and ±5 V. The input voltage range is specified from 2.7 V to 5.5 V and the output current reaches up to ±250 mA. With an operating current of only 390 µA and a 0.5-µA typical shutdown current, the LM27762 device provides an ideal performance for the power amplifier, DAC bias, and other high-current, low-noise negative voltage requirements. *This device achieves an output voltage of ±5.2 V with a 5.5-V input.* This specification is useful in an application where the amplifier with a rail-to-rail output is connected to a ±5-V input ADC and where the application requires to measure the complete range.

For more details on the LM27762, refer to the product folder at http://www.ti.com/product/lm27762.

Alternatively, transformer drivers SN6501 or SN6505B can be used for generation of the required split-rail power supply. For more details on the transformer driver solutions, visit http://www.ti.com/isolation/transformer-driver/products.html.

2.8.4.3 Dual LDO for ±12-V DC Output Using TPS7A39

Dual 150-mA, Positive and Negative LDO TPS7A39 is used to regulate the output of the TPS65131 DC-DC converter. The output of the LDO is connected to the amplifier stage. The TPS7A39 device is a dual monolithic, high-PSRR, positive and negative low-dropout (LDO) voltage regulator capable of sourcing (and sinking) up to 150 mA of current. The regulated outputs can be independently and externally adjusted to symmetrical or asymmetrical voltages, making this device an ideal dual, bipolar power supply for signal conditioning. These features make the TPS7A39 a robust, simplified solution to power op amps, digital-to-analog converters (DACs), and other precision analog circuitry. To configure the dual output LDO to power the gain amplifiers, R234 and R240 are populated and FB2 and FB3 are depopulated.

For more details on the TPS7A39, refer to the product folder at http://www.ti.com/product/TPS7A39.

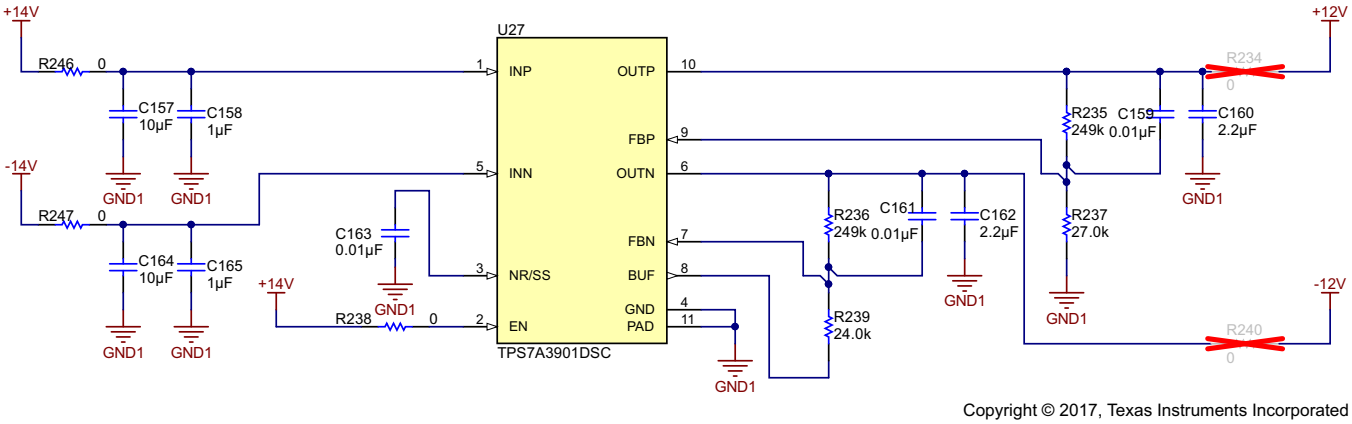


図 6. Gain Amplifier Supply Using Dual LDO Configuration

注: If excessive reverse current flow is expected in the application, then external protection must be used to protect the device (see *Figure 70: Example Circuit for Reverse Current Protection Using a Schottky Diode On Positive Rail* of the TPS7A39 datasheet.

2.8.4.4 LDOs for ±13 V

An LDO is used to regulate the output of the TPS65131 DC-DC converter. The output of the LDO is connected to the amplifier stage. This design implements the use of positive and negative output-type regulators. The selected LDOs have been rated for a higher current than that of the DAQ AFE requirement to account for future expansion. The TPS7A30 family of linear regulators is suitable for post DC-DC converter regulations. Filtering out the output voltage ripple inherent to DC-DC switching conversion allows for the maximum system performance in sensitive instrumentation, test and measurement, audio, and RF applications. To configure a separate LDO output to power the gain amplifiers, FB2 and FB3 are populated and R234 and R240 are depopulated. This is the default configuration in this design.

The TLV1117 device is a positive LDO voltage regulator which has been designed to provide up to 800 mA of output current. The device is available in 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V, and adjustable-output voltage options. The dropout voltage is specified at a maximum of 1.3 V at 800 mA, which decreases at lower load currents.

For more details on the TPS7A30 or TLV1117, refer to the product folders at http://www.ti.com/product/TPS7A30 or http://www.ti.com/product/TLV1117.

2.8.4.5 LDO for 5 V (LP2951) and 3.3 V (TPS71533DCK)

TPS715 LDO voltage regulators offer such benefits as high-input voltage, LDO voltage, low-power operation, and miniaturized packaging. The devices, which operate over an input range of 2.5 V to 24 V, are stable with any capacitor greater than or equal to 0.47 µF. The LDO voltage and low-quiescent current allow operation at extremely-low-power levels. The low-quiescent current (typically 3.2 µA) is stable over the entire range of output load current (0 mA to 50 mA).

The LP2951 devices are bipolar, LDO voltage regulators which can accommodate a wide-input supply voltage range of up to 30 V. The eight-pin LP2951 is able to output a fixed output or adjustable output from the same device. By tying the OUTPUT and SENSE pins together, as well as the FEEDBACK and VTAP pins, the LP2951 device outputs a fixed 5 V, 3.3 V, or 3 V depending on the version. Alternatively, by leaving the SENSE and VTAP pins open and connecting the FEEDBACK pin to an external resistor divider, the output can be set to any value between 1.235 V to 30 V.

For more details on the LP2951, refer to the product folder at http://www.ti.com/product/LP2951.

2.8.4.6 Isolated Power

The isolated power required for powering the high-side of the isolation amplifier is generated using a transformer driver and LDO, as the schematic in the following 図 7 shows.

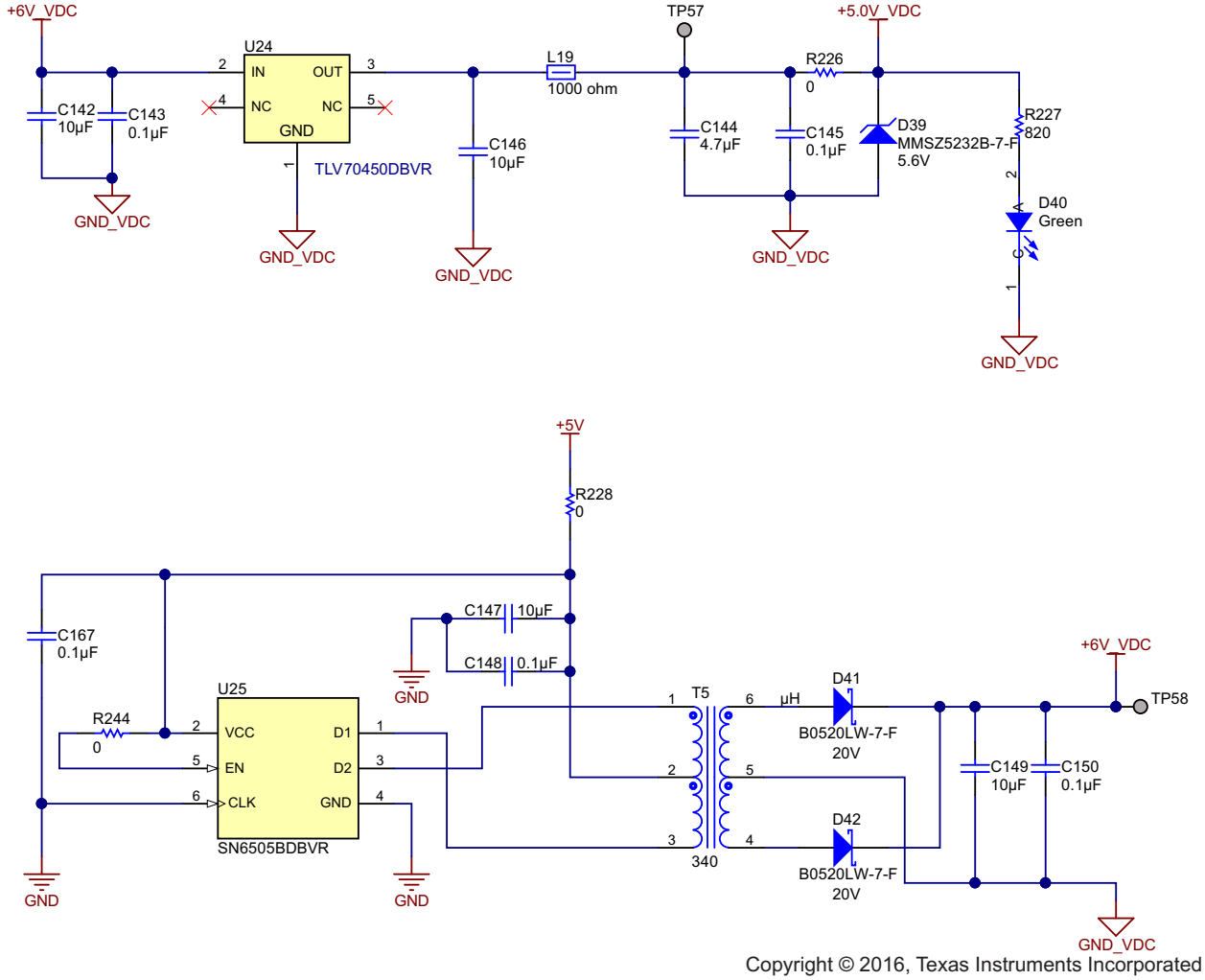


図 7. Isolated Power Supply Using Transformer Driver and LDO

2.8.4.7 DC-DC Converter Using Transformer Driver SN6505B

The SN6505B can be considered for generating the isolated power for applications that are sensitive to electromagnetic interference (EMI) or applications that require meeting EN55022 or EN55011 standards. The SN6505B is a low-noise, low-EMI, push-pull transformer driver, which has been specifically designed for small form-factor, isolated power supplies. The device drives low-profile, center-tapped transformers from a 2.25-V DC to 5-V DC power supply. Ultra-low-noise and EMI can be achieved by slew rate control of the output switch voltage and through spread spectrum clocking (SSC). The SN6505B consists of an oscillator followed by a gate drive circuit which provides the complementary output signals to drive ground-referenced, N-channel power switches. The device includes two, 1-A power-MOSFET switches to ensure start-up under heavy loads. The switching clock can also be provided externally for accurate placement of

switcher harmonics, or when operating with multiple transformer drivers. The internal protection features include a 1.7-A, current-limiting, undervoltage-lockout (UVLO), thermal-shutdown, and break-before-make circuitry. SN6505B includes a soft-start feature that prevents high inrush current during power up with large load capacitors. The SN6505B is available in a small, six-pin SOT23/DBV package. The device operation is characterized for a temperature range from –55°C to 125°C.

For more details on the SN6505B, refer to the product folders at http://www.ti.com/product/SN6505A or http://www.ti.com/product/SN6505B.

Alternatively, SN6501, a low-noise, 350-mA, 410-kHz transformer driver for isolated power supplies can be used for applications requiring lower output current.

For more details on the SN6501, refer to the product folder at http://www.ti.com/product/SN6501.

2.8.5 Stable Reference (for Future Expansion)

2.8.5.1 2.5-V Reference—REF5025 and Buffer OPA322

The REF50xx is a family of low-noise, low-drift, very-high-precision voltage references. These references are capable of both sinking and sourcing current and have excellent line and load regulation. Excellent temperature drift (3 ppm/°C) and high accuracy (0.05%) are achieved using proprietary design techniques. These features, combined with very-low noise, make the REF50xx family ideal for use in high-precision DAQ systems.

The OPA322 single-channel, CMOS operational amplifiers that feature low noise and rail-to-rail inputs and outputs are optimized for low-power, single-supply applications. Specified over a wide supply range of 1.8 V to 5.5 V, the low quiescent current per channel makes these devices well-suited for power-sensitive applications.

For more details on the REF5025 or OPA322 20MH, refer to the product folders at http://www.ti.com/product/REF5025 or http://www.ti.com/product/OPA322.

2.8.5.2 Reference Selection Jumper

The reference can be configured to a positive voltage or ground using the following jumpers in 表 5.

表 5. Reference Jumper Configuration

JUMPERS	+2.5 V	0 V
J13	1-2	2-3
J47	1-2	2-3

2.8.6 Design Enhancements

2.8.6.1 Other TI ADCs Capable of Interfacing to DAQ System

The DAQ system can be interfaced to the following ADCs in 表 6. Based on the input ranges, the gain can be adjusted to make the amplifier output compatible to the ADC input.

表 6. ADC Products Capable of Interfacing to DAQ Front End

SERIAL NUMBER	DC PART NUMBER	ADC DESCRIPTION	INPUT RANGE
1	ADS131A04	24-bit, 128-kSPS, 4-ch, simultaneous-sampling ΔΣ ADC	±4 V

表 6. ADC Products Capable of Interfacing to DAQ Front End (continued)

SERIAL NUMBER	DC PART NUMBER	ADC DESCRIPTION	INPUT RANGE
2	ADS8881	18-bit, 1-MSPS, serial interface, microPower, true-differential input SAR ADC	±5 V
3	ADS9110	18-bit, 680-kSPS, serial interface, microPower, miniature, true-differential input SAR ADC	±5 V
4	ADS8698	18-bit SAR ADC, eight channels, 500 kSPS, and bipolar inputs off +5-V supply	±10.24 V
5	ADS8688	16-bit SAR ADC, four channels, 500 kSPS, and bipolar inputs off +5-V supply	±10.24 V
6	ADS8555	16-bit, six-channel, simultaneous-sampling ADC	±12 V

2.8.6.2 Op Amp Selection

The current design has been tested with OPA2180 and OPA2188 precision amplifiers. TI has a portfolio of precision amplifiers and the following 表 7 lists the op amps to consider based on the application requirement.

表 7. Precision Op Amp Selection for DAQ Front End

SERIAL NUMBER	OP AMP PART NUMBER	OP AMP DESCRIPTION
1	OPA2197	36-V, precision, rail-to-rail input output, low-offset-voltage op amp
2	OPA2192	36-V, precision, RRIO, low-offset-voltage, low-input bias current op amp with e-trim
3	OPA2172	36-V, single-supply, 10-MHz, rail-to-rail output op amp
4	OPA2277	10-µV, 0.1-µV/°C, high-precision, low-power op amp
5	OPA2131	General-purpose FET-input op amps

2.8.6.3 Instrumentation Amplifier Selection

The current design has been tested with an INA188 instrumentation amplifier. TI has a portfolio of instrumentation amplifiers and the following 表 8 lists the amplifiers to consider based on the application requirement.

表 8. Instrumentation Selection for DAQ Front End

SERIAL NUMBER	OP AMP PART NUMBER	INSTRUMENTATION AMPLIFIER DESCRIPTION
1	INA827	Precision, G > 5, 200-uA, 2.7-V to 36-V supply instrumentation amplifier
2	INA826	Precision, 200-µA supply current, 36-V supply instrumentation amplifier
3	INA163	Low-noise, low-distortion instrumentation amplifier
4	INA126	Micropower instrumentation amplifier – single and dual versions
5	INA821	35-µV offset, 7-nV/√Hz noise, low-power, precision instrumentation amplifier
6	INA828	50-µV Offset, 7-nV/√Hz Noise, Low-Power, Precision Instrumentation Amplifier

2.8.6.4 Interface to Other TI Designs With Fluxgate Sensors

Fluxgate current sensors are used for measuring AC or DC current in grid infrastructure applications. Some of the recommended fluxgate sensors that can be used for current measurement include the DRV421 and DRV425. The following TI Designs can be considered for interfacing a fluxgate current sensor output to a DAQ front end:

- TIDA-00201: http://www.ti.com/tool/TIDA-00201
- TIDA-00208: http://www.ti.com/tool/TIDA-00208
- TIDA-00905: http://www.ti.com/tool/TIDA-00905

2.8.6.5 Onboard Temperature Sensor

In precision power measurement applications, the measurement system automatically adjusts its calibration parameters based on real-time temperature readings. Onboard sensors are provided for temperature measurement. A temperature sensor with an analog output LMT70/TMP235 or a digital output LM92/TMP112 can be considered for these applications. The HDC1080 or HDC2010 can be considered for an application that measures temperature and humidity.

2.8.6.6 Interface to AM437x Processor Family

An interface header for easy connection to a precision host interface (PHI) controller board has been provided on the ADS8588S EVM. The PHI controller board uses a Spartan-6 SLX16 and AM335x device to implement the interface between the ADC and the GUI. TI provides other family of processors that can be considered for interfacing with the ADS8588S EVM.

Sitara™ AM437x processors feature:

- Scalable ARM® Cortex®-A9 from 300 MHz up to 1 GHz
- 3D graphics option for enhanced user interface
- Quad-core Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU-ICSS) for industrial Ethernet protocols and position feedback control
- Customer-programmable secure boot option

For more details, refer to the tool folder at: http://www.ti.com/tool/TIDEP0025.

2.8.6.7 Interface to AM572x Processor Family

The ARM® Cortex®-A15 processor has been proven in a range of different markets and is an increasingly popular choice in networking infrastructure, delivering high-performance processing capability combined with low power consumption. The Cortex-A15 processor delivers roughly twice the performance of the Cortex-A9 processor and can achieve 3.5 DMIPS/MHz.

For more details, refer to the tool folder at: http://www.ti.com/tool/TIDEP0076.

2.8.6.8 Current Measurement Using Shunt

The DAQ AFE can be modified to measure current using low-value precision Manganin® shunts. Refer to the following TI Designs for more information:

- TIDA-00738: http://www.ti.com/tool/TIDA-00738
- TIDA-00810: http://www.ti.com/tool/TIDA-00810
- TIDA-00835: http://www.ti.com/tool/TIDA-00835
- TIDA-00912: http://www.ti.com/tool/TIDA-00912
- TIDA-00445: http://www.ti.com/tool/TIDA-00445
- TIDA-020018: http://www.ti.com/tool/TIDA-020018

For measurement of the current-using shunt, the following isolation amplifiers shown in 表 9 can be considered.

表 9. Isolation Amplifier Selection Table

DEVICE	DESCRIPTION
AMC1301	Precision reinforced isolated amplifier for current sensing
AMC1302	Precision reinforced isolated amplifier with ±50-mV input and high CMTI
AMC1300	Reinforced isolated amplifier for current sensing
AMC1300B	Reinforced isolated amplifier for current sensing
AMC1200	±250-mV input, basic isolated amplifier for current sensing
AMC1100	±250-mV input, basic isolated amplifier

2.8.6.9 Isolated Interface for ADS8588S

This section provides approaches to implementing isolated interface when the ADS8588S is interfaced using serial interface. The following signals shown in 表 10 are used to maximize the performance when the ADC is interfaced using serial interface.

表 10. Interface Signals Between ADS8588S and Host Processor

FUNCTION	HOST SIDE (PROCESSOR)	ADS8588S ADC SIDE
CONVSTA	Output	Input
CONVSTB	Output	Input
DOUTA	Input	Output
DOUTB	Input	Output
SCLK	Output	Input
/CS	Output	Input
FRSTDATA	Input	Output
BUSY	Input	Output

For isolation, each signal needs an isolation channel. Based on the performance requirements, the interface can be optimized to minimize the isolation channels as shown in 表 11.

表 11. Optimized Interface Signals Between ADS8588S and Host

FUNCTION	HOST SIDE (PROCESSOR)	ADS8588S ADC SIDE
CONVSTA and CONVSTB Shorted	Output	Input
DOUTA	Input	Output
SCLK	Output	Input
/CS	Output	Input

There are multiple approaches to implementing isolated interface. Isolation using digital isolators provides improved performance and reliability. The following devices can be used to implement isolated interface. The required isolated power can be generated using an external DC/DC converter or transformer driver. Alternatively, digital isolators with integrated power can be used. 表 12 lists some of the commonly used devices for isolations.

表 12. Devices for Implementing Isolated Interface

DEVICE	DESCRIPTION
ISOW7841	High-efficiency, low-emissions, reinforced digital isolator with integrated power
ISO7841	High-immunity, 5.7-kVRMS reinforced quad-channel 3/1 digital isolator, 100 Mbps
ISO7741	High-speed, low-power, robust EMC quad-channel digital isolator
DCH010505S	Miniature, 1-W, 3k VDC isolated DC/DC converters
DCR010505	Miniature, 1-W isolated regulated DC/DC converters
DCP010505	Miniature, 1-W isolated unregulated DC/DC converters
SN6501	Low-noise, 350-mA, 410-kHz transformer driver for isolated power supplies
SN6505B	Low-noise 1-A, 420-kHz transformer driver for isolated power supplies

2.8.6.10 Negative LDO selection

The Signal conditioning amplifier at the input requires dual supply. The following LDO can be considered for generating the required negative voltage supply as shown in table 13

表 13. LDO selection for dual supply output

LDO	Description
TPS7A30	Vin -3V to -36V, -200mA, Ultra-Low-Noise, High-PSRR, Low-Dropout (LDO) Linear Regulator
TPS723	200mA Negative-Output Low-Dropout (LDO) Linear Regulator
TPS7A3401	–20V, –200mA, Low-Noise, Negative-Voltage Low-Dropout Linear Regulator

3 Hardware, Testing Requirements, and Test Results

3.1 Required Hardware

The following connections are required for testing the AFE:

- DC power supply
- Jumper configuration based on the input selection
- AC voltage and current input selection
- Current input
- Interface to EVM with PHI controller board
- Connection for coherent sampling

Connectors have been provided to interface the input. Care must be taken to use the proper connectors, which have been defined in the following subsections.

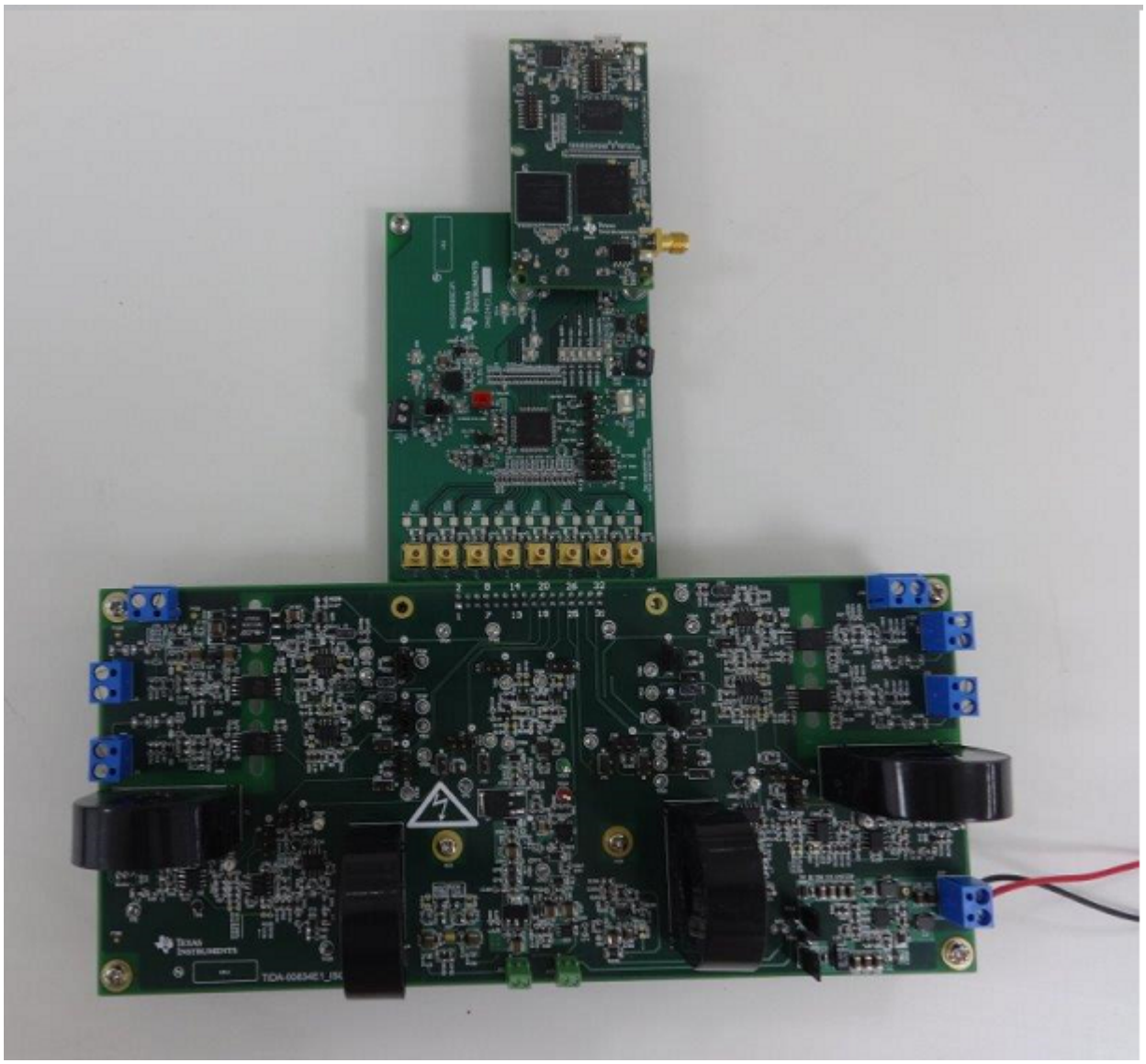


図 8. Setup of DAQ Front End for Performance Testing

3.1.1 Power Supply Jumper

3.1.1.1 External DC Input

A DC input of 5 V is connected using the jumper described in 表 14. This 5-V input generates all of the required power supply.

表 14. External DC Input Connections

JUMPER	PINS	DESCRIPTION
J10	1	DC_IN
	2	AGND

3.1.1.2 Selecting ±5 V or ±14 V for TIDA-00834_Isolated

表 15 provides information on jumper configurations for selecting the DC voltage to the signal-conditioning circuit.

表 15. Jumpers for Configuring Different Supply Voltages for Signal Conditioning

POWER	JUMPER	MOUNT	REMOVE
±14 V	+14 V	J15	R198
	–14 V	J16	R233
±5 V	+5 V	R198	J15
	–5 V	R233	J16

3.1.1.3 Applying External ±15 V for Signal-Conditioning Circuit

表 16 provides information on jumper configurations for selecting the external DC voltage to the signal-conditioning circuit.

表 16. Jumpers for Applying External ±15 V

POWER	JUMPER	CONNECT INPUT	REMOVE
±14 V	+14 V	J11	J15
	–14 V	J12	J16

3.1.1.4 Connection for External +15 V and –15 V

表 17 provides the connector pin information to connect the ±15-V external input for operation of the DAQ front end.

表 17. Connecting +15-V input and –15-V Input

POWER	SUPPLY TYPE	CONNECT INPUT	PIN NUMBER
+15 V	+15V_Inp	J11	1
	+15V_GND		2
–15 V	–15V_Inp	J12	1
	–15V_GND		2

3.1.2 DAQ Front-End Interface

3.1.2.1 Current Inputs

3.1.2.1.1 Current Inputs Using Current Transformers

表 18 provides information on the current transformer connection that can be made for the AC current input to enable measurement by the DAQ AFE.

表 18. Current Input Connection

CURRENT INPUT	ADC CHANNEL	CURRENT TRANSFORMER
1	ADC_Ch5	T1
2	ADC_Ch6	T2
3	ADC_Ch7	T3
4	ADC_Ch8	T4

3.1.2.1.2 Configuration for Higher Burden for Current Transformer

表 19 provides information on the jumpers that can be used to configure the current transformer burden. Burden can be increased or reduced using the jumper configuration.

表 19. Current Transformer Burden Configuration

CURRENT INPUT	CURRENT TRANSFORMER	JUMPER	LOWER BURDEN	HIGHER BURDEN
1	T1	JP3	Mount	Remove
2	T2	JP4	Mount	Remove
3	T3	JP5	Mount	Remove
4	T4	JP6	Mount	Remove

3.1.2.1.3 Configuration for Higher-Burden Output to ADC

表 20 provides information on the jumpers that can be used to configure the current transformer output with a higher burden value for measurement.

表 20. Current Transformer Output With High Burden Configuration to ADC

CURRENT INPUT	CURRENT TRANSFORMER	JUMPER	LOWER BURDEN	HIGHER BURDEN
1	T1	JP19	Mount	Remove
2	T2	JP26	Mount	Remove
3	T3	JP27	Mount	Remove
4	T4	JP29	Mount	Remove

3.1.2.1.4 Selection Between Outputs—Amplifier, CT With Higher Burden, and External CT

表 21 provides information on the jumpers that can be used to configure the output of the DAQ AFE to ADC input.

表 21. Jumper Configuration for Selecting Current Measurement Output to ADC

ADC CHANNEL	JUMPER	OP AMP OUT	CT OUTPUT	EXTERNAL INPUT
ADC_CH5	J20	—	2-3	1-2
	J6	2-3	1-2	1-2
	J22	—	2-3	1-2
ADC_CH6	J21	—	2-3	1-2
	J7	2-3	1-2	1-2
	J23	—	2-3	1-2
ADC_CH7	J37	—	2-3	1-2
	J39	2-3	1-2	1-2
	J41	—	2-3	1-2
ADC_CH8	J38	—	2-3	1-2
	J40	2-3	1-2	1-2
	J42	—	2-3	1-2

3.1.2.1.5 Selection Between Instrumentation and Precision Amplifier

表 22 provides information to configure the signal-condition amplifier outputs for current measurement.

表 22. Signal-Conditioning Amplifier Output Selection

CURRENT INPUT	CURRENT TRANSFORMER	JUMPER	INA AMPLIFIER	PRECISION AMPLIFIER
1	T1	J5	1-2	2.3
2	T2	J14	1-2	2.3
3	T3	J28	1-2	2.3
4	T4	J30	1-2	2.3

3.1.2.2 Non-Isolated Voltage Input

3.1.2.2.1 Voltage Inputs

表 23 provides information on the connectors that can be used to connect the voltage input to enable measurement by the DAQ AFE.

表 23. Voltage Input Connection

VOLTAGE INPUT	ADC CHANNEL	CONNECTOR
1	ADC_CH1	J1-Pin1
2	ADC_CH2	J2-Pin1
3	ADC_CH3	J31-Pin1
4	ADC_CH4	J48-Pin1
—	Reference or neutral	J48-Pin1, J49-Pin1

CAUTION

Ensure that the voltage source has been programmed to zero and the output has been switched off before connecting the input. Also ensure that the return wires are connected to the J48 or J49 connectors.

3.1.2.2.2 Configuration for Higher-Voltage Output From Potential Divider

表 24 provides information on the jumpers that can be used to configure the potential divider output by changing the division factor.

表 24. Higher Output From Potential Divider Output Configuration

VOLTAGE INPUT	ADC CHANNEL	JUMPERS
1	ADC_CH1	JP1
2	ADC_CH2	JP2
3	ADC_CH3	JP8
4	ADC_CH4	JP9

CAUTION

Ensure that the voltage source has been programmed to zero and the output has been switched off before configuring the jumpers.

3.1.2.2.3 Configuration for Higher-Potential Divider Output to ADC

表 25 provides information on the jumpers that can be used to configure the potential divider output to the ADC for measurement.

表 25. Potential Divider Output Configuration to ADC

VOLTAGE INPUT	CONNECTOR	JUMPER	LOWER OUTPUT	HIGHER OUTPUT
1	J1-Pin1	J17	Mount	Remove
2	J2-Pin1	J18	Mount	Remove
3	J31-Pin1	J32	Mount	Remove
4	J34-Pin1	J33	Mount	Remove

3.1.2.2.4 Selection Between Amplifier Output, Potential Divider, and External

表 26 provides information on the jumpers that can be used to configure the output of the DAQ AFE to the ADC input.

表 26. Jumper Configuration for Voltage Measurement Output to ADC

ADC CHANNEL	JUMPER	OP AMP OUT	PD OUTPUT	EXTERNAL INPUT
ADC_CH1	J24	—	2-3	1-2
	J8	2-3	1-2	1-2
ADC_CH2	J25	—	2-3	1-2
	J9	2-3	1-2	1-2
ADC_CH3	J43	—	2-3	1-2
	J45	2-3	1-2	1-2
ADC_CH4	J44	—	2-3	1-2
	J46	2-3	1-2	1-2

3.1.2.3 Isolated Voltage Input

3.1.2.3.1 Voltage Inputs

表 27 provides information on the connectors that can be used to connect the AC voltage input to enable measurement by the DAQ AFE.

表 27. Voltage Input Connection

VOLTAGE INPUT	ADC CHANNEL	CONNECTOR
1	ADC_CH1	J1-Pin1
2	ADC_CH2	J2-Pin1
3	ADC_CH3	J31-Pin1
4	ADC_CH4	J34-Pin1
—	Reference or neutral	J48-Pin1, J49-Pin1

CAUTION

Ensure that the voltage source has been programmed to zero and the output has been switched off before connecting the input. Also ensure that the return wires are connected to the J48 or J49 connectors.

3.1.2.3.2 Selection Between Amplifier Output and External Input

表 28 provides information on the jumpers that can be used to configure the output of the DAQ AFE to the ADC input.

表 28. Jumper Configuration for Voltage Output Selection to ADC

ADC CHANNEL	JUMPER	OP AMP OUT	EXTERNAL INPUT
ADC_CH1	J17	Not mount	Mount
	J8	2-3	1-2
ADC_CH2	J18	Not mount	Mount
	J9	2-3	1-2
ADC_CH3	J24	Not mount	Mount
	J45	2-3	1-2
ADC_CH4	J25	Not mount	Mount
	J46	2-3	1-2

3.1.3 Coherent Sampling

3.1.3.1 Comparator Output

表 29 provides information on the jumpers that are used for connecting the ZCD output to the ADC EVM.

表 29. Configuration Jumpers for Zero-Cross Detector Output

VOLTAGE OUTPUT	JUMPER	OUTPUT CONNECTOR
PD_out1	J3	TP31
PD_out2	J4	
PD_out3	J35	TP46
PD_out4	J35	

3.1.4 DAQ Front-End Interface to ADS8588S EVM JP5

A 32-pin connector that has four-voltage- and four-current signal-conditioned inputs connected is provided for interfacing with the ADS8588S EVM. The EVM can be plugged to the DAQ AFE.

3.2 Testing and Results

3.2.1 Test Setup

図 9 shows the setup that has been made to evaluate the performance of the DAQ system with the ADS8588S device.

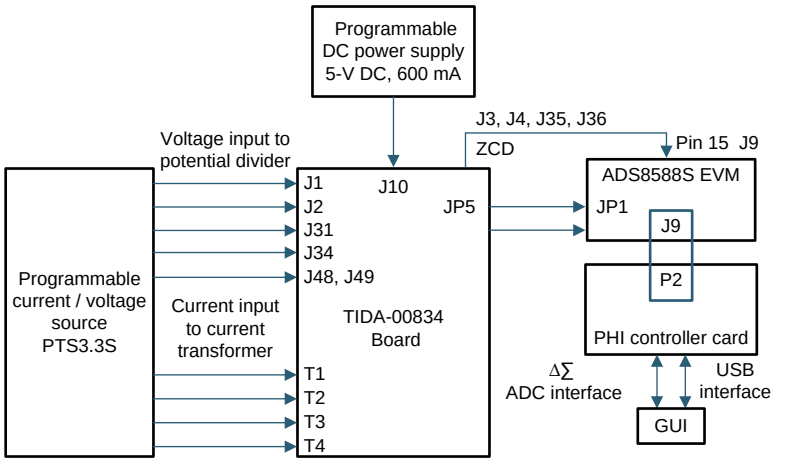


図 9. Test Setup for Interfacing TIDA-00834 With ADS8588S EVM and PHI Controller

The test setup used for testing the DAQ AFE consists of a:

- Current-controlled DC power supply
- Accurate programmable voltage and current source
- ADS8588S EVM
- PHI controller board with AM3352 device
- GUI for evaluation

CAUTION

Ensure that the test engineer makes all connections with the source switched off and experience using programmable voltage and current sources.

3.2.2 Test Results

Note the following conditions regarding the test results:

- All measurements provided in this section are RMS values
- The source uncertainty is ±0.05%
- Care must be taken not to open the current outputs during testing
- The inputs must be connected with the AC voltage and current source output programmed to zero and the output switched OFF
- DC offset was performed and the DC values were subtracted during RMS computation

3.2.2.1 Functional Testing

The functional testing was done by applying the DC input and measuring the power supply output. The required AC_{RMS} voltage and RMS currents were applied for testing the functionality of the SAR ADC.

表 30 shows measurement of different supply voltages and onboard references.

表 30. AFE Functional Testing for Power Supply and Reference

PARAMETERS	SPECIFICATIONS	OBSERVATIONS
Non-isolated power	+15-V DC-DC output	15.220
	–15-V DC-DC output	14.900
	+5-V DC-DC output	14.900
	–5-V DC-DC output	4.914
	+14 V	14.200
	–13.5 V	–13.760
	Dual LDO output +12.2, –12.3	+12.220, –12.280
	+5 V	5.067
	+3.3 V	3.310
Isolated power	+5 V	5.025
Reference	REF5025A output: 2.5 V	2.501
	REF5025A buffer OPA322 op-amp 1 output	2.501
	REF5025A buffer OPA322 op-amp 2 output	2.501
	REF3025A output	2.501

表 31 shows the test results of the amplifier output for current and voltage inputs including the zero-cross comparator output.

表 31. AFE Functional Testing for Signal-Conditioning System

PARAMETERS	SPECIFICATIONS	OBSERVATION
AFE – Current input measurement	CH5 with INA	OK
	CH5 with precision amplifier	OK
	CH6 with INA	OK
	CH6 with precision amplifier	OK
	CH7 with INA	OK
	CH7 with precision amplifier	OK
	CH8 with INA	OK
	CH8 with precision amplifier	OK
AFE – Voltage measurement	Ch1 with isolation amplifier and precision amplifier	OK
	Ch1 with precision amplifier	OK
	Ch2 with isolation amplifier and precision amplifier	OK
	Ch2 with precision amplifier	OK
	Ch3 with isolation amplifier and precision amplifier	OK
	Ch3 with precision amplifier	OK
	Ch4 with isolation amplifier and precision amplifier	OK
	Ch4 with precision amplifier	OK
ZCD for coherent sampling	Voltage input – Ch1	OK
	Voltage input – Ch2	OK
	Voltage input – Ch3	OK
	Voltage input – Ch4	OK

表 32 shows the test results for the interface between the DAQ front end, PHI controller card, and human machine interface (HMI).

表 32. AFE Interface to EVM With PHI Controller Board

PARAMETERS	SPECIFICATIONS	OBSERVATION
ADC interface	Voltage - Ch1	OK
	Voltage - Ch2	OK
	Voltage - Ch3	OK
	Voltage - Ch4	OK
	Current – Ch5	OK
	Current – Ch6	OK
	Current – Ch7	OK
	Current – Ch8	OK
Coherent sampling with	50 Hz	OK
	60 Hz	OK
ADC sampling rates per cycle	80 at 50 cycles per second	OK
	256 at 50 cycles per second	OK
	512 at 50 cycles per second	OK
	1024 at 50 cycles per second	OK
	80 at 60 cycles per second	OK
	256 at 60 cycles per second	OK
	512 at 60 cycles per second	OK
	1024 at 60 cycles per second	OK
ADC input range	±10 V	OK
	±5 V	OK
ADC interface	Serial	OK
	Parallel	OK
PHI controller board	USB interface	OK
	GUI functionality	OK

注: The tests were repeated on two additional boards and the observations were the same as shown in the preceding 表 32.

3.2.2.2 Performance Testing

Accuracy testing of the DAQ front end was tested by interfacing with the ADS8588S EVM.

The EVM was configured for internal reference and the AC inputs were applied from a high-accuracy programmable power source. Testing was done by configuring the ADC to sample at 80 samples per cycle and to capture five cycles of data.

注: Accuracy testing was performed using OPA2188, OPA2180, and INA188 amplifiers.

3.2.2.2.1 AC Input Measurement Accuracy

表 33 shows the measurement accuracy for measuring voltage, which has been configured for measurement using the precision amplifier output.

3.2.2.2.1.1 Measurement Accuracy of AC Voltage Input With Precision Op Amp

表 33. Voltage Measurement With ±10-V ADC Range

VOLTAGE (V)	ADC INPUT (mV)	ACV-1 (mV)	ACV-2 (mV)	ACV-3 (mV)	ACV-4 (mV)	ACV-1 ERROR (%)	ACV-2 ERROR (%)	ACV-3 ERROR (%)	ACV-4 ERROR (%)
3	58.5716	58.990	59.006	58.920	58.916	0.714	0.742	0.595	0.588
4	78.0955	78.106	78.094	78.035	78.059	0.014	–0.002	–0.077	–0.046
5	97.6194	97.627	97.655	97.547	97.552	0.008	0.036	–0.074	–0.069
10	195.2388	195.267	195.246	195.095	195.021	0.014	0.004	–0.074	–0.122
25	488.0970	488.231	488.188	487.826	487.609	0.027	0.019	–0.055	–0.100
50	976.1940	976.724	976.488	975.888	975.469	0.054	0.030	–0.031	–0.074
110	2147.6268	2149.914	2150.507	2148.801	2147.207	0.106	0.134	0.055	–0.020
200	3904.7760	3906.183	3905.159	3902.910	3901.365	0.036	0.010	–0.048	–0.087
230	4490.4924	4492.253	4491.163	4488.549	4486.777	0.039	0.015	–0.043	–0.083
300	5857.1640	5859.704	5858.350	5854.879	5852.767	0.043	0.020	–0.039	–0.075
Min error	—	—	—	—	—	0.008	0.004	–0.074	–0.112
Max error	—	—	—	—	—	0.106	0.134	0.055	–0.020

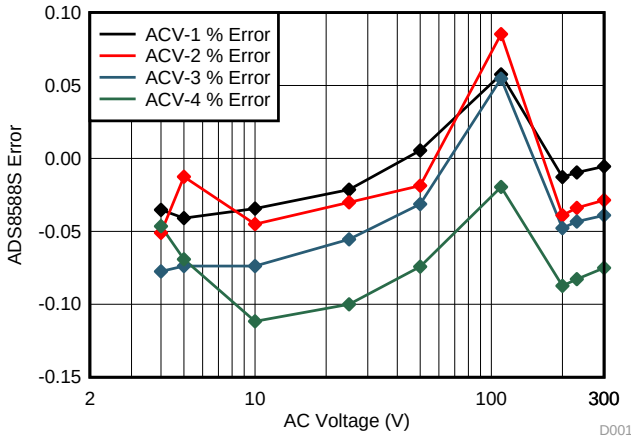


図 10. AC Voltage With Precision Op-Amp Based Amplifier (Voltage Measurement ±10 V)

3.2.2.2.1.2 Measurement Accuracy of AC Current Input With Instrumentation Amplifier

表 34 shows the measurement accuracy for current input, which has been configured for measurement using the instrumentation amplifier output.

表 34. Current Measurement With ±10-V ADC Range Using Instrumentation Amplifier

CURRENT (A)	ADC INPUT (mV)	ACI-5 (mV)	ACI-6 (mV)	ACI-7 (mV)	ACI-8 (mV)	ACI-5 ERROR (%)	ACI-6 ERROR (%)	ACI-7 ERROR (%)	ACI-8 ERROR (%)
0.1	5.4722	5.481	5.479	5.483	5.483	0.169	0.121	0.200	0.189
0.2	10.9444	10.947	10.947	10.945	10.945	0.027	0.026	0.006	0.009
0.3	16.4167	16.412	16.410	16.401	16.397	–0.030	–0.041	–0.094	–0.120
0.5	27.3611	27.362	27.370	27.341	27.321	0.004	0.031	–0.075	–0.148
1.0	54.7222	54.717	54.716	54.662	54.653	–0.009	–0.011	–0.110	–0.127
2.5	136.8056	136.886	136.951	136.775	136.777	0.059	0.106	–0.023	–0.021
5.0	273.6112	273.702	273.833	273.370	273.383	0.033	0.081	–0.088	–0.084
10.0	547.2224	547.212	547.494	546.484	546.649	–0.002	0.050	–0.135	–0.105
20.0	1094.4449	1093.979	1094.565	1093.613	1093.653	–0.043	0.011	–0.076	–0.072
50.0	2736.1122	2733.195	2735.373	2731.308	2731.298	–0.107	–0.027	–0.176	–0.176
80.0	4377.7795	4373.928	4376.577	4370.770	4370.669	–0.088	–0.027	–0.160	–0.162
100.0	5472.2244	5462.499	5465.866	5462.111	5462.088	–0.178	–0.116	–0.185	–0.185
125.0	6840.2805	6830.541	6834.835	6827.081	6826.802	–0.142	–0.080	–0.193	–0.197
Error min	—	—	—	—	—	–0.178	–0.116	–0.193	–0.197
Error max	—	—	—	—	—	0.169	0.121	0.200	0.189

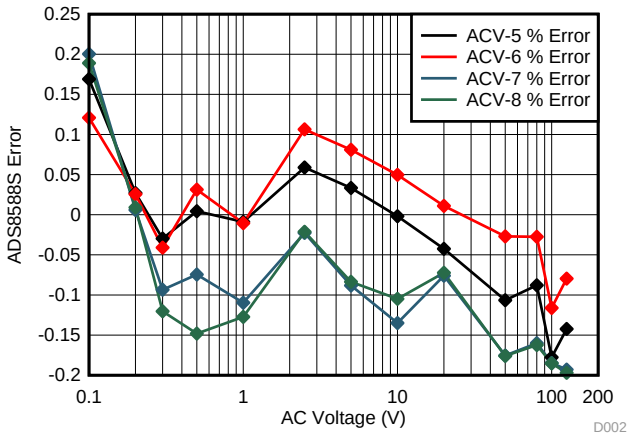


図 11. AC Current I With Instrumentation Amplifier (Current Measurement ±10 V With INA)

3.2.2.2.2 Summary of Accuracy Measurement With Internal Reference

This section provides a summary of the different measurements that have been taken with the DAQ front end with different configurations and sampling rates.

3.2.2.2.2.1 Accuracy Measurement for Voltage Input With ±10-V, 50-Hz ADC Input Range

表 35 provides the measurement accuracy range for voltage inputs with different input and gain amplifier configurations. The errors have been shown as the range for the input voltage and measurement error.

Sufficient points have been measured to be able to plot a graph based on customer requests for data.

表 35. Accuracy Measurement for Voltage Input With Amplifier for ±10-V, 50-Hz ADC Input Range

INPUT TYPE	SAMPLES PER CYCLE	CYCLES AVERAGED	ADC INPUT CHANNEL	AC INPUT	MIN ERROR (%)	MAX ERROR (%)
Potential divider + precision op amp	80	5	1	3 V to 4 V	0.0135	0.7144
				5 V to 300 V	0.0079	0.1064
			2	3 V to 4 V	–0.0021	0.7423
				5 V to 300 V	0.0037	0.1341
			3	3 V to 4 V	–0.0774	0.5945
				5 V to 300 V	–0.0738	0.0546
			4	3 V to 4 V	–0.0464	0.5877
				5 V to 300 V	–0.1116	–0.0195
Potential divider + precision op amp + 4× OSR			1	4 V	0.0483	
				5 V to 300 V	0.0183	0.1120
			2	4 V	0.0981	
				5 V to 300 V	–0.0053	0.0884
			3	4 V	–0.0539	
				5 V to 300 V	–0.0647	0.0430
			4	4 V	–0.0432	
				5 V to 300 V	–0.1024	–0.0055
Potential divider + precision op amp + isolation amplifier			1	3 V	0.5083	
				5 V to 300 V	–0.060	0.0697
			2	3 V	0.491986	
				5 V to 300 V	–0.0714	0.0109
			3	3 V	0.4894	
				5 V to 300 V	–0.0685	0.0118
			4	3 V	0.5901	
				5 V to 300 V	–0.0094	0.0685

表 36 provides the measurement accuracy range for voltage inputs without a gain amplifier.

The errors have been shown as the range for the input voltage and measurement error. Sufficient points have been measured to be able to plot a graph based on customer requests for data.

表 36. Accuracy Measurement for Voltage Input Without Amplifier ±10-V, 50-Hz ADC Input Range

INPUT TYPE	SAMPLES PER CYCLE	CYCLES AVERAGED	ADC INPUT CHANNEL	AC INPUT	MIN ERROR (%)	MAX ERROR (%)
Potential divider with no amplification	80	5	1	3 V to 4 V	0.3131	1.2778
				5 V to 240 V	–0.2138	0.3139
			2	3 V to 4 V	0.2508	1.2032
				5 V to 240 V	–0.3248	0.2508
			3	3 V to 4 V	0.2593	1.2118
				5 V to 240 V	–0.2619	0.2729
			4	3 V to 4 V	0.2199	1.1829
				5 V to 240 V	–0.3208	0.2199
110-V potential transformer with no amplification			1	1 V to 2 V	0.2438	0.4677
				5 V to 150 V	–0.1266	0.0177
			2	1 V to 2 V	0.2233	0.4797
				5 V to 150 V	–0.1350	0.0093
			3	1 V to 2 V	0.2750	0.5152
				5 V to 150 V	–0.1895	0.0446
			4	1 V to 2 V	0.2167	0.4628
				5 V to 150 V	–0.1291	0.0117

表 37 provides the measurement accuracy range for voltage inputs with the precision gain amplifier OPA2180. The errors have been shown as the range for the input voltage and measurement error. Sufficient points have been measured to be able to plot a graph based on customer requests for data.

表 37. Accuracy Measurement for Voltage Input With ±10-V, 50-Hz ADC Input Range (OPA2180)

INPUT TYPE	SAMPLES PER CYCLE	CYCLES AVERAGED	ADC INPUT CHANNEL	AC INPUT	MIN ERROR (%)	MAX ERROR (%)
Potential divider + precision op amp + isolation amplifier	80	5	1	3 V	0.3130	
				5 V to 300 V	–0.0840	0.0700
			2	3 V	0.491986	
				5 V to 300 V	–0.0450	0.0500
			3	3 V	0.20	
				5 V to 300 V	–0.0845	0.0198
			4	3 V	0.20	
				5 V to 300 V	–0.0250	0.0685

3.2.2.2.2 Accuracy Measurement for Voltage Input With ±10-V, 60-Hz ADC Input Range

表 38 provides the measurement accuracy range for the voltage inputs with different input configurations. The errors have been shown as the range for the input voltage and measurement error. Sufficient points have been measured to be able to plot a graph based on customer requests for data

表 38. Accuracy Measurement for Voltage Input With ±10-V, 60-Hz ADC Input Range

INPUT TYPE	SAMPLES PER CYCLE	CYCLES AVERAGED	ADC INPUT CHANNEL	AC INPUT	MIN ERROR (%)	MAX ERROR (%)
Potential divider + precision op amp + isolation amplifier	80	5	1	3 V	0.6803	
				5 V to 300 V	–0.0757	0.0021
			2	3 V	0.6949	
				5 V to 300 V	–0.0762	0.0077
			3	3 V	0.7443	
				5 V to 300 V	–0.0311	0.0516
			4	3 V	0.8042	
				5 V to 300 V	0.0343	0.1122

3.2.2.2.3 Accuracy Measurement for Voltage Input With ±5-V, 50-Hz ADC Input Range

表 39 provides the measurement accuracy range for voltage inputs with different input configurations. The errors have been shown as the range for the input voltage and measurement error. Sufficient points have been measured to be able to plot a graph based on customer requests for data.

表 39. Accuracy Measurement for Voltage Input With ±5-V, 50-Hz ADC Input Range

INPUT TYPE	SAMPLES PER CYCLE	CYCLES AVERAGED	ADC INPUT CHANNEL	AC INPUT	MIN ERROR (%)	MAX ERROR (%)
Potential divider + precision op amp	80	5	1	2 V to 180 V	–0.0775	0.1634
			2	2 V to 180 V	–0.0871	0.1283
			3	2 V to 180 V	–0.1872	0.0620
			4	2 V to 180 V	–0.1637	0.0744
Potential divider with no amplification			1	2 V to 3 V	0.2850	0.5581
				5 V to 115 V	–0.3277	0.2066
			2	2 V to 3 V	0.3032	0.5615
				5 V to 115 V	–0.3494	0.1308
			3	2 V to 3 V	0.3237	0.5796
				5 V to 115 V	–0.2970	0.3237
			4	2 V to 3 V	0.3220	0.5844
				5 V to 115 V	–0.3066	0.1651
110 V with only potential transformer			1	1 V to 80 V	–0.1805	0.1865
			2	1 V to 80 V	–0.1835	0.1906
			3	1 V to 80 V	–0.1841	0.1979
			4	1 V to 80 V	–0.1848	0.1898

3.2.2.2.2.4 Accuracy Measurement for Current Input With ±10-V, 50-Hz ADC Input Range

表 40 provides the measurement accuracy range for the current inputs with different input and amplifier configurations. The errors have been shown as the range for the input voltage and measurement error. Sufficient points have been measured to be able to plot a graph based on customer requests for data.

表 40. Accuracy for Current Input With Gain Amplifier for ±10-V, 50-Hz ADC Input Range

INPUT TYPE	SAMPLES PER CYCLE	CYCLES AVERAGED	ADC INPUT CHANNEL	AC INPUT	MIN ERROR (%)	MAX ERROR (%)
Current transformer + INA	80	5	5	0.1 A to 125 A	–0.1777	0.1690
			6	0.1 A to 125 A	–0.1162	0.1208
			7	0.1 A to 125 A	–0.1929	0.2003
			8	0.1 A to 125 A	–0.1970	0.1889
Current transformer + INA + OSR			5	0.1 A to 125 A	–0.1375	0.2258
			6	0.1 A to 125 A	–0.0748	0.1684
			7	0.1 A to 125 A	–0.2083	0.2960
			8	0.1 A to 125 A	–0.2084	0.2562
Current transformer + precision op amp			5	0.1 A to 125 A	–0.2089	0.1949
			6	0.1 A to 125 A	–0.1016	0.1659
			7	0.1 A to 125 A	–0.1073	0.1954
			8	0.1 A to 125 A	–0.2106	0.1854

表 41 provides the measurement accuracy range for current inputs without amplifier configurations. The errors have been shown as the range for the input voltage and measurement error. Sufficient points have been measured to be able to plot a graph based on customer requests for data.

表 41. Accuracy for Current Input Without Gain Amplifier for ±10-V, 50-Hz ADC Input Range

INPUT TYPE	SAMPLES PER CYCLE	CYCLES AVERAGED	ADC INPUT CHANNEL	AC INPUT	MIN ERROR (%)	MAX ERROR (%)
Current transformer with higher burden and no amplifier	80	5	5	0.1 A	0.3361	
				0.2 A to 105 A	–0.1909	0.1750
			6	0.1 A	0.2687	
				0.2 A to 105 A	–0.1299	0.1895
			7	0.1 A	0.1730	
				0.2 A to 105 A	–0.1263	0.0681
			8	0.1 A	0.0979	
				0.2 A to 105 A	–0.0737	0.0889

3.2.2.2.2.5 Accuracy Measurement for Current Input With ±5-V, 50-Hz ADC Input Range

表 42 provides the measurement accuracy range for current inputs with different input configurations. The errors have been shown as the range for the input voltage and measurement error. Sufficient points have been measured to be able to plot a graph based on customer requests for data.

表 42. Accuracy Measurement for Current Input With ±5-V, 50-Hz ADC Input Range

INPUT TYPE	SAMPLES PER CYCLE	CYCLES AVERAGED	ADC INPUT CHANNEL	AC INPUT	MIN ERROR (%)	MAX ERROR (%)
Current transformer + INA	80	5	5	0.06 A	0.4067	
				0.1 A to 65 A	–0.1790	0.2205
			6	0.06 A	0.6540	
				0.1 A to 65 A	–0.2049	0.1910
			7	0.06 A	0.3794	
				0.1 A to 65 A	–0.2005	0.2055
			8	0.06 A	0.3804	
				0.1 A to 65 A	–0.0605	0.2064
Current transformer + precision op amp			5	0.06 A	0.544745	
				0.1 A to 65 A	–0.2023	0.1830
			6	0.06 A	0.3814	
				0.1 A to 65 A	–0.1934	0.1104
			7	0.06 A	0.1829	
				0.1 A to 65 A	–0.1794	–0.0256
			8	0.06 A	0.1613	
				0.1 A to 65 A	–0.1561	0.0662
Current transformer with higher burden and no amplifier			5	0.05 A	0.3663	
				0.1 A to 65 A	–0.1159	0.1745
			6	0.05 A	0.23	
				0.1 A to 65 A	–0.1366	0.056
			7	0.05 A	0.525407	
				0.1 A to 65 A	–0.1321	0.1430
			8	0.05 A	0.1334	
				0.1 A to 65 A	–0.1797	0.0139

3.2.2.2.2.6 Accuracy Measurement for One Cycle Current and Voltage Input With ±10-V, 50-Hz ADC Input Range

表 43 provides the measurement accuracy range for the current and voltage inputs with different input configurations. The errors have been shown as the range for the input voltage and measurement error. Sufficient points have been measured to be able to plot a graph based on customer requests for data.

表 43. Accuracy Measurement for One Cycle Current and Voltage Input With ±10-V, 50-Hz ADC Input Range

INPUT TYPE	SAMPLES PER CYCLE	CYCLES AVERAGED	ADC INPUT CHANNEL	AC INPUT	MIN ERROR (%)	MAX ERROR (%)
Potential divider + precision op amp	80	1	1	2 V to 300 V	–0.1730	0.1786
			2	2 V to 300 V	–0.1339	0.1830
			3	2 V to 300 V	–0.1584	0.1891
			4	2 V to 300 V	–0.2063	0.1785
Current transformer + INA			7	0.1 A to 130 A	–0.1735	0.3839
			8	0.1 A to 130 A	–0.1540	0.2484

3.2.2.2.2.7 Accuracy Measurement for 512 Samples Per Cycle Current and Voltage Input With ±10-V, 60-Hz ADC Input Range

表 44 provides the measurement accuracy range for the current and voltage inputs with different input configurations. The errors have been shown as the range for the input voltage and measurement error. Sufficient points have been measured to be able to plot a graph based on customer requests for data.

表 44. Measurement With 512 Samples Current and Voltage Input With ±10-V, 60-Hz ADC Input Range

INPUT TYPE	SAMPLES PER CYCLE	CYCLES AVERAGED	ADC INPUT CHANNEL	AC INPUT	MIN ERROR (%)	MAX ERROR (%)
Potential divider + precision op amp	512	5	1	2 V to 4 V	0.4206	0.9390
				5 V to 300 V	–0.0879	0.0184
			2	2 V to 4 V	0.4607	1.0026
				5 V to 300 V	–0.0312	0.0807
			3	2 V to 4 V	0.4423	0.9741
				5 V to 300 V	–0.058	0.0483
			4	2 V to 4 V	0.4074	0.9237
				5 V to 300 V	–0.1007	0.0309
Current transformer + INA			7	0.1 A	0.3555	
				0.2 A to 130 A	–0.0823	0.0530
			8	0.1 A	0.2295	
				0.2 A to 130 A	–0.1164	0.1823

3.2.2.2.2.8 Accuracy Measurement for 1024 Samples Per Cycle Current and Voltage Input With ±10-V, 60-Hz ADC Input Range

表 45 provides the measurement accuracy range for the current and voltage inputs with different input configurations. The errors have been shown as the range for the input voltage and measurement error. Sufficient points have been measured to be able to plot a graph based on customer requests for data.

表 45. Measurement With 1024 Samples Per Cycle Current and Voltage Input With ±10-V, 60-Hz ADC Input Range

INPUT TYPE	SAMPLES PER CYCLE	CYCLES AVERAGED	ADC INPUT CHANNEL	AC INPUT	MIN ERROR (%)	MAX ERROR (%)
Potential divider + precision op amp	1024	5	1	2 V to 4 V	0.3205	0.8436
				5 V to 300 V	–0.0682	0.0325
			2	2 V to 4 V	0.3114	0.8551
				5 V to 300 V	–0.0744	0.0464
			3	2 V to 4 V	0.3545	0.8843
				5 V to 300 V	–0.0503	0.0641
			4	2 V to 4 V	0.3028	0.5666
				5 V to 300 V	–0.0939	0.0447
Current transformer + INA			7	0.1 A	0.2705	
				0.2 A to 130 A	–0.1000	0.0246
			8	0.1 A	0.1917	
				0.2 A to 130 A	–0.1173	0.1634

3.2.2.2.3 Summary of Accuracy Measurement With External Reference

3.2.2.2.3.1 Accuracy Measurement for ±10-V, 50-Hz ADC Input Range

表 46 provides the measurement accuracy range for the current and voltage inputs with different input configurations. The errors have been shown as the range for the input voltage and measurement error. Sufficient points have been measured to be able to plot a graph based on customer requests for data.

表 46. Accuracy Measurement for ±10-V, 50-Hz ADC Input Range

INPUT TYPE	SAMPLES PER CYCLE	CYCLES AVERAGED	ADC INPUT CHANNEL	AC INPUT	MIN ERROR (%)	MAX ERROR (%)
Potential Divider + precision op amp	80	5	1	1 V to 4 V	–0.0683	0.5827
				5 V to 300 V	–0.1808	–0.0071
			2	1 V to 4 V	–0.0414	0.6396
				5 V to 300 V	–0.1424	0.0496
			3	1 V to 4 V	0.0849	0.7315
				5 V to 300 V	–0.0190	0.1729
			4	1 V to 4 V	–0.0064	0.6459
				5 V to 300 V	–0.1151	0.0963
Current transformer + INA			7	0.05 A to 0.1 A	0.4033	0.9424
				0.2 A to 130 A	–0.1356	0.0788
			8	0.05 A to 0.1 A	0.3347	0.6370
				0.2 A to 130 A	–0.1235	0.0985
Potential divider + precision op amp	256		1	1 V to 4 V	0.1243	0.3896
				5 V to 300 V	–0.1187	–0.0452
			2	1 V to 4 V	0.1294	0.4542
				5 V to 300 V	–0.0703	0.0136
			3	1 V to 4 V	0.1159	0.4281
				5 V to 300 V	–0.0880	–0.0129
			4	1 V to 4 V	0.1249	0.3978
				5 V to 300 V	–0.0954	0.0864
Current transformer + INA			7	0.1 A to 130 A	–0.1594	0.1752
			8	0.1 A to 130 A	–0.1551	0.1634

3.2.2.2.3.2 Accuracy Measurement for ±10-V, 60-Hz ADC Input Range

表 47 provides the measurement accuracy range for the current and voltage inputs with different input configurations. The errors have been shown as the range for the input voltage and measurement error. Sufficient points have been measured to be able to plot a graph based on customer requests for data.

表 47. Accuracy Measurement for ±10-V, 60-Hz ADC Input Range

INPUT TYPE	SAMPLES PER CYCLE	CYCLES AVERAGED	ADC INPUT CHANNEL	AC INPUT	MIN ERROR (%)	MAX ERROR (%)
Potential divider + precision op amp	80	5	1	2 V to 4 V	0.1730	0.2878
				5 V to 300 V	–0.1274	–0.0020
			2	2 V to 4 V	0.0623	0.2844
				5 V to 300 V	–0.0700	0.0564
			3	2 V to 4 V	0.1103	0.2976
				5 V to 300 V	–0.0434	0.0777
			4	2 V to 4 V	0.1957	0.2926
				5 V to 300 V	–0.0272	0.1004
Current transformer + INA			7	0.1 A to 130 A	–0.1502	0.1858
			8	0.1 A to 130 A	–0.1541	0.1929

3.2.2.2.3.3 Accuracy Measurement for 256 Samples: ±10-V, 60-Hz ADC Input Range

表 48 provides the measurement accuracy range for the current and voltage inputs with different input configurations. The errors have been shown as the range for the input voltage and measurement error. Sufficient points have been measured to be able to plot a graph based on customer requests for data.

表 48. Accuracy Measurement for 256 Samples: ±10-V, 60-Hz ADC Input Range

INPUT TYPE	SAMPLES PER CYCLE	CYCLES AVERAGED	ADC INPUT CHANNEL	AC INPUT	MIN ERROR (%)	MAX ERROR (%)
Potential divider + precision op amp	256	5	1	2 V to 300 V	–0.0556	0.1716
			2	2 V to 300 V	–0.1149	0.1337
			3	2 V to 300 V	–0.0679	0.1550
			4	2 V to 300 V	–0.1200	0.0354
Current transformer + INA			7	0.1 A to 130 A	–0.1949	0.1641
			8	0.1 A to 130 A	–0.0814	0.1457

3.2.2.2.3.4 Accuracy Measurement for One and Three Cycles: ±10-V, 50-Hz ADC Input Range

表 49 provides the measurement accuracy range for the current and voltage inputs with different input configurations. The errors have been shown as the range for the input voltage and measurement error. Sufficient points have been measured to be able to plot a graph based on customer requests for data.

表 49. Accuracy Measurement for One and Three Cycles: ±10-V, 50-Hz ADC Input Range

INPUT TYPE	SAMPLES PER CYCLE	CYCLES AVERAGED	ADC INPUT CHANNEL	AC INPUT	MIN ERROR (%)	MAX ERROR (%)
Potential divider + precision op amp	80	3	1	2 V to 4 V	0.1146	0.6893
				5 V to 300 V	–0.1492	0.147115
			2	2 V to 4 V	0.0872	0.7239
				5 V to 300 V	–0.0911	0.2043
			3	2 V to 4 V	0.0847	0.7055
				5 V to 300 V	–0.1231	0.1769
			4	2 V to 4 V	0.1112	0.6703
				5 V to 300 V	–0.0944	0.2004
Current transformer + INA			7	0.1 A	0.5477	
				0.2 A to 130 A	–0.1706	0.1406
			8	0.1 A	0.4222	
				0.2 A to 130 A	–0.1569	0.1433
Potential divider + precision op amp		1	1	1 V to 4 V	0.4994	0.7521
				5 V to 300 V	–0.0177	0.1275
			2	1 V to 4 V	0.3078	0.6597
				5 V to 300 V	–0.1565	–0.0062
			3	1 V to 4 V	0.5421	0.7551
				5 V to 300 V	0.00172	0.1578
			4	1 V to 4 V	0.4740	0.7323
				5 V to 300 V	–0.0382	0.1416
CT + INA			7	0.1 A to 130 A	–0.1961	0.2861
			8	0.1 A to 130 A	–0.1887	0.2080

3.2.2.2.3.5 Accuracy Measurement Without Amplification for ±10-V, 50-Hz ADC Input Range

表 50 provides the measurement accuracy range for the current and voltage inputs with different input configurations. The errors have been shown as the range for the input voltage and measurement error. Sufficient points have been measured to be able to plot a graph based on customer requests for data.

表 50. Accuracy Measurement Without Amplification for ±10-V, 50-Hz ADC Input Range

INPUT TYPE	SAMPLES PER CYCLE	CYCLES AVERAGED	ADC INPUT CHANNEL	AC INPUT	MIN ERROR (%)	MAX ERROR (%)
110-V potential transformer – no op amplifier	80	5	1	2 V	–0.1545	
				5 V to 150 V	–0.0221	0.1092
			2	2 V	–0.1956	
				5 V to 150 V	–0.0405	0.1480
			3	2 V	–0.1799	
				5 V to 150 V	–0.0414	0.1504
			4	2 V	–0.2017	
				5 V to 150 V	–0.0414	0.1550
CT without amplifier, higher burden			7	0.1 A to 100 A	–0.1533	0.2006
			8	0.1 A to 100 A	–0.1946	0.1512

3.2.2.2.3.6 Accuracy Measurement for ±5-V, 60-Hz ADC Input Range

表 51 provides the measurement accuracy range for the current and voltage inputs with different input configurations. The errors have been shown as the range for the input voltage and measurement error. Sufficient points have been measured to be able to plot a graph based on customer requests for data.

表 51. Accuracy Measurement for ±5-V, 60-Hz ADC Input Range

INPUT TYPE	SAMPLES PER CYCLE	CYCLES AVERAGED	ADC INPUT CHANNEL	AC INPUT	MIN ERROR (%)	MAX ERROR (%)
Potential divider + precision op amp	80	3	1	2 V to 4 V	0.1637	0.2665
				5 V to 175 V	–0.1798	0.1596
			2	2 V to 4 V	0.1892	0.2703
				5 V to 175 V	–0.156	0.1815
			3	2 V to 4 V	0.2752	0.4019
				5 V to 175 V	–0.0341	0.1731
			4	2 V to 4 V	0.1531	0.2535
				5 V to 175 V	–0.1702	0.1753
Current transformer with higher burden and no amplifier			7	0.05 A	0.6884	
				0.1 A to 65 A	–0.1401	0.1964
			8	0.05 A	0.5128	
				0.1 A to 65 A	–0.2298	0.2200

3.2.2.2.3.7 Accuracy Measurement for 512 Samples: ±10-V, 60-Hz ADC Input Range

表 52 provides the measurement accuracy range for the current and voltage inputs with different input configurations. The errors have been shown as the range for the input voltage and measurement error. Sufficient points have been measured to be able to plot a graph based on customer requests for data.

表 52. Accuracy Measurement for 512 Samples: ±10-V, 60-Hz ADC Input Range

INPUT TYPE	SAMPLES PER CYCLE	CYCLES AVERAGED	ADC INPUT CHANNEL	AC INPUT	MIN ERROR (%)	MAX ERROR (%)
Potential divider + precision op amp	512	5	1	2 V to 4 V	0.2274	0.5316
				5 V to 300 V	–0.1495	0.0095
			2	2 V to 4 V	0.2983	0.5547
				5 V to 300 V	–0.1685	0.0240
			3	2 V to 4 V	0.2494	0.5700
				5 V to 300 V	–0.1452	0.0430
			4	2 V to 4 V	0.2533	0.5556
				5 V to 300 V	–0.1277	0.0714
Current transformer + INA			7	0.1 A	0.2894	
				0.2 A to 130 A	–0.0906	0.0212
			8	0.1 A	0.2200	
				0.2 A to 130 A	–0.1182	0.1303

3.2.2.2.3.8 Accuracy Measurement for 1024 Samples: ±10-V, 60-Hz ADC Input Range

表 53 provides the measurement accuracy range for the current and voltage inputs with different input configurations. The errors have been shown as the range for the input voltage and measurement error. Sufficient points have been measured to be able to plot a graph based on customer requests for data.

表 53. Accuracy Measurement for 1024 Samples: ±10-V, 60-Hz ADC Input Range

ADC INPUT RANGE AND FREQUENCY	INPUT TYPE	SAMPLES PER CYCLE	CYCLES AVERAGED	ADC INPUT CHANNEL	AC INPUT	MIN ERROR IN %	MAX ERROR IN %
±10 V, 60 Hz	Potential divider + precision op amp	1024	5	1	2 V to 4 V	0.2256	0.7443
					5 V to 300 V	–0.1462	0.0300
				2	2 V to 4 V	0.2095	0.7820
					5 V to 300 V	–0.1381	0.0402
				3	2 V to 4 V	0.2442	0.7969
					5 V to 300 V	–0.1161	0.0566
				4	2 V to 4 V	0.2463	0.8016
					5 V to 300 V	–0.0984	0.0882
	Current transformer + INA			7	0.1 A	0.2705	
					0.2 A to 130 A	–0.1073	0.0152
				8	0.1 A	0.1728	
					0.2 A to 130 A	–0.1332	0.1020

3.2.3 Performance Testing With Other ADS85XXS Family Devices

There are devices with different analog input and resolution in the ADS85XXS family. In this design, performance testing is done with the following devices listed in 表 54. The performance is within the expected measurement accuracy range.

表 54. Details of Different ADCs Interfaced to TIDA-00834 TI Design

DEVICE	DESCRIPTION
ADS8578S	14-Bit High-Speed 8-Channel Simultaneous-Sampling ADC With Bipolar Inputs on a Single Supply
ADS8584S	16-Bit High-Speed 4-Channel Simultaneous-Sampling ADC With Bipolar Inputs on a Single Supply
ADS8586S	16-Bit High-Speed 6-Channel Simultaneous-Sampling ADC With Bipolar Inputs on a Single Supply
ADS8588H	16-Bit 500kSPS 8-Channel Simultaneous-Sampling ADC With Bipolar Inputs on a Single Supply
ADS8598S	18-Bit 200kSPS 8-Channel Simultaneous-Sampling ADC With Bipolar Inputs on a Single Supply
ADS8598H	18-Bit 500kSPS 8-Channel Simultaneous-Sampling ADC With Bipolar Inputs on a Single Supply

3.2.4 Additional Accuracy Test Results With ADS85XXX Family of Devices

The following family of simultaneous-sampling ADCs with bipolar inputs on a single supply are available to choose based on the application requirement and were tested for performance.

- ADS8598H, 18-Bit 500kSPS 8-Channel Simultaneous-Sampling ADC With Bipolar Inputs on a Single Supply
- ADS8598S, 18-bit 200-kSPS 8-channel simultaneous-sampling ADC with bipolar inputs on a single supply
- ADS8588H, 16-bit 500-kSPS 8-channel simultaneous-sampling ADC with bipolar inputs on a single supply
- ADS8588S, 16-bit high-speed 8-channel simultaneous-sampling ADC with bipolar inputs on a single supply
- ADS8586S, 16-bit high-speed 6-channel simultaneous-sampling ADC with bipolar inputs on a single supply
- ADS8584S, 16-bit high-speed 4-channel simultaneous-sampling ADC with bipolar inputs on a single supply
- ADS9578S, 14-bit high-speed 8-channel simultaneous-sampling ADC with bipolar inputs on a single supply

表 55 provides the summary of tests performed and the test results for the ADS85XXX family of devices.

表 55. ADS85XXX ADC Family of Devices Test Summary

TESTS	OBSERVATIONS FOR ADS8598S and ADS8598H	OBSERVATIONS FOR ADS8588H	OBSERVATIONS FOR ADS8584S	OBSERVATIONS FOR ADS8578S
±5-V, ±10-V range measurement accuracy	Meets requirements	Meets requirements	Meets requirements	Meets requirements
Measurement range	>1:1000	>1:1000	>1:1000	>1:250
Measurement accuracy	±0.1%	±0.25%	±0.25%	±0.25%
Serial and parallel interface	OK	OK	OK	OK
All input channels measurement accuracy	All 8 channels	All 8 channels	All 4 channels	All 8 channels
Sampling speed and measurement accuracy	Sampled up to 200 KSPS, meets requirements	Sampled up to 500 KSPS, meets requirements	Sampled up to 330 KSPS, meets requirements	Sampled up to 200 KSPS, meets requirements
Oversampling and measurement accuracy	Meets requirements	Meets requirements	Meets requirements	Meets requirements
Measurement accuracy with internal reference	Meets requirements	Meets requirements	Meets requirements	Meets requirements
Measurement accuracy with external reference (J2, J5 on EVM mounted)	Meets requirements	Meets requirements	Meets requirements	Meets requirements

3.2.4.1 Test Results for ADS8598S

The ADS8598S device is an 8-channel, integrated data acquisition (DAQ) system based on a 18-bit successive approximation (SAR) analog-to-digital converter (ADC). All input channels are simultaneously sampled to achieve a maximum throughput of 200 kSPS per channel. The device features a complete analog front-end (AFE) for each channel, including a programmable gain amplifier (PGA) with high input impedance of 1 MΩ, input clamp, low-pass filter, and an ADC input driver. This section provides details of the tests done. Refer to the product folders at http://www.ti.com/product/ADS8598S for more information.

Tests were done under the following conditions:

- Sampling rate and number of cycles captured: 256 samples per cycle for 5 cycles
- Input frequency: 50 Hz
- OSR : 0
- Interface: serial

The measurement accuracy for an input current range of 0.1 A to 125 A was less than ±0.1%. Accuracy was tested for ADC channel 4 and ADC channel 5, and the results were within ±0.1% for both of the channels. Detailed test results are provided in 表 56.

表 56. ADS8598S Measurement With ±10-V ADC Range

CURRENT (A)	ADC INPUT (mV)	ACI-5 (mV)	ACI-6 (mV)	ACI-5 (% ERROR)	ACI-6 (% ERROR)
0.10035	5.4914	5.494	5.49	0.054	-0.017
0.2003	10.9609	10.959	10.955	-0.019	-0.054
0.5003	27.3775	27.39	27.39	0.047	0.046
1	54.7222	54.715	54.749	-0.014	0.049
2.5	136.8056	136.886	136.885	0.058	0.058
5	273.6112	273.607	273.648	-0.002	0.013
10	547.2224	547.085	547.132	-0.025	-0.017
20	1094.4449	1094.662	1094.763	0.02	0.029
50	2736.1122	2734.931	2735.354	-0.043	-0.028
80	4377.7795	4378.214	4378.516	0.01	0.017
100	5472.2244	5474.075	5475.187	0.034	0.054
120	6566.6693	6570.111	6568.447	0.052	0.027
125	6840.2805	6838.087	6839.797	-0.032	-0.007
Minimum error				-0.043	-0.054
Maximum error				0.058	0.058

注: ADS8598H was tested as above and Similar measurement performance was observed

3.2.4.2 Test Results for ADS8588H

This section provides details of different performance tests and observations for the ADS8588H including accuracy and SNR performance with different OSR configurations.

3.2.4.2.1 Measurement Accuracy Testing

The ADS8588H device is an 8-channel, integrated data acquisition (DAQ) system based on a 16-bit successive approximation (SAR) analog-to-digital converter (ADC). All input channels are simultaneously sampled to achieve a maximum throughput of 500 kSPS per channel. The device features a complete analog front-end for each channel, including a programmable gain amplifier (PGA) with a high input impedance of 1 MΩ, an input clamp, low-pass filter, and an ADC input driver. This section provides details of the tests done. Refer to the product folders at http://www.ti.com/product/ADS8588H for more information.

Tests were done under the following conditions:

- Sampling rate and number of cycles captured: 256 sample per cycle for 5 cycles
- Input frequency: 50 Hz
- OSR: 0
- Interface: serial

The measurement accuracy for an input current range of 0.1 A to 125 A was less than ±0.25%. Accuracy was tested for ADC channel 4 and ADC channel 5, and the results were within ±0.25% for both of the channels. Detailed test results are provided in 表 57.

表 57. ADS8588H Measurement With ±10-V ADC Range

CURRENT (A)	ADC INPUT (mV)	ACI-5 (mV)	ACI-6 (mV)	ACI-5 (% ERROR)	ACI-6 (% ERROR)
0.10035	5.4914	5.485	5.482	-0.112	-0.175
0.2003	10.9609	10.963	10.97	0.022	0.081
0.5003	27.3775	27.384	27.395	0.023	0.065
1	54.7222	54.749	54.788	0.049	0.119
2.5	136.8056	137.027	136.961	0.162	0.114
5	273.6112	273.903	274.065	0.107	0.166
10	547.2224	547.441	547.771	0.04	0.1
20	1094.4449	1095.466	1096.093	0.093	0.151
50	2736.1122	2737.949	2739.645	0.067	0.129
80	4377.7795	4379.613	4382.236	0.042	0.102
100	5472.2244	5476.774	5480.198	0.083	0.146
120	6566.6693	6577.261	6577.257	0.161	0.161
125	6840.2805	6845.213	6849.696	0.072	0.138
Minimum error				-0.112	-0.175
Maximum error				0.162	0.166

注: Note: The accuracy was verified using the OPA2180, OPA2188 and OPA2171, and the performance was within the expected accuracy range for all amplifiers.

3.2.4.2.2 SNR Performance Testing With Different OSR Configurations

The ADS8588H device is an 8-channel, integrated data acquisition (DAQ) system based on a 16-bit successive approximation (SAR) analog-to-digital converter (ADC). All input channels are simultaneously sampled to achieve a maximum throughput of 500 kSPS per channel. In applications requiring higher SNR, ADS8588H with OSR programmed provided higher sampling rate with improved SNR. 表 58 summarizes the performance of the ADS8588H with a different OSR.

表 58. ADS8588H Performance With Varying OSR

TBD	TBD	TBD	TBD	TBD	TBD
Input voltage, RMS V	6.55	6.55	6.55	6.55	6.55
Input frequency Hz	1000	1000	1000	1000	1000 Hz
OSR	0, 500K	2, 260.42K	4,128.2K	8,63.6K	16, 31.65K
Sampling rate	500K	260.42K	128.2K	63.6K	31.65K
ENOB	14.93	15.042	15.089	15.097	15.127
SNR	91.72	92.43	92.86	93.457	93.942
THD	-108.1	-107.864	-108.86	-108.2	-108.7

注: Ground the negative input of the ADC for better performance.

3.2.4.3 Test Results for ADS8578S

The ADS8578S device is an 8-channel, integrated data acquisition (DAQ) system based on a 14-bit successive approximation (SAR) analog-to-digital converter (ADC). All input channels are simultaneously sampled to achieve a maximum throughput of 200 kSPS per channel. The device features a complete analog front-end for each channel, including a programmable gain amplifier (PGA) with high input impedance of 1 MΩ, input clamp, low-pass filter, and an ADC input driver. This section provides details of the tests done. Refer to the product folders at http://www.ti.com/product/ADS8578S for more information.

Tests were done under the following conditions:

- Sampling rate and number of cycles captured: 256 sample per cycle for 5 cycles
- Input frequency: 50 Hz
- OSR: 0
- Interface: serial

The measurement accuracy for an input current range of 0.1 A to 125 A was less than ±0.75%. Accuracy was tested for ADC channel 4 and ADC channel 5, and the results were within ±0.75% for both of the channels. Detailed test results are provided in 表 59.

表 59. ADS8578S Measurement With ±10-V ADC Range

CURRENT (A)	ADC INPUT (mV)	ACI-5 (mV)	ACI-6 (mV)	ACI-5 (% ERROR)	ACI-6 (% ERROR)
0.10035	5.4914	5.52	5.523	0.528	0.571
0.2003	10.9609	10.955	10.965	-0.05	0.036
0.5003	27.3775	27.251	27.311	-0.461	-0.245
1	54.7222	54.522	54.632	-0.366	-0.164
2.5	136.8056	136.377	136.614	-0.314	-0.14
5	273.6112	272.531	273.005	-0.395	-0.222
10	547.2224	544.68	545.62	-0.465	-0.293

表 59. ADS8578S Measurement With ±10-V ADC Range (continued)

CURRENT (A)	ADC INPUT (mV)	ACI-5 (mV)	ACI-6 (mV)	ACI-5 (% ERROR)	ACI-6 (% ERROR)
20	1094.4449	1089.684	1091.561	-0.435	-0.264
50	2736.1122	2726.247	2730.038	-0.361	-0.222
80	4377.7795	4359.421	4367.056	-0.419	-0.245
100	5472.2244	5445.562	5455.2	-0.487	-0.311
120	6566.6693	6538.846	6550.469	-0.424	-0.247
125	6840.2805	6815.437	6826.393	-0.363	-0.203
Minimum error				-0.487	-0.311
Maximum error				0.528	0.571

3.2.5 Reliability Testing

The ADS8588S has been tested for a number of reliability tests. A few of the tests are listed in the following tables with details of the tests and observations. Additional reliability tests have been performed. More details on the reliability tests and observations are available based on request.

3.2.5.1 EFT Testing With Class B Criteria

The following section provides details of the EFT tests that have been performed on the ADS858XS. The test setup for EFT testing is as follows:

1. EFT generator, for generating EFT pulses as per IEC61000-4-4 riding over 50-Hz mains input.
2. The EFT were connected to a potential transformer PT. The secondary of the PT was connected to the ADS8588S input through R (on both inputs) and C (across ADC) filter, and EFT pulses were applied simultaneously on multiple channels with low series protection resistance.
3. The SNR performance data was captured before applying EFT and after applying EFT.
4. The data was captured for two ADS858XS devices.
5. For the ADS858XS device, the channel which was stressed was CH1, CH3, CH4, CH5, and CH6.

表 60 provides details of the captured data.

表 60. ADS858XS EFT Testing Observations

TEST	DEVICE	STRESS LEVEL	BURST SIGNAL AMPLITUDE	BURST FREQUENCY	CHANNEL STRESSED	CHANNEL CAPTURED	AMPLITUDE (dBFs)	SNR
Pre EFT	1	NA	NA	NA	NA	1	-2.43	89.67
Pre EFT	1	NA	NA	NA	NA	2	-0.44	91.4
Post EFT	1	500 V	22.7 V	5 kHz	1	1	-2.43	89.75
Post EFT	1	500 V	22.7 V	5 kHz	1	2	-0.44	91.4
Post EFT	1	2 kV	90.9 V	5 kHz	1	1	-2.43	89.8
Post EFT	1	2 kV	90.9 V	5 kHz	1	2	-0.44	91.51
Post EFT	1	4 kV	181.8 V	5 kHz	1	1	-2.4	89.65
Post EFT	1	4 kV	181.8 V	5 kHz	3,4,5,6	1	-2.38	89.67
Post EFT	1	4 kV	181.8 V	5 kHz	1	2	-0.44	91.44
Post EFT	1	4 kV	181.8 V	5 kHz	3,4,5,6	2	-0.44	91.52

表 60. ADS858XS EFT Testing Observations (continued)

TEST	DEVICE	STRESS LEVEL	BURST SIGNAL AMPLITUDE	BURST FREQUENCY	CHANNEL STRESSED	CHANNEL CAPTURED	AMPLITUDE (dBFs)	SNR
Post EFT	1	4 kV	181.8 V	5 kHz	3,4,5,6	3	-0.44	91.13
Post EFT	1	4 kV	181.8 V	5 kHz	3,4,5,6	4	-0.44	91.2
Post EFT	1	4 kV	181.8 V	5 kHz	3,4,5,6	5	-0.44	91.1
Post EFT	1	4 kV	181.8 V	5 kHz	3,4,5,6	6	-0.44	91.47
Post EFT	1	5.5 kV	250 V	5 kHz	1	1	-2.38	89.91
Post EFT	1	5.5 kV	250 V	5 kHz	1	2	-0.44	91.29
Pre EFT	2	NA	NA	NA	NA	1	-2.38	89.88
Pre EFT	2	NA	NA	NA	NA	2	-0.44	91.24
Post EFT	2	2 kV	90.9 V	5 kHz	1	1	-2.38	89.87
Post EFT	2	2 kV	90.9 V	5 kHz	1	2	-0.44	91.14
Post EFT	2	4 kV	181.8 V	5 kHz	1	1	-2.38	89.73
Post EFT	2	4 kV	181.8 V	5 kHz	1	2	-0.44	91.11
Post EFT	2	4 kV	181.8 V	100 kHz	1	1	-2.37	89.61
Post EFT	2	4 kV	181.8 V	100 kHz	1	2	-0.44	91.51
Post EFT	2	5.5 kV	250 V	5 kHz	1	1	-2.37	89.78
Post EFT	2	5.5 kV	250 V	5 kHz	3,4,5,6	1	-2.37	89.87
Post EFT	2	5.5 kV	250 V	5 kHz	1	2	-0.44	91.29
Post EFT	2	5.5 kV	250 V	5 kHz	3,4,5,6	2	-0.44	91.39
Post EFT	2	5.5 kV	250 V	5 kHz	3,4,5,6	3	-0.44	91.49
Post EFT	2	5.5 kV	250 V	5 kHz	3,4,5,6	4	-0.44	91.26
Post EFT	2	5.5 kV	250 V	5 kHz	3,4,5,6	5	-0.44	91.5
Post EFT	2	5.5 kV	250 V	5 kHz	3,4,5,6	6	-0.44	91.66

Descriptions of the 表 60 columns are as follows:

- Performance Test: Data captured before EFT and post EFT
- Stress Level: Before transformer – EFT burst amplitude from the EFT generator (500 V, 2 kV, 4 kV, 5.5 kV)
- Burst Signal Amplitude: Riding on sine wave, EFT burst amplitude after transformer connected to system input (22.7 V, 90.9 V, 181.84 V, 250 V)
- Burst Frequency: From the EFT generator (5 kHz, 100 kHz)
- Channel Stressed: Channel on which the burst signal was applied

- Channel Captured: Channel on which performance data is captured
- Amplitude (dBFs): Measured signal amplitude
- SNR (dB): Measured SNR performance

3.2.5.2 Out of Range DC Input Voltage Stress Testing

The purpose of this test is to check the impact on adjacent channels when an out-of-range DC input voltage is applied on CH1 of the ADC. This section provides details of the test setup and performance with out-of-range DC input voltage applied. The setup includes:

1. High-voltage DC input applied for a minimum of 5 minutes for each setting.
2. The input structure for stressed ADC channel is an R (on both inputs) and C (across ADC) filter.
3. The stressed ADC channel is CH1.
4. The ADC CH2 SNR performance was captured after the voltage stress.
5. The captured data is available in 表 61.

表 61. High Voltage DC Input Test Observations

CH 1 DC VOLTAGE (V)	DC CURRENT (mA)	Dev1, CH 2 SNR at 0.3 dBFs	Dev2, CH 2 SNR at 0.3 dBFs
Float	0	92.33	92.33
1	0	92.16	92.16
5	0	92.27	92.27
11.4	0	92.2	92.2
21.8	0	92.16	92.16
30.1	0	92.4	92.4
40.5	0	92.21	92.21
50.9	0	92.31	92.31
61.3	0	92.21	92.21
75.9	0	92.3	92.3
90.4	0	92.3	92.3
100.9	5	92.27	92.27
125.8	7	92.12	92.12
150.8	8	92.2	92.2
175.7	9	92.18	92.18
200.7	10	92.02	92.02

Descriptions of the 表 61 columns are as follows:

- CH1 DC Voltage: Channel on which stressed DC voltage was applied.
- DC Current mA: The current drawn from the High Voltage DC source.
- CH 2 SNR at 0.3 dBFs: Measured SNR performance on adjacent CH 2.

注: Additional tests with four channels simultaneously stressed with lower series resistance values also did not impact the device performance.

3.2.5.3 Out-of-Range AC Signal Input Stress Test

The purpose of this test is to showcase the impact on adjacent channels when a stressed AC signal (V_{stress}) is applied on CH1 of the ADC. This section provides details of the test and performance with out-of-range AC input voltage applied. The test conditions are as follows:

1. Apply high-voltage AC (V_{stress}) to the driven channel.
2. Increase the amplitude and check FFT on adjacent channels.
3. Apply AC signal (Vs) on adjacent channel, where amplitude is ±9.39 V (18.76 Vpp) which is -0.5 dBFS.
4. All tests were done on the same EVM board, same RC components, and same GUI.

3.2.5.3.1 Performance Measurements and graphs for ADS8588S

This section provides details of the stress test performed on competition device. 表 62 provides the SNR and THD values for all the channels that were not stressed.

表 62. Measurements for ADS8588S ADC

	V_{stress} V_{pp}:	**30**	**34.9**	**36**	**37.8**	**42**	**48**	**60**
ADS8588S Unit2	**V_{stress} on CH1 (Amplitude)**	**±15.0 V**	**±17.44 V**	**±18 V**	**±18.9 V**	**±21.0 V**	**±24.0 V**	**±30.0 V**
CH2	SNR (dB)	91.7	91.6	91	87	84.2	83.2	83.1
	THD (dB)	-107.8	-108.9	-106.1	-102.3	-99.9	-97.4	-95.6
CH3	SNR (dB)	92.1	92.1	92.1	92.1	92	92	92.1
	THD (dB)	-110.7	-110.8	-110.9	-110.5	-110.7	-110.8	-109.7
CH4	SNR (dB)	92.3	92.2	92.2	92.2	92.1	92.1	92.1
	THD (dB)	-111.9	-110.4	-112.4	-111	-111.4	-111.9	-111.8
CH5	SNR (dB)	92.1	92.3	92.2	92.1	92.1	91.9	92.2
	THD (dB)	-109.8	-110	-111.2	-109.6	-109.6	-109.7	-110.4
CH6	SNR (dB)	92.2	91.9	92.3	92.1	92	92.1	92.1
	THD (dB)	-108.1	-109.2	-109.3	-108.5	-108.7	-108.2	-108.7
CH7	SNR (dB)	92.3	92.2	92.2	92.2	92.2	92.4	92.1
	THD (dB)	-110.2	-110.4	-110.1	-110.5	-110.1	-110	-110.5
CH8	SNR (dB)	92	92.1	92.2	92	92	92	92.1
	THD (dB)	-110.1	-110.2	-109.6	-110.2	-109.8	-110	-109.9

図 12 provides the plot for the ADS8588S SNR performance (D001_TIDUC09) for all of the channels that were not stressed and indicates the effect of the voltage stress on adjacent channels.

図 12. ADS8588S SNR Performance With Voltage Stress Applied

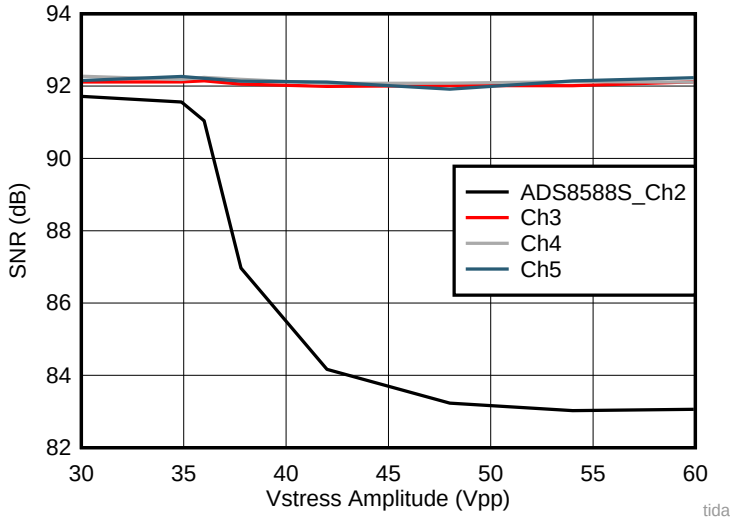
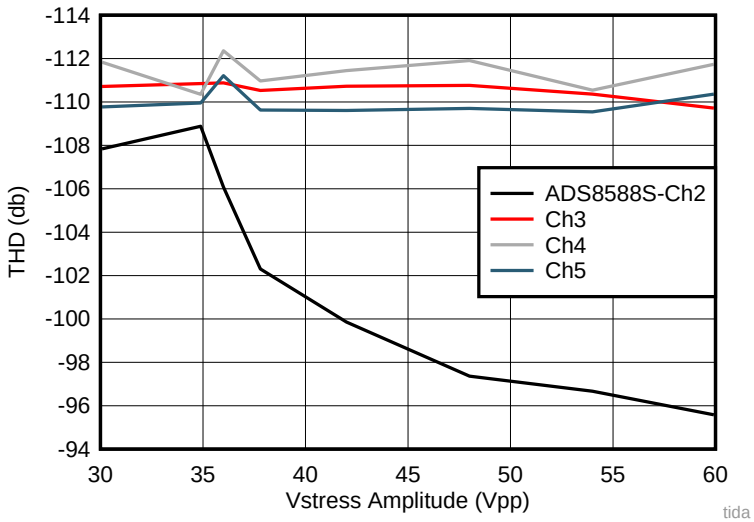


図 13 provides the plot for the ADS8588S THD performance (D003_TIDUC09) for all of the channels that were not stressed and indicates the effect of the voltage stress on adjacent channels.

図 13. ADS8588S THD Performance With Voltage Stress Applied



3.2.5.3.2 Miscellaneous Measurements and graph (using Competition Device)

This section provides details of the stress test performed on competition device. 表 63 provides the SNR and THD values for all of the channels that were not stressed.

表 63. Measurements for Competition ADC

	V_{stress} V_{pp}:	30	34.9	35.1	36	40	48	60
Competition Unit1	**V_{stress} on CH1 (Amplitude)**	**±15.0 V**	**±17.44 V**	**±17.55 V**	**±18.0 V**	**±20.0 V**	**±24.0 V**	**±30.0 V**
CH2	SNR (dB)	89.3	71.8	51	36	31.9	30.3	29.8
	THD (dB)	-103.5	-94.5	-74.5	-57.6	-50.2	-45.7	-44
CH3	SNR (dB)	89.2	88.1	71.6	56.7	52.2	50.7	50.4
	THD (dB)	-104.7	-103.5	-96.6	-78.6	-71.5	-67	-64.9
CH4	SNR (dB)	89.2	89.2	89.1	81.4	77.5	76.2	76.1
	THD (dB)	-105	-104.2	-104	-100.4	-94.6	-91.4	-89.3
CH5	SNR (dB)	89.2	89.1	89.2	88.1	86.5	85.1	85.8
	THD (dB)	-104.6	-104.2	-104.5	-104.3	-104.3	-102.7	-101.3
CH6	SNR (dB)	89.1	89.3	89.3	89.3	89.4	89.4	89.3
	THD (dB)	-105.2	-105	-105.7	-105.5	-104.7	-105.1	-105.7
CH7	SNR (dB)	89.3	89.1	89.3	89.4	89.3	89.2	89.4
	THD (dB)	-104.9	-104.7	-105.8	-105	-105.1	-105.3	-105.1
CH8	SNR (dB)	89.3	89.2	89.2	89	89.3	89.3	89.5
	THD (dB)	-104.5	-103.9	-105.2	-105.1	-104	-104.3	-104.4

図 14 provides the plot for SNR performance (D002_TIDUC09) for all of the channels that were not stressed and indicates the effect of the voltage stress on adjacent channels.

図 14. ADC SNR Performance With Voltage Stress Applied

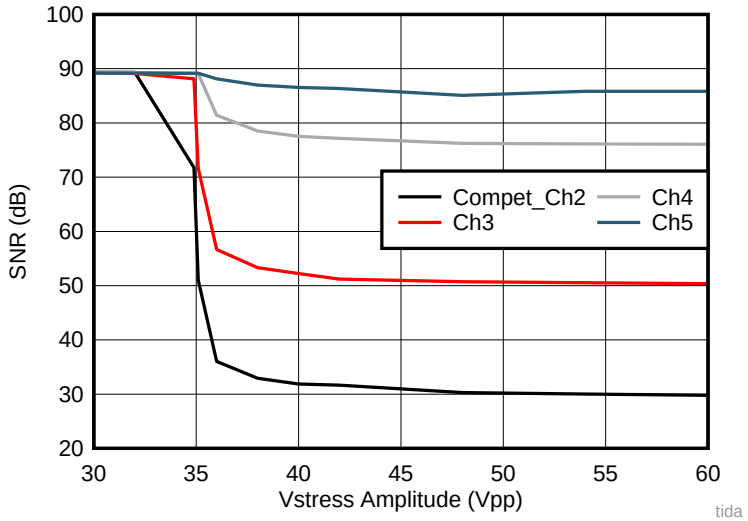
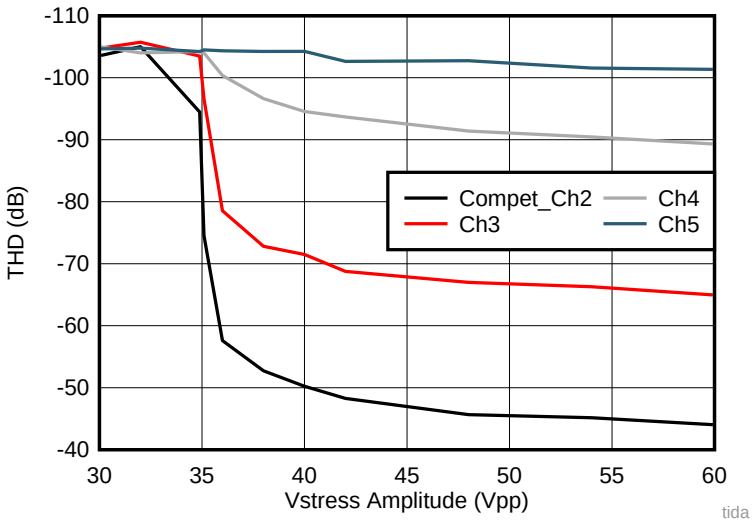


図 15 provides the plot for THD performance (D004_TIDUC09) for all of the channels that were not stressed and indicates the effect of the voltage stress on adjacent channels.

図 15. ADC THD Performance With Voltage Stress Applied



3.2.6 ISO224 Isolation Amplifier Performance Testing

The ISO224 is a precision isolation amplifier with an output separated from the input circuitry by a silicon dioxide (SiO2) barrier that is highly resistant to magnetic interference. This barrier has been certified to provide basic galvanic isolation of up to 7000 V_{PEAK} according to UL1577 and IEC60747-5-2 specifications. The input of the ISO224 is optimized for accurate sensing of ±10-V signals that are widely used in industrial applications. The ISO224 operates on a single 5-V power supply on the high-side which dramatically simplifies the design of the isolated power supply which reduces overall system costs.

3.2.6.1 ISO224 Isolation Amplifier Interfaced to ADS8588H Performance

The ADS8588S ADC is used in applications with ±10-V input. When isolation is required for the inputs, TI provides isolation amplifier solutions ISO224 which can directly measure this ±10-V input, simplifying the system design. The ISO224 is a precision isolation amplifier with an output separated from the input circuitry by a silicon dioxide (SiO2) barrier that is highly resistant to magnetic interference. This barrier has been certified to provide basic galvanic isolation of up to 7000 V_{PEAK} according to UL1577 and IEC60747-5-2 specifications. The input of the ISO224 is optimized for accurate sensing of ±10-V signals that are widely used in industrial applications. The ISO224 operates on a single 5-V power supply on the high-side which dramatically simplifies the design of the isolated power supply which reduces overall system costs. The performance was tested using the ISO224 evaluation module. Refer to the product folders at http://www.ti.com/tool/iso224evm

The analog output from the ISO224 is a fully-differential signal centered at VDD2/2. Two differential- to single-ended output options are also included. U4 provides a bi-polar output signal and the output of U4 is interfaced to ADS8588H with a ±10-V input for testing. Power supply up to ±15 for U4 is provided via three-terminal screw connector J5. Testing was done with a number of op-amp families and the performance is summarized in 表 64.

表 64. Isolation Amplifier ISO224 Performance Testing With Different Op-Amps

PARAMETERS	APPLIED AC INPUT	OPA277	OPA188	OPA180	OPA171
AC voltage, 1000 Hz	6.746	6.653	6.652	6.655	6.656
AC voltage, 50 Hz	6.746	6.633	6.632	6.635	6.636
AC voltage, 1000 Hz	3.42	3.374	3.374	3.375	3.375
ENOB	Bits	13.65	13.41	13.68	13.71
SNR	dB	86.78	86.74	87.3	87.1
THD	dB	-87.5	-87.5	-87.3	-87.52

3.2.6.2 High-Side Supply Voltage Detection

The integrated high-side supply voltage detection feature simplifies system level diagnostics The ISO224 offers a fail-safe output that simplifies diagnostics on system level. The fail-safe output is active when the high-side power supply VDD1 of the device is missing, independent of the input signal at the IN pin. When power supply VDD1 of the device is missing both outputs, OUTP and OUTN, of the device are actively driven close to GND2.

3.2.7 ADC Input Protection Against Surge and Overvoltage Using Flat Clamp

The ADS8588S, ADS8598S, and other devices in the 16-bit, 8-channel, simultaneous-sampling SAR ADC family have a continuous maximum rating of ±15 and are connected to sensors placed in harsh environments. A flat clamp TVS TVS1400 or TVS1401 connected at the input protects the ADC from these transients. Refer to the product folders at http://www.ti.com/interface/circuit-protection/esd-protection-and-tvs-surge-diodes/overview.html and refer to the Flat-clamp TVS based reference design for protection against transient for grid applications for more details.

3.2.8 Summary

表 65 provides a summary of the tests that have been performed for the DAQ AFE and the observations of the tests performed

表 65. Test Results Summary for DAQ Front End

SERIAL NUMBER	PARAMETERS	OBSERVATION
1	±15-V DC-DC converter output	OK
2	±5-V DC-DC with LDO output	OK
3	+13-V, –13-V, +5-V, +3.3-V LDO output	OK
4	Isolated power DC-DC and LDO output	OK
5	±12.2-V dual LDO output	OK
6	Reference output	OK
7	ZCD comparator output for different voltage outputs	OK
8	ADS8588S ADC interface with GUI with parallel or serial interface	OK
9	Current measurement with instrumentation amplifier	OK
10	Current measurement with precision op amp	OK
11	Voltage measurement with potential divider and op amp	OK
12	Voltage measurement with potential divider, isolation amplifier and differential op amp	OK
13	Measurement accuracy with ±10-V and ±5-V input ranges configured	OK
14	Measurement accuracy with different sampling rates configured 80, 256, 512, 1024 samples per cycle	OK
15	Measurement accuracy with reference configured for internal or reference	OK
16	Measurement accuracy with 1, 3, or 5 cycles of sample value capture	OK

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-00834.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00834.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00834.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-00834.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00834.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00834.

5 Related Documentation

1. Texas Instruments, *ADS8588S evaluation module*, ADS8588EVM-PDK Tool Folder (http://www.ti.com/tool/ads8588sevm-pdk)
2. Texas Instruments, *High-accuracy AC current measurement reference design using PCB Rogowski coil sensor*
3. Texas Instruments, *Shunt-based, 200-A peak current measurement reference design using reinforced isolation amplifier*
4. Texas Instruments, *Flat-clamp TVS based reference design for protection against transients*
5. Texas Instruments, *Moving from conventional to intelligent substations white paper*
6. Texas Instruments, *Interfacing multiple ADCs to a single processor for grid protection and control*

5.1 商標

6 Terminology

AFE— Analog front end

CT— Current transformer

DAQ— Data acquisition

INA— Instrumentation amplifier

OPA— Operational precision amplifier

PD— Potential divider

PHI— Precision host interface

ZCD— Zero-cross detector

7 About the Authors

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改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (September 2017) から **Revision B** に変更 **Page**

- ドキュメントのタイトル 変更 1
- 「概要」の情報 変更 1
- 「特長」の情報 変更 1
- 「リソース」に ADS8588H、ADS8598S、INA821、ISO224A、ISO224B、OPA2180、OPA2277、AMC1200、AMC1300、AMC1300B、LM5017、LM5160、SN6505B、SN6501 を 追加 1
- information in 表 1 変更 3
- information regarding the interface connector to 2.2 追加 4
- information regarding the OPA2171 to 2.8.2.2 追加 14
- 2.8.3.2 title from *Measurement With Precision Op Amp OPA2188 or OPA2180 and Isolation Amplifier AMC1301* to *Measurement With Precision Op Amp OPA2188 and Isolation Amplifier AMC1301 or ISO224* 変更 15
- information regarding the ISO224 to 2.8.3.2 追加 16
- information regarding the SN6501 and SN6505B to 2.8.4.1 and 2.8.4.2 追加 19
- information regarding the SN6501 to 2.8.4.7 追加 21
- 表 8 title from *Precision Instrumentation Selection for DAQ Front End* to *Instrumentation Selection for DAQ Front End* 変更 24
- information to 表 8 追加 24
- TMP235 and HDC2010 to 2.8.6.5 追加 24
- TIDA-020018 and 表 9 to 2.8.6.8 追加 25
- 2.8.6.9 追加 26
- information to 表 54 追加 51
- 3.2.4 追加 52
- list items 4, 5, and 6 to 5 追加 65

2017年1月発行のものから更新 **Page**

- 現行のデザイン・ガイドのテンプレートに合わせてレイアウトを 変更 1
- 14-bit option of ADC in *Table 1: Key System Specifications* 追加 3
- Updated *Figure 1: Block Diagram of DAQ Front End With Isolation and Dual LDO* 8
- Section 2.8.4.2 title from *DC-DC Converter for ±5-V LM27762* to *Inverter and LDO for ±5-V Using LM27762* 変更 19
- *Section 2.8.4.3: Dual LDO for ±12-V DC Output Using TPS7A39* 追加 19
- Dual LDO output info to *Table 25: AFE Functional Testing for Power Supply and Reference* 追加 37
- *Section 4.3: Performance Testing With Other ADS85XXS Family Devices* 追加 51

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