参考資料

TI Designs
シャントおよび電圧測定を使用する、入力電圧範囲の広い保護リレーのリファレンス・デザイン

TEXAS INSTRUMENTS

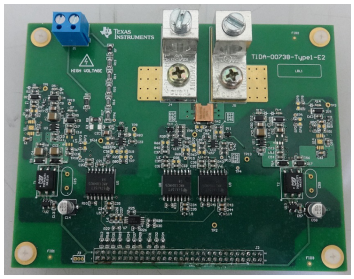
デザイン概要

このTI Designは、AMC1304M05絶縁デルタ-シグマ(ΔΣ)変調器による、値の低い4線式の、既製のシャント測定を使用して、入力電流の測定範囲を拡大する独自の手法を示しています。このデザインでは、AMC1304M25絶縁ΔΣ変調器を使用した広い入力電圧範囲の測定についても示しています。消費電力を最小にする小さい値のシャントを注意深く選択し、低ノイズのフロントエンド・アンプを選択し、2つのゲイン・パスを導入することで、電流範囲を0.1 In(公称電流)から、40 In (または60 In)に拡大できます。このデザインでは、変調器の出力をAM437xホスト・プロセッサに接続し、必要なSinc3フィルタ処理を行うことで、電流と電圧の両方の測定について±0.5%未満の精度を実現しています。必要な絶縁電源は、変圧器ドライバとLDOを使用してオンボードで生成されます。

設計リソース

TIDA-00738	デザイン・ファイルを含むツール・フォルダ
AMC1304M05	プロダクト・フォルダ
AMC1304M25	プロダクト・フォルダ
TPS7A3001	プロダクト・フォルダ
SN6501	プロダクト・フォルダ
TLV70450DBV	プロダクト・フォルダ
TPS70925DRV	プロダクト・フォルダ
OPA188	プロダクト・フォルダ
CDCLVC1104	プロダクト・フォルダ
AM437x 産業用開発キット	ツール・フォルダ

TI E2E™ Community　E2Eエキスパートに質問

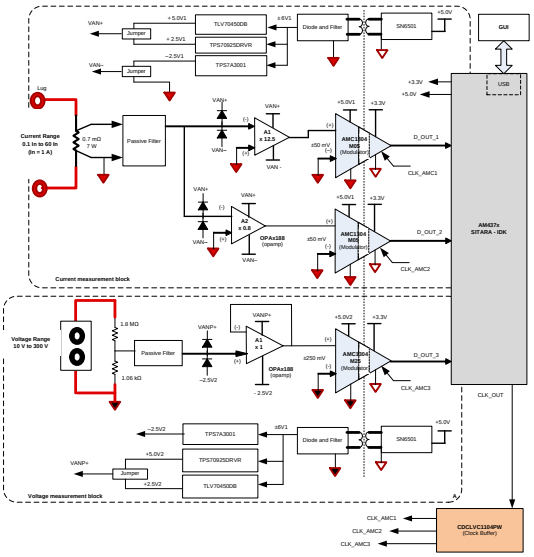


デザインの特長

- 絶縁ΔΣ変調器(AMC1304M05)を使用する単相電流測定(シャントをベースとする)と、AMC1304M25を使用する電圧測定
- 測定精度:
  - AC電流: In = 1Aで、0.1A～40A (または60A)について±0.5%未満
  - AC電圧: 5V～350Vについて±0.5%未満
- ホストMCU (TI製のAM437x Sitara™ ARM® Cortex®-A9プロセッサ)とAFE接続し、PRU-ICSSを使用してSinc3デジタル・フィルタ処理を実行
- クロック・バッファを使用して、単一のマスタ・クロック(AM437xから供給)から複数の変調器用のクロック入力を生成
- 変圧器ドライバとLDOを使用して、AMC1304Mx5およびOPA188用のオンボードの絶縁±2.5Vおよび+5.0V電源を生成
- 電流および電圧のサンプルをキャプチャし、分析(パラメータおよび波形)を行うためのGUI
- 5Aアプリケーション用に構成可能(シャント値とゲイン抵抗の変更による)
- 小さい値の4線式シャント(0.7mΩ、7W)により、0.1A～40A (または60A)で動作するように設計され、消費電力を最小化(60Aで約2.5VA)

主なアプリケーション

- 保護リレーおよびIED



1 System Description

Grid infrastructure applications cover the protection, control and monitoring of systems that generate, transmit and distribute power. Some of the applications include multifunction protection relays, transformer monitoring, motor monitoring, power quality analyzers, and so forth. These systems can be rack-mounted (AC mains operated) or portable (battery operated). The portable systems require separate, galvanically-isolated channels for measuring input voltages and currents.

1.1 Protection Relays

The function of protection relays is to provide protection to grid equipment during fault conditions by measuring multiple voltages and currents. Protection relays measure signals from current transformers (CTs) and voltage transformers (VTs). If the relays detect a stressed condition, a trip signal is sent to the circuit breaker to disconnect the faulty components from the power system. Protection relays are categorized based on the equipment type protected, such as generators, transmission lines, transformers, and feeders. A protection relay typically has the following functional blocks:

- Analog front end for measuring inputs from CT and VT
- Local controller or a processor for processing the measured signals
- Digital, analog input, or analog output
- Mains or auxiliary power supply
- Communication boards
- Central processing unit (CPU)

1.2 Current Measurement in Protection Relays

Protection relays measure wide input currents (within a specified accuracy). The current range depends on the manufacturers and target functionality. Commonly specified ranges include:

- 0.1 A to 40 A (up to 60 A) for a 1-A nominal current
- 0.5 A to 200 A (up to 300 A) for a 5-A nominal current

Sensors for measuring current input include CTs, Rogowski coils, and shunts. The type of sensor selected for a given application depends on the following requirements:

- Measurement accuracy at 50- or 60-Hz input
- Linearity and phase shift
- Saturation
- Safety (isolation)
- Electromagnetic compatibility (EMC) performance
- Cost, size, and reliability

1.2.1 Comparison of Current Sensing Options

表 1 compares the commonly used transducers.

表 1. Current Sensors Comparison

CURRENT SENSOR TYPE	ADVANTAGES	DISADVANTAGES
CT	• Provides galvanic isolation from the primary circuit • Accurate over defined range of current input • Low power loss • Not affected by common-mode noise input	• Tend to be bulky and expensive (depends on accuracy and current level requirements) • Requires more board area • External magnetic fields and frequent overloads affect the performance and reduce the usable life of CTs
Rogowski coil	• Provides galvanic isolation from the primary circuit • Does not saturate (wide dynamic range) and no magnetizing current error because of non-magnetic core • Linear and not affected by DC • Electrically safe when open • Very low primary burden • Potential for lower cost • Smaller in size and weighs less in comparison to CT	• Has lower sensitivity • Lower temperature stability • Needs integrator (hardware or software) • Low frequency noise is magnified • Sensitive to position of the primary current conductor carrying • Limited external magnetic field immunity • Manufacturing tolerance is high
Shunt	• Can measure AC and DC with high accuracy • Is linear over measurement range • Does not have current saturation problem as CT • Lower cost and smaller size	• Does not provide isolation • Amplification or attenuation required at output • Has DC offset problem • VA loss (power consumption) depends on shunt value

The lost cost of a shunt and its performance advantages make it an attractive option for use in next-generation protection relays.

1.3 Migration From CT to Shunt

Traditionally, current transformers have been used for protection. A shunt (such as Manganin®) can be used along with an isolated delta-sigma (ΔΣ) modulator to replace a CT as a more accurate and less expensive option for measuring current and voltage. A ΔΣ modulator converts an analog input signal into a high-frequency stream of single bits without off-band noise. The advantage of moving the quantization noise to higher frequency bands include simpler anti-aliasing filtering, a low-cost solution by eliminating the cost of drivers, filters, and a scalable performance.

The AMC1304Mx5 isolated ΔΣ modulator has been designed to connect directly to a current shunt and also has a galvanic isolation barrier. The AMC1304Mx5 modulator is a second-order ΔΣ modulator with reinforced isolation. The device has two variants that accept ±50- and ±250-mV inputs. In this design, a narrow-input range device is used to measure current and a wide-input range device is used to measure voltage. Limiting the input voltage range for current measurement to ±50 mV significantly reduces the power dissipation in a shunt.

1.4 Isolated Current Measurement Using Shunt

The isolation between the input side (shunt) and the output side (host) can be achieved using any of the following approaches.

- Analog Isolators: An *Isolation amplifier* provides isolation and an analog output that is proportional to the input. This isolated analog output is fed to the input of the ADC.
- Digital Isolators: The output of the shunt is converted to a digital code using an analog-to-digital converter (ADC). The output of the ADC is then isolated using a *digital isolator*.

Each implementation has a different set of pros and cons and must be carefully analyzed depending on the application.

This design focuses on extending the input current measurement range using isolated ΔΣ modulators. Even though a common practice is to gain the input signal to match the wider input range of an ADC, a lower ADC input range is a preferred option when using shunts because this option reduces dissipation. A ΔΣ modulator with a ±50-mV input range reduces the required shunt value and results in reduced power dissipation. To achieve the expected accuracy and to cover a wide current range, this design uses two modulators.

1.5 Isolated Voltage Measurement

The secondary voltage is measured using a potential divider (multiple series resistors). Using a potential divider reduces the board size and improves linearity performance. In many applications, protection relays are specified to have channel-to-channel isolation for analog input measurement. Isolation can be provided for the voltage input using isolated ΔΣ modulators. A potential divider is typically > 1 MΩ. Because the input impedance is high, a ±250-mV device can be used. A higher impedance voltage divider introduces additional errors during measurement. Reduce this error by providing an op amp buffer stage before the modulator.

1.6 Host Interface

The ΔΣ modulator output interfaces to a host processor for performing Sinc3 filtering of the modulator data output. The AM437x industrial development kit (IDK) interfaces to the modulator for filtering and oversampling. The AM437x IDK features a 1-GHz Texas Instruments (TI) AM437x Sitara™ ARM® CORTEX A9 processor that can be used for implementing additional functionalities, including communication and supporting protocols such as IEC61850, which is required for protection relays.

2 Shunt-Based Isolated Current Measurement

To cover a wide range of current input starting from 0.1 A to 40 A (or 60 A) for a 1-A nominal current (In), choosing an adequate shunt value is critical. Shunt values are specified in mΩ. Using a 7-mΩ shunt for a 0.1-A input, the voltage drop is 0.7-mV RMS, which is an approximate 2% input for a ±50-mV modulator. The modulator is specified to measure input accurately from 0.7 mV to 35 mV. At 60 A the power dissipation for a 7-mΩ shunt is 25 W. Use a lower value shunt with a front end amplifier to reduce the power dissipation. A lower value shunt with an amplifier eliminates the requirement for a multi-tap shunt. To cover a wide input range, one of the modulator inputs can have a higher amplification and the other modulator input can have a lower amplification to cover the wide current input range.

2.1 TI Design Advantage and Implementation

The TIDA-00738 TI Design has a provision to measure a single-phase input (one current and one voltage input). The current and voltage inputs provide the following isolation: channel-to-channel isolation and input-to-output isolation.

This design measures a wide current input using two ±50-mV modulators. One of the modulators measures current from 0.1 A to 4 A and the second modulator measures current from 4 A to 40 A (or 60 A). The design utilizes a standard, off-the-shelf 0.7-mΩ shunt. An inverting amplifier is used across the shunt to provide the required amplification. The design also implements an op amp with low offset and low biasing current. The output of the amplifier is connected to the ΔΣ modulators. The output of the modulators interface to the AM437X IDK. A graphical user interface (GUI) is used to perform the measurement.

The following subsections outline the implementation of voltage and current measurement.

2.1.1 Voltage Measurement

A voltage up to 300 V can be applied to the board without an external potential transformer (PT). The voltage inputs are attenuated by the onboard potential dividers and demonstrate the following functionality in 表 2.

表 2. Voltage Measurement

FUNCTIONALITY	SUMMARY
Voltage input providing input-to-output isolation and channel-to-channel isolation	• One voltage input with a range of 10- to 300-V AC • A potential divider (voltage divider) using multiple resistors • A ΔΣ modulator with a ±250-mV input is used to sample the input voltage • An op amp in a buffer configuration is used to reduce errors caused by an impedance mismatch • The output of the modulator interfaces to the AM437X IDK for Sinc3 filtering of the modulator bit-stream data
Power supply	• A transformer driver is used to generate the isolated power supply • Low dropout voltage (LDO) regulators are used to generate the required positive and negative supplies

2.1.2 Current Measurement

The current inputs are applied across the onboard shunt and demonstrate the following functionality in 表 3.

表 3. Current Measurement

FUNCTIONALITY	SUMMARY
Current input providing input-to-output and channel-to-channel isolation	• Two ΔΣ modulators with a ±50-mV input are used for sampling the input current • One modulator is used to measure the lower current from 0.1 A to 4.0 A with a gain stage of ≥ 12.5 • A second modulator is used to measure the higher current from 2 A to 40 A (or 60 A) with a gain stage of ≤ 0.8 • A four-terminal, 0.7-mΩ, 7-W shunt is used to sense the input current • The output of the modulators interface to the AM437X IDK for Sinc3 filtering of the modulator bit-stream data • Aluminum lugs have been provided to connect the current to the analog front end (AFE)
Power supply	• A transformer driver is used to generate the isolated power supply • LDOs are used to generate the required positive and negative supplies • The same power supplies connect to both modulators

3 Key System Specifications

表 4. AFE Specifications

PARAMETERS	SPECIFICATIONS AND FEATURES
Measurement parameters	Single-phase (one) current input
	Current range: 0.1- to 40-A (or 60-A) AC for accuracy performance
	Single-phase (one) voltage input
	Voltage range: 10- to 300-V AC for accuracy performance
	Input type: AC or DC input
	Frequency: 50 Hz or 60 Hz
Measurement accuracy	< ±0.5% for voltage and current
OSR and filter	128, Sinc3
Host interface connector	60-pin, 2.54-mm pitch
Host	AM437x IDK; Sinc3 digital filters on TI AM437x Sitara™ ARM® Cortex®-A9 processor using Programmable Real-Time Unit Subsystem (PRU-ICSS)
Power supply	Input supply of 5 V and +3.3 V through interface connector
	Isolated supply of 5 V and ±2.5 V derived from 5 V using a transformer driver and LDOs
Input clock for modulators	5-MHz clock from AM437x IDK with an onboard 1:4 clock buffer

注: The input current range depends on the shunt value used.

4 Block Diagram

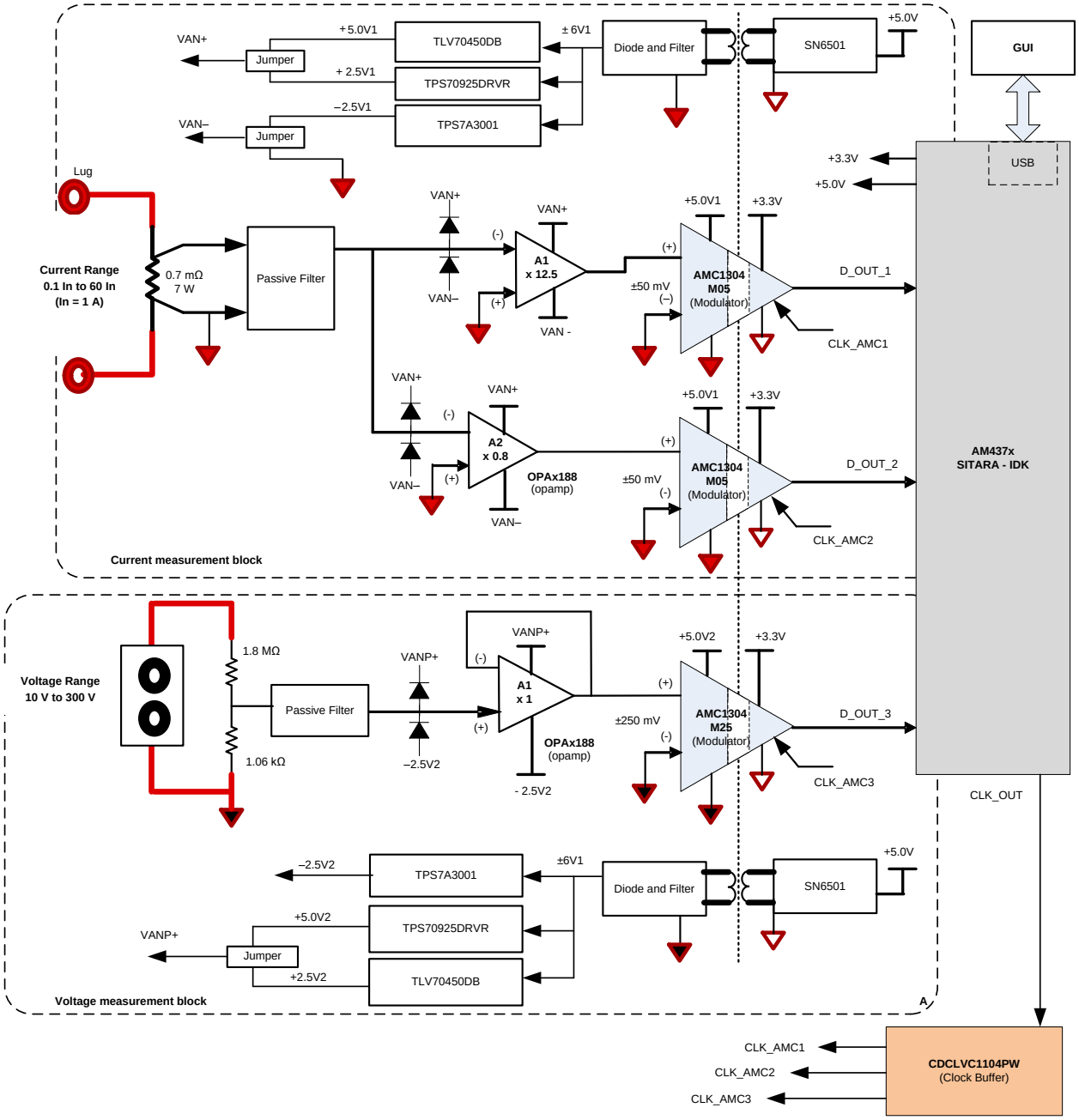


図 1. TIDA-00738 Block Diagram

This design showcases the use of an AMC1304Mx5 ΔΣ modulator for isolated current and voltage measurement. These modulators interface to an AM437x Sitara ARM Cortex-A9 processor for demodulation using a PRU-ICSS-implemented Sinc3 filter.

This design provides the ability to measure one current input and one voltage input.

The firmware is used to configure the Sinc3 filters, set the modulator frequency, and receive data from the Sinc3 filters. The design also provides a run-time GUI to help the user validate the AMC1304Mx5 performance and supports configuration changes to Sinc3 filter parameters in the AM437X IDK. 6 describes the implementation of the current and voltage measurement system.

5 Highlighted Products

5.1 AMC1304M05/AMC1304M25 (ΔΣ) Modulator

The AMC1304Mx5 is a precision, ΔΣ modulator with a capacitive double isolation barrier that is highly resistant to magnetic interference. The modulators are used in this design to measure voltage and current. The modulator provides the required isolation between the input and the output. A ±50-mV modulator is used for current measurement and a ±250-mV modulator is used for voltage measurement.

The input of the AMC1304Mx5 device has been optimized for a direct connection to a shunt or other low-voltage signal sources. The unique low-input voltage range of the ±50-mV device allows for a significant reduction of the power dissipation through the shunt while supporting excellent AC and DC performance. By using an appropriate digital filter to decimate the bit stream, the device can achieve 16 bits of resolution with a dynamic range of 81 dB or a 13.2 effective number of bits (ENOB) at a data rate of 78 kSPS.

On the high side, an integrated LDO regulator supplies the modulator, which allows an unregulated input voltage between 4 V and 18 V (LDOIN). The isolated digital interface operates from a 3.3- or 5-V power supply (DVDD).

Features:

- Pin-compatible family optimized for shunt-resistor-based current measurements:
  - ±50- or ±250-mV input voltage ranges
  - Complementary metal-oxide semiconductor (CMOS) or low-voltage differential-signaling (LVDS) digital interface options
- Excellent DC performance supporting high-precision sensing on system level:
  - Offset error: ±50 µV (max) or ±100 µV (max)
  - Offset drift: 1.3 µV/°C (max)
  - Gain error: ±0.2% (max) or ±0.3% (max)
  - Gain drift: ±40 ppm/°C (max)

For more details on this device and related documents, consult the AMC1304M05 product page at: http://www.ti.com/product/amc1304m05.

注: Depending on the application requirement, the AMC1305M05 or AMC1305M25 can also be used for this design.

5.2 OPA188AIDBVR Operational Amplifier (Op Amp)

In protection relays, the input current rating is 1 A or 5 A. For a 1-A CT input, the current from 0.1 A to 40 A (or 60 A) must be measured accurately, which requires more than one modulator. The power dissipation across the shunt is also a concern when a wide range of current input requires measuring. To reduce shunt dissipation, an amplifier can be used before the modulator and a smaller shunt value can be used. The OPA188 op amp, which has a low-offset voltage and zero drift, has been selected for this application.

This miniature, high-precision, low-quiescent amplifier offers high input impedance and a rail-to-rail output swing within 15 mV of the rails. The input common-mode range includes the negative rail. Either single or dual supplies can be used in the range of 4 V to 36 V (or ±2 V to ±18 V).

For more details on this device and related documents, consult the OPA188 product page at: http://www.ti.com/product/opa188.

5.3 CDCLVC1104PW

The host processor generates one clock output that can be used as a clock input for the ΔΣ modulators. When implementing multiple modulators, a clock buffer is used to generate the required clock outputs. The clock output of the host processor is buffered to avoid loading. This design uses two modulators for current and one modulator for voltage. A 1:4 clock buffer has also been used.

The CDCLVC11xx is a modular, high-performance, low-skew, general-purpose clock buffer. All family members share the same high-performance characteristics such as low additive jitter, low skew, and wide operating temperature range. The CDCLVC11xx supports an asynchronous output enable control (1G), which switches the outputs into a low state when the 1G is low.

For more details on this device and related documents, consult the CDCLVC1104 product page at: http://www.ti.com/product/cdclvc1104.

5.4 Isolated Power

AMC1304Mx5 modulators provide the required signal isolation. The modulators and amplifiers must be powered by an isolated power supply. The required isolated power supply is generated by using a transformer driver and LDOs. An SN6501 device provides the simplest solution to generate the isolated power supply.

5.4.1 SN6501DBVR

The TIDA-00738 design uses the SN6501 to generate the required isolated power supplies for voltage and currents. The design utilizes two SN6501 devices, one to drive the voltage input and one to drive the current input.

The SN6501 is a monolithic oscillator or power-driver that has been specifically designed for small form factor, isolated power supplies in isolated interface applications. The device drives a low-profile, center-tapped transformer primary from a 3.3- or 5-V DC power supply. The secondary can be wound to provide any isolated voltage based on the transformer turns ratio.

The SN6501 consists of an oscillator followed by a gate drive circuit, which provides the complementary output signals to drive the ground referenced N-channel power switches. The internal logic ensures that a break-before-make action occurs between the two switches.

For more details on this device and related documents, consult the SN6501 product page at: http://www.ti.com/product/sn6501.

5.4.2 TPS7A3001DGNR

The TPS7A3001 is a negative, high-voltage (–36 V), ultralow-noise (15.1 μV_{RMS}, 72-dB power supply rejection ratio (PSRR)) linear regulator capable of sourcing a maximum load of 200 mA. These linear regulators include a CMOS logic-level compatible enable pin and capacitor.

For more details on this device and related documents, consult the TPS7A30 product page at: http://www.ti.com/product/tps7a30.

5.4.3 TLV70450DBVR

For more details on this device and related documents, consult the TLV704 product page at: http://www.ti.com/product/tlv704.

5.4.4 TPS70925DRV

For more details on this device and related documents, consult the TPS709 product page at: http://www.ti.com/product/tps709.

5.5 Sitara AM437x Processor

The Sitara AM437x processor family is based on the powerful ARM Cortex-A9 Core. 図 2 shows the block diagram of the processor and integrated peripherals. This processor integrates a quad-core programmable real-time unit (PRU), which has been designed to implement deterministic, real-time processing of industrial communication protocols such as EtherCAT, PROFIBUS, and position encoder interfaces like EnDat2.2, BiSS, and ΔΣ demodulator interfaces. This make AM437x processors ideal for industrial communications, industrial control, and industrial drives applications. The processor has a rich peripheral set for industrial interfaces, motor control, graphics, and security. The device can boot from various sources including QSPI and NAND. The JTAG interfaces all cores including PRUs and the PRU can be debugged using the Code Composer Studio™ (CCS) software from Texas Instruments (TI). Parallel debug of ARM and PRUs is supported. The reference document for AM437x can be found at http://www.ti.com/product/AM4379.

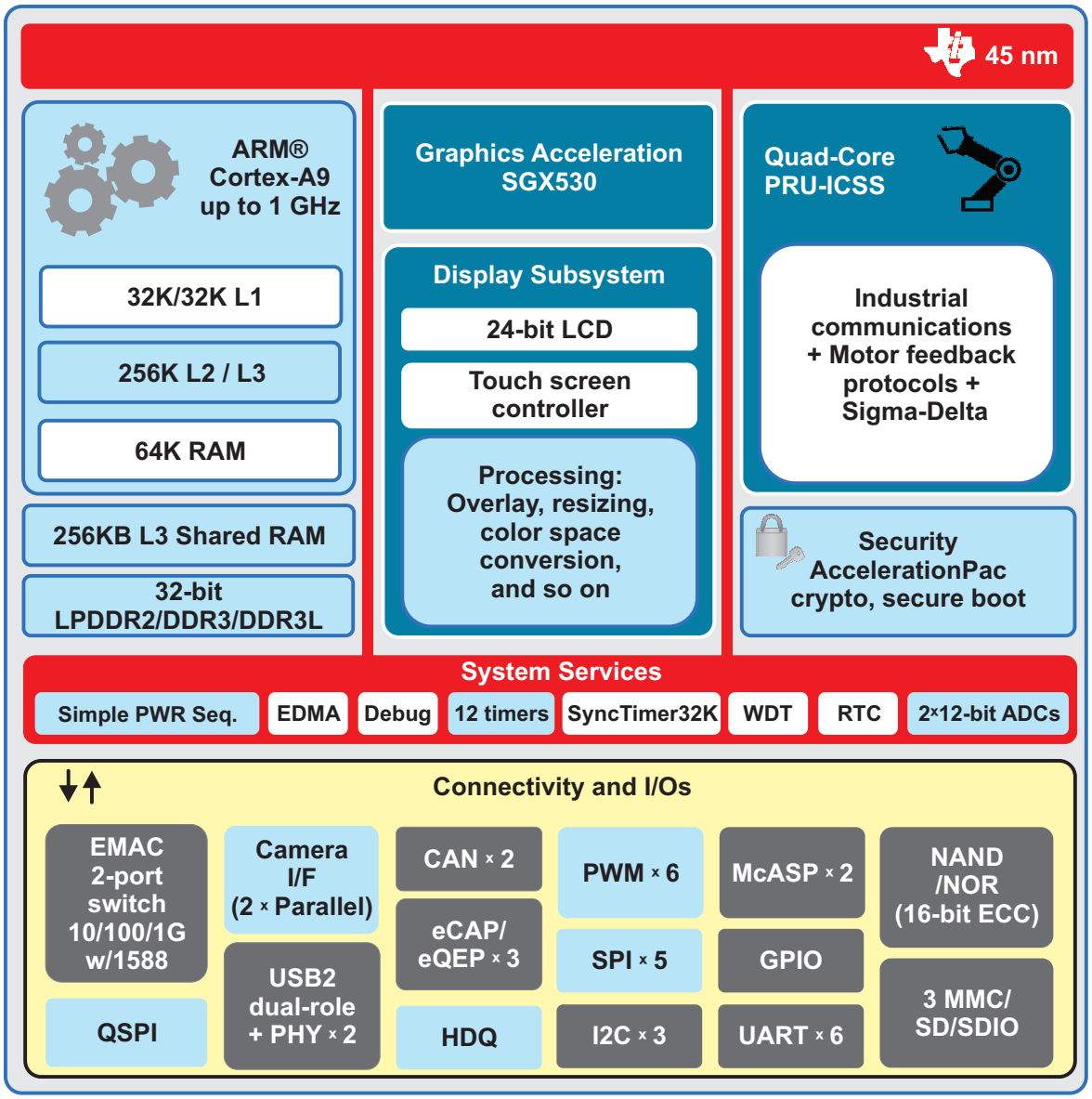


図 2. AM437x Functional Block Diagram

5.5.1 PRU-ICSS

The programmable real-time unit (PRU-ICSS) is a separate processing unit from the ARM core. The PRU can operate independent of the ARM core after initialization. Also, the PRU is clocked independently for greater efficiency and flexibility and can be used for offloading tasks from ARM. Alternatively, the PRU-ICSS can be used to implement additional peripheral interfaces and real-time protocols such as EtherCAT, PROFINET, EtherNet/IP, PROFIBUS, Ethernet Powerlink, Sercos3, EnDat2.2, and ΔΣ de-modulator. The PRU core runs at a 200-MHz frequency and each PRU instruction takes 5 ns to execute. This feature makes the PRU perfect for implementing real-time communication and control systems. Each PRU core has its own instruction and data memory, has access to all parts of a system-on-chip (SoC), has access to all pins, and can talk to all memories and I/Os except the ARM CPU memory, interrupt ARM, and receive events from ARM. The PRU can interact with other processors as defined by the firmware loaded into instruction memory. Two ICSS blocks (each with two PRU cores), namely ICSS0 and ICSS1, are available for industrial Ethernet and motor-side communication. The block diagram of both PRUs is shown in 図 3. For more details on PRU-ICSS, refer to the *AM437x ARM Cortex-A9 Processors Technical Reference Manual*.

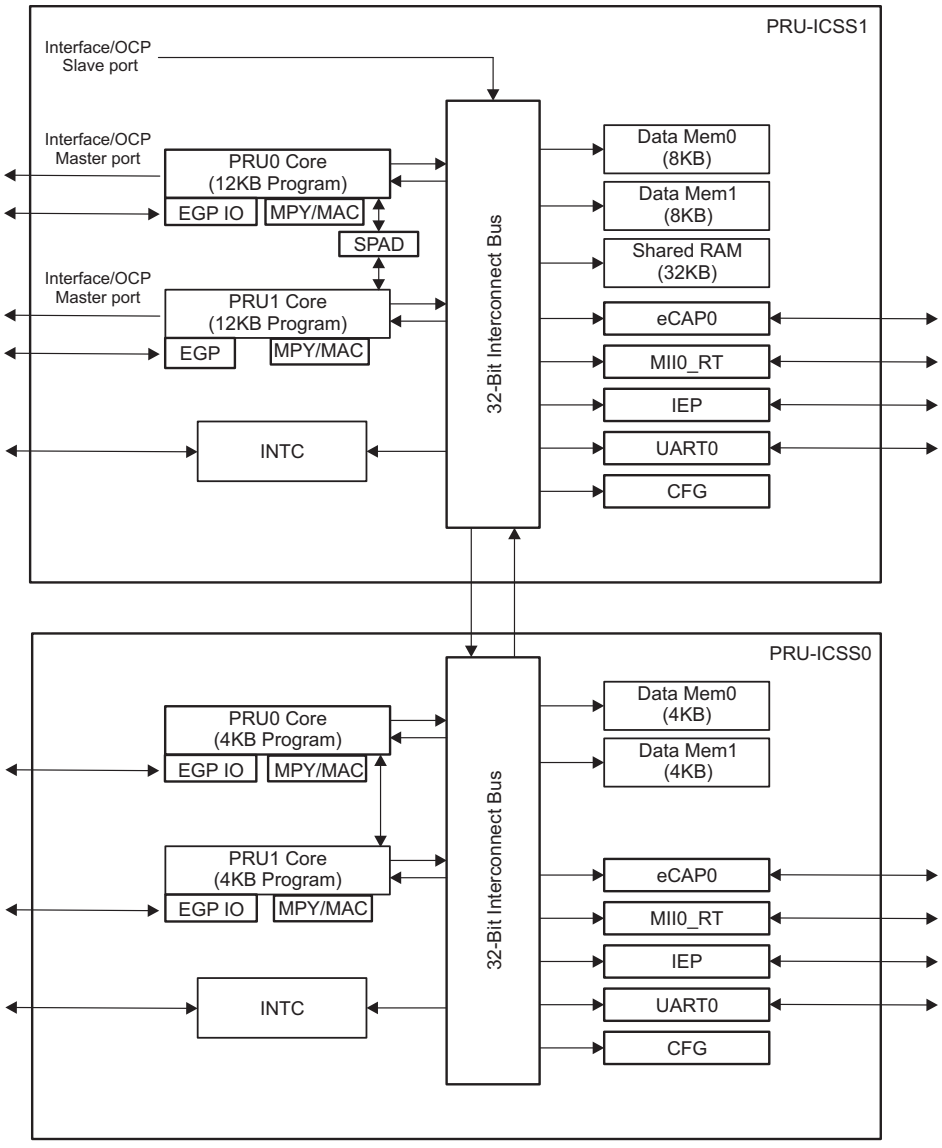


図 3. PRU-ICSS Block Diagram

5.5.1.1 ΔΣ Decimation Filter

ΔΣ Sinc3 filtering is achieved by the combination of PRU hardware and firmware. PRU hardware provides hardware integrators that do the accumulation part of Sinc3 filtering, while the differentiation part is done in firmware. In the following topic, the filter implementation is explained for Sinc3 implementation; however, the same method can be used to implement other filtering.

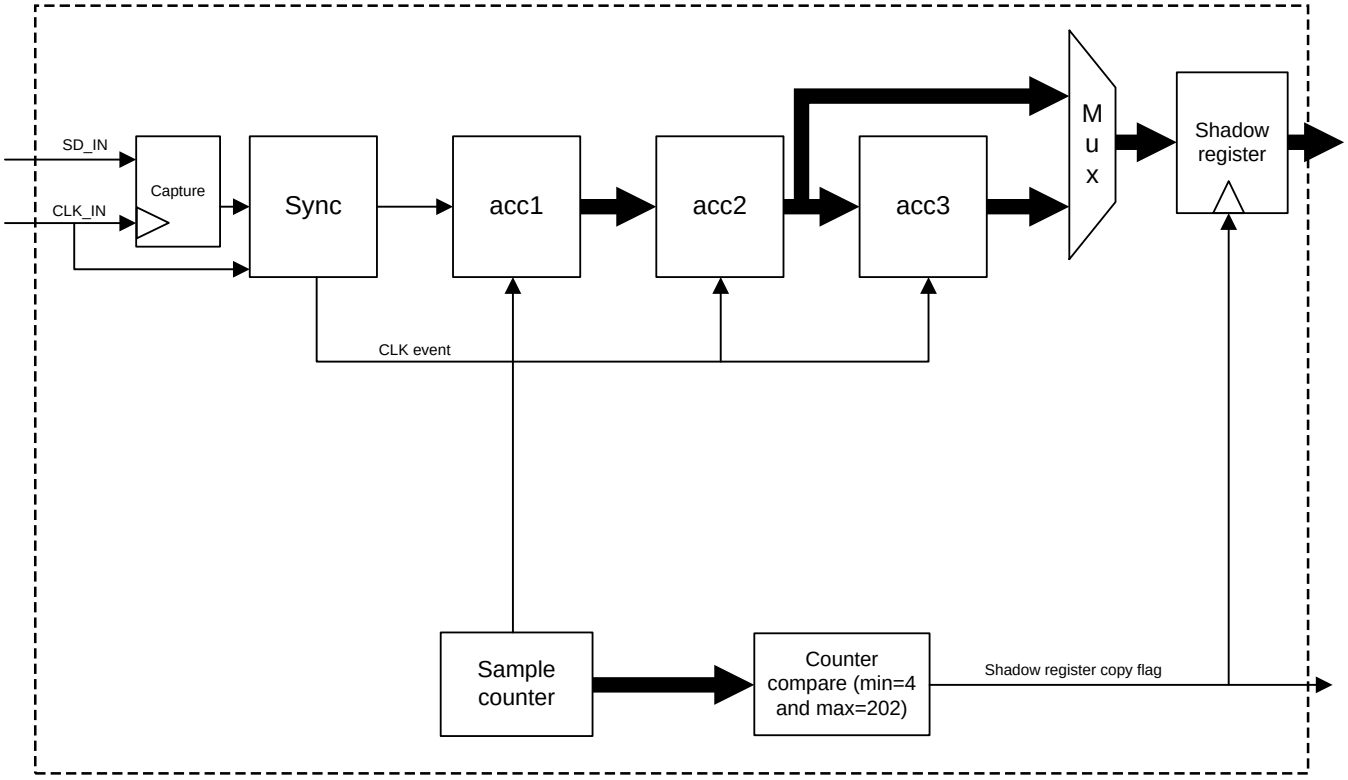
Integration (PRU Hardware)

Both ICSS0 and ICSS1 implement the integrators of the ΔΣ demodulators in the Enhanced General Purpose Input Output (EGPIO) peripheral of the PRU. The integrator serves to count the number of 1s per clock event. Each channel has three cascaded counters, which are the accumulators for the Sinc3 filter. Each counter is 24 bits, giving a maximum count of 16,777,215. Each channel has a free-running rollover clock counter. This sample counter updates the count value on the effective clock event for that channel. Each channel also contains a programmable counter compare block and the compare register has a size of 8 bits. However, the minimum value is 4 and maximum value is 202 because of the 24-bit accumulator. When the sample counter compare value has been reached, the shadow register copy is updated and the shadow register copy flag is set.

Features of the integrators in PRUs EGPIO:

- Up to nine channels with concurrent counting
- Flexible clock source configuration for each channel; option of independent clock source for each channel or one clock source for three channels
- Programmable, 8-bit sample counter compare register; used to set the OSR of Sinc3 filter
- Three 24-bit cascaded counters per channel for accumulation, only Sinc3 and Sinc2 modes supported
- Common channel enable (all channels are active or none are)

図 4 shows the implementation of an integrator with an ICSS-PRU.



Note:

All acc are simple 24 bit adders
acc1 input is 1-bit
acc2 and acc3 inputs are 24-bit, rollover will occur at 0xff_ffff

Example: if acc2 = 0x10 and acc3 = 0xff_ffff,
next clk_event will have acc3 = 0x0_000f

Every rising edge of CLK_OUT then
acc1 = acc1 + sd_sync
acc2 = acc2 + acc1
acc3 = acc3 + acc2
sample_count = sample_count +1

Note:

1) if (over_sample_counter = over_sample_size)
then
Update shadow copy
set shadow_update_flag
reset over_sample_counter

2) snoop is optional method to read acc2 or acc3 directly

3) when sample_counter_select = 1
then
sample_count is read,
if snoop = 1
then
direct read of active counter

図 4. Integrator Block Diagram in ICSS-PRU

Differentiation (PRU Firmware)

An overview of the firmware functions is shown in 図 5. The firmware functions mainly consist of a set of different equations, referred to as the filter calculations. This firmware function is repeated for each channel. There are two data paths per channel shown in the firmware function: One path does a Sinc3 decimation part of the filter calculation at a higher OSR used for accuracy and the other path is at a lower OSR used to quickly respond to short-circuit conditions. The results of the higher OSR filter calculation are used by the application software. The digital value obtained with this filter is copied to a circular buffer of 126 samples and the beginning of the buffer contains a write pointer that points to the latest sample in the buffer.

The lower OSR filter is a parallel data path to the higher OSR filter. The output of the lower OSR filter is compared with a threshold value in the PRU firmware. If the threshold is exceeded, the PRU indicates this event on a general purpose input/output (GPIO) pin with a signal transitioning from low to high. This path is faster to calculate the result as it uses a smaller OSR; therefore, the path is used for input fault detection. The OSR is configurable in both data paths.

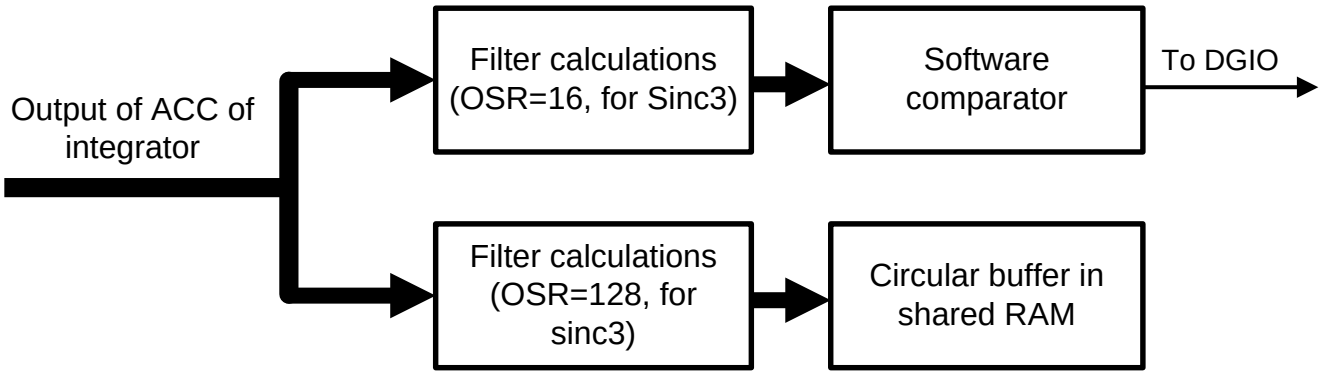


図 5. Firmware Functions Overview

The implementation within the filter calculation block of 図 5 is shown in 図 6. 図 6 is the differentiation, or the delta part, of the Sinc3 filter. The filter for both the high OSR filter and low OSR filter is of the same type.

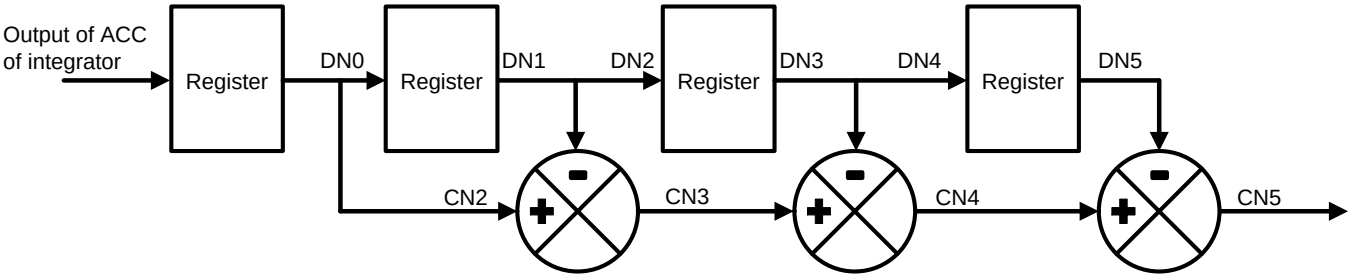


図 6. Sinc3 Filter Differentiation Implementation in PRU

The calculation done in PRU to implemented the differentiation block is given here:

```
dn1  =  dn0
cn3  =  dn0 – dn1
dn3  =  cn3
cn4  =  cn3 – dn3
dn5  =  cn3
cn5  =  cn4 – dn5
dn5  =  cn4
cn5  =  cn4 – dn5
```

‘dn0’ is the accumulated value for Sinc3 filter. This value is read from PRU hardware explained above. ’cn5’ is the conversion result of the ΔΣ Sinc3 filtered. Other values are initialized to zero in the beginning.

The sample counter compares register sets up the OSRs of the filters. The shadow register copy flag is used to initiate the filter calculation and the shadow register copy flag is generated when the sample counter overflows when it is equal to the sample counter compare register. However, because there is only one flag per channel, the sample counter compare register is set up for the lower OSR. The higher OSR filter calculation is done by decimating the shadow register copy flag, which is done by a software counter.

For example, for a lower OSR of 16 and a higher OSR of 128, the sample counter compares register is 16 (that is, the lower OSR). For the higher OSR filter, the filter calculation is done every eighth time the shadow copy flag is generated, resulting in an OSR of 128 as 16 × 8 = 128. This also implies that the higher OSR has to be a multiple of the lower OSR.

The firmware can be modified to have a different OSR. Overcurrent detection can be modified to either use Sinc2 or accumulator value of Sinc2 or Sinc3 based on the requirement.

6 Getting Started

6.1 Signal Conditioning for Current and Voltage Input

6.1.1 Isolated Current Measurement

A shunt is used to measure the input current instead of a conventional current transformer.

Shunt selection:

The TIDA-00738 design can measure a current range of 0.1 A to 40 A (or 60 A). The shunt value and wattage are both important to minimize power dissipation across the shunt, which is mounted on the board. This design uses a 0.7-mΩ shunt (see 図 7). 表 5 summarizes the power loss for the selected shunt value.

表 5. VA Drop Across Shunt

SHUNT VALUE	CURRENT RANGE		VOLTAGE DROP ACROSS SHUNT	
0.7 mΩ	I_{MIN}	I_{MAX}	V_{SHMIN}	V_{SHMAX} at 60 A
	0.1 A	40 A (or 60 A)	70 µV	42 mV

注: The expected nominal burden at In is < 0.1 VA at In = 1 A.

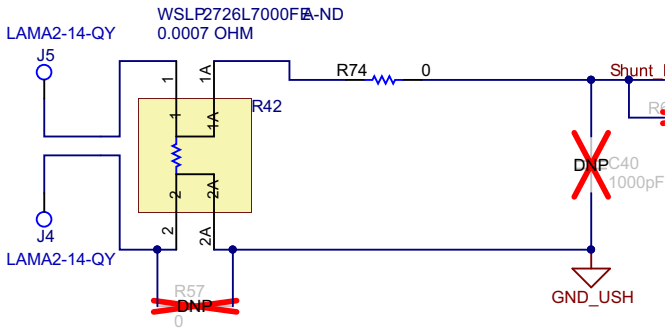


図 7. Onboard Shunt

Gain amplifier configuration:

The following 表 6 shows the voltage input to the modulator, which is based on the configured gain.

表 6. Voltage Input (Current Output) to Modulator

GAIN	CURRENT	SHUNT	±50-mV MODULATOR INPUT
X 12.5	0.1 A to 4 A	0.7 mΩ	0.875 mV_{RMS} to 35 mV_{RMS}
X 0.8	2 A to 40 A (or 60 A)	0.7 mΩ	1.12 mV_{RMS} to 22.4 mV_{RMS} (or 33.6 mV_{RMS})

図 8 shows a schematic of the modulator with a high-gain amplifier input is linear that can be used up to 4 A. 図 9 shows a schematic of the modulator with a low-gain amplifier input that can be used from 4 A to 40 A (or 60 A).

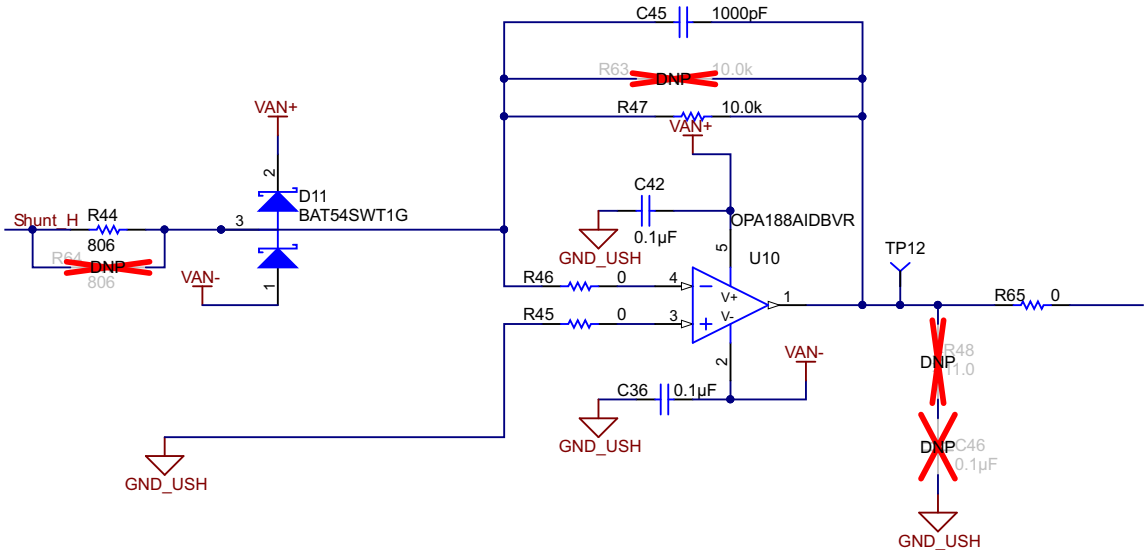


図 8. High-Gain Amplifier Stage

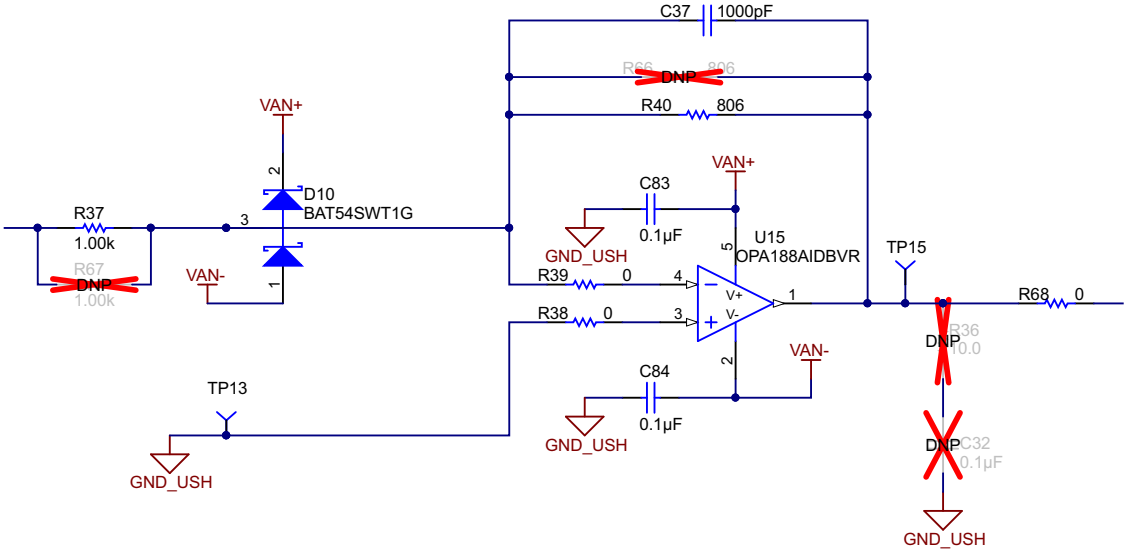


図 9. Low-Gain Amplifier Stage

注: The gain resistor values have been chosen based on accuracy testing performed on the wide current input. Any change in the value must be tested before implementing in the design.

6.1.2 Isolated Voltage Measurement

The design uses a potential instead of a conventional potential transformer to measure voltage. Multiple resistors are used to divide the input to increase reliability and withstand the rated voltage continuously. The voltage can be directly applied when measuring. Select the resistor values to ensure that the input to the AMC1304M25 device is less than the differential input range at the maximum AC input.

Potential divider calculation:

Max sensing voltage → V_{MAX} = 300 V_{RMS} (+ 30% of 230 V)

Peak max sensing voltage → V_{MAX_PK} = V_{MAX} × 1.4142 = 425 V

The peak voltage output of the resistor divider used for measurement must be less than the input voltage range of the AMC1304M25 device, which is ±250 mV. The potential divider ratio is selected such that the output voltage is less than the AMC1304M25 voltage at the maximum input voltage (see 図 10). This design uses a 1.02-KΩ for measurement. The following 式 1 provides the calculation for the resistor value that is used to connect to the modulator.

$$R2 \geq \frac{V_{OUT}}{\left(V_{MAX\_PK} - V_{OUT}\right)} \times 1.66\ M\Omega$$

$$R2 \geq 0.978\ k\Omega \quad (1)$$

The AMC1304M25 is optimized for use in current-sensing applications that use low-impedance shunts; however, the device can also be used in isolated voltage-sensing applications after accounting for the impact of the (typically higher) impedance of the resistor used in this case.

Refer to the *Isolated Voltage Sensing* section in the SBAS654 data sheet for more details on the errors caused by higher impedance.

This design uses the OPA188 operational amplifier as a buffer to minimize the errors caused by higher impedance (see 図 11).

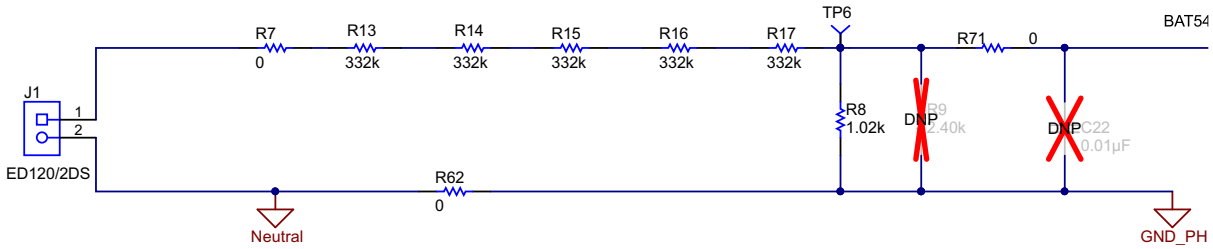


図 10. Potential Divider

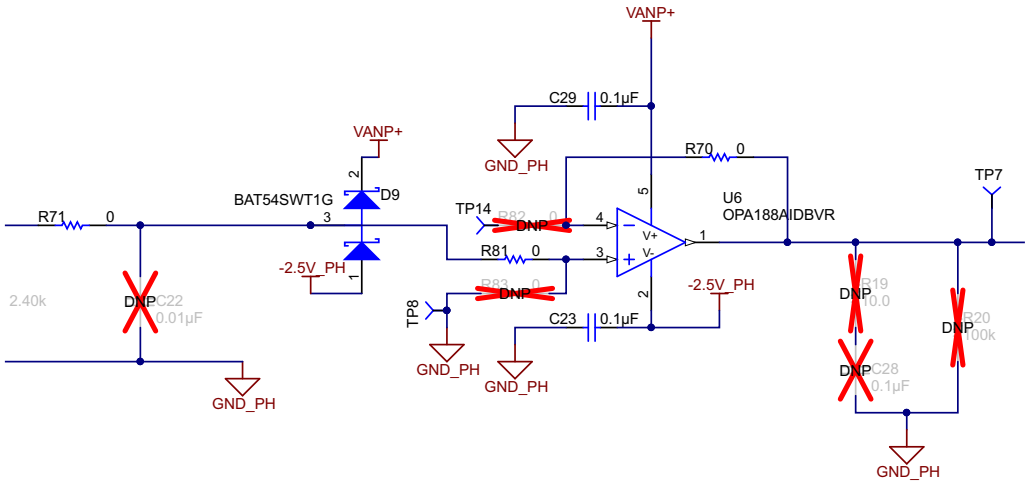


図 11. Buffer for Voltage Input

Potential divider selection:

Multiple resistors have been used to divide the input voltage to a ±250-mV input. Using multiple resistors increases the reliability. The number of resistors to use depends on the application and can be optimized after testing the product or system for conformance based on intelligent electronic device (IED) standards.

6.2 Isolated ΔΣ Modulators

6.2.1 AMC1304M05 ΔΣ Modulator for Current Measurement

The input of the AMC1304M05 has been optimized for connecting directly to a shunt. The unique, low-input voltage range of the ±50-mV device reduces power dissipation through the shunt while supporting AC and DC measurement. The following schematics in 図 12 show the use of two modulators for measuring wide input current. The modulators provide reinforced isolation and a CMOS digital interface.

On the high side, the modulator is supplied by an integrated LDO regulator, which allows an unregulated input voltage between 4 V and 18 V (LDO_{IN}). Both modulators share a common power supply.

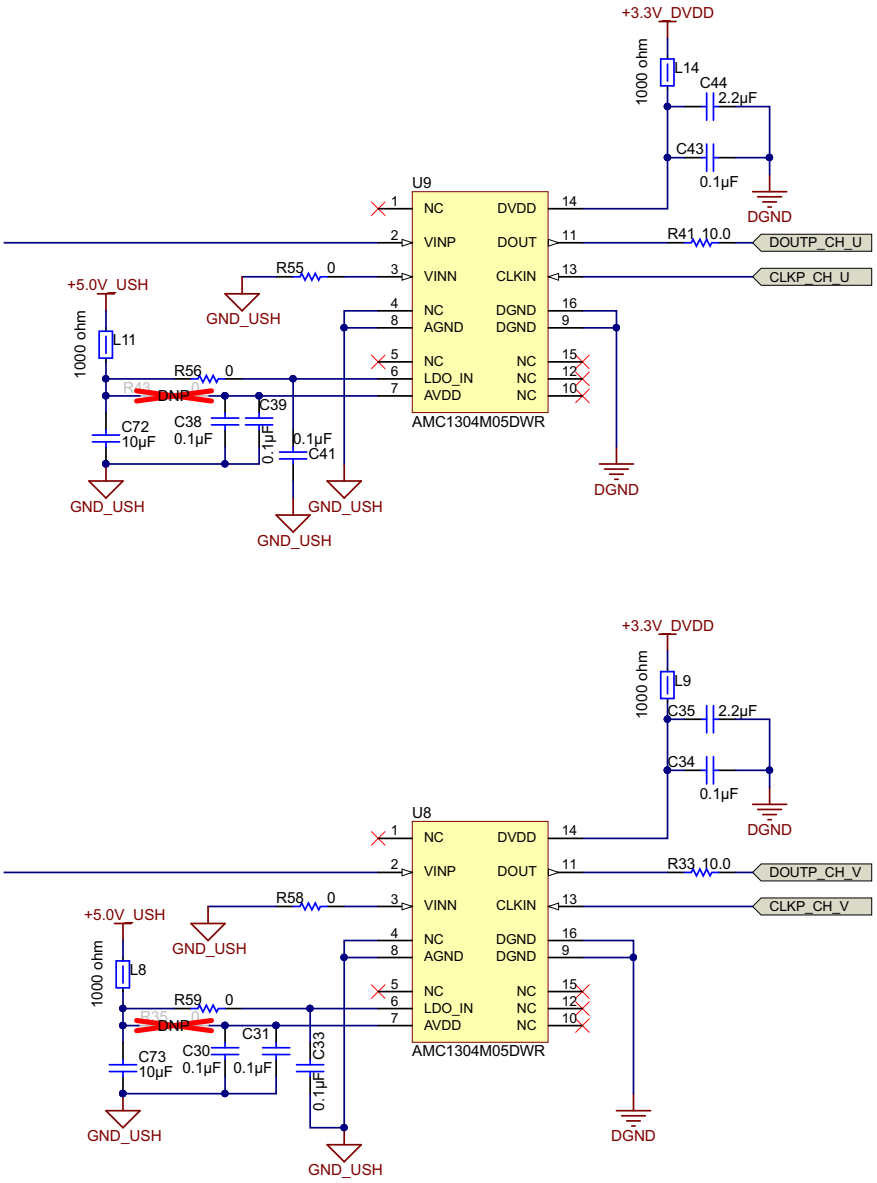


図 12. Modulators for Current Measurement

6.2.2 AMC1304M25 ΔΣ Modulator for Voltage Measurement

The modulator used to measure voltage has a ±250-mV input voltage range (see 図 13). The power supply to the voltage modulator is isolated from the current measurement modulators.

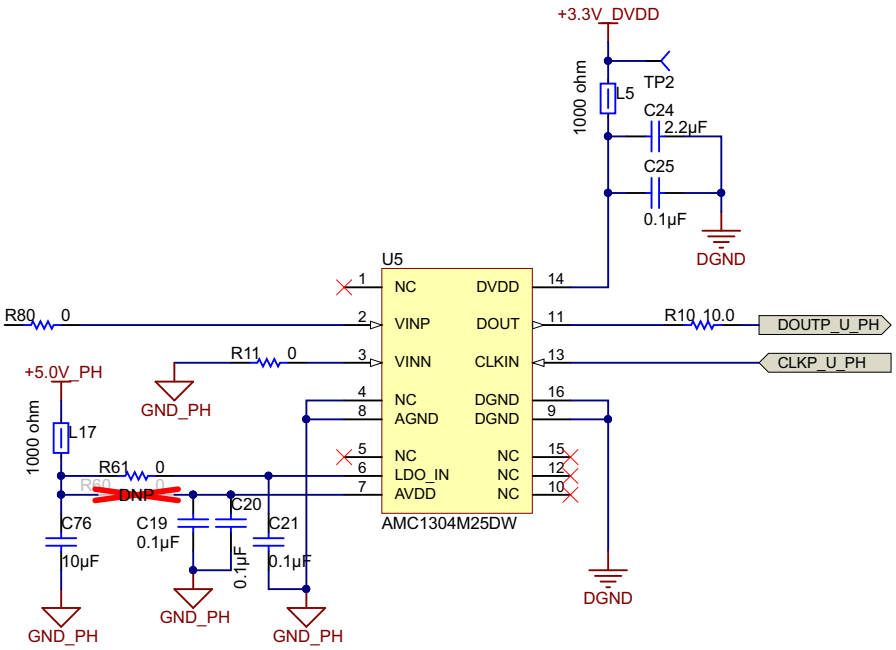


図 13. Modulator for Voltage Measurement

6.3 Isolated Power Supply

6.3.1 Current Measurement

A transformer driver is used to generate the required isolated DC voltage output for measuring current and voltage (see 図 14). This design implements two separate drivers to generate the power supply for the AFE. The design uses an isolation transformer with a 1.64:1 turns ratio to generate ±6 V. The ±6 V is regulated using LDOs to generate the required DC power supply rails.

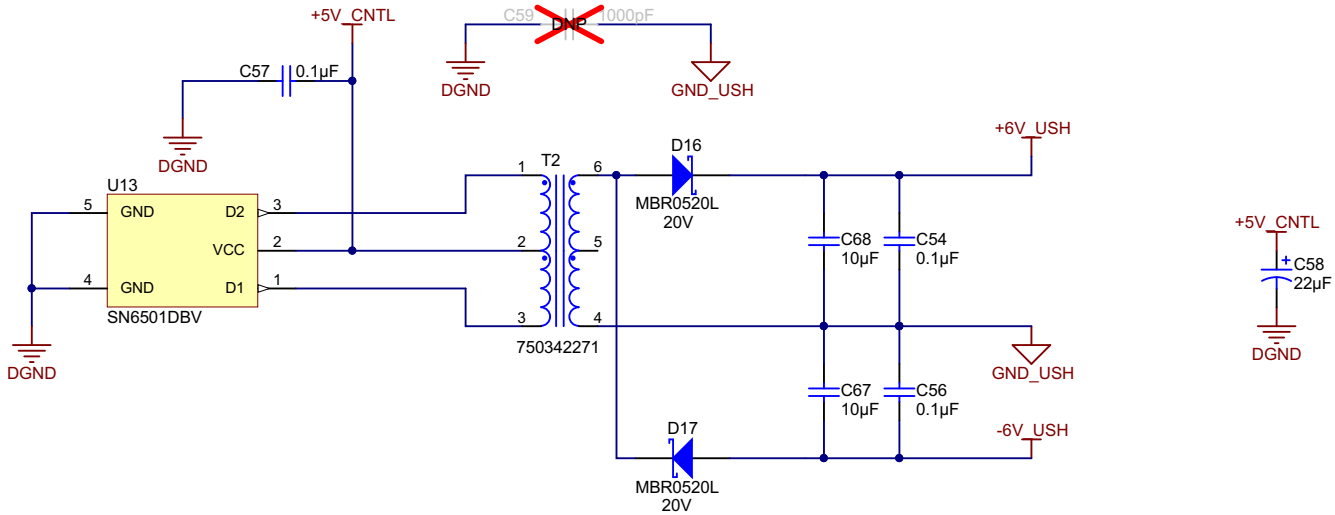


図 14. Isolated Power Supply for Current Measurement

6.3.1.1 +5 V and ±2.5 V for Current

The following voltages are used to operate the AFE:

- +5 V for modulators
- +5 V or +2.5 V and –2.5 V for op amp

The output of the transformer driver is regulated using the LDOs in the following 図 15 and 図 16. The power supply outputs in both figures have protection against overvoltage and electrostatic discharge (ESD).

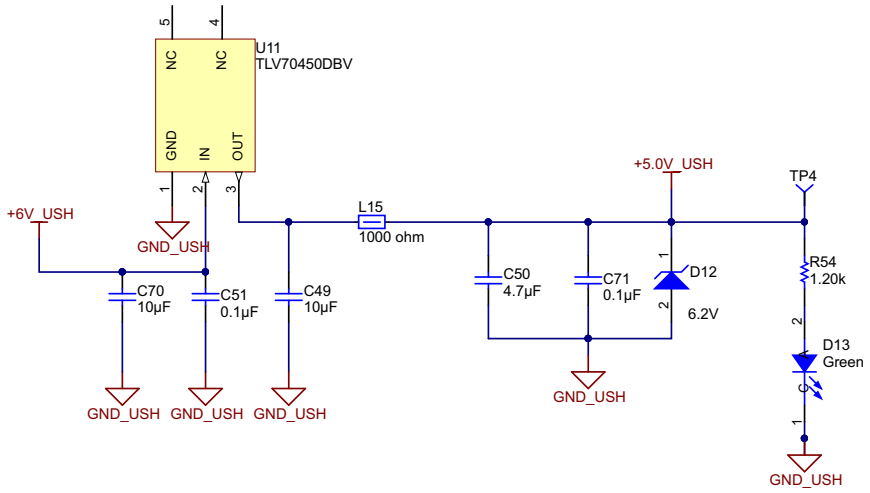


図 15. +5-V Supply for Modulators

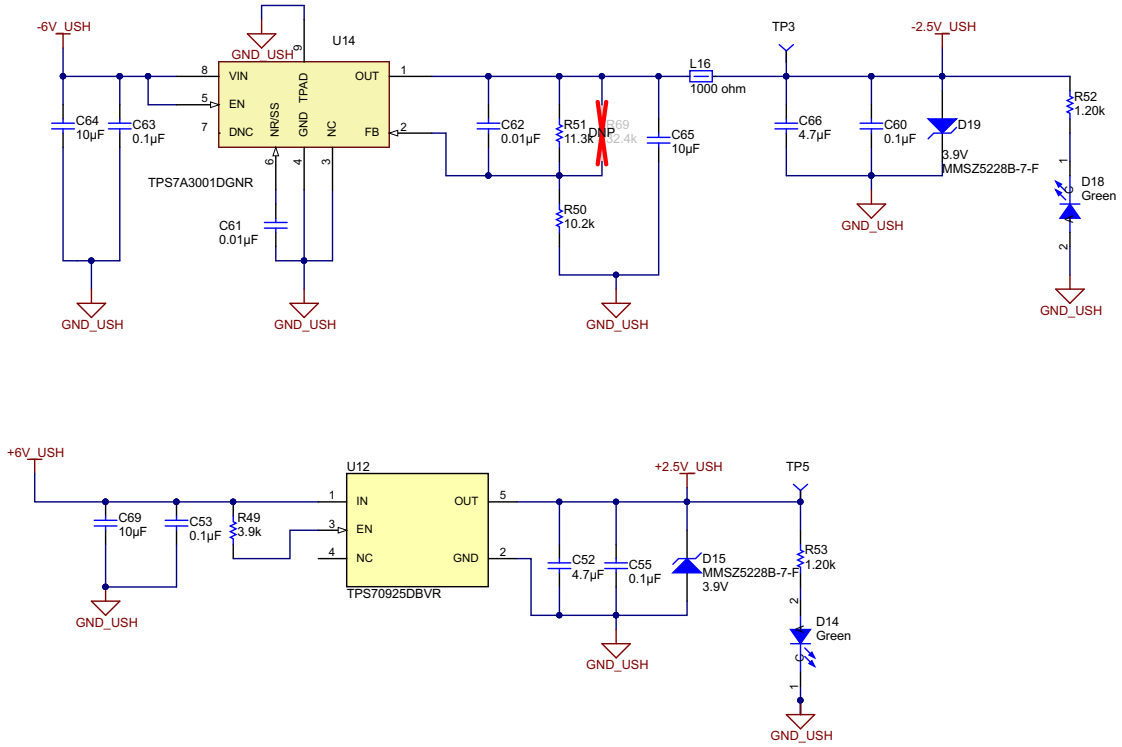


図 16. ±2.5-V Supply for Op Amp

注: 2.5 V is optional and is not required for use in this design.

6.3.2 Voltage Measurement

The isolated power supply design is similar to the current measurement block. The power supply outputs shown in 図 17 have protection against overvoltage and ESD.

The following voltages are used to operate the AFE:

- +5 V for modulator
- +5 V or +2.5 V and –2.5 V for op amp

The output of the transformer diver is regulated using the LDOs in the following 図 17.

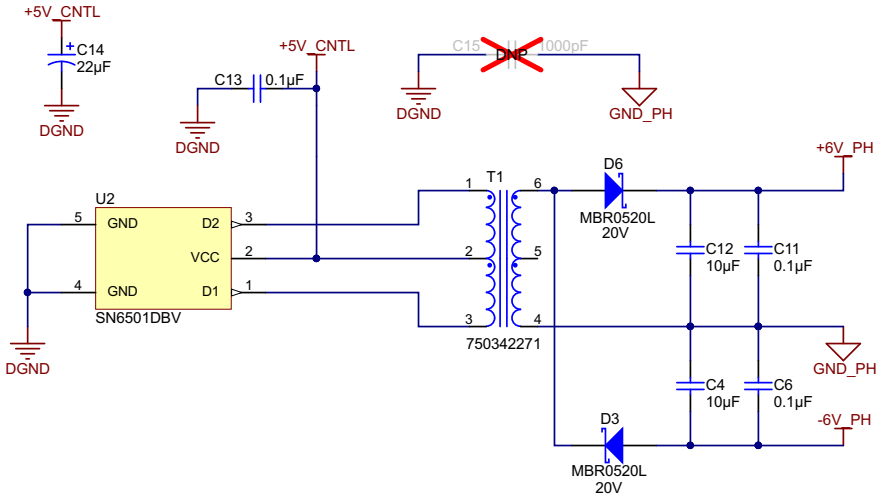


図 17. Isolated Power Supply for Voltage Measurement

6.3.2.1 *+5 V and ±2.5 V for Voltage*

The following 図 18 and 図 19 show the LDOs used to generate the power supply for the voltage modulators.

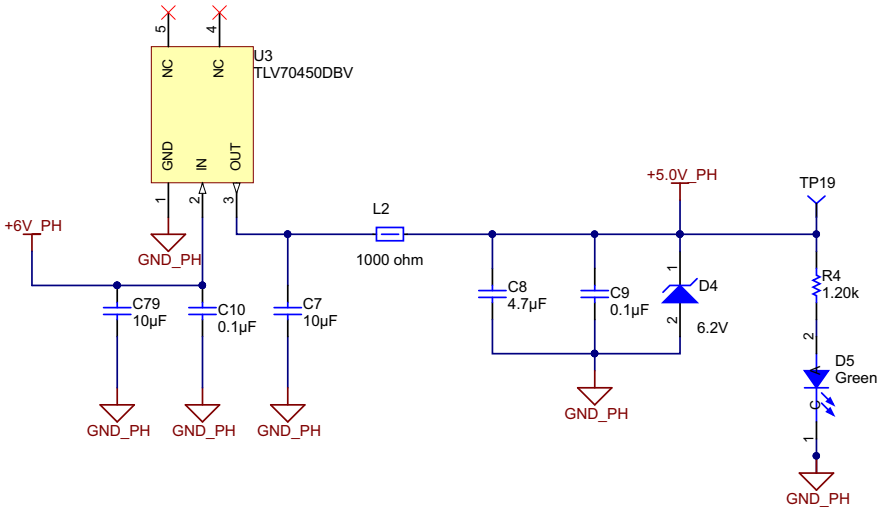


図 18. +5 V for Voltage Modulator

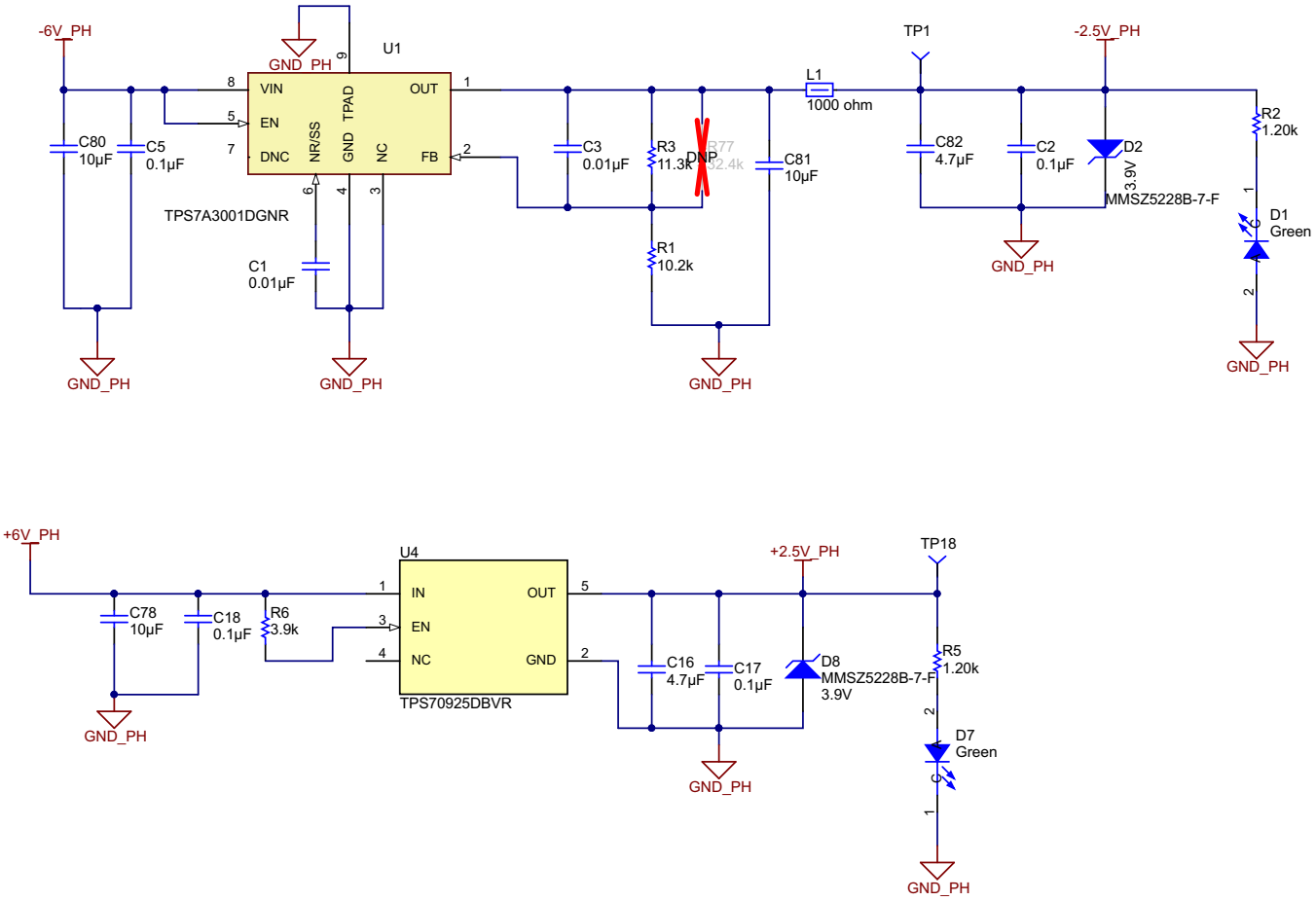


図 19. ±2.5-V Rails for Op Amp

6.3.3 Digital Power Supply Connector

The power supply can be applied externally to test the AFE functionality. The 3.3 V and 5 V can be applied from an external DC power supply for testing (see 図 20).

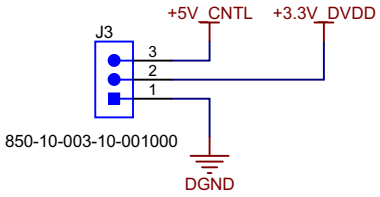


図 20. Test Connector for Applying 5- and 3.3-V Supply

6.4 Clock Buffer for Modulators CDCLVC1103PW

The AM437x IDK generates one clock, which is available on the header J2 of the adapter card. This clock requires a connection to multiple AMC1304Mx5 devices. Select a clock buffer to provide the required source and sink currents. The CDCLVC1103 is a high-performance, general-purpose clock buffer that can supply up to three outputs (see 図 21). This part belongs to the CDCLVC11xx family of devices. The CDCLVC11xx family has low jitter and low-skew LVCMOS fan-out buffer outputs.

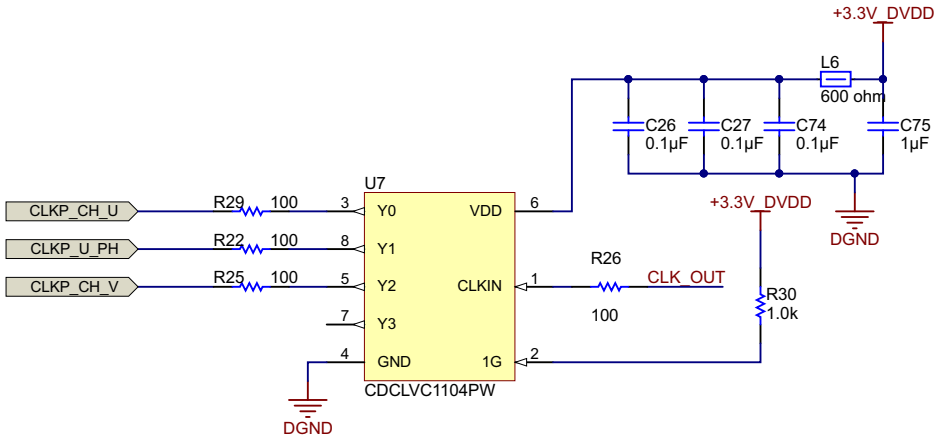


図 21. 1:4 Clock Buffer for Voltage and Current Modulators

6.5 Processor AM437x IDK (Host) Interface Connector

The AM437x IDK interface consists of a fan-out clock buffer that generates three clock outputs from a single clock input (from the IDK). This section also contains the routing of DOUT signals from the AMC1304Mx5 modulator to the AM437X IDK (see 図 22).

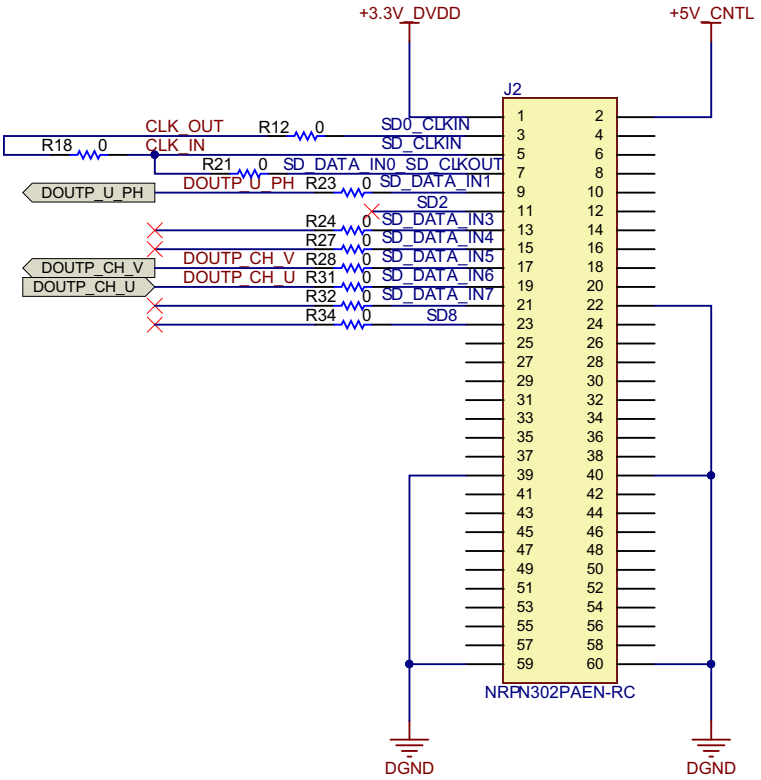


図 22. AFE to AM437X IDK Interface Connector

6.6 AM437x IDK

The IDK is a self-contained evaluation module for the AM437x Sitara processor with onboard memory, power supplies, and power management. A 24-V input is stepped down using a buck converter to generate all of the power rails required for the AM437x processors and memory. The 5 V and 3.3 V generated are tapped to supply the other boards in the circuit. An onboard XDS100V2 is provided for JTAG connection using a micro-USB connector. The XDS100V2 device also provides a universal asynchronous receiver/transmitter (UART) connection to the Sitara processor, which enables communication with the GUI. The IDK supports various expansion headers interfacing with other boards. A 2×30-header is used to interface to the adapter card.

The AM437x IDK is an application development platform for evaluating the industrial communication and control capabilities of Sitara AM4379 and AM4377 processors for industrial applications (see 図 23).

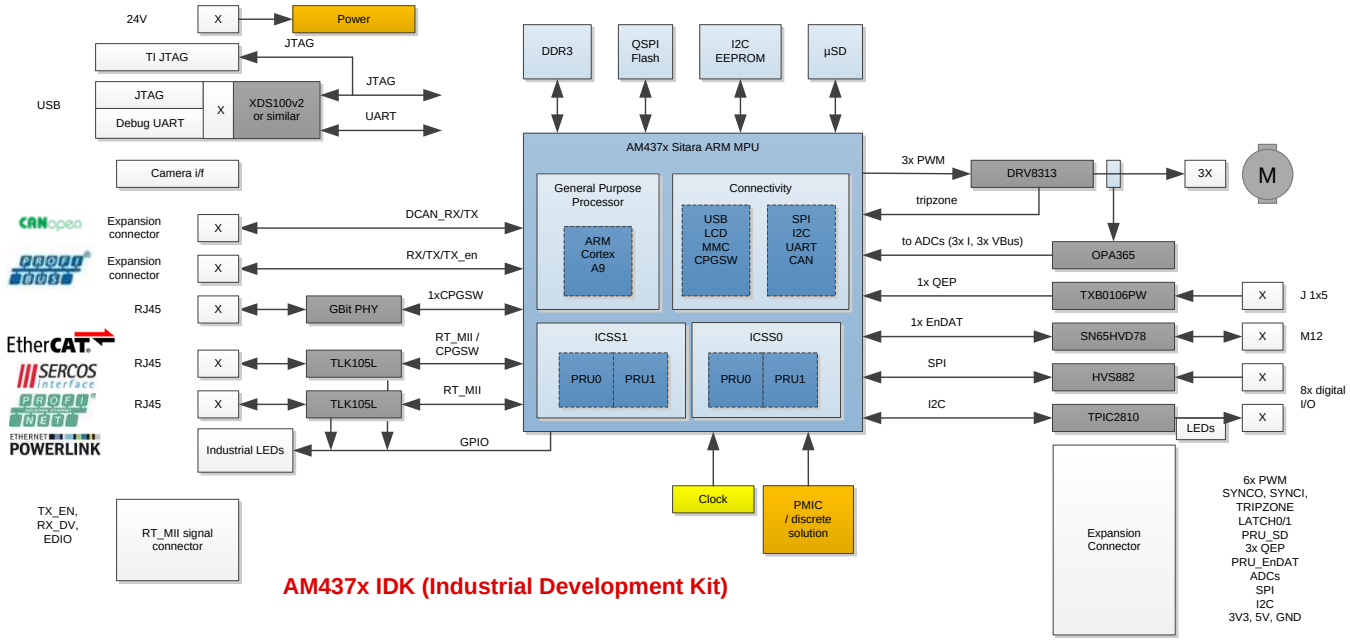


図 23. AM437x IDK Block Diagram

The AM437x IDK features:

- Connectivity: The IDK supports many connectivity options used in motor drives like EtherCAT®, EnDat 2.2 BiSS, PROFINET, CANOpen, PROFIBUS®, POWERLINK, Ethernet/IP, SERCOS III, and IEC61850
- Position encoder interface
- Three-phase motor driver
- microSD card: used to store the application software
- Onboard Isolated JTAG Emulation: the JTAG interface supported by the onboard XDS100V2 emulator is used for a convenient interface with TI's Code Composer Studio™ (CCS) software. The XDS100V2 also interfaces with the AM437x UART, which connects to the GUI.
- Multiple expansion headers: breakout for digital inputs and outputs (I/O), pulse width modulation (PWM), serial peripheral interface (SPI), and ΔΣ decimation filter

The following 図 24 highlights the aforementioned features and more.

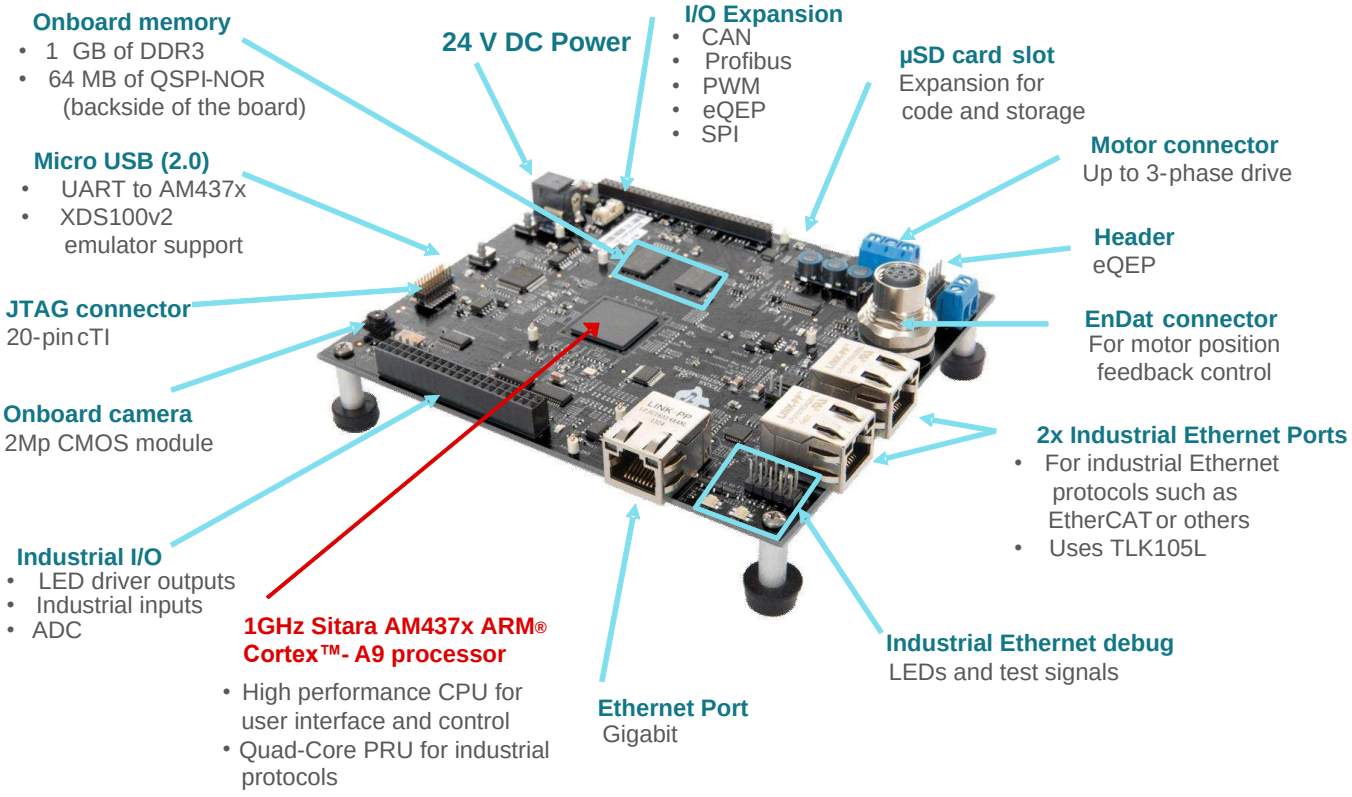


図 24. AM437x IDK

The firmware implements for four channels: 1, 5, 6, and 7. The firmware only implements four channels because some of the pins used for ΔΣ demodulation have been allocated for other functions on the IDK. A custom design can support up to nine channels of ΔΣ demodulators. A higher oversampling rate (OSR) of 128 is used and must be a multiple of the lower OSR (for fault current processing).

6.7 Application Software Description

図 25 shows the interaction between the ARM, PRU, and ΔΣ modulator card.

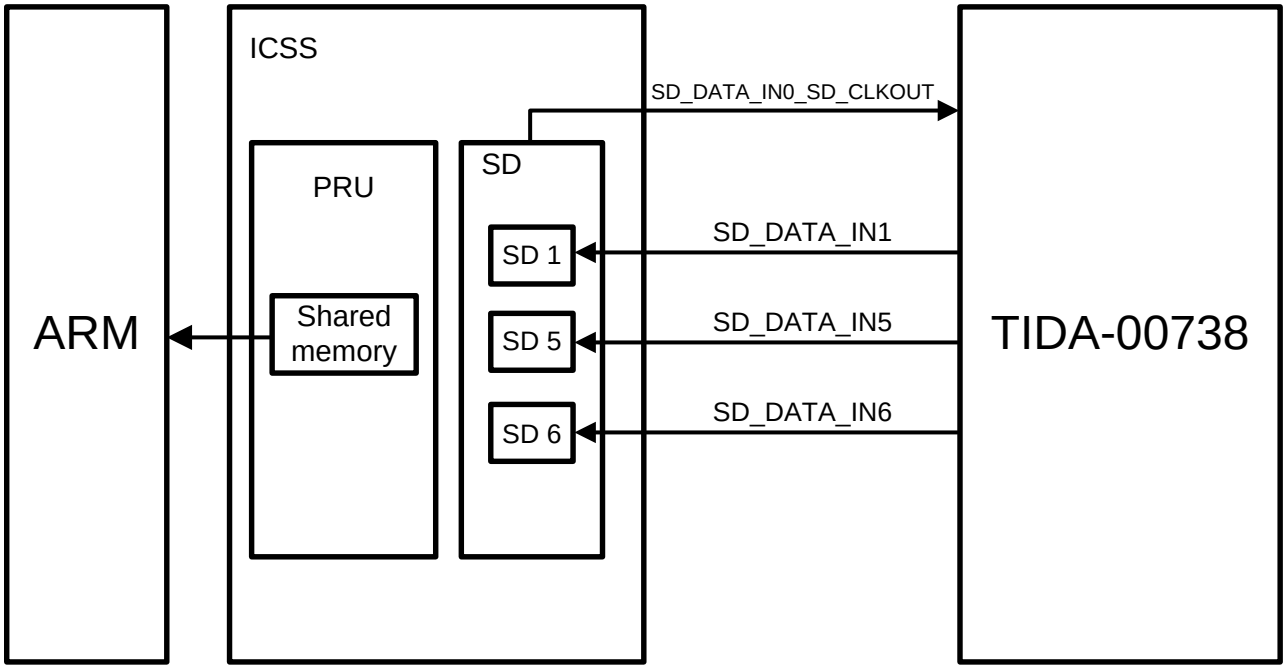


図 25. Interaction Between ARM, ICSS, PRU, and TIDA-00738

The software for this design has been developed as a SYSBIOS CCS project. The SYSBIOS contains a StarterWare™ software library from TI for handling various peripherals on the AM437x. The purpose of the software is to set up the pinmux, start PRU execution, handle the UART port (available over USB through an onboard FTDI) to interface with the GUI in a host PC so the user can validate the AMC1304Mx5 performance, and configure the OSR and ΔΣ modulator clock frequency.

The software initially controls the setup of the pinmux for the ΔΣ clock, signal lines, and PRU digital I/Os. The software then Initializes the PRU1 of ICSS_L, loads the ΔΣ firmware onto its instruction memory, and starts execution. Next, the UART is set up using StarterWare libraries. The AM437x device provides the clock for the ΔΣ modulator and the software configures the PRU to provide the required clock frequency. The GUI in the host PC can configure OSR. The software mostly functions like a client for the GUI and handles the configuration of the PRU ΔΣ OSR accordingly. The software also controls the transfer of sampled values through the UART so that the GUI can display the measured samples. Because the GUI requires 16-bit signed data, a sample value is signed and the majority of significant 16 bits are extracted and then sent to the GUI.

6.7.1 Getting Started

This software has been compiled from CCS. The SD card is loaded with two files: ‘app’, which is the generating executable binary, and 'mlo', the bootloader. On power up, the AM437x loads the application from the SD card located in the micro SD card slot on the IDK. For further details on creating these files from the source code, consult the *AM437x SYSBIOS Industrial SDK 02.00.00.02 User Guide* [3].

7 GUI User's Guide

This section describes the functionality of the GUI for isolated current and voltage measurements.

7.1 Installing Run-Time Engine

Follow these steps to download and install the LabVIEW™ run-time engine to use the IVIM Test Bench:

1. Click on the link to install the LabVIEW Run-Time Engine 2010 SP1 (32-bit Standard RTE): http://www.ni.com/download/labview-run-time-engine-2010-sp1/2292/en/
2. Run *LVRTE2010_SP1f5std.exe* to install the LabVIEW 2010 SP1 Run-Time Engine (32-bit).
3. Follow the installation wizard and complete the installation.

The installation files for the run-time engine are automatically extracted to a directory on disk. The installer does not remove the files after installing. To remove these files from the disk, note their location during the unzipping process.

7.2 Installing VISA

Follow these steps to download and install the VISA driver to communicate with the device:

1. Click the link to install the NI-VISA 5.0.3: http://www.ni.com/download/ni-visa-5.0.3/2251/en/
2. Run the *visa503full_downloader.exe*.
3. Follow the installation wizard and complete the installation.

7.3 Installing IVIM Test Bench

The GUI can be found at TIDA-00209:

1. Select the *Destination Directory* for IVIM Test Bench and click the *Next* button.

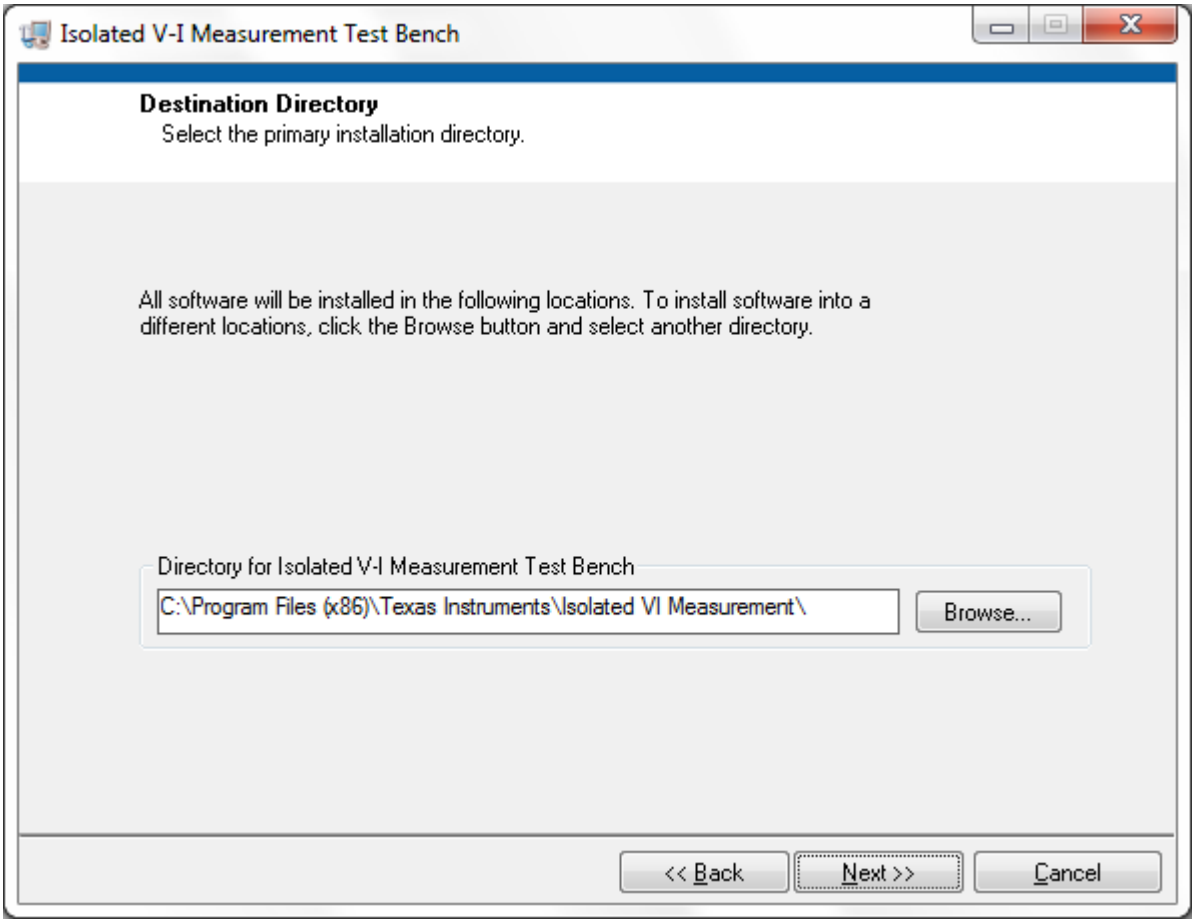


図 26. Destination Directory Selection Window for IVIM Test Bench

2. 図 27 shows the list of files that will be added or modified with this installation. Click the *Next* button.

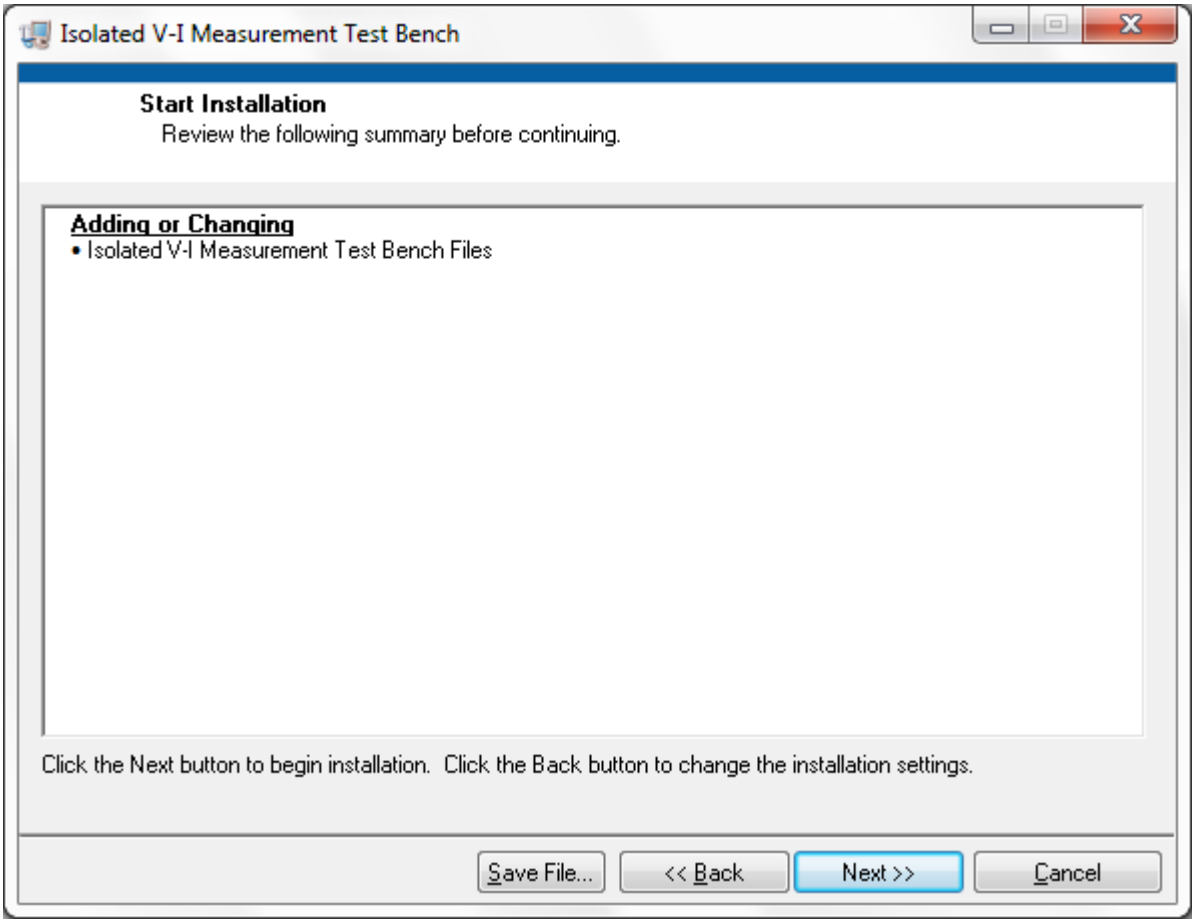


図 27. List of Files Added or Modified With Installation

3. After starting the installation and then finishing, click the *Finish* button as shown in 図 28.

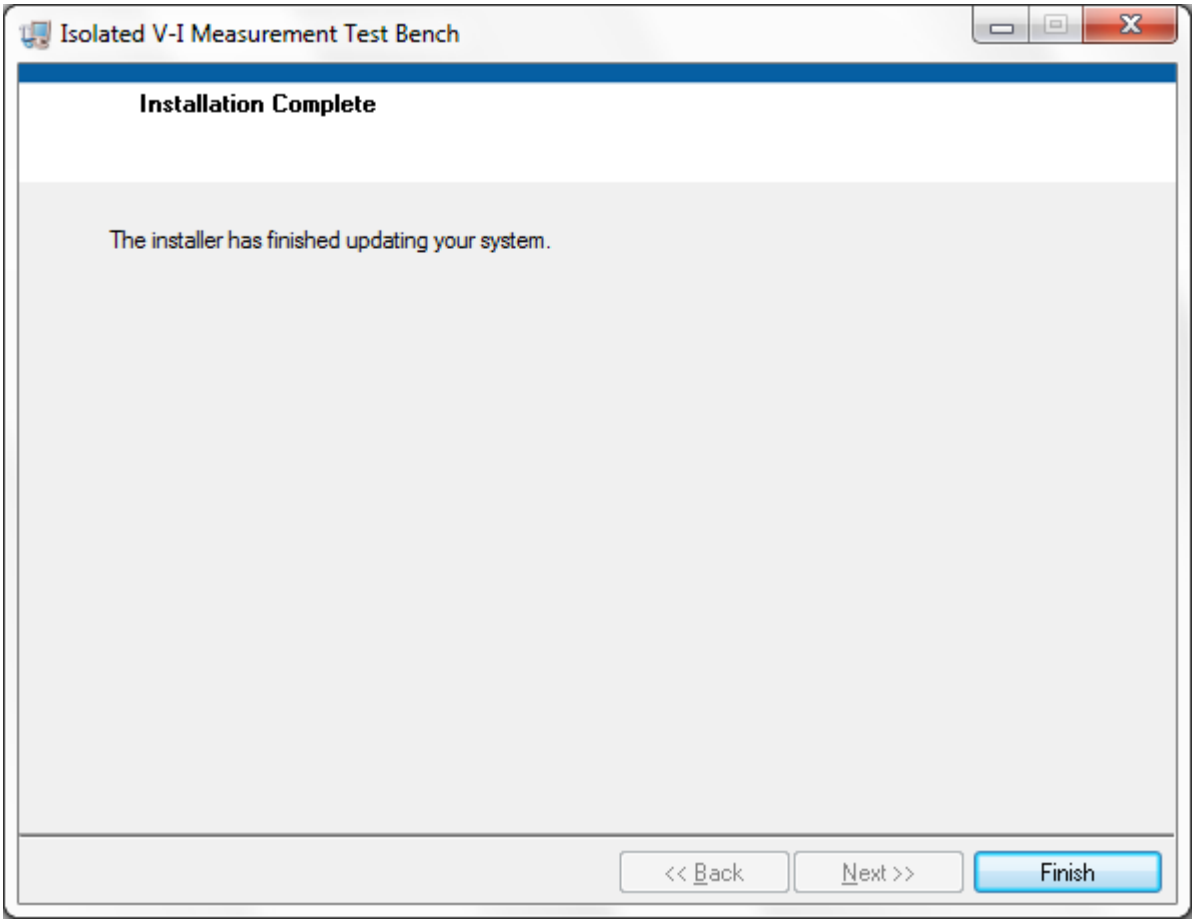


図 28. Window After Successful Installation

7.4 Launching IVIM Test Bench

Follow these steps to launch the IVIM Test Bench:

1. Locate the IVIM Test Bench through any of these approaches:
   - Desktop shortcut
   - Start menu shortcut
   - Installed folder location; the default location is:
     C:\Program Files (x86)\Texas Instruments\Isolated VI Measurement
2. Double-click on the *Isolated V-I Measurement.exe* (図 29)

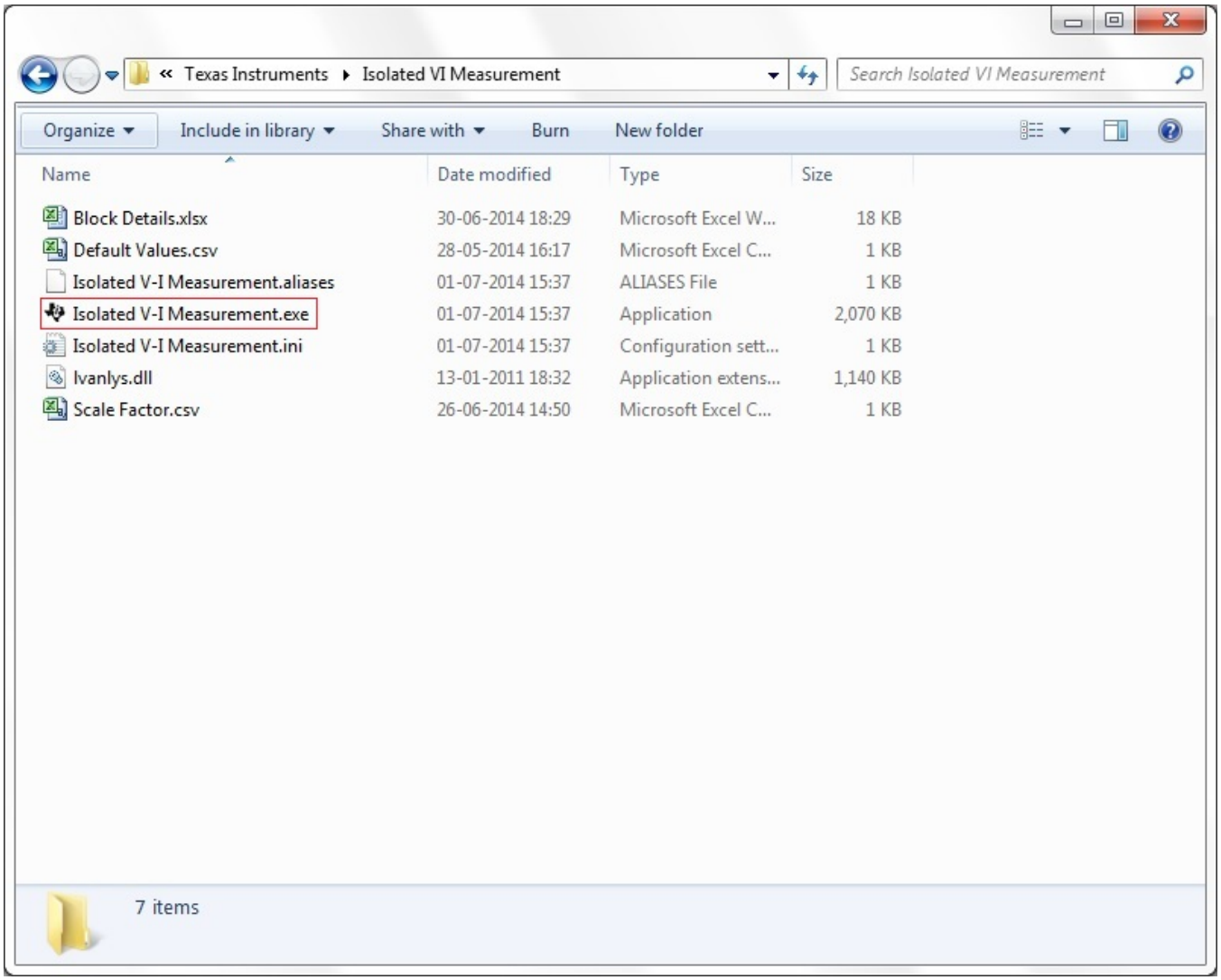


図 29. Isolated VI Measurement Folder Structure

7.5 Mode Selection

The *Select a Mode* dialog box pops up as the application is launched (図 30). Select *Sitara* and the corresponding VISA resource name (the communication port number that appears when the AM437X IDK is connected to the computer).

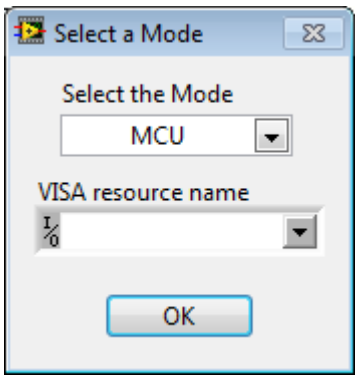


図 30. Mode Selection

As soon as the user selects the mode, the GUI starts to initialize.

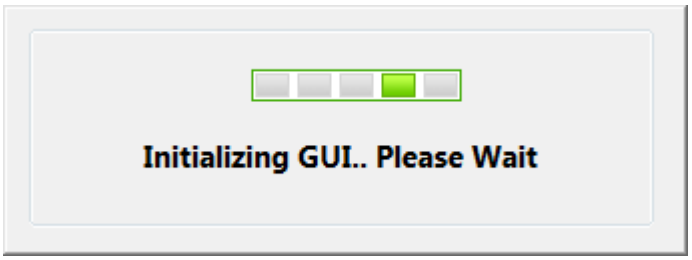


図 31. GUI Initialization

Proceed to use the GUI after the initialization completes.

7.6 IVIM Pages

The IVIM Test Bench has three pages:

1. System Layout
2. Config
3. Graph

7.6.1 System Layout

The *System Layout* page shows the block diagram with a description of the parts used in the isolated current and voltage measurement. Moving the mouse pointer over any of the blocks shows the description of the same on the right side of the page with web links for reference. Refer to 図 32.

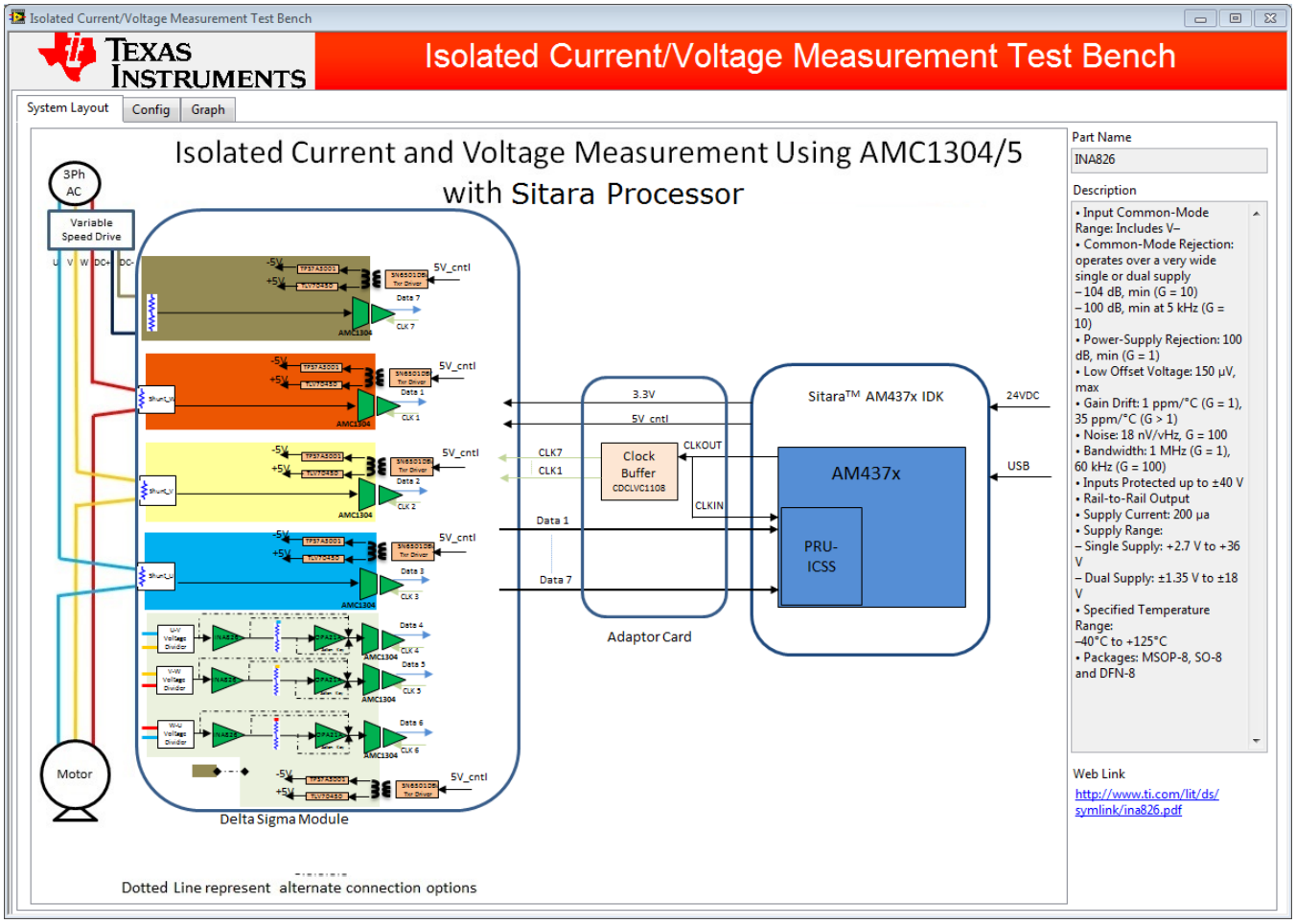


図 32. System Layout

- *Block Diagram*: The block diagram gives the detailed description of the parts used for isolated voltage and current measurement.
- *Part Name*: This box displays the part name selected.
- *Description Box*: This box displays a brief description about the part in the block diagram.
- *Web Link Box*: This box displays the web reference of the part.

7.7 Config Page

This page allows the user to configure the ΔΣ filter parameters.

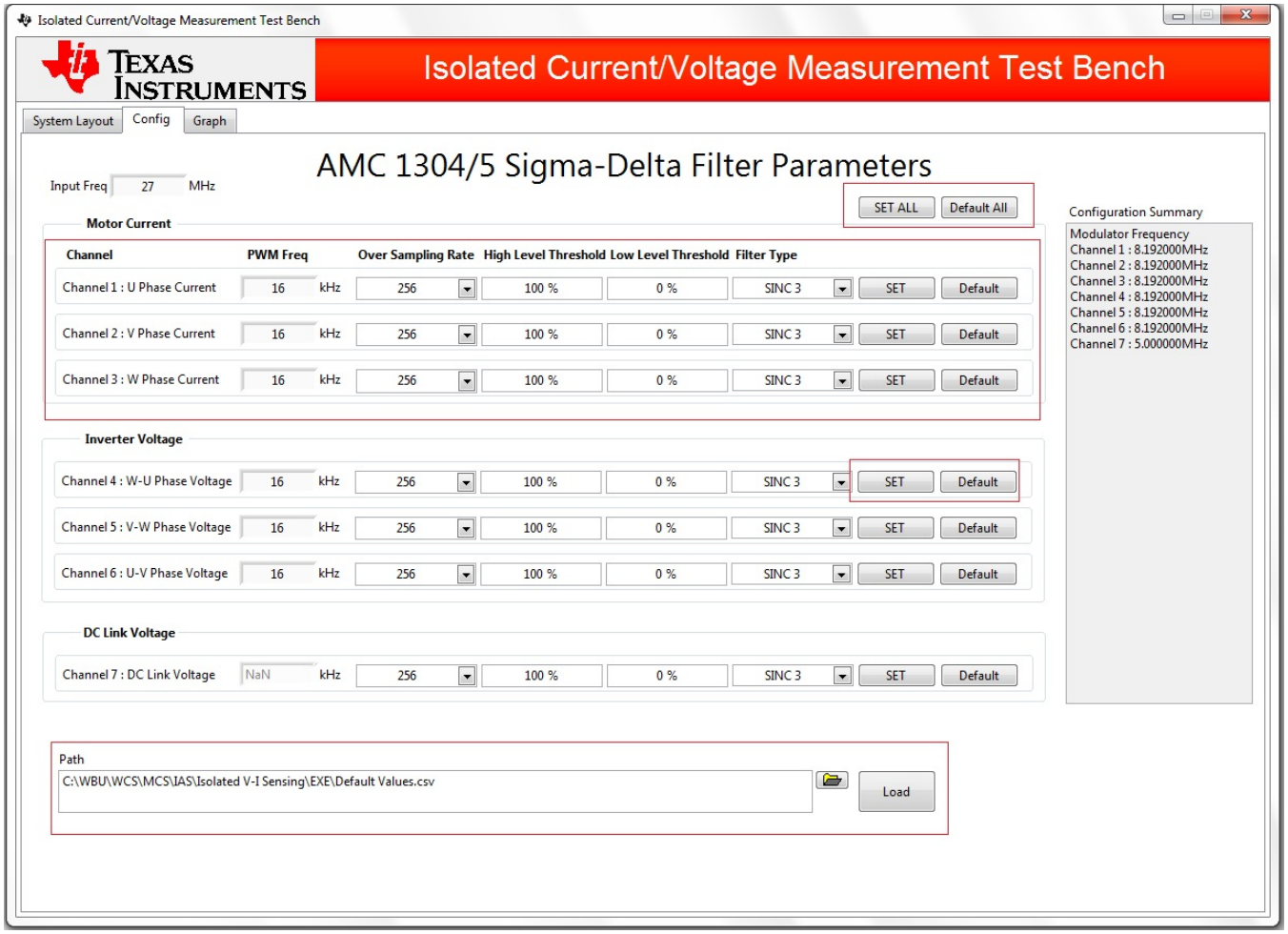


図 33. Config Page

- *Motor Current*: This option contains the settings for three channels to be configured for respective phase current.
- *Inverter Voltage*: This option contains the settings for three channels to be configured for respective phase voltage.
- *DC Link Voltage*: This option contains the setting for a channel to be configured for DC Link voltage.
- *Set*: This button sets the configured settings for the corresponding row.
- *Set All*: This button sets the configured value for all channels.
- *Default All*: This button sets the default values for all channels.
- *Load*: This button loads the values for each parameter form the file specified in the in the path dialog box.
- *Configuration Summary*: This option displays the modulated frequency for each of the channels.

7.7.1 Setting Oversampling Rate

- *Oversampling Rate*: Enter the desired OSR for the Sinc filter. The oversampling rate can be selected from the list.

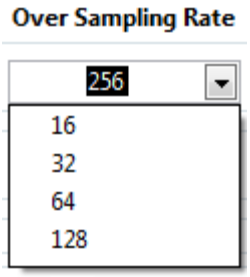


図 34. OSR Selection

- *Modulator Frequency*: This is a calculated value, which is the frequency of the clock signal given to the ΔΣ modulator. The modulator frequency depends on the PWM frequency and oversampling rate. Considering two samples are required for every PWM period, the required sampling rate is twice the PWM frequency. The modulator frequency is calculated as 2 × (PWM Frequency) × OSR. The two samples requirement is a suggestion; however, it can be changed depending on the application requirement. The modulator frequency is limited to 20 MHz.
- *Input Frequency*: Enter the frequency of the input clock or crystal on the board. The GUI uses this value along with the required modulator frequency to calculate the PLL configuration registers and clock dividers on the board.

7.7.2 Setting Filter Type

Select the desired filter type for each channel from the list shown in 図 35:

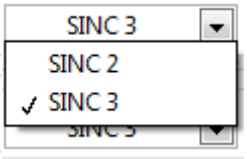


図 35. Channel Filter Type

7.7.3 Setting Default Value

Each channel can be configured to their default values using the *Default* button provided for each channel. The user can also use the *Default All* button to set default values to all the channels.

7.7.4 Configuration Summary

The configuration summary box gives the calculated modulator frequency for each channel. The modulator frequency has a limit of 5 MHz to 20 MHz. When the set values exceed the limit, the values are coerced and the summary box indicates the error with a notification, as 図 36 shows.

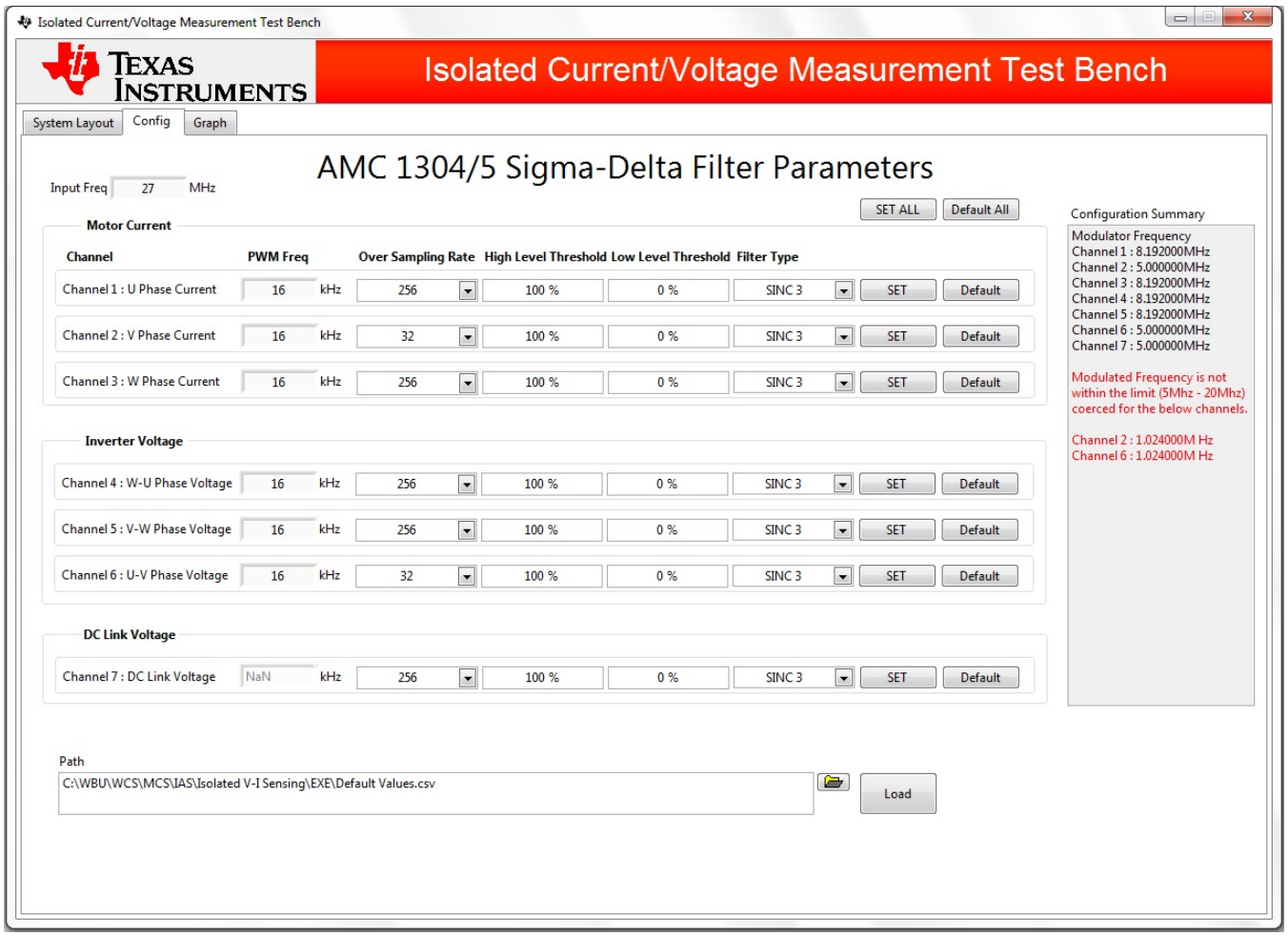


図 36. Configuration Summary

7.7.5 Loading Default Values File

Select the default values file using the available path control. Click on the *Load* button to load the settings to the user interface.

図 37. Load Default Values File

7.7.6 Setting Configuration

Set the final channel configuration by using the *Set* buttons provided with each channel or the *Set All* button to set the configurations of all the channels. When the *Set All* button is pressed, all the settings in the *Config* page are sent to the MCU as previously selected.

7.8 Graph Display for Measured Parameters

The *Graph* page is the result display and processing page (図 38). The captured values are displayed as graphs in this page in either the time domain or frequency domain.

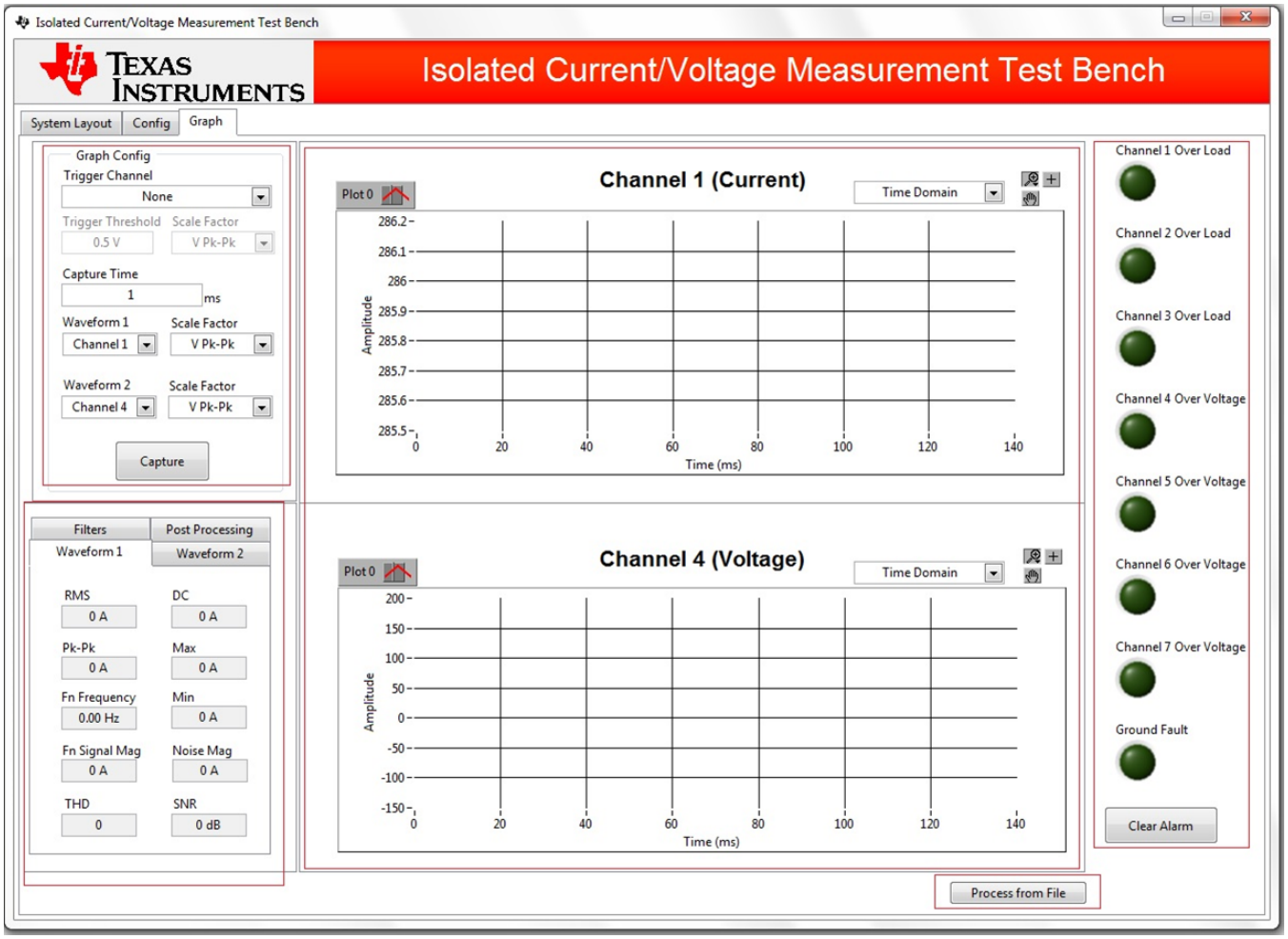


図 38. Graph Page

- *Graph Config*: This pane sets the trigger modes and selects the waveforms to display.
- *Waveform Parameter*: This pane displays the parameters of the selected waveform.
- *Graph Pane*: The captured data is plotted in the form of a graph in this pane.
- *Error Indicators*: The graph page has eight indicators to detail the error. The *Clear Alarm* button erases the indications.
- *Process from File*: This button plots the data from the file in a graph.

7.8.1 Setting Trigger Channel and Capture Time

The trigger channel can be set using the *Trigger Channel* control. Select any of the channels available. Set the trigger threshold of the selected channel in the *Trigger Threshold* control. The trigger channel and trigger threshold vales are sent to the target, where the target waits for the input on this channel to cross the trigger threshold value.

Select the scale factor from the *Scale Factor* control to calculate the digital value corresponding to the trigger threshold value (see 図 39).

Set the capture time in milliseconds (ms) in the *Capture Time* control. The maximum value is 100 ms, which is limited because of the amount of memory reserved for buffering the samples. The GUI can request for more than 100 ms, but the data will be clipped because of rollover from the buffer pointer inside the firmware of Sitara.

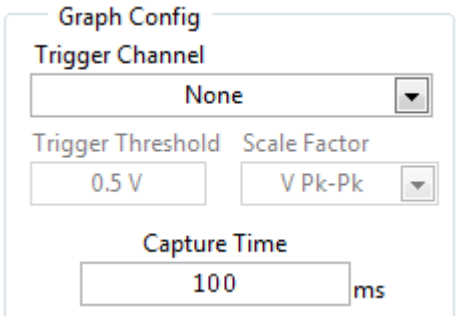


図 39. Trigger Configuration

7.8.2 Selecting Waveform and Scale Factor

The waveform to be displayed and its corresponding scale factors can be selected from the *Waveform 1* and *Waveform 2* control (see 図 40). The scale factors are selected from their respective controls. The scale factor here selects how the digital value received for the target corresponds to voltage or current values on the waveform.

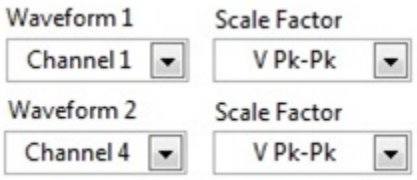


図 40. Waveform Settings

7.8.3 Selecting Filter

The *Filters* tab shows the post processing options that can be done by the GUI. Select the configuration from the *Filters* tab.

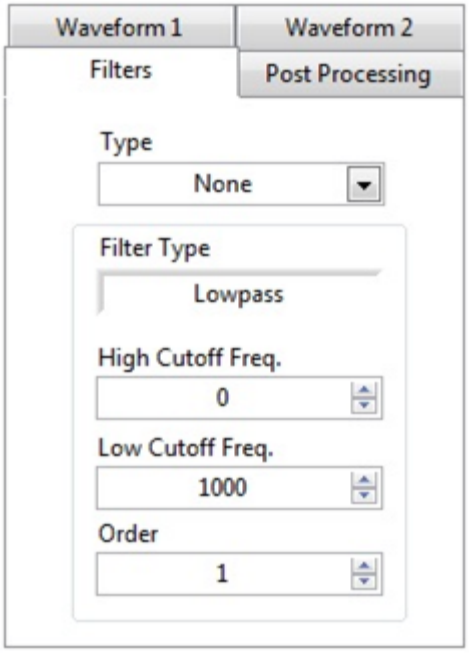


図 41. Filter Selection

The filter can be selected from the *Type* control.

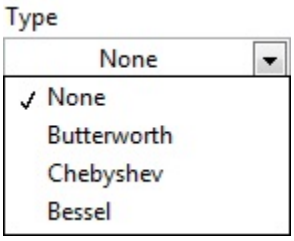


図 42. Filter Type Selection

The filter characteristics can be selected using the *Filter Type*, *High and Low Cutoff Freq*, and *Order* controls. The low-pass filter ignores the *High Cuttoff Freq* setting and the high-pass filter ignores the *Low Cutoff Freq* filter setting.

7.8.4 FFT Window Selection

FFT windows can be selected using the *FFT-Window* control in the *Post Processing* tab. This selection affects the FFT graph if the graph is selected to display FFT of the waveform captured (see 図 43).

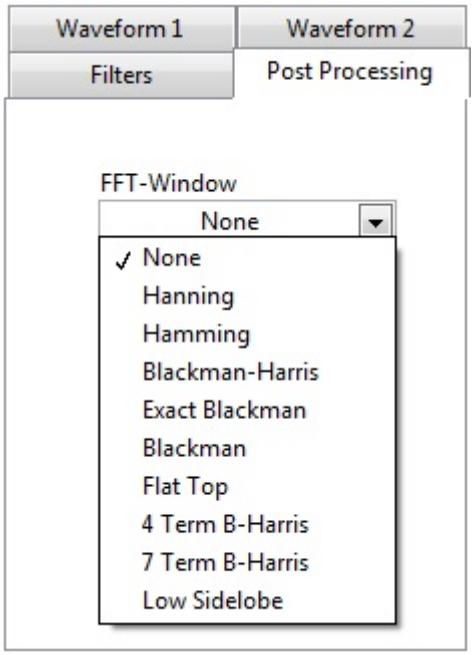


図 43. FFT Window Selection

7.8.5 Waveform Parameter Display

The parameters of the selected channel can be noted from the waveform page as in 図 44.

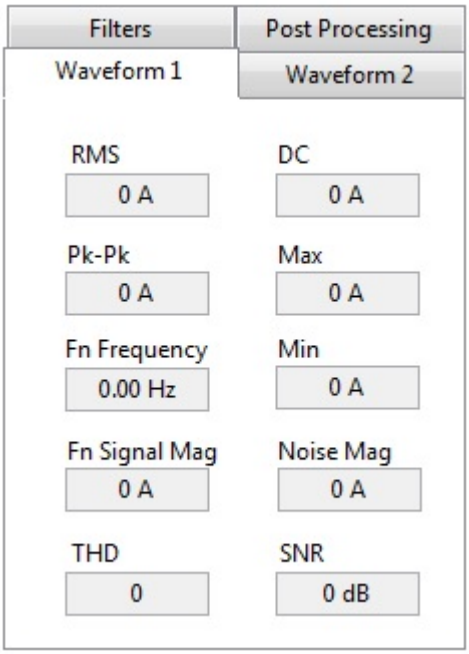


図 44. Waveform Parameter Display

7.8.6 Data Capture

Click on the *Capture* button shown in 図 45 to obtain the results.

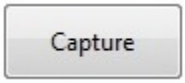


図 45. Data Capture Button

Capture mode sends the corresponding settings to the target, retrieves the data for the time specified, and displays it in the graph once.

7.8.7 Selecting Domain

Select the graph domain using the control provided for each graph and the time or frequency domain using the control as shown in 図 46.

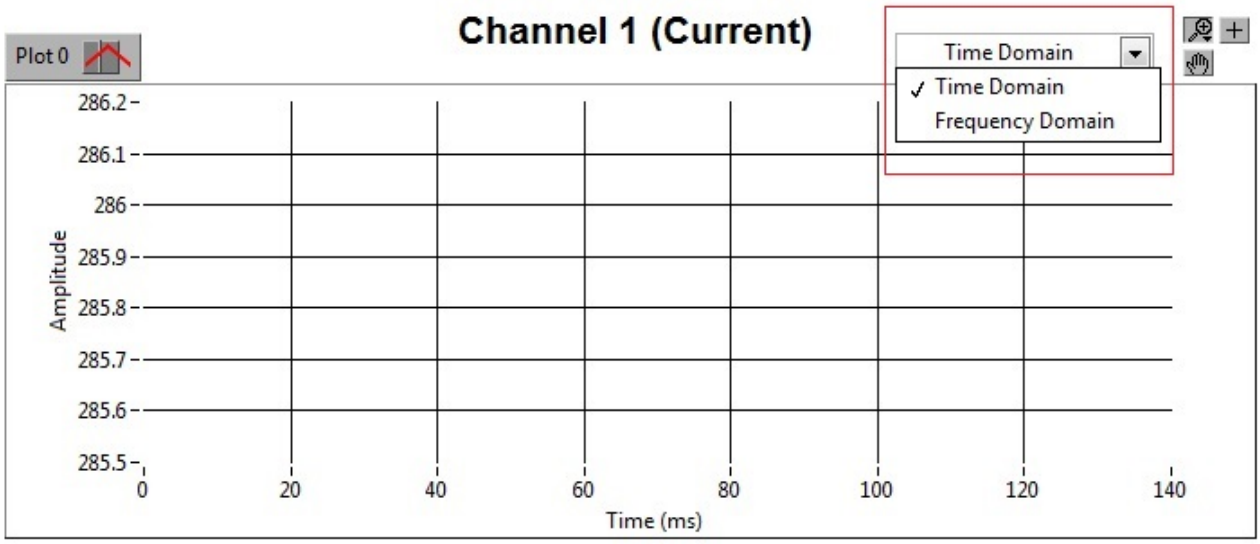


図 46. Graph Domain Selection

7.8.8 Waveforms

The following waveforms in 図 47 and 図 48 show current waveforms for high-gain and low-gain modulator paths.

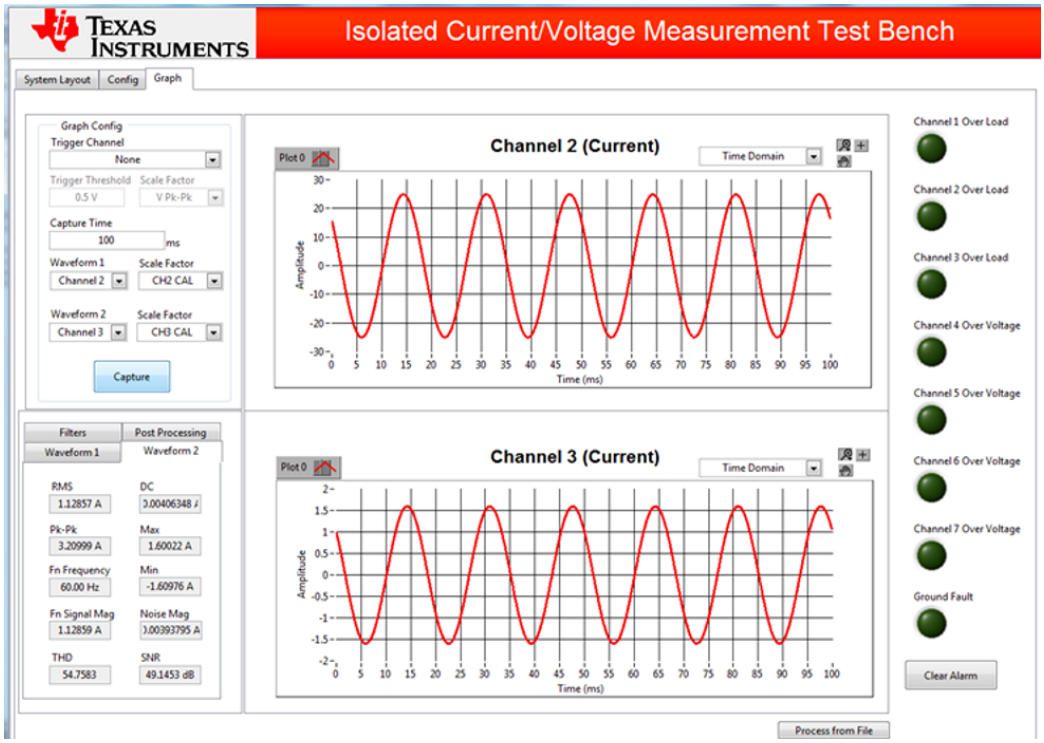


図 47. Current Input Waveform at 60 Hz

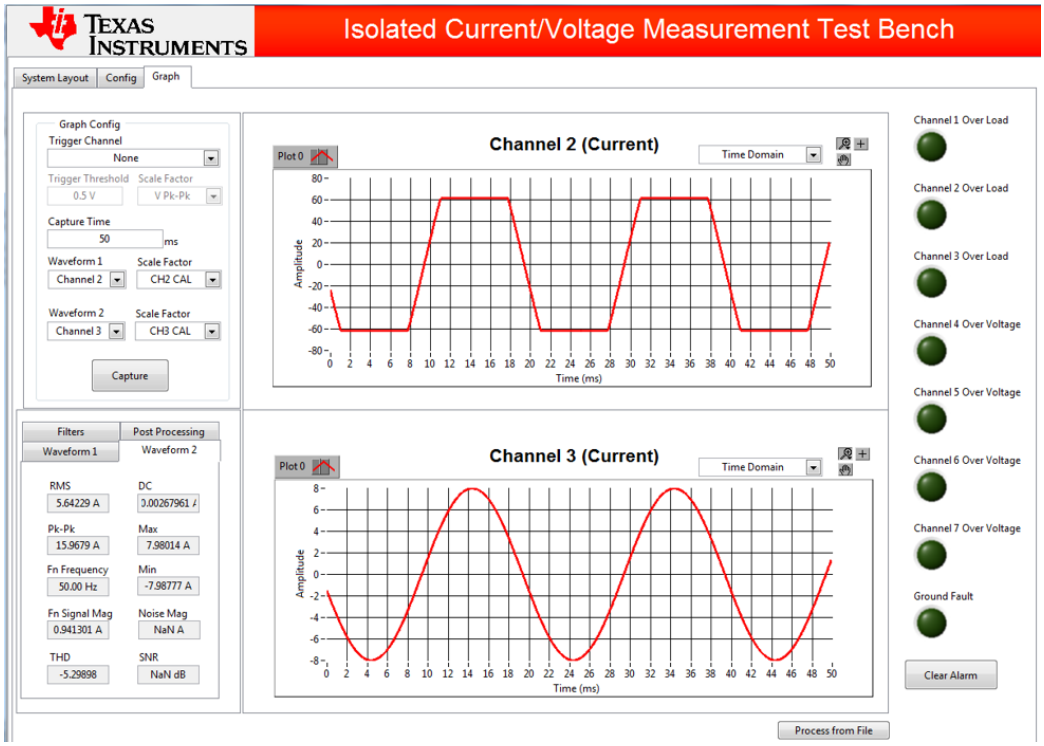


図 48. 10-A Input at High-Gain Modulator (Saturated) and Low-Gain Modulator

7.9 Layout Guidelines

- Modulator: Follow the layout design guidelines as recommended in the *Layout* section of the AMC1304Mx5 datasheet (SBAS655).
- Clock buffer: Follow the layout design guidelines as recommended in the *Layout* section of the CDCLVC1104 datasheet (SCAS895).
- Transformer driver for isolated power supplies: Follow the layout design guidelines as recommended in the *Layout* section of the SN6501 datasheet (SLLSEA0).
- Shunt: The current applied flows across the shunt and the current input terminal. Ensure proper copper flow to reduce the heating of the board.

7.10 Future Enhancements

Use of a higher shunt value:

Based on the application, if the design requires the use of a higher shunt, the gains of the amplifiers can be adjusted to vary the gain.

Measuring a wider current range:

The gain X 0.8 can be reduced further if the range of current to be measured is higher than 60 X In.

Configuring the design for a 5-A application:

This design can be used in applications with a 5-A nominal current by reducing the shunt value and adjusting the gain of the amplifiers.

8 Getting Started

8.1 EVM (IDK) Interface

The current inputs are connected using J4 and J5 terminals and the voltage input is connected using connector J1.

8.1.1 Connecting AFE and EVM (IDK)

表 7 shows the channels that are used for current and voltage measurement by the IDK.

表 7. GUI Channels for Current and Voltage Measurement

ADC OUTPUT	GUI CHANNEL SELECTED
High-gain stage AMC1304M05 output	Channel 2
Low-gain stage AMC1304M05 output	Channel 3
Voltage measurement AMC1304M25 output	Channel 6

注: Only two channels of data can be analyzed by the GUI at a given time.

8.1.2 Program the IDK

The firmware required for interfacing the AMC437X IDK with the modulator is provided as executables. Two files are generated after compilation in the release folder of the IDK: 'app' and 'MLO'. Copy the *app* and *MLO* executables in the micro-SD card available in connector J19 of the IDK.

8.1.3 Interface With AM437X IDK

図 49 shows how to connect the TIDA-00738 board to the AM437x IDK.

Align the connector J2 pin 1 on the TIDA-00738 board with the I/O expansion connector J16 pin 1 on the IDK. Press the J2 connector carefully in the I/O expansion connector J16 on the IDK while being cautious of ESD and mechanical strength.

図 50 shows the power and USB connections. J12 is the power connection and J18 is the USB connection.

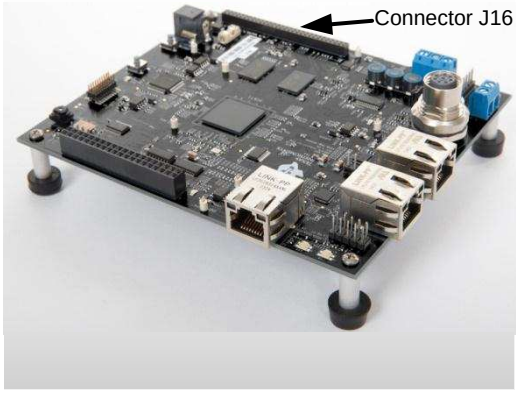


図 49. Connecting TIDA-00738 Board to AM437x IDK

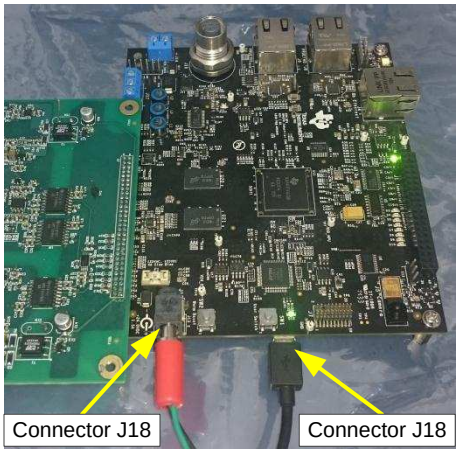


図 50. Power and USB Connection

注: The following steps are important to note before making any changes:

- Ensure that the power to the AM437X IDK has been switched off
- Be sure to insert the AFE connector into the correct position of the IDK connector

8.1.4 Powering AM437x and TIDA-00738 AFE Boards

Set the power supply to 24-V DC with a current limit of 300 mA. Connect the DC input to the 24-V DC power connector J12 on the AM437X IDK board. The light-emitting diodes (LEDs) on the TIDA-00738 board must be ON. The current shown in the power supply should be around 200 mA.

8.1.5 AM437X IDK USB Interface With GUI

Connect a USB cable between J18 and the GUI host computer to establish communication with the AM437X IDK.

8.1.6 Voltage and Current Input

Connect a programmable current source at J5 (M – Current In) and J4 (L – Current Out). Connect a programmable voltage source at connector J1 (Pin 1 – Phase and Pin 2 Neutral).

8.2 Setting Up Scale Factor for Measurement

8.2.1 Current

The GUI collects samples from the AM437X IDK after performing the Sinc3 filtering with the specified OSR. The GUI computes the RMS values using the samples. The samples are scaled to mV or the input values using a scaling factor. The modulator used for the current measurement is ±50 mV. The total full-scale range of the AMC1304M05 device is 62.5 mV to –62.5 mV. This range corresponds to a range of 32767 to –32768 for a 16-bit result register.

式 2 shows the conversion factor for mV:

$$\frac{\left(62.5\ \text{mV} - \left(-62.5\ \text{mV}\right)\right)}{\left(32767 - \left(-32768\right)\right)} = 0.0019073\ \text{mV/count} \tag{2}$$

Converting mV to input current:

This design uses a shunt value of 0.7 mΩ. The mV measured is converted to the input current as 式 3 shows:

$$\frac{0.0019073\ \text{mV/count}}{0.7\ \text{m}\Omega} = 0.002724825\ \text{A/count} \tag{3}$$

Because the high-gain stage provides an X 12.5 gain, the scale factor must be multiplied by 12.5. A high-gain modulator output is connected to channel 2 (GUI) of the AM437X IDK.

The scale factor for the high-gain stage channel 2 (GUI) is 0.000219621 A/ADC count.

The low-gain stage is connected to channel 3 (GUI) of the AM437X IDK. Because the low-gain stage provides an X0.8 gain, the scale factor must be multiplied by 0.8. The scale factor for the low-gain stage channel 3 (GUI) is 0.003380677 A/count.

8.2.2 Voltage

The modulator used for the voltage measurement is ±250 mV. The total full-scale range for the AMC1304M25 device is 312.5 mV to –312.5 mV. This range corresponds to a range of 32767 to –32768 for a 16-bit result register. 式 4 shows the conversion factor for mV:

$$\frac{(312.5\ \text{mV} - (-312.5\ \text{mV}))}{(32767 - (-32768))} = 0.0095362767\ \text{mV/count} \quad (4)$$

Converting to input voltage:

The potential divider ratio is 1: 0.000615; the applied voltage can be calculated by dividing the mV/count by the voltage divider factor. This calculation results in a 0.015515154-V/count. The voltage measurement channel is connected to channel 6 (GUI) of the AM437X IDK.

8.3 Test Setup for Voltage Input Measurement

図 51 shows the diagram of the test setup for measuring the AC voltage input. The test was performed using a 6½-digit multimeter as the reference meter. The test was also performed with a modulator clock configured at 5 MHz and a Sinc3 filter with an OSR of 128.

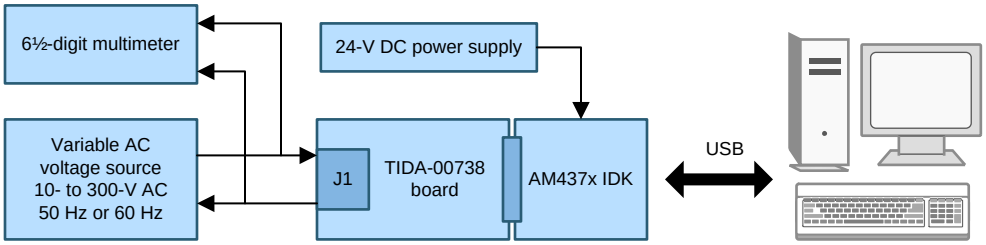


図 51. Test Setup for Voltage Measurement

8.4 Test Setup for Current Input Measurement

図 52 shows a diagram of the test setup for measuring the AC Current input. The test was performed using a 6½-digit multimeter as the reference meter. The test was also performed with a modulator clock configured at 5 MHz and a Sinc3 filter with an OSR of 128.

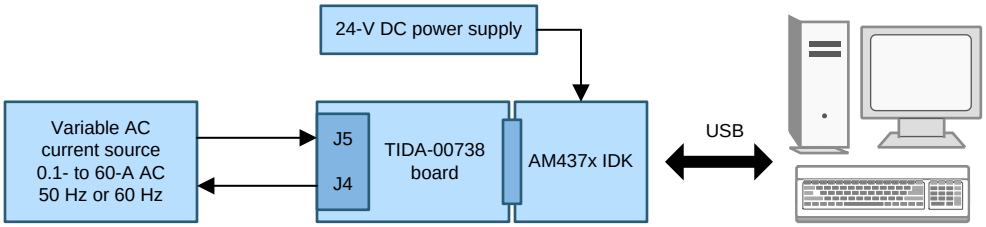


図 52. Test Setup for Current Measurement

9 Test Data

Sampling rate:

The modulator clock is 5 MHz and the OSR used is 128. The sampling rate is 39062.5 samples per second (5 MHz / 128).

The AFE can be used to measure to measure the following:

- Wide AC current input
- Wide DC current input
- Wide AC voltage input
- Wide DC voltage input
- Input frequency can be 50 Hz or 60 Hz

The single-ended measurement mode is used when measuring current and voltage.

Using a shunt provides the advantage of measuring AC or DC current. Similarly, using a resistor as the potential divider provides the advantage of measuring AC or DC voltage.

The data from two channels can be collected for analysis at a given time. In the TIDA-00378 design, three modulator inputs have been connected to the processor.

Test conditions for measuring voltage or current inputs:

The number of samples used for the computation of RMS current is 60 ms or 100 ms (three to five cycles at 50 Hz).

The number of samples used for the computation of RMS voltage is 100 ms (five cycles at 50 Hz).

Shunt value:

The AFE has been tested for accuracy performance with 0.7 mΩ and 1 mΩ.

Choosing the shunt value:

If the minimum current input to be measured within a specified accuracy is ≥ 100 mA, then 0.7 mΩ can be considered. For measuring lower currents, ≤ 50 mA, 1 mΩ is recommended.

表 8 shows a summary of the performance tests with the TIDA-00738 board.

表 8. Summary of Performance Tests

SERIAL NUMBER	TEST	DETAILS
1	Current measurement	Current measurement at 50 Hz with 0.7- and 1-mΩ shunts
		Current measurement at 60 Hz with 0.7-Ω shunt
		DC current measurement with 0.7-mΩ shunt
2	Voltage measurement	AC voltage measurement at 50 Hz and 60 Hz
		DC voltage measurement
3	Repeatability	Repeatability testing—power cycling and long-term stability
4	VA burden	VA burden for current input

9.1 Current Measurement

> **注:** The current input range used for testing the accuracy performance is based on a 1-A In. For an improved accuracy performance at lower currents, populate R64 and R64.

Two modulators have been used to ensure that the wide current input is measured within a specified accuracy.

- A modulator with a X 12.5 gain (amplifier output gain) is used to measure 0.1 A to 4 A. The result was monitored on channel 2 of the GUI.
- A modulator with X 0.8 gain is used to measure 1 A to 40 A (or 60 A). The result was monitored on channel 3 of the GUI.

The accuracy measurement was performed at the 50- and 60-Hz inputs.

9.1.1 Current Measurement at 50 Hz

表 9. Current Measurement at 50-Hz Input, 60-ms Sampling, and 0.7-mΩ Shunt

INPUT CURRENT	EXPECTED mV INPUT TO HIGH-GAIN MODULATOR	MEASURED	%ERROR_Hg	EXPECTED mV INPUT TO LOW-GAIN MODULATOR	MEASURED	%ERROR_Lg
0.050	0.434	0.4381	0.9405	—	—	—
0.075	0.651	0.6517	0.1105	—	—	—
0.10	0.868	0.8687	0.0837	—	—	—
0.20	1.736	1.7355	–0.0301	0.112	0.1125	0.4535
0.50	4.34	4.3430	0.0685	0.28	0.2805	0.1799
1.00	8.68	8.6902	0.1176	0.56	0.5606	0.1080
2.00	17.36	17.3823	0.1286	1.12	1.1221	0.1854
3.00	26.04	26.0766	0.1407	1.68	1.6828	0.1686
4.00	34.72	34.7719	0.1496	2.24	2.2439	0.1743
5.00	43.4	43.3390	–0.1406	2.8	2.8049	0.1757
6.00	52.08	47.6988	–8.4124	3.36	3.3659	0.1763
10.00	—	—	—	5.6	5.6098	0.1753
20.00	—	—	—	11.2	11.2206	0.1837
30.00	—	—	—	16.8	16.8289	0.1721
40.00	—	—	—	22.4	22.4193	0.0860
50.00	—	—	—	28	28.0066	0.0237
60.00	—	—	—	33.6	33.6205	0.0609

表 10. Current Measurement at 50-Hz Input, 100-ms Sampling, and 0.7-mΩ Shunt

INPUT CURRENT	EXPECTED mV INPUT TO HIGH-GAIN MODULATOR	MEASURED	%ERROR_Hg	EXPECTED mV INPUT TO LOW-GAIN MODULATOR	MEASURED	%ERROR_Lg
0.050	0.434	0.4366	0.6075	—	—	—
0.075	0.651	0.6523	0.2073	—	—	—
0.100	0.868	0.8673	–0.0791	—	—	—
0.200	1.736	1.7371	0.0617	0.112	0.1125	0.4366
0.500	4.34	4.3423	0.0531	0.28	0.2804	0.1373
1.000	8.68	8.6897	0.1123	0.56	0.5608	0.1512
2.000	17.36	17.3829	0.1320	1.12	1.1219	0.1721
3.000	26.04	26.0777	0.1449	1.68	1.6829	0.1704
4.000	34.72	34.7694	0.1423	2.24	2.2439	0.1748
5.000	43.4	43.3421	–0.1334	2.8	2.8050	0.1774
6.000	52.08	47.6998	–8.4105	3.36	3.3660	0.1795
10.000	—	—	—	5.6	5.6100	0.1780
20.000	—	—	—	11.2	11.2204	0.1819
30.000	—	—	—	16.8	16.8294	0.1751
40.000	—	—	—	22.4	22.4275	0.1229
50.000	—	—	—	28	28.0144	0.0514
60.000	—	—	—	33.6	33.6256	0.0763

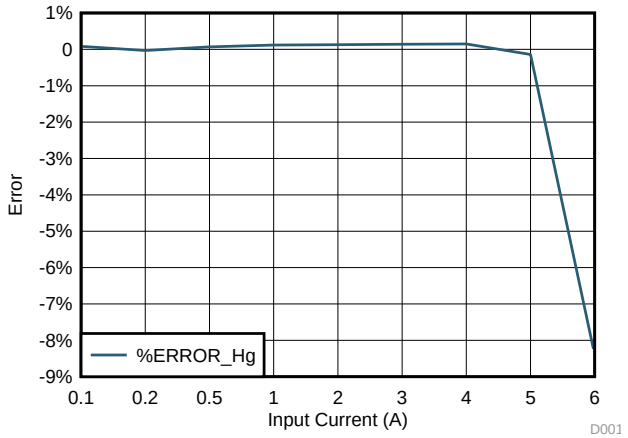


図 53. Current Measurement at 50-Hz Input, 60-ms Sampling Period, 0.7-mΩ Shunt, and High Gain

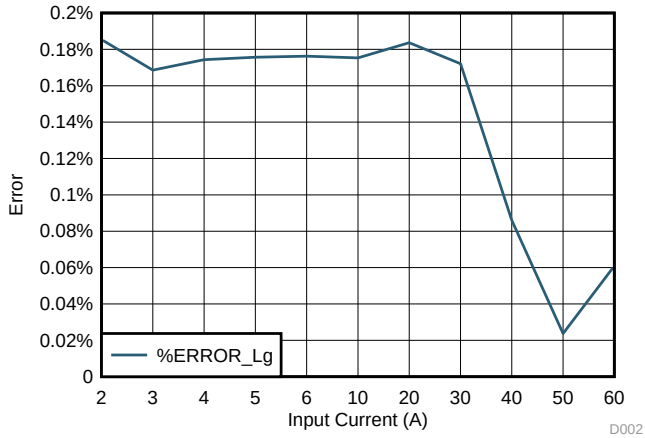


図 54. Current Measurement at 50-Hz Input, 60-ms Sampling Period, 0.7-mΩ Shunt, and Low Gain

Board testing with a 1-mΩ shunt:

表 11. Current Measurement at 50-Hz Input, 60-ms Sampling, and 1-mΩ Shunt

INPUT CURRENT	EXPECTED mV INPUT TO HIGH-GAIN MODULATOR	MEASURED	%ERROR_Hg	EXPECTED mV INPUT TO LOW-GAIN MODULATOR	MEASURED	%ERROR_Lg
0.050	0.62	0.6218	0.2978	—	—	—
0.075	0.93	0.9312	0.1274	—	—	—
0.100	1.24	1.2399	–0.0055	—	—	—
0.200	2.48	2.4813	0.0540	—	—	—
0.500	6.2	6.2005	0.0088	0.4	0.4003	0.0757
1.000	12.4	12.4035	0.0283	0.8	0.8007	0.0894
2.000	24.8	24.8100	0.0402	1.6	1.6016	0.0984
3.000	37.2	37.2139	0.0373	2.4	2.4024	0.1018
4.000	49.6	45.8367	–7.5873	3.2	3.2035	0.1101
5.000	—	—	—	4	4.0046	0.1160
6.000	—	—	—	4.8	4.8062	0.1302
10.000	—	—	—	8	8.0120	0.1506
20.000	—	—	—	16	16.0385	0.2407
30.000	—	—	—	24	24.0660	0.2751
40.000	—	—	—	32	32.1298	0.4056
50.000	—	—	—	40	40.2686	0.6715
60.000	—	—	—	48	45.6094	–4.9803

注: The error at higher current varies as a result of self heating on the shunt.

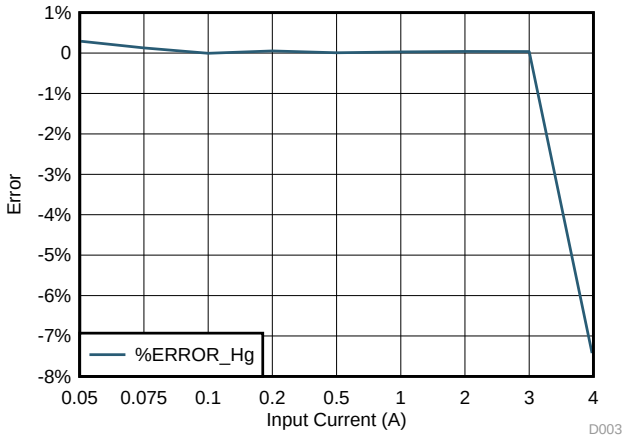


図 55. Current Measurement at 50-Hz Input, 60-ms Sampling Period, 1-mΩ Shunt, and High Gain

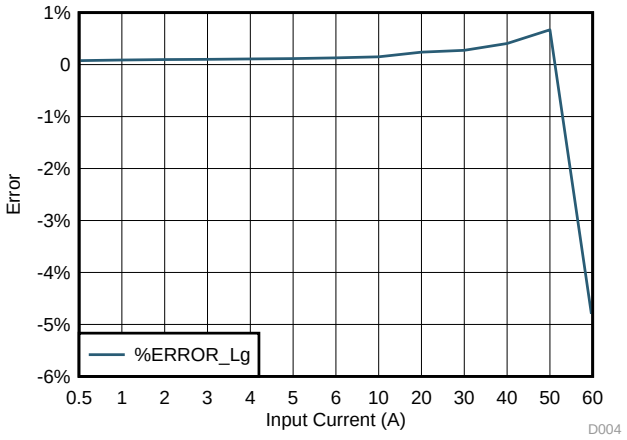


図 56. Current Measurement at 50-Hz Input, 60-ms Sampling Period, 1-mΩ Shunt, and Low Gain

9.1.2 Current Measurement at 60 Hz

表 12. Current Measurement at 60-Hz Input, 60-ms Sampling, and 0.7-mΩ Shunt

INPUT CURRENT	EXPECTED mV INPUT TO HIGH-GAIN MODULATOR	MEASURED	%ERROR_Hg	EXPECTED mV INPUT TO LOW-GAIN MODULATOR	MEASURED	%ERROR_Lg
0.050	0.434	0.4376	0.8273	—	—	—
0.075	0.651	0.6527	0.2604	—	—	—
0.10	0.868	0.8678	-0.0222	—	—	—
0.20	1.736	1.7363	0.0169	0.112	0.1123	0.2964
0.50	4.34	4.3426	0.0590	0.28	0.2804	0.1526
1.00	8.68	8.6885	0.0976	0.56	0.5611	0.1970
2.00	17.36	17.3796	0.1128	1.12	1.1219	0.1668
3.00	26.04	26.0711	0.1196	1.68	1.6827	0.1633
4.00	34.72	34.7630	0.1238	2.24	2.2437	0.1646
5.00	43.4	43.3299	-0.1615	2.8	2.8045	0.1590
6.00	52.08	47.6932	-8.4232	3.36	3.3654	0.1600
10.00	—	—	—	5.6	5.6093	0.1652
20.00	—	—	—	11.2	11.2190	0.1695
30.00	—	—	—	16.8	16.8274	0.1632
40.00	—	—	—	22.4	22.4265	0.1184
50.00	—	—	—	28	28.0016	0.0056
60.00	—	—	—	33.6	33.6213	0.0633

表 13. Current Measurement at 60-Hz Input, 100-ms Sampling, and 0.7-mΩ Shunt

INPUT CURRENT	EXPECTED mV INPUT TO HIGH-GAIN MODULATOR	MEASURED	%ERROR_Hg	EXPECTED mV INPUT TO LOW-GAIN MODULATOR	MEASURED	%ERROR_Lg
0.050	0.434	0.4363	0.5211	—	—	—
0.075	0.651	0.6517	0.1132	—	—	—
0.10	0.868	0.8675	–0.0544	—	—	—
0.20	1.736	1.7354	–0.0364	0.112	0.1122	0.2209
0.50	4.34	4.3433	0.0767	0.28	0.2804	0.1480
1.00	8.68	8.6883	0.0959	0.56	0.5610	0.1712
2.00	17.36	17.3805	0.1179	1.12	1.1218	0.1650
3.00	26.04	26.0729	0.1264	1.68	1.6827	0.1609
4.00	34.72	34.7602	0.1159	2.24	2.2433	0.1459
5.00	43.4	43.3363	–0.1467	2.8	2.8045	0.1622
6.00	52.08	47.6945	–8.4207	3.36	3.3657	0.1704
10.00	—	—	—	5.6	5.6092	0.1650
20.00	—	—	—	11.2	11.2195	0.1739
30.00	—	—	—	16.8	16.8254	0.1514
40.00	—	—	—	22.4	22.4260	0.1162
50.00	—	—	—	28	28.0074	0.0266
60.00	—	—	—	33.6	33.5981	–0.0057

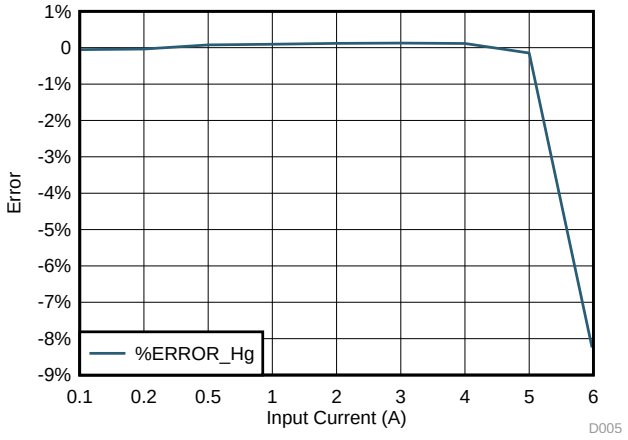


図 57. Current Measurement at 60-Hz Input, 100-ms Sampling Period, 0.7-mΩ Shunt, and High Gain

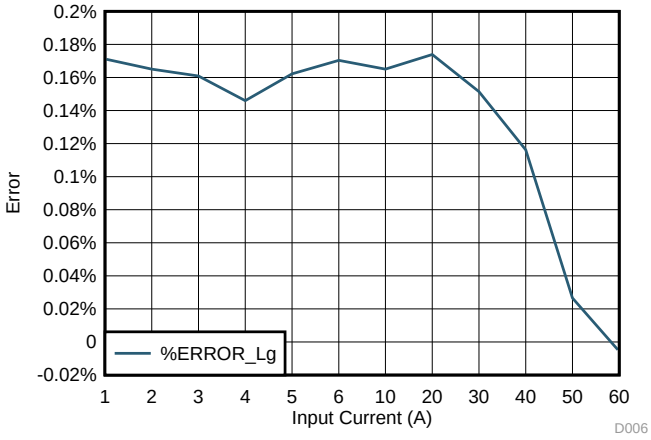


図 58. Current Measurement at 60-Hz Input, 100-ms Sampling Period, 0.7-mΩ Shunt, and Low Gain

9.1.3 DC Current Measurement

表 14. DC Current Measurement—High-Gain Stage With 100-ms Samples and 0.7-mΩ Shunt

CURRENT INPUT NORMAL			CURRENT INPUT REVERSED (NEGATIVE SIGN NOT SHOWN)				
INPUT CURRENT	GUI MEASUREMENT		INPUT CURRENT	GUI MEASUREMENT		AVERAGE	
IDC (A)	IDC (A)	%ERROR	IDC (A)	IDC (A)	%ERROR	CURRENT	%ERROR
0.051	0.0503	–0.3201	0.051	0.0513	1.5460	0.0508	0.6130
0.075	0.0752	–0.3004	0.075	0.0764	1.1996	0.0758	0.4496
0.100	0.1005	0.0226	0.100	0.1012	0.7550	0.1008	0.3888
0.200	0.2009	0.2078	0.200	0.2013	0.4292	0.2011	0.3185
0.500	0.5016	0.2263	0.500	0.5020	0.3131	0.5018	0.2697
1.000	1.0026	0.2607	1.000	1.0034	0.3380	1.0030	0.2993
2.000	2.0067	0.3325	2.000	2.0058	0.2923	2.0062	0.3124
3.000	3.0081	0.2697	3.000	3.0090	0.2986	3.0085	0.2841

9.1.3.1 Repeatability Testing With AC Current Input and Power Cycling of AFE Board

The repeatability testing was performed with a 2-A current using a modulator with a high-gain amplifier input.

Procedure:

- The board is powered up and a 2-A current is applied for 10 to 15 min.
- After 15 min of accuracy, the AFE is tested and the measurements are noted.
- The board DC input voltage is powered off for 5 min, including current input.
- The measurement cycle is repeated.

表 15. Repeatability Testing at 50-Hz High-Gain Stage With Samples Taken for 100 ms

BOARD STATUS	APPLIED CURRENT INPUT	GUI MEASUREMENT (A)	% ERROR
Reading Number 1			
Reading	2.0	2.0036	0.1827
Reading Number 2			
Reading	2.0	2.0034	0.1719
Reading Number 3			
Reading	2.0	2.003202	0.1600
Reading Number 4			
Reading	2.0	2.0033	0.1661
Reading Number 5			
Reading	2.0	2.0037	0.1890
Reading Number 6			
Reading	2.0	2.0035	0.1789

9.1.4 Repeatability Testing (Long-Term Stability) With AC Current Input

A constant current was applied and measurements were repeated every 15 min.

表 16. Repeatability Testing at 50-Hz Input, 100-ms Sampling

INPUT CURRENT	EXPECTED mV INPUT TO HIGH-GAIN MODULATOR	MEASURED	%ERROR_Hg	EXPECTED mV INPUT TO LOW-GAIN MODULATOR	MEASURED	%ERROR_Lg
3.0	26.0400	26.0754	0.1358	1.6800	1.6829	0.1704
3.0	26.0400	26.0765	0.1400	1.6800	1.6826	0.1556
3.0	26.0400	26.0771	0.1426	1.6800	1.6829	0.1733
3.0	26.0400	26.0765	0.1400	1.6800	1.6827	0.1621
3.0	26.0400	26.0759	0.1377	1.6800	1.6827	0.1627
3.0	26.0400	26.0772	0.1430	1.6800	1.6828	0.1674
3.0	26.0400	26.0765	0.1400	1.6800	1.6828	0.1668
3.0	26.0400	26.0775	0.1441	1.6800	1.6826	0.1562
3.0	26.0400	26.0771	0.1426	1.6800	1.6828	0.1662
3.0	26.0400	26.0782	0.1468	1.6800	1.6829	0.1698

注: The variation is less than 0.1% for measurements that were taken for more than two hours.

9.1.5 VA Burden for Current Input (Power Dissipation Across Shunt at Nominal Current In of 1 A)

表 17. Shunt Input VA Measurement

PARAMETER	VALUE
Expected burden at 1-A In	< 0.1 VA
Measured VA drop for 0.7 mΩ	0.0007 VA (0.7 mΩ × 1 A = 0.7 mVA)
Measured VA drop for 1 mΩ	0.001 VA (1 mΩ × 1 A = 1 mVA)

9.2 Voltage Measurement

A ±250-mV input-rated modulator was used to measure the AC voltage input. The result was monitored on channel 6 of the GUI. The voltage was applied across the onboard potential divider to enable a direct connection of voltage up to 300 V.

9.2.1 AC Voltage Measurement

表 18. Voltage Measurement at 50-Hz Input and 60-ms Sampling

INPUT VOLTAGE	EXPECTED mV INPUT TO MODULATOR	MEASURED	%ERROR
1.000	0.615	0.6142	–0.1332
2.500	1.5375	1.5360	–0.0995
5.000	3.075	3.0717	–0.1067
10.000	6.15	6.1456	–0.0723
25.000	15.375	15.3627	–0.0798
50.000	30.75	30.7311	–0.0615
100.000	61.5	61.4766	–0.0381
150.000	92.25	92.2343	–0.0170
200.000	123	123.0046	0.0038
250.000	153.75	153.7943	0.0288
300.000	184.5	184.5990	0.0537
325.000	199.875	199.9858	0.0554
350.000	215.25	215.3957	0.0677

表 19. Voltage Measurement at 60-Hz Input and 60-ms Sampling

INPUT VOLTAGE	EXPECTED mV INPUT TO MODULATOR	MEASURED	%ERROR
1.000	0.615	0.6143	–0.1109
2.500	1.5375	1.5364	–0.0746
5.000	3.075	3.0711	–0.1279
10.000	6.15	6.1442	–0.0944
25.000	15.375	15.3624	–0.0818
50.000	30.75	30.7238	–0.0851
100.000	61.5	61.4573	–0.0694
150.000	92.25	92.2171	–0.0357
200.000	123	122.9825	–0.0142
250.000	153.75	153.7731	0.0150
300.000	184.5	184.5688	0.0373
325.000	199.875	199.9616	0.0433
350.000	215.25	215.3766	0.0588

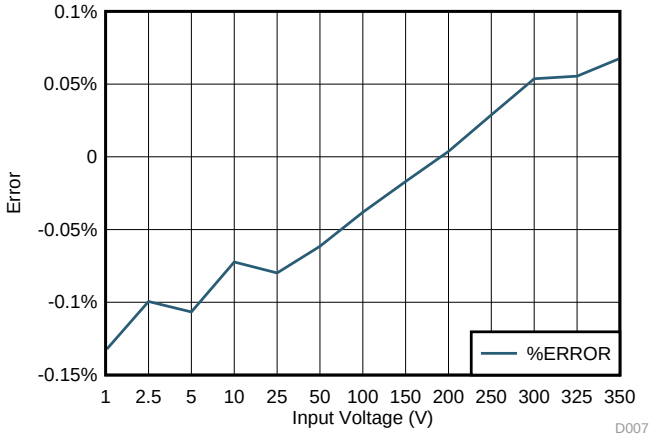


図 59. Voltage Measurement at 50-Hz Input and 60-ms Sampling

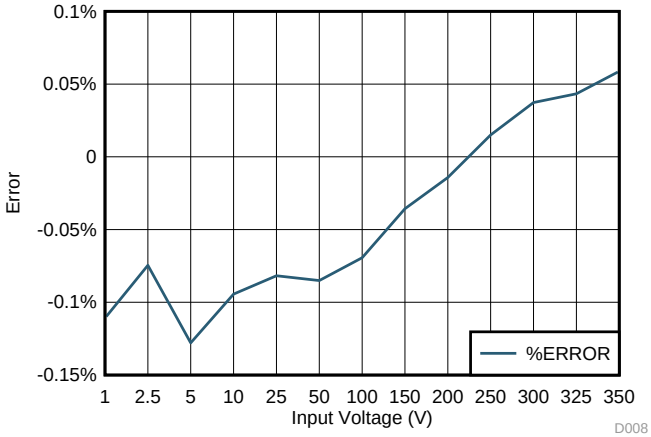


図 60. Voltage Measurement at 60-Hz Input and 60-ms Sampling

Accuracy testing for second board:

表 20. Voltage Measurement at 50-Hz Input and 60-ms Sampling

INPUT VOLTAGE	EXPECTED INPUT mV TO MODULATOR	MEASURED	%ERROR
1.000	0.615	0.613629	–0.22295
2.500	1.5375	1.536675	–0.05365
5.000	3.075	3.073672	–0.04319
10.000	6.15	6.147233	–0.04499
25.000	15.375	15.36675	–0.05365
50.000	30.75	30.73672	–0.04319
100.000	61.5	61.48429	–0.02554
150.000	92.25	92.25619	0.006706
200.000	123	123.0411	0.033451
250.000	153.75	153.8474	0.063356
300.000	184.5	184.6708	0.092553
325.000	199.875	200.0875	0.106296
350.000	215.25	215.5102	0.120878

9.2.2 DC Voltage Measurement

The TIDA-00738 TI Design can be used for DC measurement. 表 21 shows the test results for DC voltage measurement.

表 21. DC Voltage Measurement at 60 ms

VOLTAGE INPUT (+ THEN –)			VOLTAGE INPUT (– THEN +)		
V_{IN}	GUI MEASUREMENT		V_{IN}	GUI MEASUREMENT	
V-DC (V)	V-DC (V)	%ERROR	V-DC (V)	V-DC (V)	%ERROR
10.075	10.07	0.027	–10.045	–10.08	–0.358
20.055	20.06	–0.032	–20	–20.05	–0.251
30.054	30.08	–0.086	–30.075	–30.14	–0.202
40.035	40.07	–0.092	–40.039	–40.12	–0.196
100.071	100.21	–0.136	–100.045	–100.22	–0.179
110.085	110.24	–0.144	–110.093	–110.29	–0.181
120.025	120.20	–0.147	–120.05	–120.27	–0.185
130.045	130.24	–0.148	–130.04	–130.28	–0.184
220.06	220.47	–0.186	–220	–220.47	–0.212
240.09	240.56	–0.195	–240	–240.52	–0.216
280	280.62	–0.220	–280.09	–280.73	–0.230
300.09	300.75	–0.219	–300.06	–300.77	–0.236

9.3 Summary of Test Results

表 22. Test Results Summary

SERIAL NUMBER	MEASUREMENT PARAMETER	VALUE		FREQUENCY (Hz)	SAMPLING TIME	RESULT
		MIN	MAX			
1	Current AC (A)	0.1	5	50 or 60	3 or 5 cycles	<± 0.5%
		1	40 (or 60)	50 or 60	3 or 3 cycles	<± 0.5%
2	Voltage AC (V)	10	300	50	5 cycles	<± 0.5%
		10	300	60	5 cycles	<± 0.5%
3	Repeatability testing with power cycling AC current (A)	2		50	5 cycles	<± 0.5%
4	Power supply testing					
	Isolated power for current measurement	+5 V isolated		N/A	N/A	OK
		±2.5 V Isolated		N/A	N/A	OK
	Isolated power for voltage measurement	+5 V isolated		N/A	N/A	OK
		±2.5 V Isolated		N/A	N/A	OK
5	DC current measurement	OK				
6	DC voltage measurement	OK				

10 Design Files

10.1 Schematics

To download the schematics for each board, see the design files at TIDA-00738.

10.2 Bill of Materials

To download the Bill of Materials (BOM), see the design files at TIDA-00738.

10.3 Layout Prints

To download the layout prints for each board, see the design files at TIDA-00738.

10.4 Altium Project

To download the Altium project files for each board, see the design files at TIDA-00738.

10.5 Gerber Files

To download the Gerber files for each board, see the design files at TIDA-00738.

10.6 Assembly Drawings

To download the assembly drawings for each board, see the design files at TIDA-00738.

11 References

1. Texas Instruments, *Isolated Current (Shunt-Based) and Voltage Sensing for Smart Grid Applications*, TIDA-00080 Design Guide (TIDU429)
2. Texas Instruments, *Isolated Current Shunt and Voltage Measurement Kit*, TIDA-00171 Design Guide (TIDU499)
3. Texas Instruments, *AM437x SYSBIOS Industrial SDK 02.00.00.02 User Guide*, Wiki (http://processors.wiki.ti.com/index.php/AM437x_SYSBIOS_Industrial_SDK_02.00.00.02_User_Guide)
4. Texas Instruments, *Isolated Current Shunt and Voltage Measurement for Motor Drives Using AM437x*, TIDA-00209 Design Guide (TIDU755)

12 Terminology

AFE— Analog front end

CT— Current transformer

IDK— Industrial development kit

IED— Intelligent electronic device

PD— Potential divider

PRU-ICSS— Programmable Real-Time Unit Subsystem

In— Nominal current

LVCMOS— Low-voltage complementary metal-oxide semiconductor

13 About the Author

AMIT KUMBASI is a systems architect at Texas Instruments Dallas where he is responsible for developing subsystem solutions for Grid Infrastructure within Industrial Systems. Amit brings to this role his expertise with defining products, business development, and board level design using precision analog and mixed-signal devices. He holds a Master's in ECE (Texas Tech) and an MBA (University of Arizona). He can be reached at amit-kg@ti.com.

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お客様は、個別のTIリソースにつき、当該TIリソースに記載されているTI製品を含むアプリケーションの開発に関連する目的でのみ、使用、コピー、変更することが許可されています。明示的または黙示的を問わず、禁反言の法理その他どのような理由でも、他のTIの知的所有権に対するその他のライセンスは付与されません。また、TIまたは他のいかなる第三者のテクノロジまたは知的所有権についても、いかなるライセンスも付与されるものではありません。付与されないものには、TI製品またはサービスが使用される組み合わせ、機械、プロセスに関連する特許権、著作権、回路配置利用権、その他の知的所有権が含まれますが、これらに限られません。第三者の製品やサービスに関する、またはそれらを参照する情報は、そのような製品またはサービスを利用するライセンスを構成するものではなく、それらに対する保証または推奨を意味するものでもありません。TIリソースを使用するため、第三者の特許または他の知的所有権に基づく第三者からのライセンス、あるいはTIの特許または他の知的所有権に基づくTIからのライセンスが必要な場合があります。

TIのリソースは、それに含まれるあらゆる欠陥も含めて、「現状のまま」提供されます。TIは、TIリソースまたはその仕様に関して、明示的か暗黙的かにかかわらず、他のいかなる保証または表明も行いません。これには、正確性または完全性、権原、続発性の障害に関する保証、および商品性、特定目的への適合性、第三者の知的所有権の非侵害に対する黙示の保証が含まれますが、これらに限られません。

TIは、いかなる苦情に対しても、お客様への弁護または補償を行う義務はなく、行わないものとします。これには、任意の製品の組み合わせに関連する、またはそれらに基づく侵害の請求も含まれますが、これらに限られず、またその事実についてTIリソースまたは他の場所に記載されているか否かを問わないものとします。いかなる場合も、TIリソースまたはその使用に関連して、またはそれらにより発生した、実際的、直接的、特別、付随的、間接的、懲罰的、偶発的、または、結果的な損害について、そのような損害の可能性についてTIが知らされていたかどうかにかかわらず、TIは責任を負わないものとします。

お客様は、この注意事項の条件および条項に従わなかったために発生した、いかなる損害、コスト、損失、責任からも、TIおよびその代表者を完全に免責するものとします。

この注意事項はTIリソースに適用されます。特定の種類の資料、TI製品、およびサービスの使用および購入については、追加条項が適用されます。これには、半導体製品(http://www.ti.com/sc/docs/stdterms.htm)、評価モジュール、およびサンプル(http://www.ti.com/sc/docs/sampterms.htm)についてのTIの標準条項が含まれますが、これらに限られません。