参考資料

デザイン・ガイド: TIDA-00929
スペクトラム・アナライザ: アーク・シグネチャ・キャプチャ用信号コンディショニングおよび処理のリファレンス・デザイン

概要

このデザインでは、広い周波数帯域のスペクトラムを低消費電力でキャプチャするよう最適化された、帯域幅最適化のアナログ・フロントエンド (AFE) およびリアルタイム FIR 実装を紹介します。各信号パスのオペアンプは、ゲイン、信号帯域幅、低ノイズ、レール・スイングの要件と、低消費電力に基づいて選択されています。波形は、数学エンジンが組み込まれたミクスト・シグナル・プロセッサにより、周波数ドメインと時間ドメインの両方で処理されます。周波数成分は次のように分析されます。

- 特定の周波数帯用に、両方の信号パスを最適化します。
- ADCのデータ・キャプチャ速度を、内部のメモリと一致させ、最適な周波数分析を行います。
- 非同期タイマを使用して、時間ドメインの分析を行います。

リソース

TIDA-00929	デザイン・フォルダ
MSP430FR5994	プロダクト・フォルダ
OPA835	プロダクト・フォルダ
OPA836	プロダクト・フォルダ
TLV316	プロダクト・フォルダ
UCC28880	プロダクト・フォルダ
LP5907	プロダクト・フォルダ
TLV3202	プロダクト・フォルダ
TPS3820	プロダクト・フォルダ

TI E2E™ Community　E2E™エキスパートに質問

特長

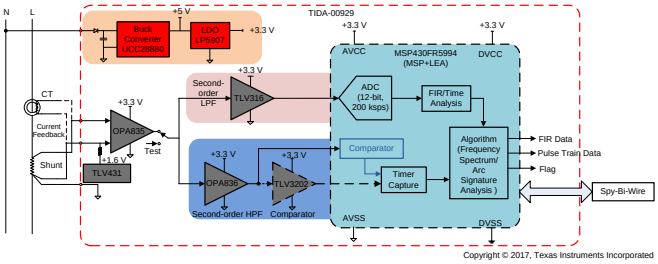
- AFE により、低周波の信号と高周波のフォルトの両方を効果的に送信し、同時にノイズを抑制
- 周波数スペクトラム分析: LEA (Low Energy Accelerator) を使用して、MSP430™内で 最高 200ksps (12ビット SAR ADC) のデータ・キャプチャ速度と、リアルタイムの FIR フィルタリングを実現
- 高周波のノイズおよび過渡事象検出:過渡およびアーク・シグネチャの捕捉
  - MSP430 の内部コンパレータを使用して最高 3MHz
  - 外部コンパレータを使用して最高 10MHz
- 単相 AC K (85～270V_{RMS}) から最大 10mA の I_Q、100mA に拡張可能
- 変流器、計器用変圧器、シャントなど各種の入力センサと互換

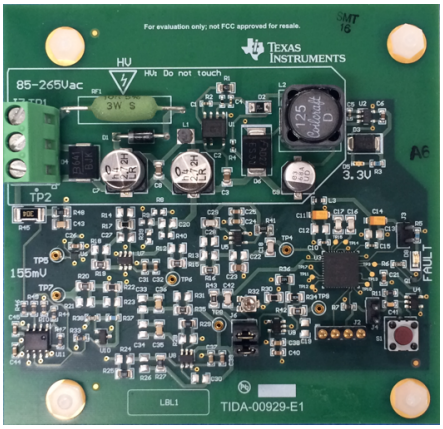
アプリケーション

- アーク・フォルト電流断続器 (住居用または産業用)
- 電圧電源での周波数補償
- 測定および保護:信号測定時の過渡スパイクの検出

注

このデザインは、アークを表す単一の波形について、周波数成分を捕捉し分析するサブシステムです。これは完全なソリューションではなく、安全規格を満たすための認定プロセスも行われていません。このデザインは情報を処理する最適な方法を示してはいますが、リファレンス・デザインとしてのみ意図されたもので、お客様は最終的なアプリケーションで使用する前に独自の機能を組み込み、正しい動作を検証し、標準化ラボで認定を受けるため、妥当な作業を行う必要があります。





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1 System Description

Some applications in grid infrastructure require simultaneous measurements of signal and detection of fault conditions. This includes equipment such as arc fault circuit interrupters, transient fault recorders, arc flash sensors, breakers, and so on. While the fundamental signal is lower in frequency, the faults and transients have frequencies that are much higher order in magnitude. Designing a data acquisition card for such an application requires optimization for performance and speed, which are often conflicting. It gets further distorted by the fluctuations introduced by load switching and due to the reactive loads.

Arcing is one such event where high energy arc condition has to be detected while the fundamental signal is being monitored. An arc could be a series or a parallel arc. A series arc is generated when a cable, in series with the load, creates low resistance path as insulation wears off. Under such a condition, the fault current cannot be greater than the load current that the conductor serves. Even though the current levels are small and within the rating of the outlet, this may result in damages to the property and life. Parallel arc fault is more dangerous where either line-neutral or line-ground has short circuit, resulting in higher currents in the cable. Again, this can result from weak insulation or damage caused to the wire. Parallel arc further carbonizes the wire insulation, resulting in greater damages.

Detecting such faults is challenging as "operational arcs" can result in similar signature as arcs due to series or parallel faults. Appliances that contain motors (such air compressors) have huge spikes in inrush current during start-up. Vacuum cleaners have comparatively smaller inrush current; however, draw distorted current waveform from the mains. Electric drills generate noise in the line that looks closer to operational arcs, which is enough to be detected by the broadband RF detector. Newer loads such as LEDs and dimmers can generate spikes in currents and introduce distortion that when analyzed have frequency similar to that of arc faults.

This TI Design shows a novel way of conditioning certain aspects of the signal based on customers band of interest and to analyze the spectrum using the following:

- Analog front-end: This device uses current signal taken from a wide bandwidth current sensor and provides appropriate signal filtering and conditioning prior to data acquisition. This action gives users the flexibility in narrowing down to the frequency of interest and optimizing the gain for that band.
- Digital signal processing: This signal is conditioned in analog domain and is digitized to capture various

attributes of the waveform. This gives users the flexibility in terms of tuning the programming and changing the algorithm without having to change the hardware.

1.1 Arc Fault Capture

Solutions that detect arc faults are available in two forms: breakers and receptacles. Both solutions are designed to sense arc faults under various load conditions. They house a solenoid to interrupt the circuit when an arc event is detected. They are designed for very small form factors and must withstand high temperatures.

- Current measurement: These solutions are designed to measure one-phase line currents up to 100 A, with a nominal frequency of 50 or 60 Hz (±10%). Some of the solutions also include measuring ground fault current, which measures leakage currents up to 5 mA, with a nominal frequency of 50 or 60 Hz (±10%).
- Signal processing: This process can be implemented either using the digitized signal from the ADC or by a comparator. Cost is one of the primary drivers that decides which of these two options is used. Digitizing the waveform using ADC can be expensive, but any frequency band can be analyzed using this approach. The comparator provides the lowest cost solution but has limitations as some of the signal information is lost after the comparator output.
- Arc fault sensing: Irrespective of the methodology used, each customer has a specific frequency spectrum that can be used to identify signatures that are unique to arc faults. Advanced algorithms are also implemented in the firmware to make it highly selective for arc faults while rejecting operational arcs.
- Power supply: There are multiple ways of deriving DC power supply from a single-phase AC source. Commonly used methods are capacitor-drop supply or diode rectifier followed by off-line DC-DC converters. Off-line converters are better in terms of efficiency when converting line supply to DC voltage.
- Circuit interrupt: A solenoid is driven to interrupt the load from the line. An action is taken only when certain conditions are met, which indicates a true arcing condition.
- Test mode: An alternate path is provided and used to verify the working of various subsystems. In order to verify the interrupt mechanism, a test signal is generated with certain frequency to which the circuit is tuned.

This TI Design is focused only on the subsystem that is used for measuring line currents and for detecting arc signatures.

1.2 Transient and Fault Detector

Applications such as fault recorders in power quality analyzers are designed for capturing short transient faults and disturbances in addition to measuring line signal at 256, 512, and 1024 samples per cycle for harmonic, frequency, and power analysis. These end equipment require an ADC sampling at high data rates to capture the signal information (1024 samples for 50 or 60 Hz ±10%). In addition, they are often designed to capture waveform and time information when such disturbances occur. Fault recorders detect transients as short as 20 μs at 50 Hz (17 μs at 60 Hz) to identify problems as a result of short disturbances (for example, the switching of capacitors and so forth).

Transient recorders are used to detect impulsive or oscillatory transients, which are unipolar or bipolar voltage or current waveforms. IEC 61000-4-5 standard defines surge waveforms as 1.2×50 µs for an open-circuit voltage and 8×20-µs for a short-circuit current. The open-circuit voltage waveform has a front time of 1.2 µs and time-to-half value of 50 µs. The short-circuit current waveform of the same generator has a 8-µs front time and a 20-µs time-to-half value as shown in the TIDA-00499 design.

As shown in this TI Design, a spectrum analyzer can be used for both continuously sampling the input waveform and for detecting high frequency content from transient faults. In the event where only faults have to be detected and recorded, the same can be used to keep the current consumption low. This can be done by optimizing a path for detecting high frequency transient bursts and using that as a trigger to capture the data using the ADC while the CPU is in the low power mode.

1.3 Circuit Breaker

A circuit breaker acts as an electrical switch that protects expensive electrical end equipment and circuits from damage when it detects faults. These faults could be due to a short-circuit or an overload condition. Fault recording and event logging is an essential function that breakers perform beyond measurement and metering capabilities. A typical architecture includes an MSP with an integrated ADC for monitoring current and voltage levels during normal working conditions. One of the common challenges occurs right after the breakers trip. Once the faults are cleared, the breakers are required to detect a presence or absence of faults as soon as they are powered on.

This TI Design shows one way to address this issue. The branch with a faster response time can be used for detecting fault conditions, which can then serve as one of the inputs for the tripping unit. The other path can be used for measurement and metering purposes.

1.4 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Type of current sensor (external)	Shunt, CT, or Rogowski coil	2.3.1
Current sensor input	±155-mV peak	2.3.1
AC line voltage	85- to 265-V_{RMS}, 50 or 60 Hz	2.3.3
Frequency domain analysis	Maximum frequency: 100-kHz Resolution: 0.08 mV at the input voltage	2.3.1.2
Time domain analysis:	Frequency: 100 kHz to 10 MHz	2.3.1.3
Option 1	Using internal comparator: up to 3 MHz	2.3.1.4.1
Option 2	Using external comparator: up to 10 MHz	2.3.1.4.2
Supply voltage surge	4 kVp 1.2 × 50 µs	2.3.3

2 System Overview

2.1 Block Diagram

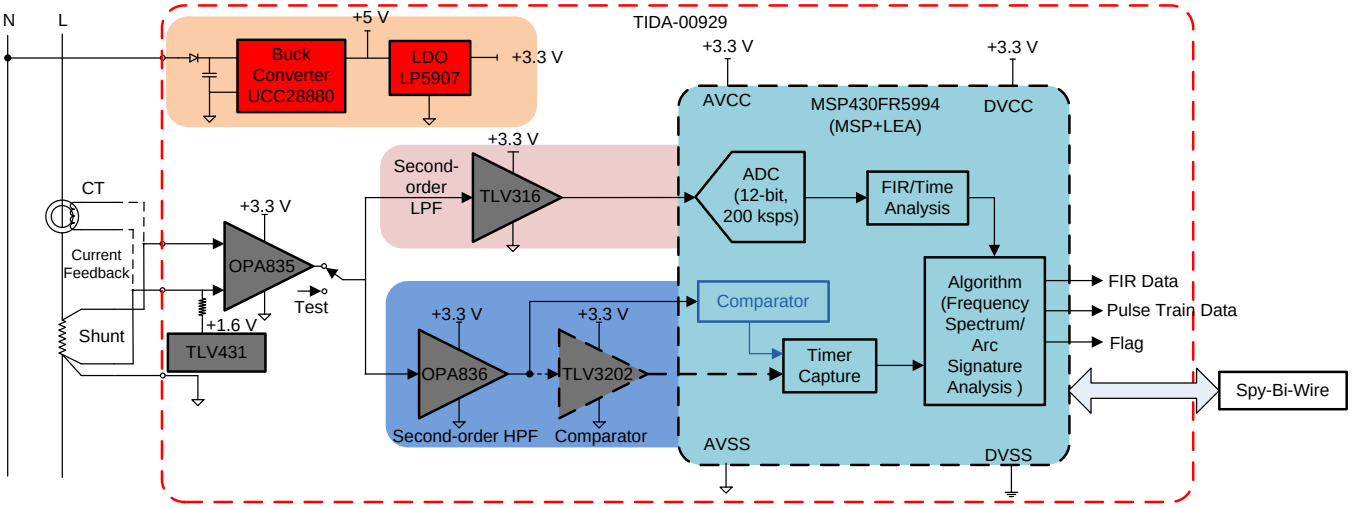


図 1. System Block Diagram of TIDA-00929

2.2 Highlighted Products

2.2.1 OPA835: Ultra-Low-Power Op Amp

The OPA835 is a single-channel ultra-low-power, rail-to-rail output (RRO), negative-rail input, voltage-feedback (VFB) operational amplifier designed to operate over a power supply range of 2.5 to 5.5 V with a single supply, or ±1.25 to ±2.75 V with a dual supply. Consuming only 250 µA per channel and with a unity gain bandwidth of 56 MHz, this amplifier sets an industry-leading performance-to-power ratio for rail-to-rail amplifiers.

For applications where power consumption is of key importance, the low-power consumption and high-frequency performance of the OPA835 device offers performance versus power that is not attainable in other devices. Coupled with a power-savings mode to reduce current to < 1.5 µA, these devices offer an attractive solution for high-frequency amplifiers in battery powered applications. The OPA835 device is characterized to operate over the extended industrial temperature range of –40°C to 125°C.

Key features of this device include:

- Ultra-low-power:
  - Supply voltage: 2.5 to 5.5 V
  - Quiescent current: 250 µA/ch (typical)
  - Power down mode: 0.5 µA (typical)
- Bandwidth: 56 MHz (A_V = 1 V/V)
- Slew rate: 160V/µs
- SNR: 0.00015% (–116.4 dBc) at 1 kHz (1 V_{RMS})
- THD: 0.00003% (–130 dBc) at 1 kHz (1 V_{RMS})
- Input voltage noise: 9.3 nV/√Hz (f = 100 kHz)
- Input offset voltage: 100 µV (±500-µV maximum)
- RRO
- Input voltage range: –0.2 to 3.9 V (5-V supply)

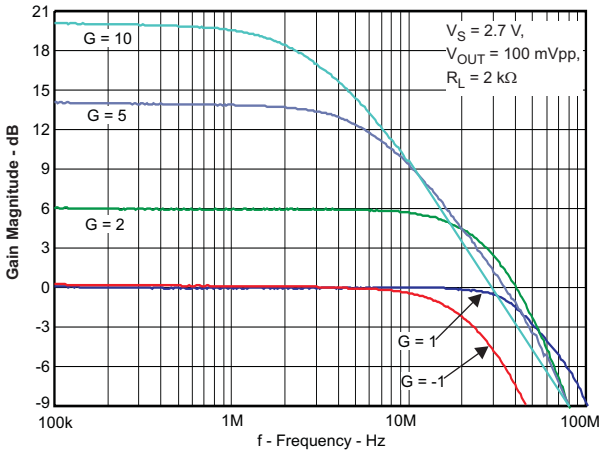


図 2. Gain Bandwidth of OPA835

2.2.2 TLV316: 1.8-V CMOS Op Amp

The TLV316 (single) is a general-purpose, low-power op amp. This device features rail-to-rail input and output swings, low quiescent current (400 µA/ch typical) combined with a wide bandwidth of 10 MHz, and very low noise (12 nV/Hz at 1 kHz), which is attractive for a variety of applications that require a good balance between cost and performance. The low-input bias current supports op amps that are used in applications with megaohms source impedances. The robust design of the TLV316 device provides ease-of-use to the circuit designer—a unity-gain stable, integrated RFI and EMI rejection filter, no phase reversal in overdrive condition, and high electrostatic discharge (ESD) protection (4-kV HBM). The TLV316 is optimized for low-voltage operation as low as 1.8 V (±0.9 V) and up to 5.5 V (±2.75 V). This latest addition of low-voltage CMOS op amps to the portfolio offers bandwidth, noise, and power options to meet the needs of a wide variety of applications.

Key features of this device include:

- Unity-gain bandwidth: 10 MHz
- Low I_Q: 400 µA/ch
  - Excellent power-to-bandwidth ratio
  - Stable I_Q over temperature and supply range
- Wide supply range: 1.8 to 5.5 V
- Low noise: 12 nV/√Hz at 1 kHz
- Low input bias current: ±10 pA
- Offset voltage: ±0.75 mV
- Unity-gain stable
- Internal RFI and EMI filter
- Extended temperature range: –40°C to 125°C

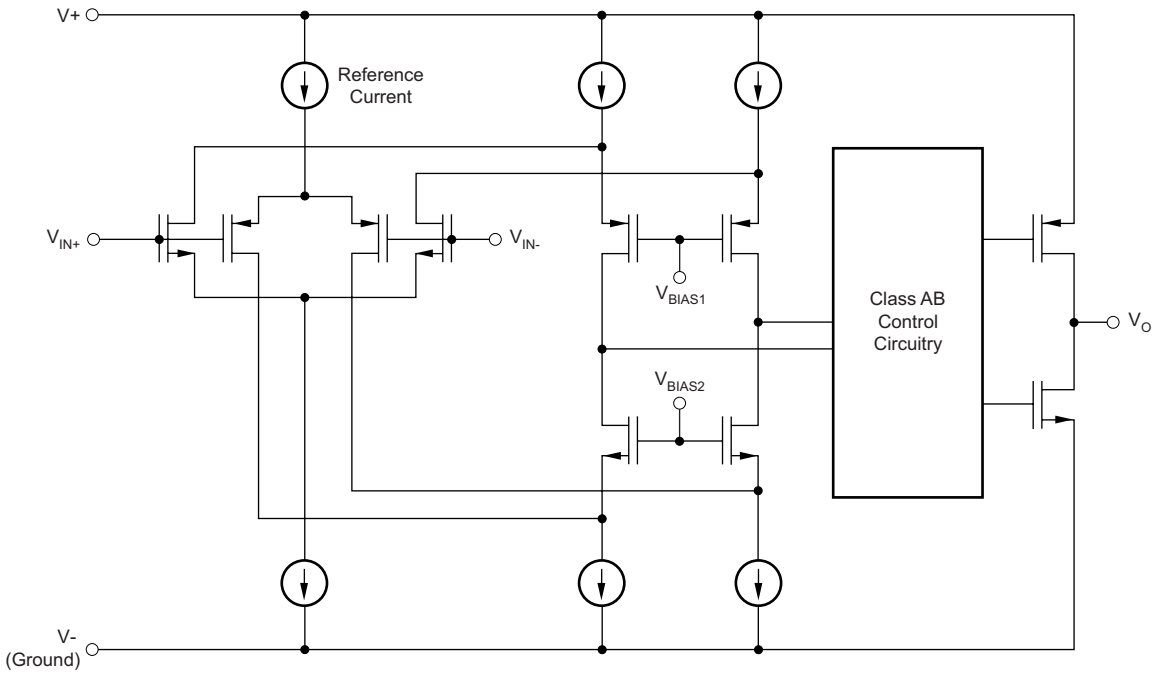


図 3. Functional Block Diagram of TLV316

2.2.3 OPA836

The OPA836 is a single-channel, ultra-low-power, RRO, negative-rail input, voltage-feedback op amp designed to operate over a power-supply range of 2.5 to 5.5 V (single supply), or ±1.25 to ± 2.75 V (dual supply). Consuming only 1 mA per channel and a unity gain bandwidth of 205 MHz, this amplifier sets an industry-leading power-to-performance ratio for rail-to-rail amplifiers.

For applications where power is a key importance, the low-power consumption and high-frequency performance of the OPA836 and OPA2836 devices offer designers performance versus power that is not attainable in other devices. Coupled with a power-saving mode that reduces current to less than 1.5 µA, these devices offer an attractive solution for high-frequency amplifiers in battery-powered applications.

Key features of this device include:

- Low power:
  - Supply voltage: 2.5 to 5.5 V
  - Quiescent current: 1 mA (typical)
  - Power down mode: 0.5 µA (typical)
- Bandwidth: 205 MHz
- Slew rate: 560 V/µs
- Rise time: 3 ns (2 V_{STEP})
- Settling time (0.1%): 22 ns (2 V_{STEP})
- Overdrive recovery time: 60 ns
- SNR: 0.00013% (–117.6 dBc) at 1 kHz (1 V_{RMS})
- THD: 0.00003% (–130 dBc) at 1 kHz (1 V_{RMS})
- HD2/HD3: –85 dBc/–105 dBc at 1 MHz (2 V_{PP})
- Input voltage noise: 4.6 nV/√Hz (f = 100 kHz)
- Input offset voltage: 65 µV (±400-µV maximum)
- CMRR: 116 dB
- Output current drive: 50 mA
- RRO
- Input voltage range: –0.2 to 3.9 V (5-V supply)
- Operating temperature range: –40°C to 125°C

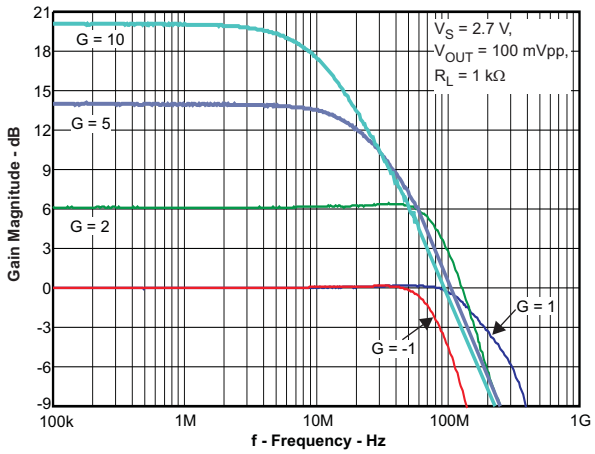


図 4. Gain-Bandwidth of OPA836

2.2.4 TLV3201: Micropower Comparator

The TLV3201 is a single-channel comparator that offers the ultimate combination of high speed (40 ns) and low-power consumption (40 µA), all in an extremely small package with features such as rail-to-rail inputs, low-offset voltage (1 mV), and large output drive current. This device is also very easy to implement in a wide variety of applications where response time is critical.

Key features of this device include:

- Low propagation delay: 40 ns
- Low quiescent current: 40 µA per channel
- Input common-mode range extends 200 mV beyond either rail
- Low input offset voltage: 1 mV
- Push-pull outputs
- Supply range: 2.7 to 5.5 V
- Industrial temperature range: –40°C to 125°C
- Small packages

2.2.5 TLV431: Low-Voltage Adjustable Precision Shunt Regulator

The TLV431 device is a low-voltage three-terminal adjustable voltage reference with specified thermal stability over applicable industrial and commercial temperature ranges. Output voltage can be set to any value between V_{REF} (1.24 V) and 6 V with two external resistors. This device operates from a lower voltage (1.24 V) than the widely used TL431 and TL1431 shunt-regulator references.

Key features of this device include:

- Low-voltage operation, V_{REF} = 1.24 V
- Adjustable output voltage, V_O = V_{REF} to 6 V
- Reference voltage tolerances at 25°C: 0.5% for TLV431B
- Typical temperature drift
  - 4 mV (0°C to 70°C)
  - 6 mV (–40°C to 85°C)
  - 11 mV (–40°C to 125°C)
- Low operational cathode current, 80 µA typ
- 0.25-Ω typical output impedance
- Ultra-small SC-70 package offers 40% smaller footprint than SOT-23-3

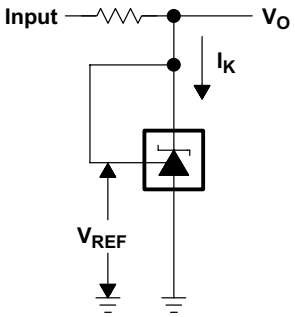


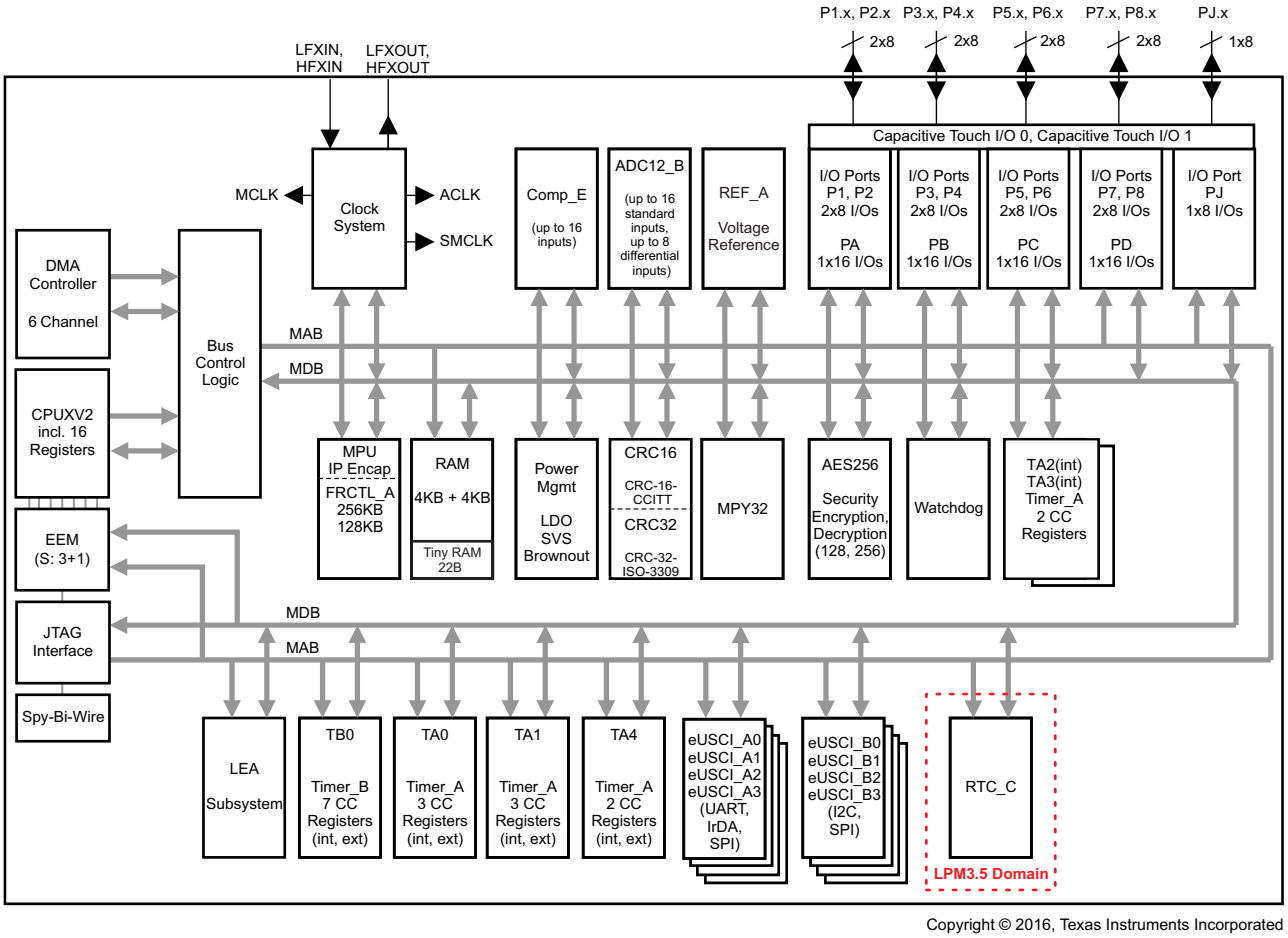
図 5. Functional Block Diagram of TLV431

2.2.6 MSP430FR5994

The MSP ultra-low-power ferroelectric random access memory (FRAM) microcontroller (MCU) platform combines uniquely embedded FRAM and a holistic ultra-low-power system architecture, allowing system designers to increase performance while lowering energy consumption. FRAM technology combines the low-energy fast writes, flexibility, and endurance of RAM with the non-volatility of flash.

The MSP430FRxx MCU portfolio consists of a diverse set of devices ranging from 4KB to 256KB of nonvolatile memory with intelligent peripherals targeted for various applications. The ULP architecture showcases seven low-power modes, optimized to achieve extended battery life in energy-challenged applications.

The MSP430F599x MCUs take low power and performance to the next level with the low-energy accelerator (LEA), a co-processor optimized for signal processing. This accelerator enables developers to efficiently process data using complex functions such as FFT, FIR, and matrix multiplication. This device requires no DSP expertise to implement, with a free optimized DSP Library available. Additionally, with up to 256KB FRAM, these devices offer more space for advanced applications and flexibility for effortless implementation of over-the-air firmware updates.



The device has 8KB of RAM, and 4KB of the RAM is shared with the LEA subsystem. The CPU has priority over the LEA subsystem.

図 6. Overall Functional Diagram of MSP430FR5994

Key features of this device include:

- Embedded MCU:
  - 16-bit RISC architecture up to 16-MHz clock
  - Up to 256KB of FRAM:
    - Ultra-low-power writes
    - Fast write at 125 ns per word (64KB in 4 ms)
    - Flexible allocation of data and application code in memory
    - 10^{15} write cycle endurance
    - Radiation resistant and nonmagnetic
  - Wide supply voltage range: 1.8 to 3.6 V
- Optimized ultra-low-power modes:
  - Active mode: Approximately 120 μA/MHz
  - Standby mode with real-time clock (RTC) (LPM3.5): 450 nA
  - Shutdown (LPM4.5): 30 nA
- LEA for vector math operations:
  - Operation independent of CPU
  - 4KB of RAM shared with CPU
  - Efficient 256-point complex FFT: 35× faster than ARM® Cortex®-M0+ Core
- Intelligent digital peripherals:
  - 32-bit hardware multiplier (MPY)
  - Six-channel internal DMA
  - RTC with calendar and alarm functions
  - Six 16-bit timers with up to seven capture/compare registers each
  - Six 16-bit timers with up to seven capture/compare registers each
- High-performance analog:
  - 16-channel analog comparator
  - 12-bit ADC featuring window comparator, internal reference, and sample-and-hold, up to 20 external input channels
- Multifunctional input/output ports:
  - All pins support capacitive-touch capability with no need for external components
  - Accessible bit-, byte-, and word-wise (in pairs)
  - Edge-selectable wake from LPM on all ports
  - Programmable pullup and pulldown on all ports
- Code security and encryption:
  - 128- or 256-bit AES security encryption and decryption coprocessor
  - Random number seed for random number generation algorithms
  - IP encapsulation protects memory from external access
- Flexible clock system:

  - Fixed-frequency DCO with 10 selectable factory-trimmed frequencies
  - Low-power low-frequency internal clock source (VLO)
  - 32-kHz crystals (LFXT)
  - High-frequency crystals (HFXT)
- Development tools and software: Free professional development environments with EnergyTrace™ technology

The LEA is an execution unit for vector-based arithmetic and signal conditioning-based operations. This execution unit processes the vast numbers of operations of the same type that are needed for FIR filtering, FFT calculations, and many other signal conditioning and vector operations. The LEA is an execution module and is integrated into the MSP430FR5994 to boost performance and achieve much lower power consumption for the target applications. A functional block diagram of the LEA engine is as shown in 図 7.

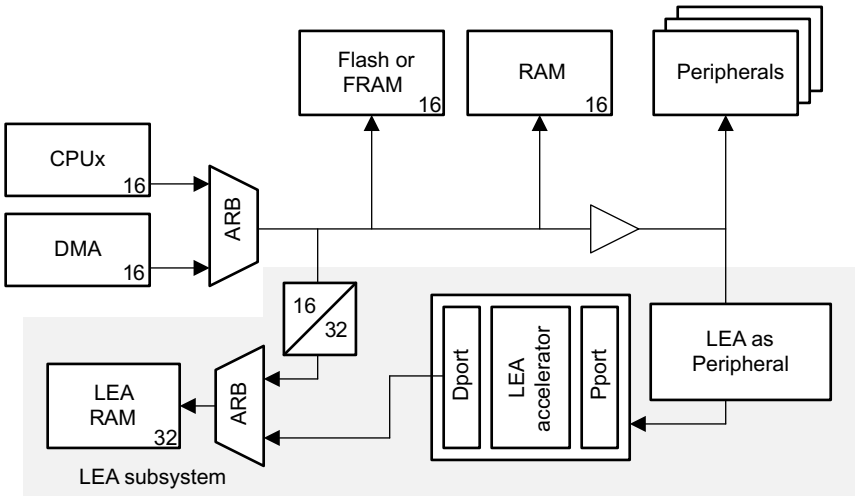


図 7. Functional Block Diagram of LEA

2.2.7 UCC28880: 700-V, 100-mA Low Quiescent Current Off-Line Converter

The UCC28880 integrates the controller and a 700-V power MOSFET into one monolithic device. The device also integrates a high-voltage current source, enabling start up and operation directly from the rectified mains voltage.

The low quiescent current of the device enables excellent efficiency. With the UCC28880, the most common converter topologies such as buck, buck-boost, and flyback can be built using a minimum number of external components. The UCC28880 incorporates a soft-start feature for controlled start-up of the power stage, which minimizes the stress on the power-stage components.

Key features of this device include:

- Integrated power MOSFET (switch) rated to 700-V drain-to-source voltage
- Integrated high-voltage current source for internal low-voltage supply generation
- Soft start
- Self-biased switcher (start-up and operation directly from rectified mains voltage)
- Supports buck, buck-boost, and flyback topologies
- Robust performance with inductor current runaway prevention
- Thermal shutdown
- Protection: Current limit, overload, and output short circuit

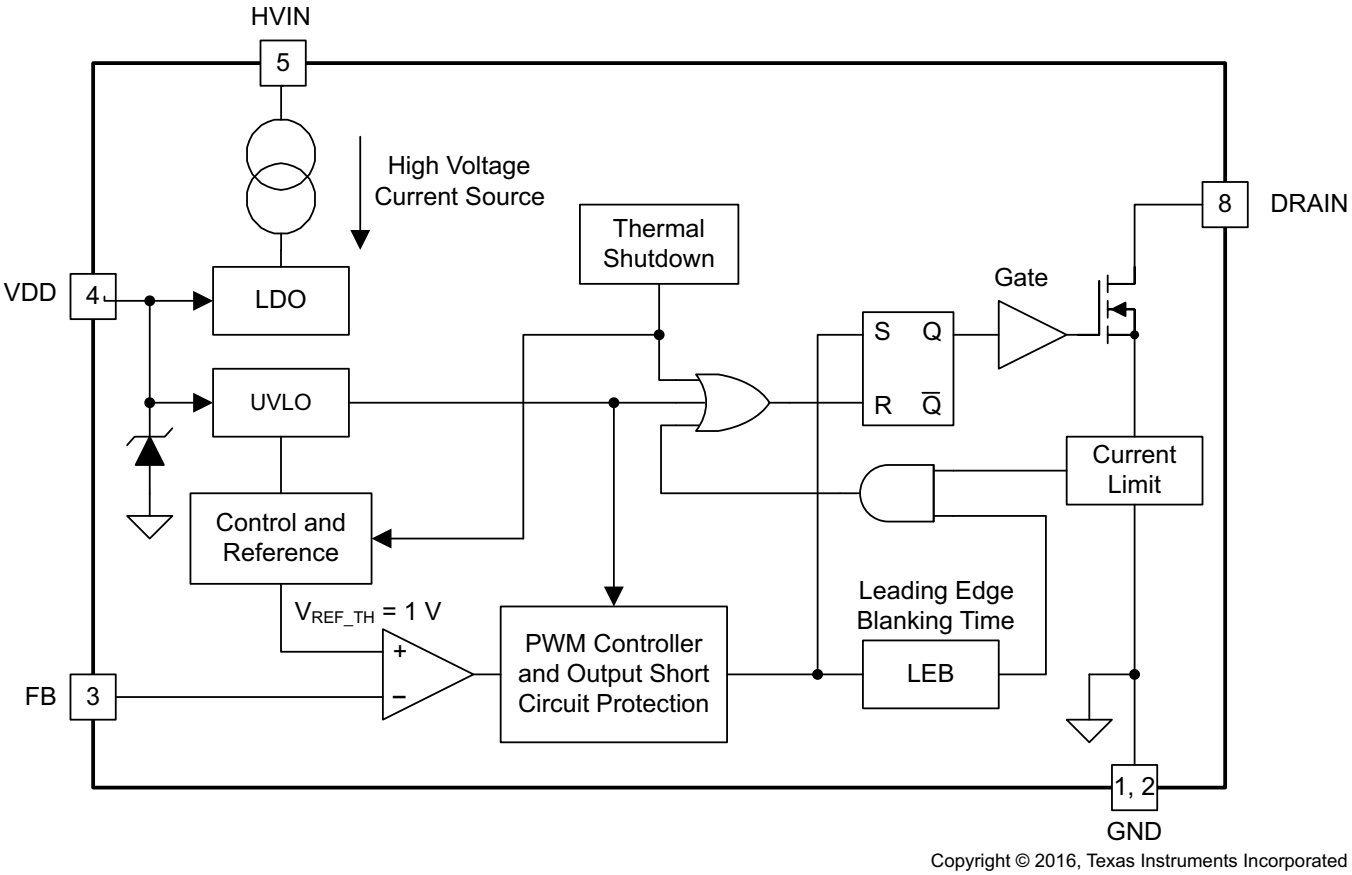


図 8. Internal Functional Block Diagram of UCC28880

2.2.8 LP5907: 250-mA Ultra-Low-Noise LDO

The LP5907 is a low-noise LDO capable of supplying a 250-mA output current. Designed to meet the requirements of RF and analog circuits, the LP5907 device provides low noise, high PSRR, low quiescent current, and low line or load transient response figures. Using new innovative design techniques, the LP5907 offers class-leading noise performance without a noise bypass capacitor and the ability for remote output capacitor placement.

The device is designed to work with a 1-µF input and a 1-µF output ceramic capacitor (no separate noise bypass capacitor is required). This device is available with fixed output voltages from 1.2 to 4.5 V in 25-mV steps.

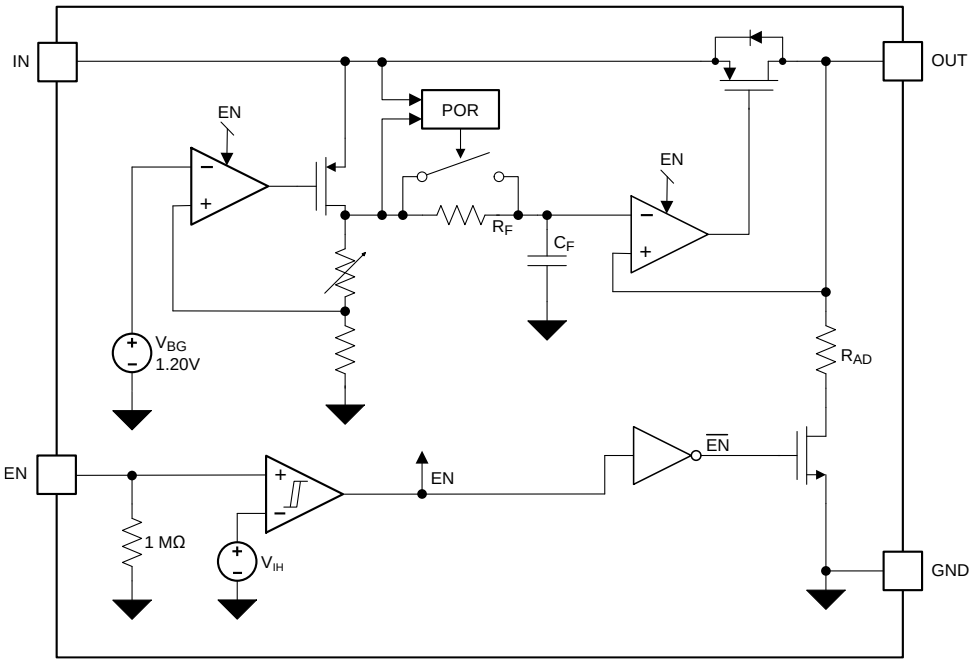


図 9. Functional Block Diagram of LP5907

Key features of this device include:

- Input voltage range: 2.2 to 5.5 V
- Output voltage range: 1.2 to 4.5 V
- Output current: 250 mA
- Stable with 1-µF ceramic input and output capacitors
- No noise bypass capacitor required
- Remote output capacitor placement
- Thermal-overload and short-circuit protection
- –40°C to 125°C junction temperature range for operation
- PSRR: 82 dB at 1 kHz
- Low output voltage noise: < 10 μV_{RMS}
- Output voltage tolerance: ±2%
- Virtually zero I_Q (disabled): < 1 µA
- Very low I_Q (enabled): < 12 µA

- Start-up time: 80 µs
- Low dropout: 120 mV (typical)

2.3 System Design Theory

2.3.1 Analog Signal Conditioning

The TIDA-00929 design gets signal input from an external current sensor, which could be either a shunt, CT, or Rogowski coil. Bandwidth of the current sensor must be sufficient to pass the entire spectrum for the analysis. Take care while designing sensor based on CT or Rogowski coil to make sure its bandwidth performance even though this provides galvanic isolation and eliminates common-mode noise input. On the other hand, shunt provides a linear, low-cost, and compact solution with high accuracy. However, the power supply on the board needs to be well designed to account for the absence of isolation.

The TIDA-00929 is designed for measuring currents up to 100 A using a 1-mΩ shunt. Hence, the input voltage range has to be at least ±141 mV. In case of higher current requirements, a shunt of lower value can be chosen. In this TI Design, peak input voltage of ±155 mV has been considered. In order to measure voltage across the current feedback, a differential gain stage is used. For the low frequency path, output from the differential stage is input to a low-pass filter that goes to ADC for further processing in digital domain. On the high-frequency path, specific band of frequency has been chosen by passing the signal through an effective band-pass filter.

For the analog signal conditioning, five of the potential op amps have been selected, which are listed in 表 2.

表 2. List of Potential Op Amps

PART	GBW (MHz)	SLEW RATE (V/µs)	I_Q (mA)	CM i/p RANGE		O/p SWING		I/p VOLTAGE NOISE (nV/Hz)	NOISE (nV)
				MIN	MAX	MIN	MAX		
LMH6645	40	15	0.65-1.25	–0.1	V_{cc}+0.1	0.15	V_{CC}-0.15	17	107 at 40 MHz
TLV316	10	6	0.575	–0.2	V_{cc}+0.2	0.125	V_{CC}-0.125	12	37 at 10 MHz
OPA835	30 to 51	110	0.345	0	V_{cc}-1.2	0.2	V_{CC}-0.25	9.3	51 at 30 MHz
OPA836	200	240	1.15	0	V_{cc}-1.2	0.2	V_{CC}-0.15	4.6	36 at 60 MHz
OPA890	130 to 170	300	1.25		V_{cc}-1.35	1.1	V_{CC}-1.1	10	114 at 130 MHz

2.3.1.1 Differential Gain Stage

This stage is designed as a differential amplifier with a DC shift to maintain its output between 0 and 3.3 V. Because this stage feeds both the low-frequency path and high-frequency path, the bandwidth at this stage has to be high enough to pass the entire necessary frequency spectrum. In addition, gain needs to be provided to increase input signal levels from ±155 mV to obtain a full voltage swing. 図 10 shows a block schematic of the differential stage.

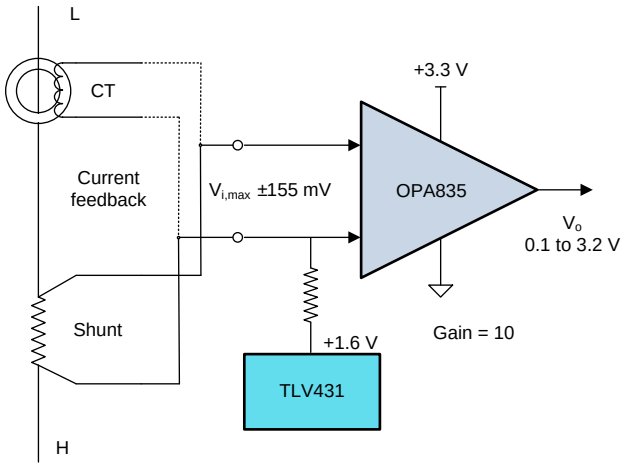


図 10. Block Diagram of Differential Gain Stage

From 表 2, the LMH6645 and OPA835 have sufficient GBW to provide a bandwidth of 3 MHz with a gain of 10. Out of these two options, the OPA835 is selected over the LMH6645 due to its lower I_Q. Even though the OPA835 has a higher CM input voltage range, it is not of a concern in this stage due to lower input voltage levels.

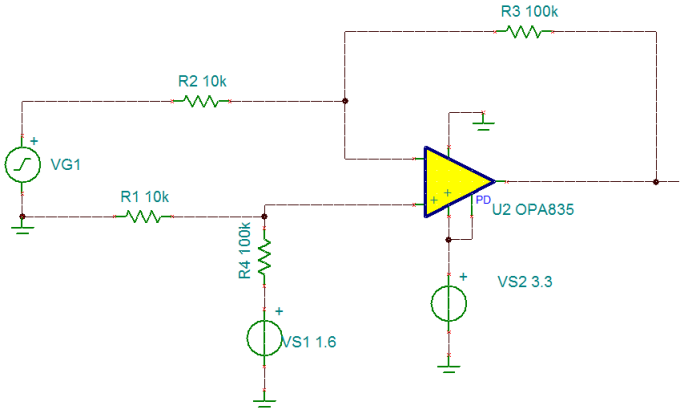


図 11. Schematic of Differential Gain Stage

注: If there is a requirement of higher bandwidth, then the user can replace OPA835 with OPA836 which has GBW of 200MHz and has pin compatibility. Alternate way is to combine differential gain stage and HPF in one part using OPA2836.

図 11 shows the differential gain stage of the TIDA-00929. A reference voltage of 1.6 V is derived from the TLV431. Design the voltage reference by following the TLV431 datasheet *TLV431x Low-Voltage Adjustable Precision Shunt Regulator* and application report *Setting the Shunt Voltage on an Adjustable Shunt Regulator*.

Verify the performance of the differential gain stage by simulating the designed circuit in TINA-TI™. 図 12 shows the gain versus frequency plot for the first stage that is designed using the OPA835.

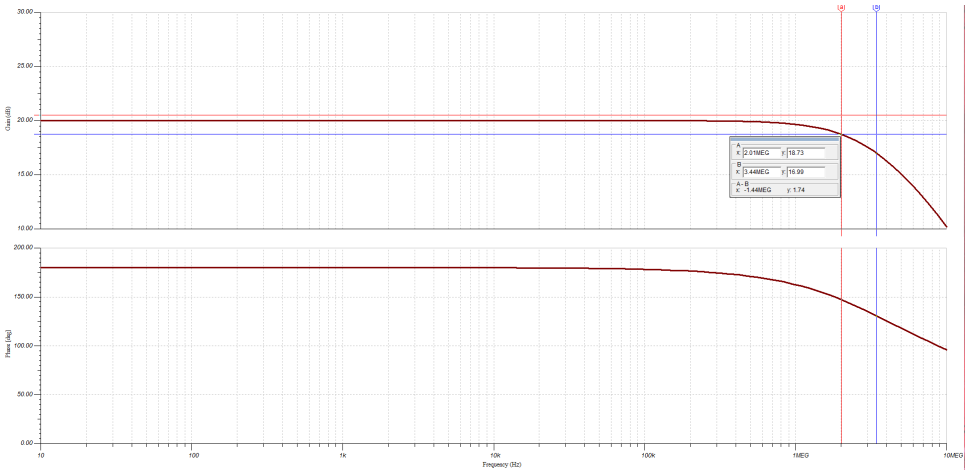


図 12. TINA-TI Analysis of Frequency Response for Differential Gain Stage

2.3.1.2 Low-Pass Filter

This filter is used to eliminate the high-frequency components going into the ADC of the MSP430. The cutoff frequency of the filter is selected to be less than half of the ADC sampling rate. If the ADC is sampled at 200 ksps, then the value of the cutoff frequency has to be less than 100 kHz. The low-pass filter can be designed to filter for a cutoff frequency that has to be less than half the ADC sampling frequency. Because the input voltage to the low-pass filter has a full voltage swing, a unity gain second-order filter configuration has been selected. Criteria for the selection of op amp is rail-to-rail both input and output voltage swings.

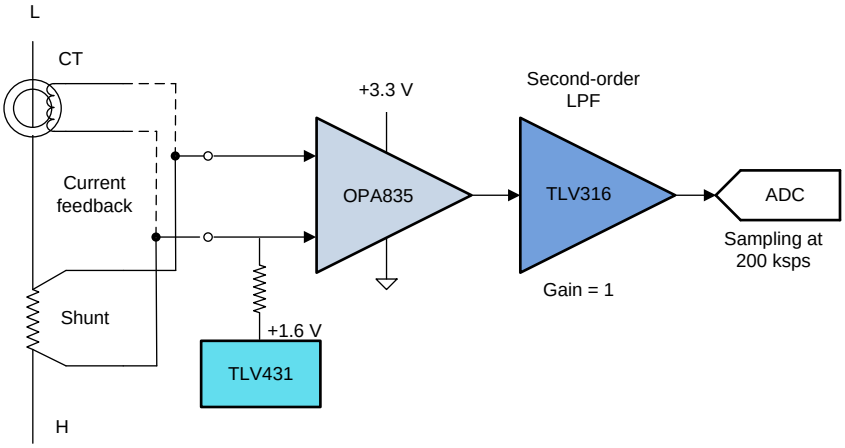


図 13. Block Diagram of Frequency Domain Analysis

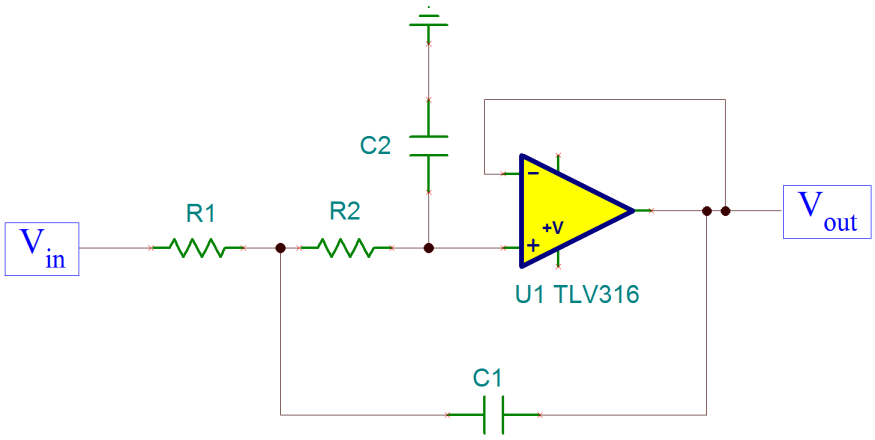


図 14. Second-Order Sallen-Key Filter

A second-order Sallen-Key low-pass filter has been implemented to remove high-frequency signals going to the ADC. This filter topology also helps to eliminate the aliasing effect of ADC sampling. The transfer function of the Sallen-Key filter shown in is given by 式 1:

$$H(s) = \frac{\omega^2}{s^2 + 2\alpha s + \omega^2} \ldots \quad (1)$$

where:

- w is the cutoff frequency of the filter in rad/sec
- α is the attenuation factor

$$\omega = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}} = 2\pi f_o \ldots \quad (2)$$

Q is the Q-factor of the filter, which is selected as 0.707 and derived as:

$$Q = \frac{\omega}{2\alpha} = \frac{\sqrt{R_1 R_2 C_1 C_2}}{C_2 (R_1 + R_2)} \ldots \quad (3)$$

$$R_1 = R_2 = R \ldots \quad (4)$$

$$\text{For } Q = \frac{1}{\sqrt{2}} : C_1 = 2 \times C_2 = 2 \times C \ldots \quad (5)$$

$$\omega = 2\pi f_O = \frac{1}{RC \times \sqrt{2}} \ldots \quad (6)$$

Resistors and capacitors for a given cutoff frequency can be calculated using these equations. The frequency response of the designed low-pass filter can be verified in TINA-TI.

For a filter with a cutoff frequency of 100 kHz, a frequency response analyzed using TINA-TI is shown in 図 15.

表 3. Low-Pass Filter Parameters

CUTOFF FREQUENCY (kHz)	R_1 AND R_2 (kΩ)	C_1	C_2
3.2	51	1.38 nF	0.68 nF
10	51	0.44 nF	0.225 nF
50	51	88 pF	44 pF
100	10	225 pF	110 pF

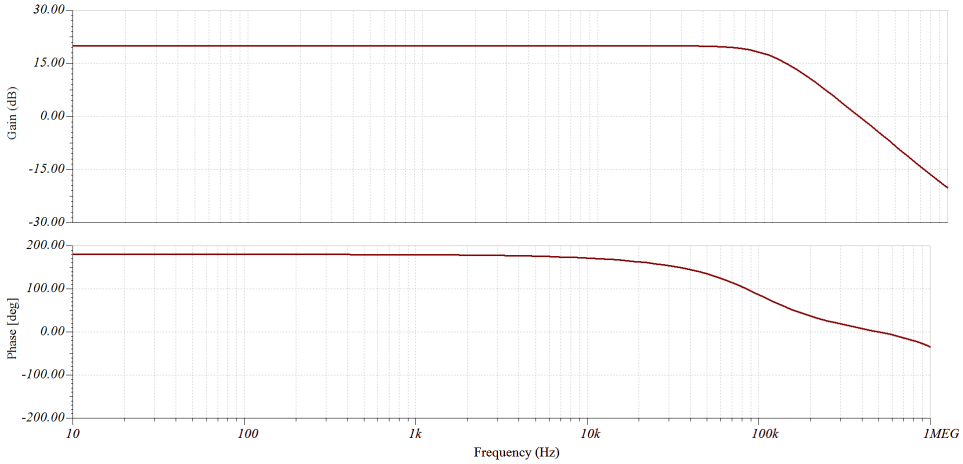


図 15. Frequency Response of Low Frequency Path

2.3.1.3 High-Pass Filter

To capture high-frequency noise, a high-pass filter can be used to eliminate the low-frequency component from the signal. For capturing noise of very low levels in the input signal, an additional gain stage is included along with the high-pass filter to improve the resolution of the high-frequency capture. Along with the gain, it is also required to have very high bandwidth to pass all the high-frequency noise necessary for the analysis. From 表 2, the OPA836 and OPA890 have enough GBW to allow necessary signal conditioning. However, the OPA890 has a lower output voltage swing, which makes the OPA836 as a suitable candidate for the high-pass filter. Although the OPA836 has limited input voltage swing due to filtering low frequency and the DC component at the input of the high-pass filter, the input voltage at the OPA836 is corresponding to high-frequency noise, which is smaller than the input voltage swing. 図 16 shows a block diagram of the high frequency path.

注: Even though a high-pass filter configuration has been used in this stage effectively, this stage acts like a band-pass filter due to the GBW of the op amp that is being used. Hence, the upper cutoff frequency of the filter is decided by the GBW of the op amp (OPA836 in this case).

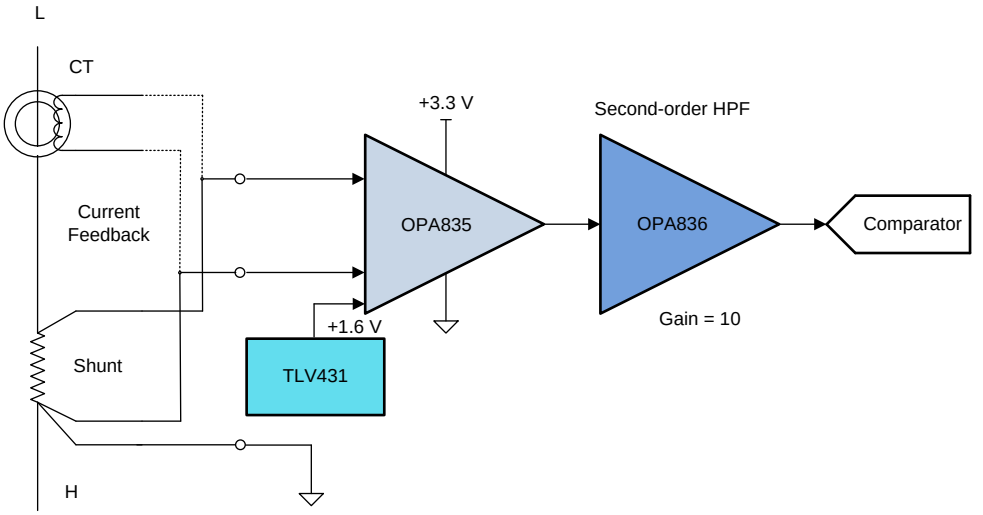


図 16. Block Diagram for Time Domain Analysis

shows a schematic of the high-pass filter with gain by using R3 and R4 in the feedback. Non-inverting multiple feedback in high-pass filter topology has been used. Passive components are designed for a cutoff frequency of the filter and the gain. 図 4 shows the gain bandwidth for the OPA836, where it demonstrates possibility of using the OPA836 to process frequency up to 10 MHz for a gain of 10. As a result, the upper cutoff frequency of this stage is limited by the GBW of the op amp. A circuit diagram of the high-pass filter is shown in 図 17. The design is verified in TINA-TI, and the frequency response of the entire high-frequency path, which includes both differential gain stage and high-pass filter, is shown in 図 18. The upper cutoff frequency has been limited by the first stage. In case of a higher frequency requirement, the OPA836 can be used at the differential gain stage.

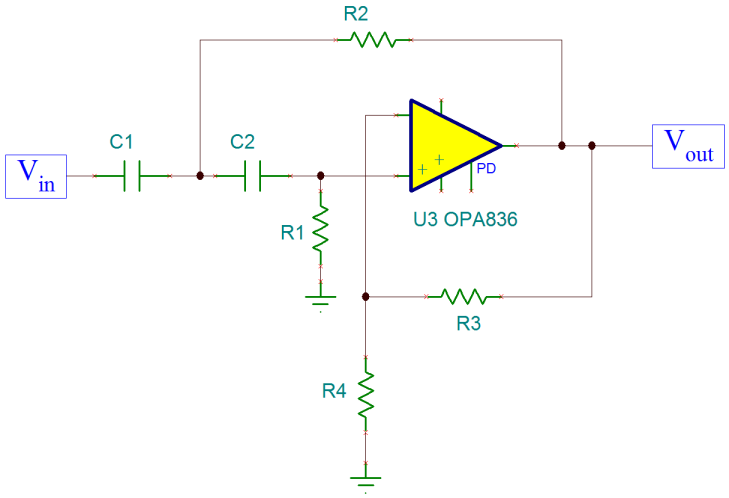


図 17. High-Pass Filter With Gain

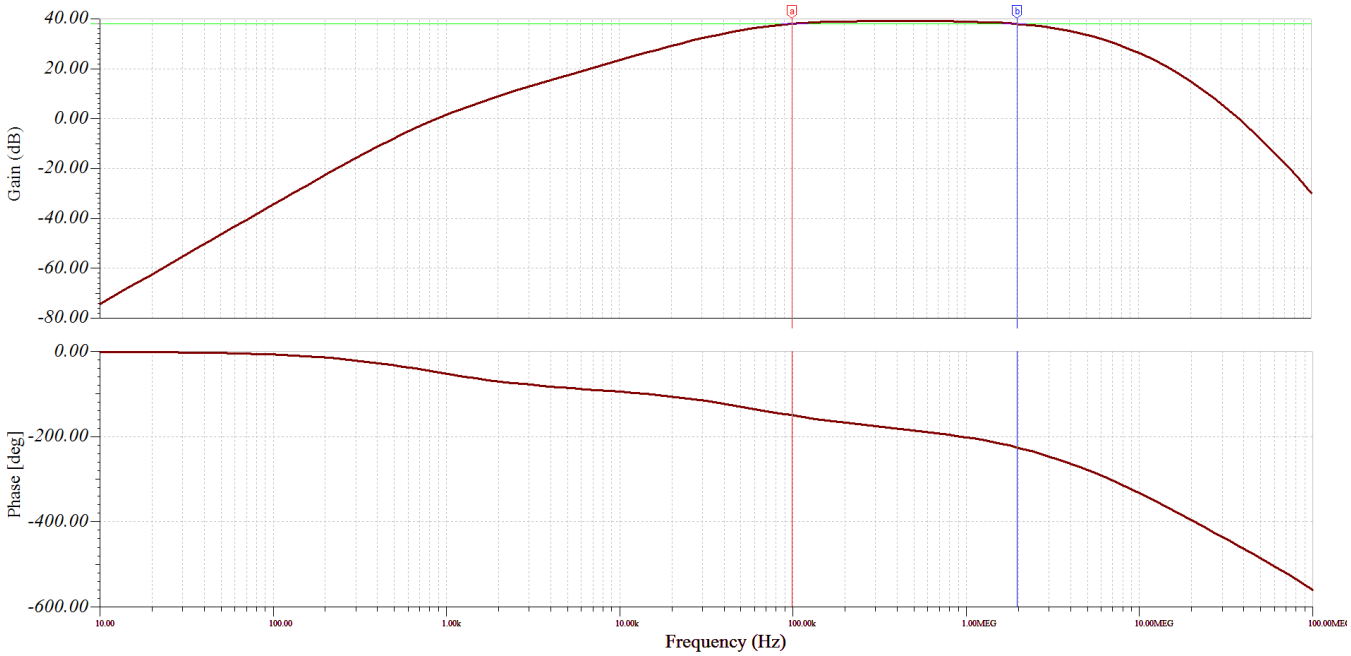


図 18. TINA-TI Analysis for High-Frequency Path

Because all the op amps are powered by a single-ended supply, voltage output at the high-pass filter will be a half wave rectifier sine wave where negative cycle is saturated to 0 V as shown in 図 19.

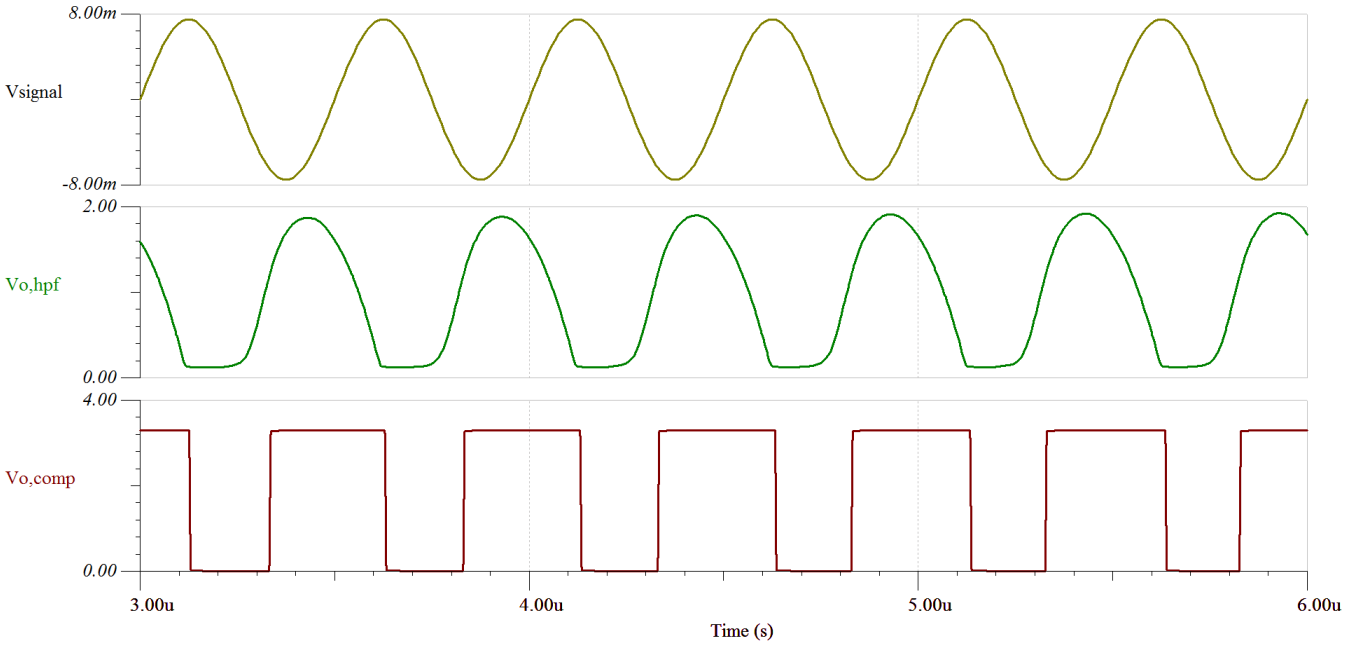


図 19. Voltage Output at High-Pass Filter and Comparator

2.3.1.4 Comparator

The comparator is used to convert the high-frequency noise from the high-pass filter to a pulse train signal, which can be analyzed in time domain. In this TI Design, the pulse train is obtained using either of the two following options: using an internal comparator or an external comparator.

2.3.1.4.1 Using Internal Comparator

The MSP430 has an analog comparator built in, which can be programmed to generate a signal when its input signal crosses a set threshold value and goes below the threshold value for falling edge. This comparator has an internal input resistance of 3 kΩ and capacitance of 10 pF as shown in 図 20. This acts like a low-pass filter limiting the bandwidth of the comparator. Theoretically, this has a 10% attenuation frequency of 1.8 MHz and a 3-dB cutoff frequency of 5.3 MHz. Values for the positive and negative edge comparator threshold can be set by configuring the internal control registers of the MSP430. It is possible to get a resolution of 1/32nd of the reference voltage, which is generally the supply voltage (3.3 V)

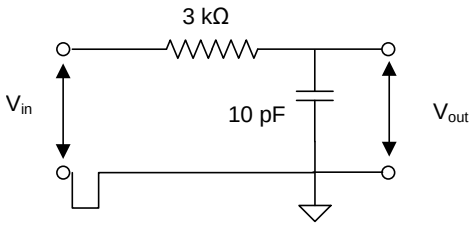


図 20. Input Characteristic of Internal Comparator

2.3.1.4.2 Using External Comparator

The frequency spectrum that can be captured using the internal comparator is limited by the internal parameters of the MSP430. To analyze frequency components above this limit, use an external comparator, which is fast enough to capture high-frequency broadband noise. 図 21 shows the block diagram for the time domain analysis using an external comparator. This path has been designed to capture pulse trains of up to 10 MHz with a minimum pulse width of 20 ns. As a rule of thumb, the comparator selected has a propagation delay skew of at least 1/10th of the minimum pulse width.

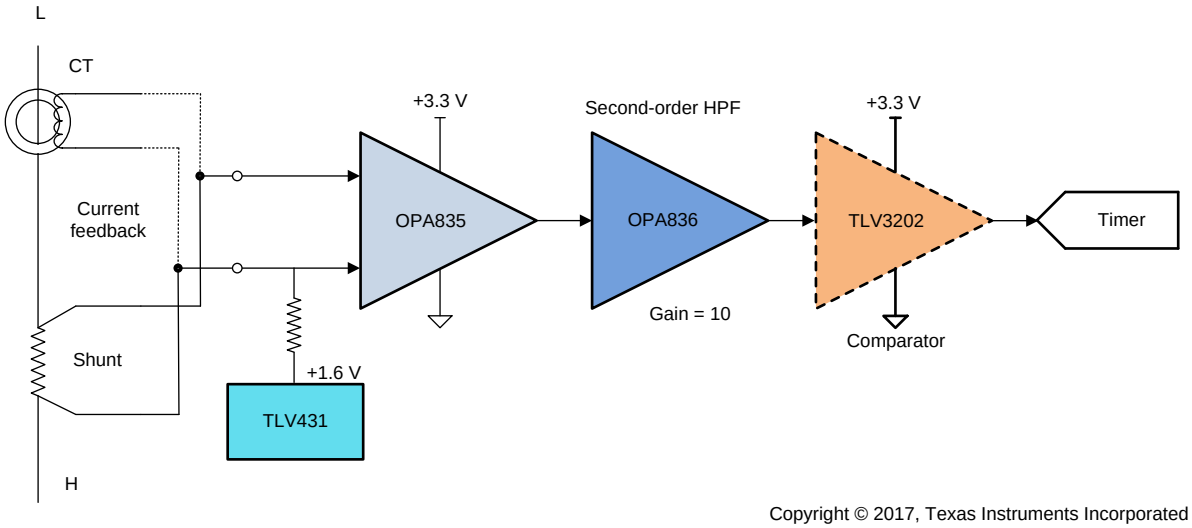


図 21. Block Diagram of Time Domain Analysis Path

2.3.2 Embedded Processing

2.3.2.1 Hardware

A block schematic of the MSP430 with various connections is shown in 図 22. Peripheral modules such as the ADC (ADC12_B), comparator (COMP_E), timer counter, timer capture, GPIO, and Spy-Bi-Wire are used in this TI Design, which will be discussed in detail.

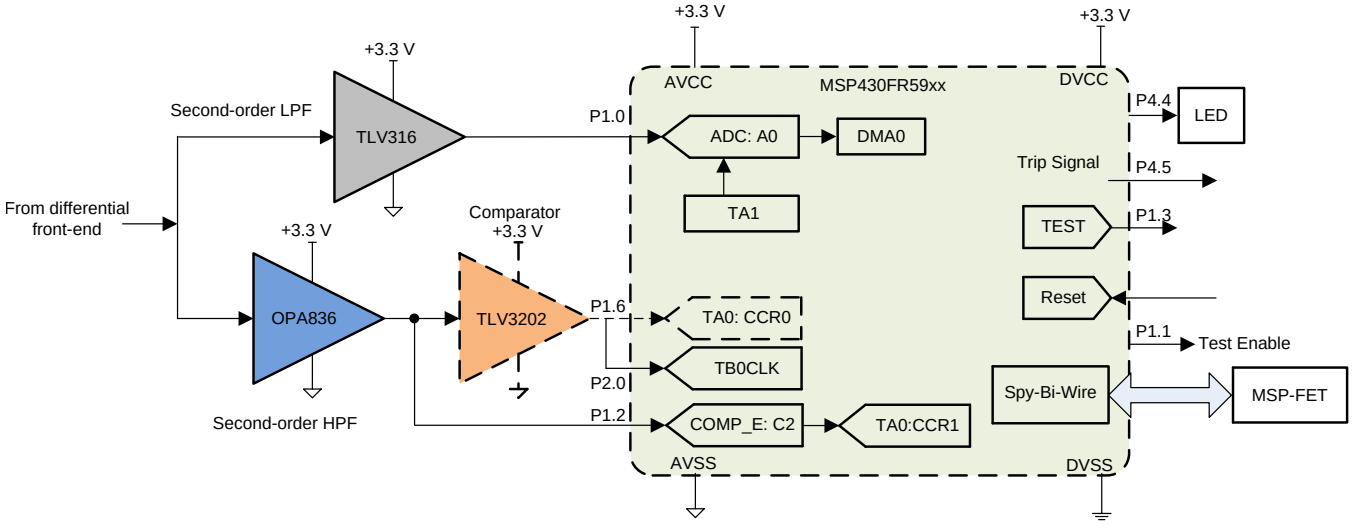


図 22. Block Diagram of MSP430 Showing Port and Pin Selection

2.3.2.1.1 ADC

The MSP430 has a 12-bit SAR ADC that is clocked by the internal MODCLK with a frequency of 4 to 5.4 MHz. The maximum conversion time can be up to 3.5 µs. To achieve an overall ADC sampling frequency of 200 ksps, it is critical to design the sample-and-hold circuit to limit the sampling time within 1.5 µs. The ADC12_B module has an internal MUX ON resistance of 4 kΩ and an input capacitance of 15 pF. The external RC filter can be designed to limit the sampling time to 1 µs using 式 7:

$$\left(R_S + R_I\right) \times \mathrm{IN}\left(2^{n+2}\right) \times \left(C_I + C_{ext}\right) \le t_{sample} \cdots \quad (7)$$

2.3.2.1.2 Comparator

As discussed in 2.3.1.4.1, the internal comparator of the MSP430 has a 3-dB bandwidth of 5.3 MHz. The RC filter is added at the output of the high-pass filter and is designed to have a cutoff frequency higher than 5.3 MHz to use the full bandwidth of the internal comparator. The pin for the comparator input is selected from one of 16 channels available for configuring as a comparator input.

2.3.2.1.3 Spy-Bi-Wire

The input clock for Spy-Bi-Wire is obtained from SBWTCK, and data is transferred at SBWTDIO. Find more details on the design constraints for debuggers in the MSP Debuggers User's Guide.

2.3.2.2 Software

2.3.2.2.1 ADC

As discussed in 2.3.2.1.1, the conversion time for the ADC is 3.5 µs and the sampling time is at least 1 µs. As a result, it is possible to configure the ADC sampling frequency to be approximately 200 ksps. Because frequency domain analysis is done in a digital domain, it is always recommended to use a fixed sampling frequency. Selecting a sampling frequency depends on the fundamental frequency of the input signal, which is discussed in 2.3.2.2.3. To sample the ADC at a regular time interval, ADC conversion is triggered by a timer of fixed frequency. DMA is used to transfer data from ADC result register to the LEA shared memory for further processing.

It is possible to analyze the input signal at the ADC using either fast Fourier transform (FFT) or finite impulse response (FIR).

2.3.2.2.2 FFT Drawbacks

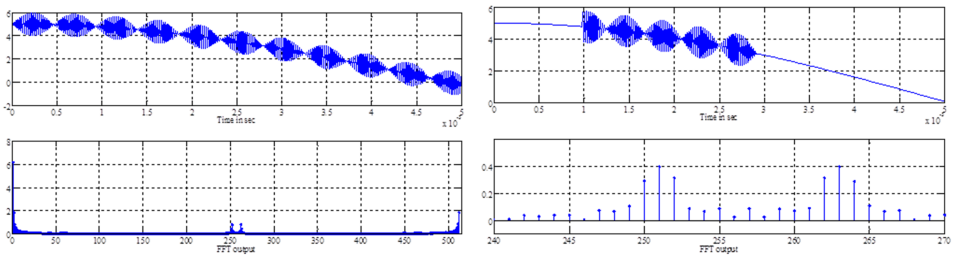
FFT computes frequency components from samples in a time domain. In digital processors such as the MSP430FR5994 with an engine dedicated for vector math calculation, the number of cycles needed for calculation can be much lower than other processors. This is possible when the number of samples is a power of 2^n, such as 64, 128, 512, and 1024. The output of the FFT has the same number of values as the input samples that correspond to the magnitude and phase of different frequency components hidden in the input signal. Output values correspond to frequencies that are multiples of the fundamental frequency whose time period is decided by the sampling rate and length of samples.

For example, for an input fundamental signal of 50 Hz, if 512 samples are taken during its period (that is, 20 ms), then the sampling rate is given as 50 Hz × 512 = 25.6 ksps. The result from FFT has 256 pairs of real and imaginary values, which corresponds to frequencies multiples of fundamental (50 Hz in this case). As a result, the maximum frequency component that can be captured using FFT will be 50 × 256 = 12.8 kHz, which is half the sampling frequency. If the input signal has a frequency component higher than

the fundamental value (for example, 1 kHz), then it would appear at the 1k/50 = 20th sample of the FFT output. The magnitude of the output depends on the input signal strength. If a 1-kHz signal is riding over a 50-Hz signal throughout the entire period, then the output corresponds to the peak value of the 1-kHz component. The output value gets attenuated by a factor if this high frequency component is present for only few cycles instead of continuous. If the 1-kHz component is present for one in 20 cycles of fundamental, then the output value gets attenuated by a factor of 1/20. On the other hand, if the high frequency is not an integer multiple of the fundamental frequency, then it would be reflected in samples around that frequency and magnitude gets spread over several components reducing the peak value that is being seen by FFT.

This has been demonstrated using the example in 図 23. Over a 50-Hz signal, a noise of 1 V, 50 kHz has been injected in the signal. A 512-point FFT for the signal captured using 200 ksps has been carried out to observe that the entire 1 V has been reflected on the output of FFT as shown in the right side of 図 23. When the noise of 50 kHz has been injected for only 40% of the sampling interval, a fraction of the voltage amplitude is being observed at the output of FFT. Instead of 1 V, only 0.4 V is observed.

In case of arc signatures, broadband noise riding on top of the fundamental could be of any random frequency and present for only very few cycles. If FFT of this signal is performed, then the peak value of high-frequency noise gets attenuated at the output. With the 200-ksps sampling rate, it is possible to extract frequencies up to 100 kHz, which is 2000 times the fundamental frequency of 50 Hz, which means there will be 2000 cycles of 100 kHz. If there is a burst of few cycles of 100 kHz over 50-Hz samples, then it would get attenuated by (U)/2000, where U is the number of high-frequency samples in a fundamental cycle. 図 24 presents FFT analysis on a typical signal that contains broadband or pink noise. A 512-point FFT has been performed for a signal obtained using a 200-ksps sampling frequency. Different segments of the waveform have various levels of noise and FFT on these signals are being performed. FFT clearly shows the presence of wide frequency components in the signal. Distributing broadband noise along with attenuating due to aperiodicity of the noise increases the difficulty level of capturing the noise in the signal using FFT.



Periodic high frequency signal on fundamental　　Aperiodic high frequency signal on fundamental

図 23. Comparison of FFT Analysis for Periodic and Aperiodic Noise Signals

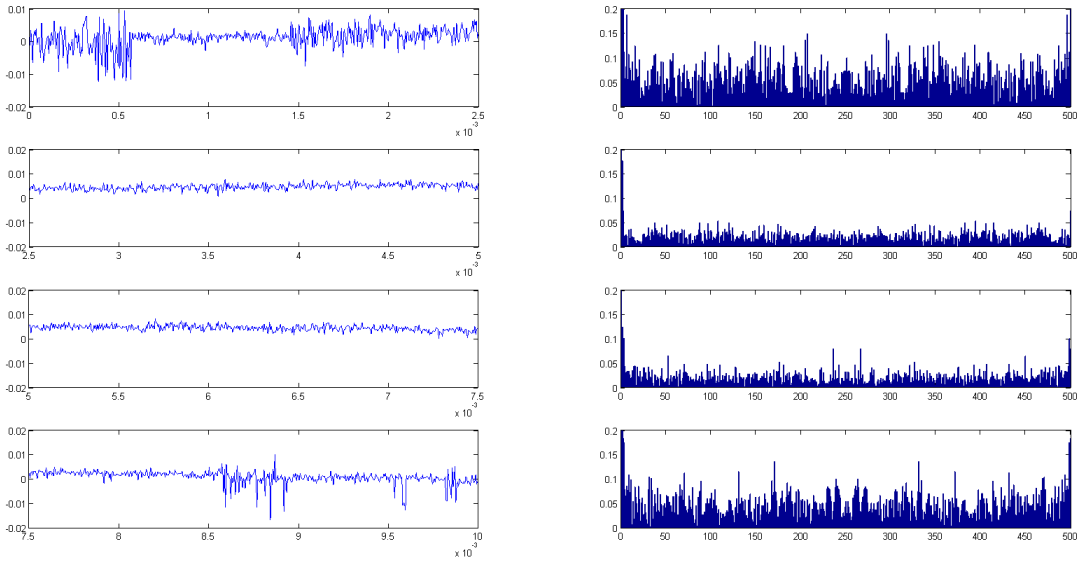


図 24. 512-Point FFT of Typical Signal Containing Broadband Noise

2.3.2.2.3 FIR Filter

A FIR filter is a digital implementation of the filter whose impulse response is finite. In contrast to FFT, the output samples from the FIR filter are still in time domain. If there is a signal burst at the input, then it would appear directly at the output without any attenuation, provided the frequency falls into pass band of the FIR filter. Added to this, if the noise frequency is distributed around a frequency band, then it would be passed through the filter without any attenuation. Hence, it is easier to capture short bursts of broadband noise using FIR rather FFT. It is also beneficiary to use FIR for capturing transient in the signal.

The size of the FIR filter is represented by its order, which is also termed as number of taps, N. To calculate size, the FIR filter needs present input samples and N previous samples. It is possible to collect an array of input samples and calculate the FIR for the same using N previous samples. For an "X+N" number of input samples, "X" number of output samples are obtained using a N^{th} order FIR.

The MSP430FR5994 has LEA to enable vector-based arithmetic and signal conditioning operation at a lesser number of cycles, which can be used to perform FIR filtering. As shown in 図 7, LEA shares RAM with the CPU, which is limited to 4kB in this processor. For all the calculations done using LEA, input and output data needs to be placed in the LEA shared memory, which is accessed independent of CPU state. This not only increases operation speed, but it also reduces power consumption.

To perform real-time FIR filtering, a ping-pong buffer is used. While data is being stored in one of the memory buffers (pong), FIR is being performed on the alternate buffer (ping) where ADC results are stored in the previous cycle. As a result, the size required to store input data is double the number of samples. For the results buffer, size has to be same as the number of samples that are being input to the FIR filter. Based on these constraints and available LEA shared RAM, it is possible to go up to a 512-point FIR. See 図 25 on how to use LEA memory, where 2kB of RAM is allocated for storing input data using a ping-pong buffer and 1kB for the results vector. The remaining memory is reserved for miscellaneous variables such as the filter coefficient, intermediate variables, and system parameters.

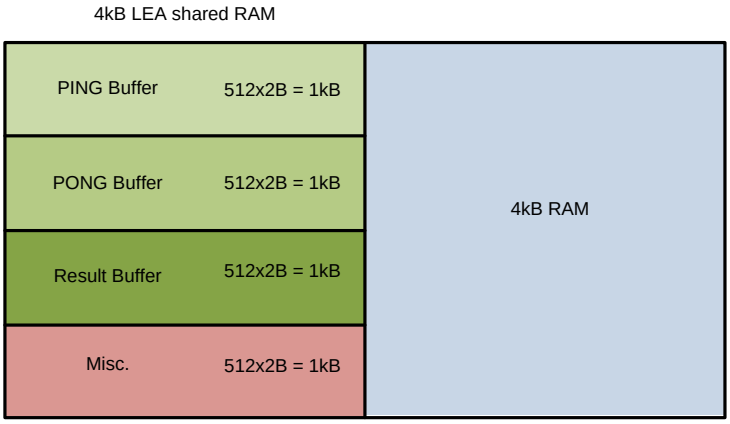


図 25. Using Shared LEA Memory in MSP430

FIR filtering is done once every 512 samples. To analyze a 50-Hz signal, it is recommended to perform FIR at a frequency that is even multiples of fundamental. In that case, it is possible to analyze the signal every half cycles precisely. It is possible to divide the 50-Hz cycle into eight equal segments S1 through S8 to do the calculations as shown in 図 26. To obtain 512 samples every 2.5 ms, it is necessary to sample ADC at 204.8 ksps, which can be done by using the MSP430FR5994.

注: For a 60-Hz signal, to obtain equal segments over a full cycle, the signal can be broken into six segments. In that case, calculations are done every 2.78 ms, which is done by sampling at 184.32 ksps. This limits the frequency spectrum to 92 kHz instead of 100 kHz.

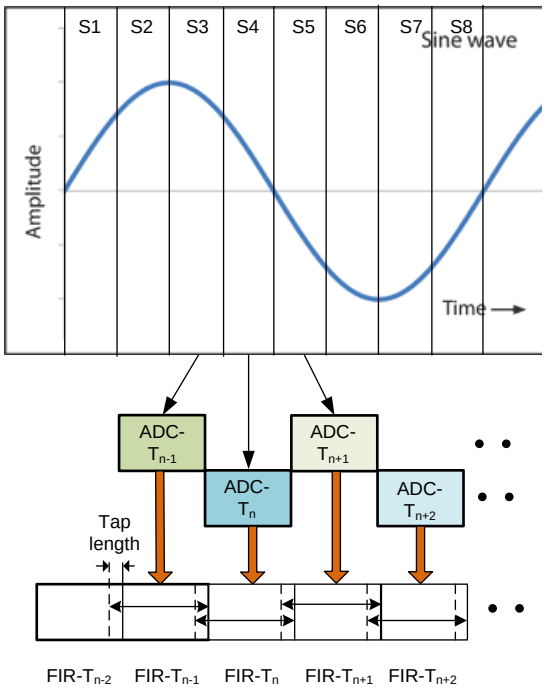


図 26. Performing Real-Time FIR in MSP430

Follow these steps to perform a real-time buffer using a ping-pong buffer. In this example, a 512-point FIR is illustrated, which means buffering has twice the sample length (that is, 1024).

1. Initialize the entire buffer to zeroes.
2. Sample the ADC at a regular interval and use DMA to place the ADC result on to the circular buffer starting from address 000 to 511 as shown in 図 27.
3. Once DMA transfers 512 samples, the ADC starts placing the results from 512 through 1023. FIR will be performed on samples stored in 000 to 511. To incorporate for the previous samples, FIR is done for samples starting N samples prior (1023-N) as shown, where N is the tap length. Because zeroes have been placed during Step 1, it takes zeroes for its first calculation. Calculation are completed before the ADC overwrites on to the registers (1023-N) through 1023.
4. ADC samples are placed in block A in registers starting from 0 to 511. FIR is performed on samples starting from (511-N) through 1023.

These steps of swapping between block A and block B are repeated in continuous fashion to perform a real-time FIR.

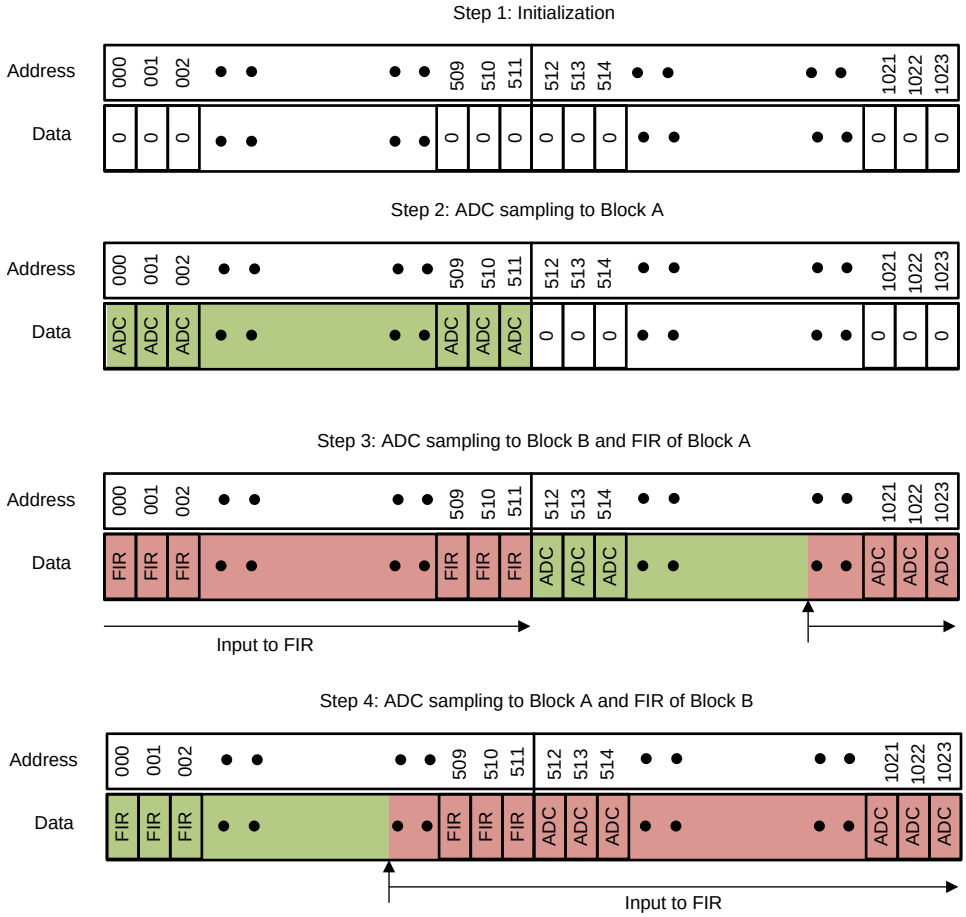


図 27. Operation of Online FIR Calculation Using Ping Pong Buffer

2.3.3 Power Supply

Both analog signal conditioning and digital processing are performed using a 3.3-V supply. 図 28 shows the estimated power consumption from different parts. The power supply is derived from a single-phase AC supply with a wide voltage variation of 85 to 270 V_{RMS}. The board requires less than 10 mA of supply current. The power conversion from AC to DC is obtained using the offline power converter UCC28880, which can provide up to 100 mA. 図 29 shows a schematic of the power conversion stage designed to obtain 5-V DC from the AC supply. The converter can be designed using WEBENCH. The TVS diode and fusible resistor are added at the AC input to protect the board from unwanted voltage surges. It can withstand up to a 3-kV voltage surge for a 50-Ω surge generator.

For optimized size and BOM, the PMP21750 can be referred for designs requiring up to 30 mA. In the test report, a single-layer PCB has been optimized for space (0.68" x 0.48") and test results are presented.

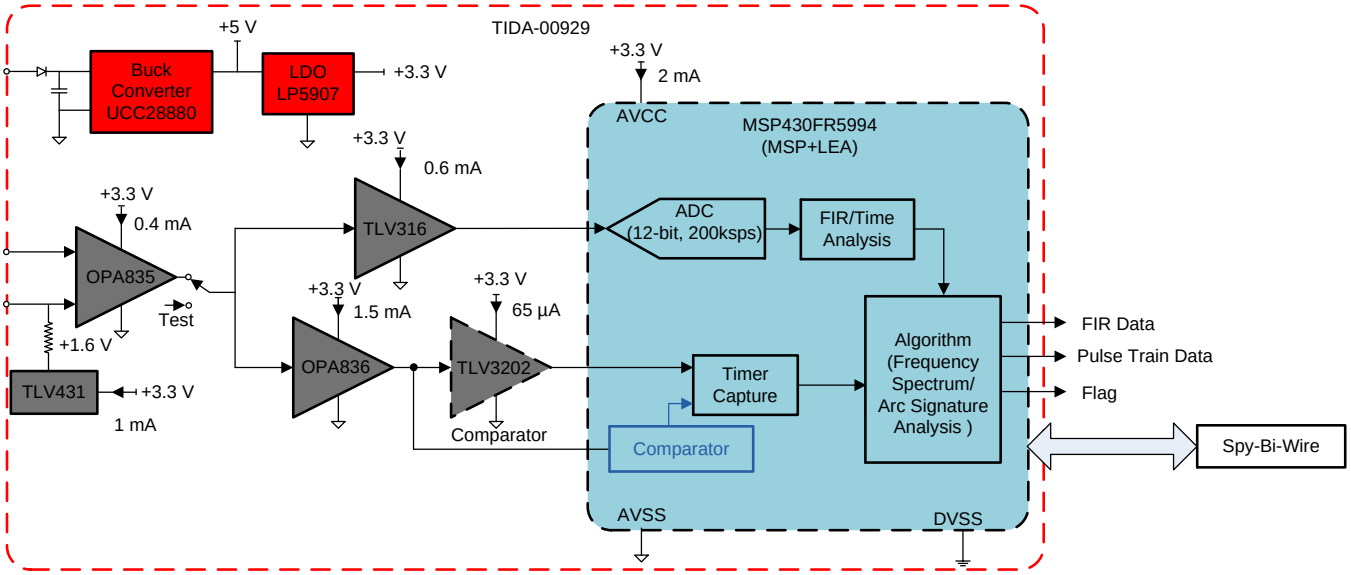


図 28. Power Consumption by Various Parts

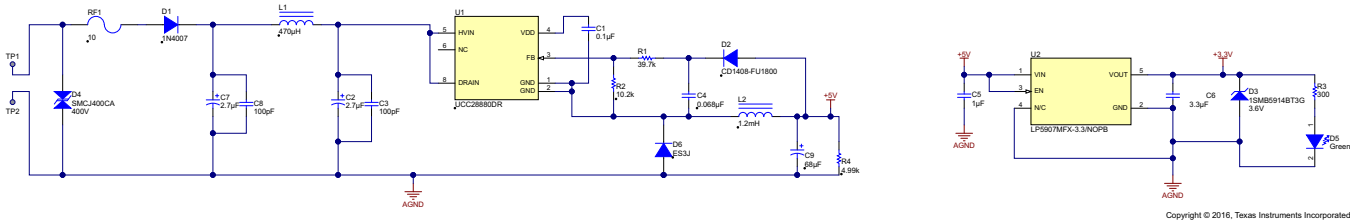


図 29. Schematic of Power Conversion Stage Using UCC28880

3 Hardware, Software, Testing Requirements, Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

表 4 lists connector details for this TI Design:

表 4. Connector Details for TIDA-00929

TYPE OF CONNECTOR OR PIN	R/W	CONNECTOR
Current signal	IN	TP5 and TP7
Power supply: AC input	IN	TP1 and TP2
Output flag	OUT	J3 (J3.1: GND, J3.2: Flag)
Spy-Bi-Wire	I/O	J2.1: GND
		J2.2: TEST/SBWTCK
		J2.3: Reset
		J2.4: 3.3 V
JUMPER SELECTION		
MSP430 internal comparator	—	Short J5.2 to J6.2 and J5.1 to J6.1
External comparator	—	Short J5.1 to J5.2 and J6.1 to J6.2
TEST POINTS		
Output from the differential gain stage	—	TP6
Output from the low-pass filter	—	TP4
Output from the band-pass filter	—	TP8
Output from the comparator	—	TP9
Reset switch	—	S1
Comparator threshold settings	—	R32

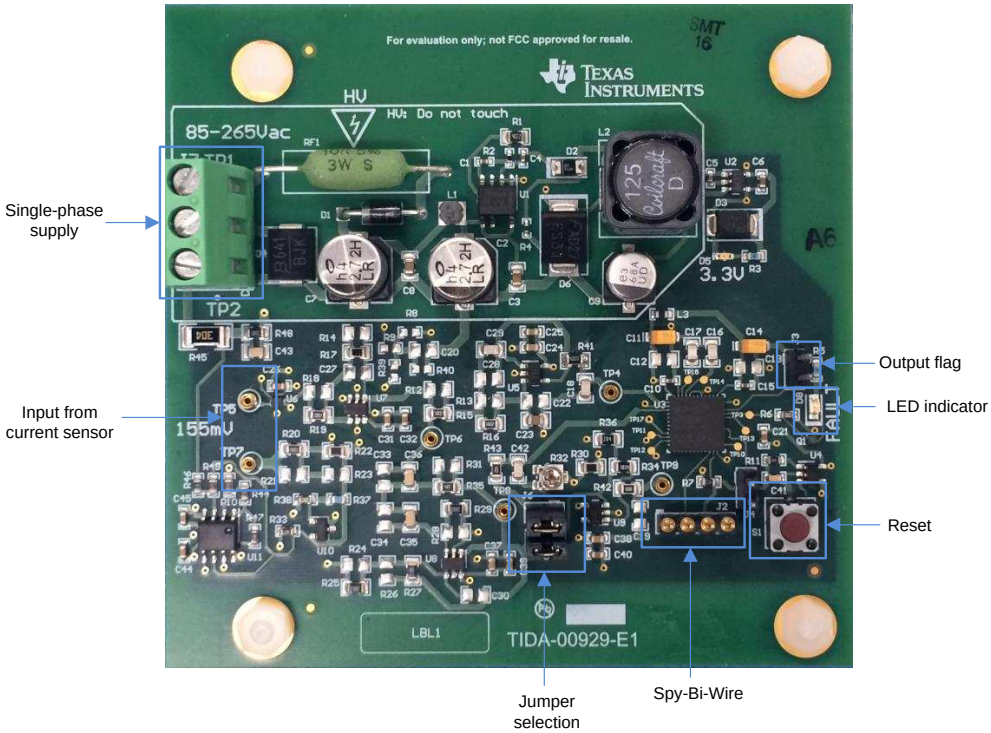


図 30. Diagram Showing Connectors

3.1.2 Software

3.1.2.1 Initialization

To use the full computation speed and ADC sampling, the internal DCO is set to maximum frequency, 16 MHz. Changing the DCO from the default value of 8 to 16 MHz is provided as follows:

```
// Clock System Setup
        CSCTL0_H = CSKEY_H;                     // Unlock CS registers
        CSCTL1 = DCOFSEL_0;                     // Set DCO to 1MHz
        // Set SMCLK = MCLK = DCO, ACLK = VLOCLK
        CSCTL2 = SELA__VLOCLK | SELS__DCOCLK | SELM__DCOCLK;
        // Per Device Errata set divider to 4 before changing frequency to
        // prevent out of spec operation from overshoot transient
        CSCTL3 = DIVA__4 | DIVS__4 | DIVM__4;   // Set all corresponding clk sources to divide by
4 for errata
        CSCTL1 = DCOFSEL_4 | DCORSEL;           // Set DCO to 16MHz
        // Delay by ~10us to let DCO settle. 60 cycles = 20 cycles buffer + (10us / (1/4MHz))
        __delay_cycles(60);
        CSCTL3 = DIVA__1 | DIVS__1 | DIVM__1;   // Set all dividers to 1 for 16MHz operation
        CSCTL0_H = 0;
```

- Fundamental frequency is set to either 50 or 60 Hz, which changes the ADC sampling rate and the buffer to capture analyzed data over a full cycle.
- Timer is set, which triggers ADC conversion at regular intervals. For 50 Hz, the frequency is set to 204.8 kHz to enable ADC conversion at 204.8 ksps. For 60 Hz, the ADC is sampled at 184.32 ksps.
- ADC is triggered by the timer, and upon its end of conversion, this triggers the DMA transfer. DMA is configured to transfer 512 samples every time. Once it transfers 512 samples of ADC results, a DMA interrupt is called.
- Configuring the comparator: If an internal comparator is used, then a port needs to be configured. COUT is used to capture number of pulses. For an external comparator, a port 2.0 needs to be configured to capture number of pulses.

3.1.2.2 Computation in Real-Time

Once the timer, ADC, and DMA are configured to operate in this sequence, the DMA interrupt is triggered every 2.5 or 2.77 ms depending on the frequency settings for the current signal. DMA transfer can be performed independent of the CPU, so it can be in LPM0 mode during a DMA transfer. Upon interrupt, the destination for the DMA transfer is swapped between the ping and pong buffer. Once the ISR is serviced, it wakes up the CPU from LPM0 mode. When CPU comes out of LPM0, it starts analyzing the data that have been capturing in 2.5 ms. FIR calculation, analysis of FIR result, updating the number of pulse train signals, and RMS calculation are performed, the results of which are stored in a buffer. Every half or full cycle, the analyzed data are further processed to formulate the algorithm for arc detection where each customer may have their own optimal method of interpreting the data.

3.1.2.3 Design of FIR Filter Using MSP-DSPLIB GUI

The design of the FIR filter for the MSP430 can be done using the Digital Signal Processing (DSP) Library for MSP Microcontrollers (MSP-DSPLIB), which provides highly optimized functions to perform many common signal processing operations. Using this GUI, FIR or IIR filters can be designed with ease.

図 31, 図 32, and 図 33 show FIR filters designed using MSP-DSPLIB, which are used for analysis in 3.2. Parameters of these three FIR filters are listed in 表 5

表 5. FIR Filter Parameters

PARAMETER	FIR-1	FIR-2	FIR-3
Type	High pass	Band pass	Band pass
Method	Exponential	Exponential	Exponential
Number of taps	30	30	30
Cutoff frequency	4889 Hz	10 to 99.99 kHz	10 to 70 kHz

To obtain a better frequency response from the FIR filter, a higher number of taps can be used. However, this increase burdens the processor by increased computation. For real-time FIR computation, make sure that FIR calculation and other miscellaneous computation are completed before the next DMA interrupt. LEA cycle count for FIR computation is given by 式 8:

$$\text{Cycles} = 17 + \frac{N}{2} \times \left(12 + 4 \times \frac{\text{Tap size}}{2}\right) \ldots \quad (8)$$

where:

- N is the FIR block size
- Tap size represents the order of FIR filter

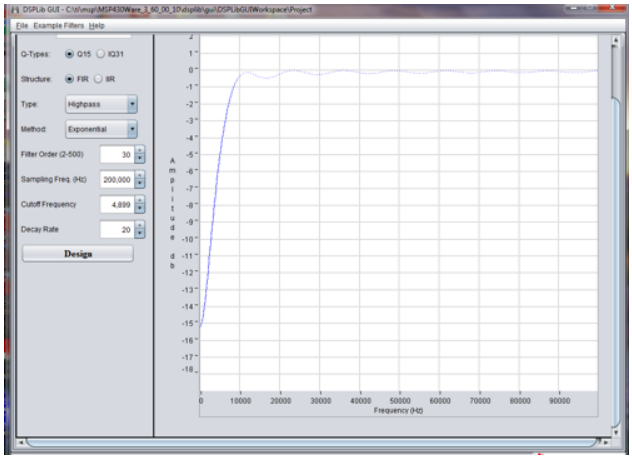


図 31. Example Showing Design of FIR Filter

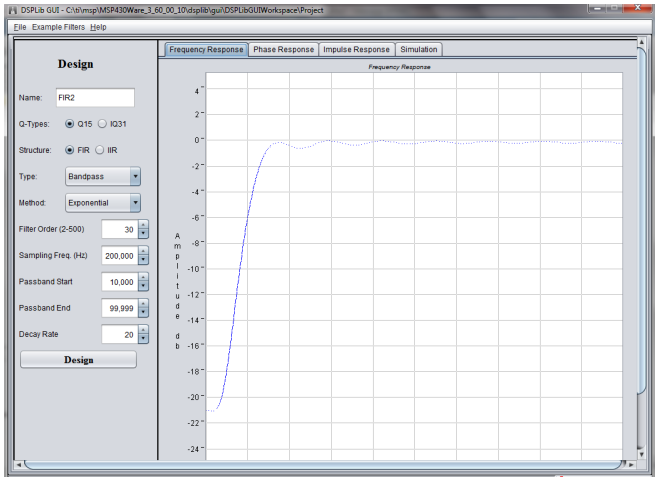


図 32. MSP-DSPLIB GUI for Designing Band-Pass Filter

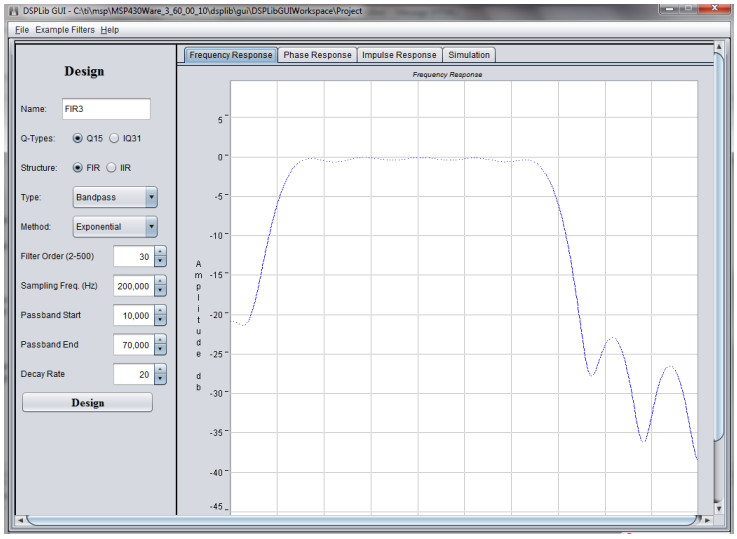


図 33. FIR Filter

3.2 Testing and Results

3.2.1 Functional Tests

- *Power*: Power to all the parts are tested by supplying a 110- or 230-V, 50- or 60-Hz signal.
- *Spy-Bi-Wire*: Using MSP-FET, the MSP430 is connected to the computer through Spy-Bi-Wire. Verify the connection by programming basic example codes. GPIO P1.1 is set to high to enable the analog switch, which bypasses input current signal on to the board.
- *Differential gain stage*: An input signal from a functional generator is given to the board, and output voltage at the TP6 is observed. Verify the input and output voltage swing, DC voltage offset, and gain bandwidth of the first stage by changing the amplitude and frequency of the input signal. 図 34 shows the frequency response obtained from the experimental setup.
- *Low-pass filter*: By sweeping frequency of the input signal, the output of the low-pass filter is measured, and frequency response is obtained for the frequency domain analysis as shown in 図 35.
- *High-pass filter*: Similar to the low-frequency path, the output of the high-pass filter is measured for a wide sweep of the input signal. Gain bandwidth of the high-pass filter stage is verified using this. 図 36 shows the frequency plot for time domain analysis.
- *ADC sampling*: The MSP is programmed to sample an analog signal from the low-pass filter at 204.8 ksps. A sample signal is given at the input and ADC results are being store and plotted to verify the dynamic sampling and sampling rate.
- *Pulse train signal*: The voltage threshold value for the output of the high-pass filter can be changed by varying R32. A pulse train signal can be generated by sending a high frequency at the input and by changing the threshold value. Pulse count values can be read from the MSP430 debugger, which counts pulses for a specific time interval of either 2.5 or 2.77 ms depending on the frequency settings.

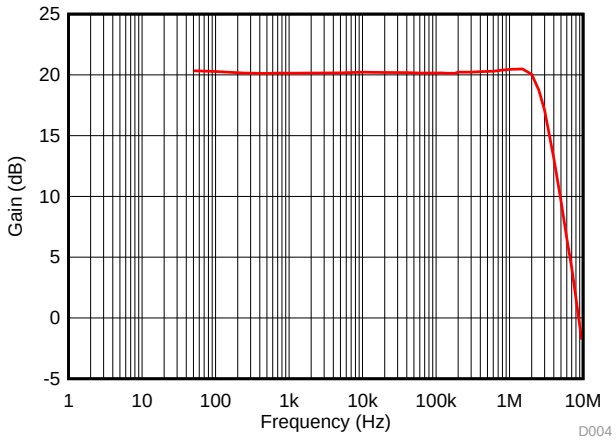


図 34. Frequency Response for Differential Gain Stage

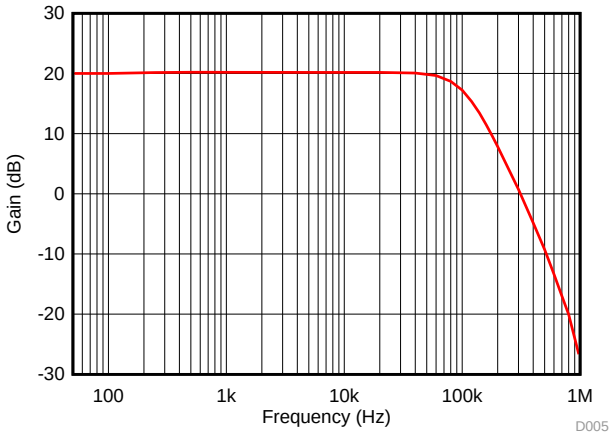


図 35. Frequency Response for Path 1 (Frequency Domain Analysis)

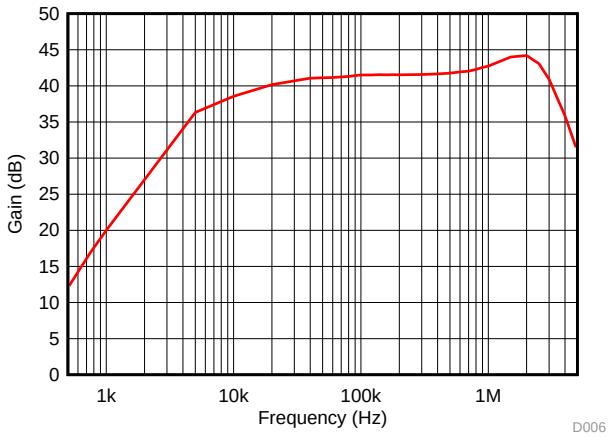


図 36. Frequency Response for Path 2 (Time Domain Analysis)

3.2.2 Performance Tests

Performance of the board has been verified to analyze typical arc signatures waveforms, which are obtained from a series arc generator.

3.2.2.1 Series Arc Generator Setup

図 37 shows the lab setup for generating a series arc. The arc generator consists of a stationary electrode and a moving electrode of copper and graphite material of 0.25" diameter. The two ends of the rods are connected in series with the 110-V AC and load. Moving rod is placed on a linear slide guide rail to adjust the distance between two rods to generate arcing. Current waveform during the series arcing is captured using two methods as shown in 図 38. Channel 1 shows the current measured using a clamp type current probe, which does not pass the high-frequency noise in the current. A shunt of 350 μΩ is connected in series with the arc generator, and voltage is measured across it, which is shown in channel 2. It clearly shows the high-frequency broadband noise in the signal along with the shoulder near zero crossing. Frequency content in this waveform is demonstrated in 図 24. The waveform captured using this setup has been used to analyze and test the TI Design, which is explained in 3.2.2.2.

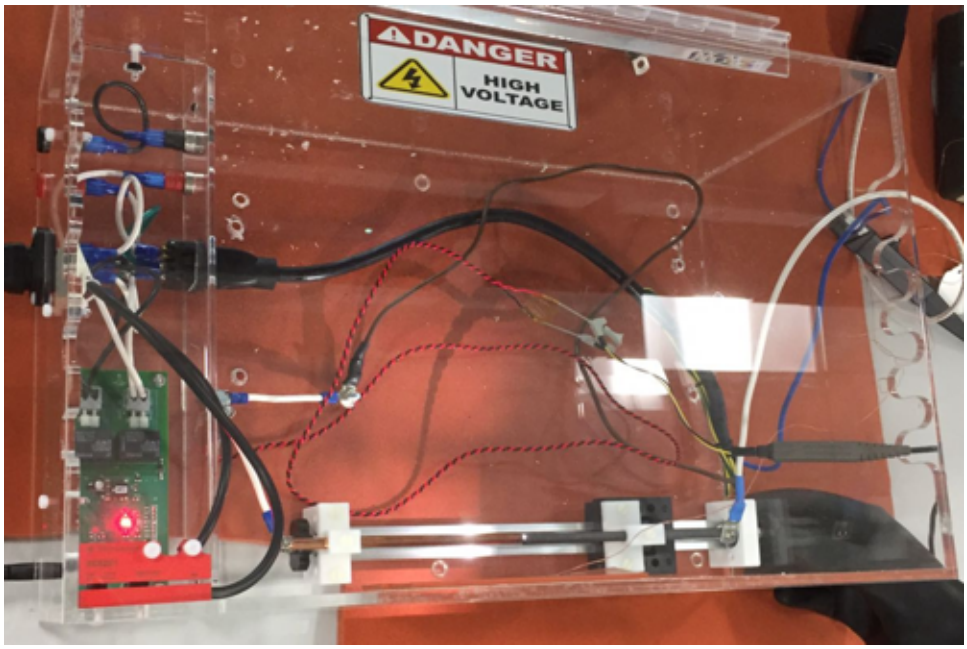


図 37. Arc Generator Setup

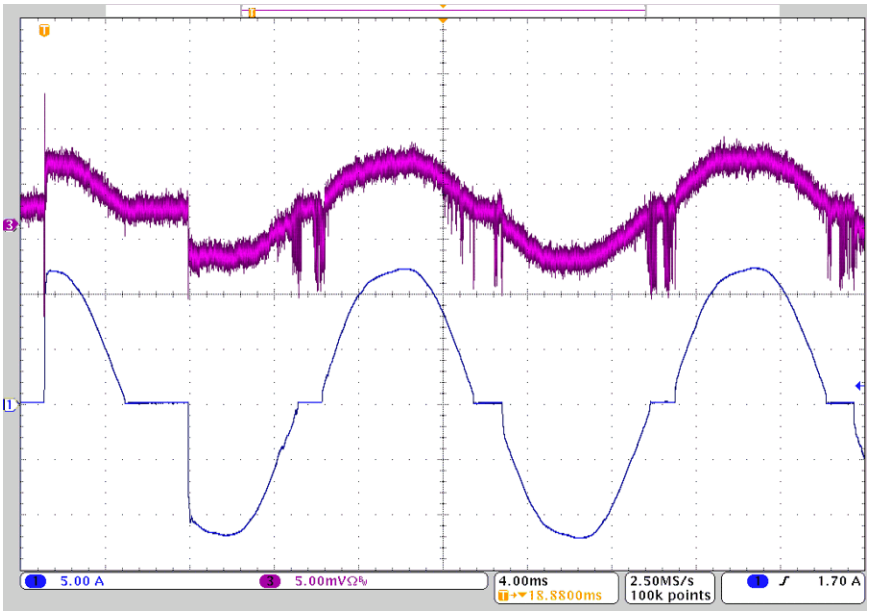


図 38. Current Waveform Captured From Arc Generator

3.2.2.2 Analog Signal Conditioning

To verify the functioning of various branches, the signal obtained from the arc generator has been emulated using an arbitrary function generator AFG3102. This generator has sample rate of 250 MS/s using a 14-bit resolution and 20 mVpp. 図 39 shows the experimental result for the frequency domain analysis. Channel 1 represents the voltage output form the differential gain stage (TP6), which has a DC shift of 1.6 V. After filtering the signal using a low-pass filter, data has been captured in channel 2. The low-pass filter with a cutoff frequency of 100 kHz is able to pass part of the broadband noise from the input signal.

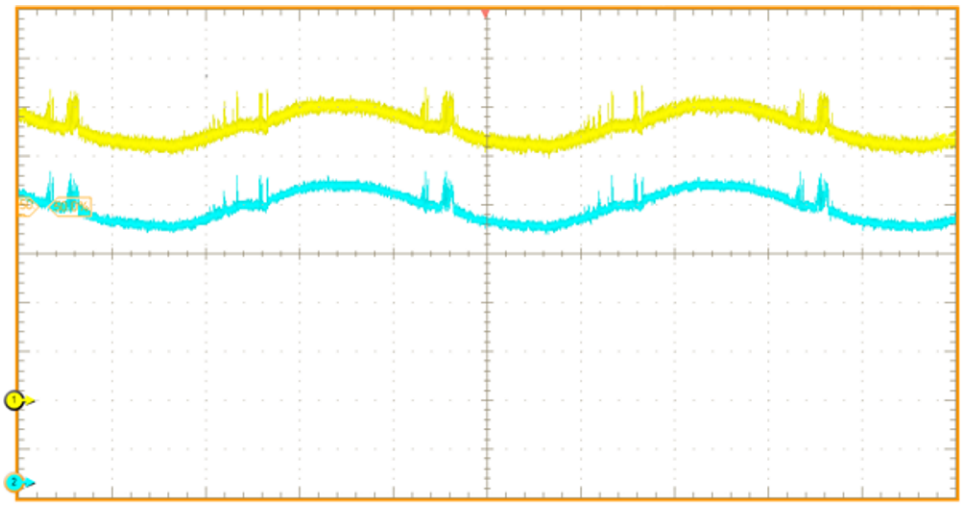


図 39. Performance of Low-Pass Filter

To verify the high-frequency signal path, the same current waveform is input to the board. 図 40 shows the voltage at the differential gain stage and the output from the high-pass filter. Only high-frequency broadband noise above 100 kHz has been passed through this stage, eliminating the DC shift and the fundamental component. High-frequency noise has been amplified by the gain stage of the filter to obtain a higher resolution.

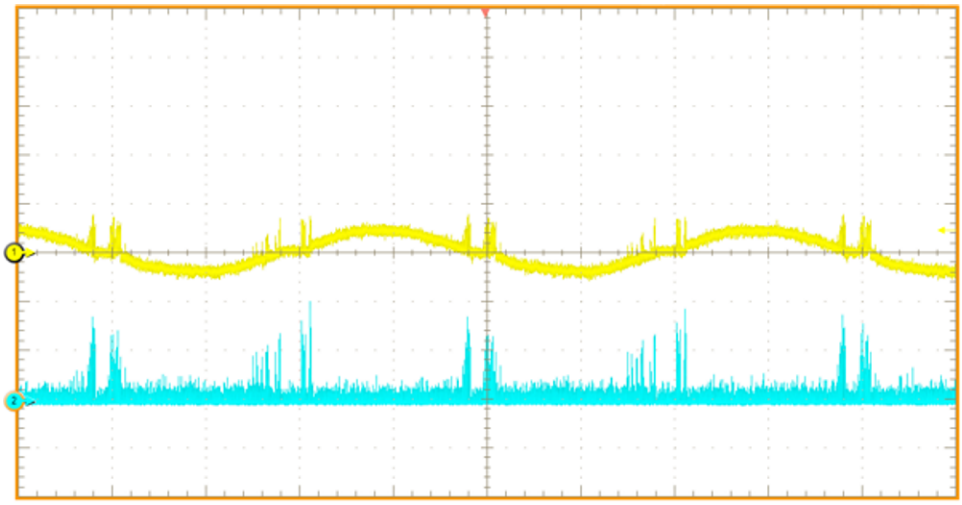


図 40. Performance of Band-Pass Filter

Generating a pulse train from the high-pass filter has been plotted in the following figures. 図 41 shows the pulse train with the input signal at the differential gain stage, and 図 42 shows with respect to the output of the high-pass filter.

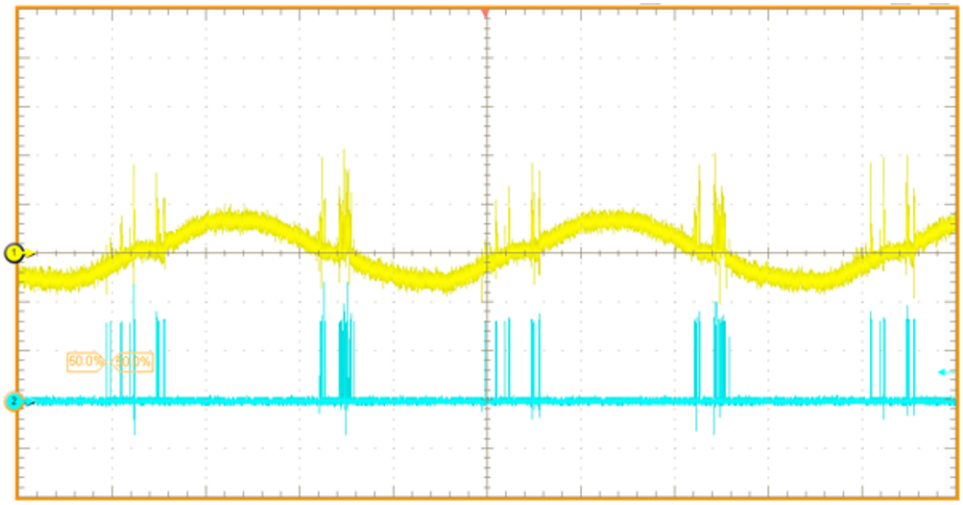


図 41. Pulse Train Generation Using External Comparator

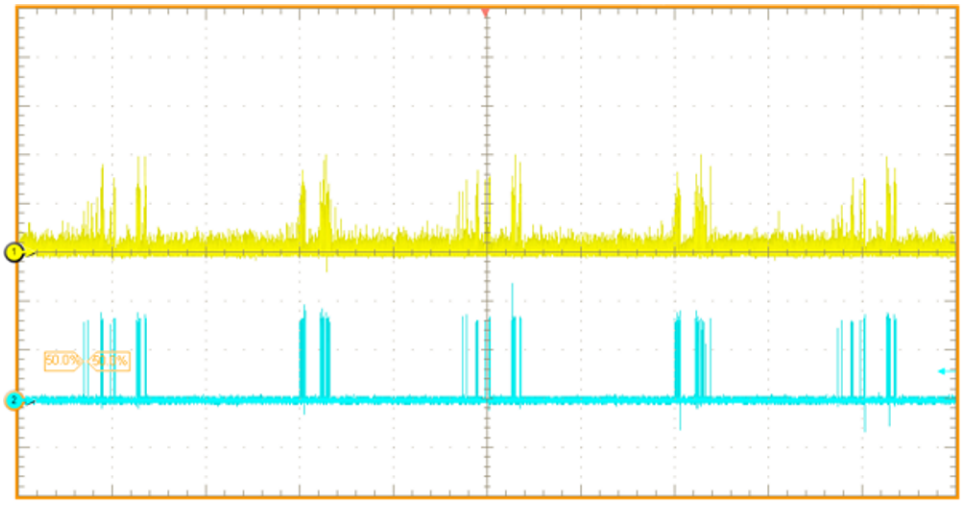


図 42. Time Domain Analysis

3.2.2.3 FIR Filter

To validate the functioning and analysis done by FIR, the performance of FIR filter in real time is captured for three different types of FIR filters designed using MSP-DSPLIB as discussed in 3.1.2.3. To perform this test, the result FIR is being transferred to FRAM memory every time the LEA completes the FIR filtering. Because FIR is performed for only 2.5 ms at a time, this is repeated for eight cycles and the results are stored in a FRAM buffer. This is potted to demonstrate the filtering using FIR. 図 43, 図 44, and 図 45 show the output of the filter for the same input signal using FIR-1, FIR-2 and FIR-3, respectively. These figures also show that the filtering in different segments take samples from previous buffers using a circular buffer to smoothly take over in the next cycle. This validates that division of fundamental cycle does not effect the overall performance.

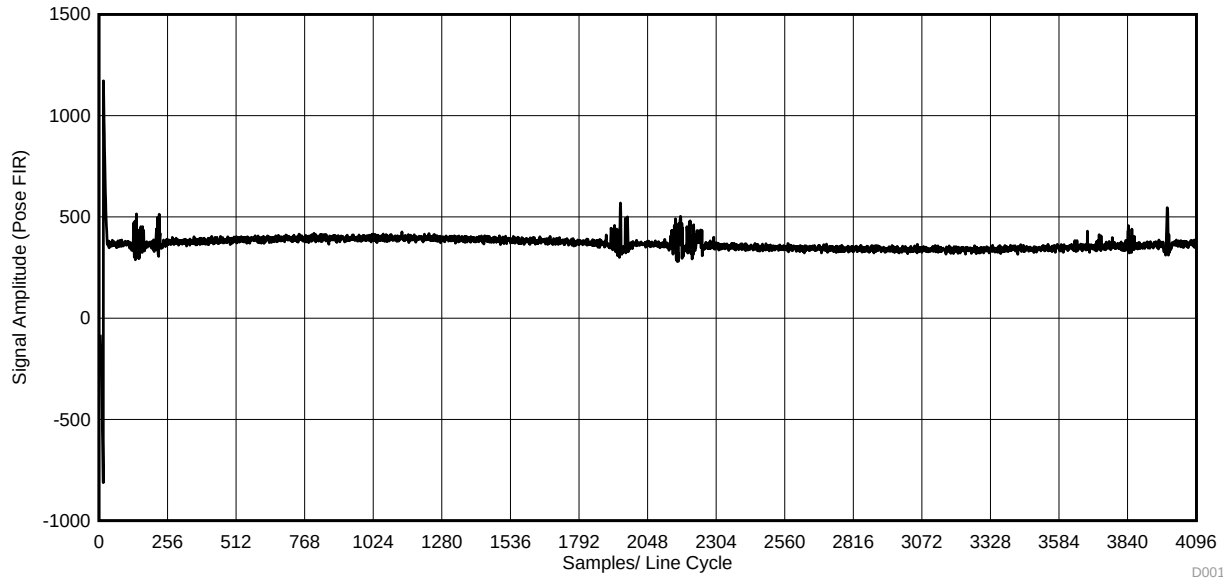


図 43. Output From FIR Filter 1

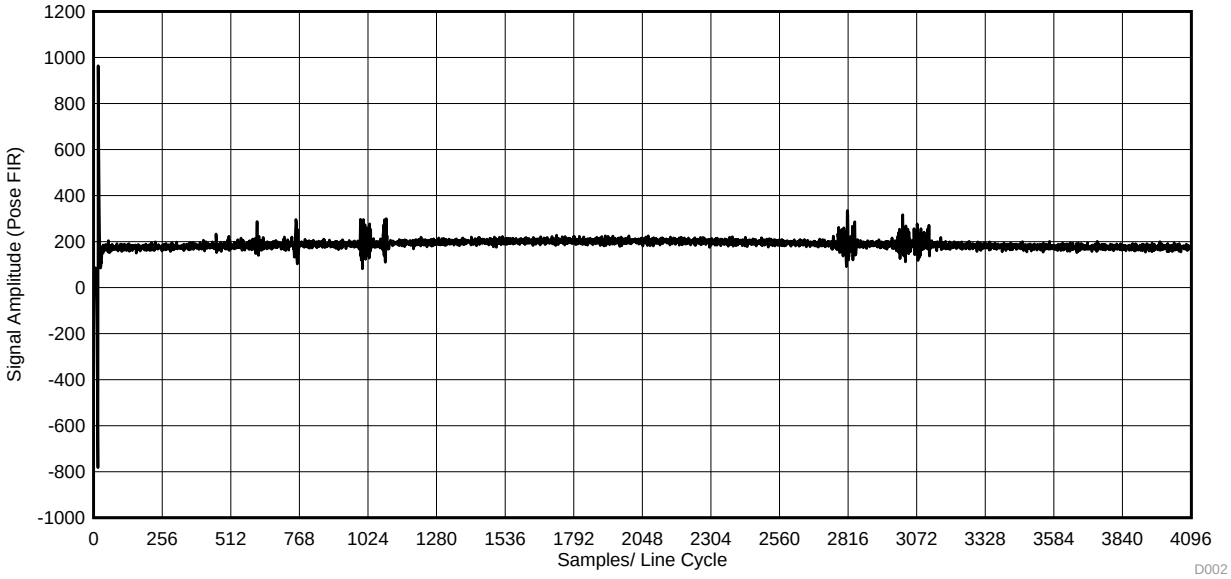


図 44. Output From FIR Filter 2

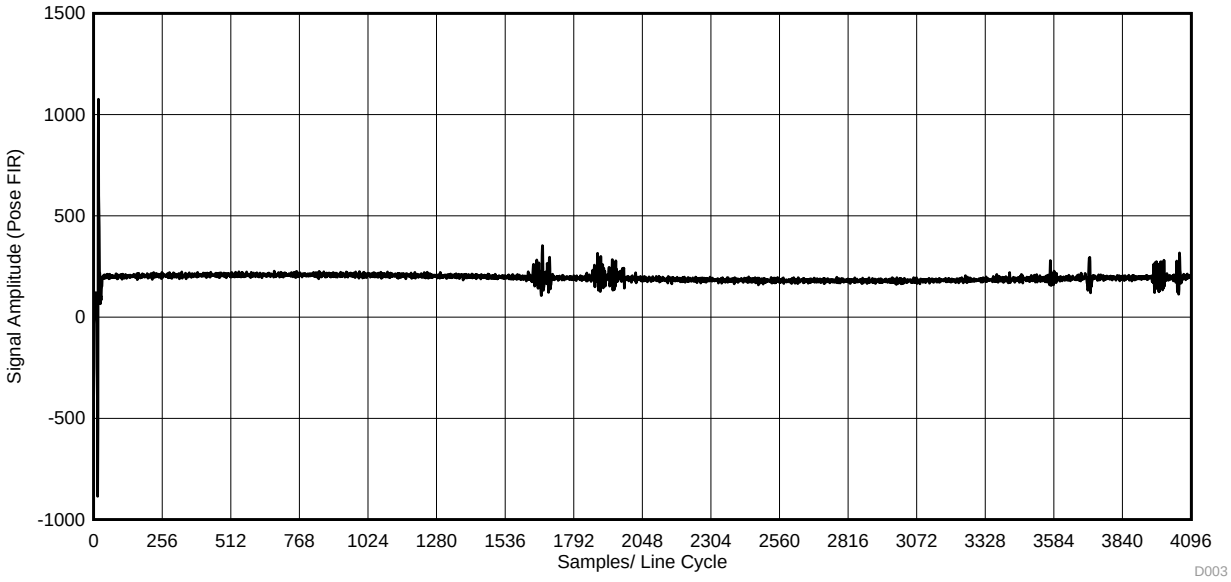


図 45. Output From FIR Filter 3

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-00929.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00929.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00929.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-00929.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00929.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00929.

5 Related Documentation

1. Texas Instruments, *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide*
2. Texas Instruments, *Benchmarking the Signal Processing Capabilities of the Low-Energy Accelerator on MSP430™ MCUs Application Report*
3. Texas Instruments, *OPA836 Low-Power Op Amp Applications Application Report*
4. Texas Instruments, *Using the UCC28880EVM-616 User's Guide*
5. Texas Instruments, *Designing for low distortion with high-speed op amps Technical Brief*
6. Texas Instruments, *Tiny, Universal Line to 3.3V/30mA Reference Design for Circuit Breakers*

5.1 商標

6 Terminology

ADC— Analog-to-digital converter

AFCI— Arc fault current interrupter

AFE— Analog front-end

BPF— Band-pass filter

CT— Current transformer

DMA— Direct memory access

FIR— Finite impulse response

FRAM— Ferroelectric random access memory

HPF— High-pass filter

ISR— Interrupt subroutine

LEA— Low-energy accelerator

LPF— Low-pass filter

LPM— Low-power mode

7 About the Authors

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8 General Texas Instruments High Voltage Evaluation (TI HV EVM) User Safety Guidelines

Always follow TI's setup and application instructions, including use of all interface components within their recommended electrical rated voltage and power limits. Always use electrical safety precautions to help ensure your personal safety and those working around you. Contact TI's Product Information Center http://support/ti./com for further information.

Save all warnings and instructions for future reference.

Failure to follow warnings and instructions may result in personal injury, property damage, or death due to electrical shock and burn hazards.

The term TI HV EVM refers to an electronic device typically provided as an open framed, unenclosed printed circuit board assembly. It is **intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise and knowledge of electrical safety risks in development and application of high voltage electrical circuits. Any other use and/or application are strictly prohibited by Texas Instruments**. If you are not suitable qualified, you should immediately stop from further use of the HV EVM.

1. Work Area Safety
    1. Keep work area clean and orderly.
    2. Qualified observer(s) must be present anytime circuits are energized.
    3. Effective barriers and signage must be present in the area where the TI HV EVM and its interface electronics are energized, indicating operation of accessible high voltages may be present, for the purpose of protecting inadvertent access.
    4. All interface circuits, power supplies, evaluation modules, instruments, meters, scopes and other related apparatus used in a development environment exceeding 50Vrms/75VDC must be electrically located within a protected Emergency Power Off EPO protected power strip.
    5. Use stable and nonconductive work surface.
    6. Use adequately insulated clamps and wires to attach measurement probes and instruments. No freehand testing whenever possible.
2. Electrical Safety
   As a precautionary measure, it is always a good engineering practice to assume that the entire EVM may have fully accessible and active high voltages.
    1. De-energize the TI HV EVM and all its inputs, outputs and electrical loads before performing any electrical or other diagnostic measurements. Revalidate that TI HV EVM power has been safely de-energized.
    2. With the EVM confirmed de-energized, proceed with required electrical circuit configurations, wiring, measurement equipment connection, and other application needs, while still assuming the EVM circuit and measuring instruments are electrically live.
    3. After EVM readiness is complete, energize the EVM as intended.

   WARNING: WHILE THE EVM IS ENERGIZED, NEVER TOUCH THE EVM OR ITS ELECTRICAL CIRCUITS AS THEY COULD BE AT HIGH VOLTAGES CAPABLE OF CAUSING ELECTRICAL SHOCK HAZARD.
3. Personal Safety
    1. Wear personal protective equipment (for example, latex gloves or safety glasses with side shields) or protect EVM in an adequate lucent plastic box with interlocks to protect from accidental touch.

Limitation for safe use:

EVMs are not to be used as all or part of a production unit.

改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision D (March 2018) から **Revision E** に変更 **Page**

- information regarding PMP21750 to *Power Supply* for designs requiring up to 30 mA 追加 33
- the PMP21750 Test Report to *Related Documentation* 追加 45

Revision C (July 2017) から **Revision D** に変更 **Page**

- リビジョンBに復帰 1

Revision B (June 2017) から **Revision C** に変更 **Page**

- リファレンス・デザインのブロック図 変更 1

Revision A (February 2017) から **Revision B** に変更 **Page**

- 現在のPCBレイアウトを反映して基板の画像を 変更 2
- power supply definition in *Arc Fault Capture* 変更 3
- all instances of "LEA_SC" to "LEA") 変更 11
- *Diagram Showing Connectors* with current PCB layout 変更 34

2016年12月発行のものから更新 **Page**

- 現行のスタイル・ガイド・テンプレートに合わせて言語と画像を 変更 1

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