参考資料

TI Designs: TIDA-00792
マルチセルの36V～48Vバッテリ管理システムのリファレンス・デザイン

概要

TIDA-00792 TI Designは、12～15セルのリチウムイオンまたはリチウム鉄リン酸塩ベースのバッテリに対して監視、平衡化、一次保護、測定を行います。この基板は、産業用システムの筐体内に取り付けるよう設計されています。このリファレンス・デザインのサブシステムは、バッテリ保護機能とパラメータによる測定設定機能を備え、コードの開発が不要で、ハイサイドの保護スイッチングにより単純なPACK-基準のSMBus通信を行います。これにより、保護中であってもバッテリの状態を確認できます。

リソース

TIDA-00792	デザイン・フォルダ
bq76940	プロダクト・フォルダ
bq78350-R1	プロダクト・フォルダ
bq76200	プロダクト・フォルダ
CSD19536KTT	プロダクト・フォルダ
CSD13381F4	プロダクト・フォルダ
TIDA-00449	ツール・フォルダ

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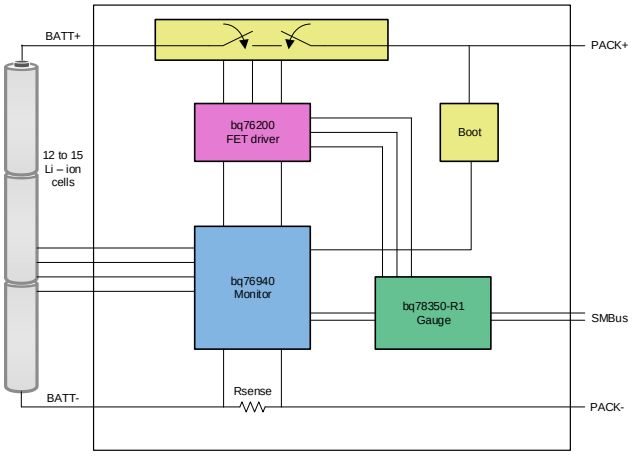
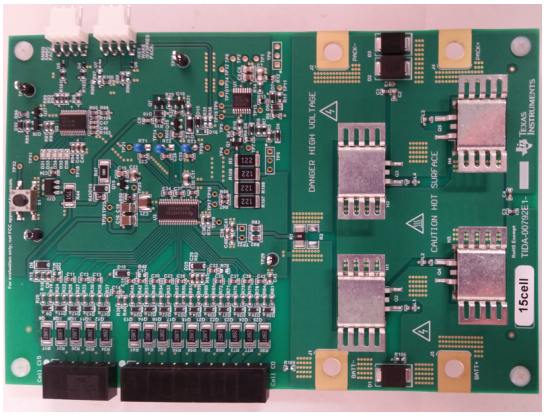
- 12～15セルのリチウムイオンおよびリン酸塩バッテリの管理システム
- NチャネルMOSFETを使用したハイサイド保護スイッチング
- セルの平衡化によるバッテリ寿命の延長
- 容量測定によるシステム実行時間の推定
- サブシステム回路デザインがテスト済みで、GUIおよび導入ガイドが付属

アプリケーション

- 産業用バッテリ・パック
- 家電機器用バッテリ・パック
- E-モビリティ
- 据え置きエネルギー・ストレージおよびUPS





1 System Description

This system design is for a 48-V nominal lithium-ion or lithium-iron phosphate battery management system (BMS) to operate over a range of approximately 36 V to 50 V using 12 to 15 cells depending on the selected battery chemistry. The design concept is for a board which could be selectively populated and configured to support a variety of systems requiring a similar battery with a variety of current requirements where form factor optimization is not required. Cell voltage, pack current, and temperature are measured and monitored to confirm the battery is operating within normal conditions. Deviations from normal can be alerted and communicated to a host system and, if they continue, the battery can be protected from continued charge or discharge. Protection switching uses high side N-channel field-effect transistors (FETs) to allow a wide selection of FETs and to maintain low-side referenced communication even during protection. Battery state-of-charge is provided using compensated end-of-discharge voltage (CEDV) or end-of-discharge voltage (EDV) gas gauging. Battery limits are set with parameters that avoid code development. The design may find use in battery packs for industrial, appliance, e-mobility or stationary energy storage, and UPS system applications whether in its rectangular shape or as a reference for a form-factor tailored solution.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Input power source	Lithium-ion or Lithium-iron phosphate battery	2.2.1
Nominal voltage	36 to 48 V	2.2.1
Cell count	12 to 15	2.2.1
Protections	Over- and under-voltage, over- and under-temperature, over current, short circuit discharge	2.2.4
Cell balancing	Required, 100 mA	2.2.9
Gauging	1 to 30 Ah	2.2.3
Communication	State of charge and status available when protected	2.2.5
Sleep mode	Required	2.2.8
Wake-up	Electrically initiated	2.2.8
Operating temperature	0°C to 50°C	2.2.2
Working environment	Indoor and outdoor	2.2.2
Form factor	4×6-inch rectangular PCB	4.3

2 System Overview

Industrial packs may be required in a variety of settings. This TIDA-00792 TI Design represents a board which can be configured into a cabinet of equipment to provide a 48-V battery for operation during frequent power loss or moving the equipment. The battery protection systems are available to keep operation in the design range of the battery. The communication path provides battery data such as state of charge to determine if the equipment is ready to go mobile. The high-side switching allows communication with a battery even if the battery is protected and allows the system to determine an appropriate recovery scenario. Lifetime data maintained in the battery can help maintenance and planning determine if a system requires replacement. A cabinet or chassis installation where the battery subsystem and management system board are mounted with other system components is an example implementation of this TI Design. Cooling may be provided for the boards and cells by additional equipment in the cabinet.

Similar to industrial applications, batteries in appliances allow portability or backup of operation in case of power loss. More types of equipment that are traditionally connected with cords may become more portable with the lighter weight of lithium-ion (Li-ion) cells. Appliances that may have operated at lower voltages may move to higher voltages to reduce the current requirements at the same power or increase the system output power. In appliance applications, space is more likely to be limited and the cooling restricted. The TIDA-00792 TI Design may be more of a reference schematic for a form factor or feature optimization in these systems. In applications where the battery is removable, the option of having fewer terminals may be attractive and the high-side switching is very important.

E-mobility applications that use heavy low-voltage batteries may have moved to the lighter Li-ion technology and seek out higher voltages to reduce current at the same power or increase power at the same current. For larger systems, the battery management system (BMS) may be a subsystem in a chassis with other equipment similar to the industrial application. For smaller systems, the battery may be removable and packaged like the appliance.

Stationary energy storage and UPS systems may use a 48-V battery for the same reasons as other equipment, to reduce currents for a given power compared to lower voltage systems. This TIDA-00792 TI Design is more applicable to renewable and stationary energy storage where the system cycles frequently compared to a backup battery where the system is rarely discharged and the gauge may not learn the battery capacity. In an energy storage system, the BMS may be packaged in a chassis with cooling available.

2.1 Block Diagram

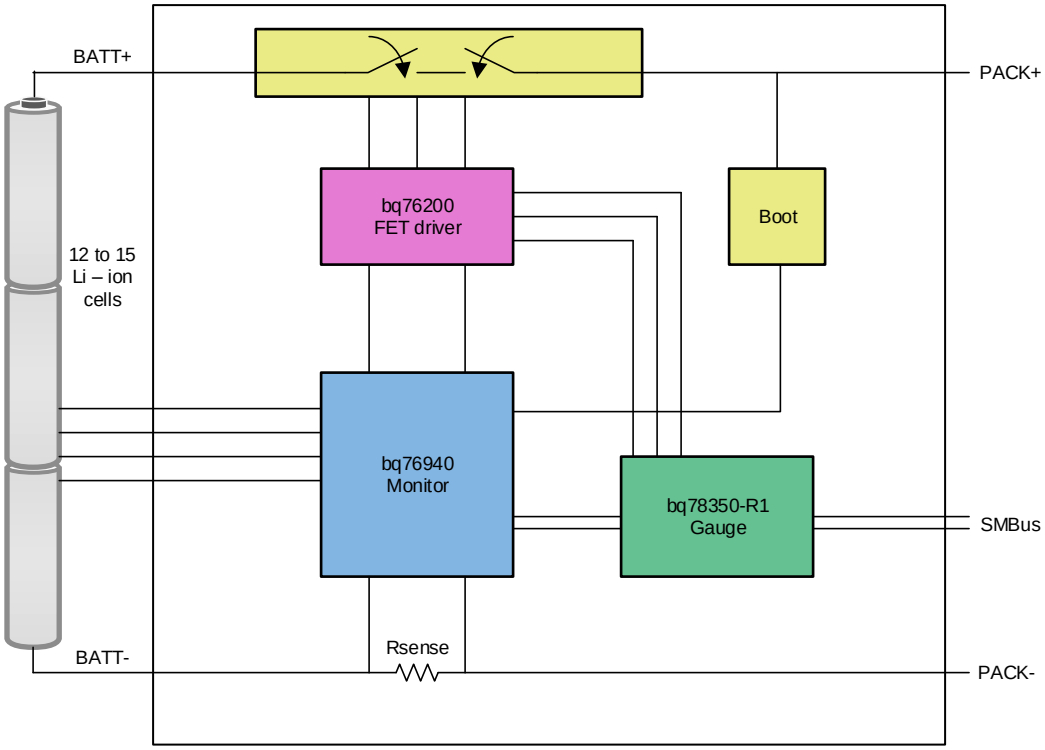


図 1. TIDA-00792 Block Diagram

2.2 Design Considerations

The TIDA-00792 design is intended for a battery subsystem for an industrial battery. Additional components may be required to customize this design for a specific use. The design does not include redundant components for reliability or include fuses required to be included elsewhere in the system.

2.2.1 Voltage and Cell Count

A variety of lithium ion (Li-ion) and lithium iron phosphate ($LiFePO_4$) cell types can be used to provide a 48-V battery depending on the requirements of the system and whether the voltage is a nominal or maximum. Various Li-ion chemistries provide cells which can be considered 3.6-V or 3.7-V cells with 4 V in the normal operating range. $LiFePO_4$ cells may be considered 3.2 V cells. At 4 V per cell, a 12-cell battery is 48 V, which means that 15 cells would be required at 3.2 V per cell. This design supports 12 to 15 cells to allow selection of various voltage cells and counts depending on the exact operating voltage range required of the battery.

The bq76940 battery monitor provides support for 9 to 15 cells and includes current measurement and protections. This device has been selected for use in this design to cover the 12- to 15-cell requirement. The design can support a wider voltage range with this device selection, although this feature is not the focus of this design. Cell count is reduced by shorting the inputs of the appropriate pins on the AFE as shown in the bq76940 datasheet[1]. 図 2 shows the input filter section component configuration for cell 14

when all cells are used. 図 3 shows the filter section component configuration when cell 14 is not used. The filter output is shorted with R70. The reader may notice that the R70 0-Ω resistor can be populated at C9 for the same connection. This technique can be used to further reduce the cell count. This design requires that the cell connection be duplicated at the input terminal to complete the cell balance path. Another design alternative is to include a 0-Ω resistor to make that connection on the board.

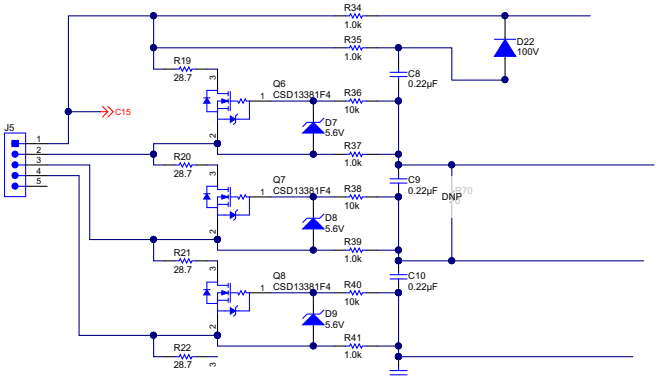


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図 2. Normal Cell Connection

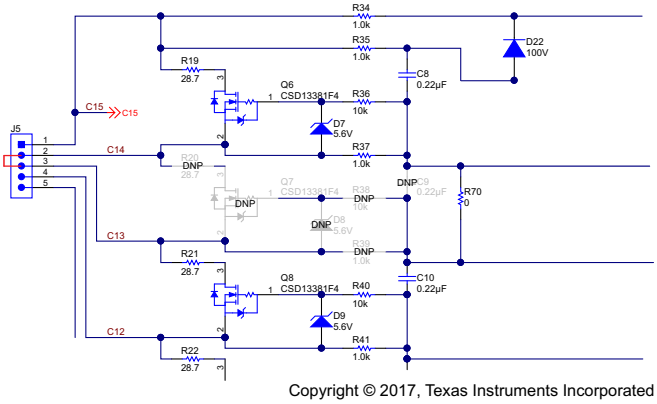

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図 3. Unused Cell Connection

2.2.2 Environment

Because this design is for an industrial battery, the operating conditions are wider than would be expected with an office environment; however, the system must be able to support the operating range of the cells it supports. Operation can be inside or outside, but the battery still requires a protective enclosure to protect against shorts. In the case of a cabinet-mounted installation, cooling may be provided separately for the electronics and the cells, which allows the board to have a different environment from the cells. At the same time, components on the board dissipate heat and will be derated. A 0ºC to 50°C operating temperature has been assigned to the board. Design of an enclosure with cooling and filtering and any board coatings are not part of this design.

2.2.3 Battery Gauging

A method to gauge the battery is required because the system must provide a state of charge. A microcontroller (MCU) may be able to provide a voltage-based estimation of the charge, but that data must be developed and built into the controller program. The bq78350-R1 gas gauge supports the bq76940 device and provides gauging with coulomb counting and either an end-of-discharge voltage (EDV) or compensated end-of-discharge voltage (CEDV) discharge termination. The state of charge can be estimated at reset from chemistry data loaded into the bq78350-R1 gauge. The gauge has a capacity of up to 320 Ah, which easily supports the 30 Ah required for this design.

2.2.4 Protections

The selected bq78350-R1 gauge implements protections based on data received and parameters set in its data flash memory. The device calculates limits for cell overvoltage (COV), cell undervoltage (CUV), overcurrent charge (OCC), overcurrent discharge (OCD), overtemperature (OT), and undertemperature (UT) based on calibrated values for the individual board. Hardware limits from the bq76940 have a factory calibration and are configured through the gauge by parameters. The gauge uses fast current comparators for short-circuit discharge protection (SCD) and fast overcurrent discharge (OCD) labeling these as ASCD and AOLD. The AFE OV and UV are used as secondary limits labeled SOV and SUV. The designer must be certain to configure the limits appropriately for the cells, features, and limits appropriate for each design implementation.

2.2.5 Communication

The bq78350-R1 provides communications through SMBus with a defined data structure. Details of the communication are provided in the *bq78350-R1 technical reference* manual[2]. SMBus is a ground referenced communication bus which can be supported by most processors. The ground reference and requirement for communication during protection requires either an isolator, which is powered on both the gauge and host side, or high-side protection switching. This design uses high-side protection to allow the simple communication bus connection and avoid the power required for the isolator.

2.2.6 High-Side Protection Switching

With high-side protection switching selected, a method to translate the low voltage signals to the battery level and provide a drive voltage above the battery is required. The bq76200 is selected to provide a compact solution with a charge pump for a charge and discharge field-effect transistor (FET) drive, a P-channel precharge control, and an internal switch for a voltage divider to monitor the PACK+ voltage.

N-channel FETs are supported by the bq76200 for the charge and discharge protection switches. 100-V FETs provide a double margin for the 48-V battery. FET selection frequently involves a tradeoff between a variety of factors including cost, $R_{DS(ON)}$, and power tolerance. Thermal management can be key to a successful product. Although a single FET may handle a high current value, it may not be possible to get the power out of the FET in a given design. Multiple FETs may be used to distribute power to keep point heat down. Despite not having a specified maximum current, which is certainly a point to check in any product design, this design uses a 1C rate for the 30-Ah capacity, or 30 A. A single FET can handle this current but two FETs are used in parallel to distribute the heat. The design uses TO-263 surface-mount FETs for a variety of options, but the CSD19536KTT FET has been selected. This FET can take up to 192 A at a case temperature of 100°C. The pair of FETs can handle higher current than required for this design as specified in the *Test Results* section of *10-s Battery Pack Monitoring, Balancing, and Comprehensive Protection, 50-A Discharge Reference Design*[10].

The FET gates are protected from transients with a Zener diode as described in the *bq76200 Beyond the Simple Application Schematic* application note[3]. The Zener diode and resistor between DSG and PACK pins are used to reduce switching losses inside the part and 620-Ω resistors are selected for the gate drive. Ferrite beads are used to avoid oscillations between the FETs during switching without significantly adding to the DC resistance.

2.2.7 Precharge Circuit

A precharge circuit provides a low current to charge deeply discharged cells if the charger does not provide reduced current. The bq76200 controls a P-channel FET with current limiting through power resistors. The FET must handle the high voltage of the system with some transient tolerance, but current is low. A signal FET and four parallel 1-W resistors have been selected for the design. The power in the resistors depends on the voltage applied, the difference between the battery pack, and the charger voltage. The batteries are not be allowed to go to 0 V without a permanent failure, but the minimum level may depend on the cells or the customer. In this design, a 25-V difference has been selected as well as a nominal 50% derating on the resistor power. The resistors are specified as 1.2 kΩ giving 0.52 W with the 25-V differential. The resulting peak precharge current is 83 mA or a very low C/360 rate for the specified 30-Ah pack. A higher precharge current requires more dissipation on the board.

2.2.8 Sleep and Wake-up Circuit

The bq78350-R1 includes a sleep mode to reduce power and also provides a shutdown mode which turns off the AFE.

With the AFE off, a method is required to boot the bq76940 and wake the battery. In systems with a host that is powered externally, the host can boot the bq76940 device with a low-voltage DC signal. Component patterns are provided in the design to provide a voltage-limited signal to the TS1 pin of the bq76940 for boot. 図 4 shows an example of the low-voltage boot circuit included in the design. The circuit is simple and has not been assembled for test on this board.

Other systems may require the battery to boot from application of a charger or test voltage from the charger. 図 5 shows a circuit implementation to boot from the charger. After some time with the battery off, PACK+ approaches PACK– potential and C36 charges to the battery voltage. A sufficient rise in the PACK+ voltage to create a drop across R79 as C36 discharges turns on Q23. Q22 comes on as a source follower and provides current into D25 and the TS1 pin to boot the part. D26 limits the voltage available to the TS1 pin when the PACK+ voltage is high. When the part is booted and the REGOUT voltages comes on, Q25 turns on to pull down the gate of Q22 to turn off the voltage to TS1 so that temperature measurements are not influenced until Q23 turns off.

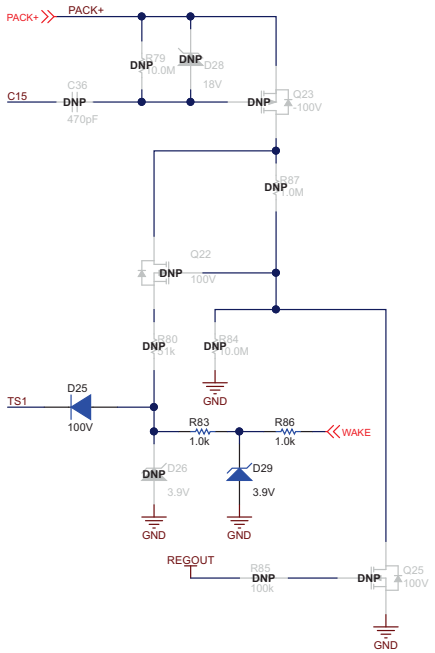

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図 4. Low-Voltage Boot Option

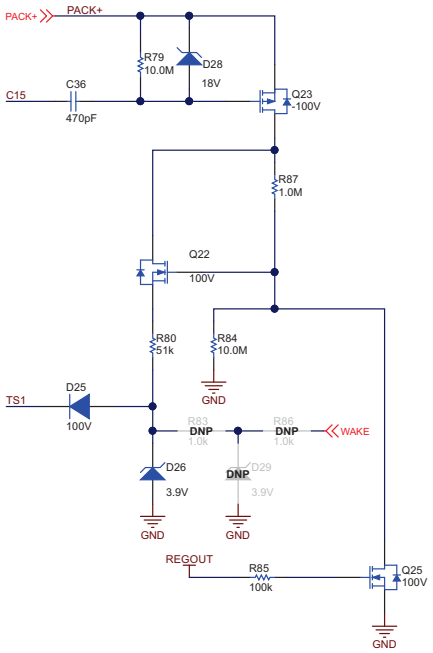

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図 5. PACK+ Boot Circuit

2.2.9 Cell Balancing

Cells matched in capacity and state of charge operate in series with each cell reaching full charge at the same time and reaching fully discharged at the same time. A group of cells may be mismatched in capacity or state of charge. Cells mismatched in capacity are limited in operation by the lowest capacity cell. When that low-capacity cell is fully charged or discharged, use of the battery must stop. State-of-charge mismatch limits the capacity which can be used in the pack even though all cells have more capacity. The charge must stop when the cells with the highest charge reach maximum voltage and the discharge must stop when the cells with the lowest charge reach minimum voltage. Cells which are

perfectly matched at the time a battery pack is assembled may become mismatched over time through different self-discharge rates, including those induced by differential temperatures in the battery pack and different electrical loads on the cells. Maintaining balance between the cells helps extend the usable life of the pack. Balancing can be done with either active or passive balancing. Passive balancing dissipates some energy from a higher capacity cell as heat, typically by bypassing some of the charge current around the cell. Passive balancing can operate without charge, but because this is a loss of energy, this is usually done during charge. Balancing based on voltage is typically done near the end of charge when currents and voltage differences from I × R drops are smaller. Passive balancing helps match the state of charge of the cells when fully charged; it cannot help with capacity mismatch. Active balancing transfers charge from one cell to another and can be used to extend the run time of batteries with mismatched cell capacities. Active balancing circuitry can be complex, but the balance currents can be high because energy is transferred rather than dissipated as heat.

The bq76940 contains a passive cell-balancing mechanism which is controlled by an algorithm programmed into the bq78350-R1 device. The balancing algorithm operates during charge and is configured by parameters, for which an additional description can be found in the *bq78350-R1 technical reference* manual[2]. An example of a differential load is present in the bq76940. The datasheet shows an increased load dI_{ALERT} of 15 µA typical on the lower cell group when the ALERT output is high. The ALERT output is set by the coulomb counter ready flag and cleared by the gauge. If ALERT is left on half of the time, a capacity offset of 5.4 mAh develops over one month. The internal cell-balancing current of the bq76940 device is limited by the architecture of the part. If the balance current is 2 mA, and because the bq76940 duty cycles balancing at 70% for measurement and the balancing can only perform on every other cell, the process requires $(5.4\text{ mAh per month}) / (2\text{ mA}) / (0.7) / (0.5) = 7.7\text{ h per month}$ to balance out that differential load. The amount of balancing time per charge cycle or the balancing current required depends on the frequency of charge. The bq76940 is often used with external balance due to its low internal-balancing current. This design requires 100-mA balance current. At 4.1 V, a 28.7-Ω resistor provides 143 mA of current, with the 70% duty cycle the average is 100 mA. Power is 0.4 W average so a 0.75-W resistor is selected.

2.2.10 AFE Circuit Design

The bq76940 AFE circuit design is selected using the considerations in the *bq769x0 Family Top 10 Design Considerations* application report[4] and by referring to the datasheet[1] and the *bq76930 and bq76940 Evaluation Module* user's guide[5]. R_f and C_f use the typical values of 1 kΩ and 10 µF. R_C uses the 1-kΩ value and C_C is selected as 0.22 µF. Even though the input filter is complex, the simple time constant such as VC0 allows 56 time constants in the 12.5-ms settling interval. Cell balance current has been selected as 100 mA using a 28.7-Ω resistor in 2.2.9. N-channel balancing is selected based on Section 4 *Cell Balance* and Section 10 *Random Cell Connection – Within Limits* of the bq76940 application report[4] to reduce stress on the inputs during cell connection. With the segmented connectors for the cells, additional components for protection from random cell-connection stresses have not been included in the design. The CSD13381F4 FET has been selected for the balancing FET because it has a small size, > 2-A current capability, and an $R_{DS(ON)}$ specified at 1.8 V and 0.5 A. The common gate protection components from Section 4 *Cell Balance* of the application report[4] are used.

The part is not used to drive FETs directly, which means the REGSRC voltage range is not a concern; however, the REGSRC does use a diode in the drain of an external follower FET. Normal supply current for the gauge is less than 1 mA and flash write current is 10 mA max, so the 1-kΩ resistor selected for the drain of the FET drops 10 V and dissipates 0.1 W. Selecting a resistor for the maximum 20 mA of the REGOUT supply drops 20 V and dissipates 0.4 W. A higher-power resistor is selected for derating.

The remaining sections of the AFE are supported with the normal connections described in the datasheet. Thermistors are used for sensing cell temperature and leaded parts are used under the expectation that long lead parts can be attached to cells.

2.2.11 Gauge Circuit Design

The circuit design for the gas gauge follows the datasheet[6] and EVM[5]. TPD1E10B06DPYT electrostatic discharge (ESD) protectors are used on the communication lines and external inputs with a series resistor to the gauge. The /KEYIN and /PRES inputs are provided with an option to be tied to ground when not in use. Battery voltage sensing with a FET switch and PACK+ sensing through the bq76200 pack monitor feature is provided using low-temperature coefficient resistors. Light-emitting diodes (LEDs) are used and powered from a high-gain NPN transistor referenced to the AFE 3.3-V CAP1 voltage.

Pullup resistors for the open-drain outputs are selected to give a voltage above V_{IH} of the bq76200 device. A smaller value is selected to operate near the transistor-specification maximum V_{GSTH} voltage for the VEN pin, which also drives the Q27 FET gate for the battery switch.

2.3 Highlighted Products

The system contains the following highlighted products, which provide most of the features of the design and determine the overall system performance:

- bq76940 battery monitor
- bq78350-R1 battery management controller
- bq76200 FET driver

2.3.1 bq769409 to 15-Series Cell Li-Ion and Li-Phosphate Battery Monitor

The bq76940 is an analog front end (AFE) for lithium-ion and phosphate cells. The device supports 9 cells to 15 cells providing measurement of individual cell voltages. A coulomb counter is provided for current measurement. Three thermistors are provided for temperature measurement. Communication of measurements runs through a digital interface. Hardware protection features are configured by registers set by the system controller and automatically switch off charge and discharge controls:

- Overcurrent in discharge (OCD)
- Short circuit in discharge (SCD)
- Overvoltage (OV)
- Undervoltage (UV)

2.3.2 bq78350 CEDV Li-Ion Gas Gauge and Battery Management Controller

The bq78350 is a battery management controller companion to the bq769x0 family of AFE protection devices. This device provides a comprehensive set of battery management system (BMS) subsystems. The BMS control firmware is preprogrammed and configured by parameters to allow faster time-to-market. The bq78350-R1 provides an accurate fuel gauge and state-of-health (SoH) monitor, as well as cell balancing and a full range of voltage-, current-, and temperature-based protection features. LED or liquid crystal display (LCD) options are provided for capacity reporting. Data is available over its SMBus 1.1 interface. Battery history and diagnostic data is also kept within the device in nonvolatile memory and is available over the same interface. Features include:

- Flexible configuration for 3- to 15-series Li-Ion and $LiFePO_4$ batteries
- Supports SMBus host communication
- Includes a compensated end-of-discharge voltage gauging algorithm
- Supports battery configurations up to 320 Ahr

- Supports charge and discharge current reporting up to 320 A
- On-chip temperature sensor option, NTC thermistor support from the AFE
- Full array of programmable protection features: voltage, current, and temperature
- Lifetime data logging
- Supports CC-CV charging including precharge, charge inhibit, and charge suspend
- Drives up to a 5-segment LED or LCD display for state-of-charge indication
- Provides SHA-1 authentication

Additional details are available in the bq78350-R1 datasheet[6] and technical reference manual[2].

2.3.3 bq76200 High-Side N-Channel FET Driver

The bq76200 high-side N-channel FET driver provides high-side protection switching using N-channel MOSFETs. The N-channel FETs offer a wider selection and typically lower $R_{DS(ON)}$ and cost than similar P-channel FETs. High-side protection switching allows continuous communication with simple ground-referenced communication during protection faults without the requirement for a communication isolator and its associated supply current. The device has an additional P-Channel FET control to allow low-current precharge to a deeply depleted battery and a PACK+ voltage monitor control for the host to sense the PACK+ voltage. The part is high-voltage tolerant (100-V absolute maximum) and operates at 40 µA typical with a 10-µA maximum shutdown current.

3 Hardware, Software, Testing Requirements and Test Results

3.1 Required Hardware and Software

The board requires power for each cell input for operation and a high current path connection. Communication is required with the board for setup and operation of the board.

3.1.1 Hardware

The board is configured during assembly with a selection of components to be installed and there are no configuration jumpers or options prior to connection.

図 6 shows the top side of the board and 図 7 shows the bottom side.

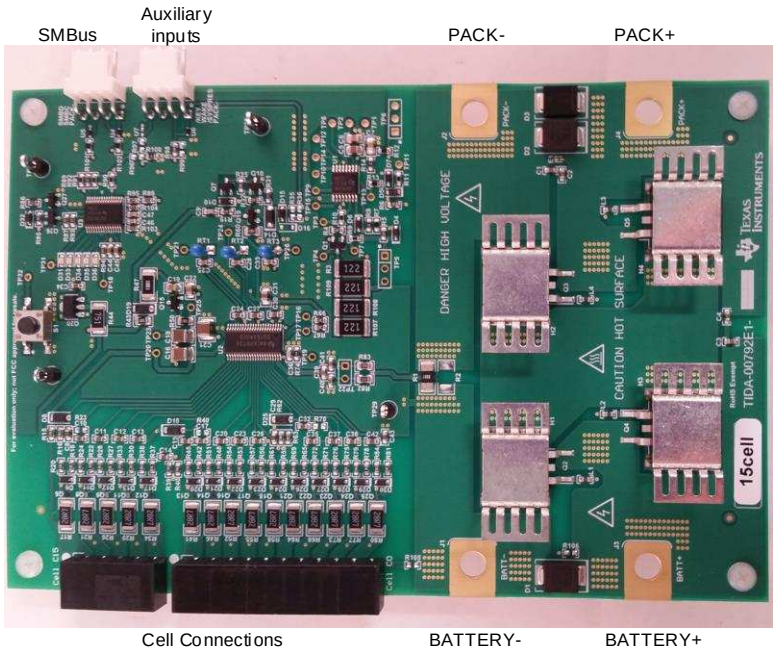

図 6. Board Top Side With Connections

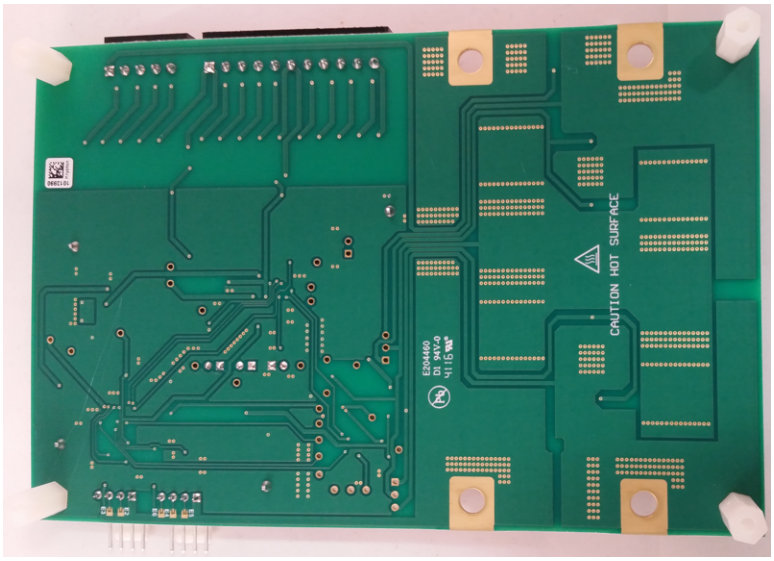

図 7. Board Bottom Side

表 2 describes the connections for the board. With this design, the cell-balancing current path for reduced cell counts must be connected at the terminal block. 表 3 shows the connections required for 15 cells or 12 cells.

表 2. Board Connections

CONNECTOR AND PIN ASSIGNMENTS	FUNCTION OR SCHEMATIC NET	NOTES
J1	BATT–	Cell stack negative; this provides a reference for the electronics and the high current path from the cells
J2	PACK-	Battery pack negative
J3	BATT+	Cell stack positive; this provides power for the high-side driver and the high current path from the cells
J4	PACK+	Battery pack positive
J5, J6	Cn	(n = 0 to 15) Cell monitor, balance, and electronics power connections; see 表 3 for pin definitions
J7	Auxiliary inputs	—
J7-1	PACK–	Reference level
J7-2	/SYSPRES	System present signal to the gauge
J7-3	WAKE	Alternate wake signal for the AFE; not used on test version
J7-4	/KEY	Key signal to the gauge; not used on test version
J8	SMBus connector	—
J8-1	PACK–	Reference level
J8-2	SMBC	SMBus clock
J8-3	SMBD	SMBus data
J8-4	Not connected	—

表 3. TIDA-00792 Cell Connections

CONNECTOR AND PIN ASSIGNMENTS	SCHEMATIC NET	15 CELL CONNECTION (–001 ASSEMBLY)	12 CELL CONNECTION (–002 ASSEMBLY)
J5-1	C15	Cell 15 (most positive)	Cell 12
J5-2	C14	Cell 14	Cell 11
J5-3	C13	Cell 13	Cell 11
J5-4	C12	Cell 12	Cell 10
J5-5	C11	Cell 11	Cell 9
J6-1	C10	Cell 10	Cell 8
J6-2	C9	Cell 9	Cell 7
J6-3	C8	Cell 8	Cell 7
J6-4	C7	Cell 7	Cell 6
J6-5	C6	Cell 6	Cell 5
J6-6	C5	Cell 5	Cell 4
J6-7	C4	Cell 4	Cell 3
J6-8	C3	Cell 3	Cell 3
J6-9	C2	Cell 2	Cell 2
J6-10	C1	Cell 1	Cell 1
J6-11	C0	Cell 1 negative (most negative)	Cell 1 negative

The board must be set up for basic operation as shown in 図 17 and described in section 3.2.1. The /SYSPRES input must be controlled or connected to PACK– at the connector. An optional resistor is provided to short the signal on the board for designs which do not use /SYSPRES.

3.1.2 Software

The bq78350-R1 is preprogrammed with firmware and the configuration is done by setting parameters in its data memory. Battery Management Studio (bqStudio) software is a graphical user interface (GUI) available for Windows computers that can be used with a compatible interface to configure the parameters. The bqStudio software is available from the bqStudio tool folder on the TI website. Compatible interfaces are the EV2300 or EV2400 available from TI.

3.1.2.1 Using bqStudio

The bqStudio software can be started from the desktop icon or the Start → Texas Instruments → Battery Management Studio menu or equivalent for supported operating systems.

When bqStudio is started while connected to a working gauge, the software detects the gauge and open its display similar to 図 8. The dashboard section on the left side of the display shows the connected interface and part and the voltage and current of the part. The dashboard refreshes periodically but can be turned off if desired. The registers tab is displayed in the middle pane, which shows a snapshot of when the tool started or from the last refresh. The tab can be refreshed by clicking the *Refresh* button in the upper-right corner of the tab or by selecting the scan button for periodic update. The *Start Log* button starts a log of the data, which is useful for recording the gauge data over time. Across the top of the bqStudio window and below the *File* menu are other tools which typically open in the center tab area of the display. On the right side of the display is a *Command* window which the user can scrolled through to display various commands that can be selected as a button. Below the *Commands* window is the *Log Panel*, which shows the command and its result. Status messages display in the bottom border of the bqStudio window.

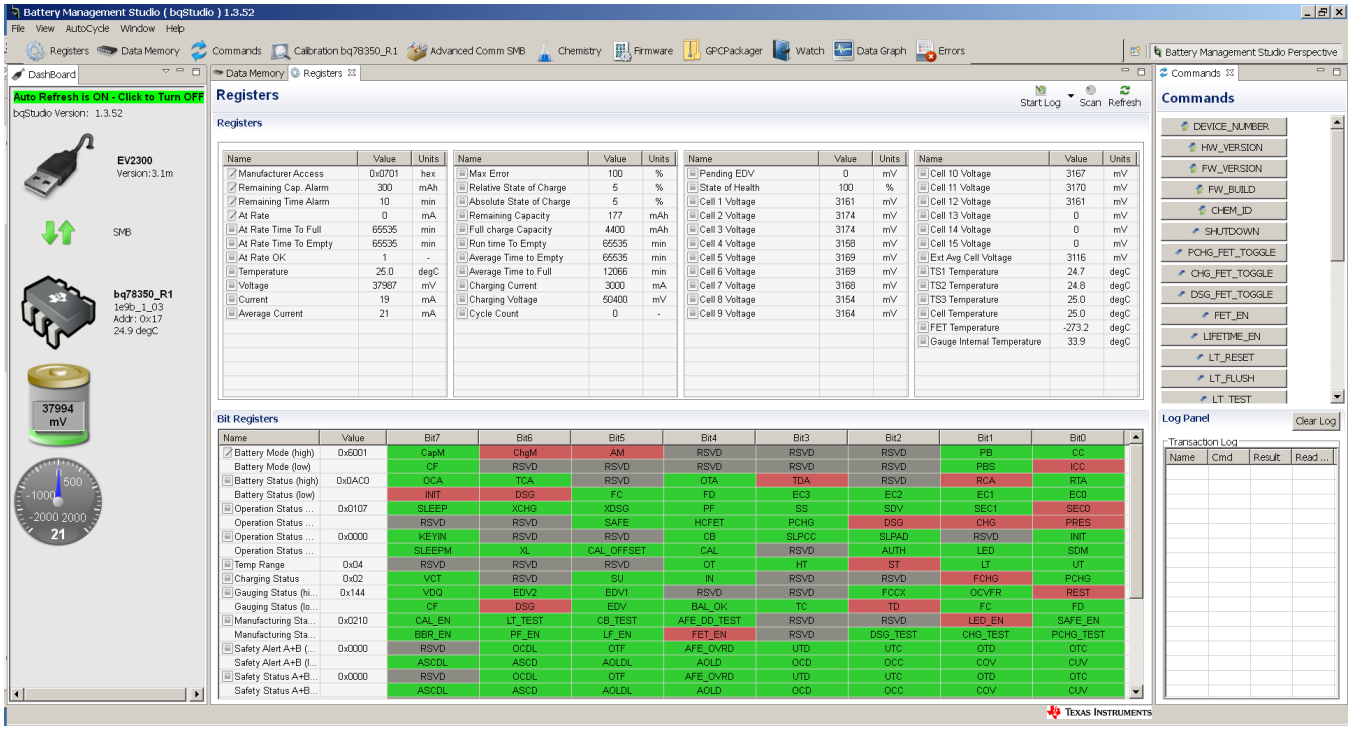

図 8. bqStudio Register Display

If bqStudio does not find an operating gauge upon starting the software, it displays a *Target Selection Wizard* window as shown in 図 9. If the user wants to set up the tool without the gauge operating, select the *Gauge* option and click the *Next* > button. A list of selected targets then display as shown in 図 10. Scroll down and select the *1E9B_1_03-bq78350-R1.bqz* entry, then click the *Finish* button and *OK* in the popup box. The register section updates when the gauge is detected.

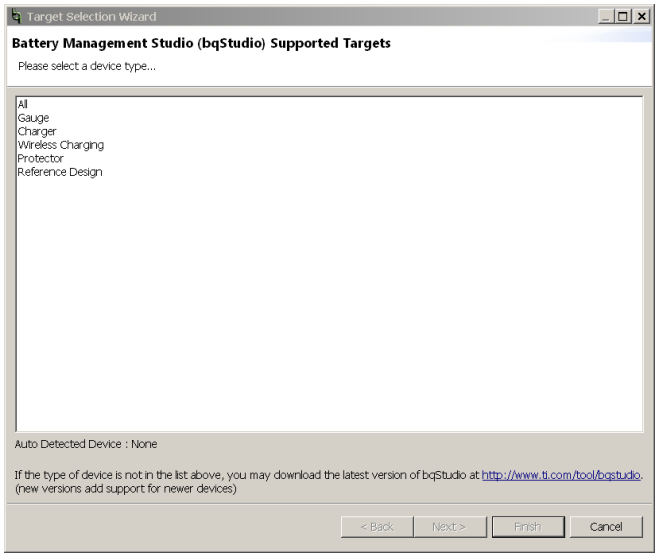

図 **9. bqStudio Target Selection**

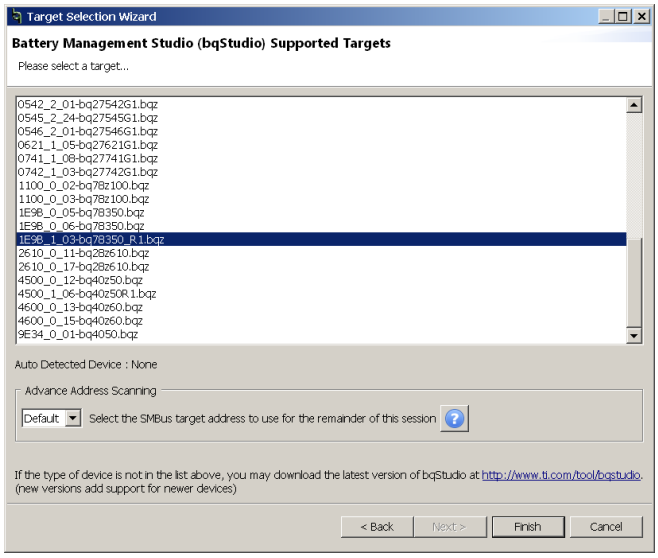

図 **10. bqStudio Supported Targets**

The bq78350-R1 gauge is configured primarily using the *Data Memory* tab shown in 図 11. The *Calibration* section is the default display. Different sections are displayed by selecting the button for the section on the left side of the pane. Many parameters are entered as a value, some are bit fields and open a bit field pop-up window to easily select bit values. 図 12 shows an example. The selection is written by clicking the *Write To Data Memory* button at the bottom of the popup. The popup must be closed with the *X* button in the top-left corner. A value can be written in the box for bit field parameters, but the popup remains in display and must be closed. Parameters can be exported to a file which can be edited and re-loaded to the part. Viewing the file as a spreadsheet is convenient but it should not be edited as a spreadsheet if it is to be loaded back to the part.

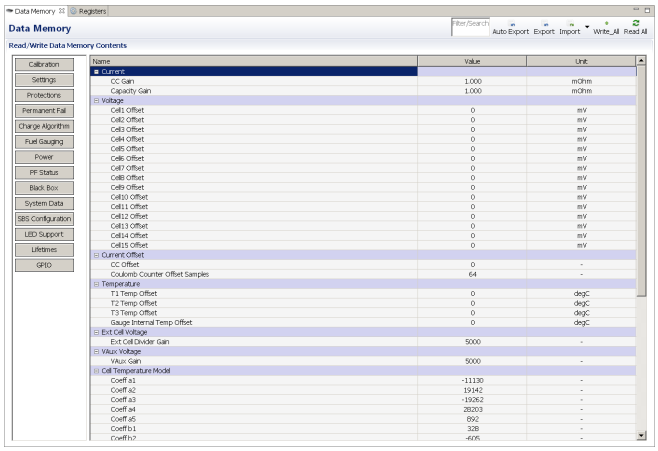

図 **11. bqStudio Data Memory Tab**

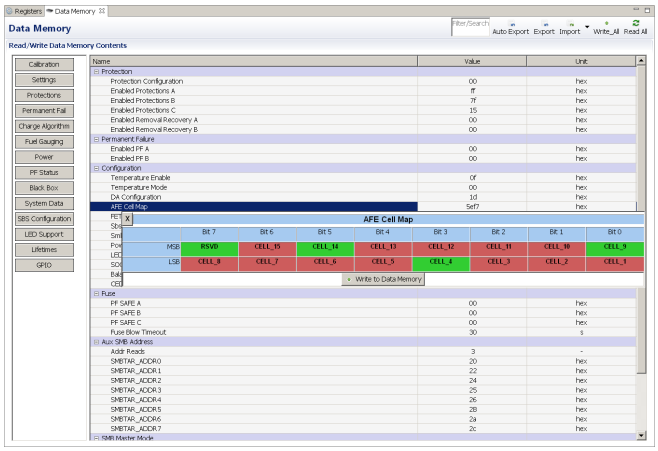

図 **12. bqStudio Bit Field Entry**

The part shows calibration data in the calibration section of the data window and the calibration tab shows a simplified calibration of the board. Selecting the *Calibration* tool opens the calibration tab. The designer can enter the measured data into the appropriate section and use the associated button to perform calibration. 図 13 shows an example of the window with a confirmation of a successful coulomb counter (CC) offset calibration, which is indicated by the green check mark. Each section of the tab operates separately and any fields left blank in the section are skipped in the calibration.

Chemistry data is used by the bq78350-R1 to estimate the state of charge on start-up. For systems which are always on, chemistry selection may not be important. If desired, chemistry data can be loaded to the device using the *Chemistry* tab shown in 図 14. The chemistry ID loaded to the device can be read from the CHEM_ID command in the *Commands* pane, for which the result is shown in the *Log Panel*.

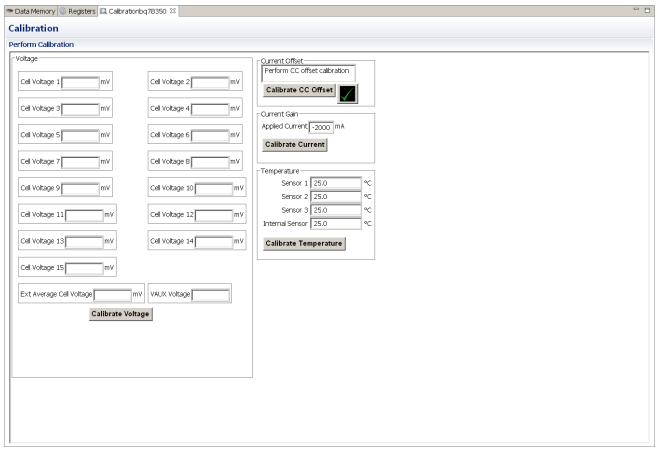

図 13. bqStudio Calibration Tab

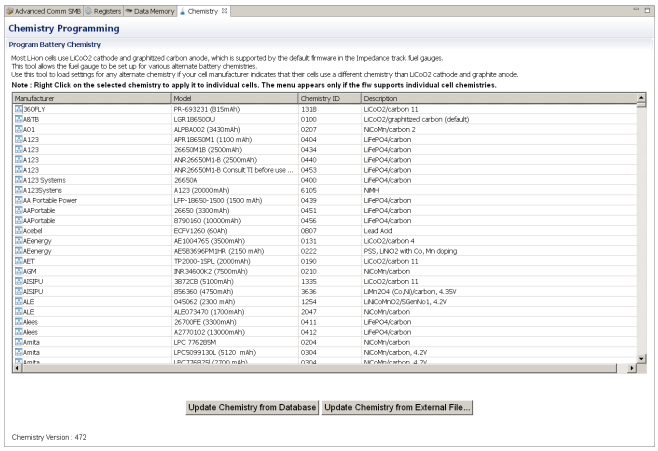

図 14. bqStudio Chemistry Tab

If the designer wishes to return to a starting location in the configuration of the gauge, the gauge firmware can be reloaded using the *Firmware* tab. Device firmware is available in the bq78350-R1 product folder tools and software tab. Install the firmware to the computer then enter the file path and select *Program*. Programming takes about 40 seconds and returns all configuration, calibration, and chemistry settings to the default values.

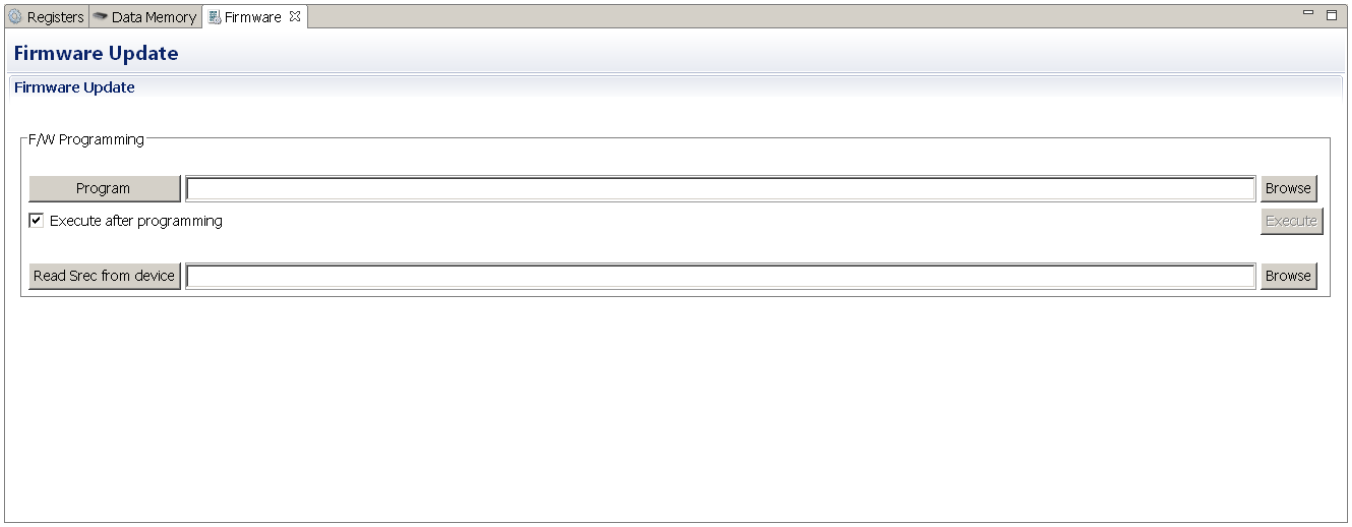

図 15. bqStudio Firmware Tab

Additional tools may be helpful when working with the bq78350-R1. The Gauging Parameter Calculator GAUGEPARCAL is used to prepare CEDV coefficients for the gauge when desired. Register logs can be collected with bqStudio and packaged with the bqStudio *GPCPackager* tab. The *Advanced Comm SMB* tab in bqStudio also allows entry of commands which are not supported in the *Commands* pane or commands that do not allow direct observation of the data. The *Watch* tab allows selection of limited registers to be observed over time and can save a log. The *Data Graph* tab plots selected registers over time and can save a an image.

3.1.3 Setting Board Specific Parameters

Certain parameters must be set for the board hardware design. Parameters are set in the bq78350-R1 data flash using the *Data Memory* tab in bqStudio. By default, the bq78350-R1 is configured for the minimum cell count of the supported bq769x0 monitor family, or three cells. The bq78350 shuts down when a cell drops below the Power|Shutdown Voltage threshold. The three-cell default configuration allows the gauge to operate to set the proper board configuration. The design uses three thermistors, so Settings|Configuration|Temperature Enable is set to 0x0F. The expectation is that the thermistors are to be used for cells, so the *Temperature Mode* is left as default. The design supports VAUX measurement of the pack voltage through the bq76200 device, so the VAUXEN bit is set and the Settings|Configuration|DA Configuration is changed to 0x19. Cell count is set in the Settings|AFE cell map where the physical cells are mapped and presented in the gauge as logical cells. For 15 cells, all cells are used and the value is 0x7FFF. For 12 cells the value is 0x5EF7. The board uses high side switching, so the polarity of the precharge output must be set to active high and PCHG_POL must be set to 1. For this design it is ideal to have the FETs turn off during overtemperature, so OTFET is set and the Settings|Configuration|FET Options parameter is set to 0x0125. 表 4 shows a summary of the parameter changes to support the board design.

表 4. Board Design Parameter Summary

PARAMETER	DEFAULT	SETTING	COMMENTS
Settings|Configuration|Temperature Enable	09	0F	Three thermistors
Settings|Configuration|DA Configuration	11	19	VAUX enable
Settings|Configuration|AFE Cell Map	13	5EF7	12 cells shown
Settings|Configuration|FET Options	21	125	Precharge polarity and temperature protection FET switching

3.1.4 Setting Chemistry

The chemistry data is loaded using the *Chemistry* tab of bqStudio rather than as a simple parameter in the data memory (refer to 3.1.2.1). For the TIDA-00792 TI Design, the test chemistry was left at the default setting. Other uses of this design may select an appropriate chemistry.

3.1.5 Setting System Design Parameters

A saved data memory file shows 469 parameters, which can be intimidating to a designer. However, a number of these parameters are output parameters and many parameters operate in their default settings, so the designer should not expect to change all parameters. Protection limits are generally set for the cells used and recovery behaviors are selected which are appropriate for the end system. Description of the parameters are provided in the *bq78350-R1 Technical Reference Manual*[2] and are not duplicated here.

The testing in this document confirms operation of the design. Various cells can be used with the design and requirements vary with the final application, so details of parameter settings are not provided here. However, a few details are worthy of note. This design uses high-side protection switching and VAUX supports PACK measurement. One use may be to measure the pack output by command. Another use of VAUX is to use pack voltage recovery for certain faults; for this function, set the VAUXR bit in the Settings|Protection|Protection Configuration parameter. The LPEN bit should not be set because this board uses high-side protection switching. As a 12- to 15-cell design, the battery voltage exceeds 32768 mV and the SBS Configuration|Data|Specification Information VSCALE should be set to 1 and battery and charging voltages should be scaled by 1/10th. The VAUX voltage and the 30-A current are within the range of the gauge and do not require to be scaling.

The parameter setting can be iterative in the development of a battery; for example, the setting may require a selection to characterize the cells for CEDV parameter generation. When all parameters are available, those parameters are entered for final development testing.

Rather than setting bits to enable certain features in the *Manufacturing Status* data memory, certain features can be set with commands. Enable the LEDs using the LED_EN command in the command window. FETs can be enabled for testing using the test commands or the FET_EN. FETs must be enabled to flow current for calibration.

3.1.6 Calibration

Calibration can be performed using the *Calibration* tab in bqStudio. The CC Offset should be calibrated before current gain. Voltages should be calibrated for each cell. Use the cells in logical order—do not skip cells. For this design, the *Ext. Average Cell Voltage*, *VAUX Voltage*, and all three temperature sensors must also be calibrated.

3.1.7 Next Steps

The board is ready for testing after calibration. Demonstration testing is included in 3.2. If development testing enables and collects the permanent fail, black box, and lifetime data, the user should clear that data before saving the settings. Details on test commands as well as reading and writing data to the gauge are described in the *bq78350-R1 Technical Reference Manual*[2]. For additional tools see the bq78350-R1 product folder or check with a TI representative.

3.2 Testing and Results

3.2.1 Test Setup

The design was constructed with 15-cell (–001) and 12-cell (–002) configurations and tested using both equipment and cells. Continuous operation was performed using simulated cells powered by a DC power supply. Gauge testing was performed using a 12S4P cell assembly. 表 5 summarizes the equipment used for testing. 図 16 shows an example test setup.

表 5. Test Equipment Summary

ITEM	MODEL OR DESCRIPTION
Oscilloscope	Tektronix TDS3054B
Current probe	TCP312 with TCPA300
Differential probe	P6246 low voltage
Power supply	Sorensen DCS150-20E
Power supply	Agilent 6654A
Power supply	HP 6031A
Electronic load	Dynaload RBL488 100-120-800
Electronic load	PLW6K800-100E
Infrared camera	FLIR i50
Multimeter	Keithley 2000
Cell simulation resistors	200 Ω
Communication adapter	Texas Instruments EV2300 or EV2400

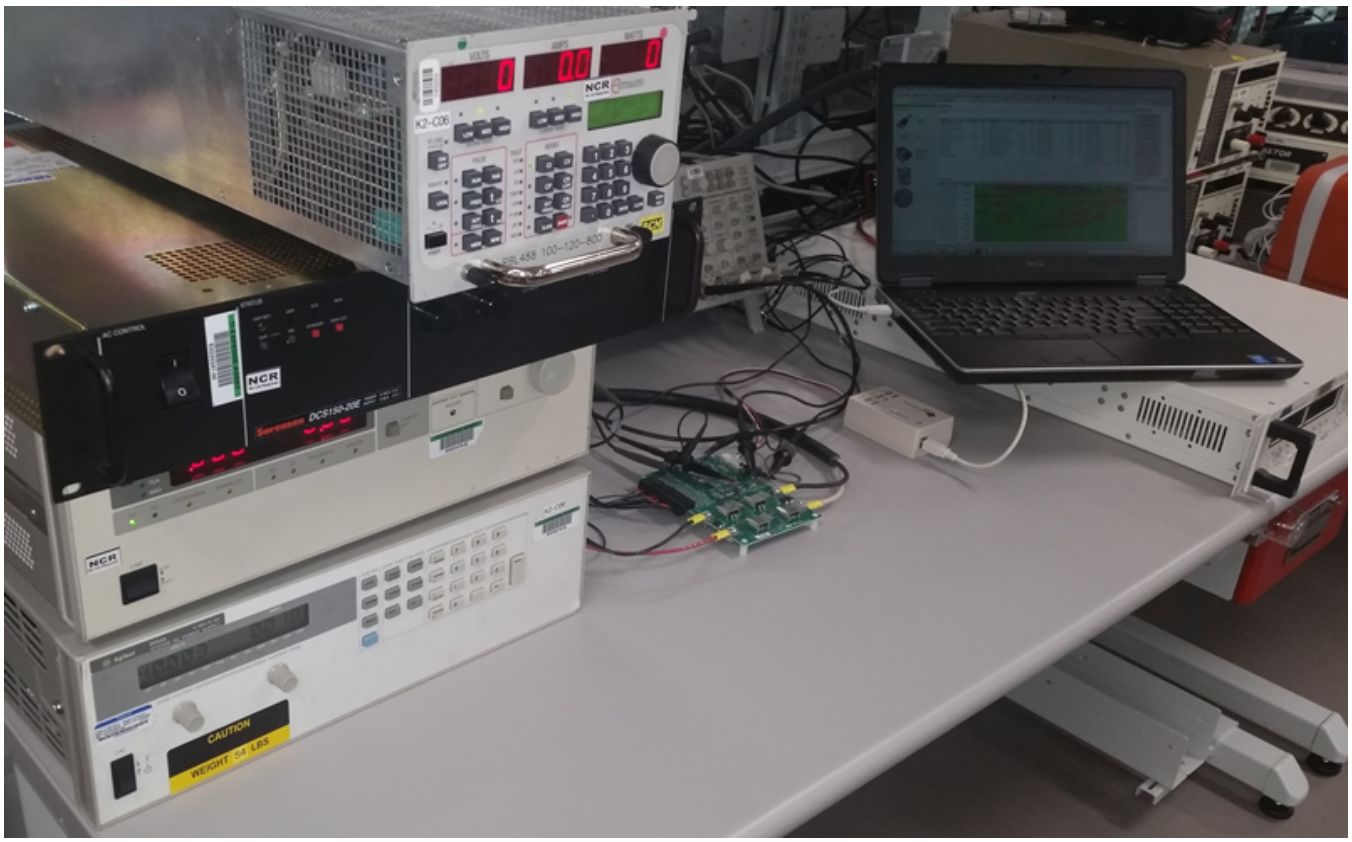

図 16. Typical Test Setup

Equipment was configured appropriately for the test to be performed. 図 17 and 図 18 show example setups. The /SYSPRES net was connected to PACK– on J8 using a shunt for most tests. Parameter thresholds were adjusted as required for the desired trips during protection testing. Due to limitations of the power supplies, continuous high-current tests were run using one supply for the cell voltages and another supply for the high current path as shown in 図 19.

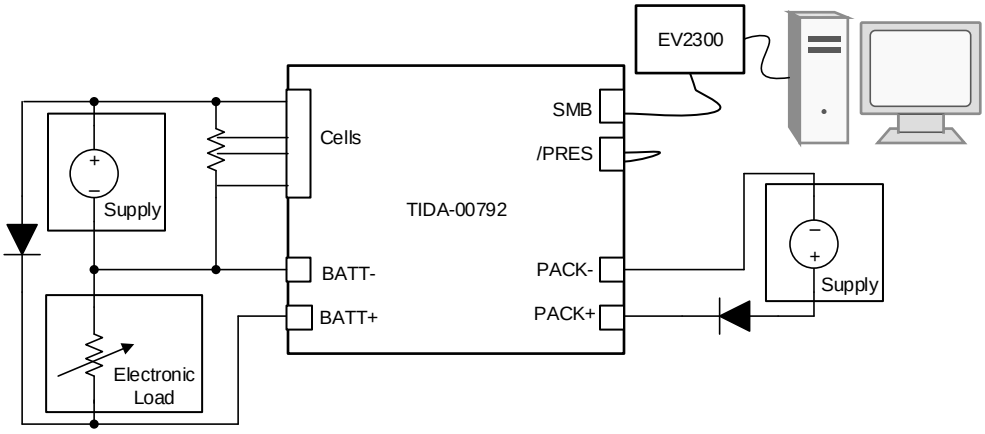

図 17. Simulated Charge Test Diagram

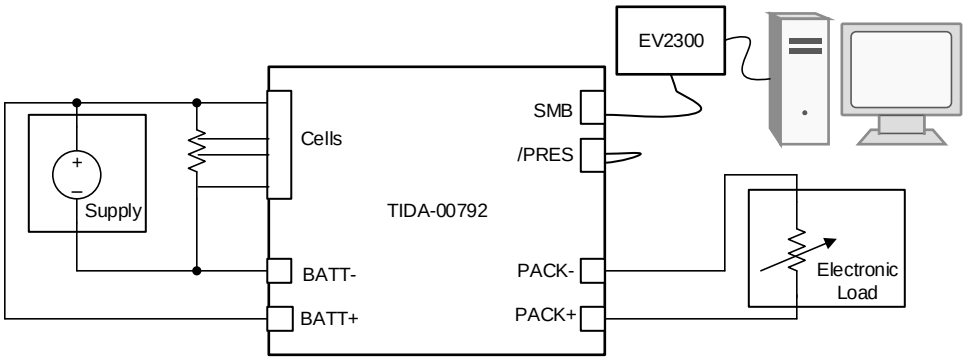

図 18. Simulated Discharge Test Diagram

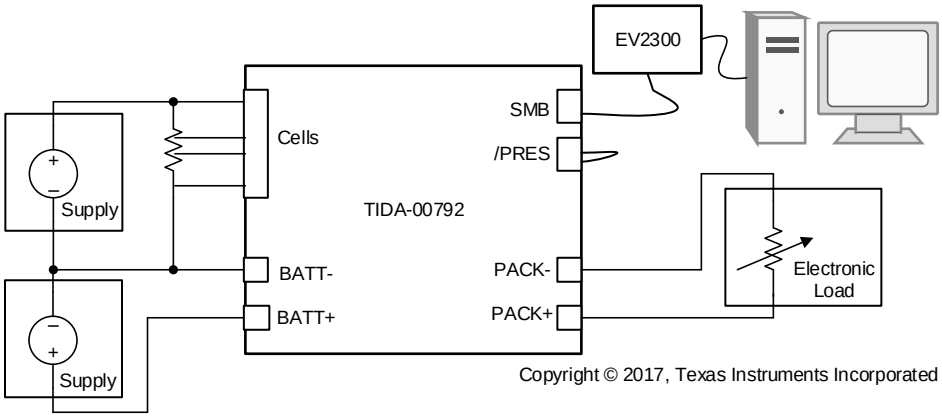

図 19. High Current Simulated Discharge Test Diagram

Cells can be charged with a supply or discharged with a load. A diode is used with a supply to simulate a charger and prevent the cells from forcing current into the supply and causing potential damage (see 図 20 and 図 21).

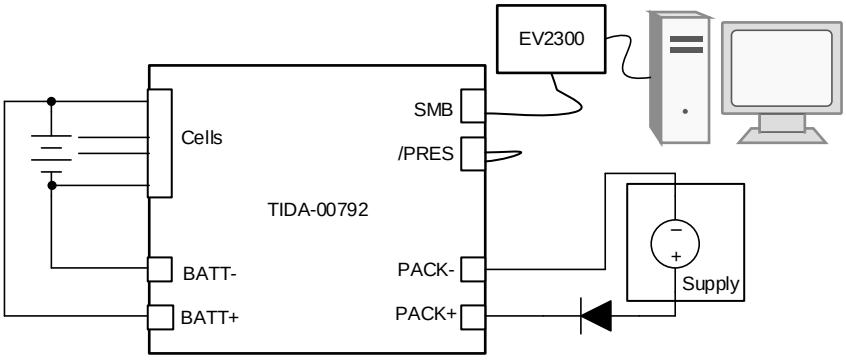

図 20. Battery Charge Test Diagram

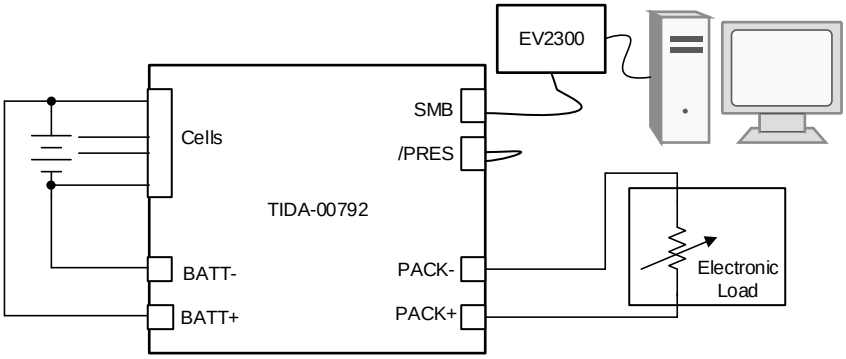

図 21. Battery Discharge Test Diagram

3.2.2 Test Results

3.2.2.1 Boot

After applying power or connecting cells, the board must be awakened. The process is know as booting the bq76940. The test versions of the board provide booting from the PACK terminals. Applying a rising voltage on PACK+ turns on the boot circuit, which applies a voltage to TS1 of the bq76940 device and starts its REGOUT regulator. When REGOUT has risen sufficiently, TS1 is pulled low by the boot circuit to prevent interference with the temperature measurement initiated by the gauge. 図 22 shows a boot example. The boot pulse is applied to TS1 by the circuit only long enough to boot the device.

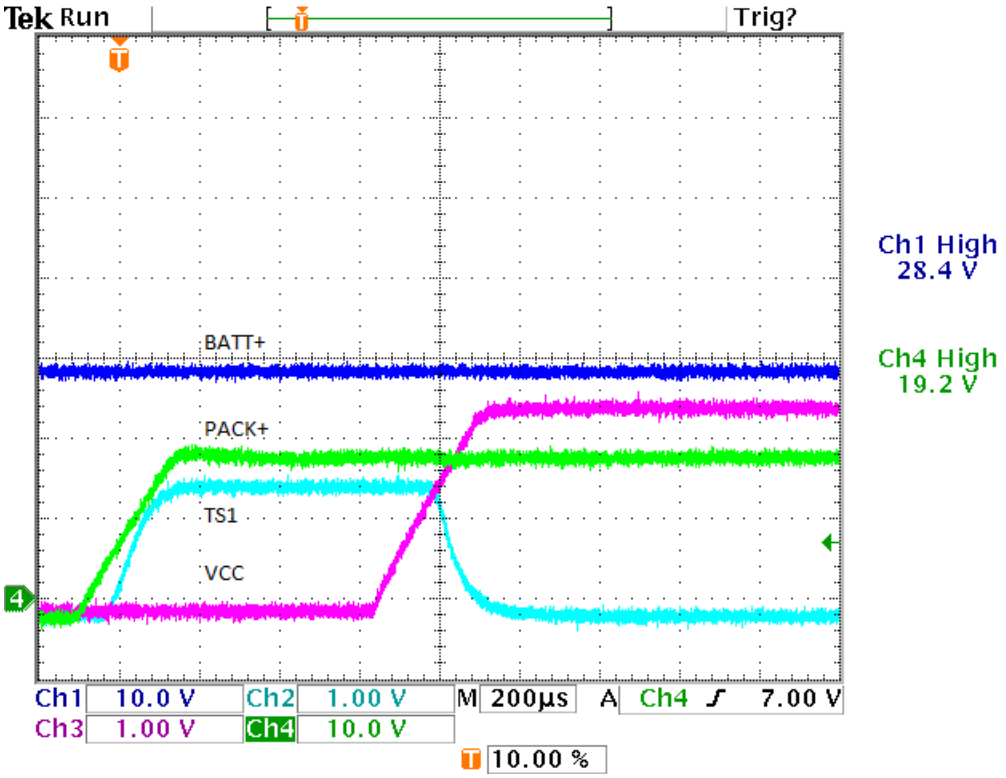

図 22. Boot

The REGOUT regulator supplies VCC to the gauge. When the gauge starts it begins taking a temperature measurement; if the checks are okay, the gauge turns on the protection FETs. 図 23 shows an example of start-up where the charger applies a test voltage or the PACK+ voltage has not risen fully before the gauge turns on the FETs. When the discharge FET closes, the battery pulls the PACK+ terminal up to the battery voltage.

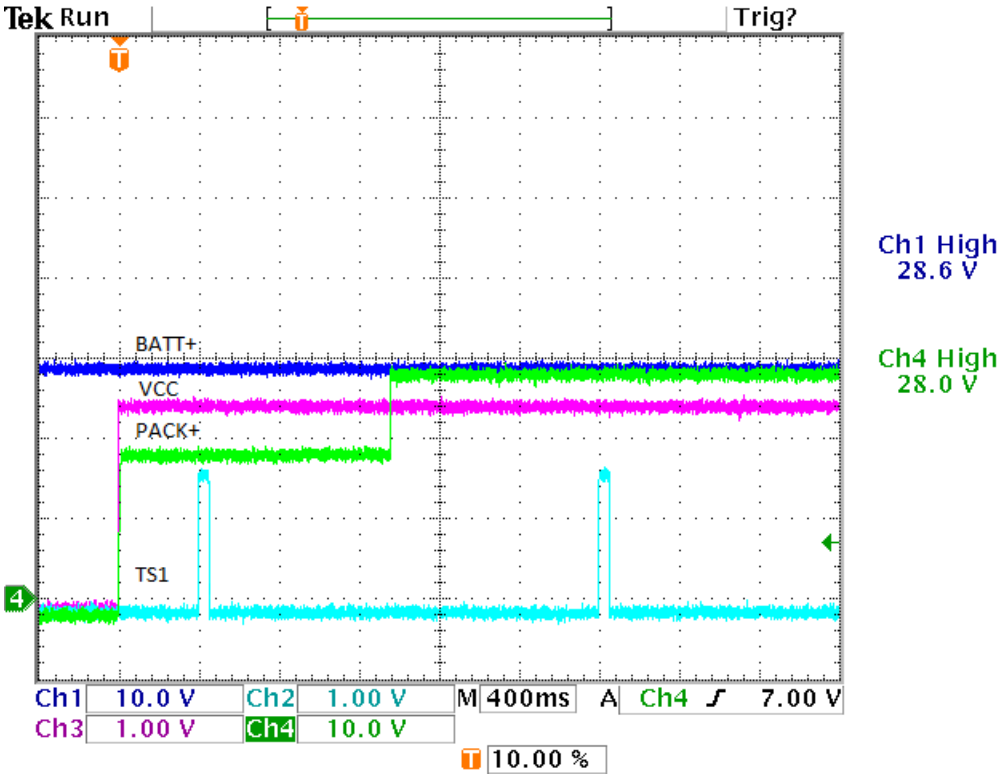

図 23. Boot With Low Charger Voltage

図 24 shows an example of start-up where the charger has reached full voltage before the FETs are turned ON. When the charge FET closes, the charger voltage on PACK+ is pulled down to the battery voltage as the charger goes into constant current mode.

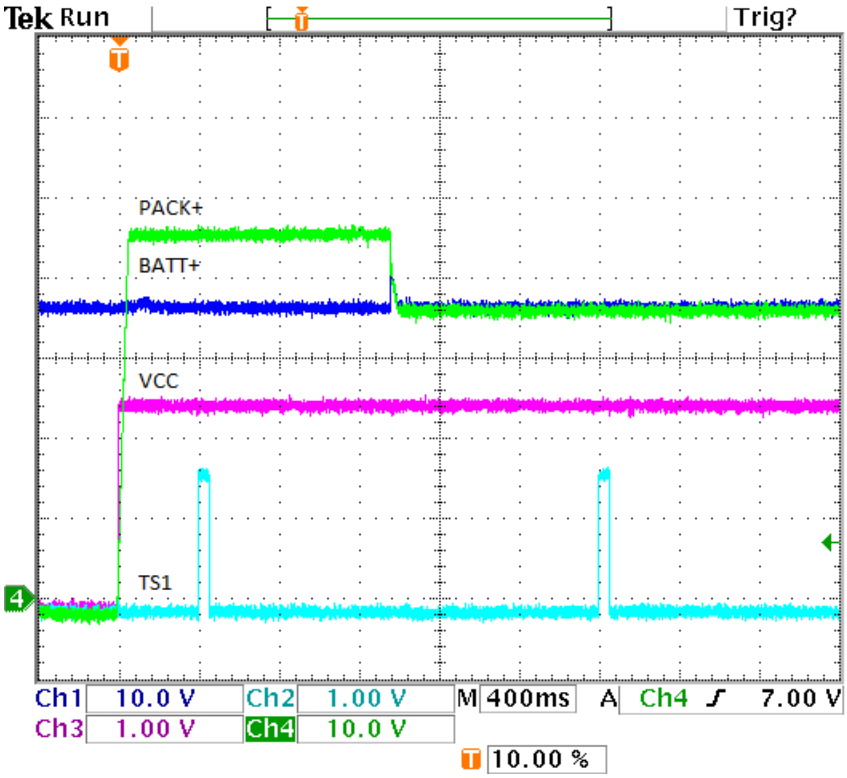

図 24. Boot With Full Charger Voltage

3.2.2.2 Thermal

With continuous current through the board, a power dissipation occurs in the sense resistor, power FETs, and board traces. 図 25 shows a thermal picture of the board after an hour of horizontal operation at 30 A in a room temperature environment. The FETs have reached a temperature of approximately 65°C. The sense resistor mounting area has reached 70°C with the resistor temperature at 92°C. The resistor is operating at 0.9 W or 60% of its rated power. From the resistor derating curve, the ambient operating temperature can rise approximately 40°C; however, for high continuous currents, using the parallel resistor pattern may be desired depending on the operating environment provided by the system.

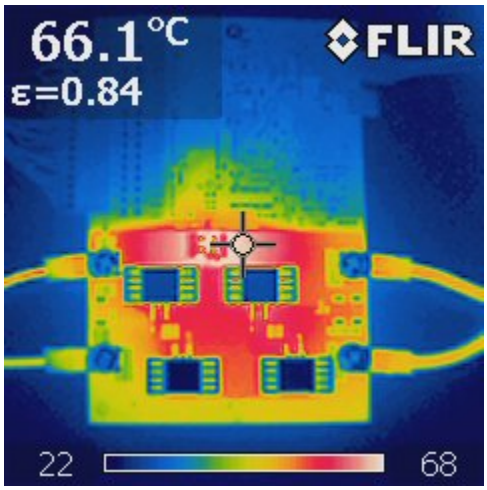

図 25. 30-A Discharge Thermal Image

At low cell voltages, the gauge transitions from a fast charge mode to precharge mode with charging current limited by the precharge path resistance. 図 26 shows the board operating for 30 minutes with a 25-V difference between the charger and battery voltages. The resistors have reached 115°C with the board mounting area at 68°C. At 25 V, the power is 0.52 W or 52% of the rated power for the resistors. From the derating curves, the ambient temperature should be able to rise an additional 40°C; however, the designer should consider the minimum cell voltage at which precharge is allowed by the gauge. A lower cell voltage results in a higher maximum differential voltage during precharge. A lower precharge current or better thermal management of the precharge resistors should be implemented in some cases.

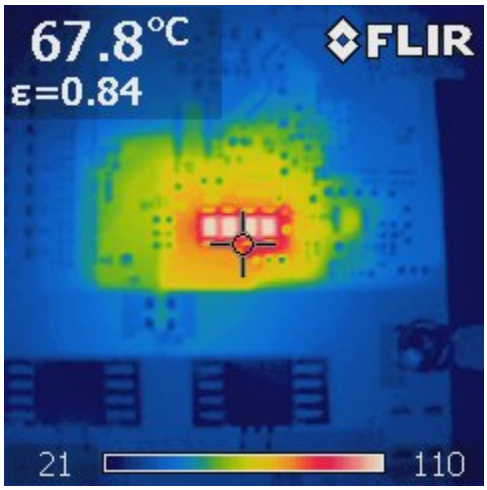

図 26. Precharge at 25-V Voltage Difference

The bq78350-R1 device balances every other cell when multiple cells require a balance to avoid exceeding the limits of the bq76940 monitor. An example of extended balancing at 4.1 V/cell is shown in 図 27. The every-other-cell balancing limits the power into the board area, but the resistors heat each other. With an extended balancing time in 図 27, the mounting area is 70°C while the resistors are at 90°C. The resistors can tolerate an additional 60°C ambient temperature rise at this power. The extra margin may be due to the duty cycling of the balancing current by the bq76940 device during balancing to allow measurement; however, balancing can occur at a higher voltage with more power, so keeping a good margin on the resistor rating is desired. 図 27 also shows that heating of the LED power supply transistor occurs due to blinking the LEDs during a charge with the LED Configuration[LEDCHG] set.

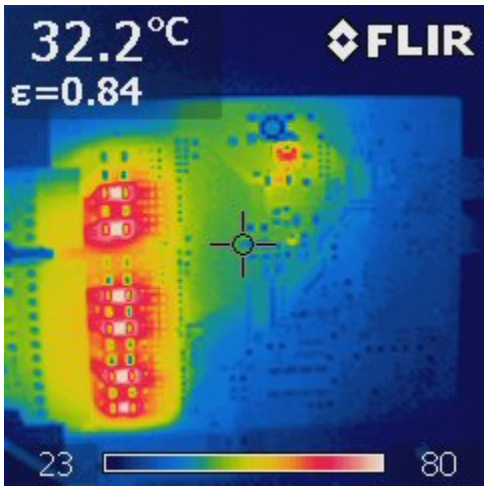

図 27. Cell Balancing: 4.1 V/Cell

3.2.2.3 Protection

During normal operation of a battery pack, the charger and load should operate within the acceptable performance range of the battery and the battery protection FETs should never switch. However if conditions exceed the established parameters, the FETs must be able to switch off to stop current flow. Different events will trigger the charge, discharge, or both FETs to turn off. When recovery conditions are met the gauge will switch on the FET.

図 28 shows the device switching off charge current from an overcurrent charge (OCC) event but typical of any charge protection event. The CHG pin is driven low but drops initially limited by the internal and external resistances. As the FET gate discharges the CHG pin continues to fall. When the gate voltage reaches the switching point of the FETs, current drops and PACK+ rises above the battery voltage. OCC protection requires a discharge to recover, but other charge protections may allow recovery with resumed current flow. 図 29 shows a recovery from overtemperature in charge fault. This capture shows the gate voltage which rises from 0 V rather than having a step like the resistive CHG pin. When the FET comes on current builds and PACK+ is pulled down to the battery voltage. Current overshoot is dependent on the equipment used.

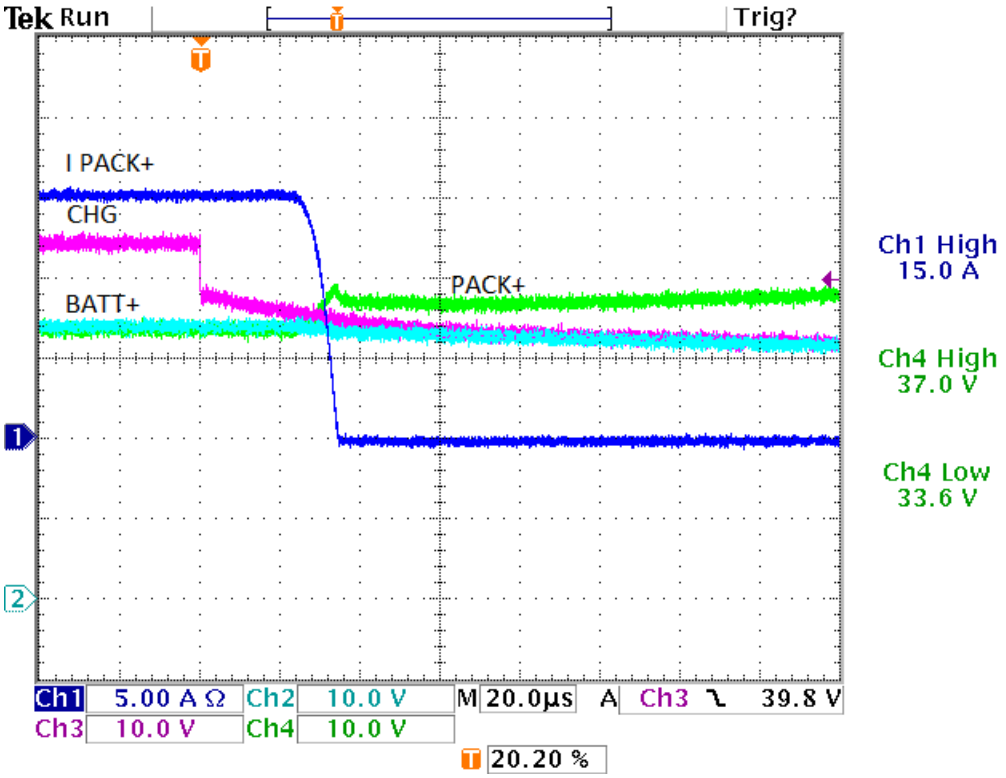

図 28. Overcurrent Charge Protection

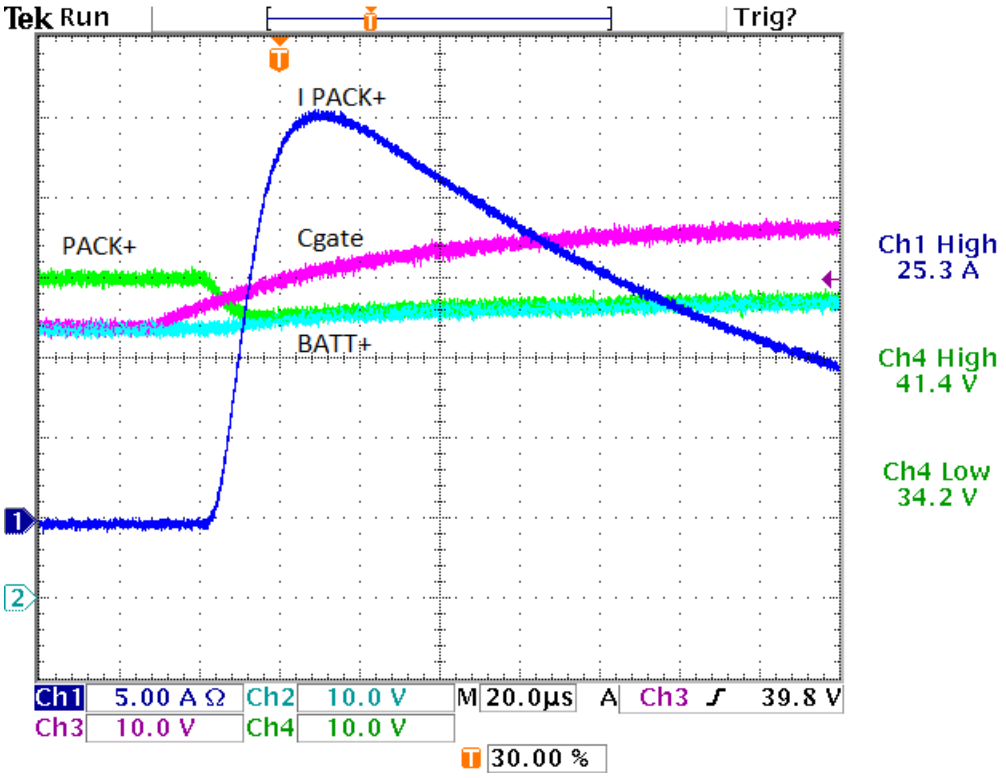

図 29. Overtemperature Charge Recovery

Discharge faults cause a turnoff of the discharge FETs using the DSG output. 図 30 shows an example of an undervoltage protection at 5 A. Similar to the charge FET, the DSG pin initially shows a step due to the internal and external resistances whereas the gate voltage transitions more smoothly as the gate capacitance discharges. The current begins to drop when the gate voltage has fallen sufficiently. The current is low as it plateaus while PACK+ drops to 0 V. With the default configuration, recovery from undervoltage occurs when the cell voltages rise sufficiently. 図 31 shows a recovery from undervoltage based on voltage rise and would represent other fault recoveries where current resumes. When the DSG is enabled, it jumps to a level set by the internal and external resistances (11 V in 図 31) and the gate begins to charge. When the gate has risen sufficiently, the FET begins to draw current and PACK+, the gate, and DSG all rise.

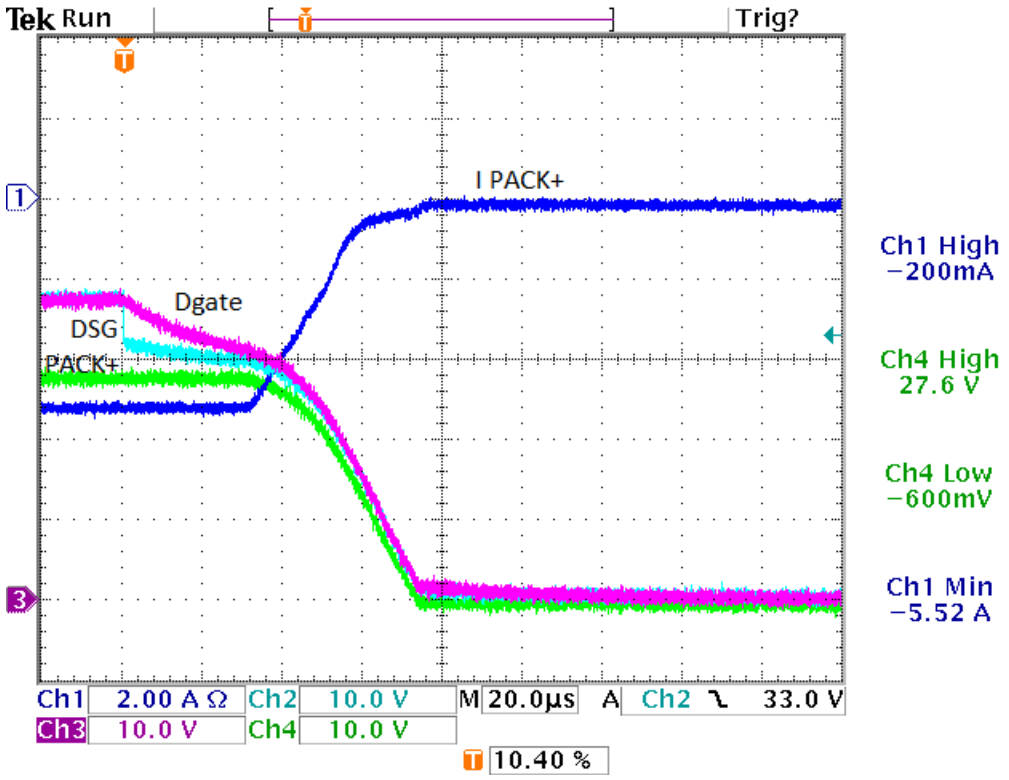

図 30. Undervoltage Protection

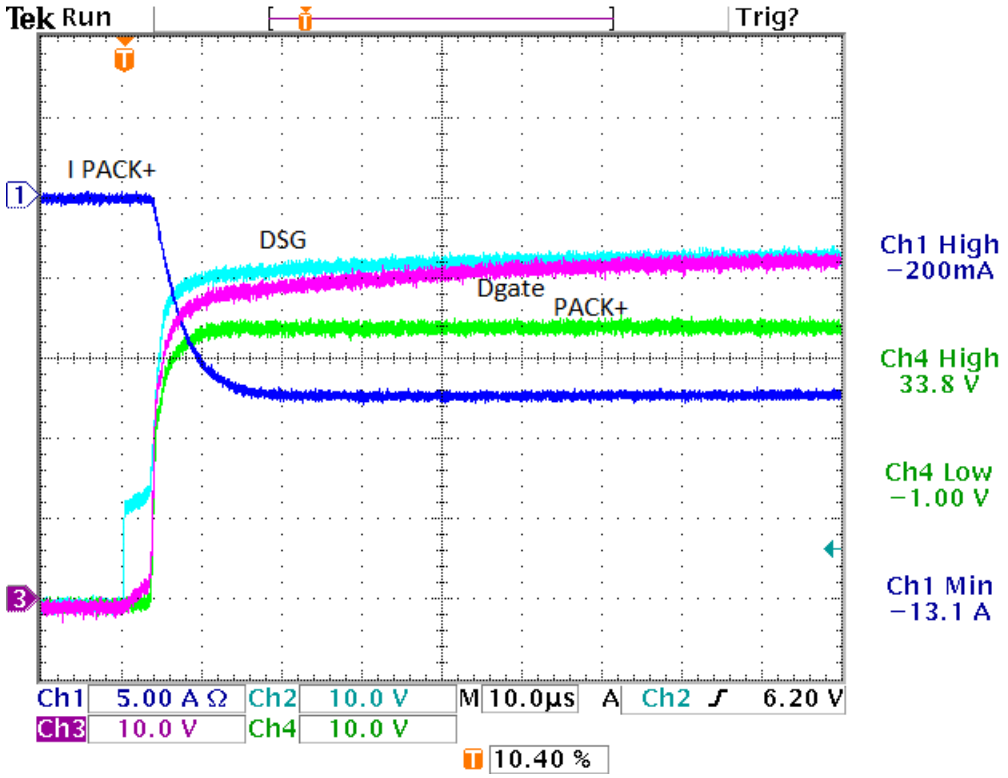

図 31. Undervoltage Recovery

When current is higher at the DSG switching, the plateau in current during the PACK+ transition is at a higher level. After PACK+ reaches 0, it is driven negative by the system inductance and PACK+ current continues to drop as the flyback diode conducts (see 図 32).

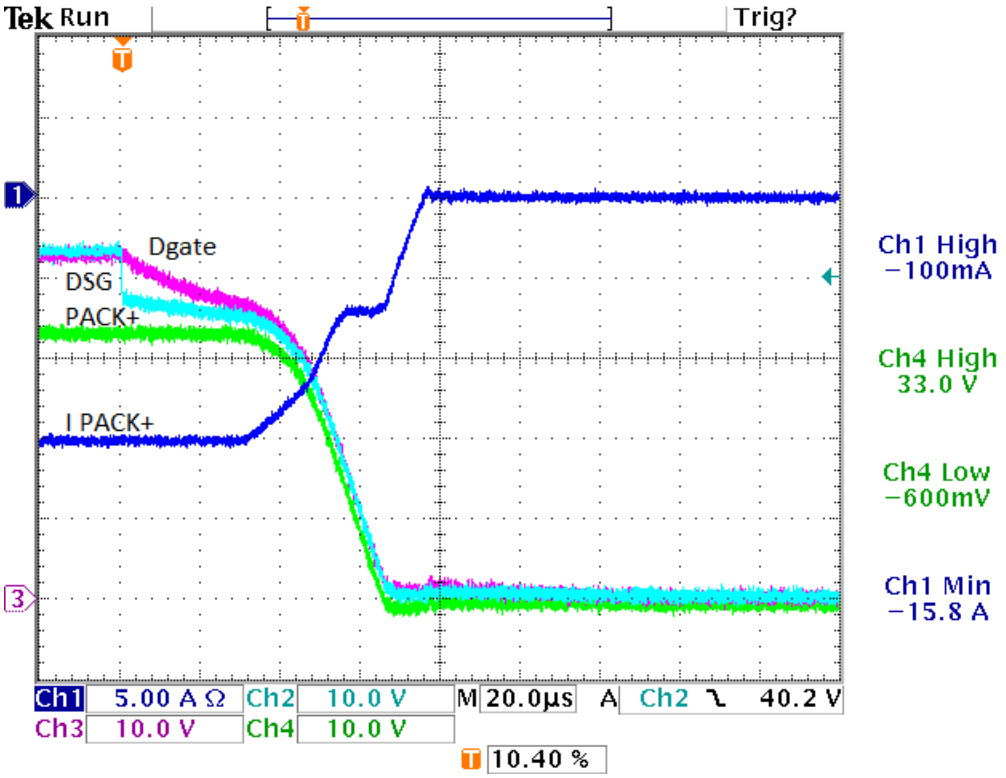

図 32. Overcurrent Protection PACK+ Current

Current from the battery can be observed by the voltage across the sense resistor. 図 33 shows the sharp drop of current at the sense resistor. This example shows a case where the current is switched while the battery is able to provide the current with little voltage drop.

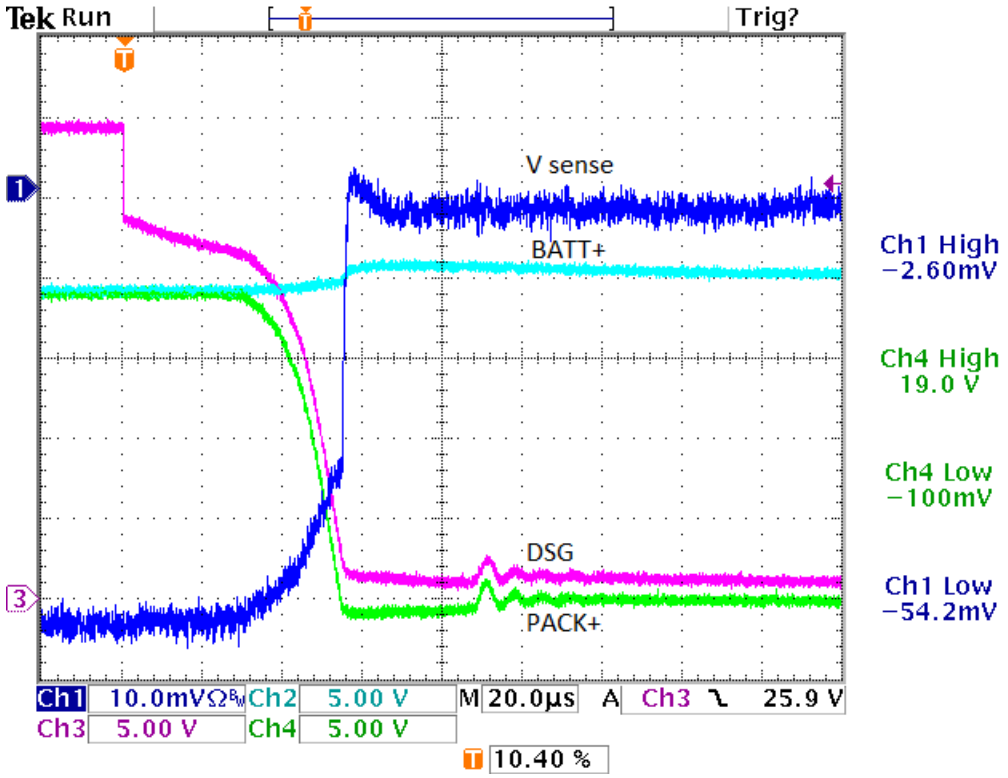

図 33. Overcurrent Protection Battery Current Sense

When the protection is from a short circuit, such as in 図 34, the battery and PACK+ voltages have been pulled near PACK–. Current may be very high: over 100 A in the figure. When DSG switches low, the gate discharges and the current at the switching level drops. As the current drops, the cells have an inductive response and BATT+ overshoots its nominal value as PACK+ drops and is forced negative by the relatively small inductance of the short circuit. Unless configured to recover with the /PRES signal in the Enabled Protections registers, the bq78350-R1 recovers from hardware overcurrent and short-circuit protections based on time. 図 35 shows a recovery into a short. As DSG rises and current flow begins, BATT+ is pulled down to PACK+. Current builds to over 100 A. After the short-circuit delay time, the bq76940 turns off DSG and switching occurs as shown in 図 34.

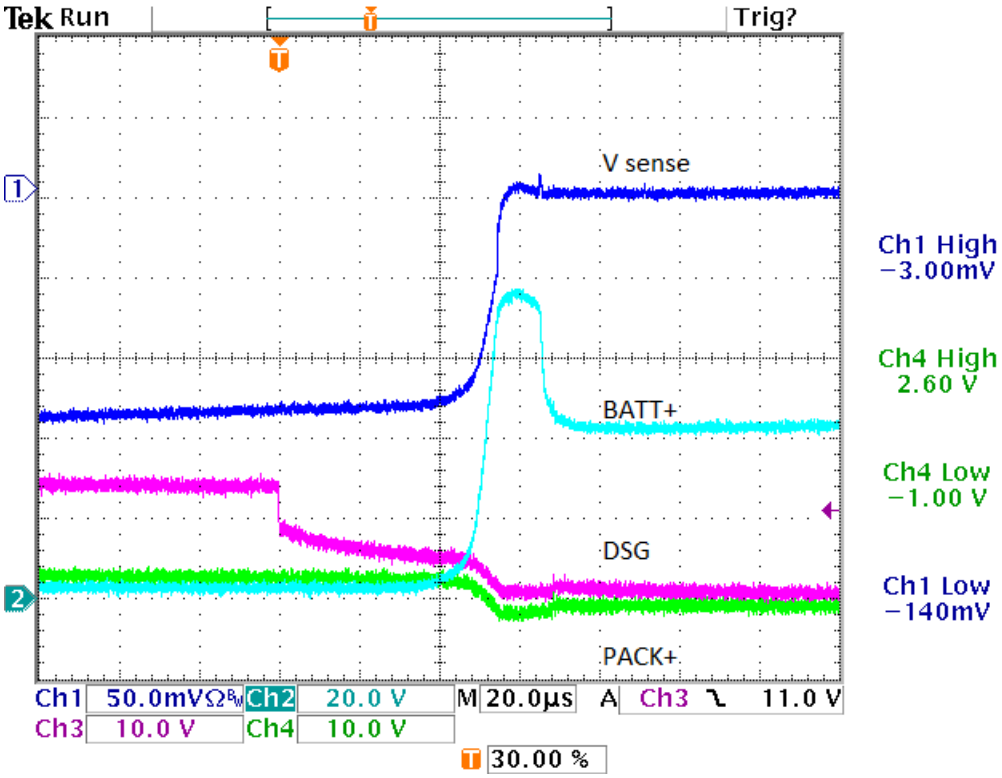

図 34. Short-Circuit Protection

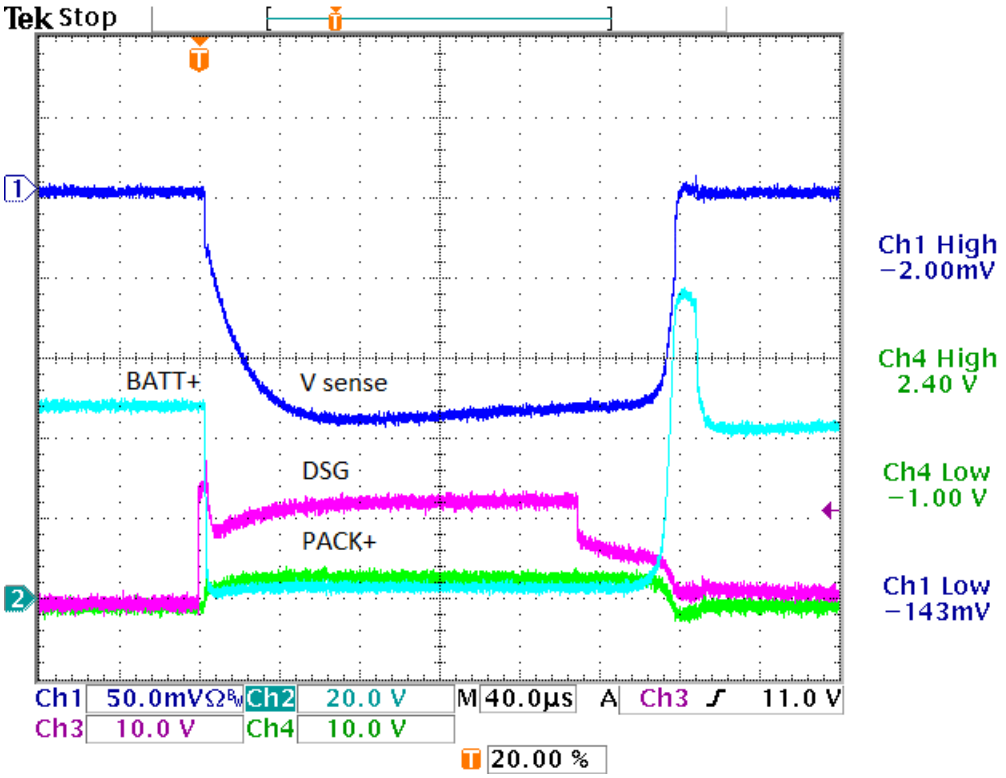

図 35. Recovery Attempt into Short Circuit

3.2.2.4 Gauging

Gauge demonstration testing was performed with a 12S4P battery assembly, which was also used for prior testing. Charge and discharge currents were selected at 10-A nominal, well within the capabilities of the parallel cells and the available equipment. The charging voltage was reduced to 4.15 V, which reduces the available capacity but extends the life of the cells. Fixed EDV was used for this demonstration test. EDV0 was set at 2.8 V, which is above the manufacturer's recommended depth of discharge to allow some voltage variation in the cells for the average voltage gauging. Based on a discharge cycle, EDV1 was set at 97% and EDV2 at 93% of the charge passed to EDV0. With the reduced voltage range, a design capacity of 20000 mAh was assigned, which is lower than the datasheet capacity.

The battery was charged to obtain a valid charge termination. 図 36 shows a discharge cycle. Notice that the relative state of charge (RSOC) held at 7% for some seconds because the battery learned a larger capacity. 図 37 shows a charge cycle of the battery.

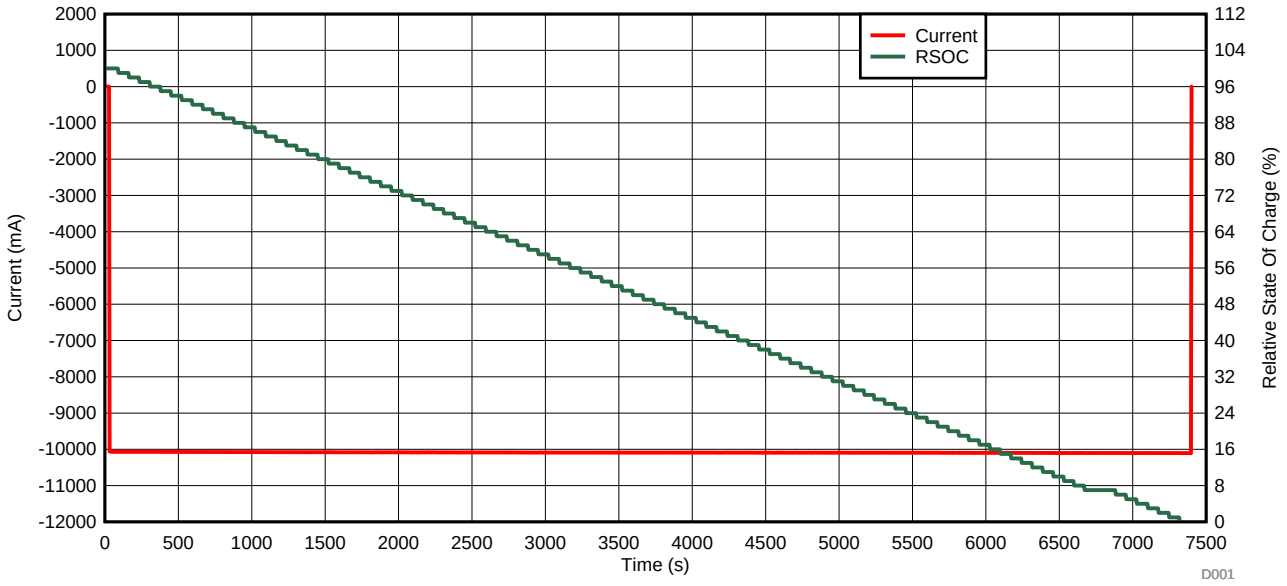

図 36. Gauging Discharge

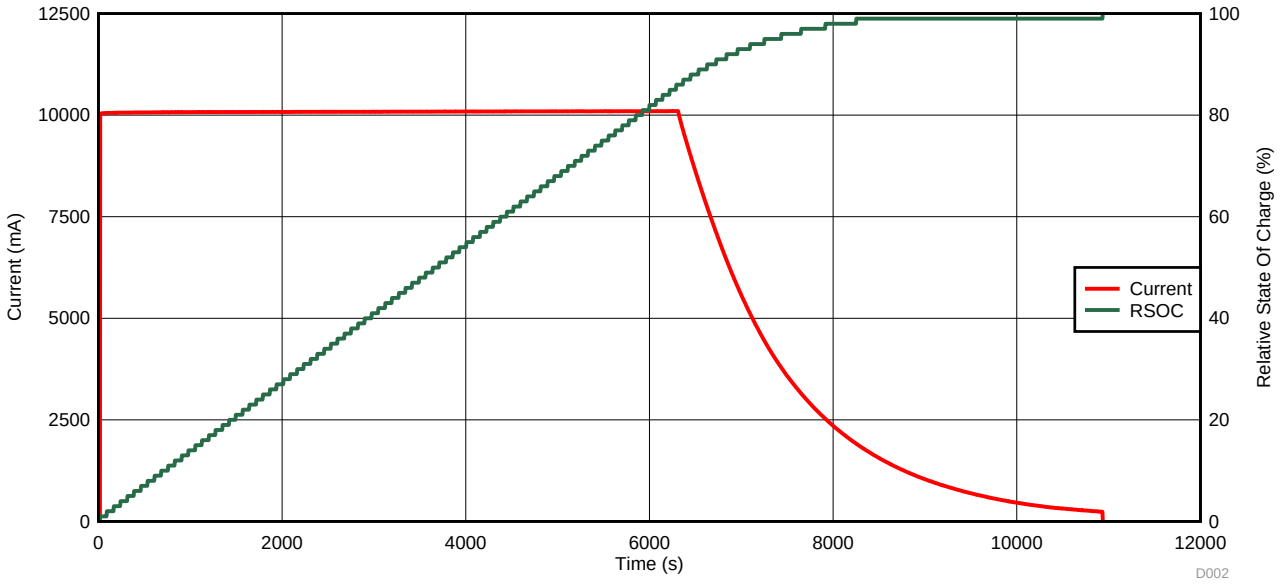

図 37. Gauging Charge

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-00792.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00792.

4.3 PCB Layout Recommendations

With a chassis mounting plan for this TI Design board, the layout is not space constrained. A single-sided assembly has been selected. While the board is intended to carry high current, a 1-oz copper is selected with plating for an approximate 2-oz final thickness. 図 38 shows the functional sections of this layout.

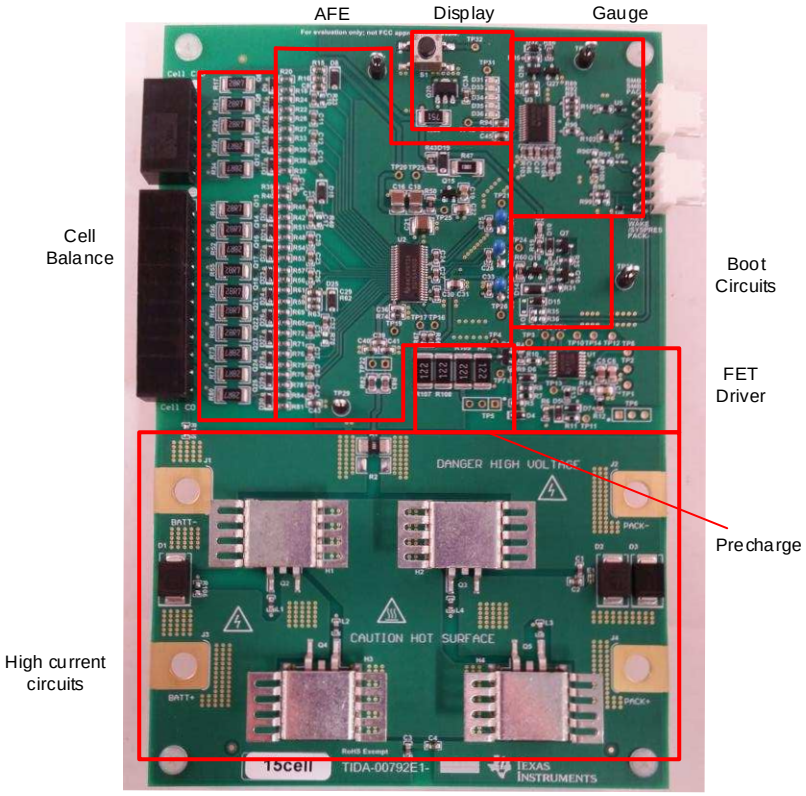

図 38. PCB Functional Sections

The high current paths on the board are the connections through the FETs and sense resistor. These paths are grouped together so the current and return paths are close together and physically separated from the low current circuits. The physical separation avoids coupling from the high current paths into sensitive low voltage circuits. While exposure to ESD in a cabinet-mounted board should be rare, ESD currents from signals likely to be exposed are directed to PACK–. Traces for these components are wide for low impedance connections. The electronics "ground" is referenced to BATT–. Rather than allowing components connected to ground to connect at various points on the BATT– path and be at different voltage potentials due to the pack current, a narrow copper connection is made between BATT– and ground on the board. This task is accomplished with the net tie shown on the schematic.

The precharge circuit is low current but may dissipate significant heat. The circuit is located near the center of the board so heat can spread in all areas. For designs allowing higher voltage differentials and dissipation, more area should be allocated to the precharge circuit or an additional heat sink should be provided.

FET drivers should be placed near the power FETs but are controlled by low voltage signaling from both the gauge and AFE and those traces should avoid coupling from high currents. The driver and related components are placed near the high current path section.

Cell inputs are brought into the board on connectors at the top left of the board view. The cell balancing connections are kept short with wide traces to help dissipate power from the balancing current. At the cell group, boundaries of the AFE routing for the different groups is separated at the connector pins. In 図 39 note that there are separate routes from the C5 connector terminal to the balance resistor R29, R57, and R59.

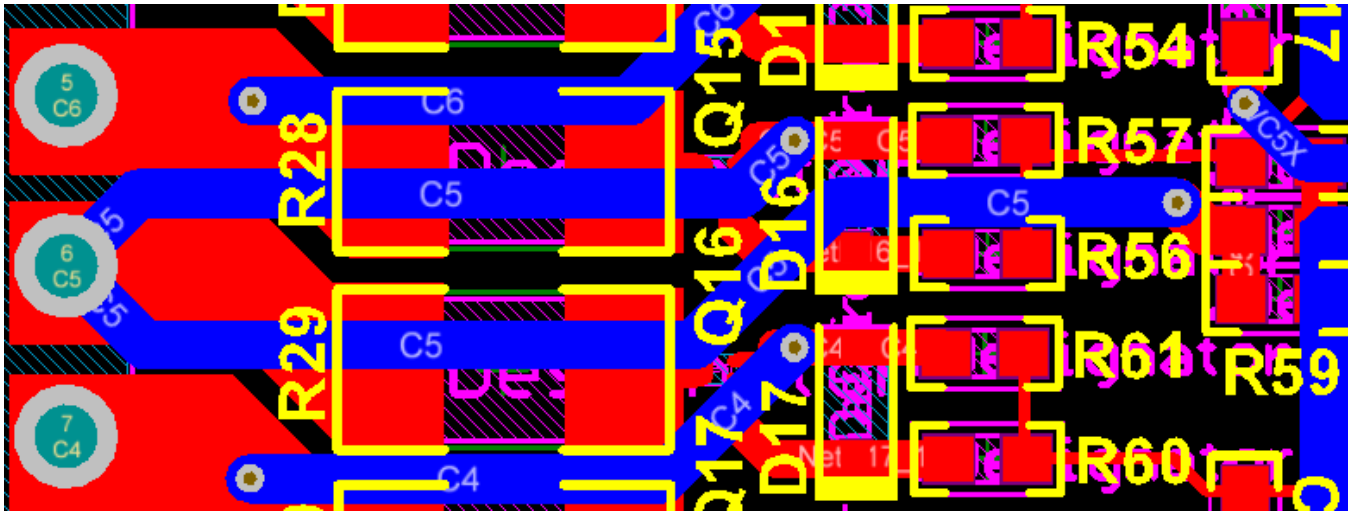

図 39. C5 Layout

The signals flow from the balance circuit to the AFE input filters and on to the AFE near the board center. Placing the input filters near the integrated circuit is preferred; however, the fanout for the pins can make this placement difficult and this design uses filters that have been arranged in a column. The current sense filter should be placed close to the AFE. Current sense routing should be symmetrical like a differential pair, not for impedance control but to minimize noise pickup on the two lines. Kelvin connections should be used for the sense resistor. In this design, the route is relatively short and a connection is made under the closest sense resistor. The boot circuit is located near the AFE and the FET driver where the required signals are available.

The gauge circuit is located away from the high current area and central to its connections to the offboard connectors, the AFE and the FET driver. The LEDs are controlled by the gauge and are arranged in order so they can be viewed through a window with the activation switch nearby. In some designs, the designer may wish to locate the display remotely and bring these to a connector; however, this option is not provided on this design.

Layout recommendations for battery fuel gauge designs are provided in the *PCB Layout Guidelines for Fuel Gauge Design* video[11].

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00792.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-00792.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00792.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00792.

5 Related Documentation

1. Texas Instruments, *bq769x0 3-Series to 15-Series Cell Battery Monitor Family for Li-Ion and Phosphate Applications*, bq76940 Datasheet (SLUSBK2)
2. Texas Instruments, *bq78350-R1 Technical Reference*, bq78350-R1 Technical Reference Manual (SLUUBD3)
3. Texas Instruments, *bq76200 Beyond the Simple Application Schematic*, bq76200 Application Report (SLUA794)
4. Texas Instruments, *bq769x0 Family Top 10 Design Considerations*, bq76940 Application Report (SLUA749)
5. Texas Instruments, *bq76930 and bq76940 Evaluation Module*, bq76940EVM User's Guide (SLVU925)
6. Texas Instruments, *bq78350-R1 CEDV Li-Ion Gas Gauge and Battery Management Controller Companion to the bq769x0 Battery Monitoring AFE*, bq78350-R1 Datasheet (SLUSCD0)
7. Texas Instruments, *bq76200 High Voltage Battery Pack Front-End Charge/Discharge High-Side NFET Driver*, bq76200 Datasheet (SLUSC16)
8. Texas Instruments, *CSD19536KTT 100-V N-Channel NexFET™ Power MOSFET*, CSD19536KTT Datasheet (SLPS540)
9. Texas Instruments, *CSD13381F4 12 V N-Channel FemtoFET™ MOSFET*, CSD13381F4 Datasheet (SLPS448)
10. Texas Instruments, *10s Battery Monitoring, Balancing, and Comp Protection, 50A Discharge Ref Design*, TIDA-00449 Reference Guide (TIDUAR8)
11. Texas Instruments; Cosby, Tom; *PCB Layout Guidelines for Fuel Gauge Design*, TI Training Video (https://training.ti.com/pcb-layout-guidelines-fuel-gauge-design)

5.1 商標

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