参考資料

TI Designs: TIDA-01168
12V/48V車載システム用双方向DC/DCコンバータのリファレンス・デザイン

TEXAS INSTRUMENTS

概要

TIDA-01168リファレンス・デザインは、12V/48V車載システム用の4相、双方向DC/DCコンバータ開発プラットフォームです。このシステムは、2つのLM5170-Q1電流コントローラと1つの C2000™TMS320F28027Fマイクロコントローラ(MCU)を使用して、電力段の制御を行います。LM5170-Q1サブシステムは、革新的な平均電流制御方式を使用して電流制御を行い、C2000™マイクロコントローラがシステムへ電圧フィードバックを行います。この制御方式により、マルチフェーズ・コンバータでは一般的な、追加の位相電流平衡化回路が不要になります。LM5170-Q1をベースとするシステムは高集積度を実現し、プリント基板(PCB)面積の低減、設計の簡素化、開発期間の短縮を可能にします。TIDA-01168のリファレンス・デザインは、12V/48V車載用システムの一般的な動作電圧要件を満たしています。

リソース

TIDA-01168	デザイン・フォルダ
LM5170-Q1	プロダクト・フォルダ
TMS320F28027F	プロダクト・フォルダ
LM5010A-Q1	プロダクト・フォルダ
TPS560200-Q1	プロダクト・フォルダ
TMP102-Q1	プロダクト・フォルダ
TPS3306-Q1	プロダクト・フォルダ
MC33063A-Q1	プロダクト・フォルダ
TLC2272-Q1	プロダクト・フォルダ

TI E2E™ Community

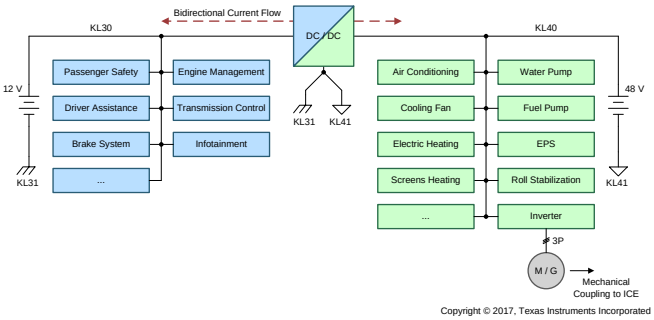
E2Eエキスパートに質問

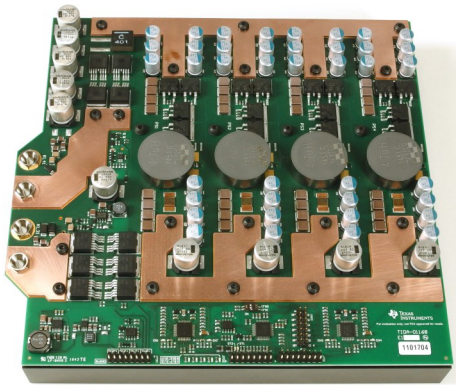
特長

- 12V入力電圧範囲: 6V～18V
- 48V入力電圧範囲: 24V～54V
- 逆極性、過電流、過電圧、過熱保護
- マルチフェーズ・スケーラブル・オプション
- 車載用認証部品を使用した高集積ソリューション

アプリケーション

- 12V/48V車載用システムでの車内用電力分配
- スーパーキャパシタまたはバッテリ・バックアップ電力コンバータ





1 System Description

A bidirectional DC-DC converter applies in efficient electrical energy transfer and storage applications. A typical system uses two batteries, battery and motor-generator, or a combination of both (see 図 1). Lithium-Ion (Li-Ion) or Lithium-Polymer (Li-Pol) technology provides the best performance. Alternatively, lead-acid batteries (Pb) are used for high-capacity and low-cost energy storage.

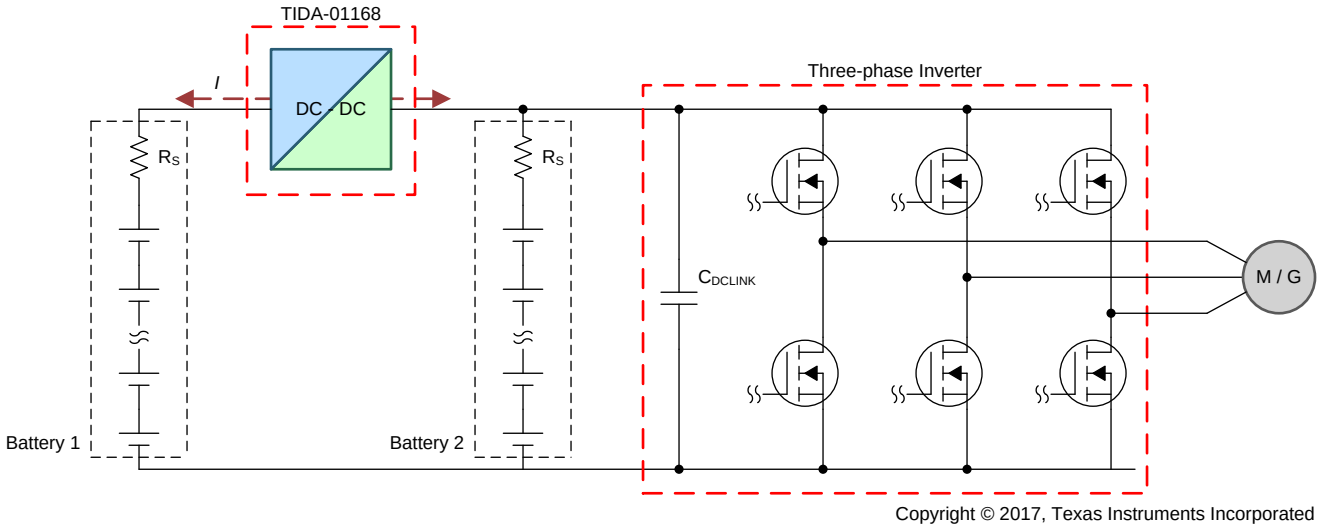


図 1. Dual Battery System Combined With Motor Generator

Modern Li-Ion and Li-Pol batteries have very-low series resistance and flat discharging curve. 図 2 shows a typical discharge curve for a Li-Pol cell. The blue and red line represent different discharge currents with reference to the nominal cell capacity C. Note that cell voltage does not change significantly with the charge level from 0% to 80%.

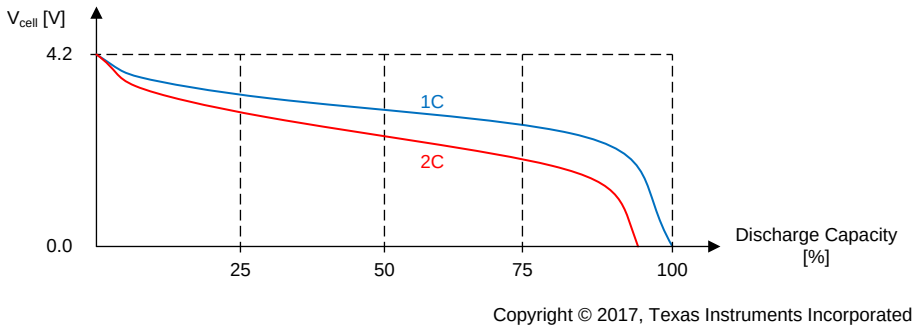


図 2. Li-Pol Cell Typical Discharge Curve

For this reason, operating voltage on the power rails does not significantly change. The charge and discharge process of the cells affects slow voltage changes whereas the internal series resistance, R_i, causes short voltage transients. Consequently, the current control loop performance is more important than the voltage loop.

The TIDA-01168 uses the LM5170-Q1, which is a bidirectional, switched-mode current controller. In this case, the DC-DC converter operates more as an ideal current source with variable direction. This configuration allows energy transfer between two voltage domains. The microcontroller-based voltage feedback only maintains output voltage within the acceptable operating range and eventually allows a custom charging profile for the battery pack. See the key system specifications in 1.1.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS
AD conversion resolution	12 b
Voltage reference	2.495 V
Control loop resolution	10 b
Switching frequency	100 kHz
MCU system clock	50 MHz
Digital loop update rate	48.828125 kHz
Number of phases	Four
Output power (BUCK mode)	< 2 kW
Output power (BOOST mode)	< 2 kW
12-V terminal input operating voltage	6 V to 18 V; nominal 12 V
48-V terminal input operating voltage	24 V to 54; nominal 48 V
Efficiency (BUCK mode)	< 97 %
Efficiency (BOOST mode)	< 97 %
Maximum output current (BUCK mode)	< 166 A
Maximum output current (BOOST mode)	< 42 A

2 System Overview

The TIDA-01168 reference design is intended to serve as a development basis for a bidirectional DC-DC converter for 12-V/48-V automotive systems, not a complete solution. Advanced features such as CAN communication or safety solutions to meet any Automotive Safety Integrity Level (ASIL) are not a part of the design.

2.1 Block Diagram

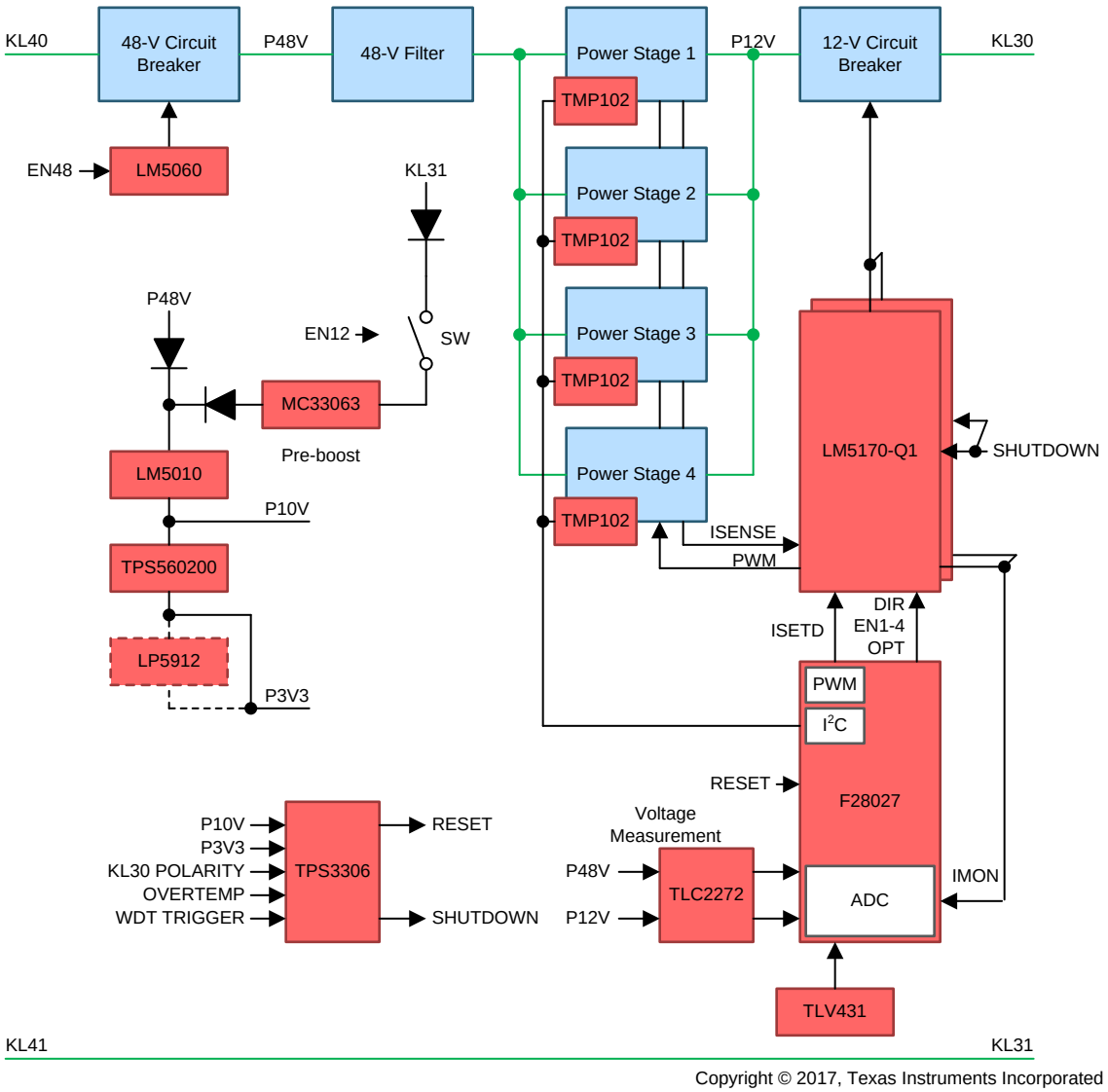


図 3. TIDA-01168 Block Diagram

2.2 Introduction to 48-V Systems

Reducing the environmental burden caused by excess emissions is an increasingly growing trend throughout the world and across all industries, including automotive. Carbon dioxide (CO_2), while not regulated as an air pollutant, is the transportation sector's primary contribution to climate change [1]. In 2009 the European Commission set a target for 2015 fleet average of CO_2 emissions to 130 grams per kilometer. Manufacturers are allowed to form a transparent pool for up to five years to achieve this target. In 2016 the average emissions level of a new car sold was 118.1 g/km. At the time of this writing, the European Commission has recently introduced a new regulation for CO_2 emission limits. An even stricter regulation with 95 g CO2 / km limit is to begin in 2020 for the fleet average of each manufacturer [2].

Violation of these regulations results in an excess emissions premium to be paid by the car manufacturer. Car manufacturers apply various strategies to fulfill these emissions requirements. Increasing the in-vehicle power voltage is one of these strategies. The European automotive industry encourages 48-V technology as the next evolution step in onboard vehicle power. 48-V technology better optimizes power distribution in a vehicle, allows weight reduction, and allows for mild-hybrid operation while keeping costs reasonable. This technology altogether helps to reduce CO2 emissions. Five European OEM car manufacturers contribute to 48-V systems standardization. System requirements are specified in the VDO320 and LV148 norms (see 図 4).

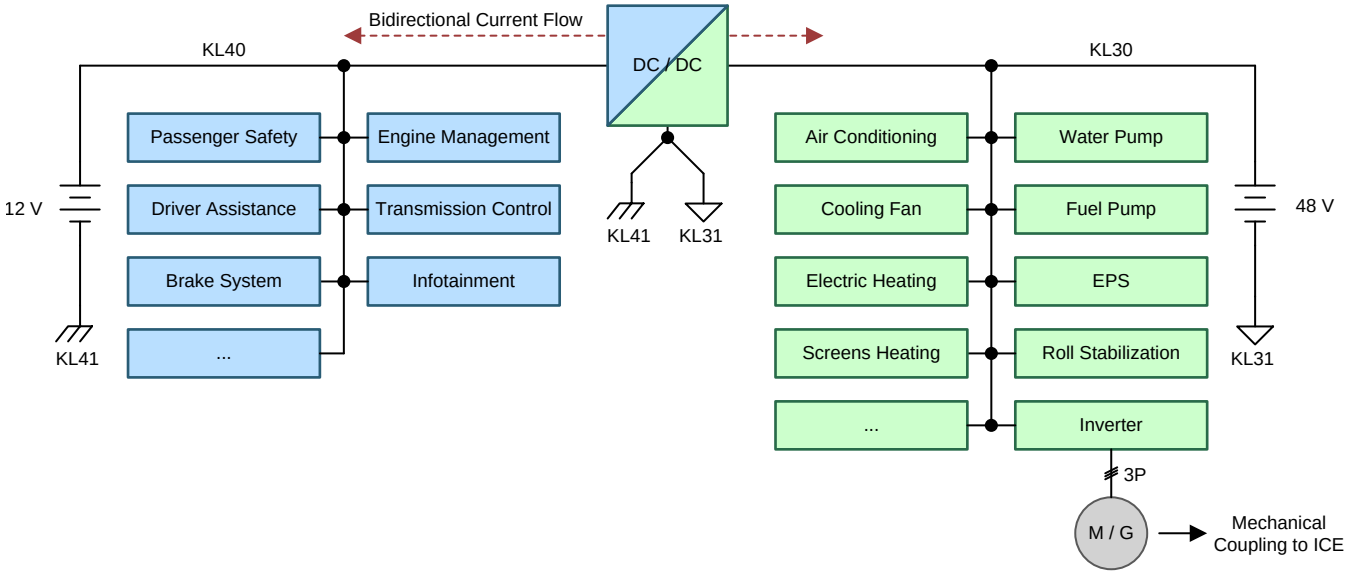


図 4. Split In-Vehicle Power in Typical 12-V and 48-V System

図 4 shows the typical structure of a split in-vehicle power network. The strategy is to move all power hungry components to the 48-V side with a Li-Ion battery, Li-Fe battery, or supercapacitor energy storage. This measure reduces input current by a factor of four for the same output power.

One trend also shows integration of the starter and generator into a single device:

- Integrated starter-generator (commercially referred to as ISG, ISA, ISAD, CAS, CSA, CISG, and so forth)
- Belt starter-generator (commercially referred to as BAS, BSG, BISG, BSA, eAssist, and so forth)

These inverter-controlled synchronous (permanent-magnet synchronous motor (PMSM)) or asynchronous machines are able to start the internal combustion engine (ICE), help with acceleration (torque assist), and recuperate energy during braking (regenerative braking). The 12-V power rail provides backward compatibility with current automotive systems such as infotainment or engine management. A traditional lead-acid battery also has better capacity-to-cost ratio, better performance at low temperatures, and lower self-discharge in comparison with supercapacitors. A bidirectional DC-DC converter is required for energy transfer between both sides. Step-down (buck) mode applies during normal operation when the ISG or BSG on the 48 V operates as a generator, such as in a conventional vehicle. Step-up (boost) mode applies during the ICE start when energy in the 48-V battery may not be sufficient. However, final implementation is different for different concepts.

2.2.1 48-V Systems Properties

図 5 shows the voltage levels specified in VDA320 and 表 2 describes them.

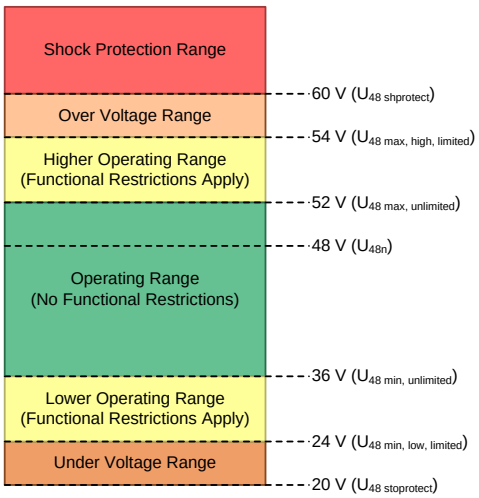


図 5. Voltage Levels Defined by VDA320

表 2. Voltage Levels Defined by VDA320

ABBREVIATION	NOTATION	VALUE
$U_{(48\ sh\ protect)}$	Shock protection voltage to fulfill the requirement to not exceed the limit for DC voltages in terms of shock protection according to ECE-R 100	60 V
$U_{(48r)}$	2-V contingency reserve to the shock protection voltage	58 V
$U_{(48\ max,\ high,\ limited)}$	Maximum voltage of the upper operating range with functional degradation	54 V
$U_{(48\ max,\ unlimited)}$	Minimum voltage of the upper operating range with functional degradation	52 V
$U_{(48n)}$	BN48 nominal voltage (the nominal voltage is based on DIN IEC 60038)	48 V
$U_{(48\ min,\ unlimited)}$	Minimum voltage of the operating range without functional degradation	36 V
$U_{(48\ min,\ low,\ limited)}$	Minimum voltage of the lower operating range with functional degradation	24 V
$U_{(48\ stoprotect)}$	Accumulator protection voltage	20 V

The following lists the general assumptions and requirements from VDA320 [11]:

- Static direct voltages ≤ 60 V occur with a maximum ripple of 10% RMS in the onboard supply voltage.
- A single error in the wiring harness must not cause the 48-V supply to short circuit to the 12-V/24-V system.
- There is a common ground for the 12-V/24-V system and the 48-V system, which are connected

through physically-separated grounding bolts or connections.

- All the voltage and current information refers to the component (terminal voltage).
- The polarity of the 48-V supply is prevented from reversing by appropriate measures in the vehicle.
- Jump starting with the 48-V power supply is prevented by appropriate measures applied in the vehicle.
- A single error must not cause a short circuit between the 48-V supply and the 12-V/24-V supply.
- Components simultaneously supplied at 48 V and 12 V/24 V, and interfaces based on 12 V/24 V, require their own ground connections for both supply voltages. These ground connections must be physically separated from one another.
- If a 48-V component loses its ground (terminal 31, terminal 41, or both), this must not disrupt or destroy communication networks or the electrical networks.
- Overcurrent tests should be detailed in the component specifications.
- No component may cause the voltage to enter the dynamic overvoltage range (for example, through a load dump or resonance peaks).
- If the voltage enters the overvoltage range up to $U_{(48r)}$, countermeasures should be taken through the component that is feeding energy back in or causing entry into the overvoltage range, so that the voltage exits the overvoltage range at the lower boundary.
- If the voltage enters the lower limited function range, countermeasures should be taken so that the voltage returns to the unlimited operation range.

2.2.2 48-V DC-DC Converter

Non-isolated synchronous step-down converter topology is the most common topology used. Synchronous switches allow bidirectional current flow in the boost mode. The topology is a synchronous step-down converter when looking from the 48-V side and the topology is a synchronous step-up converter when looking from the 12-V side, as 図 6 shows.

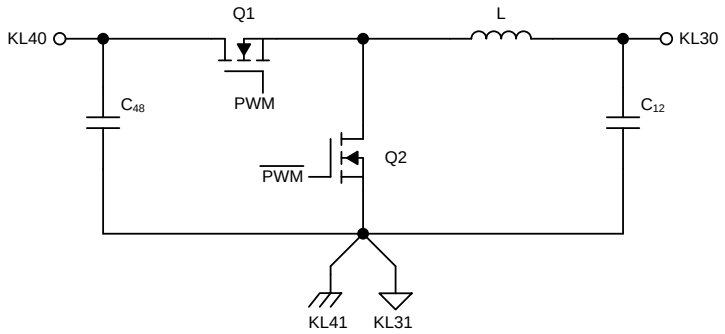


図 6. Non-Isolated Synchronous Step-Down Converter

A non-isolated DC-DC converter effectively creates a system star-point where common grounds for 12-V and 48-V voltage rails meet. This fact must be considered when designing the vehicle grounding concept. Equipment utilizing both power rails may require functional galvanic isolation to avoid ground loops that cause interference. Minimum standby current is achieved using a circuit breaker on the either side of the converter. The circuit breaker on the 12-V side also protects the converter against reverse polarity condition. Such a protection is not required on the 48-V side, which is intrinsically protected by appropriate measures in the vehicle.

The converter communicates with the host system over the system bus (CAN, FlexRay™).

2.3 High-Level Design Description

The TIDA-01168 is a multiphase DC-DC converter based on four buck power stages operating in parallel. A multiphase converter is an obvious choice for high-power applications. The typical benefits of a multiphase interleaved DC-DC converter are lower output ripple, which allows for smaller capacitors, faster transient response in comparison with a single-phase converter, smaller inductor size, and even power dissipation distribution over the board. 図 7 and 図 8 show how the root mean square (RMS) current is reduced based on the number of phases and duty cycle. The ideal case shows that the total ripple current for the given duty cycle, 25% for buck and 75% for boost mode, is reduced to the minimum. This reduced total ripple current helps to lower input and output capacitance to a minimum.

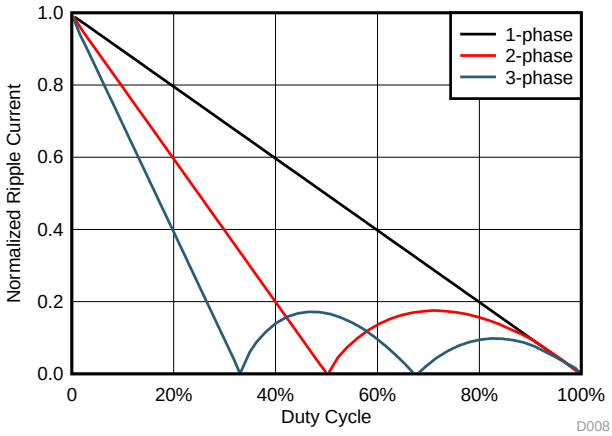


図 7. Buck Output RMS Current, Boost Input RMS Current

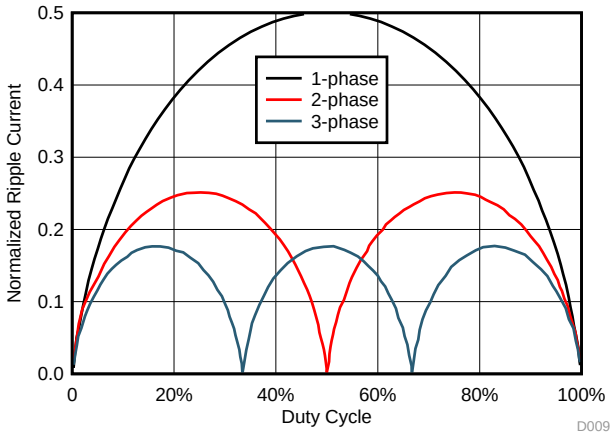


図 8. Buck Input RMS Current, Boost Output RMS Current

A pair of LM5170-Q1 devices control all four power stages. The LM5170-Q1 multiphase bidirectional current controller provides a complete control including gate drivers and current sensing. The device does not have any voltage feedback loop and acts as a switched mode current source driven by a pulse width modulation (PWM) or analog signal. The amount of current flowing to the load is given by the duty cycle on the ISETD signal. The direction (buck or boost) is set by the DIR signal.

The system uses a digital voltage feedback loop based on the TMS320F28027 C2000™ Piccolo 32-b MCU running at 50 MHz. 図 9 shows a simplified block diagram for a single phase. The 12-b analog-to-digital converter (ADC) in the MCU periodically reads output voltage every 20.48 µs. The current (set by the ISETD signal) through a load corresponds to the output voltage. The digital error amplifier compares the value from the ADC with the preset value (reference). The digital control loop with a digital compensator then calculates the error and sets a new duty cycle for the ISETD pin. The MCU optionally monitors voltage on the IMON pin, which corresponds to the current through the inductor. This information is not used for the control loop.

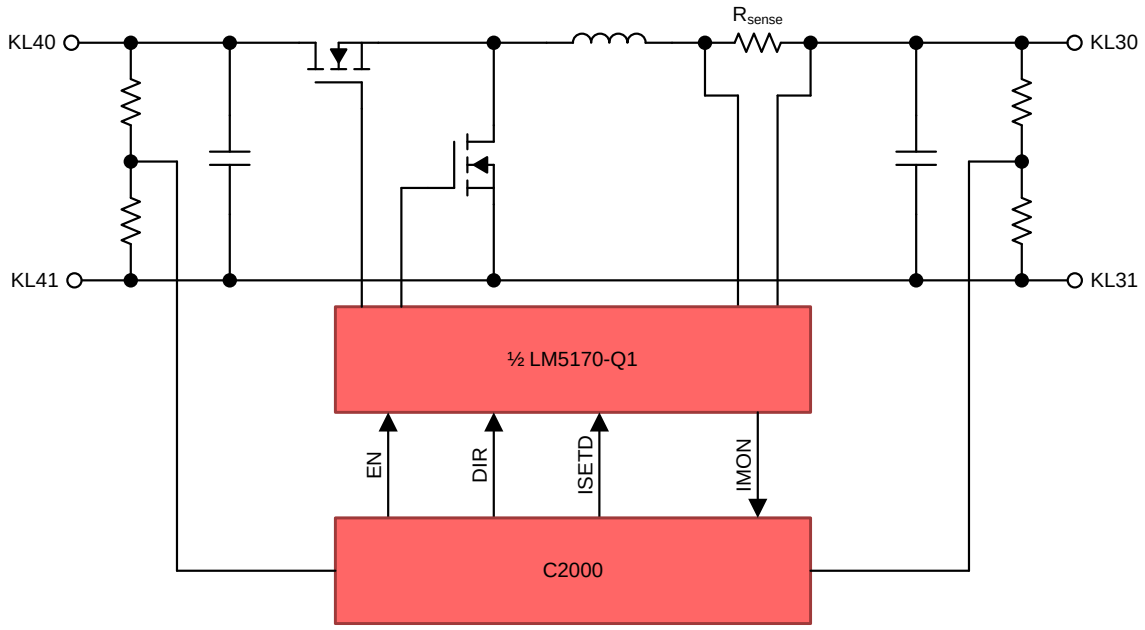


図 9. Simplified Block Diagram for Voltage and Current Feedback Loop

An L-C filter on the 48-V side helps to reduce output ripple in the boost mode. Output ripple in the boost mode is higher because, during t_{ON}, the load is energized only from the output capacitors.

Each side of the converter can be disconnected from the respective power rail by a circuit breaker based on back-to-back N-MOSFETs configuration. The circuit breaker on the 12-V side is fully controlled by the LM5170-Q1 device, which protects against reverse polarity conditions and allows very low standby current (I_Q) when the system is off. The circuit breaker is shut off when the LM5170-Q1 device detects a failure. This condition is reported by the nFAULT pin. The LM5060-Q1 high-side protection controller controls the 48-V side circuit breaker. Although reverse polarity protection is usually not required for the 48-V rail, a back-to-back N-MOSFETs configuration is used to prevent any current flow when the system is off. The LM5060-Q1 device can trigger on undervoltage, overvoltage, and overcurrent events.

The system can be turned on from either a 12-V or 48-V power rail. A pre-boost DC-DC converter based on the MC33063A-Q1 device is used in the case of a turnon from the 12-V side triggered by the EN12 signal. Input for this pre-boost circuit bypasses the high-current 12-V circuit breaker. Output of the pre-boost DC-DC converter is set to approximately 28 V to provide enough gate voltage for the 12-V circuit breaker. The pre-boost DC-DC uses a hysteretic-based control scheme and therefore automatically stops switching when the 48-V is present. Standby current consumption can be further reduced by setting the EN12 signal low when the P48V voltage is present.

Two additional DC-DC converters are required for a bias power supply. The LM5010-Q1 is a high V_{IN} step-down converter with a 10-V output for biasing LM5170-Q1 devices. The TPS560200-Q1 device is used for energizing the rest of the circuitry. The 3.3-V output matches the digital-logic operating-voltage level. An optional linear post-regulator LP5912-Q1 can be used in case the switching noise influences the analog circuitry.

A simple diagnostics block is available in the design. Four configurable TMP102-Q1 temperature sensors communicating over the I^2C bus monitor the temperature for each power stage. The ALERT output signals of these temperature sensors are connected to the shutdown signal, which switches off all the power stages after reaching the overtemperature threshold. The TPS3306-Q1 voltage supervisor and watchdog monitors the MCU and voltage rails. The programmable function input (PFI) detects polarity on KL30. Such a feature is required to restrict the 12-V circuit breaker opening during reverse polarity on the KL30. Without this restriction, high current flows through the inductor and body diode of the bottom MOSFET in all power stages, which results in permanent damage.

2.4 Mechanical Construction

The mechanical construction of TIDA-01168 has been optimized for easy debugging and affordable manufacturing costs using commercially available technologies. 図 10 shows the sandwich-like construction of the TIDA-01168 design.

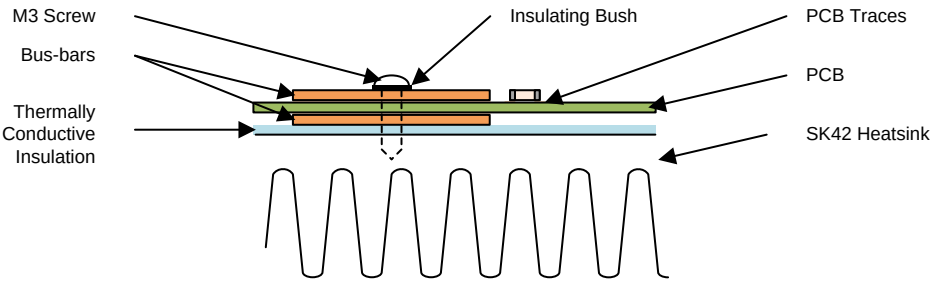


図 10. Sandwich Construction of TIDA-01168

The PCB has four layers with single-side component placement. 図 11 shows the FR-4 PCB layer stack. The current-carrying capability for high-current paths is further boosted by external, custom-built 1.5-mm thick copper bus bars. The bus bars are mounted on the top and bottom of the PCB on the exposed PCB traces. Bus bars are lacquered on visible sides with polyurethane transparent paint to prevent oxidation. Bus bars on the top layer carry positive voltages whereas the bus bar on the bottom is the common ground (negative terminal KL31, KL41).

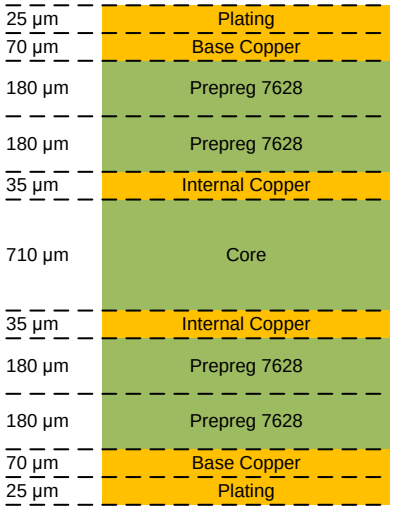


図 11. PCB Layer Stack for TIDA-01168

Thermally conductive insulator (AMEC THERMASOL: SFT80-0.15-T1) provides electrical isolation between the PCB with the bus bar on the bottom side and the heat sink. This isolation prevents the heat sink from carrying current, which is important for maintaining a defined current return path. Areas without the bottom bus bar have a 1.5-mm gap between the PCB and the heat sink. This gap is filled by "gap-filler" (T GLOBAL: L373-150-2.0A) for better heat transfer from the PCB to the heat sink. This filler is important for the power stages especially underneath of the inductor and MOSFETs.

The extruded 200×200-mm heat sink used in this design is made by Fischer Elektronik GmbH & Co. KG. The assembly is held together using M3x10 machine screws. Screws are isolated from all active conductors by isolation bushings similar to those shown in 図 12, which are typically used to isolate TO220 packages. A drilling plan for the heat sink as well as copper bus bar drawings are available as a part of the documentation.

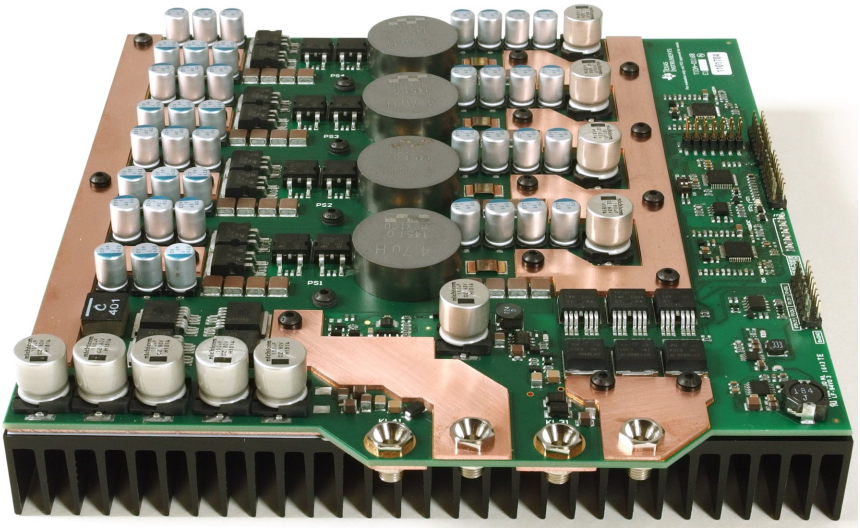


図 12. TIDA-01168 Assembled Prototype

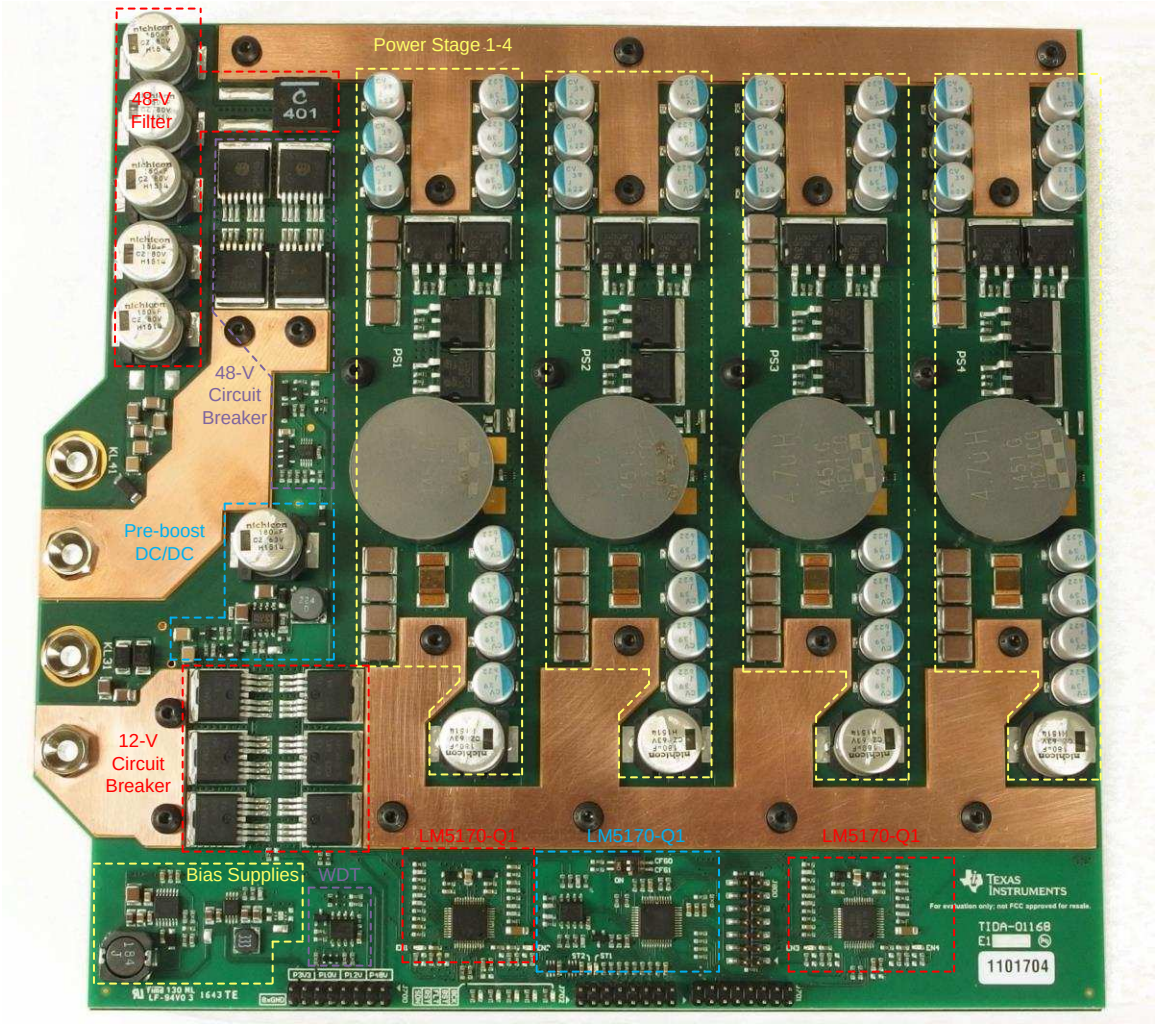


図 13. TIDA-01168 PCB Structuring

表 3. TIDA-01168 PCB Layout—Selected Design Rules

SEGMENT	DIMENSIONS
General traces (analog, digital)	8 mil minimum, 10 mil typical
Power traces – low current < 1 A	30 mil typical
Gate driver traces	30 mil typical
Via size	28 mil/12 mil (diameter/drill)
Clearance for power nets	20 mil
Clearance for other traces	6 mil minimum, 10 mil typical
Components placement	Top side only
Passive components package size	0603 (preferred) or larger

2.5 Highlighted Products

2.5.1 LM5170-Q1

The LM5170-Q1 controller provides the essential high voltage and precision elements of a dual-channel bidirectional converter for automotive 48-V and 12-V dual battery systems. The controller regulates the average current flowing between the high-voltage- and low-voltage ports in the direction designated by the DIR input signal. The current regulation level is programmed through analog or digital PWM inputs. Dual-channel differential current sense amplifiers and dedicated channel current monitors achieve typical current accuracy of 1%. Robust 5-A half-bridge gate drivers are capable of driving parallel MOSFET switches delivering 500 W or more per channel. The diode emulation mode of the synchronous rectifiers prevents negative currents but also enables discontinuous mode operation for improved efficiency with light loads. Versatile protection features include cycle-by-cycle current limiting, overvoltage protection at both HV and LV ports, MOSFET failure detection, and overtemperature protection. An innovative average current mode control scheme maintains constant loop gain allowing a single R-C network to compensate both buck and boost conversion. The oscillator is adjustable up to 500 kHz and can synchronize to an external clock. Multiphase parallel operation is achieved by connecting two LM5170-Q1 controllers for three or four-phase operation, or by synchronizing multiple controllers to phase-shifted clocks for a higher number of phases. A low state on the undervoltage lockout (UVLO) pin disables the LM5170-Q1 in a low-current shutdown mode.

2.5.2 TMS320F28027

The F2802x Piccolo™ family of microcontrollers provides the power of the C28x core coupled with highly-integrated control peripherals in low pin-count devices. This family is code-compatible with previous C28x-based code and also provides a high level of analog integration. An internal voltage regulator allows for single-rail operation. Enhancements have been made to the HRPWM to allow for dual-edge control (frequency modulation). Analog comparators with internal 10-bit references have been added and can be routed directly to control the PWM outputs. The ADC converts from 0-V to 3.3-V fixed full-scale range and supports ratio-metric VREFHI/VREFLO references. The ADC interface has been optimized for low overhead and latency.

2.5.3 LM5010A-Q1

The LM5010Ax step-down switching regulator is an enhanced version of the LM5010 with the input operating range extended to a 6-V minimum. The LM5010Ax features all the functions required to implement a low-cost, efficient, buck regulator capable of supplying in excess of 1-A load current. This high-voltage regulator integrates an N-channel buck switch and is available in thermally-enhanced 10-pin WSON and 14-pin HTSSOP packages. The constant ON-time regulation scheme requires no loop compensation resulting in fast load transient response and simplified circuit implementation. The operating frequency remains constant with line and load variations due to the inverse relationship between the input voltage and the ON-time. The valley current limit detection is set at 1.25 A. Additional features include: VCC undervoltage lockout, thermal shutdown, gate drive undervoltage lockout, and maximum duty cycle limiter.

2.5.4 TPS560200-Q1

The TPS560200-Q1 is a 17-V, 500-mA, low-I_Q, adaptive ON-time D-CAP2 mode synchronous monolithic buck converter with integrated MOSFETs in an easy-to-use 8-pin MSOP package. The TPS560200-Q1 enables system designers to complete the suite of various end-equipment power bus regulators with a cost-effective, low component count, and low standby current solution. The main control loop for the device uses the D-CAP2 mode control that provides a fast transient response with no external compensation components. The adaptive ON-time control supports seamless transition between PWM mode at higher load conditions and advanced Eco-mode™light load efficiency at light loads. The TPS560200-Q1 also has a proprietary circuit that enables the device to adopt to both low equivalent series resistance (ESR) output capacitors, such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors. The device operates from a 4.5-V to 17-V V_{IN} input. The output voltage can be programmed between 0.8 V and 6.5 V. The device also features a fixed 2-ms soft-start time. The device is available in the 8-pin MSOP package.

2.5.5 TMP102-Q1

The TMP102-Q1 device is a digital temperature sensor ideal for NTC/PTC thermistor replacement where high accuracy is required. The device offers an accuracy of ±0.5°C without requiring calibration or external component signal conditioning. Integrated circuit temperature sensors are highly linear and do not require complex calculations or look-up tables to derive the temperature. The on-chip 12-bit ADC offers resolutions down to 0.0625°C. The 1.6-mm × 1.6-mm SOT563 package has a 68% smaller footprint than an SOT23 package. The TMP102-Q1 device features SMBus™, which is compatible with two-wire and I^2C interface and allows up to four devices on one bus. The device also features an SMBus alert function. The device is specified to operate over supply voltages from 1.4 V to 3.6 V with the maximum quiescent current of 10 µA over the full operating range. The TMP102-Q1 device is ideal for extended temperature measurement in a variety of communication, computer, consumer, environmental, industrial, and instrumentation applications. The device is specified for operation over a temperature range of –40°C to 125°C. The TMP102-Q1 production units are 100% tested against sensors that are NIST-traceable and are verified with equipment that are NIST-traceable through ISO/IEC 17025 accredited calibrations.

2.5.6 TPS3306-Q1

The TPS3306 family is a series of supervisory circuits designed for circuit initialization that requires two supply voltages, primarily in digital signal processing (DSP) and processor-based systems. The product spectrum of the TPS3306-xx is designed for monitoring two independent supply voltages of 3.3 V/1.5 V, 3.3 V/1.8 V, 3.3 V/2 V, 3.3 V/2.5 V, or 3.3 V/5 V. During power up, RESET is asserted when the supply voltage VDD becomes higher than 1.1 V. Thereafter, the supervisory circuits monitor the SENSEn inputs and keep RESET active as long as SENSEn remains below the threshold voltage VIT. An internal timer delays the return of the RESET output to the inactive state (high) to ensure proper system reset. The delay time, td(typ) = 100 ms, starts after the SENSE1 and SENSE2 inputs have risen above the threshold voltage VIT. When the voltage at SENSE1 or SENSE2 input drops below the threshold voltage VIT, the output becomes active (low) again. The integrated power-fail (PFI) comparator with separate open-drain (PFO) output can be used for low-battery detection, power-fail warning, or for monitoring a power supply other than the main supply. The TPS3306-xx devices integrate a watchdog timer that is periodically

triggered by a positive or negative transition of WDI. When the supervising system fails to retrigger the watchdog circuit within the time-out interval, tt(out) = 0.50 s, the RESET becomes active for the time period td. This event also reinitializes the watchdog timer. Leaving WDI unconnected disables the watchdog. The TPS3306-xx devices are available in standard 8-pin SO packages. The TPS3306-xxQ family is characterized for operation over a temperature range of –40°C to 125°C.

2.5.7 MC33063A-Q1

The MC33063A-Q1 device is an easy-to-use integrated circuit containing all the primary circuitry required for building simple DC-DC converters. The device primarily consists of an internal temperature-compensated reference, a comparator, an oscillator, a PWM controller with active current limiting, a driver, and a high-current output switch. Thus, the device requires minimal external components to build converters in the boost, buck, and inverting topologies.

2.5.8 TLC2272-Q1

The TLC2272-Q1 and TLC2274-Q1 devices are dual and quadruple operational amplifiers from Texas Instruments. Both devices exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLC227x-Q1 family offers 2 MHz of bandwidth and 3 V/µs of slew rate for higher-speed applications. These devices offer comparable AC performance while having better noise, input offset voltage, and power dissipation than existing CMOS operational amplifiers. The TLC227x-Q1 has a noise voltage of 9 nV/$\sqrt{\text{Hz}}$, which is two times lower than competitive solutions. The TLC227x-Q1, exhibiting high input impedance and low noise, is excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. In addition, the rail-to-rail output feature, with single- or split-supplies, makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLC227xA-Q1 family is available with a maximum input offset voltage of 950 µV. This family is fully characterized at 5 V and ±5 V. The devices offer increased output dynamic range, lower noise voltage, and lower input offset voltage. This enhanced feature set allows the devices to be used in a wider range of applications. For applications that require higher output drive and wider input voltage range, see the TLV2432-Q1 and TLV2442-Q1 devices. All of the parameters of the TLC227x-Q1 family enables the device to be applicable in most automotive applications.

3 Hardware Design

注: This text does not cover the fundamental theory of operation.

3.1 48-V Circuit Breaker

3.1.1 Description

The 48-V circuit breaker allows the DC-DC to completely disconnect from the 48-V battery rail using field-effect transistors (FETs). The block also protects the DC-DC against overvoltage and overcurrent. See 表 4 for a system interface overview.

表 4. System Interface for 48-V Circuit Breaker

SIGNAL	DIRECTION	DESCRIPTION
KL40	In/Out	48-V car battery system terminal (positive)
KL41	In/Out	48-V car battery system terminal (negative)
P48V	In/Out	Protected 48-V rail (positive)
PGND	In/Out	Protected 48-V rail (negative)
KL40_M	Out	48-V battery four-wire voltage measurement terminal (positive)
KL41_M	Out	48-V battery four-wire voltage measurement terminal (negative)
EN48	In	Enable signal.; voltage greater than 2.0 V enables the circuit breaker; voltage on this pin shall not exceed 65 V

3.1.2 Considerations

The 48-V circuit breaker conducts and disconnects current up to 50 A in both directions for voltages up to 70 V. The limit of 70 V for 40 ms is given by the E48-02 Transient Overvoltage test defined in VDA320. The ability to disconnect current flow in both directions is generally required; therefore, a back-to-back MOSFETs configuration is used. This requirement is also beneficial; for example, pre-charging the 48-V side capacitors to the KL40 voltage reduces the inrush current during turnon. Selected MOSFETs have a very low $R_{DS(ON)}$ and are rated up to 100 V. MOSFETs are in parallel to further reduce I^2R losses caused by $R_{DS(ON)}$. Gate charge is not important as long as the LM5060-Q1 device is able to turn them ON and OFF fast enough. Give careful consideration to the safety operating area (SOA).

The protected side of the 48-V circuit breaker is used as a reference point for the voltage measurement circuitry.

注: The absolute maximum input and gate voltage for LM5060-Q1 is 75 V at 25°C. Contact a TI representative for 100-V capable solutions.

3.1.3 HW Implementation

図 14 shows a schematic of the 48-V circuit breaker implementation.

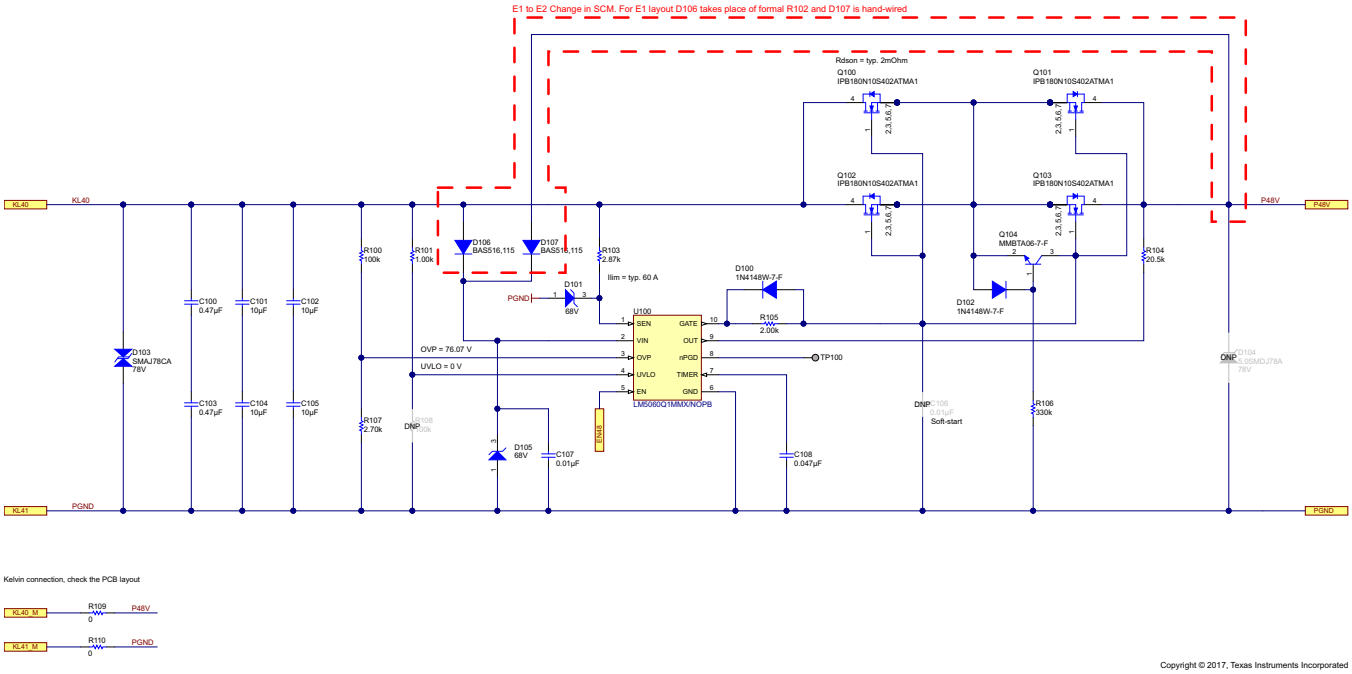


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図 14. 48-V Circuit Breaker Schematic

A transient voltage suppression (TVS) diode D103 and a group of capacitors C100 through C105 comprise the basic board-level input transient protection. The TVS diode is bidirectional to allow the input to withstand the reverse polarity condition. Capacitors in series reduce the probability of a short circuit in case of single capacitor failure. The minimum breakdown voltage for the diode must be over 70 V under any circumstances (tolerance, temperature drift) to avoid conducting during the E48-02 test. Capacitors are rated for 50 V. The series configuration for the capacitors increases the voltage rating by an approximate factor of 1.5 to 75 V considering the tolerance and manufacturing span.

注: The component values have been chosen to protect the system in a laboratory environment only. Component selection for the automotive environment depends on the mechanical construction, cable length, and required criteria.

The U100 controls the Q100 through Q103 MOSFETs using an internal charge pump. Diodes D106 and D107 protect the VIN pin of the U100 in the event of reverse polarity. "OR" configuration of the diodes allow U100 operation either from the protected P48V or unprotected KL40 rail. This measure is important for the DC-DC converter turnon. Diode D106 conducts during start-up in BUCK mode from the KL40 rail. Diode D107 conducts during start-up in BOOST mode from the KL30 rail when the voltage on the KL40 rail is not present. C107 is a 100-V rated bypass capacitor. Diodes D101 and D105 are optional transient suppressors. Two resistor dividers R100, R107 and R101, R108 set the overvoltage and undervoltage threshold for U100. Undervoltage detection is not used. Transistor Q104, diode D102, and resistor R106 protect the transistor pair Q101 and Q103 from exceeding the maximum V_{GS} during a reverse polarity event. If the voltage on the drains of any of the Q100, Q102 or Q101, Q103 pairs is below ground (KL41, KL31) then the transistor Q104 starts conducting, which reduces V_{GS} to nearly zero. Resistor R106 sets the bias current through the base of Q104. Diode D102 protects the base-emitter junction of Q104 against

reverse polarity during normal operation, which results in a small standby current through R106. The resistor R105 protects the GATE pin from reverse current exceeding 25 mA in the reverse polarity situation. R105 also affects the turnon and turnoff times for the Q100-Q103 pairs. For this reason, the diode D100 is used to reduce the turnoff time to the minimum. Capacitor C106 is the optional soft-start. Capacitor C108 is the timing capacitor, which sets the V_{DS} fault detection time for U100.

Resistors R109 and R110 allow disconnecting the voltage measurement circuitry from the measurement points during development and testing.

The PCB layout that 図 15 shows does not require any special considerations. All components are placed on the top side. Board-level input transient protection is close to the KL41 and KL40 terminals. Series-connected capacitors are 90° relative to one another. This technique is frequently used in the automotive industry to reduce the probability of simultaneous electrode cracking under mechanical stress. This technique is important because in most cases a cracked electrode of a ceramic capacitor shorts the capacitor. A hazardous situation and permanent damage of the board may occur if only a single capacitor is used or an electrode crack happens for both capacitors in series. Alternatively, capacitors with flexible SMD termination may be used. This general rule applies to all ceramic capacitors without any current-limiting element connected to the vehicle power rail.

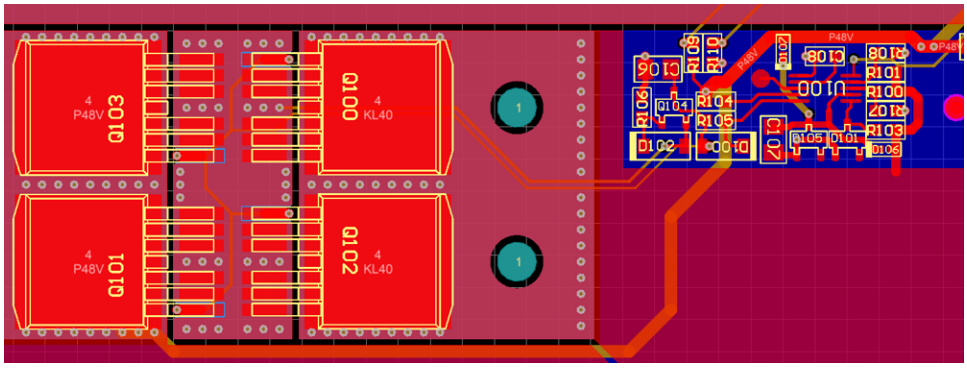


図 15. 48-V Circuit Breaker PCB Layout

3.1.4 Test Data

See 6.1 for the test data.

3.1.5 Further Reading

See the following resources for more information:

1. Texas Instruments, *Automotive 12- and 24-V Battery Input Protection Reference Design*, TIDA-01167 Reference Design (TIDUC41)
2. Texas Instruments, *Complete Front End Automotive Reverse Polarity and Series Fault Protection Reference Design*, PMP10748 Reference Design (TIDUAW9)

3.2 48-V Filter

3.2.1 Description

The L-C filter on the P48V voltage rail mainly helps to reduce output ripple in the boost mode. See 表 5 for the system interface overview.

表 5. System Interface for 48-V Filter

SIGNAL	DIRECTION	DESCRIPTION
P48V	In/Out	Protected 48-V rail (positive - filtered)
PGND	In/Out	Protected 48-V rail (negative)
P48V_NF	In/Out	Protected 48-V rail (positive - unfiltered)

3.2.2 Considerations

In contrast with a typical DC-DC converter application, a battery is connected to the output of a DC-DC converter in 12-V/48-V automotive systems. This battery effectively helps to reduce output voltage ripple, especially within a low frequency range. Adding an L-C filter on the output of a boost converter helps to reduce output voltage ripple even further. Consider the following measures:

- The highest output voltage ripple occurs in single-phase operation.
- Output voltage ripple increases with a higher load.
- Capacitors must be dimensioned for the given ripple current.
- An L-C filter affects the compensation (stability) for both BUCK and BOOST mode.
- The saturation current of the inductor must be higher than the average DC current.
- Increasing the inductance for the same cutoff frequency results in a higher Q-factor and an additional dumping network may be necessary to prevent oscillations and ringing.

注: The SPICE circuit simulator helps with identifying initial component values. Use models containing equivalent series inductance (ESL) and equivalent series resistance (ESR) for capacitors and DC resistance (DCR) for inductors. A designer can replace the power stage with an ideal current source that simulates the power inductor ripple current in continuous mode.

3.2.3 HW Implementation

図 16 shows a schematic of the 48-V filter implementation.

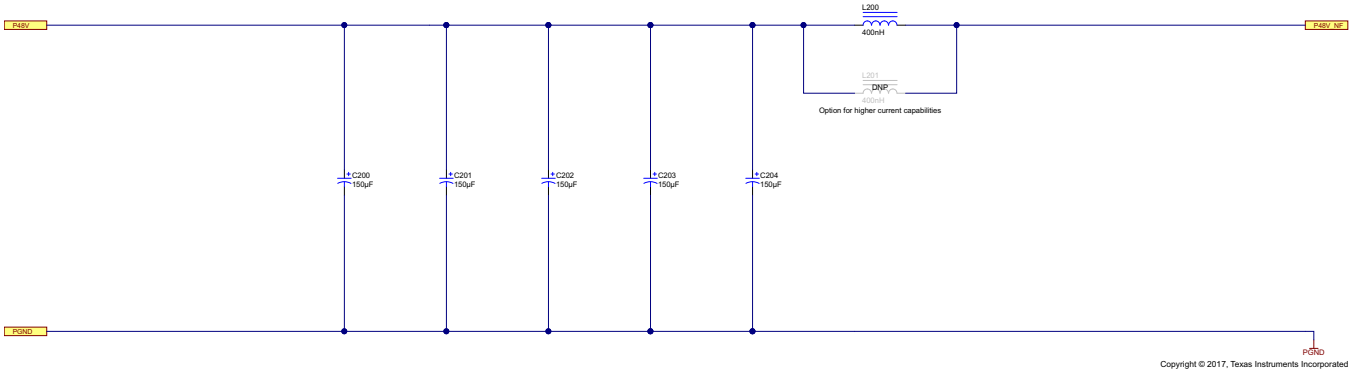


図 16. 48-V Filter Schematic

The L-C filter consists of five aluminum capacitors C200 through C204 and two inductors L200 and L201. High-performance UCZ series capacitors from Nichicon are rated up to 80 V with a capacitance of 150 µF. The ESR for these capacitors is typically 280 mΩ and a ripple current of 700 mA. Power inductors L200 and L201 are from the XAL1060 series from Coilcraft. The type of power inductors used has an 82-A saturation current and a typical DCR of 0.80 mΩ. Inductors L200 and L201 are in parallel to reduce power dissipation and provide flexibility for further optimization during development.

注: Components used in the design are selected and optimized for a DC-DC converter operating with a resistive load in laboratory environment.

The PCB layout of the 48-V filter block in 図 17 does not require any special attention. However, the designer should note the importance of connecting the capacitors to ground with a low impedance path.

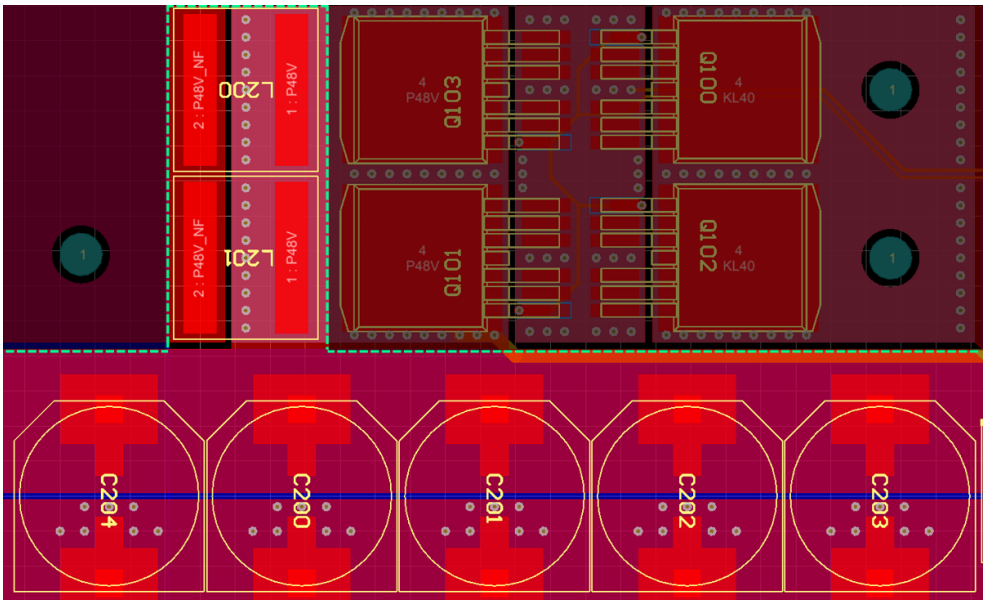


図 17. 48-V Filter PCB Layout

3.2.4 Test Data

Test data for the 48-V block is not available and is a subject for future update.

3.2.5 Further Reading

See the following resources for more information:

1. Texas Instruments, *AN-2162 Simple Success With Conducted EMI From DC-DC Converters*, AN-2162 Application Report (SNVA489)
2. Texas Instruments, *Input Filter Design for Switching Power Supplies*, Application Note (SNVA489)

3.3 Power Stages

3.3.1 Description

As previously described, the power stages use the synchronous buck converter topology as shown in the previous 図 6. All four power stages are identical including the PCB layout. See 表 6 for the system interface overview of a single-phase power stage.

表 6. System Interface for Power Stage

SIGNAL	DIRECTION	DESCRIPTION
P48V_NF_PS*n* (1)	In/Out	48-V car battery system terminal (positive)
PGND_P*n* (1)	In/Out	Power ground (negative)
SW_PS*n* (1)	Out	Switch node
HO_PS*n* (1)	In	High-side transistor gate
LO_PS*n* (1)	In	Low-side transistor gate
CSA_PS*n* (1)	Out	Shunt resistor current sensing - node A
CSB_PS*n* (1)	Out	Shunt resistor current sensing - node B

(1) Where n = 1, 2, 3, 4 represents each individual phase.

表 6. System Interface for Power Stage (continued)

SIGNAL	DIRECTION	DESCRIPTION
P12V_PS*n* (1)	In/Out	Protected 12-V rail (positive)

3.3.2 Considerations

Input and output capacitor selection is affected by the bidirectional functionality. Capacitors swap their function based on the operation mode. Increasing the output capacitance reduces output voltage ripple and output voltage overshoot during a load disconnect event. However, increased output capacitance also has a negative effect on transient response time and system costs. The selection of capacitors starts with choosing the right capacitance and a sufficient ESR to fulfil the design requirements. The selection process is then followed by choosing the other important parameters such as maximum ripple current, temperature range, and voltage rating.

注: Calculating current sharing (for ripple current analysis) between capacitors with different ESR and capacitance in parallel is not trivial. The SPICE circuit simulator is the most convenient tool for the circuit analysis. The same capacitors in parallel can be replaced by a single one. The total output capacitance is directly proportional and ESR is inversely proportional to the number of the same capacitors in parallel.

Finding a proper inductor for energy storage is challenging. The DC current rating must correspond to the maximum output current (BUCK) with some extra margin for the inductor ripple current. The inductor must never saturate. Inductance is selected based on the switching frequency. Smaller inductance inductors in the same package have a typically higher current rating due to a lower DCR, which results in a lower DC power loss. However, lower inductance increases ripple current and output ripple.

MOSFET transistor selection varies based on the system requirements. MOSFET transistors in the power stage negatively contribute to the total power dissipation, thus affecting the total system efficiency. The power dissipation results from conduction and switching losses. High-current MOSFET transistors with a low $R_{DS(ON)}$ minimize conduction losses (I^2R), but typically have greater switching losses due to higher gate charges and parasitics [1]. In an ideal case, the MOSFETs are selected in such a way that the sum of conduction and switching losses is at the minimum. Various methods are available that detail how to select the optimal MOSFETs for a DC-DC converter. See *The J/K Method: A Technique to Select the Optimal MOSFET* for an example using the J-K method.

A snubber circuit may be necessary for damping the parasitic inductances and capacitances on the switch node during switching transitions.

A shunt resistor for current measurement must be rated to withstand the maximum ripple current through the inductor. Note the importance of using a shunt that has very low parasitic inductance and good stability over the whole temperature range. See the section titled *Compensating for the Non-Ideal Current Sense Resistor* in the *LM5170-Q1 Multiphase Bidirectional Current Controller* data sheet [2] to determine how to compensate the parasitic inductance of the shunt resistor.

3.3.3 HW Implementation

図 18 shows a schematic of the power stage (single phase shown).

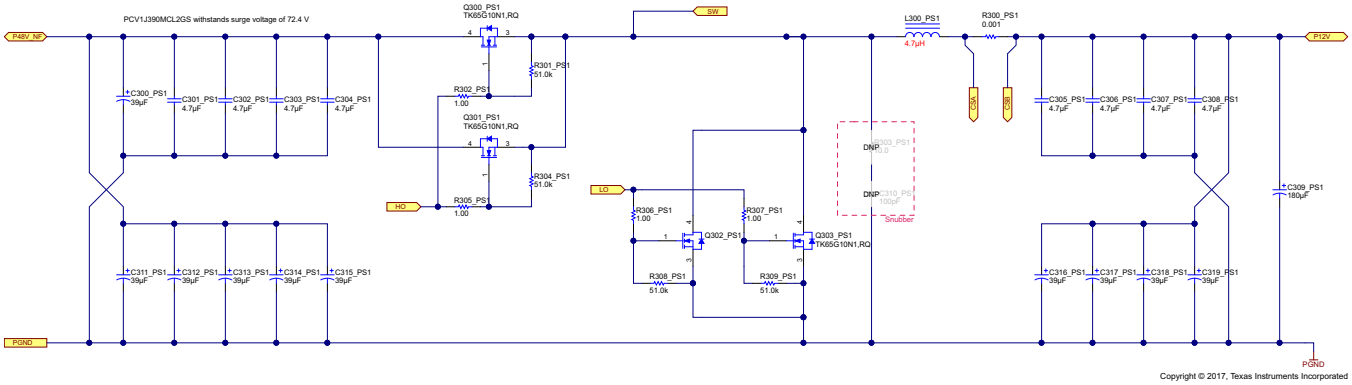


図 18. Power Stage Schematic (One Phase)

The group of small-value ceramic capacitors C301 through C304 on the 48-V side is as close to the switching node as possible. These ceramic capacitors cover small energy but very fast transients. Aluminum capacitors C300 and C311 through C315 handle low-frequency ripple and major output load changes. Capacitor groups C305 through C308, C316 through C319, and C309 serve the same purpose but on the 12-V side. All capacitors are carefully chosen to fulfill the voltage rating, ripple current rating, and temperature range. The group of 39-uF capacitors on the 48-V side are rated only to 63 V; nevertheless, their surge voltage is specified to 72.4 V for one minute, which sufficiently covers short term overvoltage cases. Power MOSFET transistors Q300 through Q303 are identical for both high side and low side. Each switch uses two 100-V rated N-FET transistors with $R_{DS(ON)}$ = 3.8 mΩ (typical) in parallel. Every individual transistor gate has a separate gate resistor R302, R305, R306, or R307. This setup reflects a good engineering practice to mitigate a potential oscillation on the gate caused by a tank circuit formed from stray gate and drain inductances and gate-to-drain (Miller's) capacitance. Gate-to-source resistors R301, R304, R308, and R309 keep the respective transistor closed in case of high-impedance failure on HO and LO gate signals. L300 is a 4.7-µH inductor IHTH-1125KZ-5A (Vishay) with a specified saturation current of 52-A DC. The SER2915L-472KL from Coilcraft or the 7443640470 from Würth Elektronik can alternatively be placed on the board. The automotive-grade current sense resistor R300 is selected for a low inductance < 3 nH and a rated power up to 4 W. The optional snubber circuit R303 and C310 is not used.

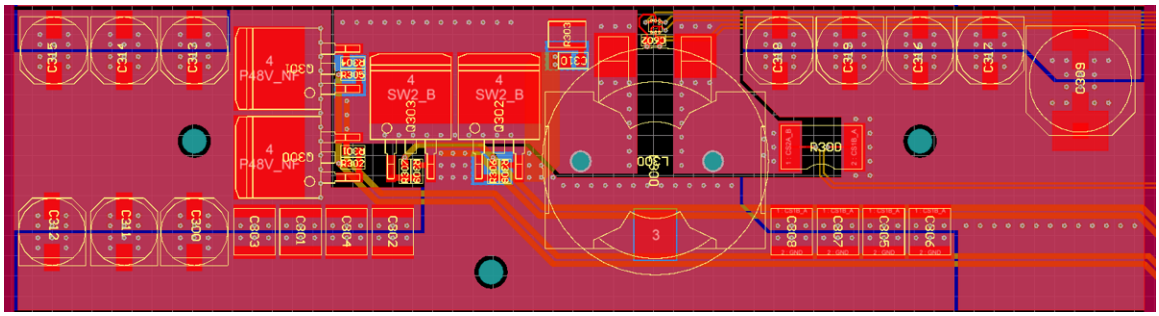


図 19. Power Stage (One Phase) PCB Layout

Various online articles describe PCB layout techniques for a synchronous step-down converter. This PCB layout is a trade-off between performance and single-side component placement for a relatively complex design. The desire is to keep high di/dt current paths as short as possible to reduce electromagnetic interference (EMI). Small capacitors are always the part of the shortest current return path, close to the switch node.

Routing the gate driver signals and current sensing signals to the optimal length is not possible due to the single-side component placement. Gate driver signals use 30-mil wide traces and current sense signals use 10-mil wide traces. These signals are routed differentially to reduce stray inductance as much as possible. An I^2C temperature sensor for each power stage is located in close proximity to the inductor with the digital ground routed separately. High current traces are supported by copper bus bars on the top and bottom side of the PCB.

3.3.4 Test Data

See 6.2 for the test data.

3.3.5 Further Reading

See the following resources for more information:

1. Texas Instruments, *Understanding Buck Power Stages in Switchmode Power Supplies*, Application Report (SLVA057)
2. Texas Instruments, *Understanding Boost Power Stages in Switchmode Power Supplies*, Application Report (SLVA061)
3. Lynch, Brian T.; *Under the Hood of a DC/DC Boost Converter*, Seminar – Topic 3 (http://www.ti.com/download/trng/docs/seminar/Topic_3_Lynch.pdf)
4. Lynch, Brian T.; Hesse, Kurt; *Under the Hood of Low-Voltage DC/DC converters*, Seminar (http://application-notes.digchip.com/001/1-2958.pdf)
5. Powerelectronics.com, Miller, James; *The J/K Method: A Technique to Select the Optimal MOSFET*, Power Electronics Online Article (http://www.powerelectronics.com/dc-dc-converters/jk-method-technique-select-optimal-mosfet)
6. Texas Instruments, Taylor, Robert; Manack, Ryan; *Controlling switch-node ringing in synchronous buck converters*, Power Management Technical Brief (SLYT465)

3.4 12-V Circuit Breaker

3.4.1 Description

The 12-V circuit breaker protects the DC-DC converter against reverse polarity and allows disconnecting the circuitry from the 12-V battery in case of a failure or to prevent current consumption when the system is switched off. The functionality is the same as the 48-V circuit breaker except the 12-V circuit breaker has a reverse polarity protection requirement. See 表 7 for a system interface overview.

表 7. System Interface for 12-V Circuit Breaker

SIGNAL	DIRECTION	DESCRIPTION
KL30_BIAS	Out	Bias voltage rail for pre-boost circuitry
KL30_POL	Out	Polarity detection for the 12-V battery
P12V	In/Out	Protected 12-V rail (positive)
PGND	In/Out	Protected 12-V rail (negative)
EN12	In	Enable signal; voltage greater than 2.0 V enables the circuit breaker; optimized for 3.3-V/ 5-V logic signals
BRKG	In	Gate signal for the circuit breaker MOSFETs
BRKS	In	Source signal for the circuit breaker MOSFETs
KL30	In/Out	12-V car battery system terminal (positive)
KL31	In/Out	12-V car battery system terminal (negative)
KL30_M	Out	12-V battery four-wire voltage measurement terminal (positive)

表 7. System Interface for 12-V Circuit Breaker (continued)

SIGNAL	DIRECTION	DESCRIPTION
KL31_M	Out	12-V battery four-wire voltage measurement terminal (negative)

3.4.2 Considerations

The DC-DC converter is disconnected from both power rails when the system is off. This setup ultimately requires an external impulse to the system to initiate device start-up. This impulse can either be the EN12 or EN48 signal. The circuit breaker on the 12-V side is controlled by the LM5170-Q1 controllers. The controllers do not contain any internal charge pump for the circuit breaker MOSFET transistors. Voltage on the HV-port must be at least 10-V higher than on the LV-port (KL30) to allow these N-MOSFET transistors to operate in the linear (ohmic) region as a switch. A back-to-back configuration of very low $R_{DS(ON)}$ MOSFET transistors must be used similarly to the 48-V circuit breaker. A simple pre-boost circuit is connected to the 12-V battery terminal (KL31) to bypass the 12-V circuit breaker and enable DC-DC start-up from the 12-V side.

Per industry expectations, the 12-V battery in a vehicle is user accessible. For this reason, a reverse polarity condition may occur. The system must detect this condition and force the 12-V circuit breaker off in case this situation arises. Opening the 12-V circuit breaker during a reverse polarity condition results in excessive current flowing through the substrate diode of the low MOSFET and the inductor in the power stage, which causes immediate damage of the system.

The protected side of the 12-V circuit breaker is used as a reference point for the voltage measurement circuitry.

3.4.3 HW Implementation

図 20 shows a schematic of the 12-V circuit breaker.

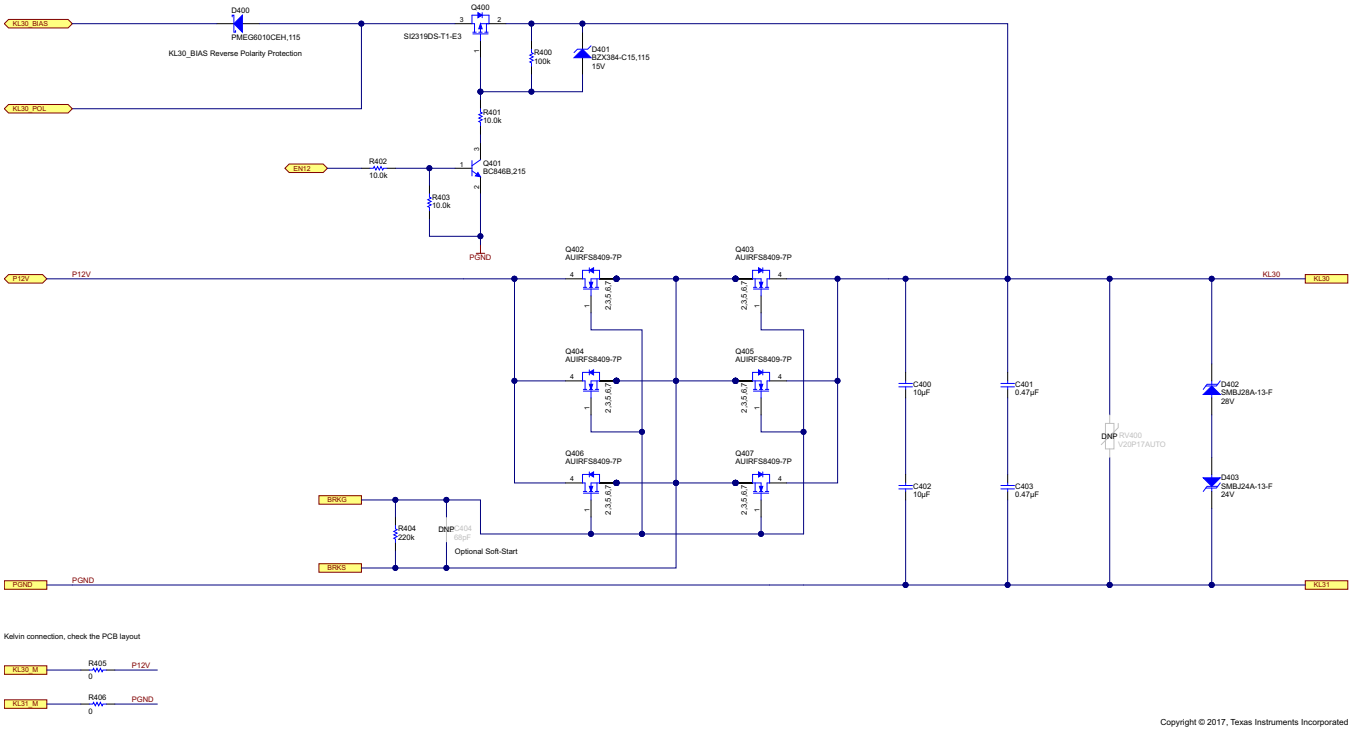


図 20. 12-V Circuit Breaker Schematic

The circuit breaker uses back-to-back configuration of N-MOSFET transistors Q402 through Q406 in parallel. Resistor R404 prevents opening transistors in the case of high impedance on the BRKG and BRKS signals. C404 is an optional soft-start capacitor. Capacitors C400 through C403 and TVS diodes D402 and D403 form a basic input transient protection. RV400 is a placeholder for an optional metal oxide varistor (MOV), which is used for further transient suppression.

A P-MOSFET transistor Q400 is used for bypassing the 12-V circuit breaker for the pre-boost circuit. Current for the pre-boost circuit is relatively low, so a cheap P-MOSFET transistor is sufficient. Resistor R400 helps to close Q400. Diode D401 protects the gate-source junction of Q400 against excessive V_{GS} voltage. Resistors R402 and R403 set bias for a transistor-based inverter Q401. Resistor R401 limits current when the Zener diode D401 starts opening due to short term overvoltage. Diode D400 is a reverse polarity protection for the pre-boost circuitry. Voltage drop on D400 is negligible and only applies when the pre-boost operates during system start-up from the 12-V battery. The node between D400 and Q400 is used by the diagnostic block for reverse polarity detection on the 12-V side.

Resistors R109 and R110 allow disconnecting the voltage measurement circuitry from the measurement points during development and testing.

図 21 shows a PCB layout of the 12-V circuit breaker. The input transient protection PCB layout is similar to that of the 48-V circuit breaker. The bypass circuitry is in close proximity to the pre-boost converter. High current traces are supported by copper bus bars on the top side and bottom side of the PCB.

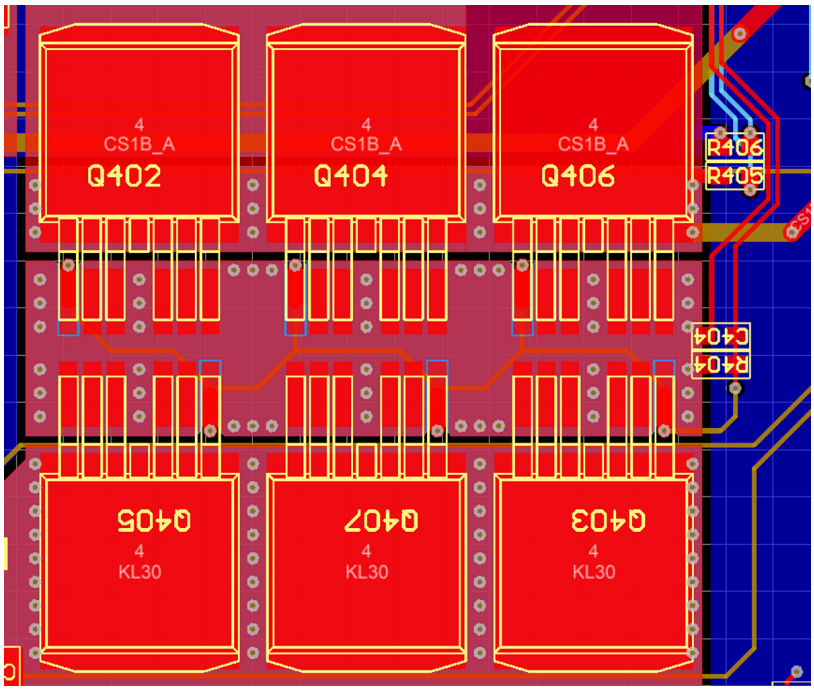


図 21. 12-V Circuit Breaker PCB Layout

3.4.4 Test Data

See 6.3 for test data.

3.5 LM5170-Q1 Subsystem

3.5.1 Description

The system uses two LM5170-Q1 subsystems for a current feedback loop: subsystem A or _LM1, subsystem B or _LM2. See the LM5170-Q1 data sheet [2] for a detailed theory of operation of the LM5170-Q1. 表 8 shows the system interface for both LM5170-Q1 subsystems.

注: The PCB layout and the netlist for both LM5170-Q1 subsystems are identical. Signals SYNCIN and SYNCOUT are used for synchronization.

表 8. System Interface for LM5170-Q1 Subsystem

SIGNAL	DIRECTION	DESCRIPTION
P10V_LM*n*	In	+10-V bias supply for LM5170-Q1
AGND_LM*n*	—	Common analog ground
SYNCOUT_LM*n*	Out	Clock synchronization (output)
ISETD_LM*n*	In	Current programming (PWM with variable duty cycle: 3.3-V logic)
VIN_LM*n*	In	HV-port (P48V) voltage (positive)
UVLO_LM*n*	In	Master enable
EN1_LM*n*	In	Channel 1 enable
DIR_LM*n*	In	Direction command (buck/boost)
SYNCIN_LM*n*	In	Clock synchronization (input)

表 8. System Interface for LM5170-Q1 Subsystem (continued)

SIGNAL	DIRECTION	DESCRIPTION
OPT_LM*n*	In	Multiphase configuration (sets phase lag of the SYNCOUT)
EN2_LM*n*	In	Channel 2 enable
NFAULT_LM*n*	In/Out	Fault flag (internal pullup to 5 V)
IOUT1_LM*n*	Out	Channel 1 current monitor output
IOUT2_LM*n*	Out	Channel 2 current monitor output
BRKS_LM*n*	Out	12-V circuit breaker common SOURCE pin
BRKG_LM*n*	Out	12-V circuit breaker common GATE pin
CS1A_LM*n*	In	Current sensing channel 1 – node A
CS1B_LM*n*	In	Current sensing channel 1 – node B
SW1_LM*n*	In	Switch node channel 1
SW2_LM*n*	In	Switch node channel 2
CS2A_LM*n*	In	Current sensing channel 2 – node A
CS2B_LM*n*	In	Current sensing channel 2 – node B
HO1_LM*n*	Out	High-side transistor gate – channel 1
LO1_LM*n*	Out	Low-side transistor gate – channel 1
HO2_LM*n*	Out	High-side transistor gate – channel 2
LO2_LM*n*	Out	Low-side transistor gate – channel 2
where n = 1,2 represents each individual subsystem		

3.5.2 Considerations

Consider the following when selecting a controller for a 12-V/48-V automotive bidirectional DC-DC converter:

- Isolated or non-isolated topology
- Bidirectional operation
- Multiphase operation and synchronization
- Current sharing between phases
- Design scalability
- Digital, analog, or hybrid control loop
- Interfacing with the host microcontroller or system
- Protection mechanisms
- Level of integration and automotive qualification

The LM5170-Q1 is the most straightforward and highly-integrated solution for the 12-V/48-V non-isolated bidirectional DC-DC converter.

3.5.3 HW Implementation

図 22 shows a schematic of the first LM5170-Q1 subsystem.

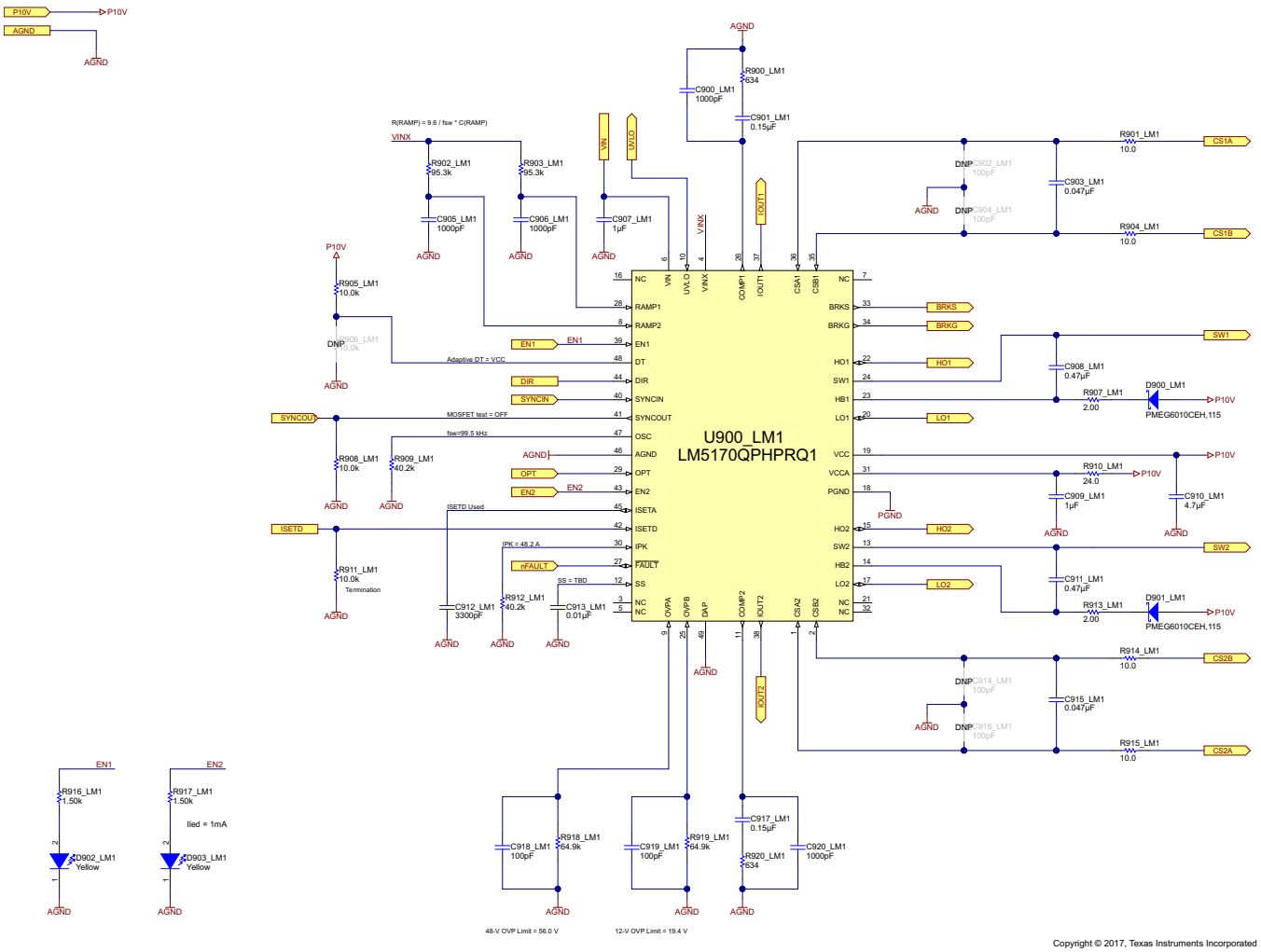


図 22. LM5170-Q1 Subsystem Schematic (Subsystem 1)

RC circuits R902, R903 and C905, and C906 are a part of the ramp generator. C907 is a bypass capacitor for the HV-input pin, which is rated up to 100 V. C910 is a bypass capacitor for the bias supply. The analog bias supply 10 V is decoupled by the RC filter R910, C909. Component groups C900, C901, R900 and C917, C920, and R920 are current-loop compensation networks for each channel, respectively. Resistors R918 and R918 set the overvoltage protection voltage threshold for the OVPA and OVPB pins. Small 100-pF capacitors C918 and C919 reduce the noise on the pins. A 10-k pulldown resistor R908 on the SYNCOUT pin disables the internal MOSFET fault check circuitry.

注: The MOSFET fault check is disabled due to high capacitance on P48V and P12V. Enabling this functionality may cause false fault reporting during LM5170-Q1 start-up.

Resistor R909 sets the switching frequency to approximately 100 kHz. The ISETD pin is used for current regulation. Pulldown resistor R911 defines the ISETD logic level when the output pins of the MCU are in a high-z state (reset). Capacitor C912 on the ISETA pin forms a low-pass filter, which converts the PWM signal from the ISETD pin to an analog voltage proportional to the duty cycle. Proper selection of this capacitor depends on the PWM for the ISETD pin and is critical for voltage loop stability. A higher capacitance adds delay to the control loop. A smaller capacitance increases voltage ripple on the ISETA pin due to a higher cutoff frequency of the RC filter.

A 10-k pullup resistor R905 sets the internal adaptive dead-time control between the high-side and low-side driver. Resistor R906 is a placeholder for the fixed dead-time settings. Resistor R912 programs the threshold for the cycle-by-cycle current limit comparator. Capacitor C913 defines soft-start time.

Component groups R901, R904, C903, C902, C904 and R914, R915, C915, C914, and C916 compensate parasitic inductance of the sense resistor. Components C908, R907, D900 and R911, R913, and R901 are bootstrap circuits for high-side MOSFET drivers.

Channel activity is visualized by LEDs D902 and D903 connected to EN1 and EN2 signals. Resistors R916 and R917 set the current through the LEDs to approximately 1 mA.

注: Always refer to the latest revision of a data sheet for proper component selection. The LM5170-Q1 data sheet contains detailed design procedure beginning in the section titled *Design Requirements* [2].

図 23 shows a PCB layout of the LM5170-Q1 subsystem. All components are placed in close proximity to the LM5170-Q1 on the top side of the PCB. The thermal pad is a reference point where analog and power ground meet.

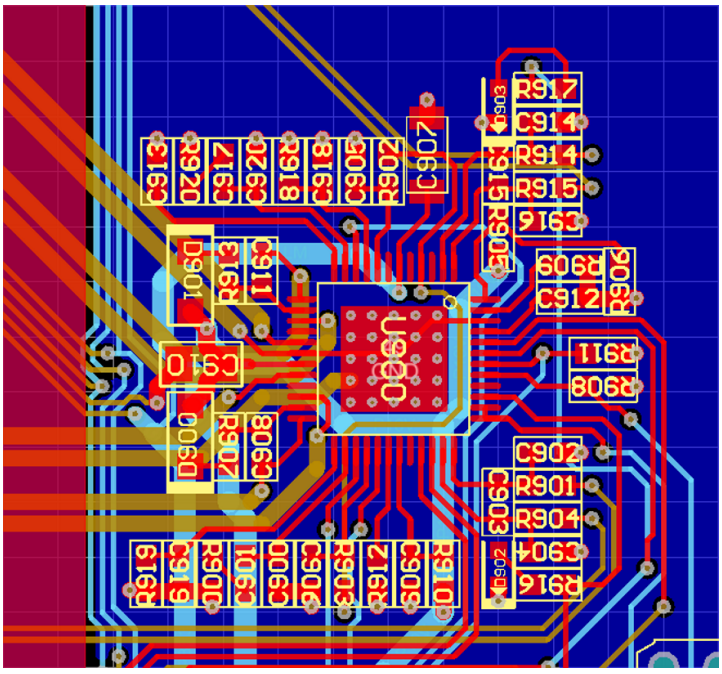


図 23. LM5170-Q1 Subsystem PCB Layout

3.5.4 Test Data

See 6.4 for the test data.

3.5.5 Further Reading

See the following resources for more information:

1. Texas Instruments, *Interconnecting automotive 48V and 12V rails in dual-battery systems*, TI E2E™ Online Community Forum – Behind the Wheel; March 2017 (https://e2e.ti.com/blogs_/b/behind_the_wheel/archive/2017/03/20/how-to-connect-dual-automotive-battery-systems-)
2. Texas Instruments, *Selecting a bidirectional converter control scheme*, TI E2E™ Online Community Forum – Power House; March 2017 (https://e2e.ti.com/blogs_/b/powerhouse/archive/2017/03/20/select-a-bidirectional-converter-control-scheme)

3.6 C2000™ MCU

3.6.1 Description

The C2000 MCU block, based on TMS320F28027F, is responsible for the outer voltage feedback loop, interfacing with LM5170-Q1 devices, and communication with the host system when applicable. See 表 9 for a system interface overview of the C2000 MCU block.

表 9. System Interface for C2000™ Control MCU

SIGNAL	DIRECTION	DESCRIPTION
P3V3	In	+3.3-V bias supply
KL30_M	In	12-V battery four-wire voltage measurement terminal (positive)
KL31_M	In	12-V battery four-wire voltage measurement terminal (negative)
KL41_M	In	48-V battery four-wire voltage measurement terminal (positive)
KL40_M	In	48-V battery four-wire voltage measurement terminal (negative)
ADCINA6	In/Out	General purpose analog input or digital input/output
ADCINA7	In/Out	General purpose analog input
ADCINB1	In/Out	General purpose analog input
ADCINB2	In/Out	General purpose analog input or digital input/output
ADCINB3	In/Out	General purpose analog input
ADCINB4	In/Out	General purpose analog input or digital input/output
ADCINB6	In/Out	General purpose analog input or digital input/output
SIMO	In/Out	SPI slave in, master out (unused)
SOMI	In/Out	SPI slave in, master out (unused)
CLK	In/Out	SPI clock (unused)
STEA	In/Out	SPI chip select (unused)
TXD	Out	Serial Communications Interface (SCI) transmit
RXD	In	Serial Communications Interface (SCI) receive
EN1_A	Out	Power Stage 1 Enable (LM5170-Q1 subsystem A, EN1)
EN2_A	Out	Power Stage 2 Enable (LM5170-Q1 subsystem A, EN2)
EN1_B	Out	Power Stage 3 Enable (LM5170-Q1 subsystem B, EN1)
EN2_B	Out	Power Stage 4 Enable (LM5170-Q1 subsystem B, EN2)
OPT	Out	Multiphase configuration (sets phase lag of the SYNCOUT)
DIR	Out	Direction command (buck/boost)
ISETD	Out	Current programming (PWM with variable duty cycle: 3.3-V logic)
IMON	In	Sum of phase-current monitor currents from both LM5170-Q1 subsystems
nFAULT	In	LM5170-Q1 subsystem fault detection monitor
SDA	In/Out	I^2C bus data

表 9. System Interface for C2000™ Control MCU (continued)

SIGNAL	DIRECTION	DESCRIPTION
SCL	Out	I^2C bus clock
nRST	In	Microcontroller reset
UVLO	In/Out	UVLO monitoring and open-collector output
WDT_TRIG	Out	External watchdog timer trigger
GND	—	Common ground

3.6.2 Considerations

MCU selection for this hybrid DC-DC converter, which combines the analog circuitry of LM5170-Q1 and the digital control for the outer voltage feedback loop, depends on several factors. In general, the batteries on 12-V and 48-V rails represent large energy storage with low internal resistance. These battery qualities free the external voltage loop from the requirement to handle ultra-fast transients known from other multi-phase converters (processor power, for example). This configuration reduces the demand on MCU computing and peripherals performance. In theory, the lowest-cost MCU with a PWM for the ISETD pin and ADC periphery for voltage measurements can be used for a digital voltage feedback loop as long as the transient response is sufficient for the given system requirements. The transient response of the system corresponds to the refresh-rate of the PWM for the ISETD pin. During this period the MCU must sample voltages on the ADC pins and calculate the new PWM duty cycle.

A difference amplifier is used for four-wire voltage measurements. This solution improves load regulation. The operational amplifier must be capable of input and output rail-to-rail operation resulting from sensing close to ground, single-supply, and interfacing with the unipolar-input ADC. The voltage control loop does not require any current measurement. Current monitoring in TIDA-01168 is used only for approximate indication. An operational amplifier configured as a current-to-voltage converter is recommended whenever more precise current measurements are required.

3.6.3 HW Implementation

図 24 shows a schematic of the C2000™ Control MCU.

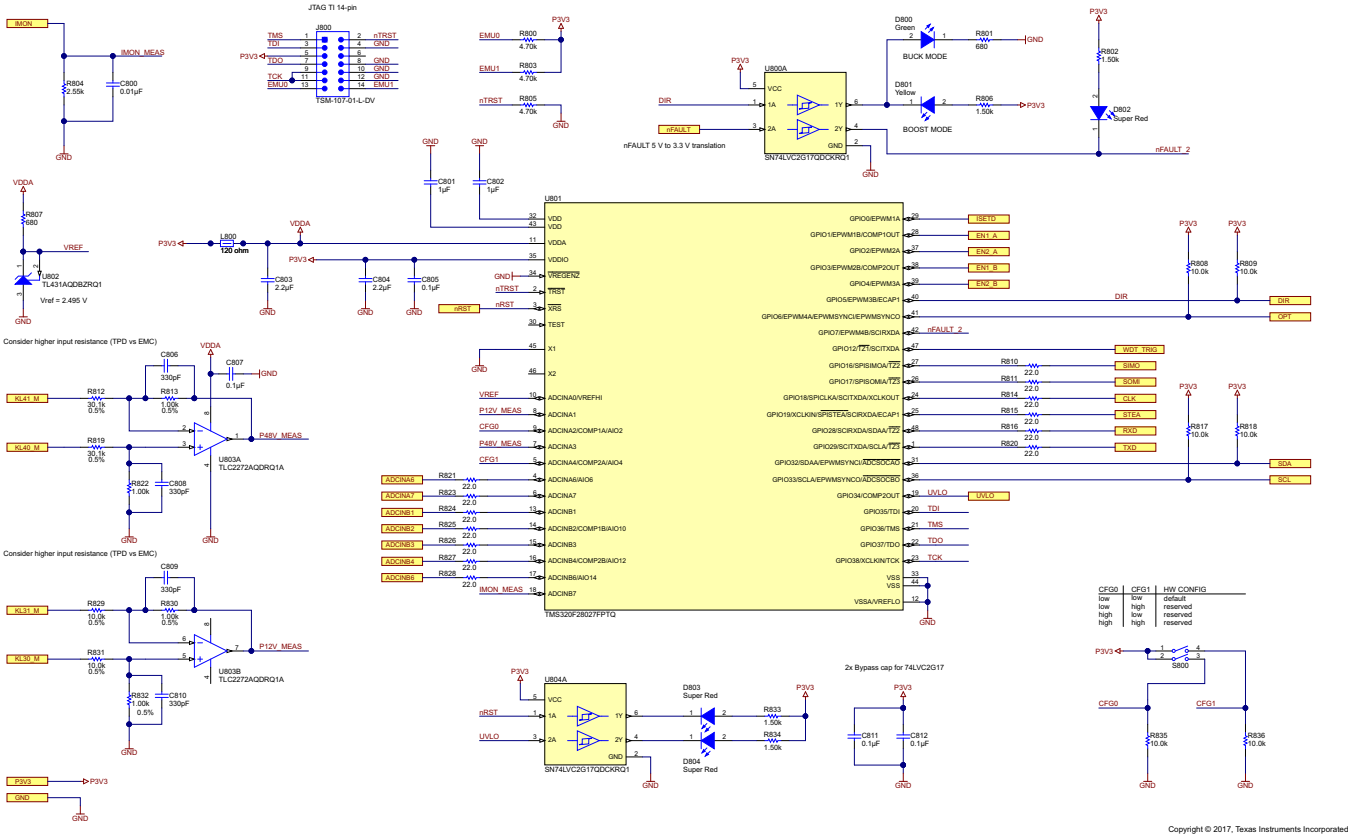


図 24. C2000™ Control MCU Schematic

The LM5170-Q1 current monitors have a current source output proportional to the current through the inductor of each respective channel. All monitor outputs are conceded together, thus the IMON signal represents the sum of currents through all phases. Resistor R804 in parallel with capacitor C800 is a simple current-to-voltage converter with a low-pass filter. The output is connected directly to the ADC. Voltage measurement is based on a dual operational amplifier U803. The operational amplifier is configured as a difference amplifier. Resistors R812, R813, R819, R822 and R829, R830, R831, and R832 set the gain for each channel. Resistors R812 and R819 must be rated up to 100 V in this application, which requires sensing up to 70 V. Capacitors C806 and C808 through C8010 set the cutoff frequency of the low-pass filter. Using the same capacitance of these capacitors is important. Any asymmetry affects the common-mode rejection ratio. Output of the operational amplifier goes directly to the ADC.

注: TI recommends to place an RC circuit between the output of the operational amplifier and the input of the ADC. This circuit improves the load response of the operational amplifier. The recommenced values are a 1-Ω to 20-Ω resistor and 10-100 pF capacitor.

The TL431-Q1 shunt regulator U802 and biasing resistor R807 provide a stable reference voltage for the ADC. Lossy ferrite bead L800 and the capacitor C803 isolate the analog power supply from the digital power supply rail. Capacitors C801 through C805 are bypassing capacitors for digital power pins and internal voltage regulators of the MCU.

The TMS320F28027F MCU is the smallest member from the C2000 real-time control MCU family. The microcontroller uses the internal 10-MHz oscillator as a clock source.

The 14-pin header connector J800 and resistors R800, R803, and R805 are required for the XDS100-compatible Joint Test Action Group (JTAG) interface. Logic gates U800 and U804 with bypass capacitors C811 and C812 drive LEDs D800 through D804. U800A does logic-level translation for the NFAULT signal from the LM5170-Q1. Resistors R801, R802, R806, R833, and R834 set the current through the LEDs to approximately 1 mA. The group of 22-Ω resistors is for the MCU interface. One common habit is to place a 22-Ω series termination for signals interfaced outside the PCB board. Resistors R808 and R809 are DIR and OPT signal pullup resistors for the LM5170-Q1. Resistors R817 and R818 are pullup resistors for the I^2C bus. The exact value of I^2C pullup resistors depends on the clock speed, number of devices connected on the bus (parasitic capacitance), and bus length. I^2C temperature sensors are located in the power stage areas. High currents resulting in strong magnetic fields couple a lot of impulse noise to I^2C signals. When debugging I^2C communication, this noise must be taken into account and active operation when all four phases are enabled is recommended.

Switch S800 and resistors R835 and R36 are reserved for firmware configuration. The current firmware v1.0 does not support this feature.

The PCB layout of the C2000 control MCU block does not have any special requirements except for the analog circuitry. See 図 25 for the PCB layout.

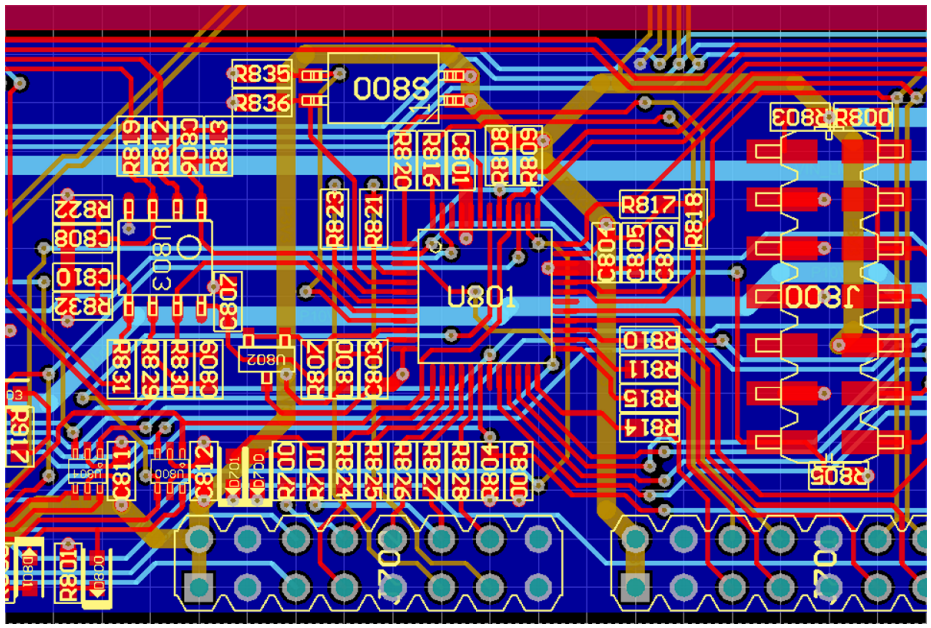


図 25. C2000™ Control MCU PCB Layout

3.6.4 Test Data

See 6.4 for the test data.

3.6.5 Further Reading

See the following resources for more information:

1. Texas Instruments, *C2000™ Real-Time Microcontrollers*, C2000 MCU Brochure (SPRB176AD)

3.7 Diagnostics

3.7.1 Description

The diagnostic block in TIDA-01168 monitors phase temperatures, MCU activity, reverse polarity condition on the 12-V rail, and bias voltages for the MCU and LM5170-Q1 subsystems. See 表 10 for a system interface overview of the diagnostic block.

表 10. System Interface for Diagnostic Block

SIGNAL	DIRECTION	DESCRIPTION
P3V3	In	+3.3-V bias supply
GND	—	Common ground
SDA	In/Out	I^2C bus data
SCL	In	I^2C bus clock
KL30_POL	In	Polarity detection for the 12-V battery
nRST	Out	MCU reset
nSHDN	Out	Emergency shutdown for LM5170-Q1s
WDT_TRIG	In	External watchdog timer trigger

3.7.2 Considerations

A basic set of diagnostic features and bias supply failure detection are beneficial even in a design intended for laboratory use. Temperature sensors monitor each power phase and react to overtemperature events independently of the control MCU. External reset circuitry with a watchdog timer is often used in systems controlled by an MCU. In the event that the MCU does not react (locks up), for example, due to a software bug or a control flow error, the watchdog timer shuts down the complete system and keeps it in a safe state. An integrated watchdog timer in the MCU can also be used if the provided level of robustness is sufficient. External watchdog circuit ICs are usually combined with voltage supervisor functionality, which make them a very robust solution. Systems with ASIL requirements often use a system basis chip (SBC). The SBC integrates even more functionality in a single chip, for example low-dropout regulators (LDOs), voltage supervisors, CAN and LIN interfaces, or wake-up signals.

Monitoring bias voltages for the MCU and LM5170-Q1 subsystems is important to ensure that all integrated circuits operate only within the specified operating voltage range. Operating within the specified operating range is important, especially during system start-up when all devices should be kept in reset or standby mode until the bias voltages reach the preset value.

3.7.3 HW Implementation

図 26 shows a schematic of the diagnostics.

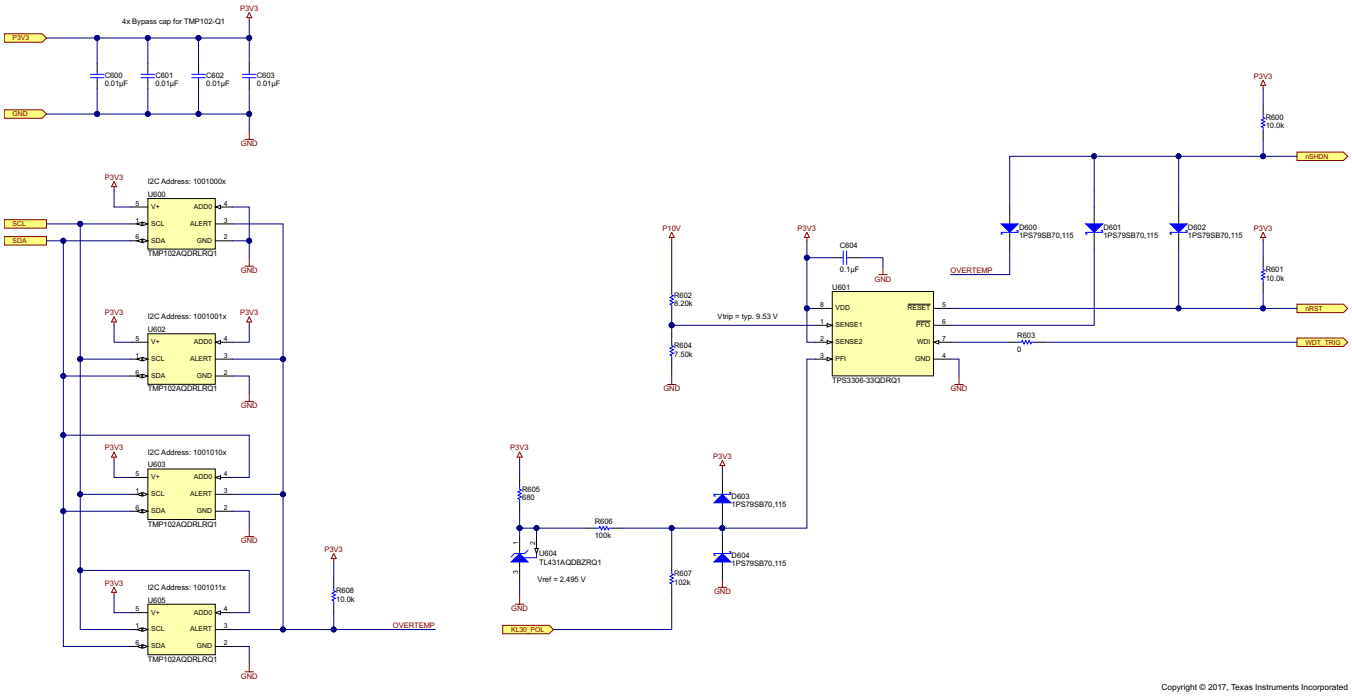


図 26. Diagnostics Schematic

U600, U602, U603, and U605 are TMP102-Q1 temperature sensors interfaced over an I^{2}C bus. The biggest benefit of these senors is the ALERT open-collector output. The temperature sensor allows the designer to set a custom overtemperature threshold in the way that the ALERT output is set low when temperature reaches the threshold. All ALERT outputs are connected together to the OVERTEMP signal. Resistor R608 is a pullup resistor and does not have a critical value. Capacitors C600 through C603 are bypass capacitors for TMP102-Q1 temperature sensors. The external watchdog and voltage supervisor U601 is TPS3306-33, which monitors 3.3-V and 10-V power supplies for the MCU and LM5170-Q1 devices (see 図 27). Resistor dividers R602 and R604 set the undervoltage threshold for the 10-V power rail. Capacitor C604 is a bypass capacitor.

A special circuitry checks the reverse polarity condition on the 12-V battery terminal (KL31). Shunt regulator U604 along with resistor R605 provide a stable nominal voltage of 2.495 V. Resistors R606 and R607 are a resistor divider. The power fail input (PFI) of U601 senses the output of the divider. If the voltage on KL30_POL is slightly negative, the voltage on the PFI is below the threshold and the power fail output (PFO) signal is low. The PFO signal, overtemperature, and reset signal are logically connected together by diodes D600 through D602. Diodes D603 and D604 protect the PFI input. If any of the signals are low, the emergency shutdown signal nSHDN switches off the LM5170-Q1 devices. The emergency shutdown also immediately disconnects the 12-V circuit breaker or prevents turning it on during a reverse polarity condition in the 12-V battery terminal. Removing the resistor R603 allows disabling the watchdog timer during development and MCU programming.

The PCB layout of the diag block is fairly simple. The I^{2}C temperature sensors are located in the power section. Wiring separate power for the sensors is important. Do not ground the sensors locally to the power ground. See 図 28 for further details.

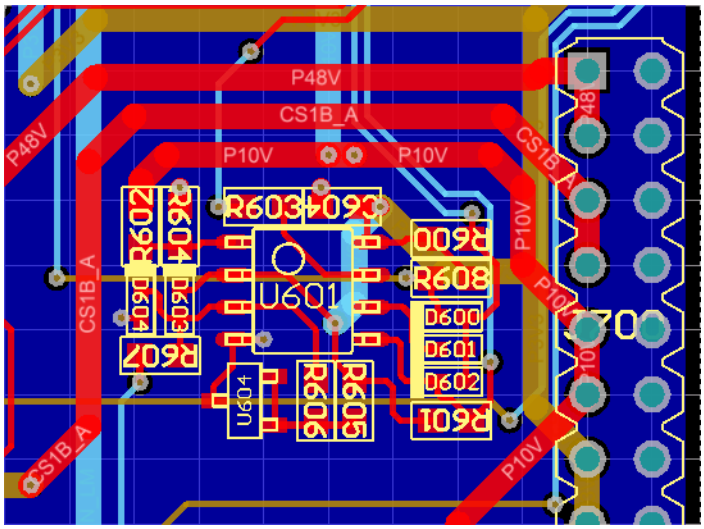


図 27. Diag PCB Layout—External Watchdog and Voltage Supervisor

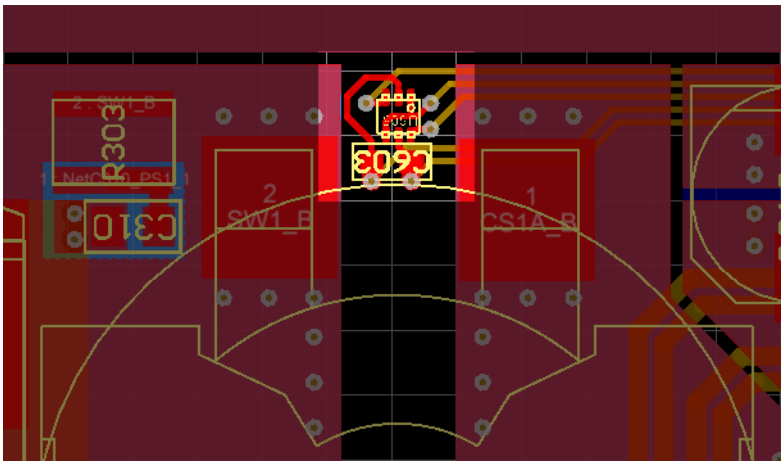


図 28. Diag PCB Layout—TMP102-Q1 Temperature Sensor in Power Stage

3.7.4 Test Data

See 6.6 for the test data.

3.7.5 Further Reading

See the following resources for more information:

1. Texas Instruments, *Understanding the I²C Bus*, Application Report (SLVA704)

3.8 Bias Supplies

3.8.1 Description

Bias supplies provide stable power to other subsystems (blocks). See 表 11 for a system interface overview of the bias supplies block.

表 11. System Interface for Power Stage

SIGNAL	DIRECTION	DESCRIPTION
P48V	In	Protected 48-V rail (positive – filtered)
KL30_BIAS	In	Bias voltage rail for the pre-boost circuitry
PGND	—	Protected 48-V rail (negative)
VIN_LM	Out	HV-port bias voltage for LM51710-Q1s; can be either P48V or the output from the pre-boost circuit
P10V	Out	10-V bias voltage
P3V3	Out	3.3-V bias voltage

3.8.2 Considerations

As previously discussed, a pre-boost circuit for the LM5170-Q1 devices is required to open the 12-V circuit breaker when the system starts from the 12-V battery. The pre-boost circuit only works under this special condition; therefore, cost optimization is preferred over performance and efficiency. A standard non-isolated boost converter with hysteretic control fulfills these requirements. When the output voltage of the pre-boost circuit is slightly lower than nominal voltage on the 48-V rail the hysteretic control automatically switches off the boost converter. This behavior eliminates the requirement for a special control circuitry. The EN12 signal can be set low during normal operation to disconnect the pre-boost circuit completely and further reduce its standby current consumption.

A wide V_{IN} step-down DC-DC converter generates the 10-V bias supply for the LM5170-Q1 devices. The wide input voltage range on the P48V rail must be considered. A second step-down converter generates a 3.3-V bias voltage from the 10-V output to operate with a reasonable duty cycle. An optional linear post-regulator connected to the output of the 3.3-V converter reduces switching noise and output ripple. In this case, the output voltage of the DC-DC converter must be set a little higher to maintain the minimally-required voltage drop on the voltage regulator.

3.8.3 HW Implementation

図 29 shows a schematic of the bias supplies.

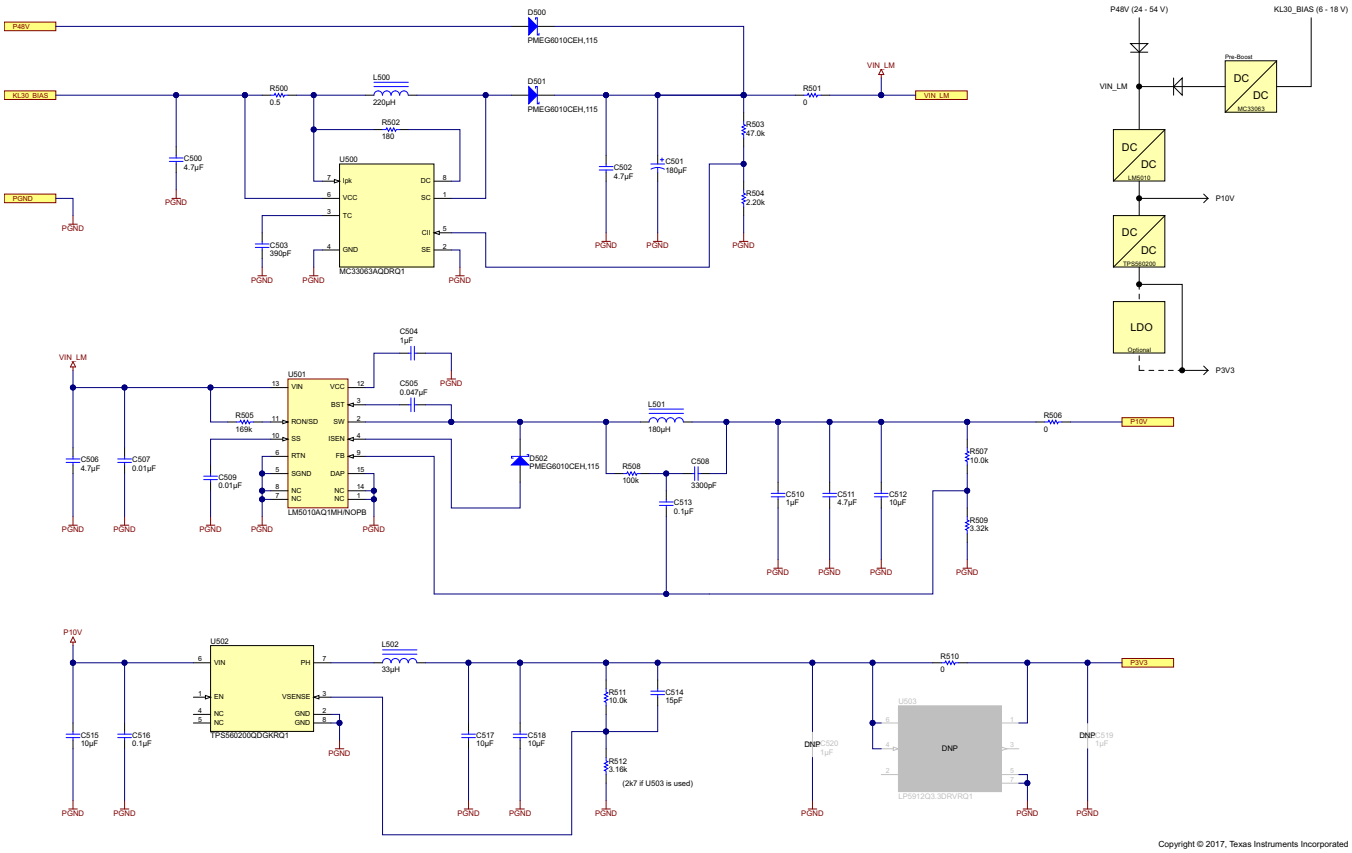


図 29. Bias Supplies Schematic

The pre-boost converter U500 is a very low-cost MC33063A-Q1 switching regulator operating as a boost converter. Capacitors C500, C501, C502, inductor L500, and diode D501 are a part of the boost topology. Resistor R500 sets the current limit. Capacitor C503 is a timing capacitor for U500. Resistor divider R503 and R504 sets the output voltage to 28 V, which is below the normal operating range for the 48-V system (see 図 5) but already high enough for the LM5170-Q1 devices to control the 12-V circuit breaker. D500 is a diode-OR for the 48-V rail. When voltage on P48V reaches approximately 28 V + $V_{f(D500)}$, then U500 stops switching.

U501 is the LM5010A-Q1 step-down switching regulator for a 10-V rail. Capacitors C506, C507, C5010, C511, C512, diode D502, and inductor L501 are a part of the buck topology. Capacitor C509 is a soft-start timing capacitor. Turn-on (T_{ON}) timing resistor R505 is set to operate the DC-DC converter in constant conduction mode. C505 is a bootstrap capacitor for the internal MOSFET driver. Capacitor C504 stabilizes the output of the internal 7-V bias voltage regulator. Feedback resistor divider R507 and R509 sets the output voltage to 10 V. The LM5010A-Q1 requires a minimum 25 mV of ripple voltage at the FB pin for stable fixed-frequency operation. TIDA-01168 uses resistor R508 and capacitors C508 and C513 as a ripple injection circuit. See the LM5010A-Q1 Data Sheet for further information [4].

The step-down DC-DC converter for the 3.3-V voltage rail is based on the TPS560200-Q1 (U502). This synchronous regulator with integrated MOSFETs requires minimum external components. Capacitors C515 through C518 and inductor L502 are a part of the buck topology. Resistor divider R511 and R512 sets the output voltage to 3.3 V. Capacitor C514 is a feed-forward capacitor which adds a zero and a pole to the control loop, which improves the phase margin and bandwidth when properly selected.

U503 is a placeholder for the LP5912 linear regulator. This regulator is selected for its very good power supply rejection ratio (PSSR) and competitive price.

Jumpers R501, R506, and R510 allow load disconnect for development.

図 31 shows the LM5010-Q1 and TPS560200-Q1 step-down converters and 図 30 shows the pre-boost converter PCB layouts. The general rules for single-side component placement are applied. Current paths with high di/dt transients are as short as possible. The thermal pad of U501 and U502 is the local reference point connected to the ground plane.

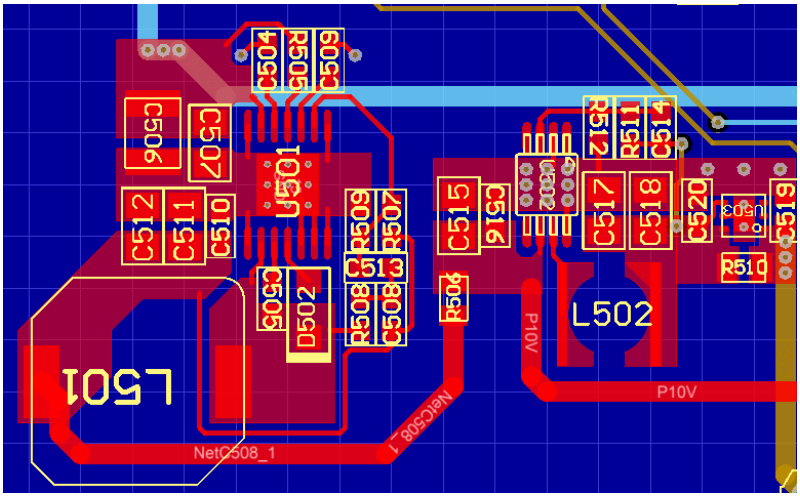


図 30. Bias Supplies PCB Layout—LM5010-Q1 and TPS560200-Q1 Step-Down Converters

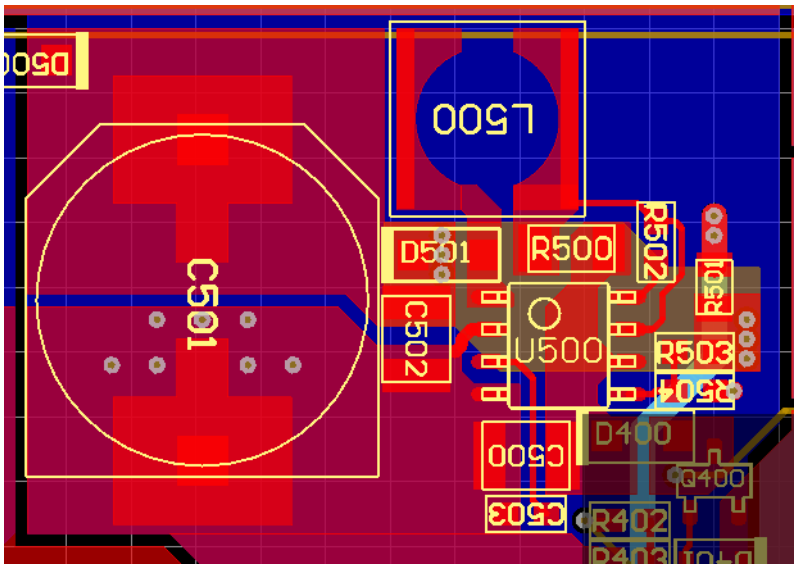


図 31. Bias Supplies PCB Layout—MC33063A-Q1 Pre-Boost Converter

3.8.4 Test Data

See 6.7 for the test data.

3.8.5 Further Reading

See the following resources for more information:

1. Texas Instruments, *Application of the MC34063 Switching Regulator*, MC34063 Application Report (SLVA252)
2. Texas Instruments, *Transient Response versus Ripple – An Analysis of Ripple Injection Techniques Used in Hysteretic Controllers*, Application Report (SLVA653)
3. ElectronicDesign.com, Glaser, Chris; *Does Inductor Ripple-Current Percentage Still Matter in Low-Power Step-Down Converters?*, Electronic Design Article, November 2015 (www.electronicdesign.com/power/does-inductor-ripple-current-percentage-still-matter-low-power-step-down-converters)

3.9 System Interface

3.9.1 Description

The system interface is a set of connectors that allow interfacing with a host system. See 表 12 for a system interface overview of the system interface block.

表 12. System Interface for System Interface

SIGNAL	DIRECTION	DESCRIPTION
P48V	Out	Protected 48-V rail (positive)
P12V	Out	Protected 12-V rail (positive)
P10V	Out	+10-V bias supply
P3V3	Out	+3.3-V bias supply
SDA	In/Out	I^2C bus data
SCL	Out	I^2C bus clock
EN48	In	Enable signal; voltage greater than 2.0 V enables the 48-V circuit breaker; voltage on this pin not to exceed 65 V
EN12	In	Enable signal; voltage greater than 2.0 V enables the 12-V circuit breaker; optimized for 3.3-V or 5-V logic signals
ADCINA6	In/Out	General purpose analog input or digital input or output
ADCINA7	In/Out	General purpose analog input
ADCINB1	In/Out	General purpose analog input
ADCINB2	In/Out	General purpose analog input or digital input or output
ADCINB3	In/Out	General purpose analog input
ADCINB4	In/Out	General purpose analog input or digital input or output
ADCINB6	In/Out	General purpose analog input or digital input or output
SIMO	In/Out	SPI slave in, master out (unused)
SOMI	In/Out	SPI slave in, master out (unused)
CLK	In/Out	SPI clock (unused)
STEA	In/Out	SPI chip select (unused)
TXD	Out	Serial communications interface (SCI) transmit
RXD	In	Serial communications interface (SCI) receive
GND	—	Common ground

3.9.2 Considerations

The system interface allows connection to various host systems. The following signals are considered to be important:

- EN12 and EN48 enable signals for the 12-V and 48-V circuit breaker
- P48V, P12V, P10V, and P3V3 bias voltages for additional circuitry, if required
- I^2C, SPI, and serial interface signals
- Multiple GPIOs and analog inputs (reserve) with two additional LEDs for system debugging and status interfacing

3.9.3 HW Implementation

図 29 shows a schematic of the system interface.

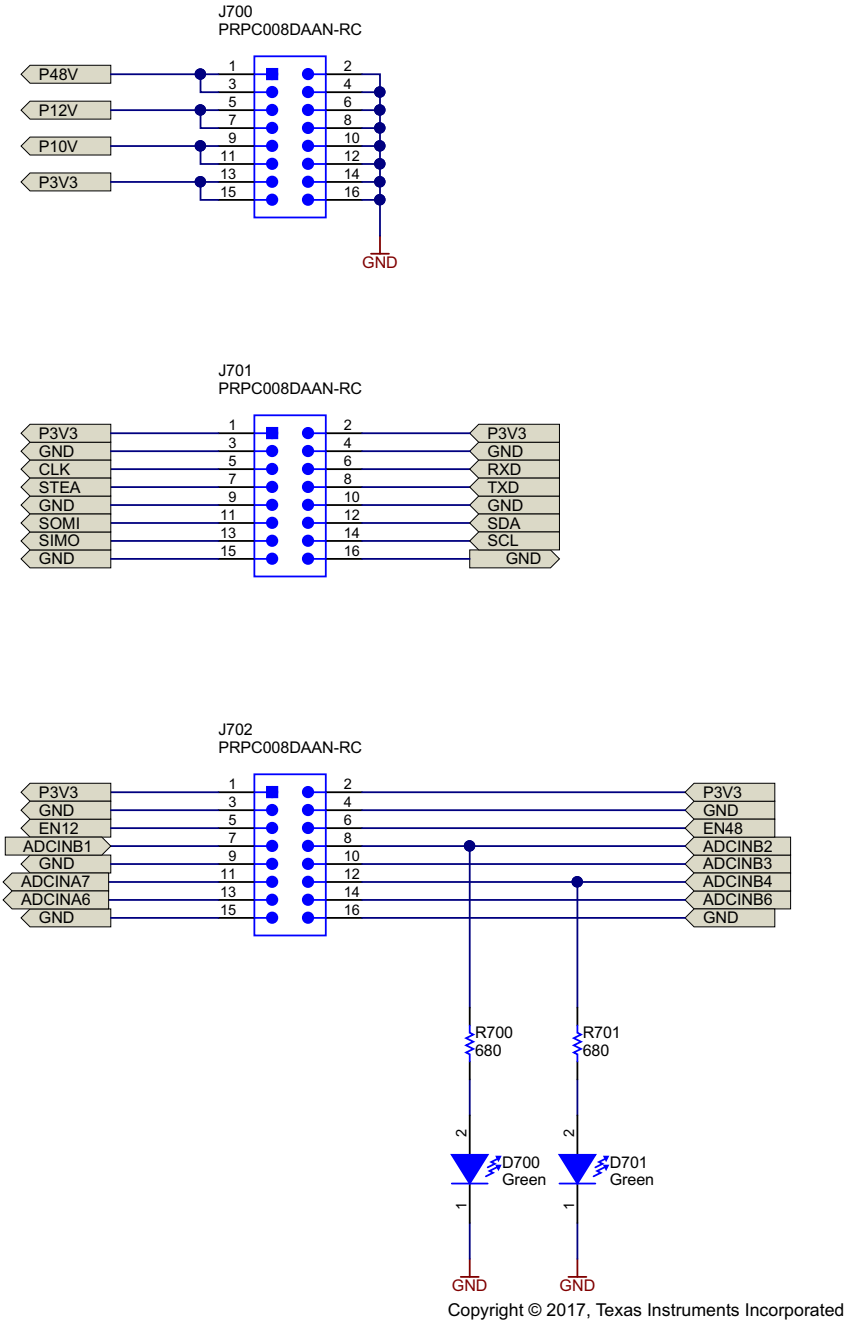


図 32. System Interface Schematic

Connectors J700 through J702 are standard through hole 2x8 pin headers with 100-mil spacing. LED diodes D700 and D701 are for debugging purposes and the user interface. Resistors R700 and R701 set the current through the LEDs to approximately 1 mA. All connectors have multiple ground signals for the optimal current return path.

3.9.4 Test Data

Test data for the 48-V block is not available and is a subject for future update.

4 Software Design

The software for the TIDA-01168 design enables basic functionality and a simple interface to a host system. The following subsections focus on the overall system architecture and voltage control loop. The software is written in C programming language and compiled using 16.9.1. LTS C2000 compiler in Code Composer Studio™ software 7.0.0.00043 from Texas Instruments.

注: The software for TIDA-01168 is developed for demonstration purposes only. Texas Instruments provides no warranty for using this software.

4.1 Architecture

The software architecture for the TIDA-01168 design follows a minimalist approach, using a layer architecture as shown in 図 33. The system does not use any real-time operating system or an extensive set of additional software libraries. Understanding the concept allows for easy modification and code porting to a different MCU.

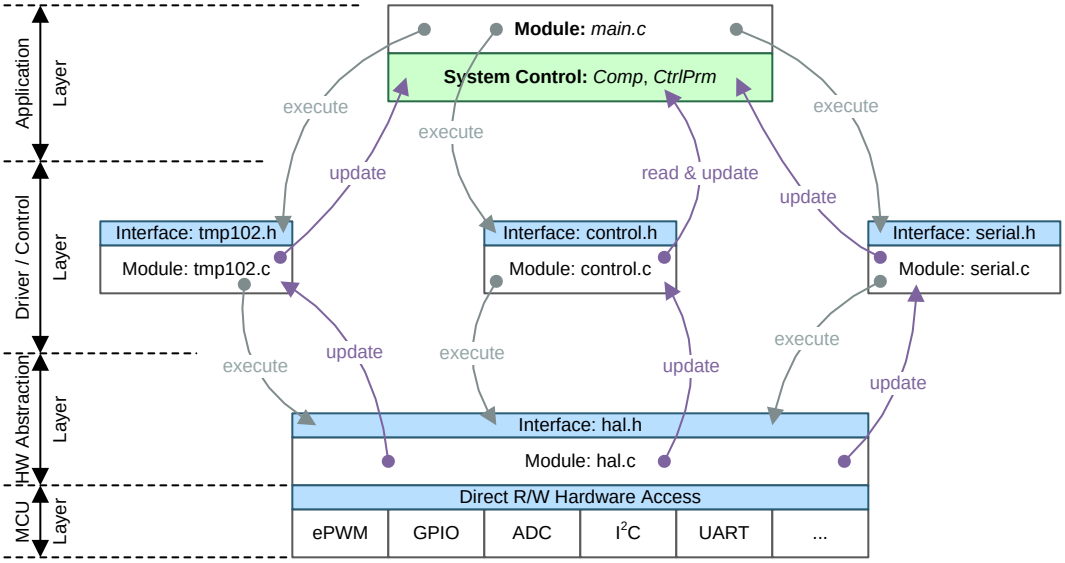


図 33. Software Architecture Diagram for TIDA-01168

The software architecture is split into four layers (see 図 33):

- Application Layer – (Module *main*)
- Driver/Control Layer – (Modules *tmp102, control, serial*)
- Hardware Abstraction Layer – (Module *hal*)
- MCU Layer – (TMS320F28027 registers and peripherals)

Communication between layers is from the top to the bottom with the given module interface. The Application Layer and Driver/Control Layer are hardware independent. Any access to the MCU registers or peripherals is in the HW Abstraction layer. This layer uses a set of functions and macros for direct access to the MCU Layer (MCU architecture). Only the HW Abstraction layer requires modification for migrating the software to a different MCU (changing the MCU layer).

The software uses a fixed-point Q number format for decimal numbers. All arithmetic operations with decimal numbers use C28X IQmath Library from Texas Instruments. This library is free of charge. See the *C28x IQmath Library* user's guide for further details [5].

4.2 The Super Loop (Main Loop)

The MCU executes the code in an endless main loop (super-loop architecture) with only two interrupts. The first interrupt is used for the control loop while the second is used for serial communication. Two main variables-structures *Comp* and *CtrlPrm* exist, which define system behavior and configuration. The type of these variables is declared in the *control* module header file and defined in the main module. See 表 13 and 表 14 for the description.

注: Q numbers have finite resolution given by the number of bits after the decimal point. This fact results in the arithmetic rounding of preset and calculated values.

表 13. Configuration Variable *CtrlPrm*

NAME	TYPE	TYPICAL VALUES	DESCRIPTION
Voltage, Current, and Temperature Measurements			
CtrlPrm.Meas.P12Vraw	Uint16	0…4095	P12V voltage AD conversion result after median-filtering
CtrlPrm.Meas.P48Vraw	Uint16	0…4095	P48V voltage AD conversion result after median-filtering
CtrlPrm.Meas.IMONraw	Uint16	0…4095	IMON voltage (current) AD conversion result after median-filtering
CtrlPrm.Meas.P12Vscaled	Q24	0…2.495	P12V voltage ADC result normalized to the voltage reference
CtrlPrm.Meas.P48Vscaled	Q24	0…2.495	P48V voltage ADC result normalized to the voltage reference
CtrlPrm.Meas.IMONscaled	Q24	0…2.495	IMON voltage (current) ADC result normalized to the voltage reference
CtrlPrm.Meas.P12Vvoltage	Q24	0…24.95	P12V voltage in Q number format
CtrlPrm.Meas.P48Vvoltage	Q24	0…75.10	P48V voltage in Q number format
CtrlPrm.Meas.IMONcurrent	Q23	0…175.685	IMON current in Q number format
CtrlPrm.Meas.TempPS1	Q4	–40…+125	Power stage 1 temperature in Q number format
CtrlPrm.Meas.TempPS2	Q4	–40…+125	Power stage 2 temperature in Q number format
CtrlPrm.Meas.TempPS3	Q4	–40…+125	Power stage 3 temperature in Q number format
CtrlPrm.Meas.TempPS4	Q4	–40…+125	Power stage 4 temperature in Q number format
Control Parameters			
CtrlPrm.Ctrl.P12Vset	Q24	6…18	Pre-set P12V output voltage for the BUCK mode
CtrlPrm.Ctrl.P48Vset	Q24	24…54	Pre-set P48V output voltage for the BOOST mode
CtrlPrm.Ctrl.NoOfPhases	Uint16 (3 bits)	0…4	Number of active phases
CtrlPrm.Ctrl.UVLOtrack	Uint16 (1 bit)	0/1	Real-time logic level of UVLO signal
CtrlPrm.Ctrl.nFAULTtrack	Uint16 (1 bit)	0/1	Real-time logic level of nFAULT signal
CtrlPrm.Ctrl.Mode	Uint16 (1 bit)	0/1 (1 = Buck, 0 = Boost)	Buck or boost operation mode
CtrlPrm.Ctrl.RefershTrig	Uint16 (1 bit)	Write 1, automatically clears to 0 when updated	Confirmation for the semi-synchronous control loop that LM5170-Q1 GPIOs shall be updated

表 14. Compensation Configuration Variable *Comp*

NAME	TYPE	TYPICAL VALUES	DESCRIPTION
Buck			
Comp.Buck.B0	Q24	–128…127.999999940	Buck digital compensator (regulator) input coefficient
Comp.Buck.B1	Q24	–128…127.999999940	Buck digital compensator (regulator) input coefficient
Comp.Buck.B2	Q24	–128…127.999999940	Buck digital compensator (regulator) input coefficient
Comp.Buck.A1	Q24	–128…127.999999940	Buck digital compensator (regulator) output coefficient
Comp.Buck.A2	Q24	–128…127.999999940	Buck digital compensator (regulator) output coefficient
Comp.Buck.Error	Q24	–2.495…2.495	Buck digital compensator (regulator) output and preset voltage difference (actual sample)
Comp.Buck.Error1	Q24	–2.495…2.495	Buck digital compensator (regulator) output and preset voltage difference (previous sample)
Comp.Buck.Error2	Q24	–2.495…2.495	Buck digital compensator (regulator) output and preset voltage difference (two samples ago)
Comp.Buck.SetOutput	Q24	0…2.495	Buck digital compensator (regulator) output (actual sample)
Comp.Buck.Output1	Q24	0…2.495	Buck digital compensator (regulator) output (previous sample)
Comp.Buck.Output2	Q24	0…2.495	Buck digital compensator (regulator) output (two samples ago)
Boost			
Comp.Boost.B0	Q24	–128…127.999999940	Boost digital compensator (regulator) input coefficient
Comp.Boost.B1	Q24	–128…127.999999940	Boost digital compensator (regulator) input coefficient
Comp.Boost.B2	Q24	–128…127.999999940	Boost digital compensator (regulator) input coefficient
Comp.Boost.A1	Q24	–128…127.999999940	Boost digital compensator (regulator) output coefficient
Comp.Boost.A2	Q24	–128…127.999999940	Boost digital compensator (regulator) output coefficient
Comp.Boost.Error	Q24	–2.495…2.495	Boost digital compensator (regulator) output and preset voltage difference (actual sample)
Comp.Boost.Error1	Q24	–2.495…2.495	Boost digital compensator (regulator) output and preset voltage difference (previous sample)
Comp.Boost.Error2	Q24	–2.495…2.495	Boost digital compensator (regulator) output and preset voltage difference (two samples ago)
Comp.Boost.SetOutput	Q24	0…2.495	Boost digital compensator (regulator) output (actual sample)
Comp.Boost.Output1	Q24	0…2.495	Boost digital compensator (regulator) output (previous sample)
Comp.Boost.Output1	Q24	0…2.495	Boost digital compensator (regulator) output (two samples ago)

Atomic instruction is required for confirming a new configuration, which is important for the digital compensator running in the interrupt routine. One example case is when the DIR signal changes polarity right before the interrupt; the digital compensator may still compensate for the old mode setting (BUCK, for example) while the DIR signal corresponds to the new mode setting (BOOST, for example).

図 34 shows a flow chart of the super-loop.

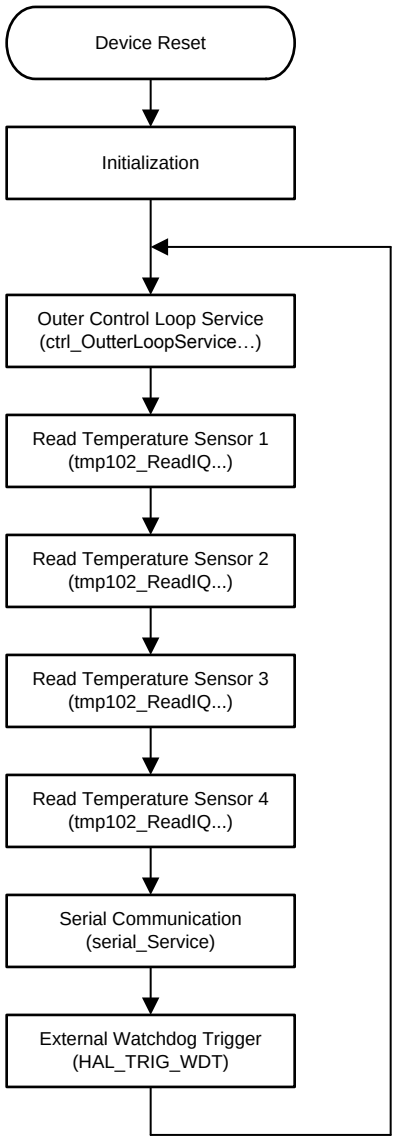


図 34. Super-Loop Flow Chart

4.3 Control Loop

The task of the control loop is to provide voltage feedback and control GPIO pins for the LM5170-Q1 subsystems, for which two sub-control loops exist:

- Synchronous interrupt-driven digital compensator
- Semi-synchronous LM5170-Q1 GPIO control

The digital compensator must be synchronous with the control loop and PWM for the ISETD signal to obtain a stable and predictable performance from the DC-DC converter. For this reason, the code is executed in the interrupt service routine, which occurs every new PWM period on the rising edge. 図 35 shows a simplified flow chart of the interrupt-driven digital compensator.

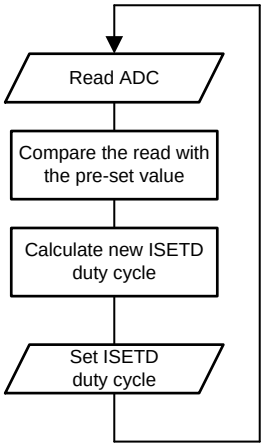


図 35. Simplified Control-Loop Flow Chart

図 36 shows the timing of the synchronous control loop. With every rising edge of the ISETD signal the interrupt routine reads the latest analog conversion results, performs filtering (median), and calculates a new duty cycle for the ISETD signal. The duty cycle is updated automatically with the next PWM period.

Consider the following timing constraints:

t_{ctrl_busy} is the amount of time the MCU spends in the interrupt service routine for the voltage feedback loop. Ensuring that this time is shorter than the control loop cycle t_{ctrl_loop} under any condition is important. This time can be measured using an oscilloscope and toggling a free GPIO pin. The TIDA-01168 reference design uses the LED700 connected to ADCINB2 which is set ON at the beginning and set OFF at the end of every control loop interrupt. The t_{ctrl_busy} / t_{ctrl_loop} ratio corresponds to the total utilization of the MCU by the control loop (omitting GPIOs control in the main super-loop). t_{ctrl_free} is the time when the MCU can perform other actions such as communication. t_{ISETD_ON} and t_{ISETD_OFF} define the duty cycle of the ISETD signal. The PWM corresponds to the control loop cycle t_{ctrl_loop} period, which is always constant. $t_{ADC\_CTRL\_SAMPL}$ is the effective sampling period of the AD converter, which is used for compensator calculations. This sampling period has small jitter due to the median filtering technique described in 4.3.1, but on average, the sampling period corresponds to the control loop cycle t_{ctrl_loop}.

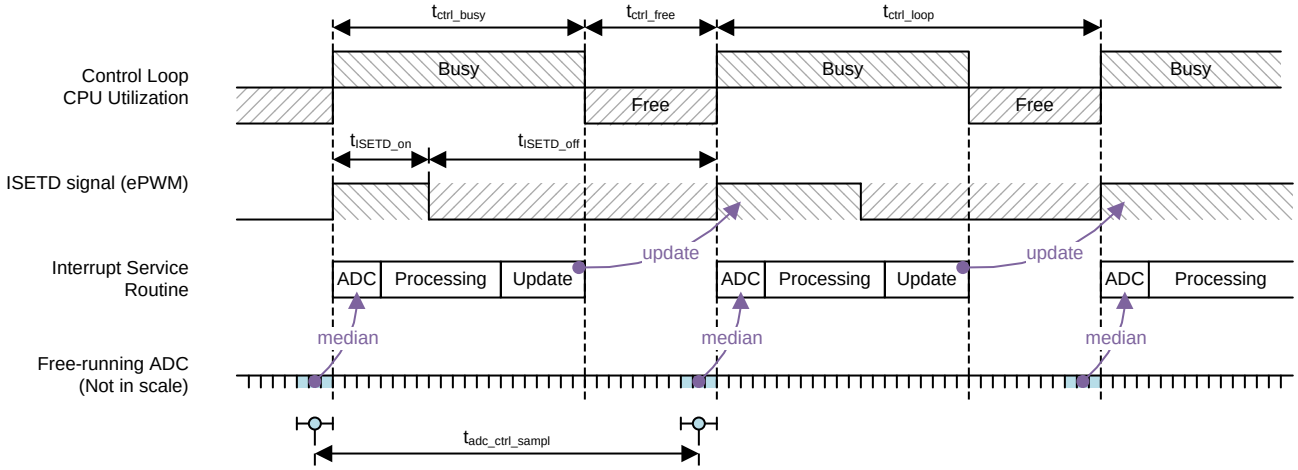


図 36. Control Loop Timing Diagram for TIDA-01168

Additional control signals for the LM5170-Q1 subsystems are not usually time critical. The second semi-synchronous control loop is executed in the main loop in the application layer. This loop is semi-synchronous because the timing may vary based on a number of other events during the main loop execution, for example, serial communication. 図 37 shows a flow chart of the semi-synchronous control loop.

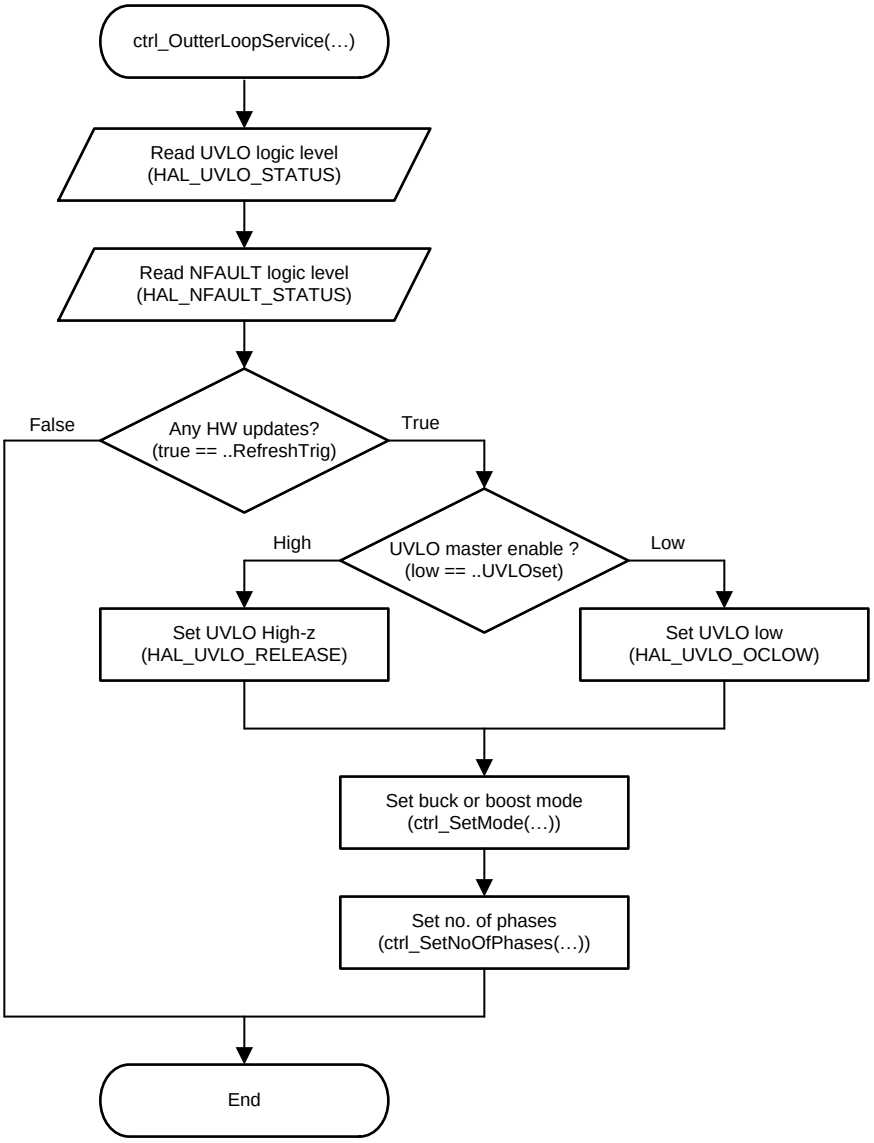


図 37. Flow Chart – Semi-Synchronous Control Loop Service

The semi-synchronous control loop periodically updates the logic levels of the UVLO and NFAULT open collector signals in the *CtrlPrm* variable to inform the host system. Successively, the algorithm checks the *RefreshTrig* bit to see if any update is required. If so, the algorithm changes the UVLO, DIR, and EN1-EN4 signals (GPIOs) according to the parameters stored in the *CtrlPrm* variable.

注: The CPU overhead for the control loop running a digital compensator can be reduced to nearly zero using advanced peripheries such as Control Law Accelerator (CLA) in selected C2000 MCUs.

4.3.1 AD Conversion

The C2000 microcontroller family has a highly-configurable AD converter periphery which allows free-running automatic sampling of multiple input channels. The ADC in the TIDA-01168 reference design is configured in such a way that every channel is sampled three times in a sequence, as 図 38 shows. Every instance of nine conversion results is stored in a different memory location.

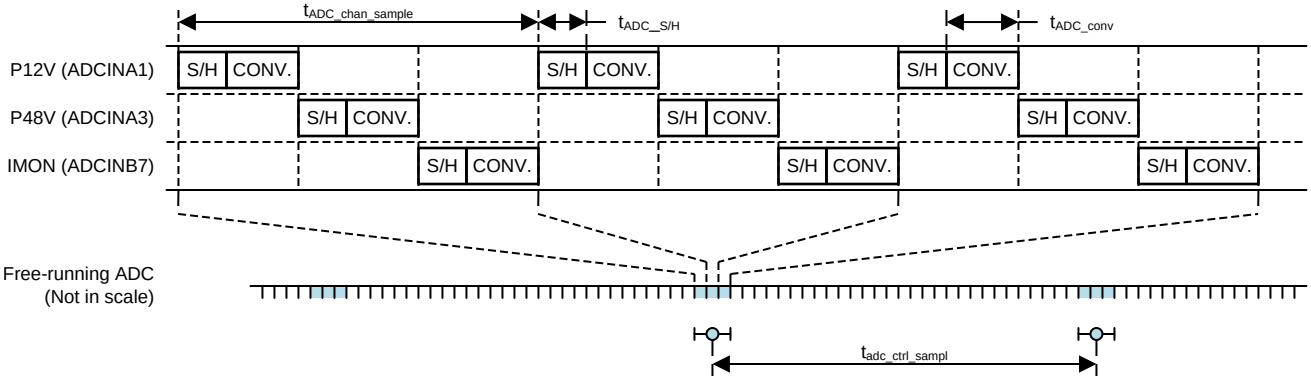


図 38. ADC Channels Conversion Timing Diagram

The ADC periphery automatically runs this sequence in the background without any MCU intervention. The benefit of this configuration is that, at any time, the system has the last three conversion results for all channels in the memory. This data is used for a simple median filter implementation, which effectively eliminates impulsive noise. The size of the filter window is three which means that the filter takes the last three conversion results and returns the mean value. 図 39, 図 40, and 図 41 show the effect of the mean filter. The charts represent the sensing stable voltage reference on the KL40_M and KL41_M signals. The charts show that random spurious peaks have been eliminated.

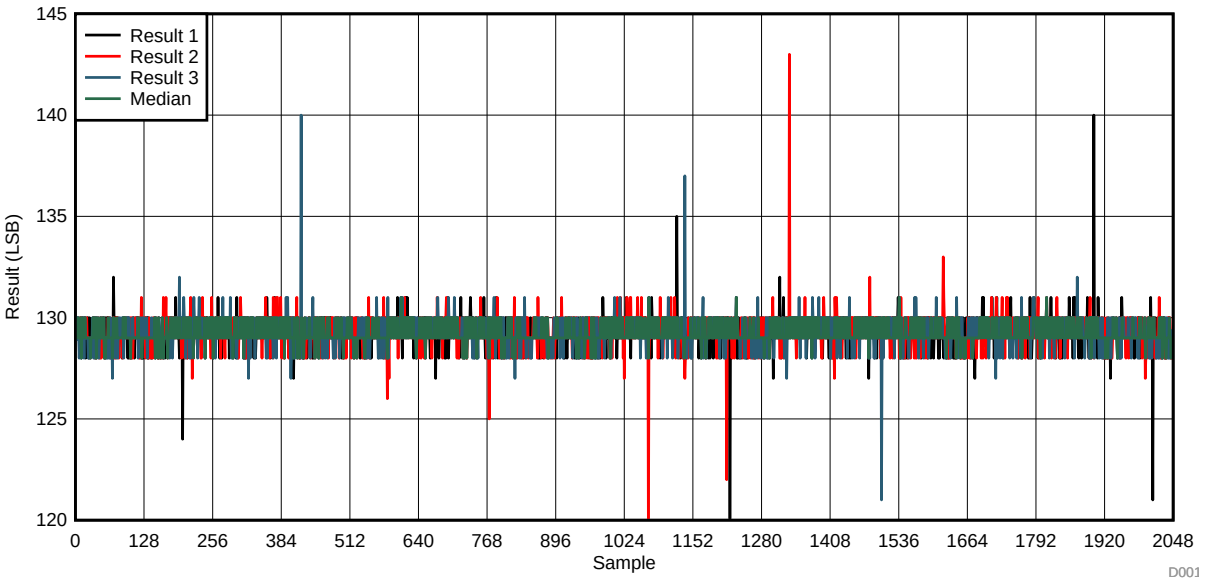


図 39. Effect of Median Filter in Time Domain

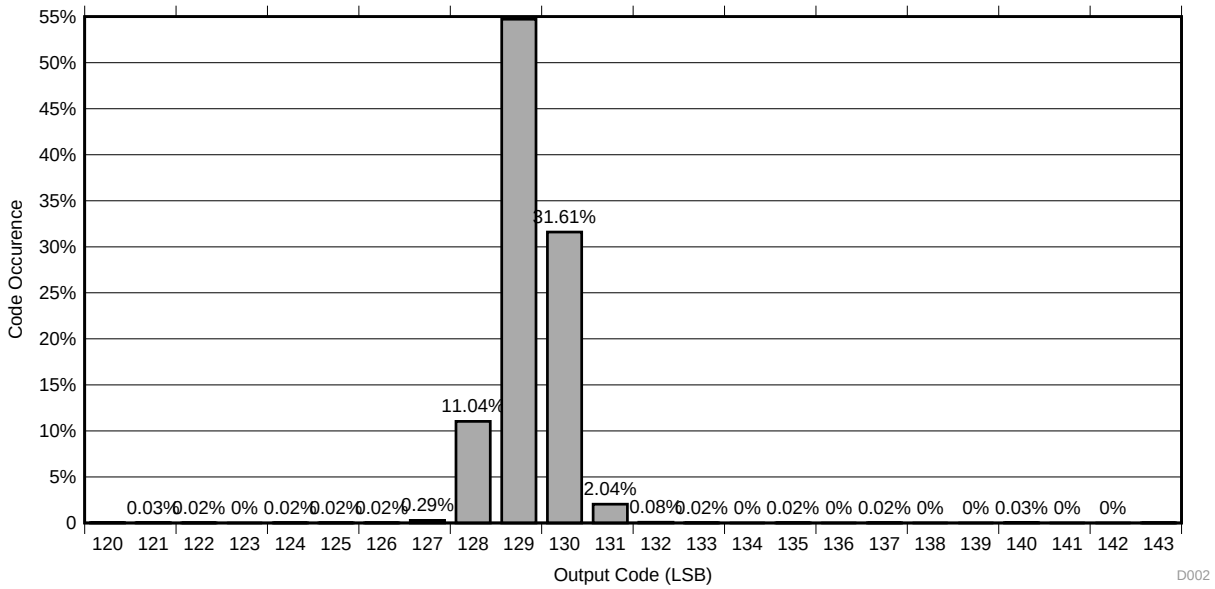


図 40. Histogram of Conversion Results Without Median Filter

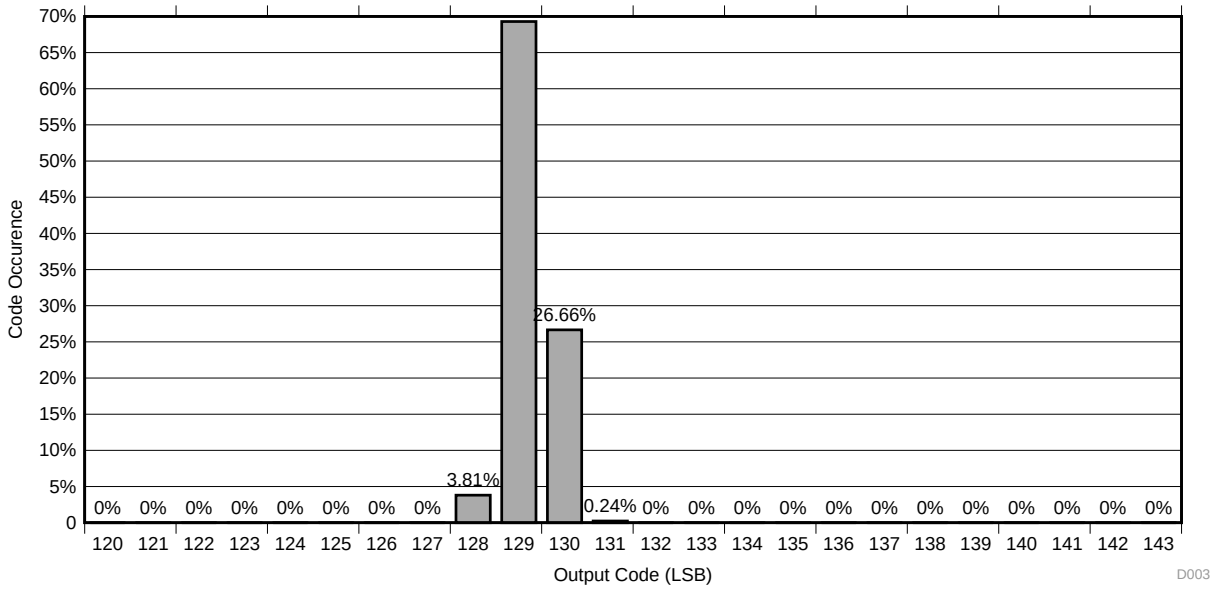


図 41. Histogram of Conversion Results With Median Filter

Understanding the timing and the effect on the system is important. Only the last three conversion results for every channel, which were taken right before the interrupt service routine, are filtered and used. Other results are discarded. For these reasons, the effective sampling frequency of the AD converter is given by $t_{adc\_ctrl\_sampl}$. The median filter introduces time jitter in the AD conversion timing because it is impossible to determine which result from the filter window is returned to the control loop algorithm. The jitter size is ±3 × $t_{ADC\_chan\_sampl}$, where $t_{ADC\_chan\_sampl}$ is the channel sampling period. The jitter size should not exceed one-tenth of the control loop cycle t_{ctrl_loop}. The conversion time t_{ADC_conv} is usually fixed and corresponds to the resolution and clock source of the ADC.

The sample-and-hold window time $t_{ADC\_S/H}$ is also important. A short transient occurs when the sample-and-hold circuit captures voltage on the pin and starts charging the internal sampling capacitor. The operational amplifier driving this pin reacts to this with a transient response with settling time t_{settle}. Note the importance of having a $t_{ADC\_S/H}$ that is longer than t_{settle} (see 図 42). This behavior can be greatly improved by adding an R-C network, as suggested in 3.6.3.

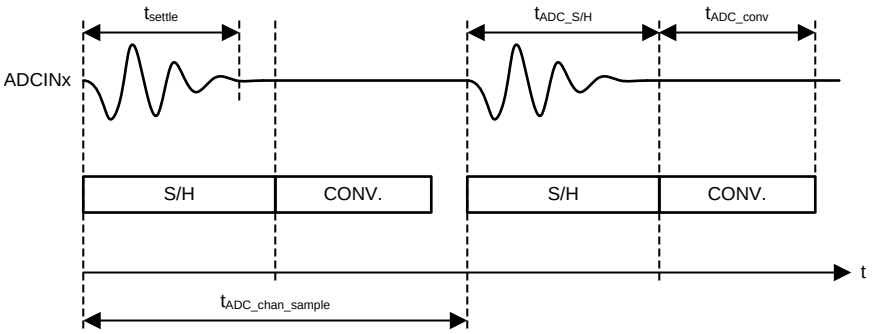


図 42. Sample-and-Hold Circuit Timing

4.3.2 Digital Compensator

A DC-DC converter is a closed-loop system that requires frequency compensation for the control loop to remain stable under any circumstances and to provide the desired step response.

Design procedure:

1. Compensate the inner current loop
   - Same compensation loop regardless of BUCK or BOOST mode
2. Compensate the outer voltage loop
   - Separate error amplifiers for each mode of operation
   - Low frequency pole is major concern in BUCK mode
   - Beware of right-half-plane zero (RHPZ) in BOOST model

The inner current control loop uses analog compensation as described in the LM5170-Q1 data sheet [2]. The following selections are applied for the analog compensation and offer a good trade-off between transient response and stability:

- Crossover frequency f_{c_curr} for the inner current loop is 1/6th of the switching frequency f_{sw}
- Compensation zero frequency f_{z1_curr} is set to half of the crossover frequency f_{c_curr}
- Compensation pole frequency f_{p1_curr} is between half of the switching frequency f_{sw} and switching frequency f_{sw} to attenuate high frequency noise

注: Various strategies are available for determining compensation parameters. Crossover frequency, compensation zero, and pole location recommendations may vary from what is recommended in the *LM5170-Q1 Design Calculator*, which is a part of the Tools & Software folder of LM5170-Q1 on TI.com.

The external voltage control loop is digital and therefore requires a digital compensator. Designing a digital compensator for a DC-DC converter has already been described in various literature and a detailed description exceeds the scope of this document. This subsection highlights design differences for a hybrid solution with a combined analog and digital feedback loop used with the LM5170-Q1.

図 43 shows the LM5170-Q1 operating in buck mode using an analog compensator for the outer voltage feedback loop. Both current (highlighted red) and voltage (highlighted blue) compensators are type-II. The main difference is that the current loop compensator uses a transconductance amplifier (OTA) while the voltage loop compensator uses a traditional operational amplifier. Both compensation networks have two poles and one zero. See the *Demystifying Type II and Type III Compensators Using OpAmp and OTA for DC/DC Converters* application report [16] for details as to how their operation differs.

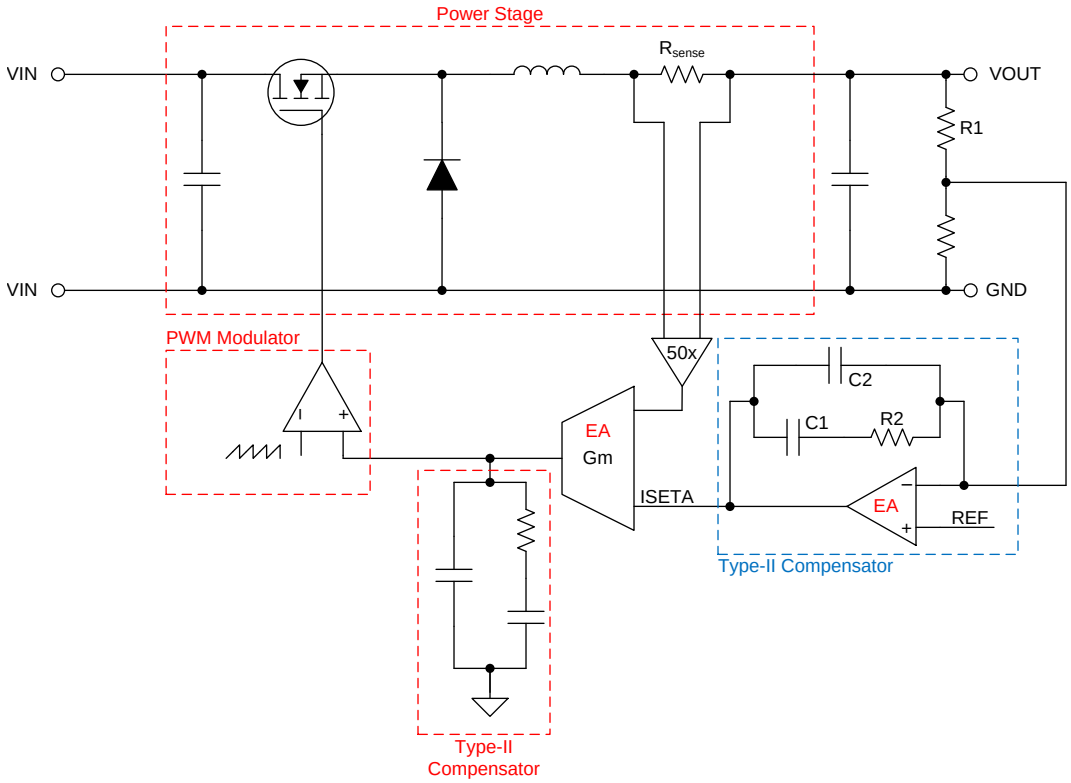


図 43. Control Loop for LM5170-Q1 With Analog Voltage Feedback Operating in BUCK Mode

The type-II controller transfer function in Laplace domain is:

$$H_C(s) = \frac{\omega_{cp0}}{s} \times \frac{1 + \frac{s}{\omega_{cz1}}}{1 + \frac{s}{\omega_{cp1}}} \quad (1)$$

where ω_{cp0} is the pole at the origin:

$$\omega cp0 = \frac{1}{R_1 C_1} \quad (2)$$

ω_{cz1} is a compensation zero:

$$\omega_{cz1} = \frac{1}{R_2 C_1} \quad (3)$$

and ω_{cp1} is a compensation pole:

$$\omega_{cp1} = \frac{1}{R_2 C_2} \quad (4)$$

図 44 shows the gain and phase curve of a type-II compensator using an operational amplifier.

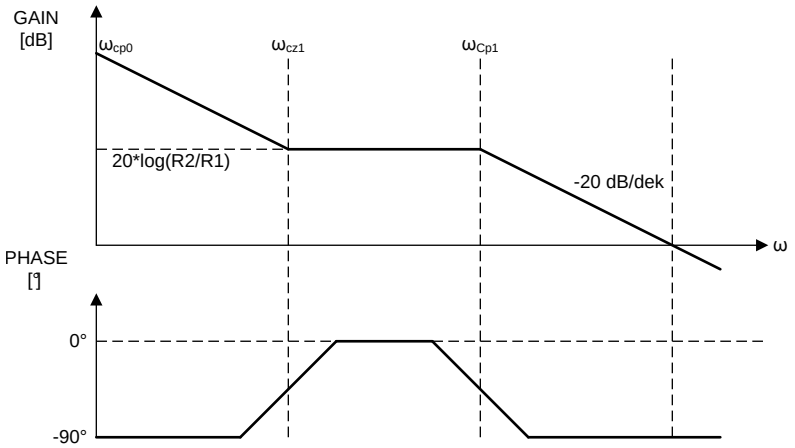


図 44. Phase and Gain of Type-II Compensator

LM5170-Q1 outer voltage feedback loop compensator

For the BUCK compensator, Texas Instruments recommends to set:

- Crossover frequency $f_{c\_volt\_buck}$ to 1/5 of the inner current loop crossover frequency f_{c_curr}
- Compensation zero frequency $f_{z1\_volt\_buck}$ to 1/10 of the outer voltage loop crossover frequency $f_{c\_volt\_buck}$
- Compensation pole frequency $f_{p1\_volt\_buck}$ between half of the switching frequency f_{sw} and switching frequency f_{sw} to attenuate high-frequency noise.

For the BOOST compensator, Texas Instruments recommends to set:

- Crossover frequency $f_{c\_volt\_boost}$ to approximately 1/5 of the current open loop crossover frequency f_{c_curr} , or 1/5 of RHP zero, whichever is lower
- Compensation zero frequency $f_{z1\_volt\_boost}$ to 1/10 of the outer voltage loop crossover frequency $f_{c\_volt\_boost}$
- Compensation pole frequency $f_{p1\_volt\_boost}$ close to half of the switching frequency f_{sw}.

図 45 shows the case when a digital solution replaces the analog compensator in the outer voltage loop. The behavior of the digital compensator is identical to the analog counterpart. To implement a discrete time compensator, poles and zeros from the analog domain must be converted into the digital domain. This task involves converting from the continuous time s-domain to the discrete time z-domain. The bilinear (also known as Tustin's or Mobius) transformation is relatively simple and effective method [17].

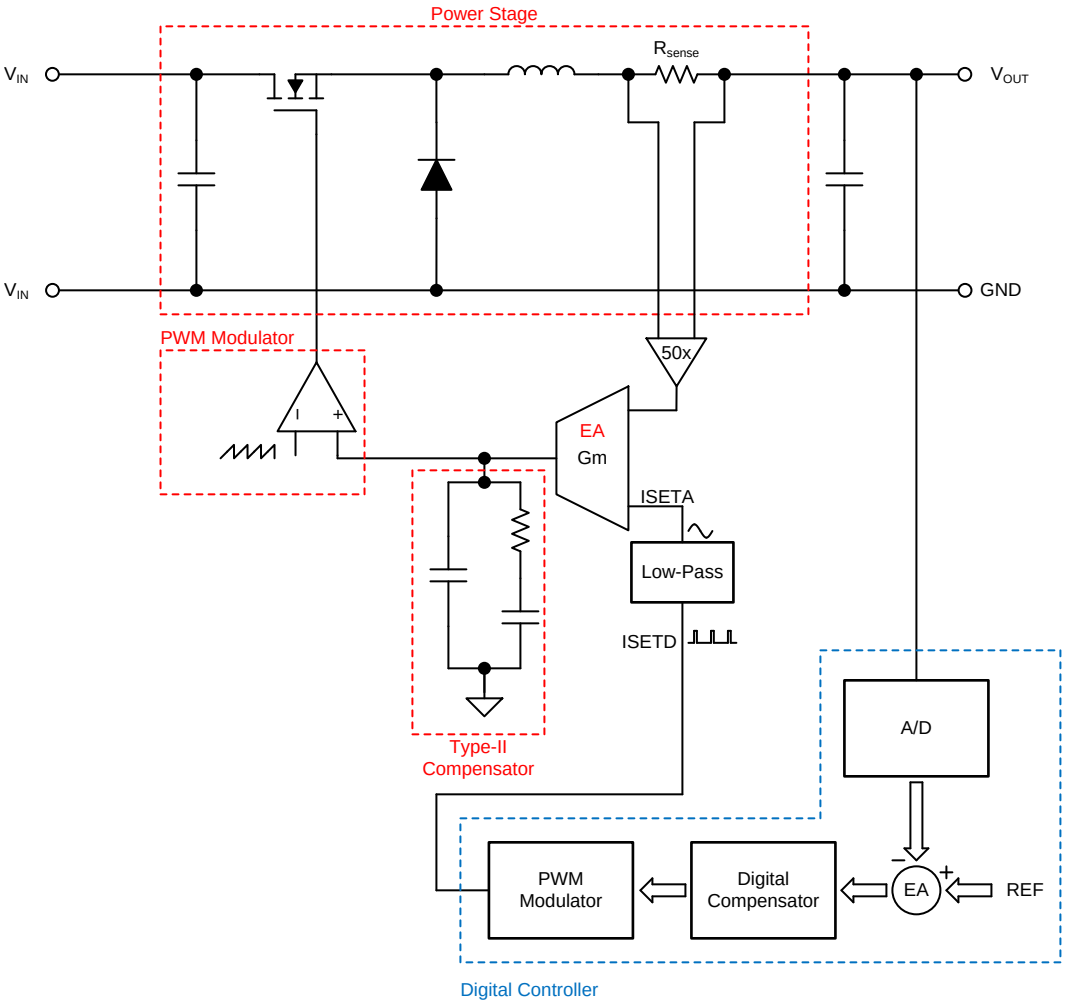


図 45. Control Loop for LM5170-Q1 With Digital Voltage Feedback Operating in BUCK Mode

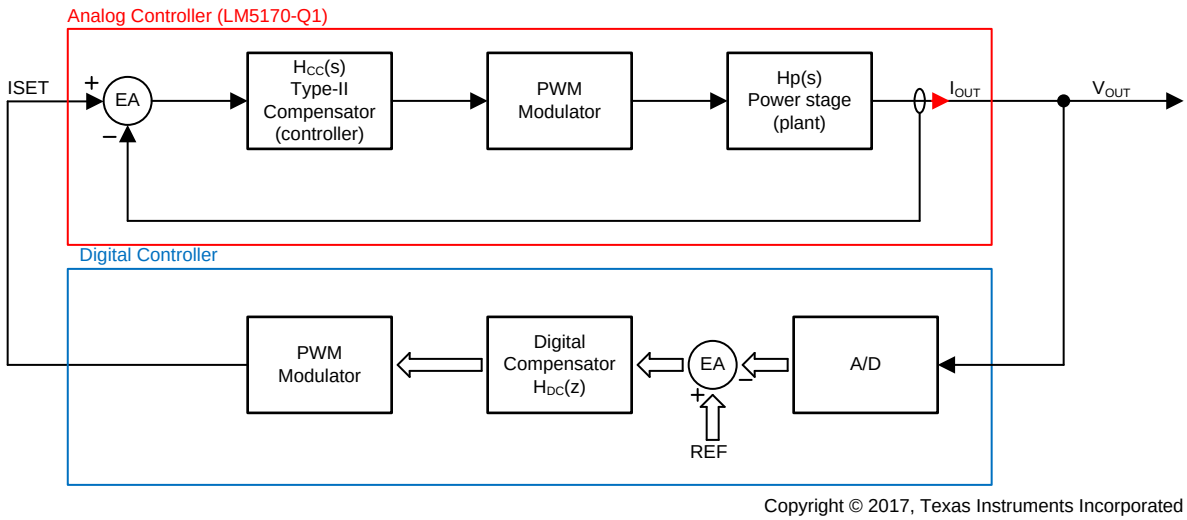


図 46. Small Signal Analysis of Control Loop for LM5170-Q1 With Digital Voltage Feedback

The transfer function of an analog compensator can be converted in to the z-domain by replacing the 's' terms with:

$$s \leftarrow \frac{2z-1}{Tz+1} \tag{5}$$

where *T* is the sampling period $t_{adc\_ctrl\_sampl}$. 式 5 may then be substituted into the type-II controller transfer function given in 式 1 to yield the equivalent discrete time compensator transfer function in 式 6.

$$H_C[Z] = \frac{\frac{\omega cp0}{2z-1}}{Tz+1} \times \frac{1+\frac{\frac{2z-1}{Tz+1}}{\omega_{cz1}}}{1+\frac{Tz+1}{\omega_{cp1}}} \tag{6}$$

After some algebraic manipulation, this function can be represented in terms of a standard discrete two-pole two-zero (2p2z) discrete controller transfer function (see 式 7).

$$H_C[Z] = \frac{B_2 + B_1 z + B_0 z^2}{-A_2 - A_1 z + z^2} \tag{7}$$

where,

$$B_0 = \frac{\left(T\omega_{cp0}\omega_{cp1}\left(2+T\omega_{CZ1}\right)\right)}{2\left(2+T\omega_{CP1}\right)\omega_{CZ1}}$$

$$B_1 = \frac{T^2\omega cp0\omega cp1}{\left(2+T\omega_{cp1}\right)}$$

$$B_2 = \frac{T\omega_{cp0\omega cp1}\left(-2+T\omega_{cz1}\right)}{2\left(2+T\omega_{cp1}\right)\omega_{cz1}}$$

$$A_1 = \frac{4}{\left(2+T\omega_{cp1}\right)}$$

$$A_2 = \frac{\left(-2+T\omega_{cp1}\right)}{\left(2+T\omega_{cp1}\right)} \tag{8}$$

To obtain the linear difference equation (LDE) from the two-pole two-zero discrete transfer function (式 7), first multiply both top and bottom through by z^{-2}, as shown in 式 9.

$$H_C[z] = \frac{y[z]}{x[z]} = \frac{B_2 z^{-2} + B_1 z^{-1} + B_0}{-A_2 z^{-2} - A_1 z^{-1} + 1} \tag{9}$$

式 9 can now be rearranged to obtain the linear difference equation that can be calculated using a microprocessor:

$$y[z]\left(-A_2 z^{-2} - A_2 z^{-1} + 1\right) = x[z]\left(B_2 z^{-2} + B_2 z^{-1} + B_0\right)$$

$$-A_2 y[n-2] - A_1 y[n-1] + y[n] = B_2 x[n-2] + B_1 x[n-1] + B_0 x[n]$$

$$y[n] = B_2 x[n-2] + B_1 x[n-1] + B_0 x[n] + A_2 y[n-2] + A_1 y[n-1] \tag{10}$$

Where x[n] is the error input to the controller for this sampling period and y[n] is the controller output for this sampling period. x[n-1] denotes the pervious sampling period and x[n-2] is two sampling periods in the past.

図 47 shows a simplified flow chart for the digital compensator. The program flow and computation is the same for BUCK and BOOST modes and only the variables differ.

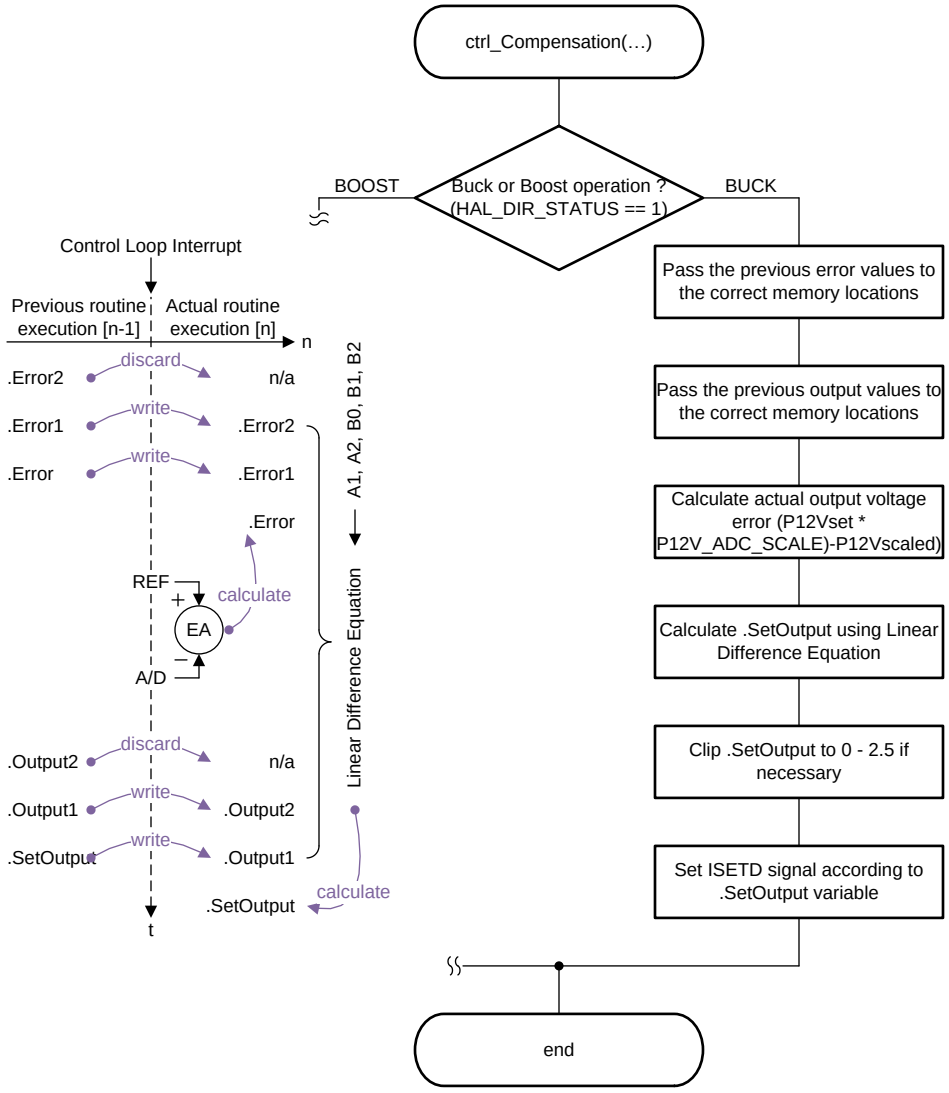


図 47. Digital Compensator Flow Chart

The following is a code snippet of the actual digital compensator for the BUCK mode visualized on 図 47.

```
...
if (HAL_DIR_STATUS == 1)/* previously = (BUCK == (*Param).Ctrl.Mode)*/
    {
        /* Pass Previous Errors to the correct memory location */
        (*Reg).Buck.Error2 = (*Reg).Buck.Error1;
        (*Reg).Buck.Error1 = (*Reg).Buck.Error;
        /* Pass previous output values to the correct memory location */
        (*Reg).Buck.Output2 = (*Reg).Buck.Output1;
        (*Reg).Buck.Output1 = (*Reg).Buck.SetOutput;
        /* Calculate error */
        (*Reg).Buck.Error = _IQmpy((*Param).Ctrl.P12Vset, _IQ(P12V_ADC_SCALE)) -
 (*Param).Meas.P12Vscaled;
        /* Sets the output using the differential linear difference equation */
        (*Reg).Buck.SetOutput = _IQmpy((*Reg).Buck.B0, (*Reg).Buck.Error) +
                                _IQmpy((*Reg).Buck.B1, (*Reg).Buck.Error1) +
                                _IQmpy((*Reg).Buck.B2, (*Reg).Buck.Error2) +
                                _IQmpy((*Reg).Buck.A1, (*Reg).Buck.Output1) +
                                _IQmpy((*Reg).Buck.A2, (*Reg).Buck.Output2);

        /* This will limit Value to % duty cycle */
        if ((*Reg).Buck.SetOutput > _IQ(2.5)) { (*Reg).Buck.SetOutput = _IQ(2.5); }
        else if ((*Reg).Buck.SetOutput < _IQ(0.000)) { (*Reg).Buck.SetOutput = _IQ(0.000); }

        /* Error becomes the Duty Cycle */
        HAL_SET_DUTY(_IQ19int(_IQ19mpy(_IQtoIQ19((*Reg).Buck.SetOutput), _IQ19(SCALE_ISETD))));
    }
    /* BOOST operation compensation */
    else
    {
    ....
```

See the *Modeling Bi-Directional Buck/Boost Converter for Digital Control Using C2000 Microcontrollers* application report [6] and the *Introduction to Digital Control of Switched-Mode Power Converters* presentation [7] for additional literature.

注: Texas Instruments has a complete set of C2000 libraries for digital power supplies. See the C28x Digital Power Library in the controlSUITE™ software or powerSUITE for more details.

4.3.3 PWM for ISETD

Consider the two following important considerations regarding PWM generation for the ISETD signal:

- Resolution
- Update behavior

PWM modulators in MCUs require a clock source which is derived from a system clock generator. The smallest step (LSB) for a PWM period or duty cycle corresponds to the clock source period. This parameter limits the maximum output frequency or resolution of the generated signal. The MCU in TIDA-01168 uses a 50-MHz system clock which is 20 ns per period. The control loop has a 10-b resolution; therefore, 1024 × 20 ns = 20.48 µs, which is the ISETD and the control loop period.

PWM modulators typically compare an internal counter with a digital comparator register. When the counter matches the comparator, the output of the modulator changes value. This action is used for duty cycle control. When the internal counter overflows, the output is changed again to the default state, which controls the period.

However, the update behavior of such a PWM modulator may be not always be as predictable as 図 48 shows. In all three cases A, B, and C, the update occurs at 25% of the PWM period.

- In the case of **A**:

  The new duty cycle (digital comparator) value is bigger than the actual value of the counter. The duty cycle changes immediately to the new value.

- In the case of **B**:

  The new duty cycle (digital comparator) value is smaller than the actual value of the counter. The duty cycle changes temporarily to the actual counter value. The new desired duty cycle transpires with the new PWM period.

- In the case of **C**:

  C is a configuration when the PWM is always updated with a PWM period. This configuration is recommended because it provides the most predictable timing for the control loop.

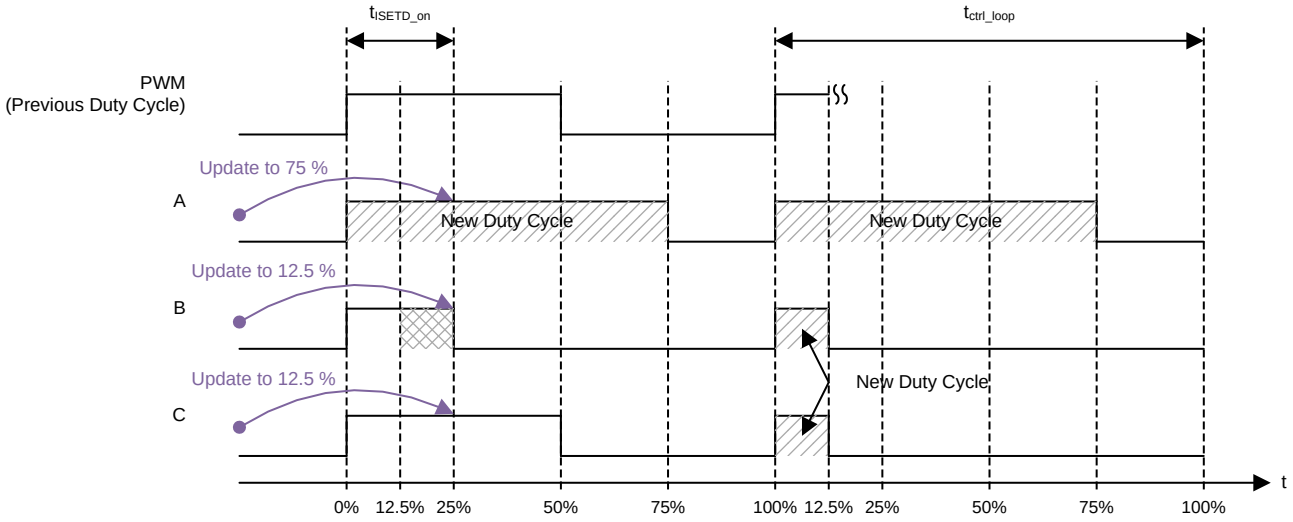


図 48. Update Behavior of PWM Modulator

注: The selected C2000 MCUs from Texas Instruments have an enhanced pulse-width modulator (ePWM) module with a high-resolution pulse-width modulator (HRPWM) extension. The HRPWM module extends the time resolution capabilities of the conventionally-derived digital pulse-width modulator (ePWM). HRPWM is typically used when the PWM resolution falls approximately below 9 to 10 bits.

5 Getting Started Hardware and Software

5.1 Hardware

5.1.1 Recommended Laboratory Setup Description

A test setup for a bidirectional DC-DC converter is quite complex. 図 49 shows a recommended hardware setup for TIDA-01168.

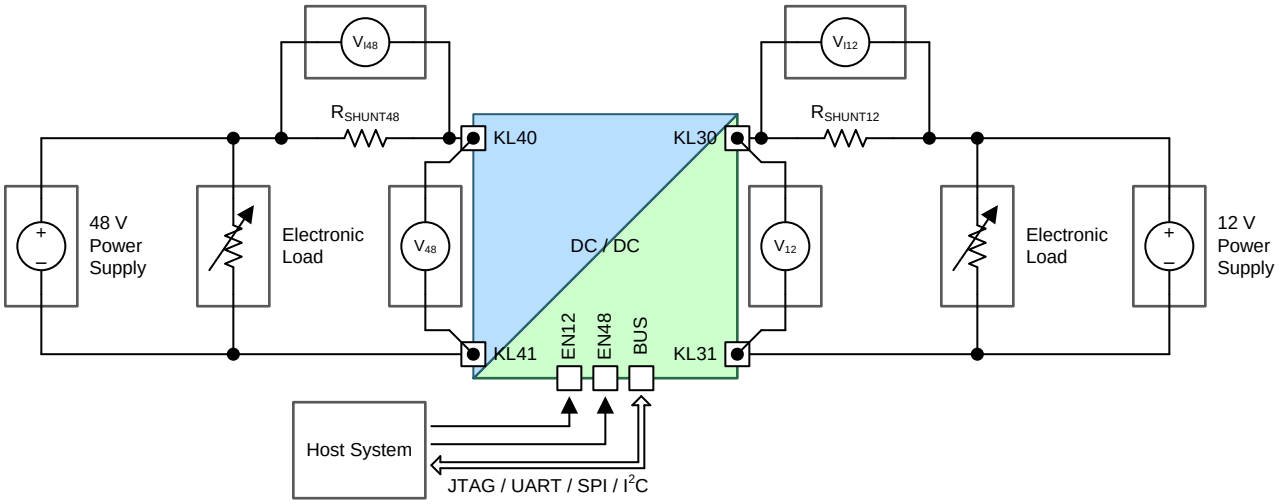


図 49. Recommended Hardware Setup for TIDA-01168

Power supplies on both sides must be able to source and sink current (two-quadrant power supply) in cases where bidirectional operation is desired. Alternatively, a traditional one-quadrant power supply can be used in parallel with an electronic load for the replacement (see 図 50). The power supply current limit corresponds to the sum of input and output currents from the system. The electronic load operates in constant current mode set to the level of maximum output current from the system. When the system operates as a load, the energy consumed by the electronic load is wasted. When the system operates as a source then the electronic load consumes all current and adds all the current from the 48-V power supply on top to achieve the preset value. See the *LM5170-Q1 EVM User Guide* [8] for further information.

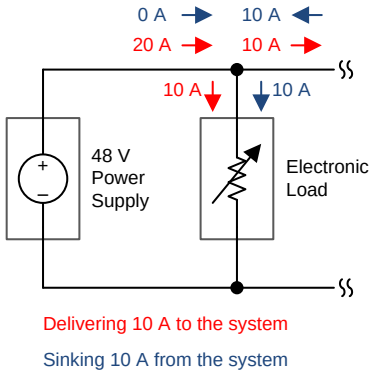


図 50. Power Supply With Electronic Load in Parallel Allowing Bidirectional Current Flow

注: The digital voltage control implemented in TIDA-01168 does not have a current limit. The voltage feedback loop must be disabled when using a power supply in parallel with an electronic load, such as in the example shown in 図 50.

High currents on power rails are measured indirectly by measuring the voltage (V_{I12}, V_{I48}) across a precision shunt resistor ($R_{SHUNT12}$, $R_{SHUNT48}$). 図 52 shows an example of these precision resistors. The power rail voltage is measured directly on KL30, KL31 and KL40, and KL41 system terminals. Terminals with cable lugs are modified as shown in 図 51 to fit the mechanical dimensions of the PCB the system. The host system is a battery-operated laptop which controls the TIDA-01168 using a JTAG or universal asynchronous receiver/transmitter (UART) interface. The EN12 and EN48 enable signals come from an additional laboratory power supply.

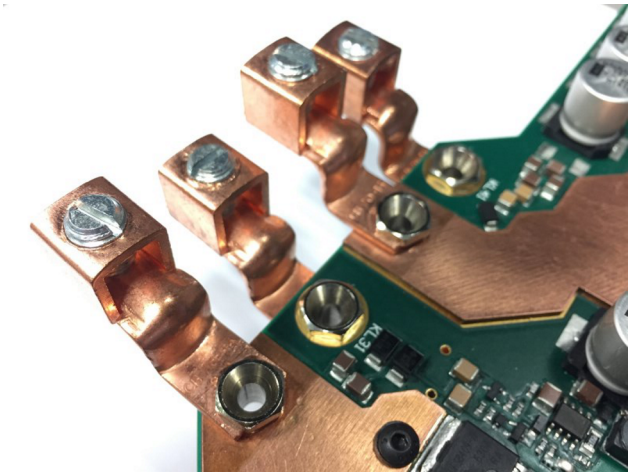


図 51. Modified Terminals for TIDA-01168

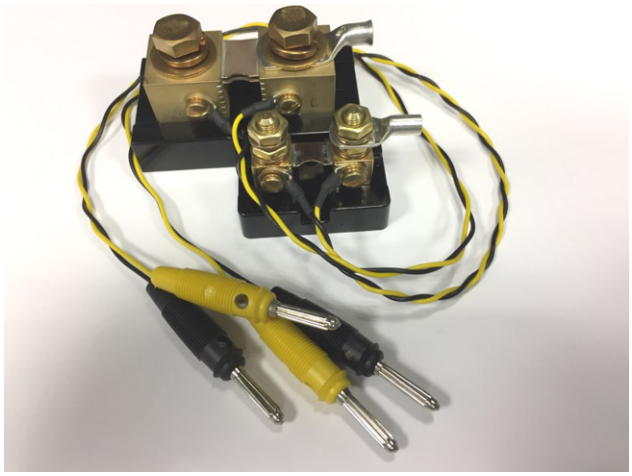


図 52. Current Shunts

See 表 15 for an overview of the selected hardware used during TIDA-01168 development.

表 15. List of Equipment Used for Test Setup

EQUIPMENT	TYPE
48-V power supply	Chroma 62024P-80-60
48-V electronic load	BK Precision 8518
12-V power supply	Supply Chroma 62012P-40-120
48-V electronic load	Kikusui PLZ10004W
V_{48}, V_{12} Voltmeters	Fluke 87-V Industrial Multimeter
V_{I48}, V_{I12} Voltmeters	Keysight 34410A
$R_{SHUNT48}$	Murata Power Solutions 3020-01108-0
$R_{SHUNT12}$	Murata Power Solutions 3020-01101-0
JTAG probe	XDS100v2 JTAG Debug Probe (14-pin TI version) (TMDSEMU100V2U-14)
Cables	AWG8, AWG6
KL40, KL41, KL30, KL31 terminals	Panduit CB70-14-CY (image of modified version in 図 51)

5.2 TIDA-01168 First Powering

This subsection describes a concise, step-by-step procedure for the turnon required by the TIDA-01168 for MCU programming.

Follow these steps when first powering the reference design in BUCK mode (unidirectional operation):

1. Make sure to switch off all the laboratory equipment (laboratory power supplies, for example).
2. Connect the 48-V power supply output to KL40 (positive) and KL41 (negative) terminals. Preset the output voltage to 48 V and set the current limit to 1 A.
3. Connect signal EN48 (J702, pin 6) and ground (J702, pin 4) to an external laboratory power supply. Preset the output voltage to 5 V and set the current limit to 10 mA. Keep the output OFF.
4. Connect the XDS100 JTAG probe to J800.
5. Connect the JTAG probe to the laptop.
6. Turn on the 48-V power supply.
7. Turn on the external laboratory power supply for the EN48.
8. Verify that the LEDs are ON.
9. Proceed to the software section.

5.3 Software

The MCU in the TIDA-01168 reference design must be programmed to make the system functional. TI recommends using the JTAG programming interface.

注: The software configuration in the following subsections utilize the Microsoft® Windows® 7 operating system SP1 (x64), build 7601 and a Google Chrome™ browser (56.0.2924.87).

5.3.1 JTAG Probe Configuration

Programming the TMS320F28027F MCU in the TIDA-01168 design requires a C2000-compatible JTAG probe. Texas Instruments recommends the ultra-low-cost XDS100V2. The driver for the XDS100v2 JTAG probe is a part of various Texas Instruments software packages:

- Code Composer Studio (complete development toolchain)
- Uniflash
- controlSUITE
- TI Cloud Agent (internet browser extension for TI Cloud Tools)

Install one of these applications if the Windows operating system prompts for a driver. 図 53 shows a screenshot of the Device Manager confirming a properly installed XDS100v2 driver. Make sure that the virtual COM port (VCP) box is checked for both channels as 図 54 shows.

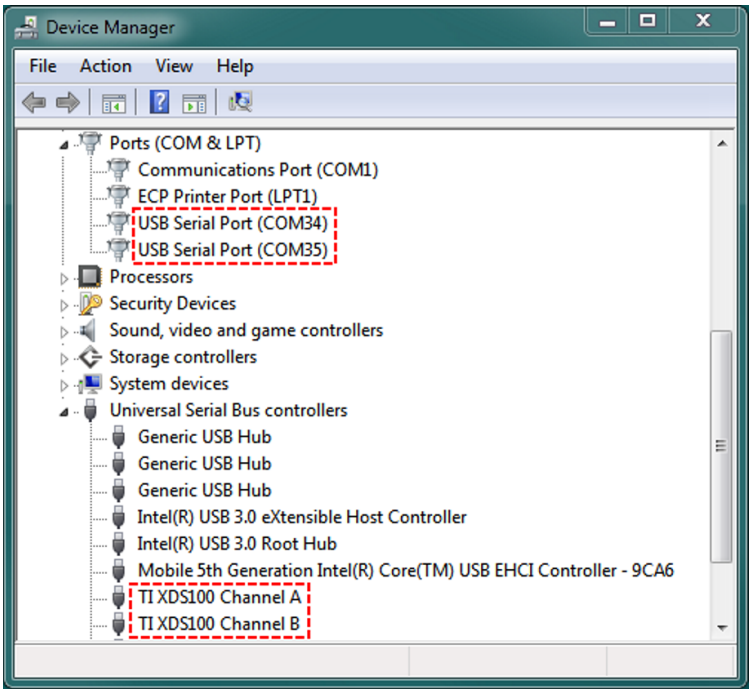


図 53. Properly Installed and Configured XDS100V2 Driver

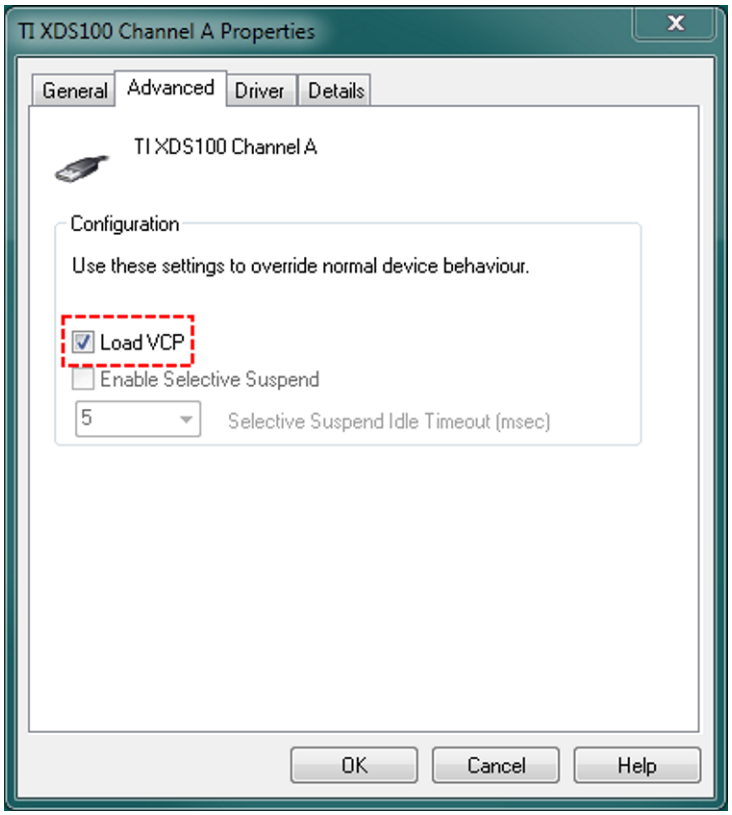


図 54. Load VCP Checkbox Enables Virtual COM Port

See the XDS100 wikipage for more information about the XDS100 or for troubleshooting.

5.3.2 Programming Microcontroller

The TIDA-01168 software package comes with a precompiled binary file. Three different tools can be used for the MCU programming:

- Code Composer Studio
- Uniflash
- Cloud-based Uniflash available on dev.ti.com

The programming procedure when using Uniflash V4 is as follows:

1. Download and install Uniflash V4 from ti.com/tool/uniflash.
2. Make sure that the JTAG probe is properly installed as described in 5.3.1.
3. Power up the board as described in 5.2.
4. Open the Uniflash software and select the MCU as shown in 図 55.
5. Select the JTAG probe as shown in 図 56.
6. Click on the *Start* button.
7. Click on the green *Browse* button and select the binary image from *TIDA-01168/Debug/TIDA-01168.out*.
8. Start programming by clicking on the *Load Image* button (図 58).
9. Check the console to confirm whether the programming is successful (図 58).

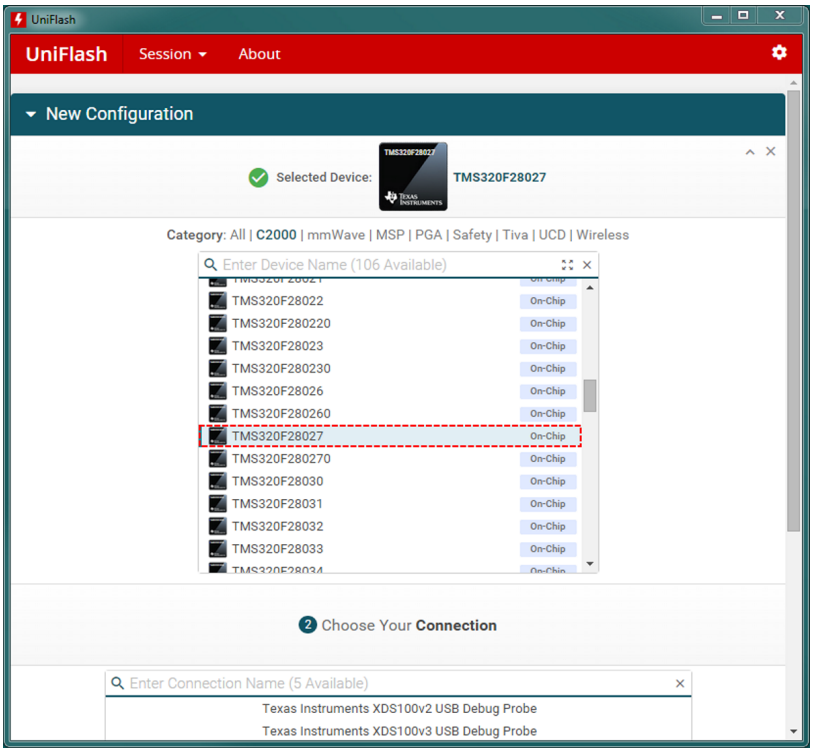


図 55. Uniflash V4—Selecting Device

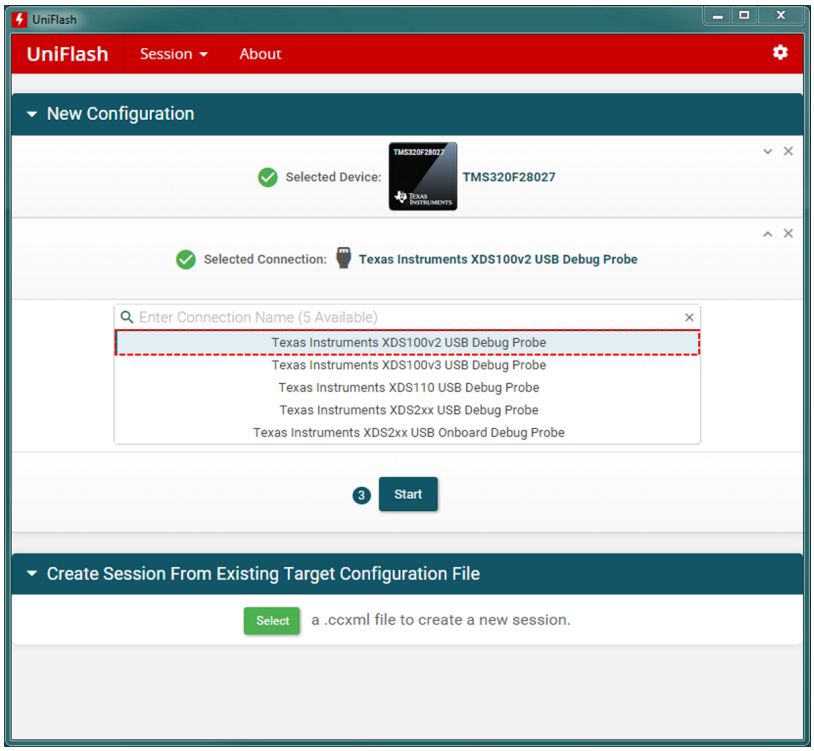


図 56. Uniflash V4—Selecting Communication Interface

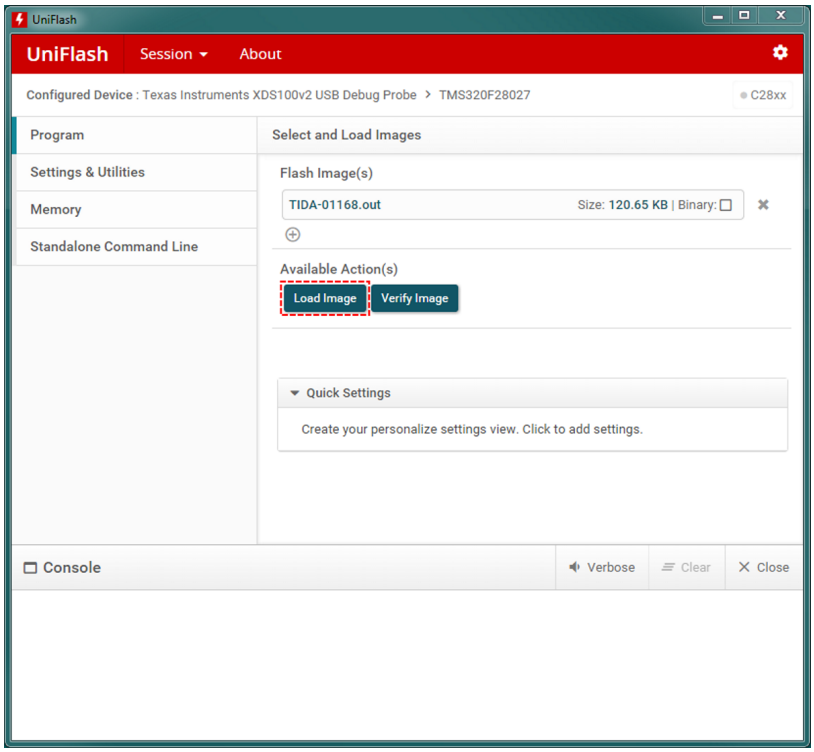


図 57. Uniflash V4—Programming

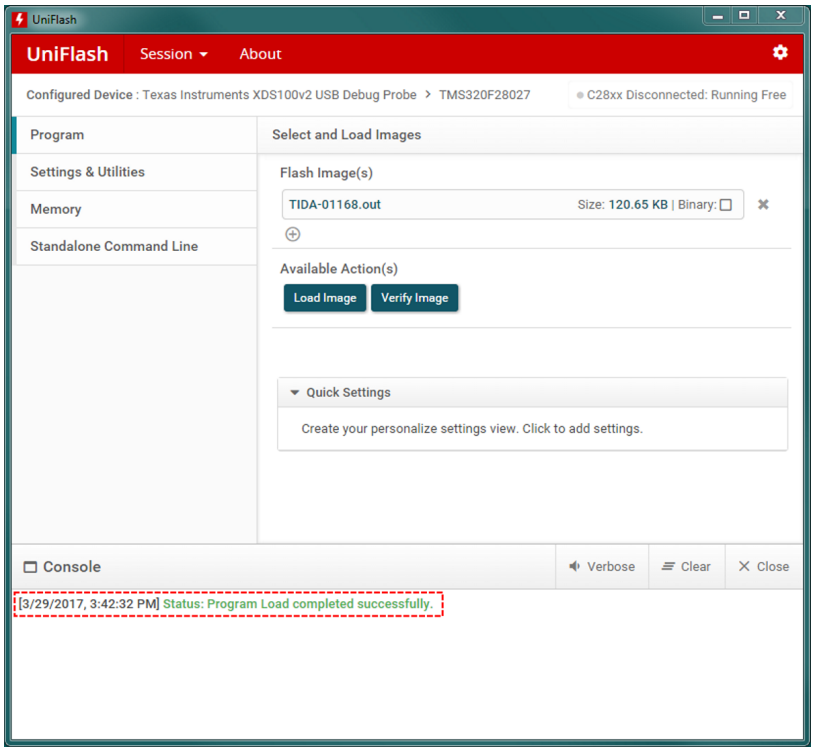


図 58. Uniflash V4—Programming Finished

注: For more information on how to modify or compile a provided source code using C2000 Compiler and Code Composer Studio visit processors.wiki.ti.com or ask on the TI E2E™ online community.

5.3.3 Using Software for TIDA-01168

The following two options are available for configuring and controlling the TIDA-01168:

- GUI Composer application (JTAG)
- Serial terminal (UART)

5.3.3.1 Using GUI Composer

GUI Composer is a cloud-based graphic user interface available on dev.ti.com. The tool uses non-intrusive JTAG access to read and write data to the MCU. System variables are displayed in the Internet browser. Google Chrome™ or Mozilla® Firefox® are the supported browsers with an additional plugin (TI Cloud Agent Bridge). Any additional communication protocol is not necessary. The user can import the project from the gallery to their workspace or download a standalone version available for various operating systems. The GUI Composer project contains the binary file and, if set properly, the file eliminates the process of programming the MCU as described in 5.3.2. The GUI Composer can program the MCU either every run or upon request from the menu.

注: The GUI Composer application is easy to use but is considered to be experimental. User experience depends on several factors such as Internet service provider (ISP) bandwidth, Internet browser, or PC hardware. TI provides absolutely no warranty for using the software.

図 59 shows the GUI Composer application.

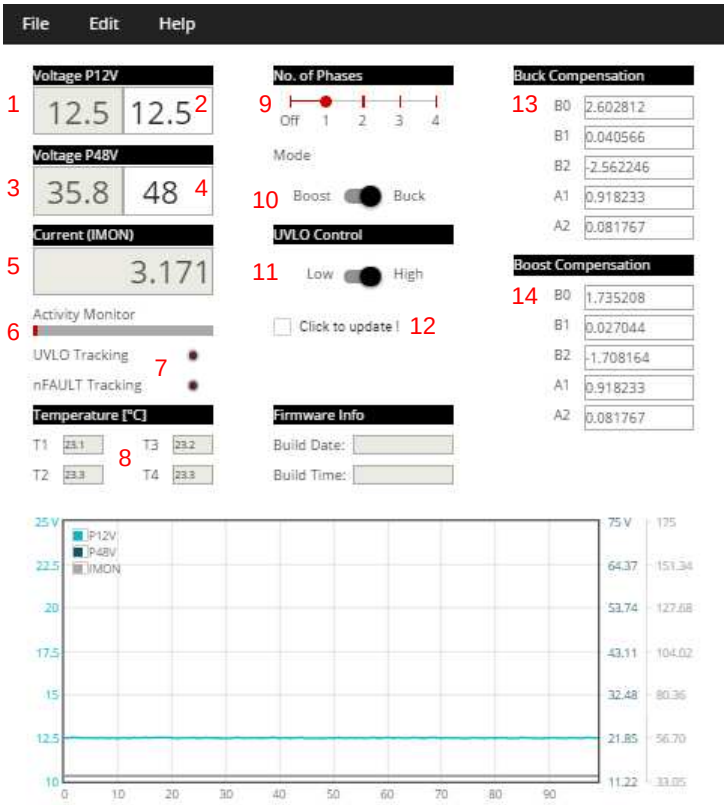


図 59. GUI Composer Application for TIDA-01168

The steps for connecting to the TIDA-01168 design using GUI Composer are as follows:

1. Make sure that the reference design has been properly turned on (see 5.2).
2. Make sure that the JTAG probe has been properly installed as described in 5.3.1.
3. Go to dev.ti.com and open TIDA-01168 from the gallery or import it to the user workspace.
4. Click on the RUN button (black triangle) from the toolbar.
5. A new window opens with the application running. Make sure that the status bar shows "target connected". The activity monitor progress-bar periodically changes value to signal MCU activity.
6. The system is ready to use.

図 59 shows the GUI Composer application controls, which are numbered as follows:

1. 12-V rail actual voltage
2. 12-V rail preset output voltage
3. 48-V rail actual voltage
4. 48-V rail preset output voltage
5. Total current flowing through all power stages (approximate value)
6. Activity monitor; value is dynamically changing
7. UVLO and NFAULT signals logic levels
8. Actual temperature for power stages 1 through 4
9. Number of active phases (requires confirmation using button 12)
10. Buck or Boost mode selector switch (requires using button 12)
11. UVLO (open collector) control (requires confirmation using button 12)

12. Update button; confirms new configuration for the control loop
13. Constants for BUCK mode digital compensator
14. Constants for BOOST mode digital compensator

All parameters are changed in the system immediately. The control loop in the MCU requires confirmation for critical parameter changes, such as *number of phases*, *UVLO level* ,or *buck/boost* operation. Any change to these parameters must always be confirmed by selecting the *click to update!* checkbox.

See the TI E2E Community forum for GUI Composer troubleshooting.

5.3.3.2 Using Serial Terminal

Serial terminal is the second option for configuring and controlling the TIDA-01168 reference design from a personal computer. A terminal software and a serial-to-USB converter are required. The Termite 3.3 software from CompuPhase is used as an example of terminal software. This software is free for personal and commercial use.

表 16 shows the serial port configuration.

表 16. Serial Port Configuration for TIDA-01168 Reference Design

PARAMETER	CONFIGURATION
Baud rate	9600
Data bits	8
Parity	None
Stop bits	1
Flow control	None
New line character	\n (0x0A)
End command with	\r (0x0D)
Logic levels	CMOS 3.3 V

Connecting to TIDA-01168 using serial interface and Termite 3.3:

1. Make sure that the system is powered up (5.2) and the MCU is preprogrammed (5.3.2).
2. Connect the serial-to-USB converter to the PC and to the board (J701, pins 4, 6, and 8). Make sure that the Rx and Tx signals are crossed and the ground is connected.
3. Download Termite 3.3 from CompuPhase and configure it as the *Serial port settings* window shows in the following 図 60. The *Port* number may vary.
4. Make sure that the terminal is not disconnected (図 61).
5. Type in the *help* command in the field at the bottom (red dashed box in 図 61) and press the ENTER key to access a menu with all the possible commands.

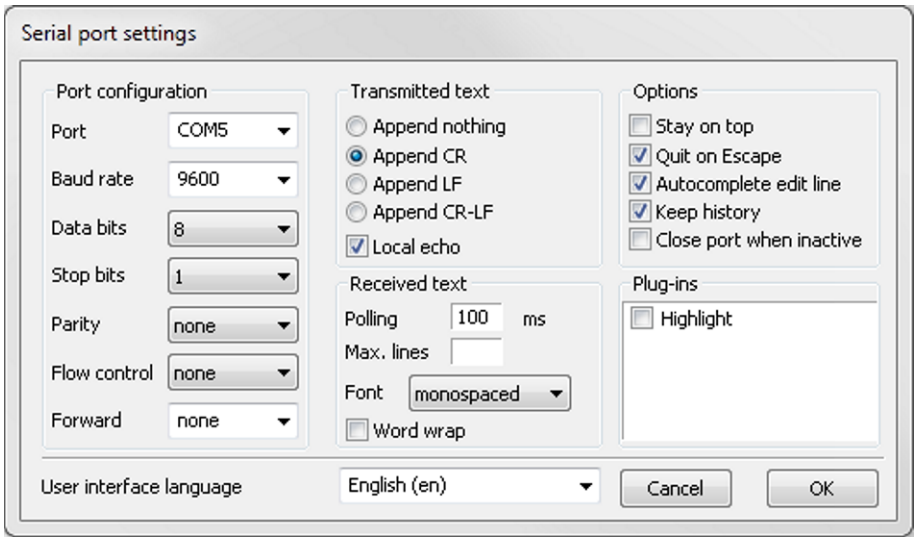


図 60. Termite 3.3 Terminal Configuration for TIDA-01168 Reference Design

図 61. Interfacing TIDA-01168 With Serial Terminal Using Termite 3.3

図 62 shows a terminal communication, which is helpful for a better understanding of the data flow. The reference design always responds with a corresponding string that shows the expected input (PRM> for a parameter and CMD> for a command). An invalid command or parameter results in error messages. 図 61 shows the list of possible commands, which can be obtained by using the *help* command. The commands description is self-explanatory.

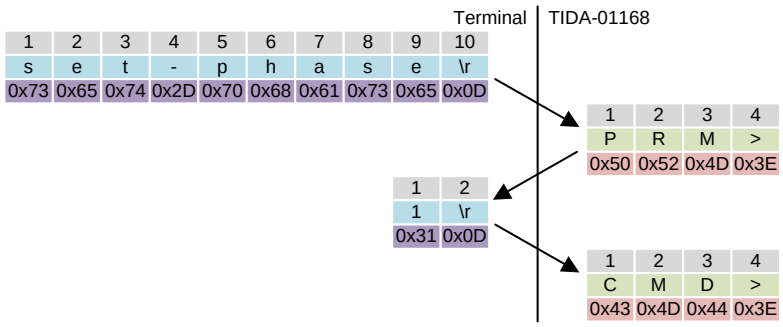


図 62. Example of Serial Communication Between Terminal and TIDA-01168

6 Testing and Results

6.1 48-V Circuit Breaker Test Data

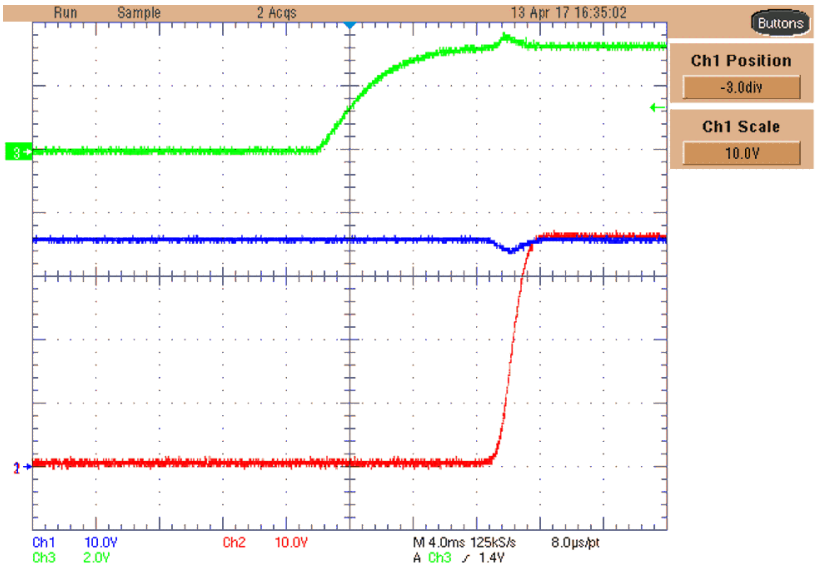


図 63. 48-V Circuit Breaker Turnon from KL40-41 Terminal (Blue = KL40-41 Terminal, Green = EN48, and Red = P48V)

6.2 Power Stages Test Data

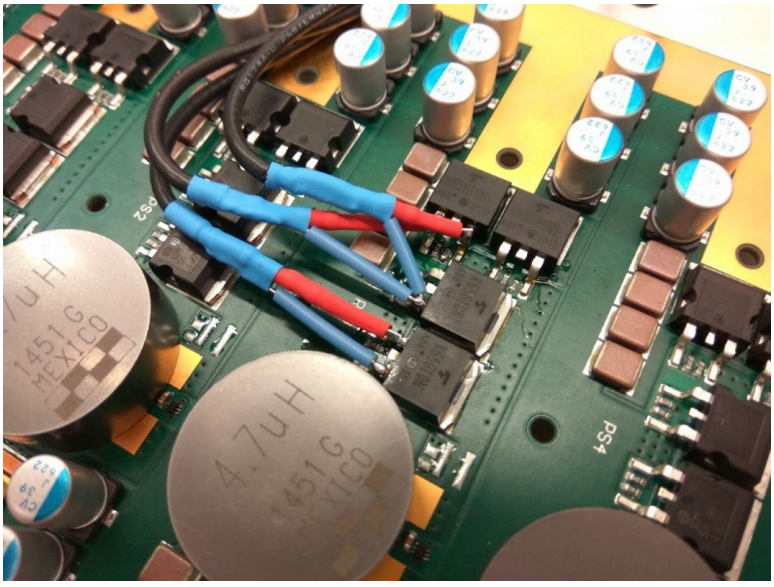


図 64. Measurement Technique for Switching Node and Gate Signals Using DIY 1:21 Passive Probe[27].

注: The gate-source voltage for the top switch is calculated in the oscilloscope because all of the channels share the same ground potential.

図 65. Switching Waveforms With Adaptive Dead-Time Settings

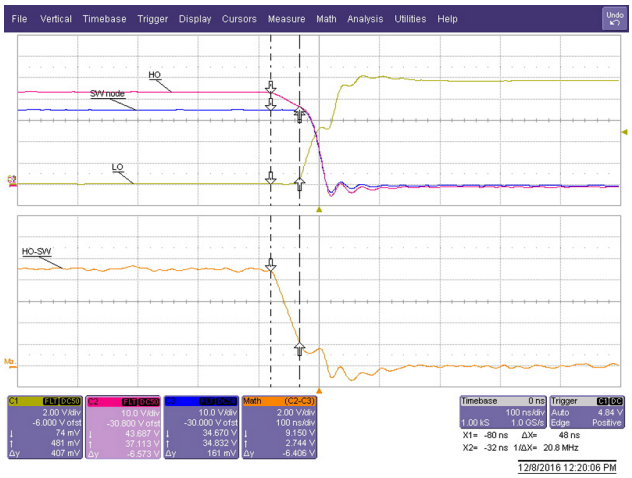


図 66. Switching Waveforms With Adaptive Dead-Time Settings (Detail)

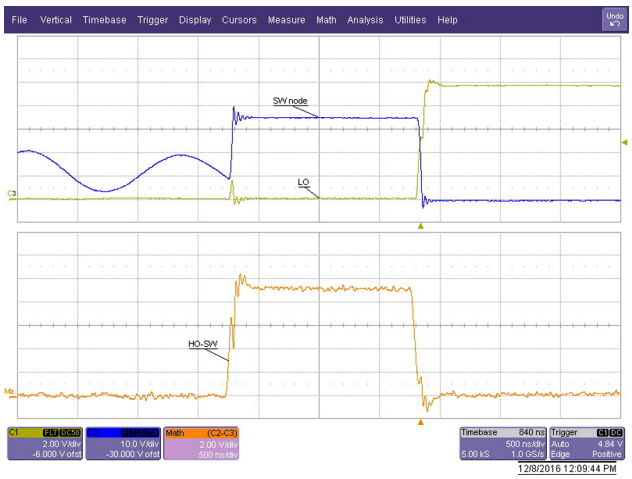


図 67. Switching Waveforms With Adaptive Dead-Time Settings (Detail)

図 68. Switching Waveforms With Fixed Dead-Time Settings (R906 = 10 k)

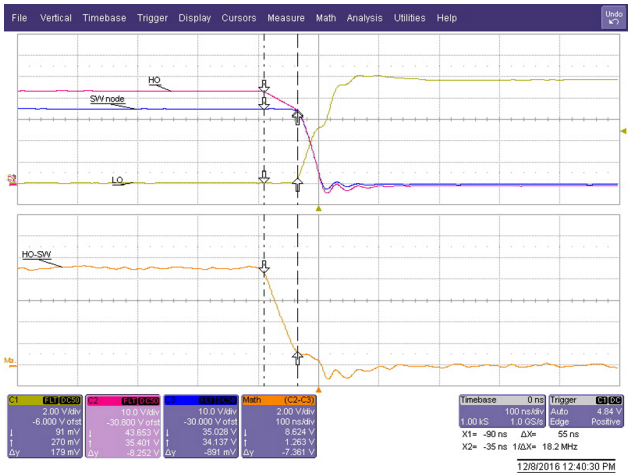


図 69. Switching Waveforms With Fixed Dead-Time Settings (R906 = 10 k) – Detail

6.3 12-V Circuit Breaker Test Data

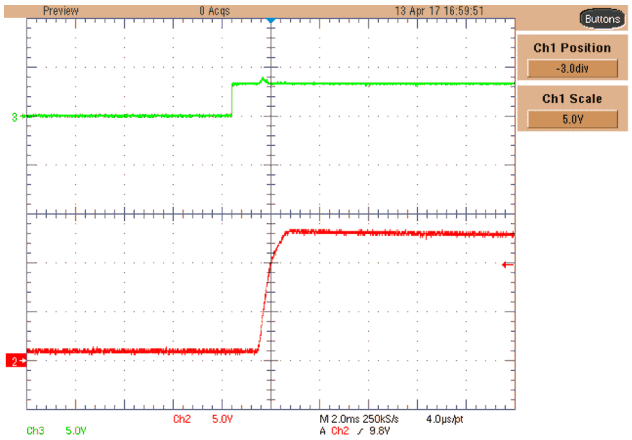


図 70. 12-V Circuit Breaker Turnon From 12-V Terminal (Green = UVLO, Red = P12V)

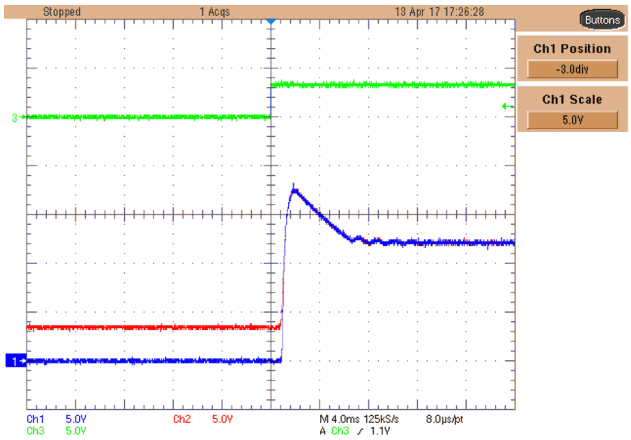


図 71. 12-V Circuit Breaker Turnon to 12-V Terminal (Blue = KL30-31 Terminal, Green = UVLO, and Red = P12V)

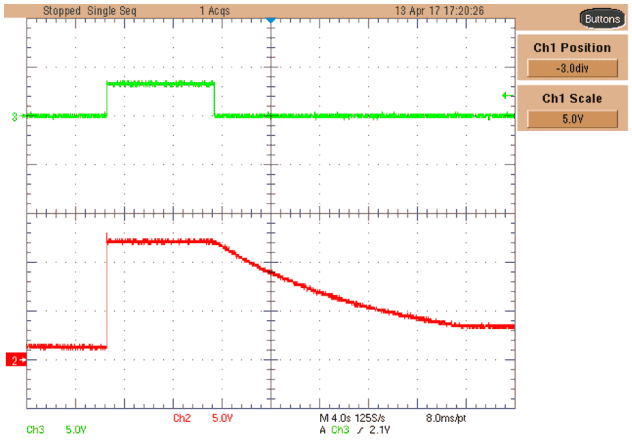


図 72. 12-V Circuit Breaker Turnoff From 12-V Terminal (Green = UVLO, Red = P12V)

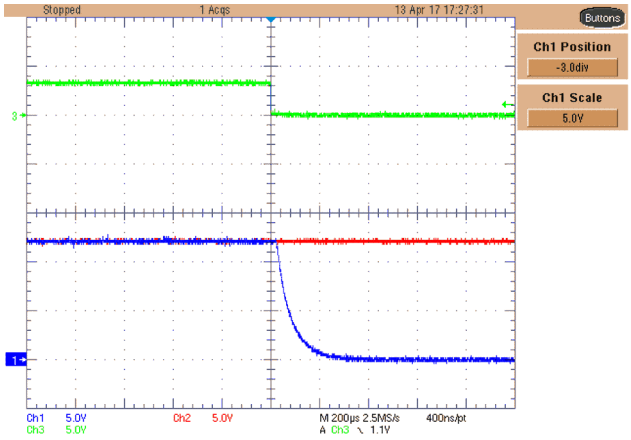


図 73. 12-V Circuit Breaker Turnoff to 12-V Terminal (Blue = KL30-31 Terminal, Green = UVLO, and Red = P12V)

6.4 LM5170-Q1 Subsystem Test Data

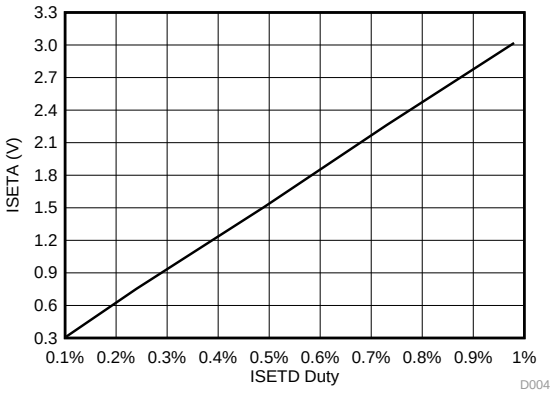


図 74. Relationship Between ISETD Duty Cycle and ISETA Voltage: C912 = 3.3 nF, f_{ISED} = 48.8 kHz

6.5 C2000™ Control MCU Test Data

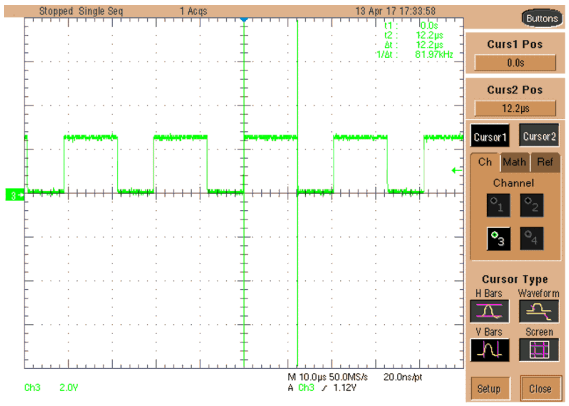


図 75. Timing of Control loop ISR Measured on Testpin ADCINB2 (D700)

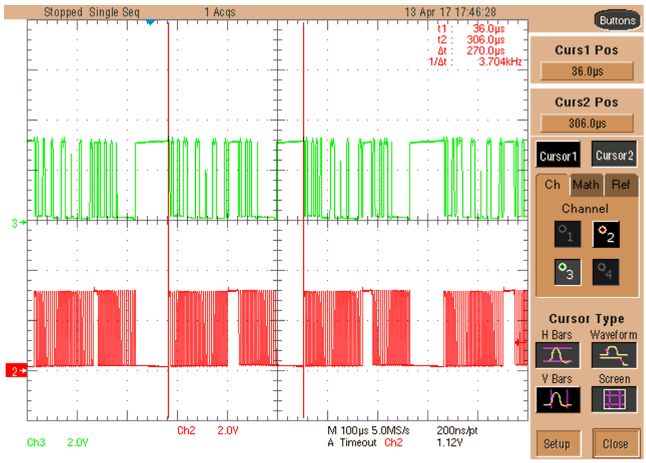


図 76. I²C Bus TMP102-Q1 Frames Timing

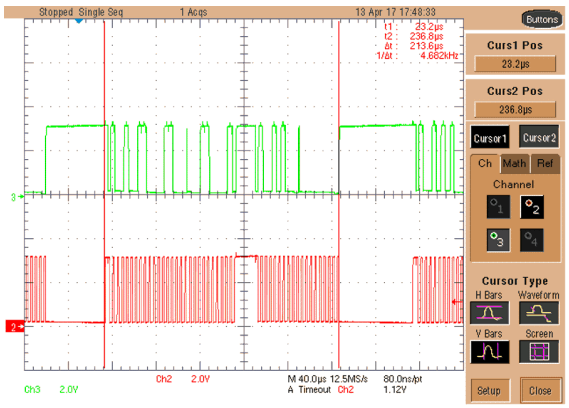


図 77. I ² C Bus TMP102-Q1 Single Frame Timing

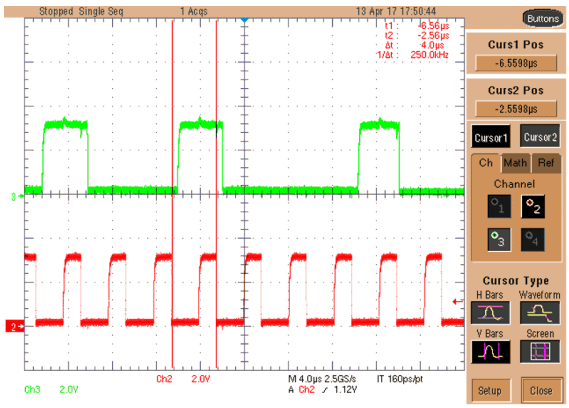


図 78. I ² C Bus TMP102-Q1 Single Frame Timing (Detail)

6.6 Diag Test Data

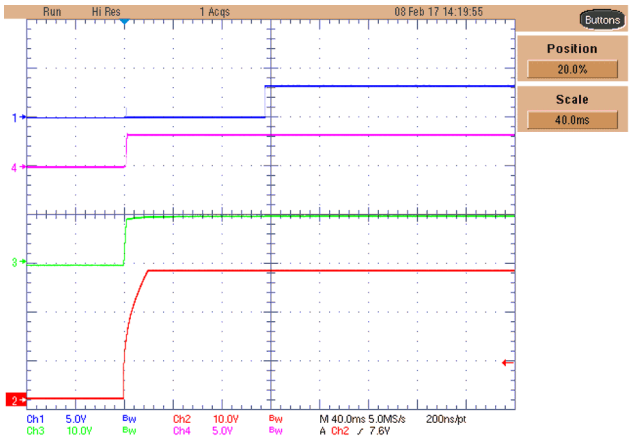


図 79. External Watchdog Behavior During Start-Up: (Blue = nRST, Violet = P3V3, Green = P10V, and Red = VIN_LM)

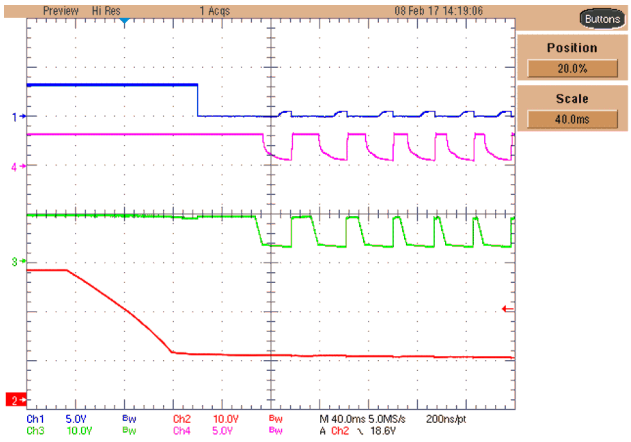


図 80. External Watchdog Behavior During Shutdown: (Blue = nRST, Violet = P3V3, Green = P10V, and Red = VIN_LM)

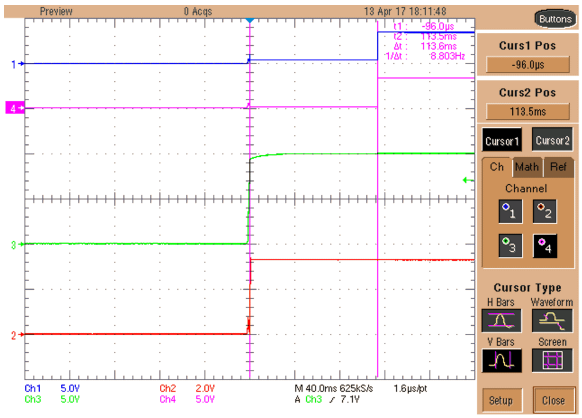


図 81. External Watchdog Behavior During Start-Up: (Blue = nRST, Violet = NSHDN, Green = P10V, and Red = P3V#)

6.7 Bias Supplies Test Data

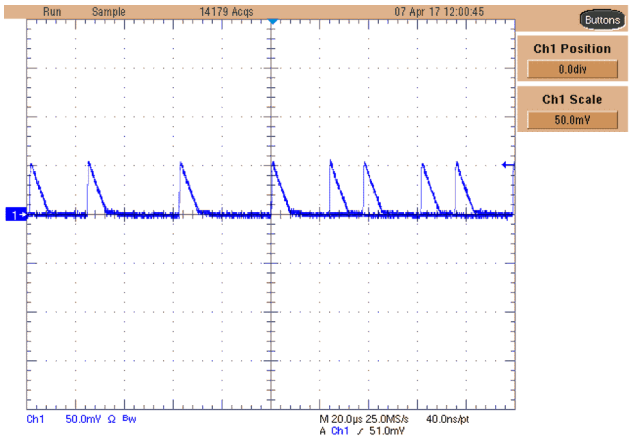


図 82. MC33063A-Q1 Pre-Boost Converter Output Ripple at 50 mA

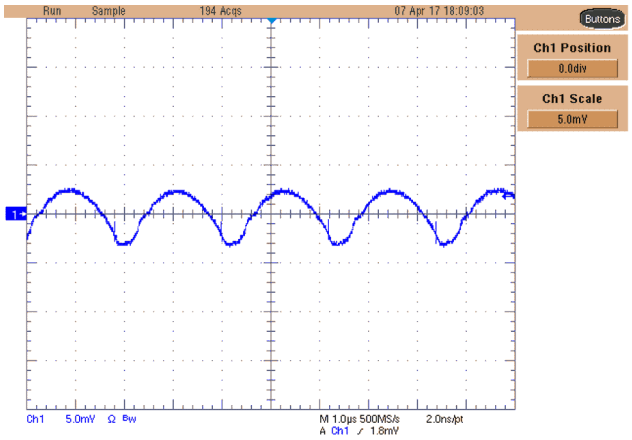
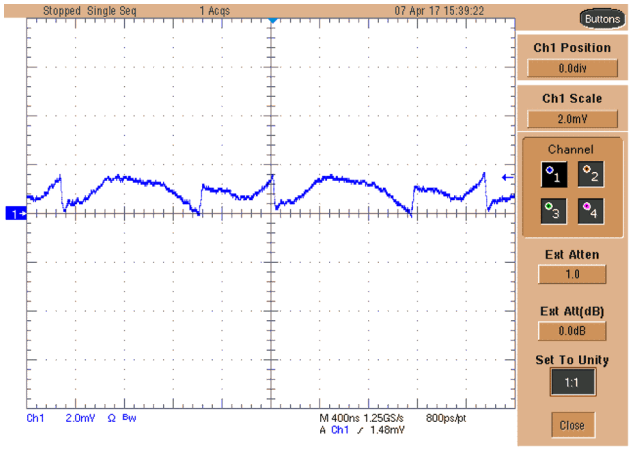


図 83. LM5010A-Q1 Step-Down Converter Output Ripple in CCM Mode



Note the effect of ESL of the output capacitors and the very fine oscilloscope vertical amplifier settings.

図 84. TPS560200-Q1 Step-Down Converter Output Ripple in CCM Mode

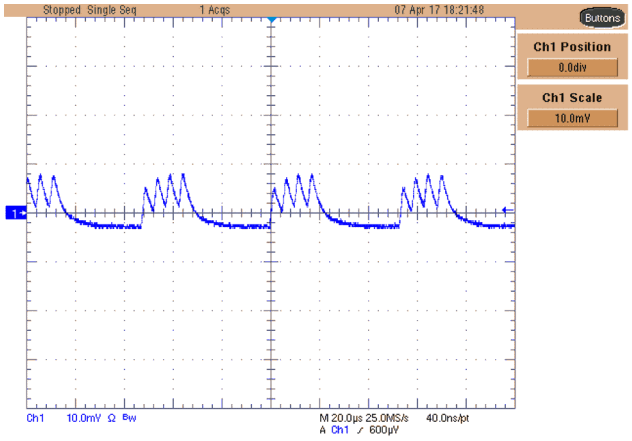


図 85. TPS560200-Q1 Step-Down Converter Output Ripple at 10-mA Light-Load Operation

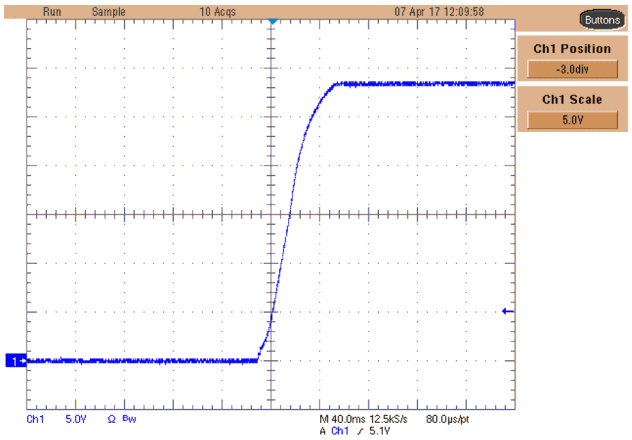


図 86. MC33063A-Q1 Pre-Boost Converter Start-Up Behavior to 650-Ω Load

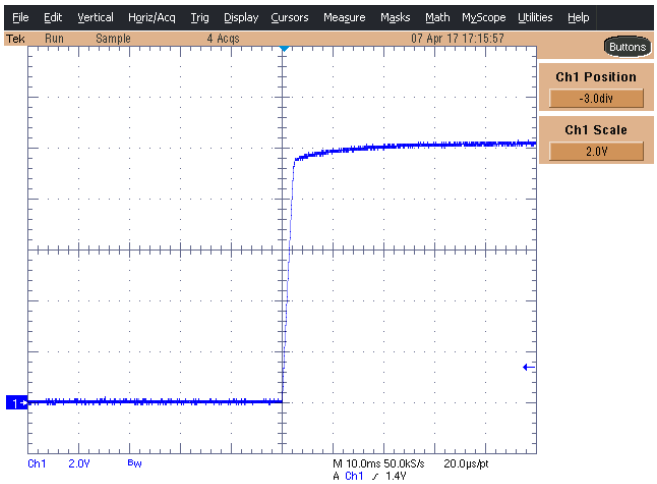


図 87. LM5010A-Q1 Step-Down Converter Start-Up Behavior to 200-Ω Load

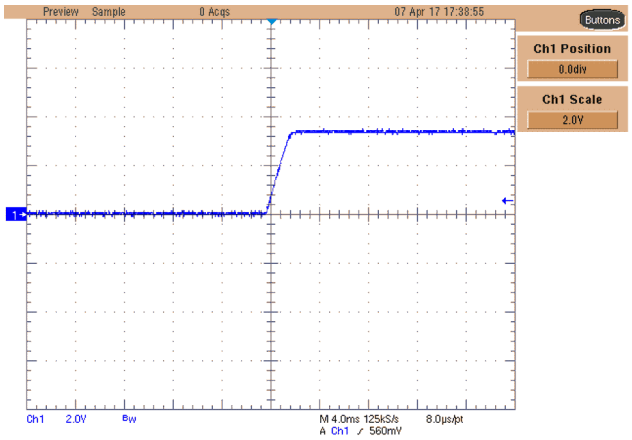


図 88. TPS560200-Q1 Step-Down Converter Start-Up Behavior to 66-Ω Load

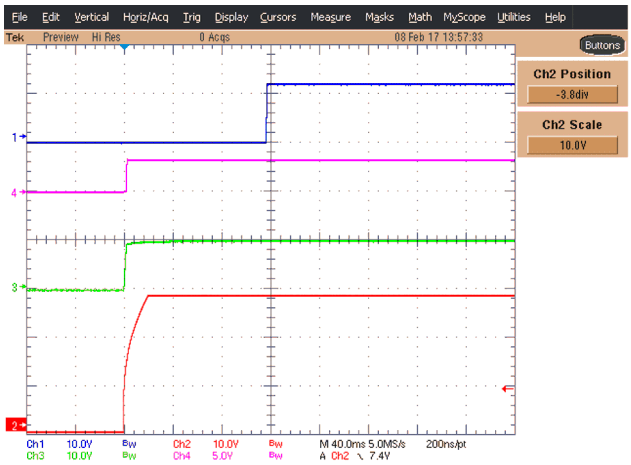


図 89. Start-Up Behavior of All Bias Power Supplies—Start Initiated by EN12 From 12-V Battery Terminal: (Blue = P12V, Violet = P3V3, Green = P10V, and Red = VIN_LM)

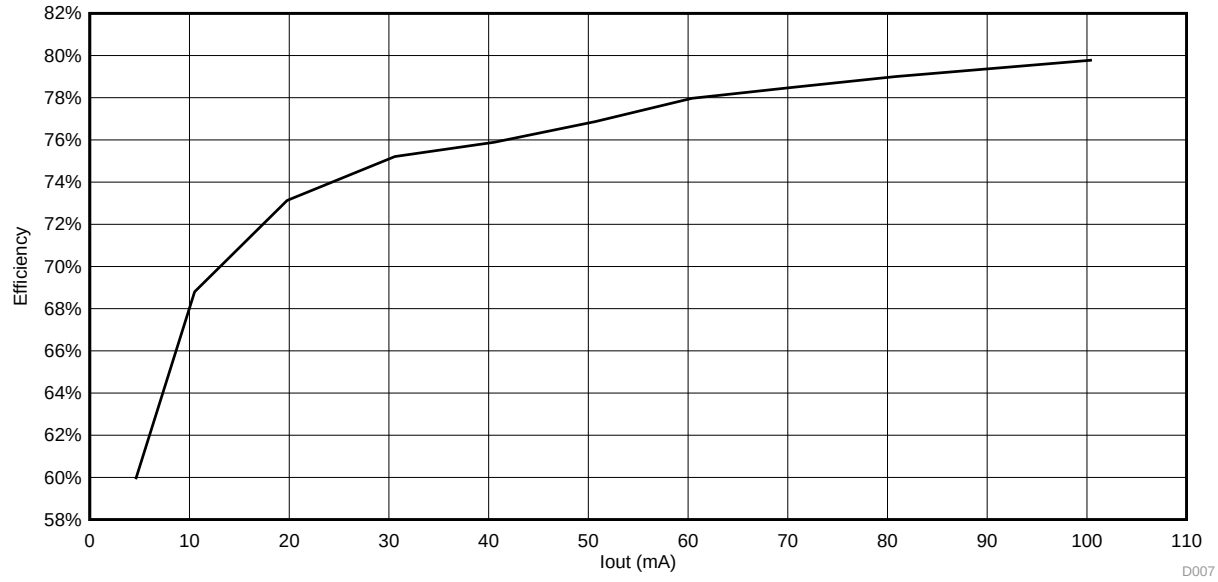


図 90. Efficiency Plot for MC33063A-Q1 Pre-Boost Converter V_{IN} = 12 V, V_{OUT} = 28 V

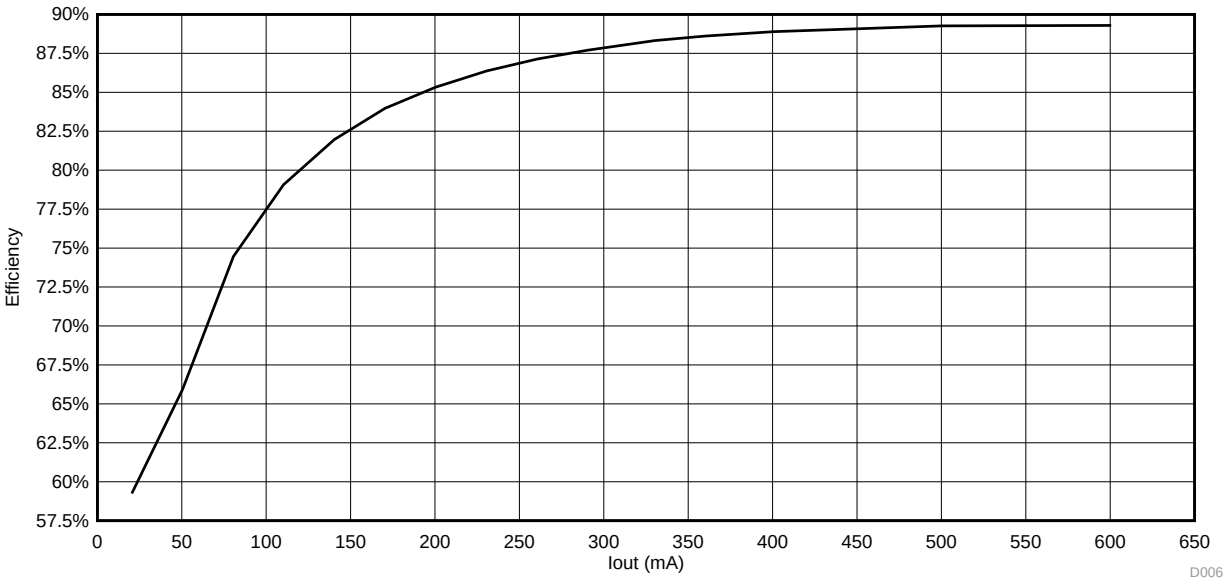


図 91. Efficiency Plot for LM5010A-Q1 Step-Down Converter V_{IN} = 48 V, V_{OUT} = 10 V

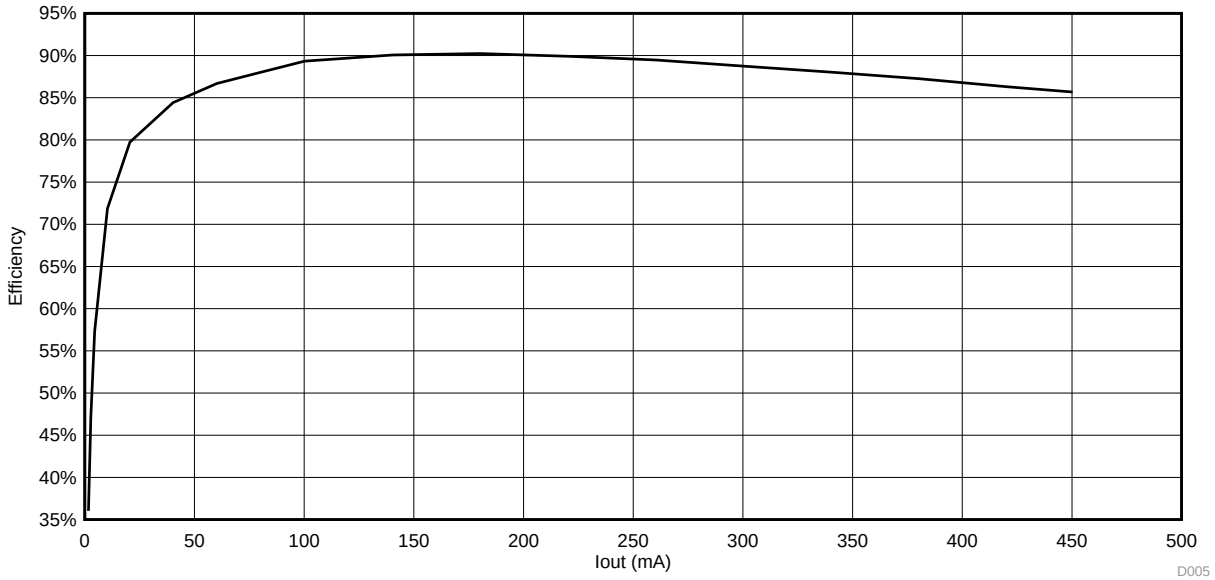


図 92. Efficiency Plot for TPS560200-Q1 Step-Down Converter V_{IN} = 10 V, V_{OUT} = 3.3 V

7 Design Files

7.1 Schematics

To download the schematics, see the design files at TIDA-01168.

7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01168.

7.3 Altium Project

To download the Altium project files, see the design files at TIDA-01168.

7.4 Gerber Files

To download the Gerber files, see the design files at TIDA-01168.

7.5 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01168.

8 Software Files

To download the software files, see the design files at TIDA-01168.

9 List Of Recommended Modifications

Increase the spacing between the heat sink and the KL40, KL41, KL30, and KL31 terminals. Optimize the mechanical construction for bigger cable lugs (see 図 93).

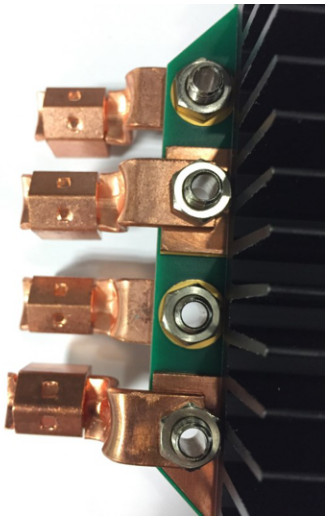


図 93. KL30, KL31, KL40, and KL41 Terminal Spacing

Change the diameter of the holes for M3 screws in the PCB to 3.81 mm. This adjustment allows placement of TO-220 isolation spacers through the complete assembly (top copper bus bars, PCB, bottom copper bus bars), as shown in 図 94.

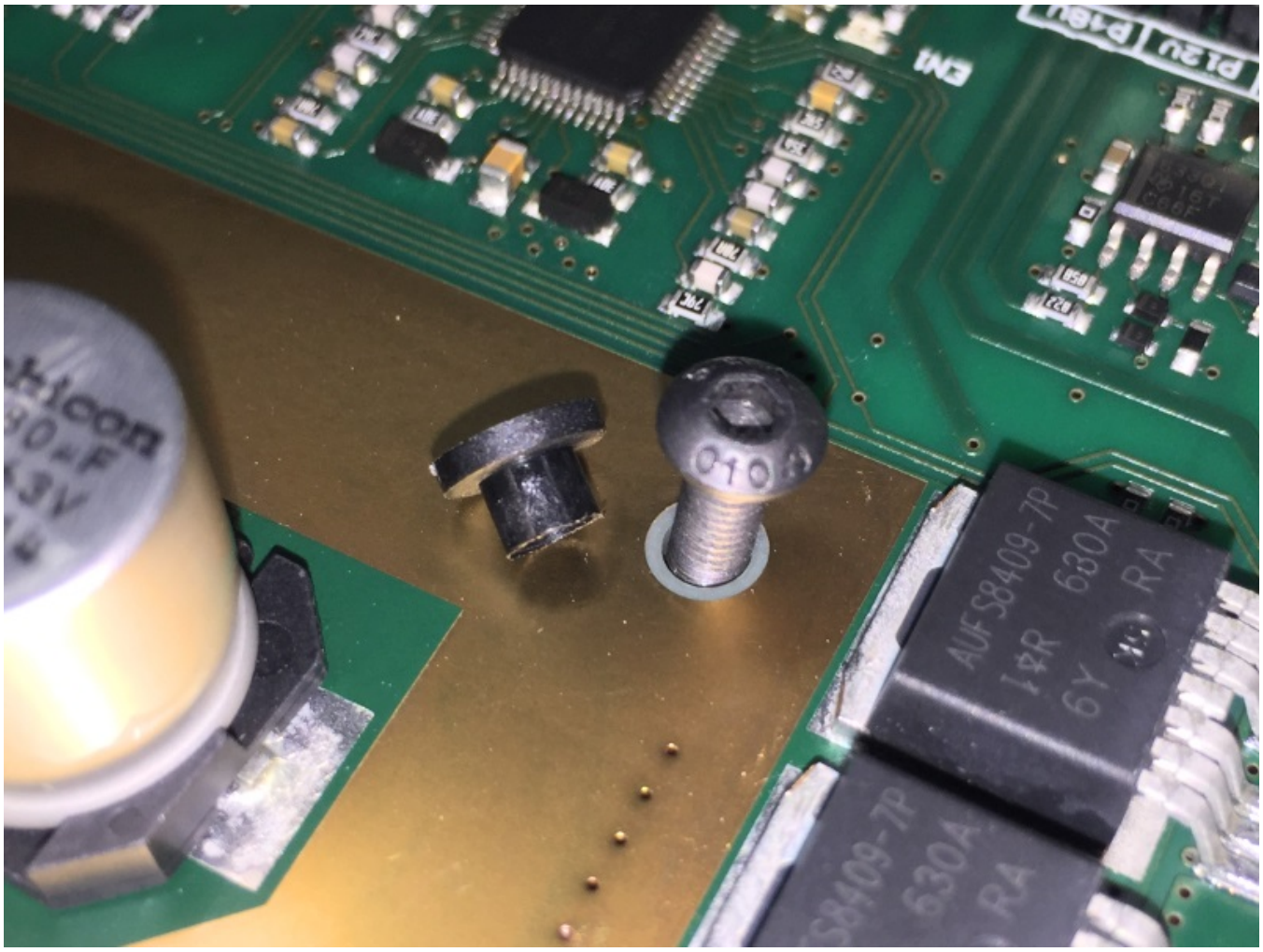


図 94. Hole for M3 Screw and Isolation Spacer

A Wurth inductor 74436410470 in the position of L300 is preferred for initial testing.

Testing during development shows that, under certain conditions (high output current, four-phase operation), the I^2C temperature sensors randomly fail to send ACK to the bus. This occurrence happens approximately six times per hour due to noise on the I^2C bus. Current firmware is able to recover from such event. Texas Instruments recommends careful selection of temperature sensors which are in close proximity to the power stage. Behavior can be improved using better PCB layout techniques, filtering, or choosing a communication bus that is more durable against impulse noise (SPI).

10 Related Documentation

1. Texas Instruments, *48V systems: Design considerations for a typical auxiliary power inverter*, TI E2E™ Online Community Forum – Behind the Wheel; July 2015 (https://e2e.ti.com/blogs_/b/behind_the_wheel/archive/2015/07/08/48v-systems-design-considerations-for-a-typical-auxiliary-power-inverter)
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4. Texas Instruments, *LM5010A, LM5010A-Q1 High-Voltage 1-A Step-Down Switching Regulator*, LM5010A/LM5010A-Q1 Data Sheet (SNVS376)
5. Texas Instruments, *C28x IQmath Library*, Software Module User's Guide (SPRC990)
6. Texas Instruments, *Modeling Bi-Directional Buck/Boost Converter for Digital Control Using C2000 Microcontrollers*, Application Report (SPRABX5)
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11. Verband der Automobilindustrie e. V., *Electric and Electronic Components in Motor Vehicles 48 V On-Board Power Supply Requirements and Tests*, VDA-320 Publication
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13. EDN.com; Hegarty, Tim; *Voltage-mode control and compensation: Intricacies for buck regulators*, EDN Network How To Article, 2008 (http://www.edn.com/design/analog/4326882/Voltage-mode-control-and-compensation-Intricacies-for-buck-regulators)
14. Ahonen, Janne, *A wideband 1:21 DIY 1 kΩ oscilloscope probe*, Online Publication (http://jahonen.kapsi.fi/Electronics/DIY%201k%20probe/)
15. Biricha DigitalPower Ltd, *Designing Stable Digital Power Supplies*, Seminar Presentation, 2011 (https://www.omicron-lab.com/fileadmin/assets/support/Presentation_-_Mr._Ali_Shirsavar.pdf)
16. Texas Instruments, *Demystifying Type II and Type III Compensators Using OpAmp and OTA for DC/DC Converters*, Application Report (SLVA662)
17. Texas Instruments, *Digital Peak Current Mode Control With Slope Compensation Using the TMS320F2803x ,* Application Report (SPRABE7)

11 Terminology

ESR— Equivalent series resistance

SAR— Successive approximation register

PWM— Pulse-width modulation

ESL— Equivalent series inductance

DCR— DC resistance

EMI— Electromagnetic interference

ADC — Analog-to-digital converter

LDO— Low-dropout

IC— Integrated circuit

SBC— System basis chip

ISP— Internet service provider

VCP— Virtual COM port

OS — Operating system

PC— Personal computer

CCM— Constant conduction mode

DCM— Discontinuous mode

12 About the Author

JIRI PANACEK is a systems engineer in the Powertrain Automotive Systems team at Texas Instruments where he develops reference designs. Jiri has five years of field experience in the industrial automation and most recently the EV/HEV automotive segment. Jiri earned his master's degree in microelectronics from the Brno University of Technology in the Czech Republic.

A special thank you goes out to Garrett Roecker and Youhao Xi for their support during the development of the TIDA-01168 reference design.

改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

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