参考資料

TI Designs: TIDA-00461
MSP430™ FRAMテクノロジの活用によるIO-Linkファームウェア更新のリファレンス・デザイン

TEXAS INSTRUMENTS

概要

インダストリー4.0の範囲において、センサやアクチュエータはエンド・ツー・エンドの自動化ネットワークのプロセスにアクティブに関与するようになりました。IO-Linkは、システム制御と現場レベルとの間で通信を行うための、新たなオプションを提供します。今日では、最も小さいセンサでも、強力なマイクロコントローラと、数千行のソフトウェア・コードを内蔵しています。バグ修正や、新しい機能を有効にするなどの目的で、ファームウェアの更新が必要になることもあります。このリファレンス・デザインでは、MSP430™マイクロコントローラとFRAMテクノロジを使用して、フラッシュ・メモリ付きMCUを使用する代わりに、IO-Linkによりファームウェアを更新する場合の利点を紹介します。

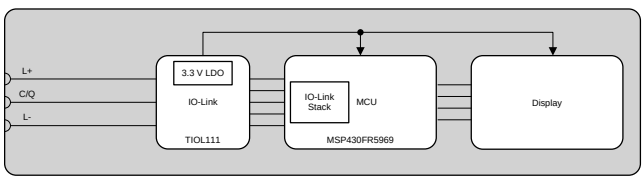
- FRAMの更新は100倍も高速で、事前消去が不要
- データをIO-Linkチャネルからそのまま FRAMに書き込むことができ、バッファリングが不要
- 書き込み中にCPUが占有されず、割り込みのブロックも不要
- 電源障害が発生してもデータが消失しない

リソース

TIDA-00461	デザイン・フォルダ
MSP430FR5969	プロダクト・フォルダ
TIOL111	プロダクト・フォルダ
430BOOST-SHARP96	ツール・フォルダ

TI E2E™ Community

E2Eエキスパートに質問



特長

- FRAMによりBLOB転送とファームウェア更新を簡単、高速、安全に実行
- IPカプセル化モジュール: メモリの一部を望まない読み出しから保護
- ±65Vの過渡耐性、100µs未満
- L+、CQ、L-に55Vまでの逆極性保護を搭載
- L+およびCQにEMC保護を搭載
  - ±16kV IEC 61000-4-2 ESD接触放電
  - ±4kV IEC 61000-4-4電気的高速過渡
  - ±1.2kV/500Ω IEC 61000-4-5サージ
- IO-Link仕様v1.1に準拠 (IO-Linkスタック・ソフトウェアはTEConceptから)
- IO-LinkプロファイルのBLOB転送およびファームウェア更新V1.0に準拠

アプリケーション

- 産業用
- ファクトリ・オートメーションとプロセス制御
- フィールド・トランスミッタおよびフィールド・アクチュエータ

1 System Description

Industrial sensors and field transmitters are an important part of the factory automation and process control industries. Digital interfaces like IO-Link on the sensor and actuator level offer advantages when it comes to maintenance and repair in addition to providing seamless communication and improved interoperability. Even for sensors and actuators, it might be necessary to do a firmware update in times of Industry 4.0. In 2016, the IO-Link community has published a new profile that supports firmware updates through the IO-Link interface. This profile is fully compliant to the IO-Link V1.1 specification.

The IO-Link firmware update reference design TIDA-00461 demonstrates the advantages when using an MSP430 microcontroller with FRAM technology for firmware updates with IO-Link instead of using a microcontroller with flash memory. This TI Design uses the MSP430FR5969 microcontroller with FRAM and the new TIOL111 IO-Link PHY. The reference design features the Sharp LCD BoosterPack™ (430BOOST-SHARP96) mounted on the board.. To demonstrate the BLOB transfer and firmware update, different pictures can be loaded through IO-Link to the MSP430 FRAM memory. The different downloaded pictures can be then shown on the Sharp LCD, which is on the connected BoosterPack.

The built-in IP encapsulation capability (IPE) of the MSP430 FRAM device can be used to protect critical pieces of code, configuration data, or secret keys in FRAM memory from being easily accessed or viewed.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	DESCRIPTION
POWER SUPPLY AND PROTECTION	
Operating supply voltage (L+ to L–)	7- to 36-V DC
LDO output voltage	3.3 V
LDO output current	20 mA
Reverse polarity protection	±55 V
Integrated protection	±8-kV IEC 61000-4-2 (ESD) Contact Discharge
	±2-kV IEC 61000-4-4 (EFT) Criterion A (5/50 ns)
	±1-kV/500-Ω IEC 61000-4-5 (Surge) (1.2/50 µs)
Fault indicator	Temperature
	Power
	Current
USER INTERFACE	
RGB LED	User definable LEDs through MSP430
Power LED (green)	Power indicator (3.3 V)
2× LED (green)	User definable LEDs through MSP430
2× buttons	User definable buttons through MSP430
IO-LINK	
IO-Link version	v1.1
Baud rate	COM1, COM2, COM3
Firmware update profile	v1.0

2 System Overview

2.1 Block Diagram

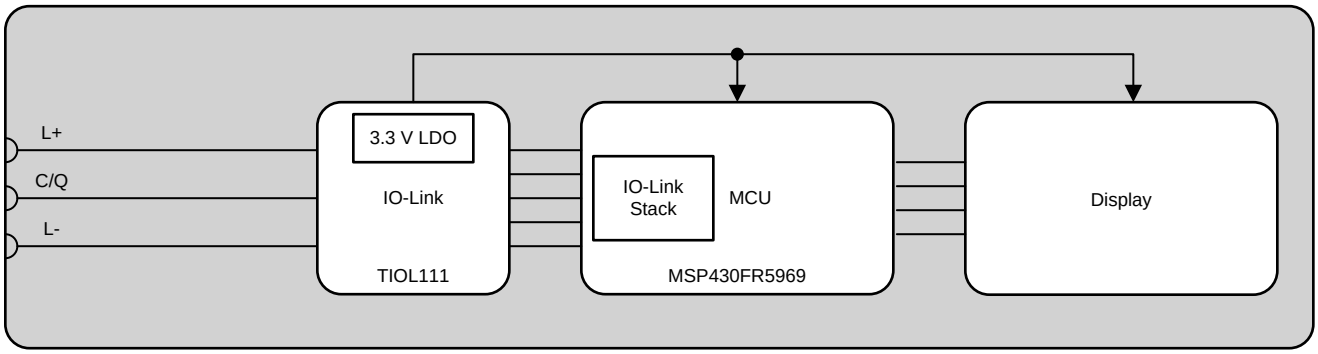


図 1. TIDA-00461 Block Diagram

2.2 Highlighted Products

The following subsections detail each circuit block in the TIDA-00461 block diagram. The TIOL111 has been chosen as the newest Texas Instruments transceiver device enabling IO-Link communication. The MSP430FR5969 has been chosen for its integrated FRAM memory. FRAM offers several advantages over traditional memory technologies such as flash, including faster write speeds, unified memory, and low-energy writes, and there is no need for pre-erasing. For more information on each of these devices, see their respective product folders at TI.com.

注: Depending on the application needs, a different MSP430 FRAM device can be used to run the application. There is a variety of smaller memory or higher integration or performance level MSP430 FRAM devices fitting the application needs.

2.2.1 MSP430FR5969

The Texas Instruments MSP430 family of ultra-low-power MCUs consists of several devices that feature different combinations of peripherals targeted for various applications. Combined with extensive low-power modes, the architecture is optimized to achieve extended battery life in portable measurement applications. The MSP430 MCU features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows the MCU to wake up from low-power modes to active mode typically in less than 10 µs.

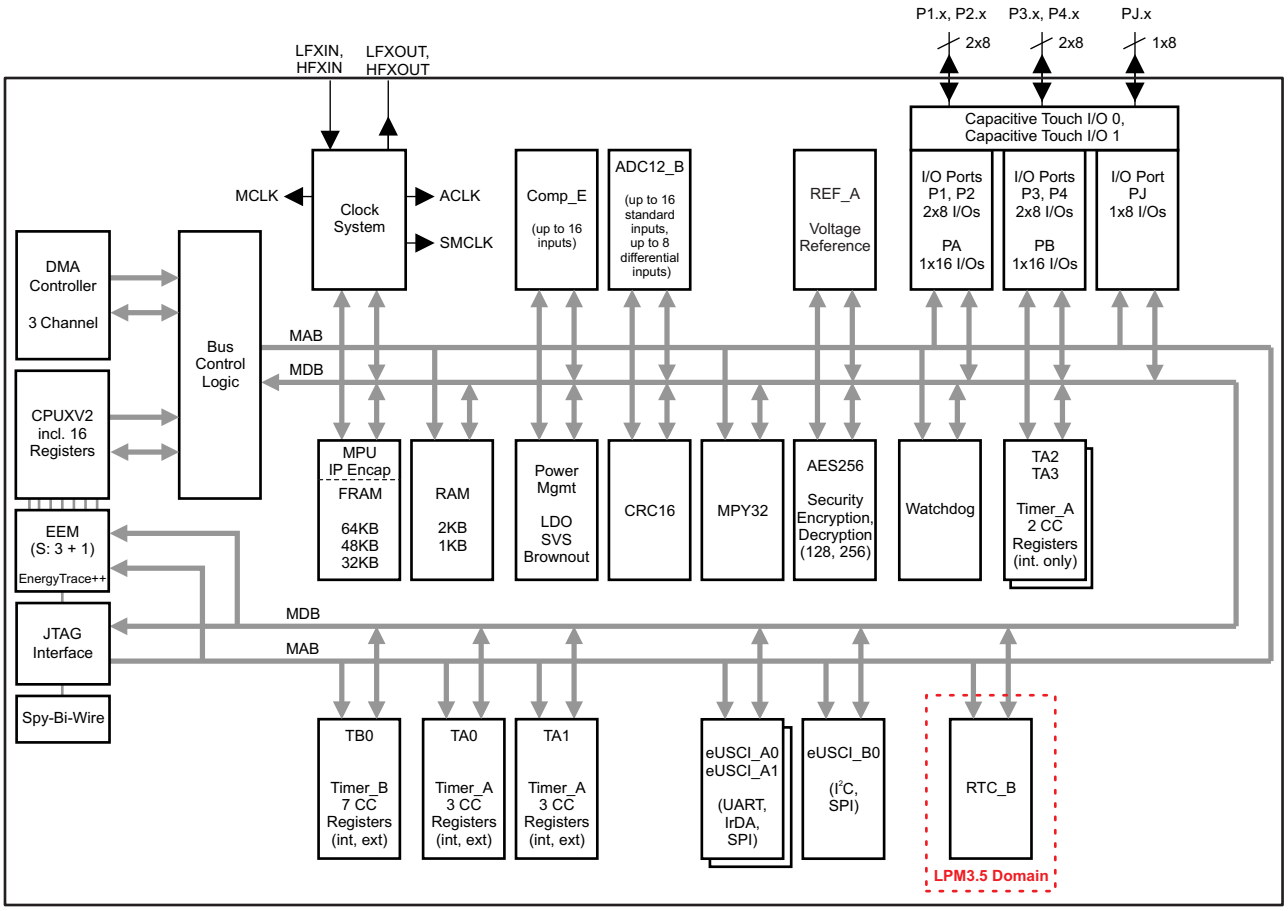


図 2. MSP430FR5969 Block Diagram

Key features of this device include:

- Embedded microcontroller:
  - 16-bit RISC architecture up to 16-MHz clock
  - Wide supply voltage range (1.8 to 3.6 V)
- Optimized ultra-low-power modes:
  - Active mode: Approximately 100 µA/MHz
  - Standby (LPM3 With VLO): 0.4 µA (typical)
  - Real-time clock (RTC; LPM3.5): 0.25 µA (typical)
  - Shutdown (LPM4.5): 0.02 µA (typical)
- Ultra-low-power FRAM:

  - Up to 64KB of nonvolatile memory
  - Ultra-low-power writes
  - Fast Write at 125 ns per word (64KB in 4 ms)
  - Unified memory = Program + Data + Storage in one single space
  - 1015 write cycle endurance
  - Radiation resistant and nonmagnetic
- Intelligent digital peripherals:
  - 32-bit hardware multiplier (MPY)
  - Three-channel internal DMA
  - RTC with calendar and alarm functions
  - Five 16-bit timers with up to seven capture/compare registers each
  - 16-bit cyclic redundancy checker (CRC)
- High-performance analog:
  - 16-channel analog comparator
  - 12-bit analog-to-digital converter (ADC) with internal reference and sample-and-hold and up to 16 external input channels
- Multifunction input/output ports:
  - All pins support capacitive touch capability with no need for external components
  - Accessible bit-, byte-, and word-wise (in pairs)
  - Edge-selectable wake from LPM on all ports
  - Programmable pullup and pulldown on all ports
- Code security and encryption:
  - 128-bit or 256-bit AES security encryption and decryption coprocessor
  - Random number seed for random number generation algorithms
- Enhanced serial communication:
  - eUSCI_A0 and eUSCI_A1 support:
    - UART with automatic baud-rate detection
    - IrDA encode and decode
    - SPI at rates up to 10 Mbps
  - eUSCI_B0 supports:
    - I^2C with multiple slave addressing
    - SPI at rates up to 8 Mbps
  - Hardware UART and I^2C Bootstrap Loader (BSL)
- Flexible clock system:
  - Fixed-frequency DCO with 10 selectable factory-trimmed frequencies
  - Low-power low-frequency internal clock source (VLO)
  - 32-kHz crystals (LFXT)
  - High-frequency crystals (HFXT)

For complete module descriptions, see the MSP430FR59xx family user's guide[2] (SLAU367).

2.2.2 TIOL111

The robust TIOL111 family of transceivers implements the IO-Link interface for industrial point-to-point communication. These devices are capable of withstanding up to 1 kV (500 Ω) of IEC 61000-4-5 surge and feature integrated reverse polarity protection.

A simple pin-programmable interface allows easy interfacing to the controller circuits. The output current limit can be configured using an external resistor.

Fault reporting and internal protection functions are provided for undervoltage, short-circuit current, and overtemperature.

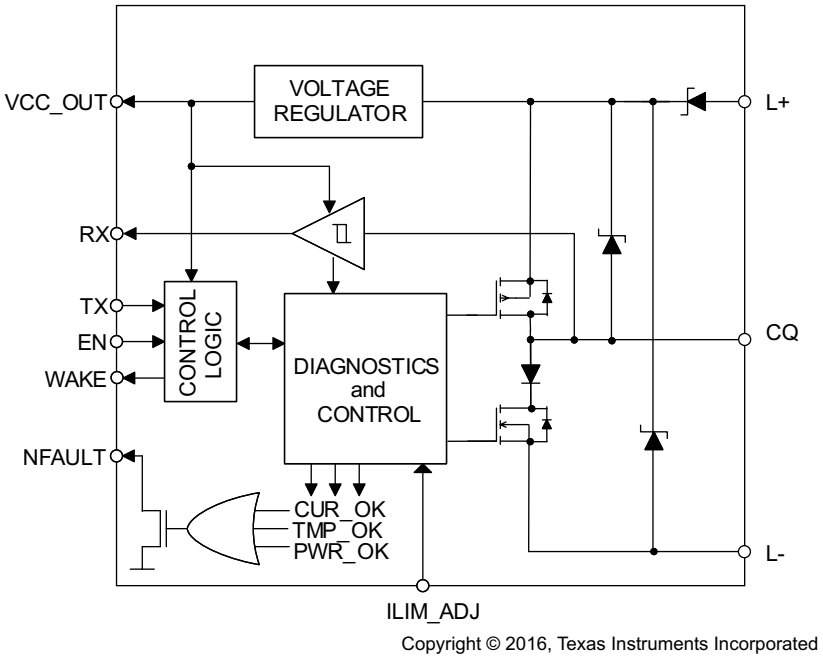


図 3. TIOL111 Block Diagram

Key features of this device include:

- 7- to 36-V supply voltage
- PNP, NPN, or IO-Link configurable output
- IEC 61131-9 COM1, COM2 and COM3 data rate support
- Low residual voltage of 1.75 V at 250 mA
- 50- to 350-mA configurable current limit
- Tolerant to ±65-V transients < 100 µs
- Reverse polarity protection of up to 55 V on L+, CQ, and L–
- Integrated EMC protection on L+ and CQ:
  - ±16-kV IEC 61000-4-2 ESD Contact Discharge
  - ±4-kV IEC 61000-4-4 Electrical Fast Transient
  - ±1.2-kV/500-Ω IEC 61000-4-5 Surge
- Fast demagnetization of inductive loads up to 1.5 H
- Large capacitive load driving capability

- < 2-µA CQ leakage current
- < 1.5-mA quiescent supply current
- Integrated LDO options for up to 20-mA current:
  - TIOL111: No LDO
  - TIOL111-3: 3.3-V LDO
  - TIOL111-5: 5-V LDO
- Overtemperature warning and thermal protection
- Remote wake-up indicator
- Fault indicator
- Extended ambient temperature: –40°C to 125°C
- 2.5-mm×3–mm 10-pin VSON package

2.3 System Design Theory

2.3.1 IO-Link

IO-Link is a serial digital communication protocol intended to be used in automation technology. This protocol connects sensors or actuators to a programmable logic controller (PLC). IO-Link digitizes the "last meter" of the communication link to the sensors and actuators. Where only binary states (on or off) or analog signals have been transmitted so far, it is now possible to read status information from a sensor or actuator and write parameterization information to the sensor or actuator. IO-Link is not just another bus system, but a point-to-point connection between the IO-Link device and an IO-Link master.

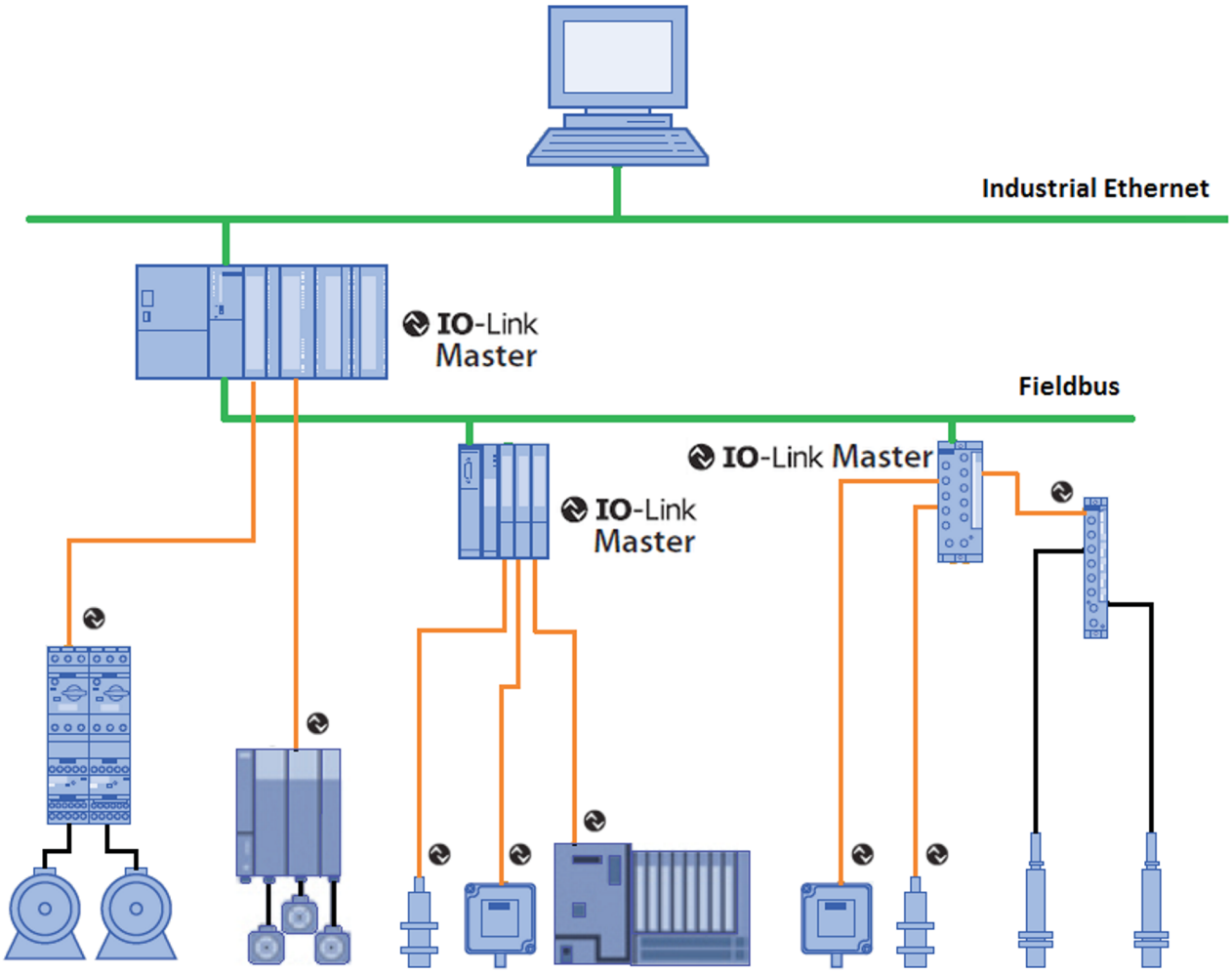


図 4. System Architecture With IO-Link

IO-Link is an answer to the need of digital and analog sensors and actuators to exchange process data, diagnosis information and parameters with a controller (PC or PLC) using a low-cost, digital communication technology while maintaining backward compatibility with the current DI or DO signals as defined in IEC 61131-2.

The IO-Link master establishes the connection between the IO-Link devices and the automation system. As a component of an I/O system, the IO-Link master is installed either in the control cabinet or as remote I/O. The IO-Link master communicates over various fieldbuses or product specific backplane buses. An IO-Link master can have several IO-Link ports (channels). An IO-Link device can be connected to each port. Hence, IO-Link is a point-to-point communication and not a fieldbus. The connection between IO-Link master and device is established through a maximum of 20 m long, unscreened three-wire cable. The wiring is standardized on the basis of M5, M8 and M12.

The IO-Link ports of the master can be operated in the following modes:

- IO-Link: In "IO-Link" mode, the port is used for IO-Link communication.
- DI: In "DI" mode, the port behaves like a digital input.
- DO: In "DO" mode, the port behaves like a digital output.

- Deactivated: "Deactivated" mode can be used for unused ports.

Three transmission rates are specified:

- COM 1 = 4.8 kbit/s
- COM 2 = 38.4 kbit/s
- COM 3 = 230.4 kbit/s

An IO-Link device supports only one data transmission rate. The IO-Link master supports all data transmission rates and adapts itself automatically to the data transmission rate supported by the device.

Four basic data types are available:

- Process data
- Value status
- Device data
- Events

The process data of the devices are transmitted cyclically. Depending on the device, 0 to 32 bytes of process data are possible. The value status indicates whether the process data are valid or invalid. Device data are exchanged cyclically and can be parameters, identification data, and diagnostic information. Events can be error messages (for example, short-circuit) or warnings.

An electronic device description, the IODD file is available for each device. The IODD file stores a variety of information for the system integration:

- Communication properties
- Device parameters with value range and default value
- Identification, process, and diagnostic data
- Device data
- Text description
- Illustration of the device
- Logo of the manufacturer

IO-Link defines a migration path from the existing digital input and digital output interfaces for switching devices towards a point-to-point communication link. Many sensors and actuators are already equipped with microcontrollers offering a UART interface that can be extended by addition of a few hardware components and protocol software to support IO-Link communication. For the connection technology, one possibility that has been defined is an M12 plug connector.

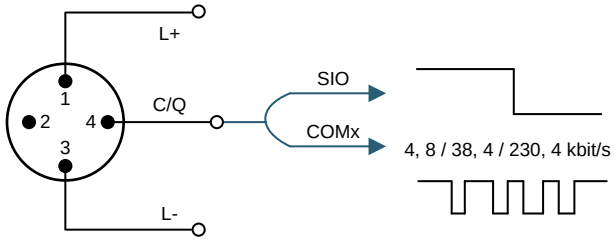


図 5. IO-Link Interface

The IO-Link connectors pin assignment is based on IEC 60947-5-2 with extensions specified in *IO-Link Interface and System Specification v1.1.2* [6]. 表 2 shows the pin assignment.

表 2. IO-Link Pin Assignment

PIN	SIGNAL	DEFINITION
1	L+	Power supply
2	I/Q	Not connected, DI, or DO
3	L–	GND
4	Q	"Switching Signal" DI (SIO)
	C	"Code switching" (COM1, COM2, COM3)

For the IO-Link Transceiver, TI offers the TIOL111. The robust TIOL111 family of transceivers implements the IO-Link interface for industrial point-to-point communication. When a device is connected to an IO-Link master through a three-wire interface, the master can initiate communication and exchange data with the remote node while the TIOL111 acts as a complete physical layer for the communication. These devices have integrated IEC surge protection and integrated reverse polarity protection for low cost and simple system design with minimal external components. Simple pin programmable interface allows easy interfacing to the controller circuits. The output current limit can be configured using an external resistor. Fault reporting and internal protection functions are provided for undervoltage, short-circuit current, and over-temperature. The TIOL111 comes in a small 2.5-mm×3.0-mm DFN package to fit in most cylindrical sensors. 図 6 shows a typical application diagram with the TIOL111 IO-Link Transceiver.

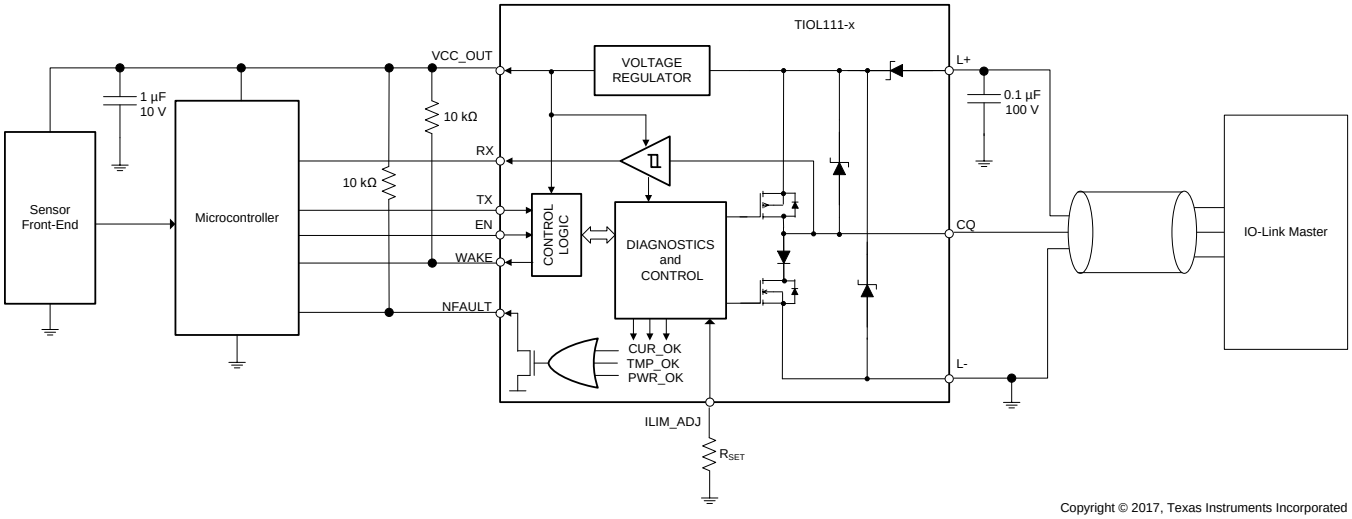


図 6. Typical Application Diagram With TIOL111

The TIOL111 may be operated in IO-Link mode or Standard Input / Output (SIO) mode to either sense or drive a wide range of sensors and loads. The TIOL111 driver output (CQ) can be used in either push-pull, high-side, or low-side configuration using the enable (EN) and transmit data (TX) input pins. The internal receiver converts the 24-V signal on the CQ line to standard logic levels on the receive data (RX) pin. A simple parallel interface is used to receive/transmit data and status information between the TIOL111 and the microcontroller. For the IO-Link firmware update reference design the MSP430FR5969 microcontroller has been used to demonstrate the advantages of the FRAM technology.

2.3.2 IO-Link Firmware Update

To standardize how the user program on the controller accesses the devices, device profiles are defined for IO-Link. The new firmware update profile consists of two parts, "BLOB" and "Firmware-Update". The first part is about the transfer of so-called binary large objects (or BLOB) such as pictures taken by an optical sensor or large amount of structured data collected by a device. Previously, if larger data volumes had to be read out from IO-Link devices, this was only possible through proprietary means. The BLOB profile now provides an option for segmenting the larger data volumes and then transferring them through the existing indexed service data unit (ISDU) communication mechanism in a controlled manner. The trick is that IO-Link is used here only as a data channel. The actual segmentation and flow control takes place in the device or in the PLC. The great advantage of this is that the IO-Link master and the field level are not affected. This means that no modification of the existing system is necessary, and devices that support BLOB transfer can be connected to any existing IO-Link application.

The second part is about firmware update of devices in the field. The firmware update profile uses the newly developed BLOB transfer for the transfer of large quantities of data. The firmware update profile deals with:

- Unlocking of a device's firmware
- Necessary commands and messages
- Firmware update file formats
- Identification, authentication, and validation issues
- Device ID and version rules
- Parameter versions
- Data storage rules

The manufacturer of the device provides a special file (*.iolfw) for the firmware update. In addition to the actual device software, this file also includes additional information, for example, for verification purposes or even with information for the customer. 図 7 illustrates the transmission of firmware updates within an automation system with IO-Link.

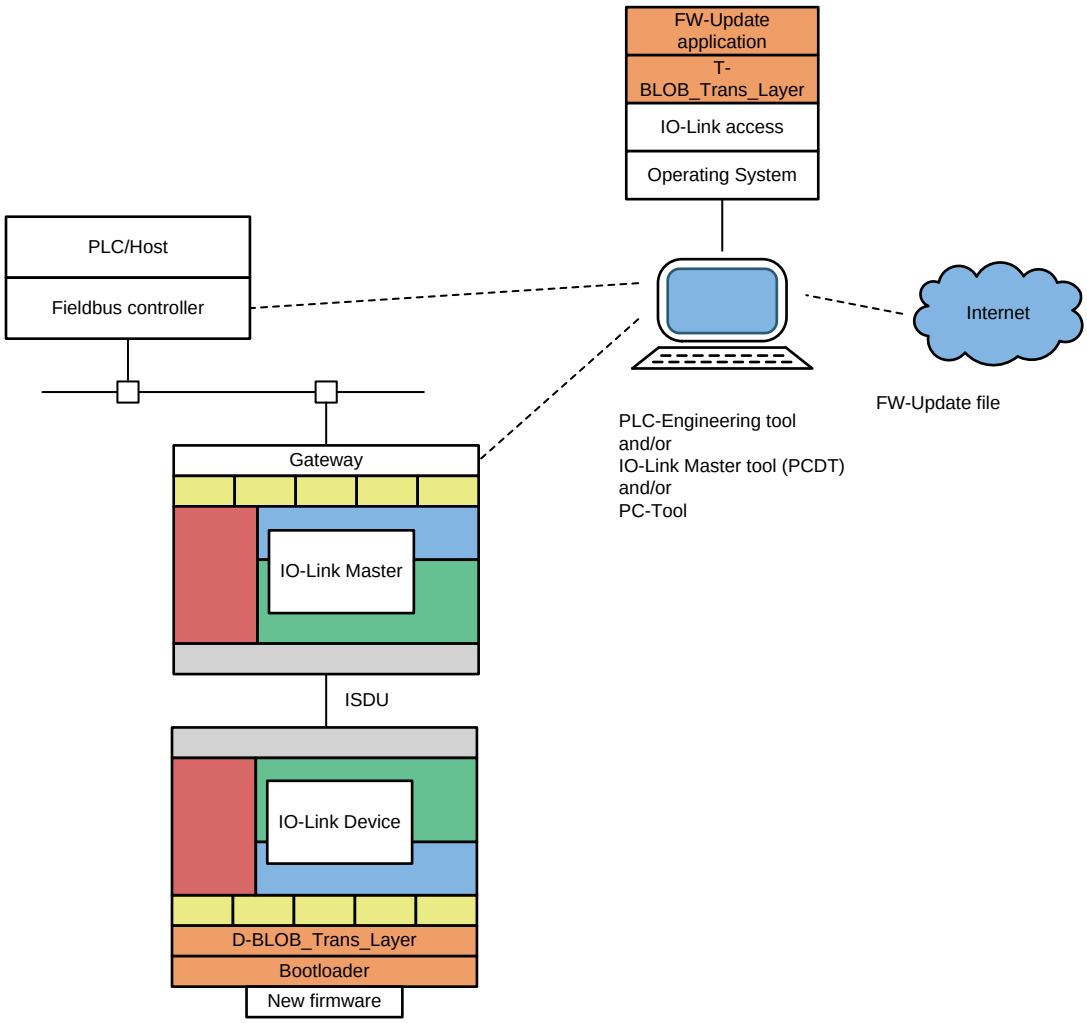


図 7. IO-Link Firmware Update

The IO-Link firmware update of a typical device with Flash memory takes about 1 minute. By using an MSP430 FRAM device instead of a microcontroller with Flash, the firmware can reduce the transfer and programming timings dramatically. FRAM is much faster to write to than flash and has near infinite endurance, which means that in a remote sensor, data could be written more often for improved data accuracy or it could collect data for longer. Due to the lack of a charge pump, FRAM enables lower average and peak power during writes. FRAM is nonvolatile (that is, it retains contents on loss of power).

The data can be written to FRAM right out of the IO-Link channel with no buffering required. The CPU is not held in the process of writes, interrupts are not blocked and the writes are completed within the instruction cycle time. If a flash device needs a memory segment to be flashed immediately, a busy message has to be sent to the master. This is not the case for MSP430 FRAM devices. Using MSP430 with FRAM does not require "busy" messages. The data can be written on-the-fly, as opposed to buffered in RAM. The bitwise programmable memory can be used at the programmer's convenience for data or program storage. FRAM also offers advantages in security. It is inherently more secure due to its makeup, and de-layering is not effective.

In comparison to MCUs with flash, FRAM:

- Is very easy to use
- Requires no setup or preparation such as unlocking of control registers
- Is not segmented and each bit is individually erasable, writable, and addressable
- Does not require an erase before a write
- Allows low-power write accesses (does not require a charge pump)
- Can be written to across the full voltage range (1.8 to 3.6 V)
- Can be written to at speeds close to 8MBps (maximum flash write speed including the erase time is approximately 14 kBps)
- Does not require additional power to write to FRAM when compared to reading from FRAM. The FRAM read current is included in the active mode current consumption numbers already.

表 3 summarizes the MSP430 FRAM advantages versus other memory technologies.

表 3. MSP430 FRAM Advantages

SPECIFICATION	FRAM	SRAM	FLASH
Write speed per word	125 ns	< 125 ns	85 µs
Erase time	No pre-erase required	No pre-erase required	23 ms for 512 bytes
Bitwise programmable	Yes	Yes	No
Write endurance	10^{15} writes	N/A	10^{5} writes per erase cycle
Nonvolatile	Yes	No	Yes
Internal write voltage	1.5 V	1.5 V	12 to 14 V (charge pump required)

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

3.1.1.1 Overview Hardware Building Blocks

図 8 shows the different building blocks of the TIDA-00461 reference design. All components are located on the top layer of the PCB for easy evaluation.

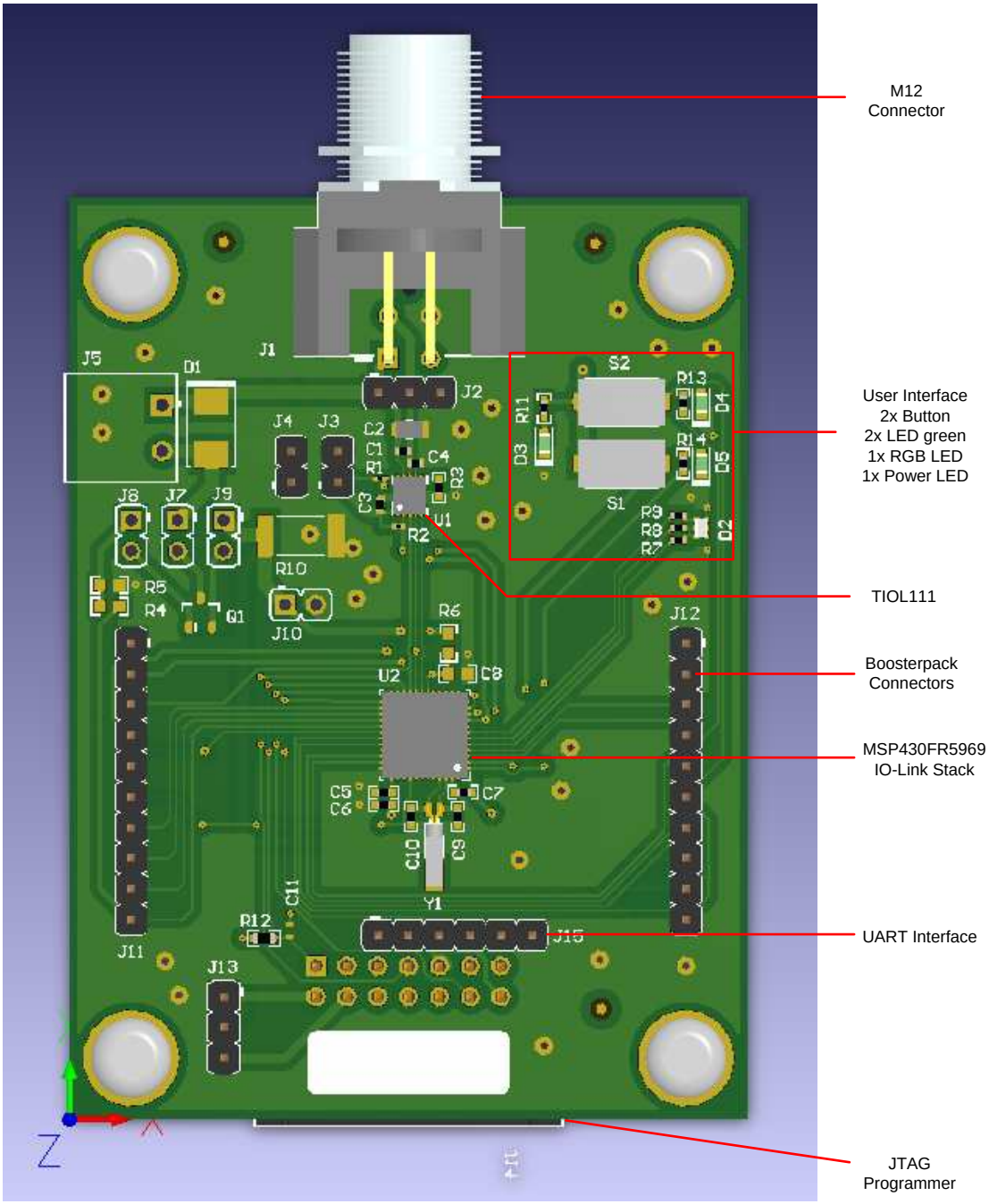


図 8. TIDA-00461 Hardware Component Description

- M12 connector: The board uses an industry standard M12 connector. L+, L–, and C/Q signals are available at this M12 connector J1 (see 図 9).
- User interface: The board indicates with a green LED the availability of the 3.3 V of the integrated LDO of the TIOL111. In addition, the user has the flexibility to use two push-buttons, two green LEDs, and one RGB LED. All can be controlled by the MSP430 MCU (see 図 11).
- TIOL111: This device is the IO-Link PHY with an integrated LDO, reverse polarity protection, and IEC 61000-4-x protection. The device also contains a fault indicator, which monitors the devices temperature, current, and power (see 図 9).
- MSP430FR5969: The MCU runs the IO-Link stack with the firmware update profile. It updates the Sharp LCD BoosterPack (430BOOST-SHARP96) with different pictures, depending on the downloaded firmware.
- UART interface: The system has the possibility to communicate through a UART interface (J15) with a PC (see 図 11).
- JTAG programmer: This is the connector (J14) for the MSP-FET430UIF programmer (see 図 10).
- BoosterPack connectors: These connectors (J11 and J12) enable the user to extend the TI Design with features provided by the BoosterPack ecosystem. For the TIDA-00461, the Sharp LCD BoosterPack (430BOOST-SHARP96) is connected here.

3.1.1.2 Power Design

The entire system is powered with a nominal 24-V DC through J1 or J2. The minimum input voltage is 7 V and is given by the minimum input voltage of TIOL111. The maximum input voltage is 36 V (TIOL111). The integrated LDO inside the TIOL111 generates 3.3 V for the remaining system with a capable output current of 20 mA. Also available is a TIOL111 device with a 5-V LDO[3]. All protection, like reverse polarity, ESD, and surge, is integrated in the TIOL111 IO-Link PHY.

It is also possible to directly provide an external 3.3 V to the system. In this case, remove SH-J3 from J3 and provide 3.3 V to J3-PIN2 and GND to J4 (see 図 9). The LED D3 indicating the availability of the 3.3-V is always active.

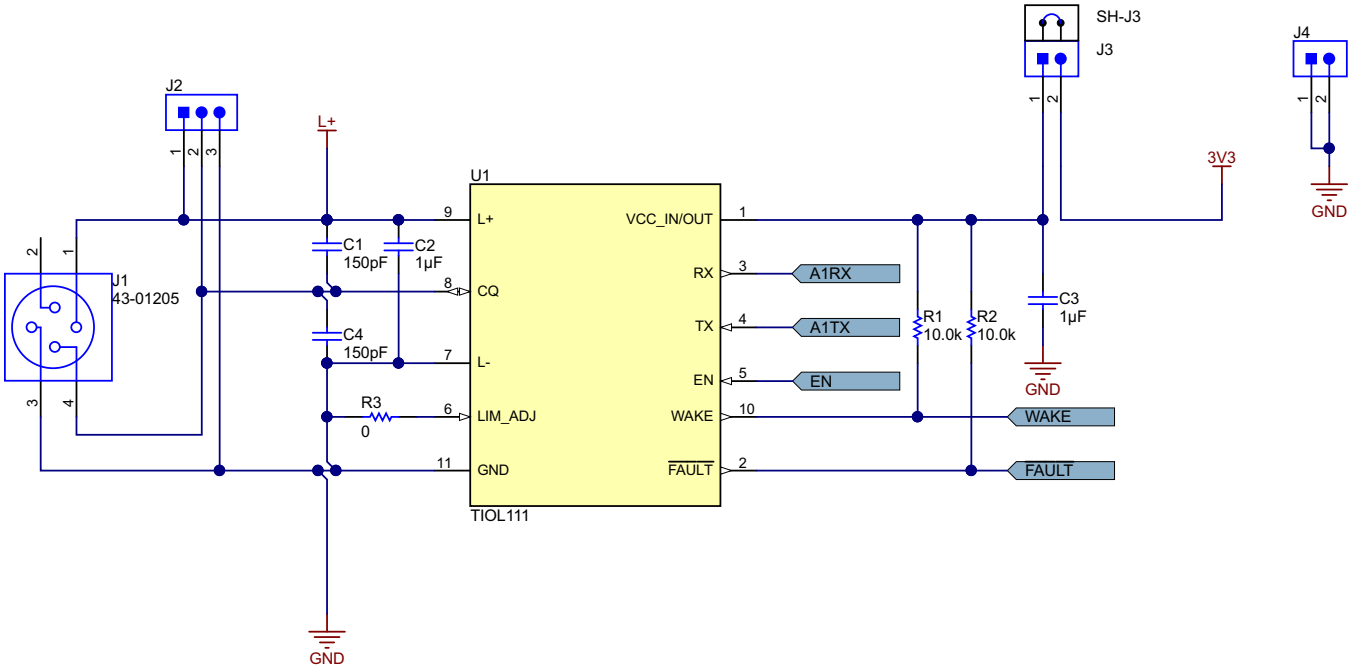


図 9. M12 Connector and IO-Link PHY TIOL111

3.1.1.3 JTAG Interface and UART Backchannel

With the JTAG connector J14, the MSP-FET430UIF can be connected to program the MSP430FR5969 (see 図 10). The UART backchannel on J15 (see 図 11) can be used to communicate with the TIDA-00461.

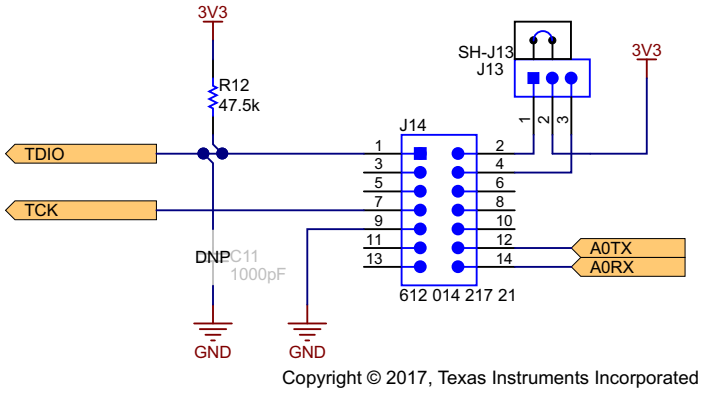


図 10. JTAG Interface for MSP-FET430UIF Programmer

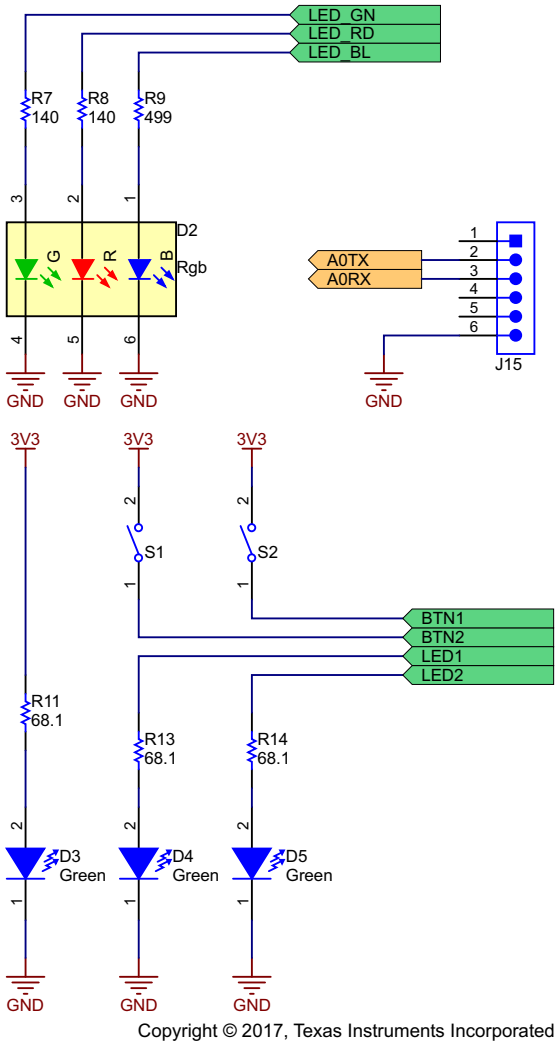


図 11. User Interface

表 4. Overview Connectors and Jumpers

CONNECTOR	DESCRIPTION
J1: M12 CONNECTOR	
J1-PIN1	24-V DC; L+
J1-PIN2	NC
J1-PIN3	GND; L–
J1-PIN4	C/Q
J2: HEADER	
J2-PIN1	24-V DC; L+
J2-PIN2	C/Q
J2-PIN3	GND; L–
J4: HEADER	
J4-PIN1	GND
J4-PIN2	GND
J5: HEADER	
J5-PIN1	24-V DC; L+

表 4. Overview Connectors and Jumpers (continued)

CONNECTOR	DESCRIPTION
J5-PIN2	GNG; L–
J11 and J12: HEADER	
J1	LaunchPad connector (details in schematic)
J12	LaunchPad connector (details in schematic)
J14: PROGRAMMING CONNECTOR	
J14	JTAG Connector for MSP-FET430UIF
J15: HEADER	
J15-PIN2	UART: TX
J15-PIN3	UART: RX
J15-PIN6	GND
JUMPER	
J3	Current measurement for 3.3 V provides external 3.3 V
J13	INT or EXT supply from MSP-FET430UIF programmer

3.1.2 Software

The demo software is a complete implementation according to IO-Link specification V1.1.2 and IO-Link Profile BLOB Transfer & Firmware Update V1.0. To demonstrate the BLOB transfer and firmware update, different pictures can be loaded through IO-Link to the MSP430 FRAM memory. The different downloaded pictures can then be shown on the Sharp LCD display, which is on the connected BoosterPack.

The built-in IP encapsulation capability (IPE) of the MSP430 FRAM device can be used to protect critical pieces of code, configuration data, or secret keys in FRAM memory from being easily accessed or viewed.

For more information on the IO-Link stack software, contact TEConcept (https://www.teconcept.de/).

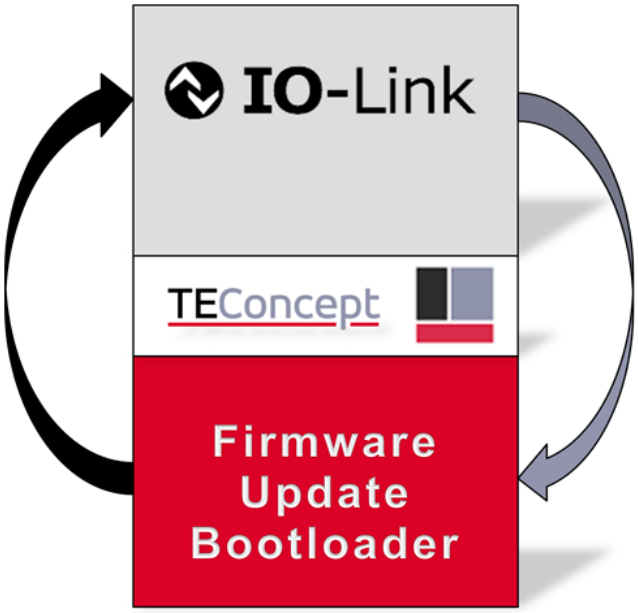


図 12. IO-Link Stack With Firmware Update From TEConcept

Several different pictures can be downloaded to the MSP430FR5969 at once. The user can then select which picture to show on the display. The different pictures can be selected through the ISDU parameter shown in 表 5.

表 5. ISDU for TIDA-00461

INDEX	SUB-INDEX	DATA LENGTH	DESCRIPTION
0x47CF	0x00	0x01	Select the picture that is shown on the display: • 0x00—Picture 1 • 0x01—Picture 2 • 0x02—Picture 3

3.2 Testing and Results

図 13 shows the test setup for the IO-Link firmware update.

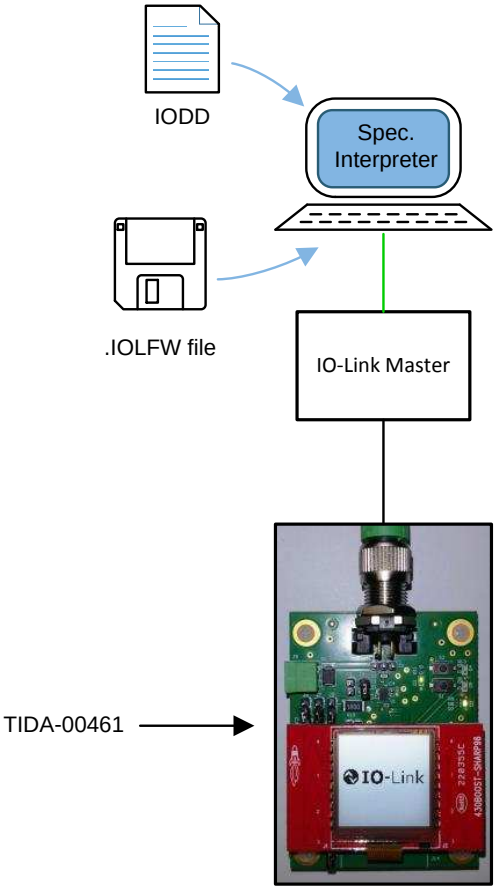


図 13. IO-Link Firmware Update Test Setup

The USB 1-Port Master from TEConcept is used for the test. This master is connected with USB to a PC. The IO-Link Control Tool is running on the PC and controls the IO-Link master. 図 14 shows this GUI on the PC. For configuration, the tool needs an IODD file and the firmware update file (.IOLFW). The FW-Update file (.IOLFW file) contains information specific to the FW-Update mechanism of devices through IO-Link communication. The file internally represents a .zip archive. The archive is a package that consists of a metadata file, binary data file with the firmware BLOB, and optionally additional resource files. The metadata file describes the FW-Update data and the internal file structure of the package. The FW-Update file can be created by the use of third party tools. Furthermore, it is possible to generate the FW-Update file by manually adding the metadata file, the binary data file (BLOB), and optionally additional resource files to a .zip archive and renaming it according to IO-Link BLOB Transfer & Firmware Update V1.0[7].

図 14 shows the GUI for the firmware update.

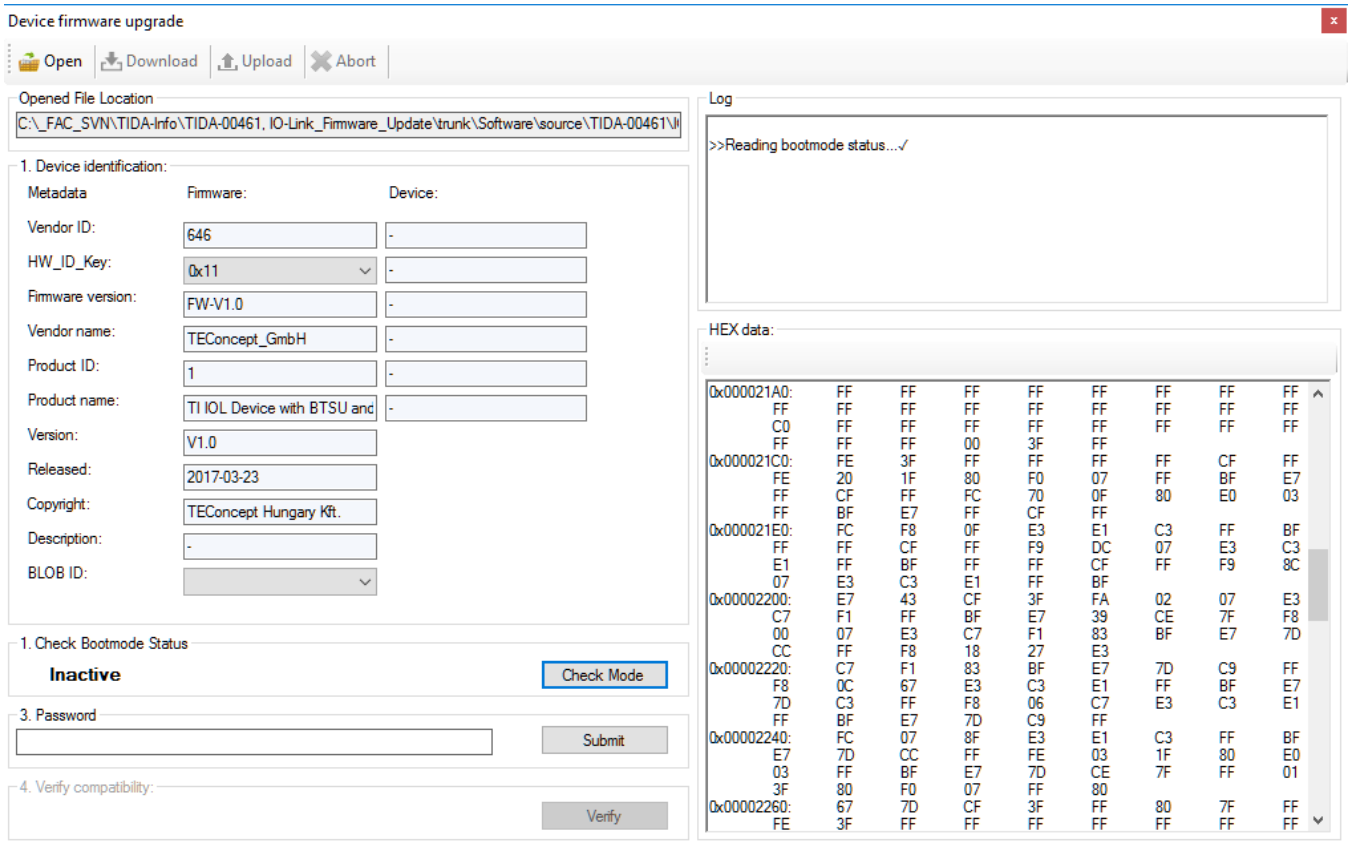


図 14. IO-Link Firmware Update GUI

The tool on the PC logs the progress of the firmware update and checks if the firmware update was successful (see 図 15).

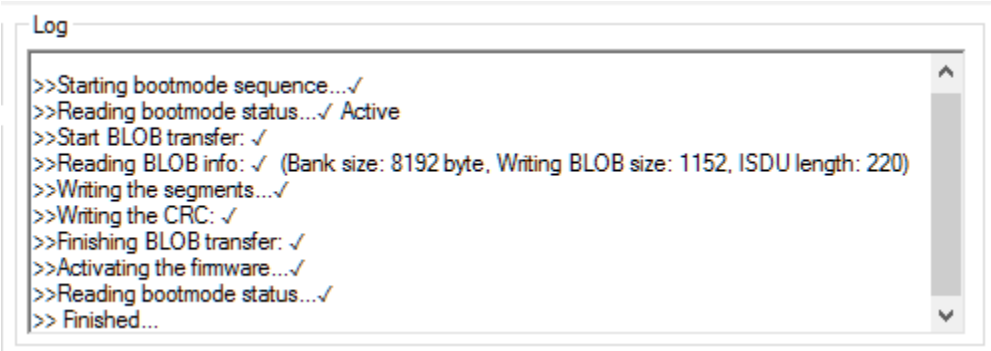


図 15. IO-Link Successful Firmware Update Log

After a successful firmware update, different pictures appear on the display.

図 16. Picture Before Firmware Update

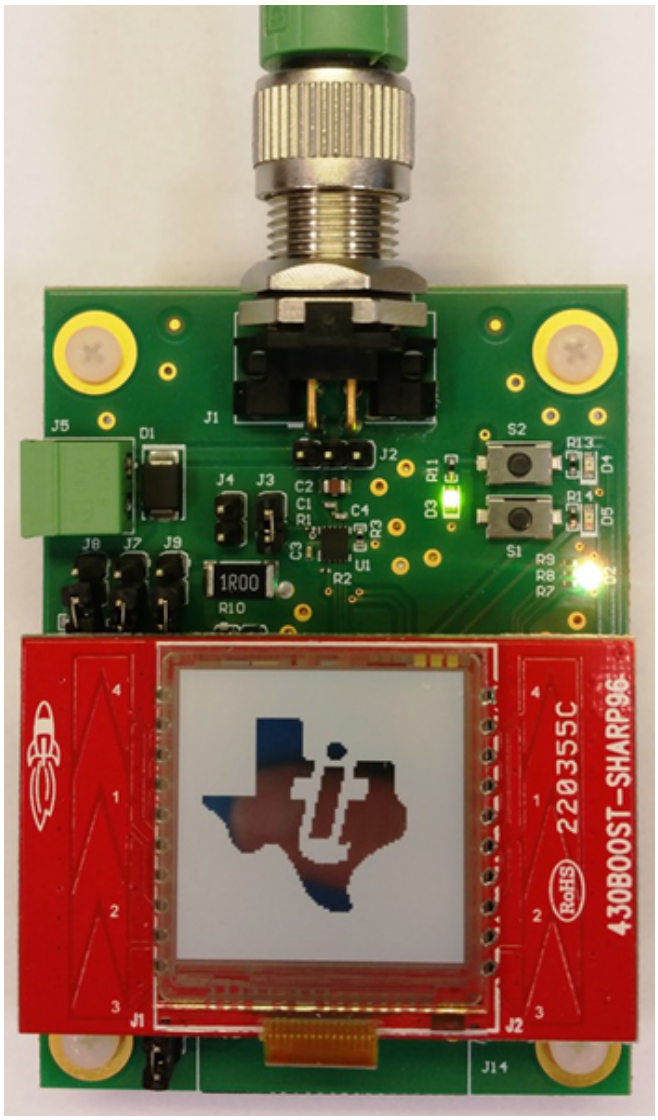


図 17. Picture After Firmware Update

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-00461.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00461.

4.3 Altium Project

To download the Altium project files, see the design files at TIDA-00461.

4.4 Gerber Files

To download the Gerber files, see the design files at TIDA-00461.

4.5 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00461.

5 Software Files

To download the software files, see the design files at TIDA-00461.

6 Related Documentation

1. Texas Instruments, *MSP430FR59xx Mixed-Signed Microcontrollers* , MSP430FR5969 Datasheet (SLAS704)
2. Texas Instruments, *MSP430FR59xx User's Guide* , MSP430FR5969 User's Guide (SLAU367)
3. Texas Instruments, *TIOL111 IO-Link Device Transceivers with Integrated Surge Protection* , TIOL111 Datasheet (SLLSEV5)
4. Texas Instruments, Code Composer Studio (CCS) Integrated Development Environment (IDE) (http://www.ti.com/tool/CCSTUDIO)
5. IO-Link Community, IO-Link Technology (http://www.io-link.com/)
6. IO-Link Community, *IO-Link Interface and System Specification V1.1.2*
7. IO-Link Community, IO-Link BLOB Transfer & Firmware Update V1.0
8. TEConcept, IO-Link Stack Software (https://www.teconcept.de/)

6.1 商標

7 Terminology

Binary large object (BLOB)— Amount of coherent data to be transferred to or from the device

Bootloader— Device application responsible for unlocking existing firmware, handling of FW-Update binaries and permanent storage (for example, flashing)

COM1— SDCI communication mode with transmission rate of 4.8 kbit/s

COM2— SDCI communication mode with transmission rate of 38.4 kbit/s

COM3— SDCI communication mode with transmission rate of 230.4 kbit/s

Cycle time— Time to transmit an M-sequence between a master and its device including the following idle time

Device— Single passive peer to a master such as a sensor or actuator download transfer of data from a tool through a master to the device

Firmware— Entire nonvolatile software of a device consisting of the technology specific application including the bootloader and the communication stack

FW update application— Computer software tool for the purpose of updating a device's firmware host PC or PLC, hosting software tools as counterpart of device applications

IODD— IO device description

ISDU— Indexed service data unit used for acyclic acknowledged transmission of parameters that can be segmented in a number of M-sequences

M-sequence— Sequence of two messages comprising a master message and its subsequent Device message

Master— Active peer connected through ports to one up to n devices and which provides an interface to the gateway to the upper level communication systems or PLCs

Message— <SDCI> sequence of UART frames transferred either from a Master to its Device or vice versa following the rules of the SDCI protocol

On-request data— A cyclically transmitted data upon request of the master application consisting of parameters or event data

PLC— Programmable logic controller

Port— Communication medium interface of the master to one device

Process data— Input or output values from or to a discrete or continuous automation process cyclically transferred with high priority and in a configured schedule automatically after start-up of a master

SDCI— Single-drop digital communication interface

SIO— Port operation mode in accordance with digital input and output defined in IEC 61131-2 that is established after power-up or fallback or unsuccessful communication attempts

Switching signal— Binary signal from or to a device when in SIO mode (as opposed to the "coded switching" SDCI communication)

Tool— Software means within controllers or personnel computers for the processing of BLOBs or firmware updates

UART frame— <SDCI> bit sequence starting with a start bit, followed by eight bits carrying a data octet, followed by an even parity bit and ending with one stop bit

Upload— Transfer of data from the device to a tool through a master

Wake-up— Procedure for causing a device to change its mode from SIO to SDCI

8 About the Author

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