参考資料

TI Designs: TIDA-01426
センサ励起を目的とした低電圧DC源からのAC入力電圧生成のリファレンス・デザイン

概要

このリファレンス・デザインは、ディスクリート部品を使用したフレーム検出で使用できる高電圧信号の生成方法を示します。このリファレンス・デザインは、低BOMコストと小型ソリューション・サイズを考慮して構築されています。プッシュプル・コンバータ・トポロジを使用すると、広い入力範囲と高速な起動時間を実現できます。

リソース

TIDA-01426	デザイン・フォルダ
TL494	プロダクト・フォルダ
TL431	プロダクト・フォルダ
CSD19538Q3A	プロダクト・フォルダ
TLV171	プロダクト・フォルダ

TI E2E™ Community

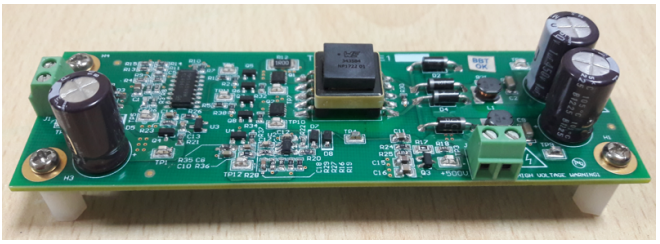
E2Eエキスパートに質問

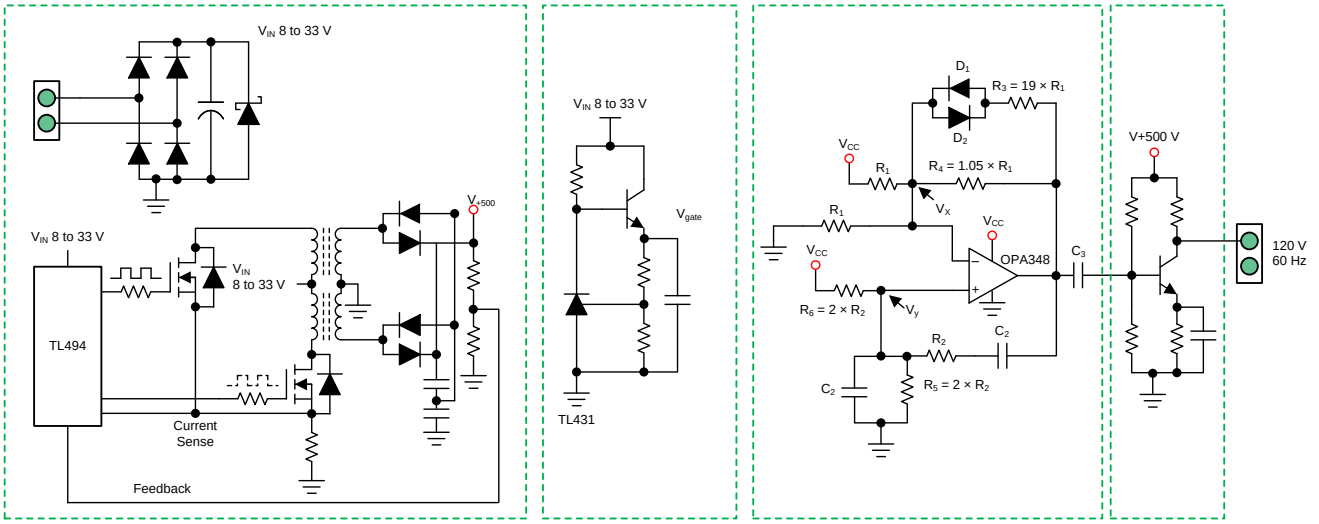
特長

- 10V～36Vの汎用入力範囲
- 120V、60Hz出力、最大4%の全高調波歪み(THD)
- 起動時間56ms (10V)
- 出力精度5%
- 最大1Wの出力
- 小さい占有面積と低いBOMコスト

アプリケーション

- HVACバルブおよびアクチュエータの制御
- HVACセンサ・トランスミッタ
- HVACシステム・コントローラ





Low-Cost, High-Efficiency Push-Pull Boost Converter

Low-Cost Regulated LDO

Low THD, Sine Wave Oscillator
*Can be generated using MCU based SPWM

Class A Amplifier
*Can be Half Bridge for SPWM signals

1 System Description

A burner system is an integral part of a heating, ventilation, and air conditioning (HVAC) system. A burner system helps generate hot water or steam for heating purposes. The hot water is circulated either for utility purposes or for temperature control. The burner system has control electronics as shown in 図 1 to operate in optimum conditions and prevent any failure with a predictive diagnosis alarm. The electronics unit has actuator control and field sensing cards for the motor drive, damper control, flow control, temperature and pressure sensing, and so on. The unit also ignites and senses flame inside the burner as shown by ECU4 (see 図 1). This reference design focuses on the excitation power supply for the flame rod.

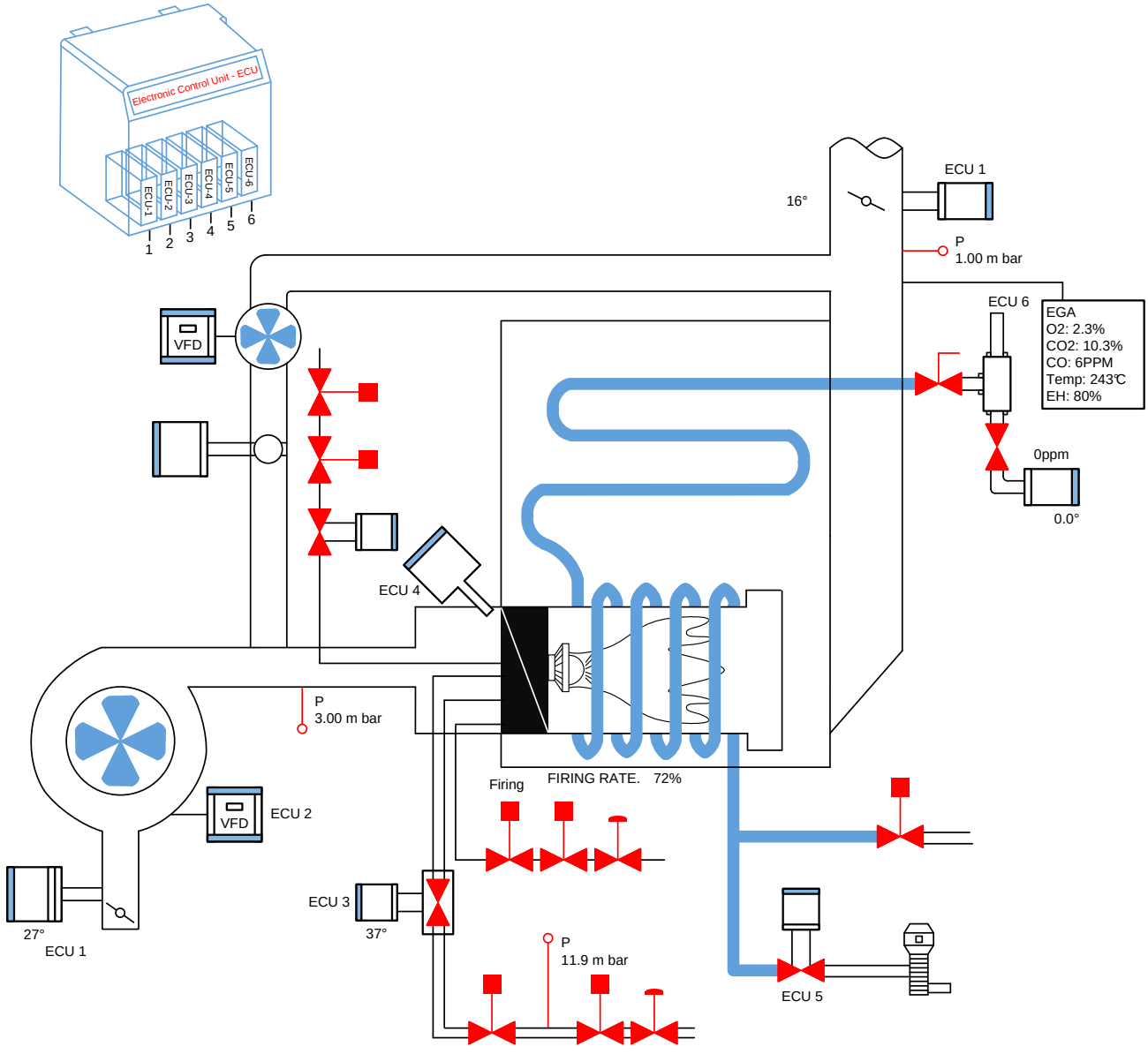


図 1. Burner Control

The flame rod sensor is a high impedance sensor. Under the presence of flame, an ionization effect takes place due to which current flows from the flame rod to earth. This current is proportional to flame intensity. As shown in 図 2, a high-voltage excitation is required for ionization effect. To prevent carbonization effect, AC excitation is applied. This excitation is usually a line supply 50- or 60-Hz signal. A low-frequency AC signal is used to prevent losses due to cable capacitance and skin effect. The geometric ratio of flame rod and earth plate decides the conduction in positive and negative polarity. Usually the ratio is lower to make the flame rod conduct more in positive half cycles and negligible in negative half cycles. This ratio results in output similar to a half wave rectifier. Thus, the flame rod is equivalent to a forward bias diode with a high series impedance, which is the function of flame intensity as shown in 図 2. A signal chain amplifies the lower AC current and controls the fuel supply for the burner firing rate.

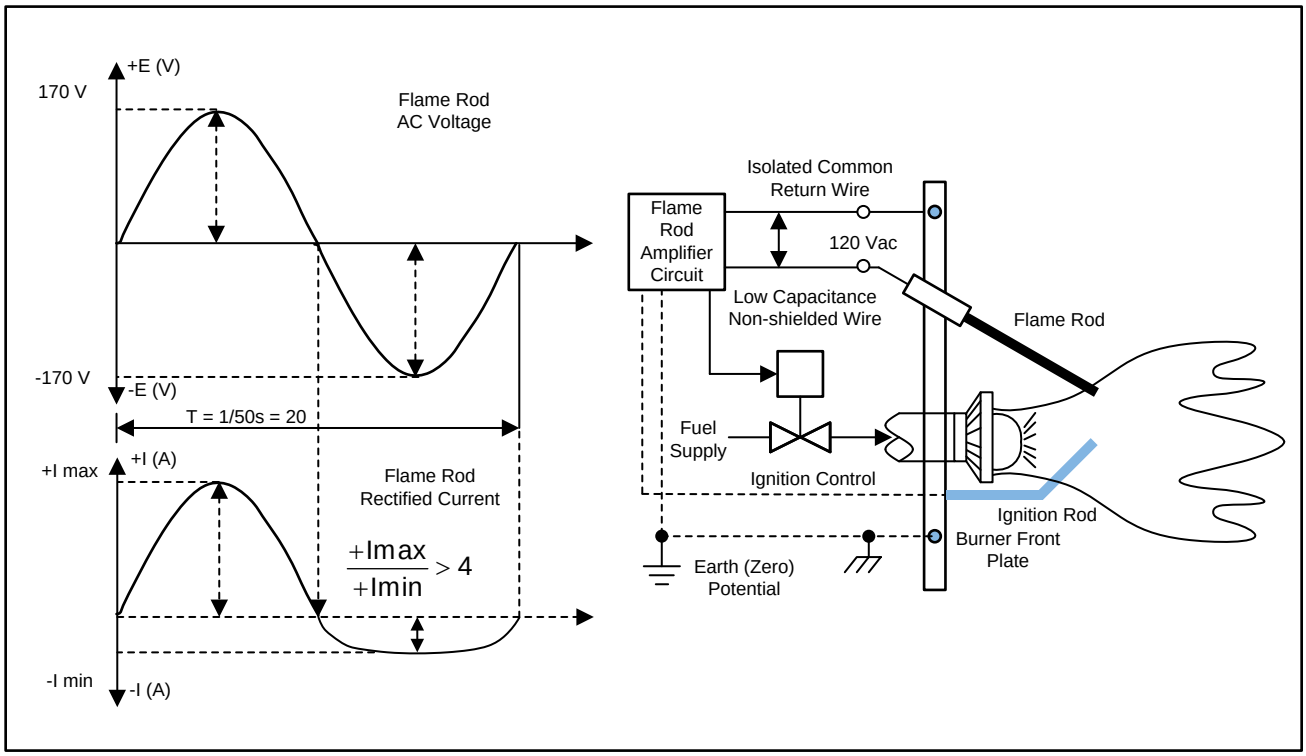


図 2. Flame Sensing Using Flame Rod

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER		SPECIFICATIONS			
		MIN	TYP	MAX	UNIT
Input supply voltage (V_{IN})	DC	10	24	33	V
	AC at 50 or 60	18	24	33	
Quiescent current (I_Q)		—	—	0.3	A
Output voltage (V_O)		105	120	140	V
Output current (I_O)		—	—	0.0015	A
Output load (R_L) Max cable capacitance 720 pF, assuming 22 AWG, 60 feet, 1 pair twisted cable 12 pF/ft		1	40	100	MΩ

表 1. Key System Specifications (continued)

PARAMETER		SPECIFICATIONS			
		MIN	TYP	MAX	UNIT
Performance	Initial accuracy	—	5	—	%
	THD	—	4	—	%
	Startup time at 10 V	—	—	100	ms

2 System Overview

2.1 Block Diagram

The power block can be divided into four sections (as shown in 図 3) for understanding system design calculations.

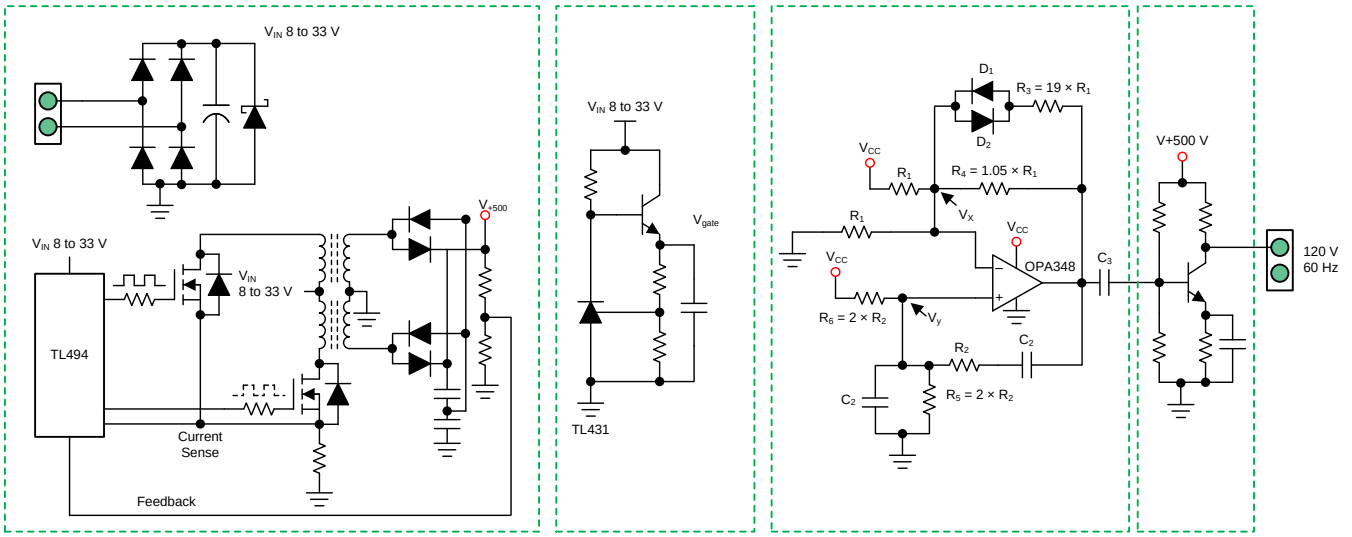


図 3. System Block Diagram

2.2 Highlighted Products

2.2.1 TL494

The TL494 device incorporates all the functions required in the construction of a control circuit for pulse width modulation (PWM) on a single chip. The TL494 device contains two error amplifiers, an on-chip adjustable oscillator, a dead-time control (DTC) comparator, a pulse-steering control flip-flop, a 5-V, 5%-precision regulator, and output control circuits. The error amplifiers exhibit a common-mode voltage ranging from –0.3 V to VCC – 2 V. The DTC comparator has a fixed offset that provides approximately 5% dead time. The uncommitted output transistors provide either common-emitter or emitter-follower output capability. The TL494 device provides for push-pull or single-ended output operation, which can be selected through the output-control function. The architecture of this device prohibits the possibility of either output being pulsed twice during push-pull operation. The TL494C device is characterized for operation from 0°C to 70°C. The TL494I device is characterized for operation from –40°C to 85°C.

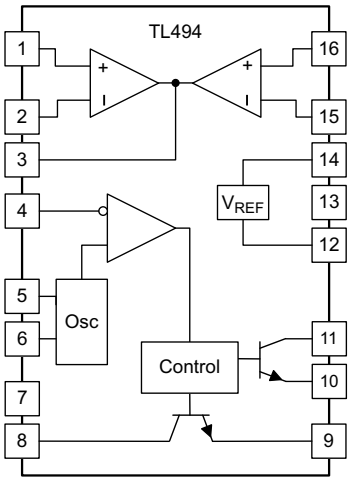


図 4. TL494 Block Diagram

2.2.2 TL431

The TL431 device is a three-terminal adjustable shunt regulator. The output voltage can be set to any value between V_{REF} (approximately 2.5 V) and 36 V with two external resistors. These devices have a typical output impedance of 0.2 Ω. Active output circuitry provides a very sharp turnon characteristic, making these devices excellent replacements for Zener diodes in onboard regulation, adjustable power supplies, and switching power supplies.

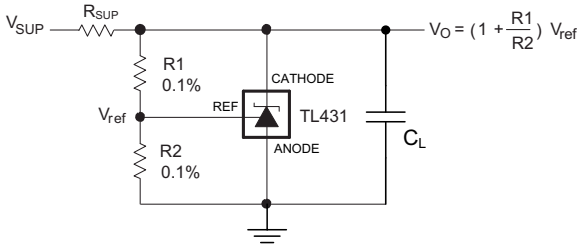


図 5. TL431 Shunt Regulator

2.2.3 TLV171

The 36-V TLV171 device provides a low-power option for cost-conscious industrial systems requiring an electromagnetic interference (EMI)-hardened, low-noise, single-supply operational amplifier (op amp) that operates on supplies ranging from 2.7 V (±1.35 V) to 36 V (±18 V). The TLV171 provides low offset, drift, and quiescent current balanced with high bandwidth for the power. Input signals beyond the supply rails do not cause phase reversal. The TLV171 is stable with capacitive loads up to 200 pF. The input can operate 100 mV below the negative rail and within 2 V of the top rail during normal operation.

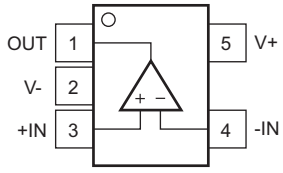


図 6. TLV171 Block Diagram

2.2.4 CSD19538Q3A

The CSD19538Q3A is NexFET™ power MOSFET with a drain-to-source voltage of 100 V, a low R_{DSon} of 49 mΩ, and small footprint SON of 3.3 mm × 3.3 mm to achieve very low conduction losses and reduce board space.

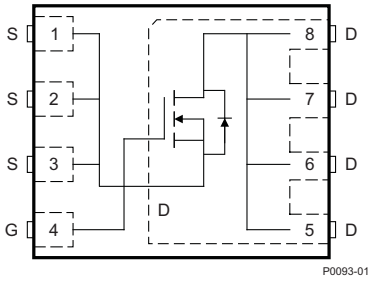


図 7. MOSFET CSD19538Q3A

2.3 System Design Theory

The TIDA-01426 design focuses on the design of a power supply targeted for flame rod excitation in burner control, as shown in 図 8. The supply needs to generate a low-voltage regulated supply for low-power peripherals and line supply voltage for flame rod excitation. Using the TL494 and TL431 devices generates the required low- and high-voltage supplies.

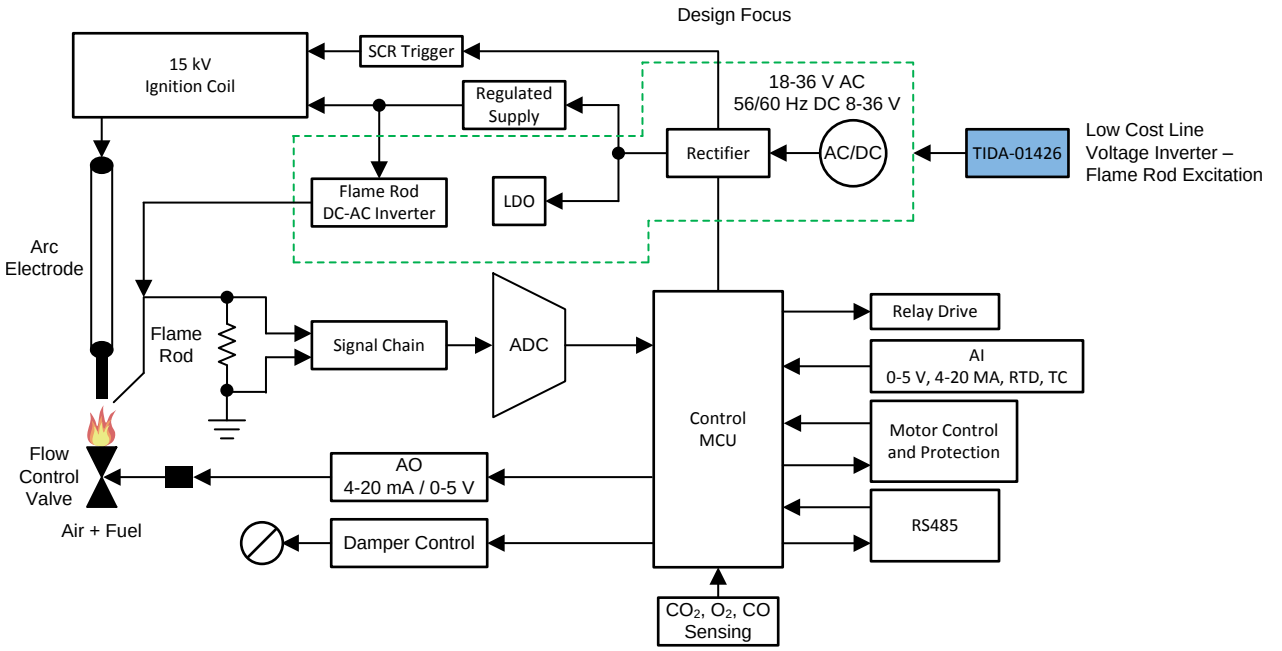


図 8. Typical Electronics Control Board

2.3.1 Designing Push-Pull Converter

2.3.1.1 TL494 Calculations

To generate high DC bus voltage, push-pull topology is implemented in this reference design. Using flux swing in both polarities and high switching frequency makes it easy to design the small size magnetic transformer. TL494 integrated peripherals like an oscillator, dead-time controller, error amplifier, and PWM generator make it possible to design a low-cost, regulated output, push-pull converter.

2.3.1.1.1 Oscillator Calculations

The oscillator of the TL494 is set by R_t and C_t. To design a smaller magnetic transformer, a 100-kHz oscillating frequency is selected. For push-pull configuration with a C_t of 1 nF, the computed R_t value is 5k as shown in 式 1. The closest standard value is 4.99k. In the schematic, R_6 and C_6 denotes R_t and C_t. For stable oscillations, a low-ppm resistor and C0G capacitor are recommended.

$$R_T = \frac{1}{2 \times f_{OSC} \times C_T} = \frac{10^9}{2 \times 100000 \times 1} = 5\,k \tag{1}$$

2.3.1.1.2 Soft-Start and Dead-Time Calculations

The TL494 can be tailored for custom soft-start and dead time to prevent high in-rush current and cross conduction. As shown in 図 9, capacitor C_2 with R_6 applies a negative slop waveform, allowing the pulse width to increase slowly. Initially capacitor C_2 forces the DTC to follow an input of 5 V, which results in 100% dead time. Soft-start can be configured in multi of clock cycle as shown in 式 2.

$$C_2 = \frac{100 \times \frac{1}{f_{SW}}}{R_6} = \frac{100 \times \frac{1}{100000}}{1000} = 1\,\mu F \tag{2}$$

As the soft-start slope slowly decays, the potential due resistor divider R_6 and R_7 with an internal 0.1-V offset result into a tailored dead time. After soft-start, the voltage at the pin is a ratio of R_6:R_7 multiplied by V_{REF}. The value for dead time is computed based on the turnon and turnoff time of the MOSFET so that enough blanking is provided to prevent cross conduction. For this reference design, a blanking time of 500 ns is provided with resistor R_7 of 5k.

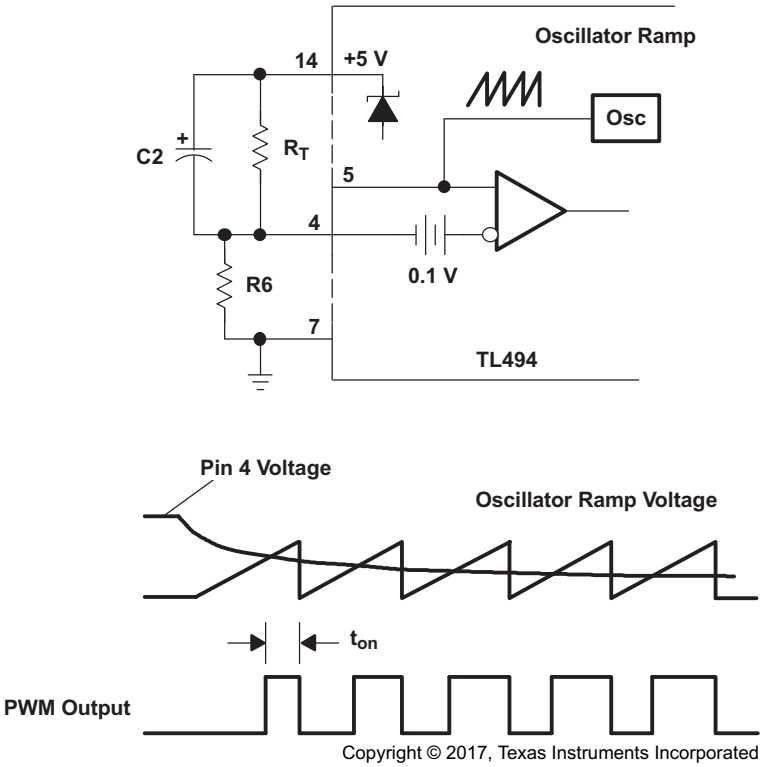


図 9. Soft-Start Circuit

2.3.1.1.3 Voltage Error Amplifier

A simple non-inverting error amplifier is implemented with one of the TL494 internal op amps. An internal reference of 5 V is divided to 2.5 using resistors R_{11} and R_{14} in board. 図 10 is shown with resistors R_3 and R_4. The desired output is scaled to 2.5 V using resistors R_{10} and R_7. The closed loop gain of the op amp (= 101) helps to maintain stable output. Resistors R_9 and R_4 are feedback resistors on board to get the desired closed loop gain.

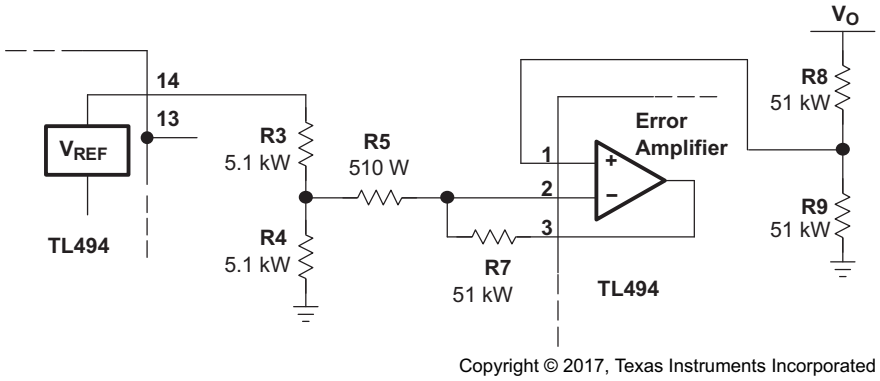


図 10. Feedback Error Amplifier

2.3.1.1.4 Overcurrent Protection

Overcurrent protection is implemented using one of the internal op amps of the TL494. A stable 1 V is applied to the negative terminal of the op amp using resistors R_{13} and R_{15} in the actual circuit. A current sense resistor R_{12} of 1 Ω is connected to the source pin of the MOSFET Q_1 and Q_2. The circuit is limited to a peak current of 1 A once the voltage across sense resistor R_{12} increases to a 1-V reference.

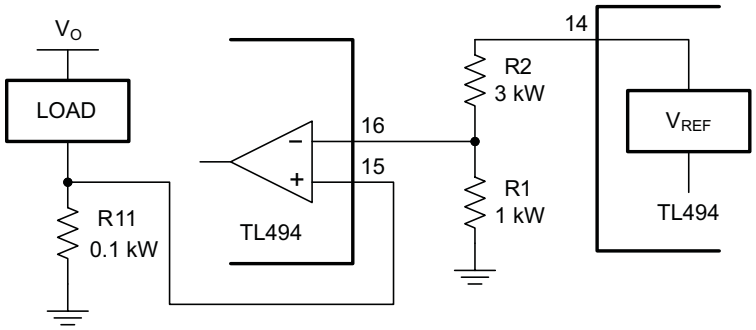


図 11. Current-Limiting Circuit

2.3.1.2 Magnetic Design

The objective for this application is to have a smaller footprint transformer. To achieve the same, this reference design has a 100-kHz switching frequency and a max duty cycle of 40%. In this application, Wurth E13 core transformer is used. For a custom transformer design, the proper core material needs to be selected. N87, N88, N95, N96, and N97 are some standard core materials available from TDK Epcos for a switching frequency up to 500 kHz. N87 core can be selected which has saturation flux of 0.39 T at 100°C with core loss of 3.75 mW / mm^3 at 100 kHz switching. This application uses a custom Wurth Transformer. The design equations shown in 表 3 can be used for a custom transformer design. For a cost-sensitive application, a Toroid core can also be used. For ease of design, the maximum flux swing (Bm) can be limited to 0.2 T with current density (J) of 3 A/mm^2. The E13 core is selected to show design calculations.

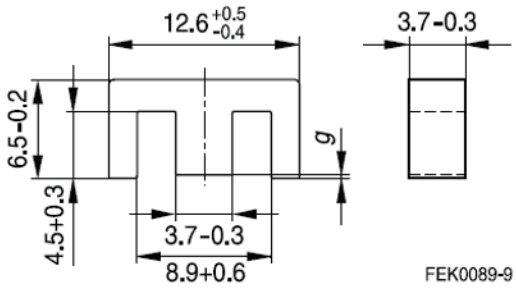
表 2. E13 Core Calculations

SR NO	PARAMETER	VALUE	UNIT
1	Cross sectional area (A_c)	12.4	mm^2
2	Window area (A_w)	$\left(\frac{(8.9-3.7)}{2}-0.3\right)\times(4.5-0.3)=9.66$ where 0.3 is for bobbin clearance	mm^2
3	Area product (A_p)	$A_c \times A_w = 82.58$	mm^4
4	Nominal inductance (A_l)	850	nH

E 13/7/4 (EF 12.6)

Core **B66305**

- To IEC 61246
- For miniature transformers
- Available with SMD coil former
- E cores with high permeability for common-mode chokes and broadband applications
- Delivery mode: single units



Magnetic characteristics (per set)

$\Sigma l/A$ = 2.39 mm^{-1}
l_e = 29.6 mm
A_e = 12.4 mm^2
A_{min} = 12.2 mm^2
V_e = 367 mm^3

Approx. weight 2 g/set

Ungapped

Material	A_L value nH	μ_e	P_V W/set	Ordering code
N30	1000 +30/–20%	1900		B66305G0000X130
T46	3600 ±30%	6839		B66305F0000X146
N27	800 +30/–20%	1510	< 0.40 (200 mT, 100 kHz, 100 °C)	B66305G0000X127
N87	850 +30/–20%	1620	< 0.20 (200 mT, 100 kHz, 100 °C)	B66305G0000X187

図 12. E13 Core Specification

表 3. Transformer Calculations

SR NO	PARAMETER	EQUATION	COMPUTED VALUE	SELECTED VALUE
1	Required area product	$A_p = \frac{\left(\sqrt{2} \times V_{DC} \times I_{DC}\right) \times \left(1 + \frac{1}{\eta}\right)}{4 \times k_w \times B_m \times f_s \times J}$ where k_w = 0.4, η = 0.8, V_{DC} = 500 V, and I_{DC} = 2 mA	33.14 mm^4	Area product computed as shown in 表 2 is greater
2	Primary turns	$N_1 = \frac{V_{MIN}}{4 \times B_m \times f_s \times A_c}$ where A_c is the cross section of the core	10	10
3	Turns ratio	$n = \frac{V_{DC}}{2 \times D_{MAX} \times V_{MIN}}$ where D_{MAX} = 0.4	62.5	63
4	Secondary turns	$N_2 = n \times N_1$	630	630
5	Secondary RMS current	$I_2 = \sqrt{D_{MAX}} \times I_{DC}$	1.43 mA	—
6	Primary RMS current	$I_1 = n \times I_2$	90.5 mA	—
7	Cross section area of primary wire	$a_1 = \frac{I_1}{J}$	0.026 mm_2	36 SWG 0.02927 mm_2
8	Cross sectional area of secondary wire	$a_2 = \frac{I_2}{J}$	0.0004 mm_2	45 SWG 0.003973 mm_2
9	Total winding area	$\sum_{i=1}^{2} a_i N_i = (2 \times N_1 \times a_1) + (N_2 \times a_2)$	3.08 mm_2	—
10	Utilization factor	$\left(\frac{\text{Total Winding Area}}{\text{Window Area } A_w}\right) \times 100$	31.88 %	Value < 40 %

Inductors can be added in series with output diodes and capacitors to limit ripple current.

2.3.1.3 MOSFET Drive and Losses

The fast switching speed, low drop voltage, and high input impedance of MOSFETs make them suitable for push-pull switching. The TI NexFET CSD19538Q3A with low drain-to-source channel resistance is selected for push-pull drive. The MOSFET is driven using an external totem pole transistor for a better drive capability.

2.3.1.3.1 Conduction Losses

The MOSFET gate drive is driven through the totem pole circuit as shown in 図 13.

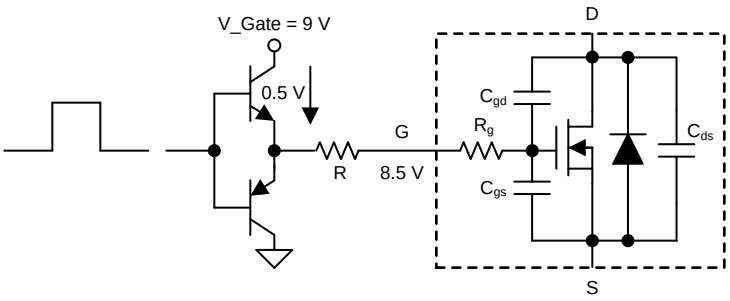


図 13. MOSFET Totem Pole Drive

During high pulse, the NPN transistor conducts resulting in a gate drive voltage of 8.5 V due to a 0.5-V drop across the collector emitter. From the MOSFET datasheet, the typical R_{DSon} for a 8-V gate-to-source voltage is 50 mΩ.

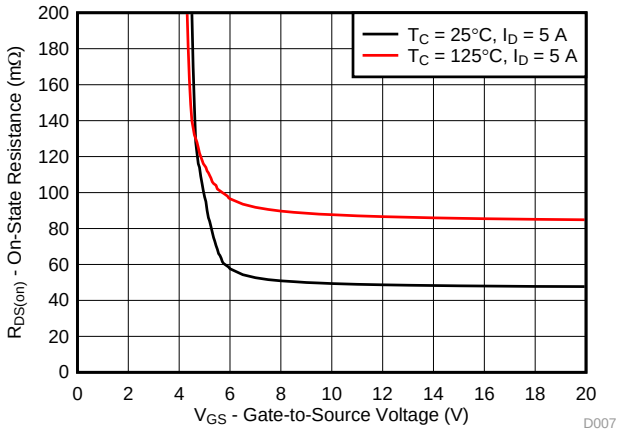


図 14. MOSFET On-State Resistance

Power loss during conduction phase is computed as shown in 式 3.

$$P_{cond} = \frac{1}{T}\int_0^{ton} (n \times I_0)^2 \times R_{DSon} dt = \frac{1}{T}(n \times I_0)^2 \times R_{DSon} \times ton = (n \times I_0)^2 \times R_{DSon} dt \times D = 317\ \mu W \quad (3)$$

2.3.1.3.2 Gate Drive Power Loss

During turnon, the gate-to-source capacitance (C_{gs}) charges through resistor R + R_g. The current waveform is exponential decay. During this period there is power loss across the N-channel transistor. Q_{gs} is obtained from the MOSFET datasheet as shown in 表 4.

表 4. Electrical Characteristics(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_D = 250 µA	100.0	—	—	V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 80 V	—	—	1.0	µA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = 20 V	—	—	100.0	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2.8	3.2	3.8	V
$R_{DS(on)}$	Drain-to-source on resistance	V_{GS} = 6 V, I_D = 5 A	—	58.0	72.0	mΩ
		V_{GS} = 10 V, I_D = 5 A	—	49.0	59.0	
g_{fs}	Transconductance	V_{DS} = 10 V, I_D = 5 A	—	6.1	—	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 50 V, f = 1 MHz	—	349.0	454.0	pF
C_{oss}	Output capacitance		—	69.0	90.0	pF
C_{rss}	Reverse transfer capacitance		—	12.6	16.4	pF
R_G	Series gate resistance	—	—	4.6	9.2	Ω
Q_g	Gate charge total (10 V)	V_{DS} = 50 V, I_D = 5 A	—	4.3	—	nC
Q_{gd}	Gate charge gate-to-drain		—	0.8	—	nC
Q_{gs}	Gate charge gate-to-source		—	1.6	—	nC
$Q_{g(th)}$	Gate charge at V_{th}		—	1.0	—	nC
Q_{oss}	Output charge	V_{DS} = 50 V, V_{GS} = 0 V	—	12.3	—	nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 50 V, V_{GS} = 10 V, I_{DS} = 5 A, R_G = 0 Ω	—	5.0	—	ns
t_r	Rise time		—	3.0	—	ns
$t_{d(off)}$	Turnoff delay time		—	7.0	—	ns
t_f	Fall time		—	2.0	—	ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 5 A, V_{GS} = 0 V	—	0.85	1	V
Q_{rr}	Reverse recovery charge	V_{DS}= 50 V, I_F = 5 A, di/dt = 300 A/µs	—	94.00	—	nC
t_{rr}	Reverse recovery time		—	32.00	—	ns

(1) T_A = 25°C

Power lost due to gate switching is computed as shown in 式 4.

$$P_{GATE} = V_{GS} \times Q_{GS} \times f_{SW} = 8.5 \times 1.6 \times 10^{-9} \times 100000 = 1.36 \text{ mW} \quad (4)$$

2.3.1.3.3 MOSFET Switching Losses

During turnon and turnoff, the gate voltage rises slowly as the input capacitance charges, this results in switching loss across MOSFET. These losses can be computed independently for turn on and turn off by computing timing of each phase. As shown in 図 15 and 図 16, during turnon initially the input capacitance charges until the gate potential reaches the gate threshold voltage. After reaching the threshold, the drain current starts to increase until the gate voltage reaches Miller voltage. After reaching Miller voltage, the drain-to-source voltage falls as the gate-to-drain capacitance charges. Switching losses are in the region between the threshold voltage to Miller voltage and from the Miller voltage to the fall of the drain-to-source voltage.

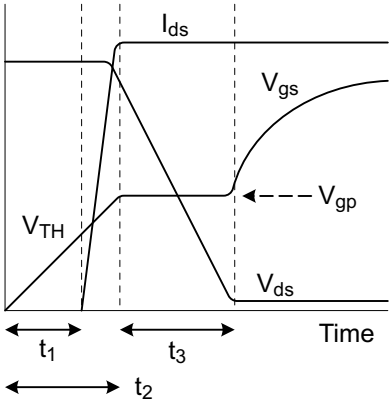


図 15. MOSFET Turnon Characteristics

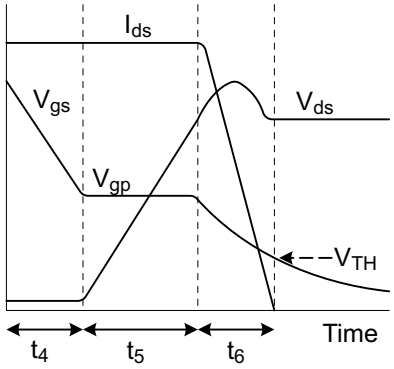


図 16. MOSFET Turnoff Characteristics

To compute the timings, the gate threshold voltage and plateau voltage need to be computed. From the MOSFET datasheet, gate voltage is computed using a two-point equation (see 図 17 and 式 5).

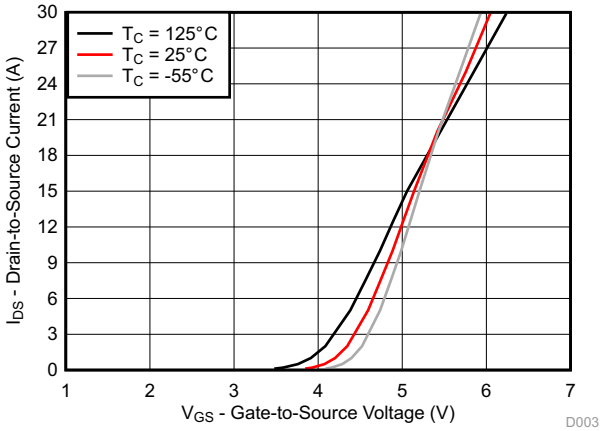


図 17. MOSFET Transfer Characteristics

$$V_{TH} = \frac{V_{GS1} \times \sqrt{I_{D2}} - V_{GS2} \times \sqrt{I_{D1}}}{\sqrt{I_{D2}} - \sqrt{I_{D1}}} = \frac{4.5 \times \sqrt{28} - 6 \times \sqrt{3}}{\sqrt{28} - \sqrt{3}} = 3.77\ V \quad (5)$$

The Miller voltage is computed as shown in 式 6.

$$V_P = V_{TH} + \sqrt{\frac{I_1}{K}} = 3.77 + \sqrt{\frac{\frac{0.07968}{I_{D1}}}{(V_{GS1} - V_{TH})^2}} = 3.77 + \sqrt{\frac{\frac{0.0905}{3}}{(8 - 3.77)^2}} = 4\ V \quad (6)$$

With the gate threshold and Miller voltage computed, turnon timings t_1, t_2, and t_3 are shown in 式 7, 式 8, and 式 9, respectively.

$$t_1 = \left(R_g + R_{ext}\right) \times C_{iss} \times \ln\left(\frac{1}{1-\left(\frac{V_{TH}}{V_{GS}}\right)}\right) = (4.6 + 4.7) \times 349\ \text{pF} \times \ln\left(\frac{1}{1-\left(\frac{1}{1-\left(\frac{3.77}{8.5}\right)}\right)}\right) = 1.9\ \text{ns} \tag{7}$$

$$t_2 = \left(R_g + R_{ext}\right) \times C_{iss} \times \ln\left(\frac{1}{1-\left(\frac{V_P}{V_{GS}}\right)}\right) = (4.6 + 4.7) \times 349\ \text{pF} \times \ln\left(\frac{1}{1-\left(\frac{4}{8.5}\right)}\right) = 1.98\ \text{ns} \tag{8}$$

$$t_3 = \left(R_g + R_{ext}\right) \times C_{GD} \times \frac{V_{MIN}}{\left(V_{GS} - V_{GP}\right)} = (4.6 + 4.7) \times 12.6\ \text{pF} \times \frac{12}{(8.5 - 3.89)} = 305\ \text{ps} \tag{9}$$

With timings t_1, t_2, and t_3 computed, power loss during turnon time is calculated using 式 10.

$$P_{ton} = \left(V_{IN} \times \frac{(n \times I_0)}{2} \times (t_2 - t_1) \times f_{SW}\right) + \left(n \times I_0 \times \frac{(V_{IN})}{2} \times t_3 \times f_{SW}\right) = 18.4\ \mu\text{W} \tag{10}$$

Similarly, the turnoff timings t_4, t_5, t_6, and turnoff loss is computed as shown in 式 11, 式 12, and 式 13.

$$t_4 = \left(R_g + R_{ext}\right) \times C_{iss} \times \ln\left(\frac{V_{GS}}{V_P}\right) = (4.6 + 4.7) \times 349\ \text{pF} \times \ln\left(\frac{12}{4}\right) = 3.65\ \text{ns} \tag{11}$$

$$t_5 = \left(R_g + R_{ext}\right) \times C_{GD} \times \frac{V_{DS}}{V_P} = (4.6 + 4.7) \times 12.6\ \text{pF} \times \frac{12}{4} = 361\,\text{ps} \tag{12}$$

$$t_6 = \left(R_g + R_{ext}\right) \times C_{iss} \times \ln\left(\frac{V_P}{V_{TH}}\right) = (4.6 + 4.7) \times 349\ \text{pF} \times \ln\left(\frac{4}{3.77}\right) = 1001\,\text{ps} \tag{13}$$

With timings t_4, t_5, and t_6 computed, power loss during turnoff time is calculated using 式 14.

$$P_{toff} = \left(n \times I_0 \times \frac{(V_{IN})}{2} \times t_5 \times f_{SW}\right) + \left(V_{IN} \times \frac{(n \times I_0)}{2} \times t_6 \times f_{SW}\right) = 22.1\,\mu\text{W} \tag{14}$$

The total power loss in MOSFET is calculated using 式 15:

$$P_T = P_{cond} + P_{GATE} + P_{ton} + P_{toff} = 1.7\ \text{mW} \tag{15}$$

2.3.1.4 LDO Using TL431

The regulated gate drive supply and peripheral supply are generated using a discrete LDO designed with the TL431. This peripheral supply can be used to power up the MCU, op amp, and other peripherals in a burner control system. In this reference design, the LDO powers up the sine wave oscillator. The components in the gate drive supply as shown in 図 18 is computed as per Section 2.2.2.1 of the TIDA-01065 design guide with a feedback current of 50 µA. The capacitor C_{13} is introduced for stability by adding zero in the feedback loop. This capacitor improves the phase margin and reduces oscillation in output.

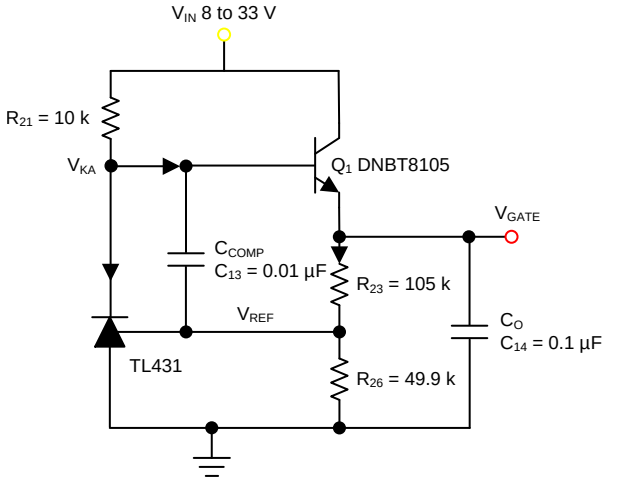


図 18. Gate Voltage Supply

The peripheral LDO is designed with an output current of 1 mA and 5 V. The values of discrete components as shown in 図 19 are computed as per Section 2.2.2.1 of the TIDA-01065 design guide with a feedback current of 50 µA. The capacitor C_{13} is introduced for stability by adding zero in the feedback loop. This capacitor improves the phase margin and reduces oscillation in output.

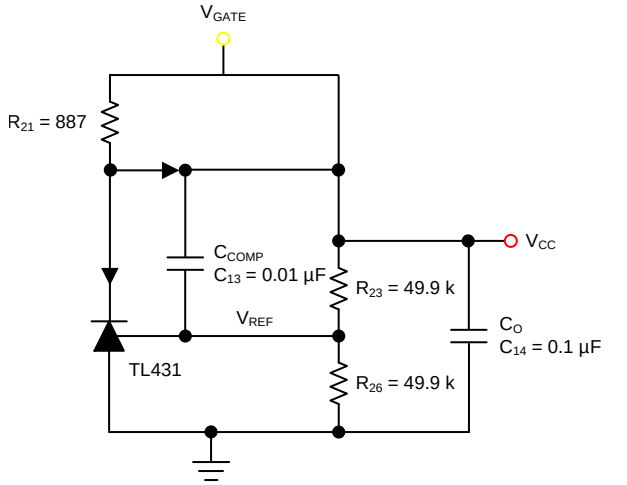
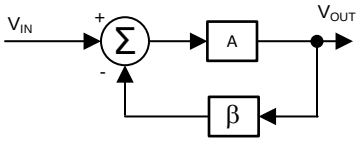


図 19. Peripheral Supply

2.3.1.5 Sine Wave Oscillator

In this reference design, a sine wave oscillator is used to generate a 50-Hz line signal by using a low THD+noise op amp. With this approach, it is possible to produce very low distorted output. As show in 図 20, the oscillator must satisfy the criteria for a closed loop positive feedback for the circuit to oscillate. Due to positive feedback, the denominator value becomes zero, resulting in instability known as Barkhausen Criterion. In unstable mode, the output of circuit tends to infinity due to the limitation of the power rail in circuit output will saturate to rail supply. For active devices, the gain of the circuit changes as output approaches the supply rail. This results in a change of value A and forces Aβ away from the singularity. Due to this change, trajectory towards power rail slows and eventually halts.



$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + A\beta}$$

$$\text{if } A\beta = -1 = 1\angle -180$$

図 20. Oscillator Control Loop

At this point, any one of these three possible conditions can occur:

- Nonlinearity in saturation or a cutoff region may result to become stable and latch at a particular output
- Initial change may cause the active device to be saturated or cut off for a long period before becoming linear and then moving to an opposite rail
- The circuit stays linear and reverses polarity to an opposite rail

The second condition results in a distorted output and is usually preferred for generating quasi square wave signals, while the third conditions produces sine wave output. The gain and phase of the circuit play a critical role for designing a sine way oscillator. For an op-amp based circuit, the phase margin of the op amp must be negligible so that the closed loop positive feedback archives ∡-180 phase shift at oscillating frequency. Considering these conditions, the closed loop gain, phase shift, THD distortion, and slew rate are some key parameters for selecting an op amp to design sine wave oscillators.

This reference design uses a single-supply Wein bridge oscillator. The classic Wein bridge oscillator has both positive and negative feedback. This helps in getting a very low distorted output. For analysis, consider the circuit as shown in 図 21. The circuit operating can be modeled as a non-inverting amplifier.

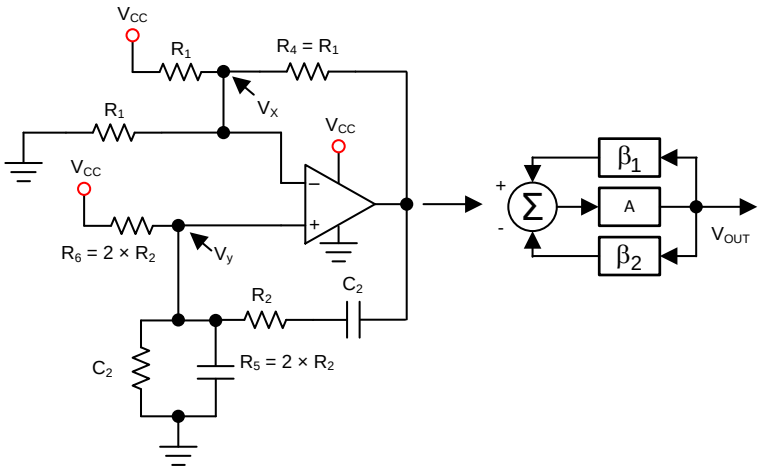


図 21. Sine Wave Oscillator for Op Amp

Voltage at the positive terminal of the op amp is given using 式 16.

$$V_y = V_O \times \left(\frac{sR_2C_2}{1 + 3sR_2C_2 - (sR_2C_2)^2} \right) \tag{16}$$

A simple form of 式 16 in a frequency parameter is given using 式 17.

$$\beta = \frac{V_y}{V_O} = \left(\frac{1}{3 + j\left(\frac{f}{f_{R_2C_2}} - \frac{f_{R_2C_2}}{f} \right)} \right), \text{ where } f_{R_2C_2} = \frac{1}{2\pi R_2C_2} \tag{17}$$

From a classic non-inverting amplifier, the closed loop gain equation ignoring the dominant pole effect at a low frequency is given using 式 18.

$$V_O = V_y \times \left(1 + \frac{R_4}{R_1} \right) \tag{18}$$

As a result, the forward gain is found using 式 19.

$$A = \frac{V_O}{V_y} = \left(1 + \frac{R_4}{R_1} \right) \tag{19}$$

The total loop gain is given using 式 20.

$$T(jf) = A\beta = \frac{\left(1 + \frac{R_4}{R_1} \right)}{\left(3 + j\left(\frac{f}{f_{R_2C_2}} - \frac{f_{R_2C_2}}{f} \right) \right)} \tag{20}$$

These equations imply system response of bandpass filter, at higher and lower frequency it approaches to zero and at peak frequency of f = f_{R2C2}, the total loop gain reduces to:

$$t_{(jf_{R_2C_2})} = \frac{\left(1 + \frac{R_4}{R_1} \right)}{3} \tag{21}$$

The magnitude of the total loop gain has three possibilities:

- $T(jf_{R_2C_2}) < 1$: The pole pair lies in the left half of the complex plane, resulting in an exponentially decaying signal.
- $T(jf_{R_2C_2}) > 1$: This condition results in unstable operation, resulting in oscillation of growing amplitude. The pole pair lies on the right half of a complex plane. The oscillation builds up until the op amp saturates to the power rail. This condition results in a distorted output.
- $T(jf_{R_2C_2}) = 1$: This condition results in neutral stability. The pole pair lies exactly on an imaginary axis of the complex plane. It satisfies the Barkhausen criterion of the loop gain of unity and a phase shift of 360°. The output is sinusoidal with very low distortion. For this condition, the R_4/R_1 ratio needs to satisfy a magnitude of 2.

Due to the drift of active and passive devices, the total loop gain does not maintain a magnitude of value 1, so modify the circuit as shown in 図 22 to achieve automatic gain control (AGC). At initial startup condition, diodes D_1, D_2, and R_3 result into condition $T(jf_{R2C2}) > 1$, resulting into oscillations quickly building up. After the oscillation has built up, the gain stabilizes to match the Barkhausen criteria due to effective resistors R3 and R4, which are in parallel to achieve a ratio close to a magnitude of 2.

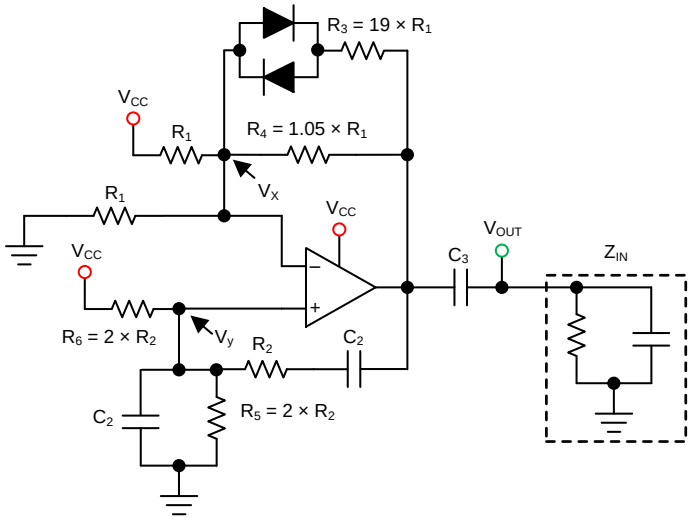


図 22. Practical Op Amp Oscillator

Select an op amp that has very low distortion for oscillating frequency, low noise, and enough of a slew rate to achieve sustain oscillation. The closed loop bandwidth needs to be greater than 270 f_{OSC}. Therefore, for a 50-Hz f_{OSC} signal, the sine wave oscillator needs a closed-loop bandwidth greater than 13.5 kHz and a slew rate of $> 2\pi f_{OSC} V_O$. Selecting TLV171 from the device datasheet gets a unity gain bandwidth of 3 MHz and a typical open loop gain of 130 dB.

表 5. TLV171 Electrical Characteristic

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	T_A = 25°C	—	0.75	±2.7	mV
		T_A = –40°C to +125°C	—	—	±3.0	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C	—	1	—	µV/°C
PSRR	Input offset voltage vs power supply	V_S = 4 V to 36 V, T_A = –40°C to +125°C	90	105	—	dB
INPUT BIAS CURRENT						
I_B	Input bias current	—	—	±10	—	pA
I_{OS}	Input offset current	—	—	±4	—	pA
NOISE						
	Input voltage noise	f = 0.1 Hz to 10 Hz	—	3	—	μV_{PP}
e_n	Input voltage noise density	f = 100 Hz	—	27	—	$nV/\sqrt{Hz}$
		f = 1 kHz	—	16	—	
INPUT VOLTAGE						
V_{CM}	Common-mode voltage range	—	(V–) – 0.1	—	(V+) – 2	V
CMRR	Common-mode rejection ratio	V_S = ±18 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V, T_A = –40°C to +125°C	94	105	—	dB
INPUT IMPEDANCE						
	Differential	—	—	100 || 3	—	MΩ || pF
	Common-mode	—	—	6 || 3	—	10^{12} Ω || pF

表 5. TLV171 Electrical Characteristic (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_S = 36 V, (V–) + 0.35 V < V_O < (V+) – 0.35 V, T_A = –40°C to +125°C	94	130	—	dB
FREQUENCY RESPONSE						
GBP	Gain bandwidth product	—	—	3.0	—	MHz
SR	Slew rate	G = +1	—	1.5	—	V/µs
t_S	Settling time	To 0.1%, V_S = ±18 V, G = +1, 10-V step	—	6	—	µs
		To 0.01% (12 bits), V_S = ±18 V, G = +1, 10-V step	—	10	—	
	Overload recovery time	V_{IN} × gain > V_S	—	2	—	µs
THD+N	Total harmonic distortion + noise	G = +1, f = 1 kHz, V_O = 3 V_{RMS}	—	0.0002%	—	—

As a result, the dominant pole frequency of the TLV171 is given using 式 22.

$$f_{dom} = \frac{f_{unity}}{10^{\frac{130}{20}}} = 0.948\ \text{Hz} \tag{22}$$

The closed loop AC gain for a non-inverting topology with a feedback factor of 1/3 at a frequency of 15 kHz is given using 式 23.

$$A_{cl} = \frac{\frac{A_{DC\_OPEN}}{1+\beta \times A_{DC\_OPEN}}}{\sqrt{1+\frac{f^2}{f_{dom}^2}\frac{1}{\left(1+\beta A_{DC\_OPEN}\right)^2}}} = \frac{\frac{3162277}{1+0.33\times 3162277}}{\sqrt{1+\left(\frac{15000^2}{0.948^2}\right)\times\left(\frac{1}{\left(1+0.33\times 3162277\right)^2}\right)}} = 3.029 \tag{23}$$

So the TLV171 meets approximately a closed loop gain of 3. Calculate the phase margin error using 式 24 to get a phase error of 0.003°.

$$\phi = 90^\circ - \left(\tan^{-1}\frac{f}{f_{dom}}\right) = 0.003^\circ \tag{24}$$

From the slew rate requirement, considering an output voltage of 4 V and a 50-Hz f_{OSC} slew rate needs to be greater than 1.25 mV/µs (ignoring asymmetric slew rate error in non-inverting mode due to a common-mode parasitic).

$$SR > 2\pi \times f_{OSC} \times V_O \times 10^{-6} = 2\pi \times f_{OSC} \times V_O \times 10^{-6} > 1.25\ \frac{mV}{\mu s} \tag{25}$$

By cross verifying with the TLV171 FPB, check that the slew rate satisfies the closed loop bandwidth requirement by using 式 26.

$$FPB = \frac{SR\ \text{in}\ \frac{V}{\mu s}}{2\pi \times V_O} = \frac{1.5\times 10^6}{8\pi} = 59.7\ \text{kHz} \tag{26}$$

2.3.1.6 High Gain Amplifier

To achieve a 120-V sine wave output, there needs to be an amplifier; this amplifier can be a topology like Class A, Class AB, and so on. To achieve the cost target, a Class A amplifier has been implemented in this reference design. Class AB can be implemented to achieve high efficiency and low distortion with a filter circuit. A Class A amplifier as shown in 図 23 operates in the linear operating region, due to which output distortion are low. In a Class A amplifier, additional quiescent current is required to bias the transistor in the operating region. Calculate the bias point to achieve linear output. This reference design uses the BSS127-S N-channel, high-voltage, low-cost MOSFET to design this Class A amplifier.

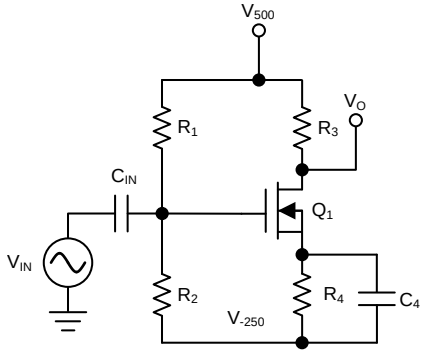
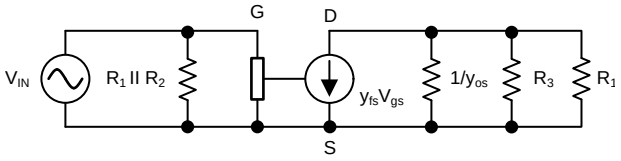


図 23. Class A Amplifier

Resistors R_1 and R_2 provide bias voltage to Q1. To calculate R_1 and R_2, first calculate the Q point of Q1 for the required gain. The AC equivalent of a circuit is as shown in 図 24.



y_{fs} : Forward tans conductance
$1/y_{os}$: Output Admittance
A_v : $y_{fs} \times (R_1 \text{ II } R_3 \text{ II } 1/y_{os})$

図 24. AC Equivalent Circuit

The drain current of the MOSFET is parabolic in nature, so the drain current is given using 式 27.

$$I_{ds} = K \times (V_{GSON} - V_{GSOFF})^2 \quad (27)$$

Solving 式 27 for V_{GSON} = 10 V, V_{GSOFF} = 3 V, and I_{ds} = 16 mA from the datasheet, compute K as shown in 式 28.

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	600	—	—	V	V_{GS} = 0V, I_D = 250µA
Zero Gate Voltage Drain Current T_J = +25°C	I_{DSS}	—	—	0.1	µA	V_{DS} = 600V, V_{GS} = 0V
Gate-Body Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(TH)}$	3	—	4.5	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	80	160	Ω	V_{GS} = 10V, I_D = 16mA
		—	95	190		V_{GS} = 5.0V, I_D = 16mA
Forward Transfer Admittance	$\|Y_{fs}\|$	—	76	—	mS	V_{DS} = 10V, I_D = 16mA
Diode Forward Voltage	V_{SD}	—	—	1.5	V	V_{GS} = 0V, I_S = 16mA
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	—	21.8	—	pF	V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	2.2	—		
Reverse Transfer Capacitance	C_{rss}	—	0.3	—		
Total Gate Charge	Q_g	—	1.08	—	nC	V_{GS} = 10V, V_{DD} = 300V, I_D = 0.01A
Gate-Source Charge	Q_{gs}	—	0.08	—		
Gate-Drain Charge	Q_{gd}	—	0.50	—		
Turn-On Delay Time	$t_{D(ON)}$	—	5.0	—	ns	V_{DD} = 300V, V_{GS} = 10V, R_{GEN} = 6Ω, I_D = 10mA
Turn-On Rise Time	t_R	—	7.2	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	28.7	—	ns	
Turn-Off Fall Time	t_F	—	168	—	ns	
Reverse Recovery Time	t_{RR}	—	131	—	ns	V_R =300V, I_F =0.016A, di/dt = 100A/µs
Reverse Recovery Charge	Q_{RR}	—	32	—	nC	

Notes:
5. Device mounted on FR-4 PCB with minimum recommended pad layout, single sided.
6. Device mounted on 1" x 1" FR-4 PCB with high coverage 2 oz. Copper, single sided.
7. Repetitive rating, pulse width limited by junction temperature, 10µs pulse, duty cycle = 1%.
8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to production testing.

図 25. MOSFET Electrical Characteristics

$$k = \frac{dI_{dsq}}{dV_{GSq}} = 2 \times K \times \left(V_{GSq} - V_{GSOFF}\right) \tag{28}$$

The transconductance of the MOSFET is found by taking the derivative of the transfer function for the drain current at a bias point of the amplifier.

$$y_{fq} = \frac{dI_{dsq}}{d_{V_{GSq}}} = 2 \times K \times \left(V_{GSq} - V_{GSOFF}\right) \tag{29}$$

Assuming the high load resistance and output admittance is sufficiently high, the impedance seen by the MOSFET is almost equal to R3. For a good biasing point, it is good to bias the output at half of the supply rails. As a result, the drain resistance is given using 式 30.

$$R_3 = 0.5 \times \frac{\left(V_{DD} + V_{SS}\right)}{I_{DQ}} \tag{30}$$

By substituting R_3 and y_{fq} for the total gain in 式 31:

$$A_{vq} = y_{fq} \times R_3 = 2 \times K \times \left(V_{GSq} - V_{GSOFF}\right) \times 0.5 \frac{\left(V_{DD} - V_{SS}\right)}{I_{DQ}} \tag{31}$$

Rearranging the terms for I_{DQ} leads to 式 32 :

$$I_{DQ} = \frac{2 \times K \times \left(V_{GSq} - V_{GSOFF}\right) \times 0.5 \times \left(V_{DD} - V_{SS}\right)}{A_{vq}} \tag{32}$$

Solving 式 27 and 式 32 graphically with V_{dd} of 500 V, V_{GSOFF} = 3 V and a gain of 330, bias points V_{GSq} and I_{GSq} can be computed using interpret of two curves (see 図 26).

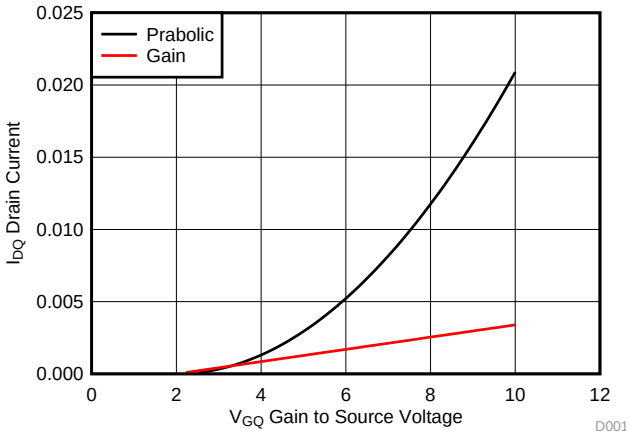


図 26. Bias Point Calculations

図 26 shows that the curve intercepts the x-axis at 3.3 V and the y-axis at 551 µA. So the bias point for BSS127-S is V_{GSQ} = 3.3 V and I_{DQ} = 551 µA.

Solving the equation with I_{DQ} = 551 µA results in R_3 = 442 k. Selecting a closed standard value of 442 kV at the source can be set close to 0.09 times the supply rail. Computing for a V_{dd} of 500 V and I_{DQ} = 551 µA results in R_4 = 82 k. Selecting the next standard resistor with a 5% tolerance we select 88.7k. With 88.7k and I_{DQ} = 551 µA, the source voltage is 48.8 V. Adding the gate-to-source bias voltage, the gate voltage needs to be 52.1 V. Using voltage divider logic, R1 and R2 can be easily computed for a low-bias current. Assuming an R_2 of 2.2 MΩ and a supply rail V_{dd} of 500 V, the required resistance R_1 is 18 MΩ. The nearest standard value to select is 18 MΩ. Capacitance C_4 is a bypass capacitor for a higher AC gain value. To calculate C4, assume impedance by capacitance for a 50-Hz frequency as 0.1 times of R4.

$$X_C = 0.1 \times R_4 = 8.8\,k \tag{33}$$

By knowing the impedance of a capacitor at a specific frequency, it is easy to calculate capacitance using 式 34.

$$C_4 = \frac{1}{2\pi f X_C} = 361\,nF \tag{34}$$

The next standard value selected is a 470-nF capacitor. Capacitance C_{in} is a high-pass-filter capacitor that blocks DC level from the oscillator output. The parallel resistance value of resistors R1 and R2 with C_{in} together form the high pass filter. By selecting a cutoff frequency of 5 Hz, compute C_{in} as per 式 35.

$$C_{in} = \frac{1}{2\pi f_C \times 0.1 \times \left(R_1 \| R_2\right)} = 162\,nF \tag{35}$$

The next standard value of 220 nF is selected for the input filter capacitor.

3 Hardware, Testing Requirements, and Test Results

3.1 Hardware

Before powering up the TIDA-01426 board, verify for any components not populated as per the schematic. Check for power nodes and shock hazard symbols to avoid electric shocks as shown in 図 27.

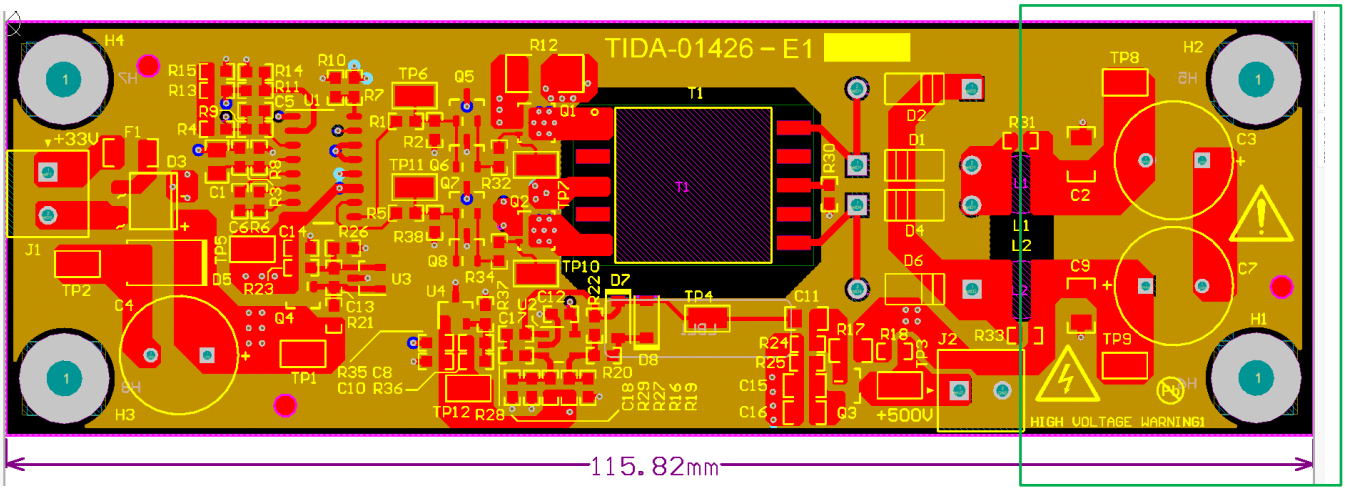


図 27. High-Voltage Section

3.1.1 Connectors

The interface board has two connectors as described in 表 6.

表 6. Input Output Connectors

CONNECTOR	DESCRIPTION	VOLTAGE
J1	Input voltage	12 to 36 V
J2	Output voltage	120 V_{RMS}, 60 Hz

3.1.2 Test Points

The required test points have been populated on the interface board to measure signals. See 表 7 for more details.

表 7. Test Points

TEST POINT NO	DESCRIPTION	VOLTAGE VALUE
TP1	Supply voltage	12 to 36 V
TP2, TP9	GND	0 V
TP5	Gate supply	8 V
TP12	Op amp supply	5 V
TP4	Sine wave oscillator	1.5 V_{RMS}, 60 Hz
TP3	Class A amplifier output	120 V_{RMS}, 60 Hz
TP6	Emitter 1 output	7-V, 100-kHz PWM
TP11	Emitter 2 output	7-V, 100-kHz PWM
TP7	Totem Pole 1 output	8-V ,100-kHz PWM
TP10	Totem Pole 2 output	8-V, 100-kHz PWM
TP8	Positive high voltage	500 V

The test setup is as shown in 図 28. Ensure the board is placed inside a safety enclosure to prevent any shock or short-circuit hazard.

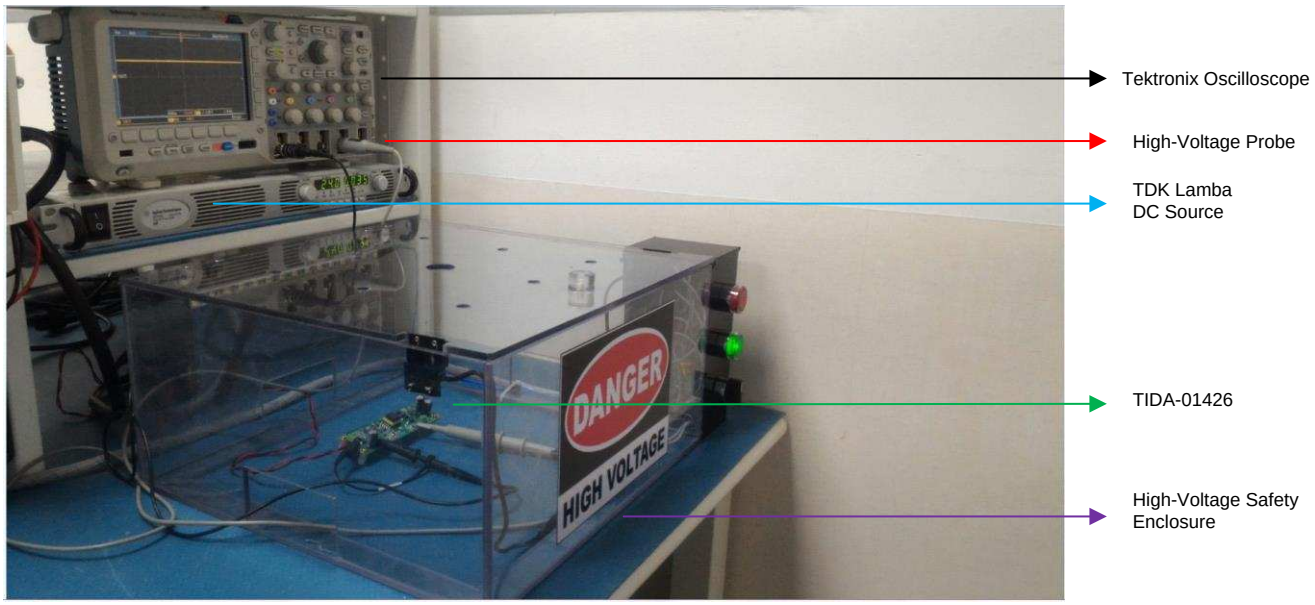


図 28. Test Setup

3.2 Testing and Results

3.2.1 Gate Supply

The following figures show the gate output voltage changes as the line voltage changes from the minimum supply to the maximum supply.

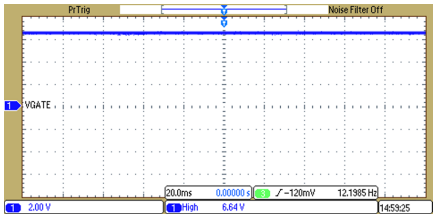


図 29. Gate Supply at 12 V_{IN}

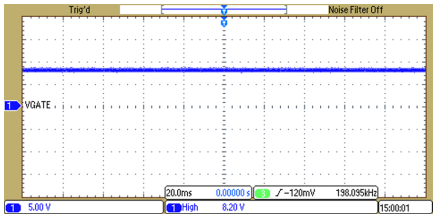


図 30. Gate Supply at 24 V_{IN}

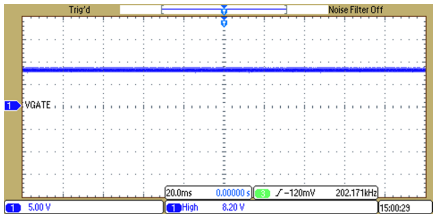


図 31. Gate Supply at 33 V_{IN}

3.2.2 LDO Supply

The following figures show the LDO output voltage as the line voltage changes from the minimum supply to the maximum supply.

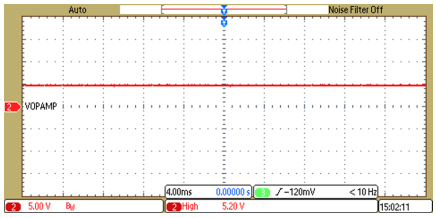


図 32. LDO Supply at 12 V_{IN}

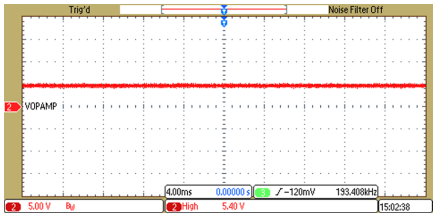


図 33. LDO Supply at 24 V_{IN}

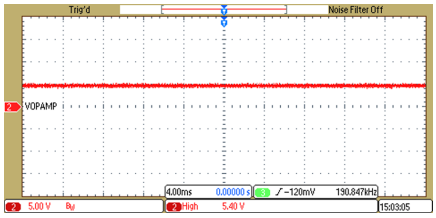


図 34. LDO Supply at 36 V_{IN}

3.2.3 Push-Pull Output

The start-up time for 500 V is tested at the lowest input supply. Yar gets a start-up time of 100 ms to achieve 55 ms as shown in 図 35.

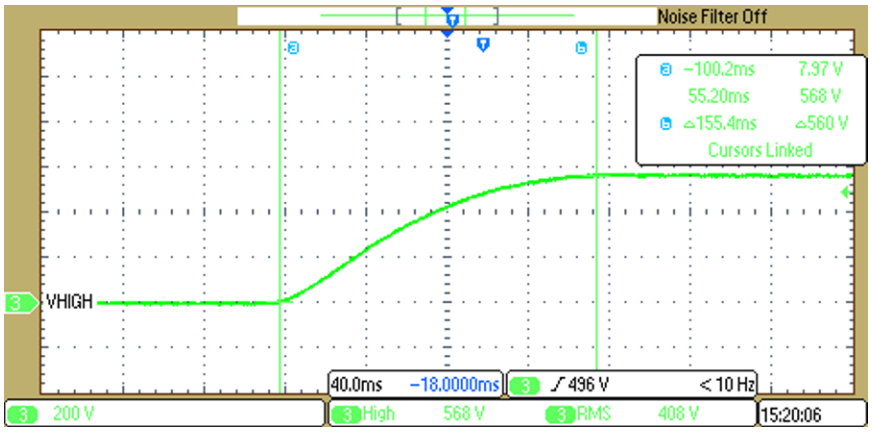


図 35. Start-up Time

3.2.4 Sensor Output

Sensor output is measured at a 24-V input, and the FFT plot is taken to verify harmonic content (see 図 36).

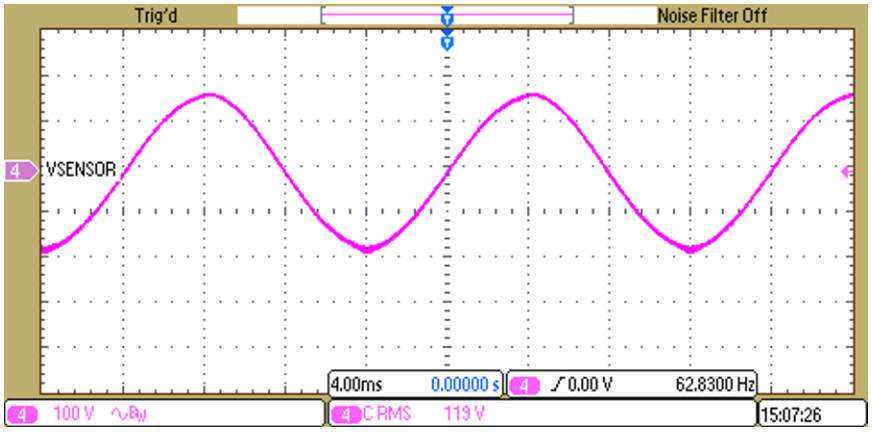


図 36. Sensor Output

As seen from 図 37, the peak is at 63 Hz with a 42-dB magnitude and harmonics with magnitudes of 7 dB, –18 dB, –12 dB, and –5 dB. The THD computed for an observed output is 1.8%.

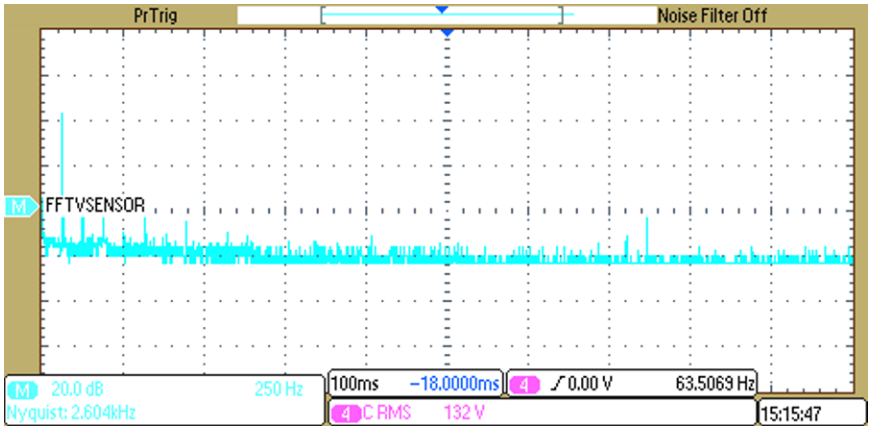


図 37. FFT Plot Sensor Output

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01426.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01426.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01426.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01426.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01426.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01426.

5 Software Files

To download the software files, see the design files at TIDA-01426.

6 Related Documentation

1. Texas Instruments, *Designing Switching Voltage Regulators With the TL494*, TL494 Application Report (SLVA001)

6.1 商標

7 About the Authors

SRINIVASAN IYER is a systems engineer at Texas Instruments India, where he is responsible for developing reference design solutions for the industrial segment. Srinivasan has six years of experience in power supply and analog circuit designs for field transmitter and signal chain. Srinivasan received his BE from the University of Pune, India.

MIROSLAV OLJACA is the end equipment manager for Building Automation applications and system solutions. Miro has nearly 30 years of engineering experience and has been granted at least a dozen patents, several related to high-performance signal processing, and he has written many articles on the subject. Miro received his BSEE and MSEE from the University of Belgrade, Serbia.

TIの設計情報およびリソースに関する重要な注意事項

Texas Instruments Incorporated ("TI")の技術、アプリケーションその他設計に関する助言、サービスまたは情報は、TI製品を組み込んだアプリケーションを開発する設計者に役立つことを目的として提供するものです。これにはリファレンス設計や、評価モジュールに関係する資料が含まれますが、これらに限られません。以下、これらを総称して「TIリソース」と呼びます。いかなる方法であっても、TIリソースのいずれかをダウンロード、アクセス、または使用した場合、お客様(個人、または会社を代表している場合にはお客様の会社)は、これらのリソースをここに記載された目的にのみ使用し、この注意事項の条項に従うことに合意したものとします。

TIによるTIリソースの提供は、TI製品に対する該当の発行済み保証事項または免責事項を拡張またはいかなる形でも変更するものではなく、これらのTIリソースを提供することによって、TIにはいかなる追加義務も責任も発生しないものとします。TIは、自社のTIリソースに訂正、拡張、改良、およびその他の変更を加える権利を留保します。

お客様は、自らのアプリケーションの設計において、ご自身が独自に分析、評価、判断を行う責任がお客様にあり、お客様のアプリケーション(および、お客様のアプリケーションに使用されるすべてのTI製品)の安全性、および該当するすべての規制、法、その他適用される要件への遵守を保証するすべての責任をお客様のみが負うことを理解し、合意するものとします。お客様は、自身のアプリケーションに関して、(1) 故障による危険な結果を予測し、(2) 障害とその結果を監視し、および、(3) 損害を引き起こす障害の可能性を減らし、適切な対策を行う目的での、安全策を開発し実装するために必要な、すべての技術を保持していることを表明するものとします。お客様は、TI製品を含むアプリケーションを使用または配布する前に、それらのアプリケーション、およびアプリケーションに使用されているTI製品の機能性を完全にテストすることに合意するものとします。TIは、特定のTIリソース用に発行されたドキュメントで明示的に記載されているもの以外のテストを実行していません。

お客様は、個別のTIリソースにつき、当該TIリソースに記載されているTI製品を含むアプリケーションの開発に関連する目的でのみ、使用、コピー、変更することが許可されています。明示的または黙示的を問わず、禁反言の法理その他どのような理由でも、他のTIの知的所有権に対するその他のライセンスは付与されません。また、TIまたは他のいかなる第三者のテクノロジまたは知的所有権についても、いかなるライセンスも付与されるものではありません。付与されないものには、TI製品またはサービスが使用される組み合わせ、機械、プロセスに関連する特許権、著作権、回路配置利用権、その他の知的所有権が含まれますが、これらに限られません。第三者の製品やサービスに関する、またはそれらを参照する情報は、そのような製品またはサービスを利用するライセンスを構成するものではなく、それらに対する保証または推奨を意味するものでもありません。TIリソースを使用するため、第三者の特許または他の知的所有権に基づく第三者からのライセンス、あるいはTIの特許または他の知的所有権に基づくTIからのライセンスが必要な場合があります。

TIのリソースは、それに含まれるあらゆる欠陥も含めて、「現状のまま」提供されます。TIは、TIリソースまたはその仕様に関して、明示的か暗黙的かにかかわらず、他のいかなる保証または表明も行いません。これには、正確性または完全性、権原、続発性の障害に関する保証、および商品性、特定目的への適合性、第三者の知的所有権の非侵害に対する黙示の保証が含まれますが、これらに限られません。

TIは、いかなる苦情に対しても、お客様への弁護または補償を行う義務はなく、行わないものとします。これには、任意の製品の組み合わせに関連する、またはそれらに基づく侵害の請求も含まれますが、これらに限られず、またその事実についてTIリソースまたは他の場所に記載されているか否かを問わないものとします。いかなる場合も、TIリソースまたはその使用に関連して、またはそれらにより発生した、実際的、直接的、特別、付随的、間接的、懲罰的、偶発的、または、結果的な損害について、そのような損害の可能性についてTIが知らされていたかどうかにかかわらず、TIは責任を負わないものとします。

お客様は、この注意事項の条件および条項に従わなかったために発生した、いかなる損害、コスト、損失、責任からも、TIおよびその代表者を完全に免責するものとします。

この注意事項はTIリソースに適用されます。特定の種類の資料、TI製品、およびサービスの使用および購入については、追加条項が適用されます。これには、半導体製品(http://www.ti.com/sc/docs/stdterms.htm)、評価モジュール、およびサンプル(http://www.ti.com/sc/docs/sampterms.htm)についてのTIの標準条項が含まれますが、これらに限られません。