参考資料

TI Designs: TIDA-01474
低レイテンシ、高速のTI DLP®デジタル・プロジェクションのリファレンス・デザイン

TEXAS INSTRUMENTS

概要

このプロジェクションのリファレンス・デザインでは、最高120fps (Frames Per Second)の映像を、わずか1フレームの遅延で表示できる、DLP®テクノロジ・サブシステムを紹介します。このデザインは、DLP470NE 1080p DMD (デジタル・マイクロミラー・デバイス)を中心として、1920×1080の表示を120Hzで行います。このデザインはゲーム、ホームシアター、レーザーTV、シミュレーションなど、各種の最終機器に内蔵できます。
多くの個人用電子機器およびビデオ・シミュレーション・アプリケーションでは、高画質で動きが早いデータを表示し、映像ソースと投影される画像との間でシステム遅延の発生を避けるため、高いフレーム・レート、短いレイテンシのソリューションが必要です。

リソース

TIDA-01474	デザイン・フォルダ
DLP470NE	プロダクト・フォルダ
DLPC4422	プロダクト・フォルダ
DLPA100	プロダクト・フォルダ
TPS65145	プロダクト・フォルダ

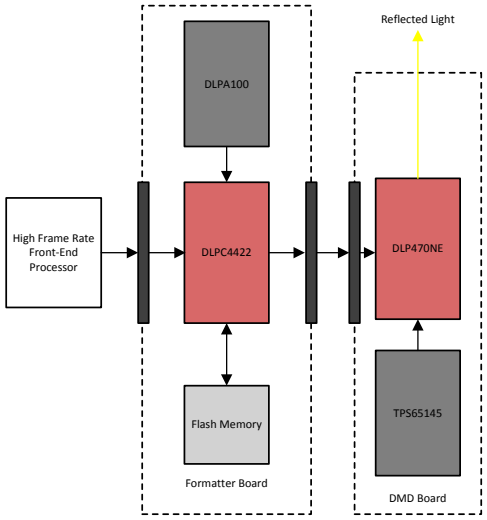
TI E2E™ Community　E2Eエキスパートに質問

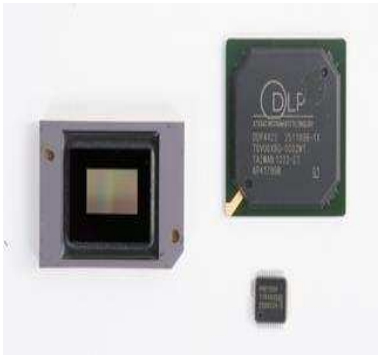
特長

- DLP470NEは、1920×1080またはフルHD 1080p解像度の画像を、50Hz、60Hz、100Hz、120Hzで生成可能
- 短いレイテンシの設計により、DLPC4422サブシステム全体を通してわずか1フレームの遅延
- 高いDMDの熱能力から、システムは4000ルーメンまでの輝度を実現可能
- PCソフトウェアGUIを使用して、DLPC4422ディスプレイ・コントローラをプログラム可能

アプリケーション

- テレビ、セットトップ・ボックス、オーディオを使用するレーザーTV
- プロジェクタを使用するホーム・シアター
- テレビ、セットトップ・ボックス、オーディオを使用するゲーム
- 宇宙、航空、防衛用のフライト・デッキ・ディスプレイ、ヘッドアップ・ディスプレイ(HUD)、フライト訓練シミュレータ





1 System Description

The DLP® 0.47-in 1080p high-speed, low-latency chipset combines the fast switching speed of the digital micromirror device (DMD) with unique image processing to enable display systems capable of creating 120-Hz full HD images with only one frame of delay through the TI subsystem. The TIDA-01474 reference design can be used for applications ranging from ultra-short throw laser TV with gaming applications in mind to flight training simulators and flight deck display solutions where up-to-date information and response time are critical. The chipset comprises the high-resolution DLP470NE DMD, the high-speed DLPC4422 digital controller, and dedicated DLPA100 power management integrated circuit (IC) and motor driver. Designers can combine these devices with many different optical and mechanical components to meet diverse display and performance-level requirements.

This reference design provides details on electrical component selection, high-speed data trace routing, electrical and software control of the DLP470NE DMD, as well as optical design choices such as illumination type and third-party optical engine information. The TIDA-01474 reference design explains how engineers and developers can incorporate this chipset to deliver high resolution and high brightness displays in an end product.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS		
	MINIMUM	NOMINAL	MAXIMUM
V_{IN} voltage	10.8 V	12 V	13.2 V
Power consumption	Overall system power consumption depends on light source and power design efficiency. The TI reference electronics subsystem, which does not include a light source, draws 10 W including fans.		
Required software	The software for DLPC4422 to control the DMD, fans, light source, and so forth are provided on TI.com. The system designer has the flexibility to control software features such as color coordinate adjustment, color space conversion, programmable degamma, and many other features. See *Software Files* for more information.		
DMD handling	See *PCB Design Requirements for DLP® Standard TRP Digital Micromirror Devices* for proper handling and installation of the DMD to avoid permanently damaging the device[5].		
DMD thermal load	The DMD is designed to absorb and dissipate heat on the back of the package. A cooling system is often required in system designs to maintain the DMD within the temperature range specified in the data sheet. For example, the array temperature must be kept between 10°C and 40°C or 10°C and 70°C for long-term operation depending on the desired DMD duty cycle. For more information, see the DLP470NE data sheet[1].		
DMD illumination wavelength and power for display applications	< 395 nm: maximum 2 mW/cm2		
	Between 395 nm and 800 nm: thermally limited		
	> 800 nm: maximum 10 mW/cm2		
Maximum projected lumens	4000 lm		
Display resolution	Up to full HD (1920 × 1080 pixels on screen)		
Supported light sources	Lamp, light-emitting diode (LED), direct laser, laser phosphor, and hybrid illumination		
Optical engine design	The DLP470NE supports both telecentric and non-telecentric optical engine designs		

2 System Overview

2.1 Block Diagram

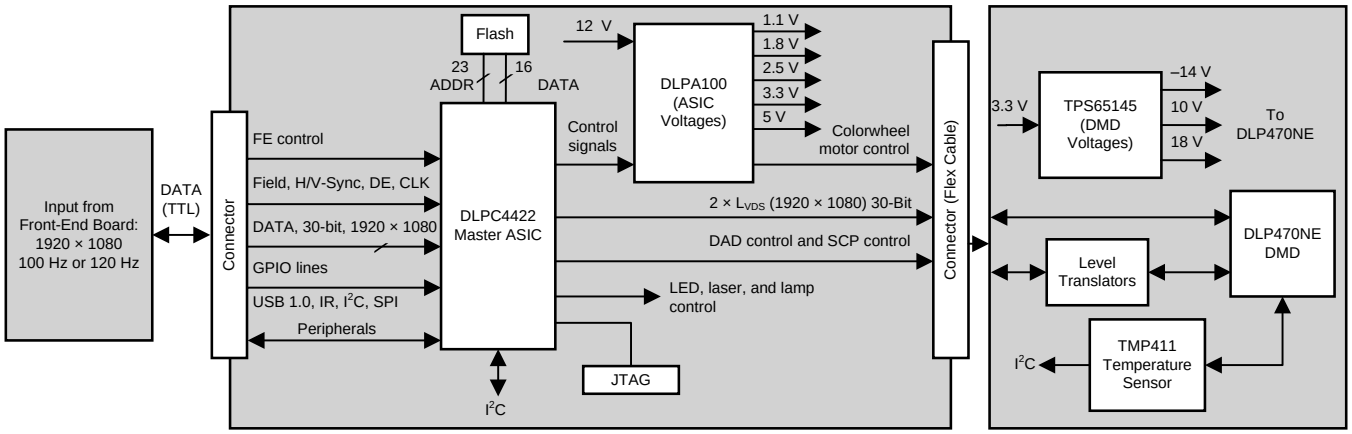


図 1. System Block Diagram

2.2 Applications

At the time of this writing, laser TV is an emerging group of products that offer large, bright projection by utilizing a laser light source. Laser light sources are considered longer lasting, more efficient, and more compact than traditional lamps. Laser TV can be incorporated into a wide array of electronic media devices such as a home-theater-in-a-box (HTiB), mobile smart TV, or mobile projectors. Furthermore, the low latency capabilities of this reference design provides a good pairing with video game consoles because limiting input delay from the controller to the screen is important to the video game experience. Due to the high brightness of the laser illumination source, laser TVs can provide a high-quality image or video with low latency without the requirement of a bulky screen. Developers interested in ultra-low-power solutions should reference DLP® Pico™ products.

The flight deck and aviation heads-up display is a key source of information with which pilots interact in an aircraft. This application must be able to display data with as little delay as possible. With this reference design, developers are able to use DLP technology to bring high-quality images at low latency to the pilot, which can allow the pilot to make the proper adjustments in a timely manner. The flexibility of the DLP470NE chipset makes it well suited for both flight deck display systems and ground-based flight training simulators.

2.3 Highlighted Products

2.3.1 DLP470NE

The DLP470NE DMD is based on the latest micromirror technology, called Tilt & Roll Pixel (TRP). With a small pixel pitch of 5.4 μm and increased tilt angle of 17º, TRP chipsets enable high resolution in a smaller form factor and enhanced image processing features while maintaining high optical efficiency. The block diagram in 図 2 shows a high-level view of the internal hardware control circuitry inside the DLP470NE DMD.

DLP470NE features:

- 0.47-in diagonal micromirror array
  - 1920×1080 array of aluminum micromirrors
  - 5.4-μm micromirror pitch
  - 17° micromirror tilt (relative to a flat surface)
  - Bottom illumination
- Two low-voltage differential signaling (LVDS) input data bus
- High thermal capacity up to 4k lumens

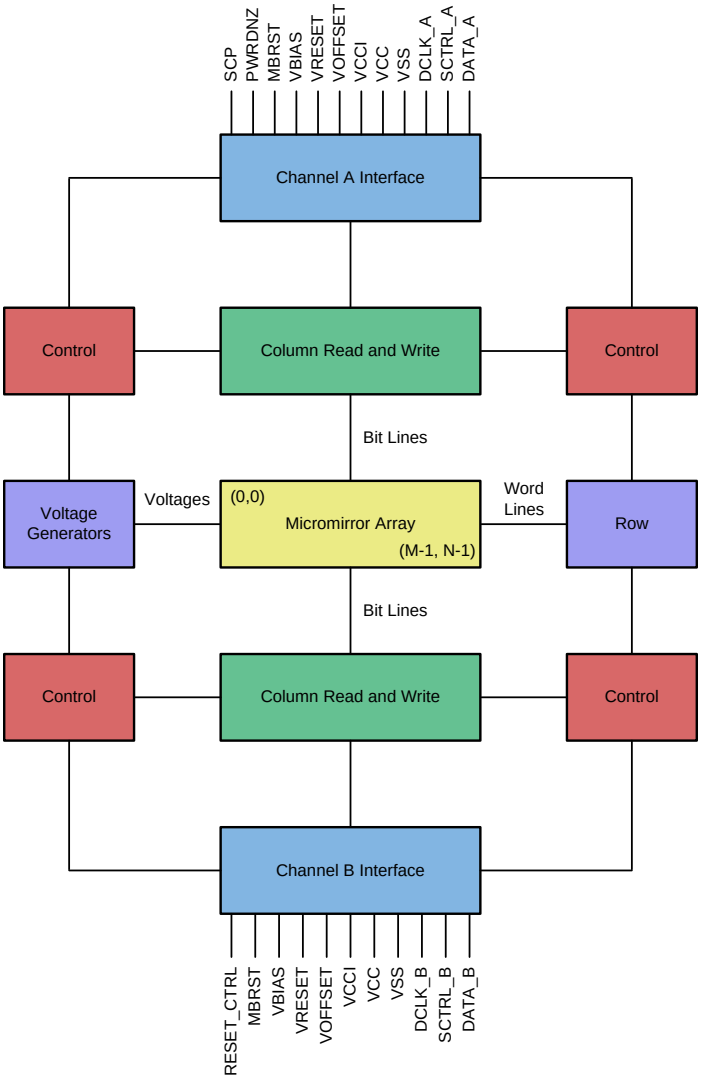


図 2. DLP470NE Block Diagram

2.3.2 DLPC4422

The DLPC4422 is a video and imaging controller chip that integrates all the DMD data formatting onto a single integrated circuit. The chip provides 1 Gb of internal dynamic random-access memory (DRAM) for all data path processing requirements. The DLPC4422 processes the digital input image and converts the data into bit-plane format as required by the DLP470NE device. The image data is 100% digital from the DLPC4422 input port to the image projected on the display screen. The image stays in digital form and is never converted into an analog signal.

This reference design utilizes a single DLPC4422 capable of handling all the high-speed image processing required to create a 1080p, 120-Hz image with only one frame of delay through the DLPC4422 controller. 図 3 shows a functional block diagram of the internal video processing provided by the DLPC4422 controller. Some of the important processing steps include chroma interpolation, color space conversion, and degamma. See the DLPC4422 data sheet for more information on these and other features.

The default operation of the DLPC4422 controller creates two to three frames of delay between the input of the controller and the image on the screen. In this reference design, the DLPC4422 controller delay is reduced to one frame to achieve low latency. To reduce the delay to one frame, the frame rate conversion feature of the controller must be disabled. With the frame rate conversion feature disabled, the DLPC4422 controller only accepts video input at 50 Hz, 60 Hz, 100 Hz, and 120 Hz. The input frame rate passes through the controller unchanged to the final projected image.

DLPC4422 features:

- Provides for two 30-bit input pixel ports, which can be used as one 60-bit port (two pixels per clock)
  - 8, 9, or 10 bits per color
  - Pixel clock support up to 175 MHz for 30-bit input pixel ports, 160 MHz for 60-bit input pixel ports
  - High-speed LVDS DMD interface
- Microprocessor peripherals:
  - 83 original equipment manufacturer (OEM) programmable general-purpose input/output (GPIO) pins
  - Programable pulse-width modulation (PWM) and capture timers
  - One USB 1.1 slave port
- System control
  - Built-in lamp ballast control
  - DMD power and reset driver control
  - DMD horizontal and vertical image flip
  - Supports lamp, hybrid, light-emitting diode (LED), and laser systems

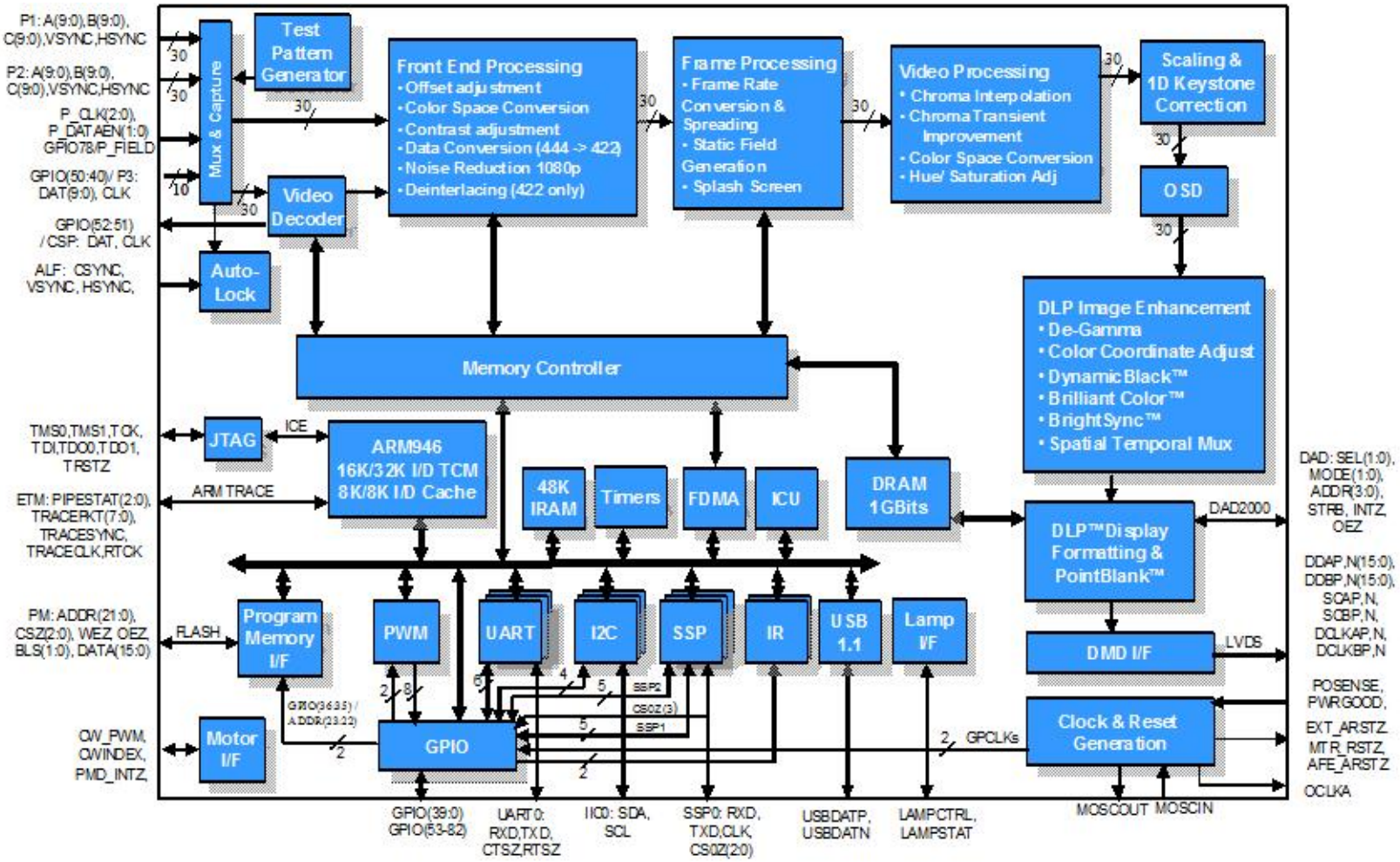


図 3. DLPC4422 Block Diagram

2.3.3 DLPA100

The DLPA100 is a power management solution and motor driver in one integrated circuit. The DLPA100 provides multiple linear and switching power regulators to power the DLP470NE, the DLPC4422, and other electronics in the TIDA-01474 reference design. The DLPA100 also contains a three-phase, back electromotive force (BEMF) motor driver and a motor supply switching regulator to power, spin, and control color-wheels and phosphor-wheels if required in an end equipment design. 図 4 shows a functional block diagram of the internal logic blocks in the DLPA100. For a more detailed description of these blocks, see the DLPA100 data sheet.

DLPA100 features:

- 2.5-V fixed-, 3.3-V fixed-, 5-V fixed-, and 1.0-V to 3.3-V adjustable switching regulators
- Two adjustable linear regulators with enable
- Power supply sequencing control
- Threes fan drivers
- Three-phase BEMF motor driver and controller
- Motor supply switching regulator

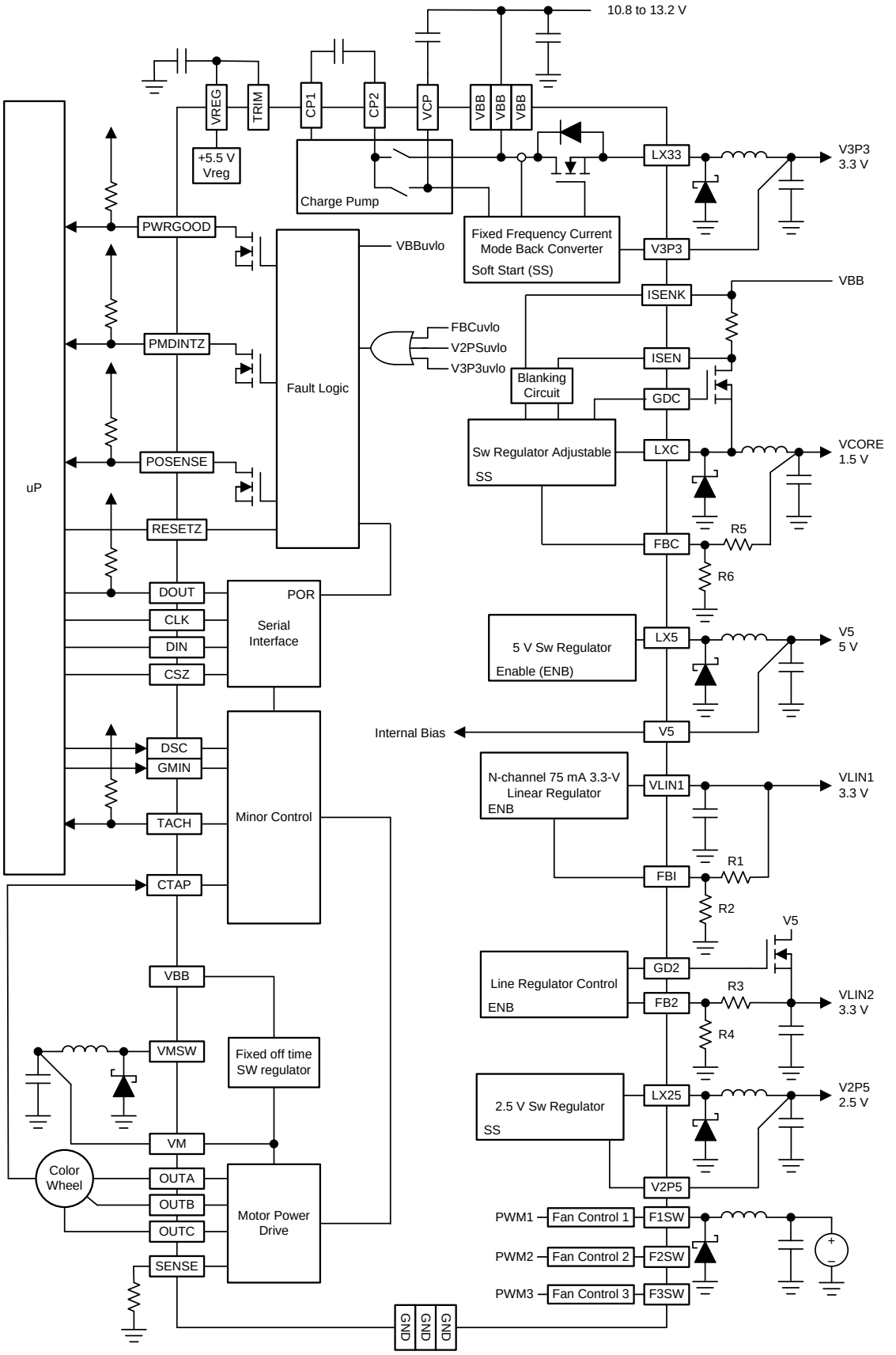


図 4. DLPA100 Block Diagram

2.3.4 TPS65145

The TPS65145 offers a compact and small power supply solution to provide all three voltages required to control the DMD. The TPS65145 provides control of the power-up sequencing of the three voltage outputs to ensure a correct power up of the DLP470NE DMD. Due to the high 1.6-MHz switching frequency of the charge pumps, inexpensive and small capacitors can be used. Additionally, the TPS65145 has a system power good output to indicate when all supply rails are acceptable for the DMD. 図 5 shows a functional block diagram of the internal logic blocks in the TPS65145. For a more detailed description of these blocks, see the TPS65145 data sheet.

TPS65145 features:

- 2.7-V to 5.8-V input voltage range
- 1.6-MHz fixed switching frequency
- Three independent adjustable outputs
- Internal soft start
- System power good

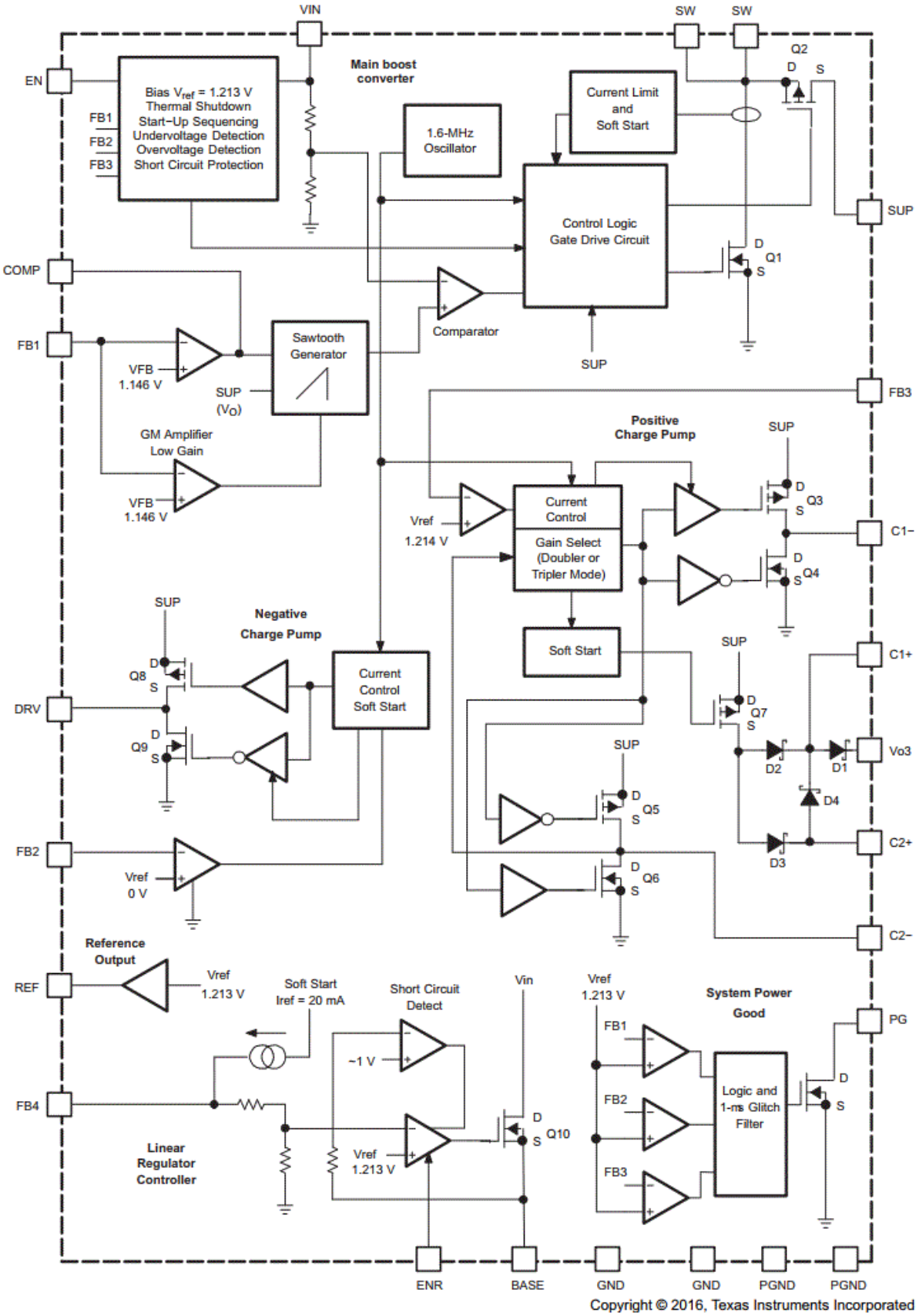


図 5. TPS65145 Block Diagram

3 Getting Started

3.1 Front-End Source Interface

図 6 shows the flow of data in a typical DLP display subsystem from the source all the way to the DMD. The source is fed into either a daughtercard or a front end. The daughtercard or front end then takes the data that is received from the video input and converts the input data into a 24-bit RGB data parallel interface (I/F). This 24-bit RGB data parallel I/F is the main format that the DLPC4422 receives before passing on the correct information to the DMD.

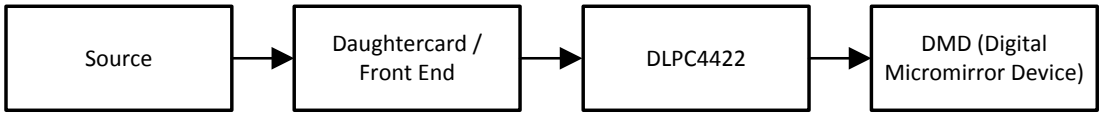


図 6. Typical DLP Display Subsystem Data Flow

Minimizing the delay in the front end and the DLPC4422 device is required to achieve low latency. To minimize the delay, the frame latency is decreased from three frames to one frame by disabling the frame rate conversion function, which has a two-frame delay (see 3.5 for more details). An important thing to note is that the front end can also be the source of video delay in the design. When using a daughtercard, a minimal amount of delay occurs because it acts as a buffer that converts the data from the source to DLPC4422. However, when using a front end, there is extra processing that could add up to a one-frame delay depending on the added processing. Therefore, the selection between using a front end or daughtercard can change the amount of frame delays even with the optimization in the DLPC4422 device.

The DLPC4422 controller accepts low-voltage transistor-transistor logic (LVTTL) input data, which then passes through one or two 30-bit input data ports depending on the input pixel clock and the DLPC4422 controller pixel mode configuration. The DLPC4422 controller supports pixel clocks up to 175 MHz in single pixel mode using one 30-bit port and up to 320 MHz (split into two 160-MHz channels) using two 30-bit ports (60 bits total). The data can be in YUV, YCbCr, or RGB data format and the source can provide 8, 9, or 10 bits of bit depth per color.

See the “Port 1 Input Pixel Interface” table in the DLPC4422 data sheet[2] for the detailed timing requirements for video signals from the front end into the controller.

The front end also sends the I^2C command to the DLPC4422 controller to enable low latency mode. For more information on I^2C commands, see *DLPC4422 Software Programmer's Guide*[3].

3.2 Hardware

As previously mentioned, the user can apply this reference design to a wide variety of projection and display systems that range from HTiB to flight simulators. The electronics that drive these systems vary greatly to suit the application. This section describes the minimum steps required to make the TIDA-01474 reference operational and to send low latency video and imaging data to the DMD. Any deviation from the reference design may require additional steps before the system is up and running.

3.2.1 Power Supply

TI recommends using an AC power adaptor with a 12-V output at 5 A. TI used the following power supply from PHIHONG: model PSAA60M-120.

3.2.2 Jumpers

Within this design, jumpers are defined as a small conductor capable of shorting two pins on the printed-circuit board (PCB) together. GPIO pins on the DLPC4422 detect this circuit change, which is then used to customize the performance of the reference design. The jumper selections required to make the design operational depend on the design choices made during schematic capture and layout. 表 2 lists the jumpers that must be connected on the PCB to power up a lamp-illuminated system. 図 7 shows the jumper locations on the PCB.

表 2. Jumper Description

JUMPER	DESCRIPTION	PIN FUNCTIONS
J4	High-current fan 5 or fan 6	Pins 1,2 connected for high current fan 5 Pins 2,3 connected for Fan 6 (Default)
J6	BT-656 port bus switch select	Uninstalled - BT656 input from front end (default) Installed - BT656 input from video decode test
J8	Digital signal processor (DSP) reset select	Pins 1, 2 connected when using DSP option Pins 2, 3 connected when not using DSP (hold in reset)(default)
J12	Lamp hot or red LED enable	Pins 1, 2 for Solid State Illumination (SSI) system using red LED enable Pins 2, 3 for lamp system using lamp hot
J13	DSP ready or LED 7 PWM	Pins 1, 2 for SSI system using red LED enable Pins 2, 3 for connected for SSI system not using DSP (default)
J14	DSP interrupt or LED 8 PWM	Pins 1, 2 for SSI system using red LED enable
		Pins 2, 3 for connected for SSI system not using DSP(default)
J15	I^2C clock select for video daughtercard	Pins 1, 2 connected SCL1 used Pins 2, 3 connected SCL0 used (default)
J16	I^2C data for video daughtercard	Pins 1, 2 connected SDA1 used Pins 2, 3 connected SDA0 used (default)
J17	Hold in boot loader	Uninstalled - Normal operation (default) Installed - Hold in boot loader
J18	DSP_P1P8V source select	Pins 1, 2 connected DSP_P1P8V from DLPA100 1 (default) Pins 2, 3 connected DSP_P1P8V from DLPA100 2
J19	FE_P1P2V source select	Pins 1, 2 connected FE_P1P2V from DLPA100 1 (default) Pins 2, 3 connected FE_P1P2V from DLPA100 2
J25	Manual reset	Uninstalled - Normal operation (default) Installed - Hold in reset
J26	Comparator sensor or analog-to-digital converter (ADC) integrating sensor	Pins 1, 2 connected ADC integrating sensor (default) Pins 2, 3 connected comparator sensor
J34	Light-to-frequency sensor or ADC integrating sensor	Pins 1, 2 connected ADC integrating sensor (default) Pins 2, 3 connected comparator sensor
J36	Ultra-low-power mode bypass	*Do not install*
J45	Blue LED enable or lamp ballast	Pins 1, 2 connected LED_EN inverted Pins 2, 3 connected LED_EN not inverted (default)
J48	Serial peripheral interface (SPI) driver control interface select	Uninstalled - SPI bus from application-specific integrated circuit (ASIC) Installed - SPI bus from DSP
J50	Half bus – Full bus DMD mode	Uninstalled - Half bus mode (default) Installed - Full bus mode

表 2. Jumper Description (continued)

JUMPER	DESCRIPTION	PIN FUNCTIONS
J51	DMD_P3P3V source select	Pins 1, 2 connected DMD_P3P3V from main DLPA100(default) Pins 2, 3 connected DMD_P3P3V from external switching regulator (for high current DMDs)

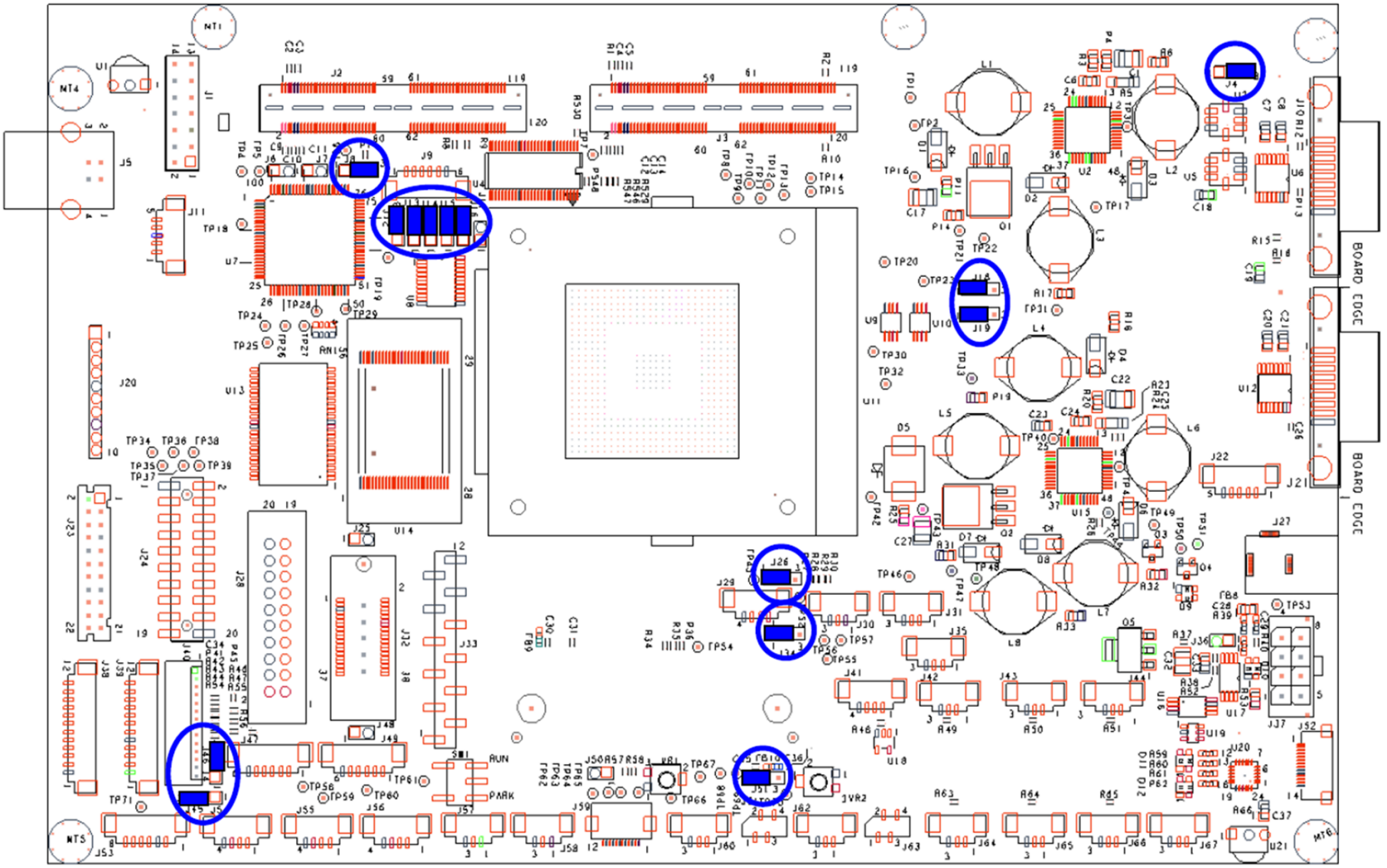


図 7. Jumper Location

3.2.3 Connections

The cable connections required to make this reference operational depend on the design choices made during schematic capture and layout. The following list explains the connections required on the PCB to power up an LED-illuminated system.

- DMD, DMD board, flex cables
  - Position the DLP470NE DMD in place on the DMD interposer.
  - Secure the DMD board and DMD against system optics (or leave them on a bench for visual evaluation of DMD mirrors).
  - Attach flex cables from the DMD board to the formatter board—this method varies depending on the choice of flex cable. Follow the instructions as specified by the manufacturer.
- PWM controlled fans
- Keypad

3.2.4 Initialize System

To initialize the system:

1. Move switch SW1 to *Park*
2. Apply power to the illumination power supply
3. Apply +12-V DC power to the TIDA-01474 electronics
4. Move switch SW1 to *Run*
5. Check to confirm heartbeat blinking from diode D11

3.3 Bootloader

This reference design requires software to run the DLPC4422 and to control the DLP470NE DMD. To be able to install the DLPC4422 into the electronics after assembly, the DLPC4422 flash memory must have an ARM bootloader programmed into it. To ensure functionality of the electronics during first start up, TI recommends loading the ARM bootloader into the DLPC4422 flash before the assembly of the electronics. Many third-party flash retailers and PCB assembly shops offer flash loading services with the bootloader binary provided with this reference design.

When the flash has been loaded with the bootloader and assembled onto the PCB, the software for the DLPC4422 can be loaded onto the board from a PC through USB using the DLP Composer™ Lite GUI.

3.4 Software

The DLPC4422 controller includes a Windows® based graphical user interface (GUI) application to control the module through I^2C commands. This section provides instructions on how to use features provided by the GUI application to communicate with the DLPC4422 controller.

3.4.1 Set Up DLP Composer™ Lite GUI

3.4.1.1 System Requirements

The following list shows the minimum recommended system requirements for the DLPC4422 Composer Lite™ GUI application software:

- PC with 1.4-GHz Pentium® IV CPU or higher
- Microsoft®Windows XP ® SP3 or higher

- 512MB of RAM
- 10MB of free hard-disk space
- USB port

The user must also have an I^2C convertor box, for which TI recommends the following resources:

- USB-I2CIO USB interface hardware at: www.devasys.com
- USB-to-I2C professional drivers at: www.i2ctools.com/manuals-and-downloads/

3.4.1.2 DLPC4422 Composer Lite GUI Software Installation

Download the installation setup for DLPC4422 Composer Lite GUI PC software from www.ti.com/product/DLPC4422. Execute the Composer Lite GUI v1.0 Setup.exe file and follow the instructions for software installation.

3.4.1.3 Communication Interface Driver Installation

When using the DLPC4422 Composer Lite GUI, the user must have an established communication link between the DLPC4422 controller and the computer running this software. This communication link allows the user to read and write to the controller from the computer. The DLPC4422 Composer Lite GUI supports I^2C. USB communication from a PC does not require any special drivers. Use a USB-to-I2C adapter and install the drivers available for download from the following links to use I^2C communication:

- DeVaSys USB-to-I2C driver at www.devasys.com
- USB-to-I2C professional drivers at DLPC4422 Composer Lite GUI: www.ti.com/tool/dlpcsw

3.4.1.4 DLP470NE Software Files

Download the DLP470NE software files. This .zip file contains the flash image and files required to communicate with the DLPC4422 controller.

- DLPC4422_p47_TRP_1080p.img – Flash image to configure DLPC4422 controller per illumination
- DLPC4422xf.projector – Projector control file used to communicate with the DLPC4422 through the DLP Composer Lite GUI
- FlashDeviceParameters.txt – Required by DLP Composer Lite GUI tool to define the flash parameters

3.4.1.5 User Interface Overview

When the installation successfully completes, open the DLP Composer Lite GUI by navigating to *Start → All Programs*, or open the shortcut provided on the desktop. When the application starts, the GUI screen in 図 8 pops up. The GUI window contains the sections as highlighted:

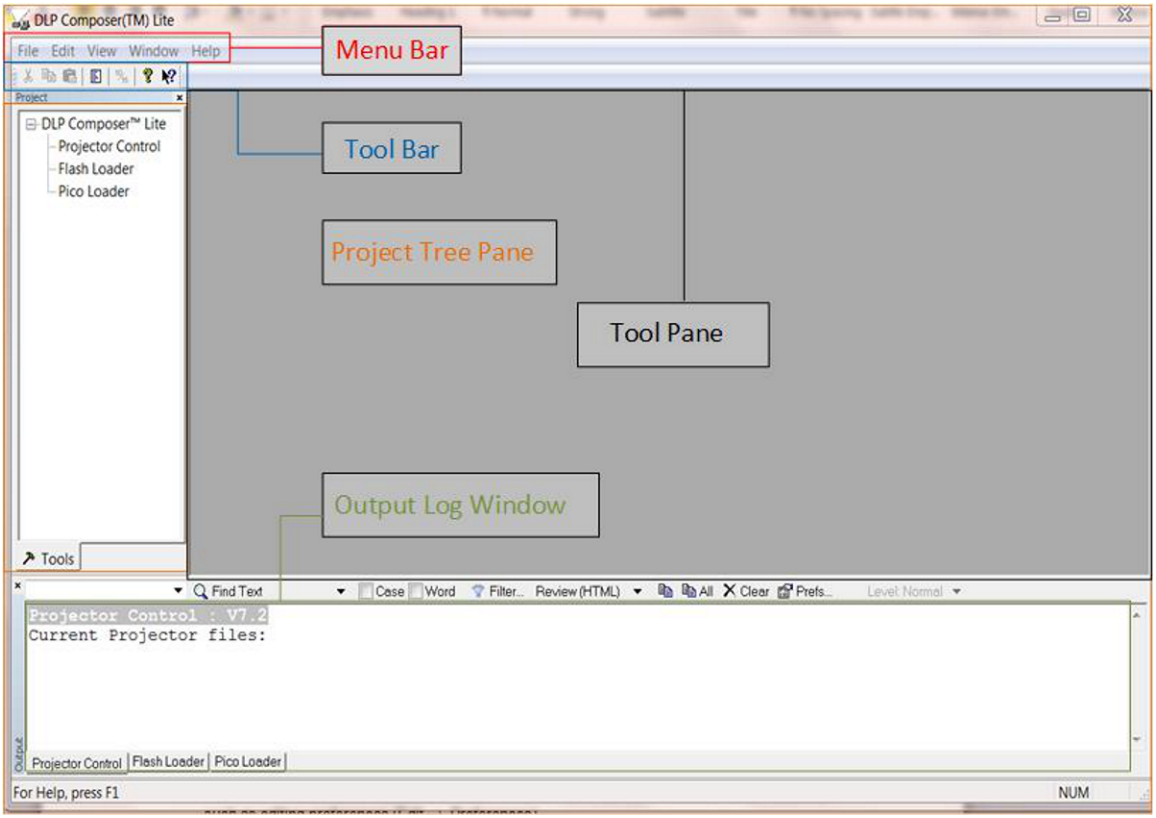


図 8. DLP Composer™ Lite GUI

- Project tree pane: The project tree pane lists the projector control tool and flash loader tool, which are used to communicate with the DLPC4422 controller. Select a tool to open the associated tool pane and any tabs or toolbars.
- Tool pane: The tool pane shows the active panel for the tool selected in the project tree.
- Output log window: The output log window shows information associated with the user's project and is mostly used for debugging. The output log window has its own set of tool tabs (projector control and so forth) located at the bottom of the window that allows the user to toggle through the various tool output logs without changing the active tool in the tool pane.
- Menu bar: The menu bar contains several menus the user can click to access other features, such as editing preferences (*Edit* → *Preferences*).
- Toolbar: This bar contains common support functions for the project selected from the project tree pane.

3.4.1.6 Using Edit Menu

In the *Menu* bar, select *Preferences* from the *Edit* menu to specify the DLP Composer Lite GUI options:

- Output window and logging options
- Communication options
- Flash loader options

3.4.1.7 I²C Interface

This Composer Lite interface can be used to make run-time changes to the TIDA-01474 reference design as well as to program a flash image to the reference design.

1. In the menu bar of DLP Composer GUI, navigate to *Edit* → *Preferences* → *Communication* → *Projector Interface* → *I2C Interfaces* as 図 9 shows and select DeVaSys (or USB from the *USB Interfaces* sub menu).
   - DeVaSys www.devasys.com
   - I2C Tools www.i2ctools.com
   - Cypress
2. At the end of the dialog box, select 100 kHz as the I²C speed (see 図 9).
3. Click the *OK* button.

注: Ignore all of the other listed communication interfaces for this device.

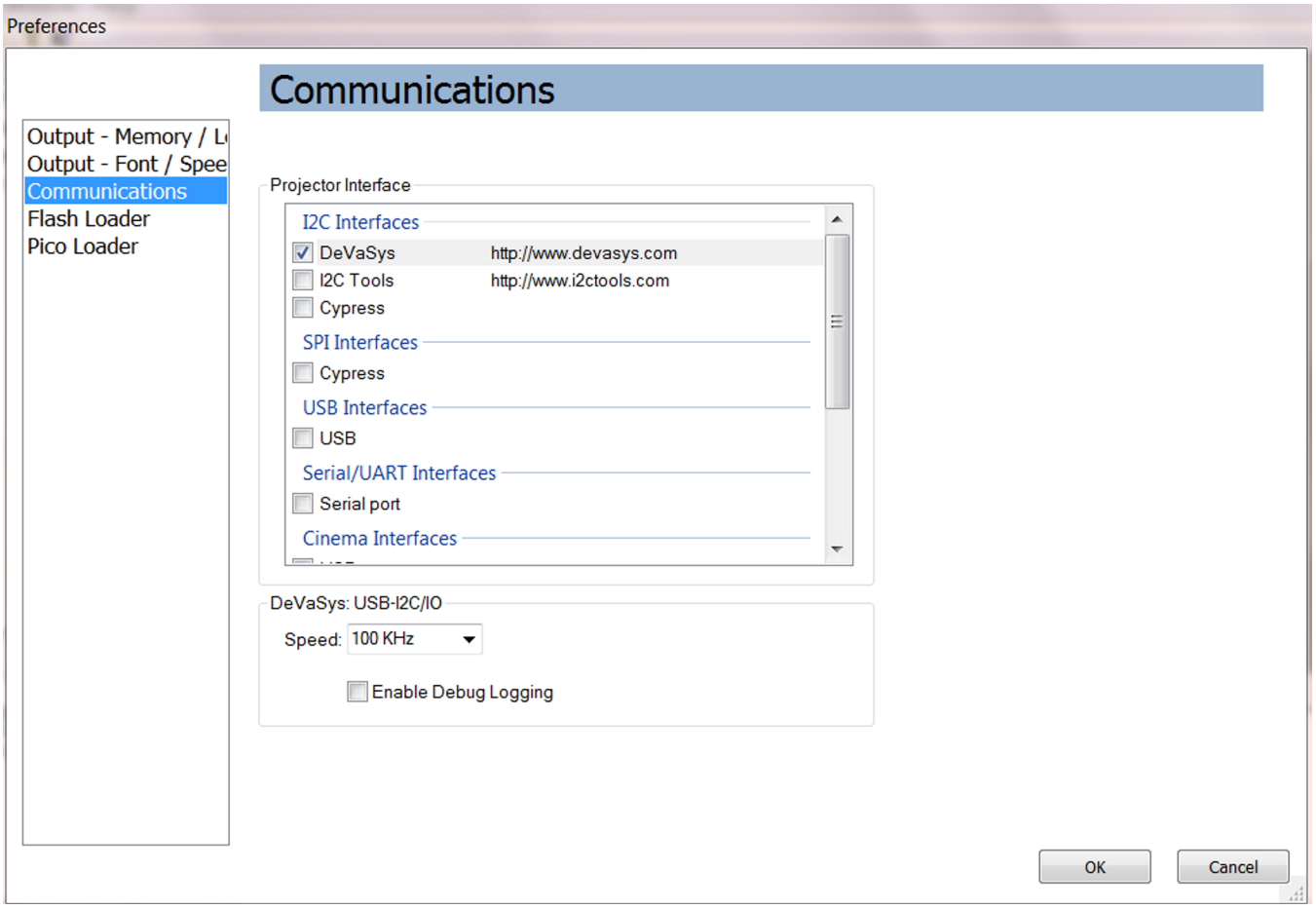


図 9. I²C Communication Options

3.4.1.8 Flash Loader Options

1. In the menu bar of the DLP Composer GUI, navigate to *Edit* → *Preferences* → *Flash Loader* as 図 10 shows.
2. Set the *Auto Restart Timer* to 30 seconds.
3. Select 20000 milliseconds as the *Programming Mode Delay*.
4. At the end of the dialog box, select 100 kHz as the I2C Device Speed (Up to 400 kHz supported).
5. Click the *OK* button.

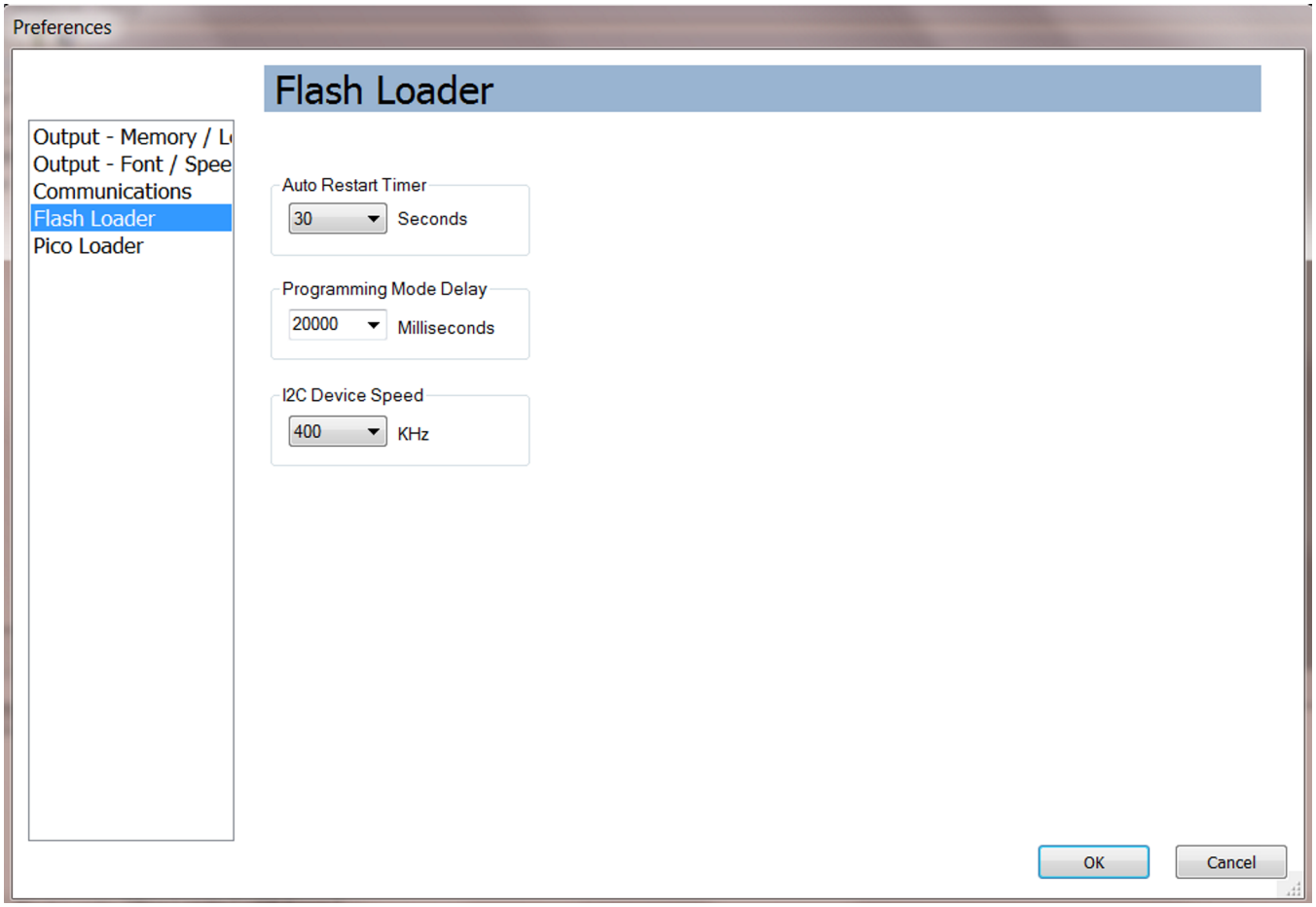


図 10. Flash Loader Options

3.4.1.9 Using Projector Control

Using Projector Control

The Projector Control tool is used to control a DLPC4422 controller by issuing I²C commands. Use this tool to construct batch files consisting of multiple I²C commands (and other commands) to automate simple tasks when developing and testing a new projector using the *Batch Files* page. Several other pages are available to issue commands and view data.

Using Flash Loader

Use this tool to send a flash image file to a DLPC4422 controller using I²C. Obtain the flash image file for the DLPC4422 controller (see 6) and copy it onto the PC. After obtaining the flash image, select *Flash Loader* from the *Project* tree pane on the left side of the interface. The *Flash Loader* GUI pops up in the tool pane (see 図 11).

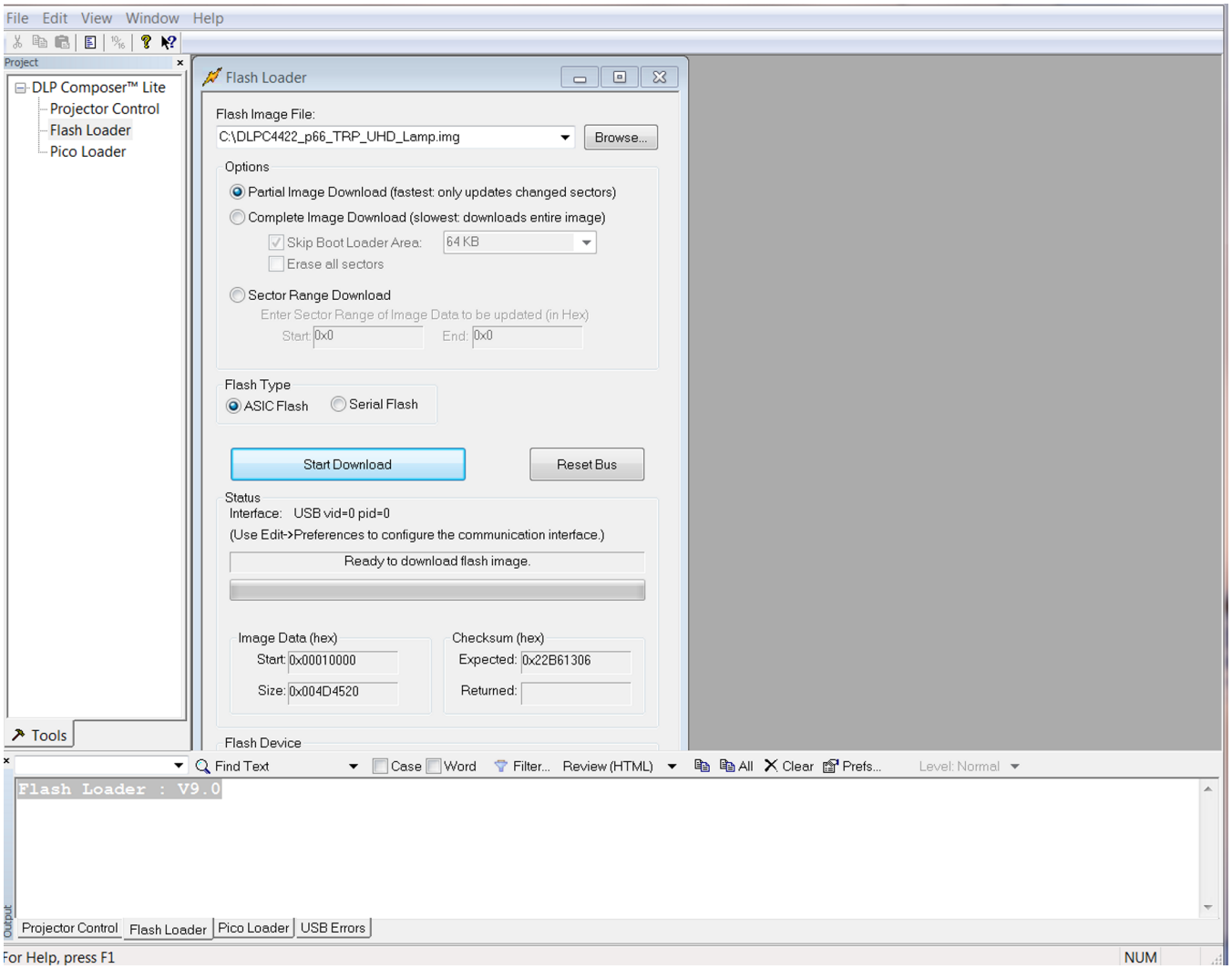


図 11. Flash Loader

To download the flash image, follow these steps:

1. Click the *Browse* button to select the filename.
2. Set the *Sector Range Download* parameters (optional).
3. Power the device by connecting the USB cable to the PC and ensure connectivity.
4. Click the *Start Download* button to begin the transfer.
5. Do not interrupt the power until after the download completes.

注: The *Partial Image Download* option can be used for consecutive downloads. This option compares flash images and only overwrites sectors that are different. *Partial Image Download* can only be used after performing a *Complete Image Download* to the unit at least one time. TI recommends skipping the bootloader option unless the user wants to purposely overwrite the bootloader.

3.5 Low Latency Mode

The default video data delay of the DLPC4422 controller is two to three frames. The *Frame Rate Conversion* feature of the DLPC4422 must be disabled to enable a single frame delay between the input data and the projected image. Note that disabling this feature specifies the DLPC4422 device to support four specific input frame rates: 50 Hz, 60 Hz, 100 Hz, and 120 Hz. The image created by the reference design has the same frame rate as the input video data.

To put the system into low latency mode, the front end processor must send an I^{2}C command to the DLP4422 controller. For more information about I^{2}C commands, see *DLPC4422 Software Programmer's Guide* (DLPU060).

To enable the low latency mode for debugging purposes, DLP Composer Lite can be used to send the I^{2}C command to the DLPC4422. From the *Project* tree pane, navigate to *Projector Control → Display*. In the tool pane for the *Display*, toggle the checkbox for *FRC Bypass Mode* to enable or disable low latency mode (see 図 12).

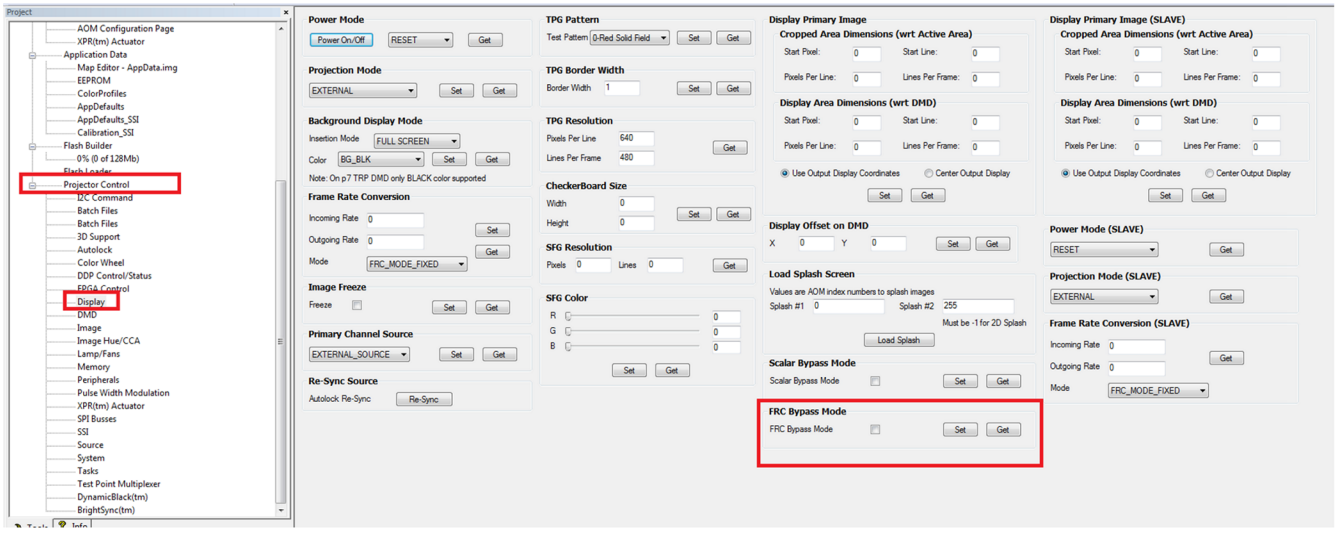


図 12. Enabling Low Latency Mode in DLP Composer™ Lite GUI

3.6 Optical Engine and Light Source

This reference design is a customizable 1080p, high-speed, low-latency display solution. The design can be paired with diverse optical engine architectures and illumination sources depending on the end application.

Display systems based on DLP technology require an illumination source to create a projected image. DLP technology can be used with a wide array of light sources, including lamps, LEDs, lasers, and laser phosphor. Many traditional projectors still use lamps as an illumination source; however, a significant market has developed for laser-phosphor illumination systems. Laser-based illumination typically lasts many times longer than lamp illumination. Laser-based system benefits can include a wide color gamut and instant ON or OFF capabilities. The illumination choice depends on the user's end application and system requirements. TI encourages that developers work with third-party optical engine manufacturers for optical system expertise, if required.

TI collaborates with third-party optical module manufacturers (OMMs) that provide optical engines and illumination sources that work in conjunction with DLP display subsystems to make the evaluation and design process simpler.

4 Testing and Results

4.1 EMI Compliance

The reference design hardware has not been optimized or tested for low electromagnetic interference (EMI) performance. Users of the information found in this reference design are responsible for ensuring that all products used meet all the applicable EMI regulations.

4.2 Start-Up and Shutdown Power Sequencing Measurements

The start-up and shutdown power sequencing of the four power supplies to the DLP470NE are critical to ensure DMD functionality. The electrodes held at three control voltages electrostatically control the micromirrors in the DMD. The VRESET (–14 V), VOFFSET (10 V), and VBIAS (18 V) supplies to the DMD provide these potentials. The fourth power supply is the CMOS logic supply, DMD_P1P8V (1.8 V). DMD_P1P8V is created directly from DMD_P3P3V (3.3 V) by a linear regulator on the DMD board; therefore, TI uses the start-up of DMD_P3P3V to trigger the measurement of the start-up and shutdown power sequencing.

The DLP470NE data sheet describes the power-up and power-down timing requirements in detail. The key signals to measure are power supplies to the DMD: DMD_P3P3V, VBIAS, VOFFSET, and VRESET. For more details on the timing requirements, see the DLP470NE device data sheet[1].

The location of test points for the four DMD voltages depends on design choices made during schematic capture and layout. 図 13 shows the locations of the test points on the TI EVM.

See the start-up and shutdown power sequence timing requirements in the DLP470NE data sheet, which must be consulted to ensure full compliance. 図 14 and 表 3 show a snapshot of these requirements.

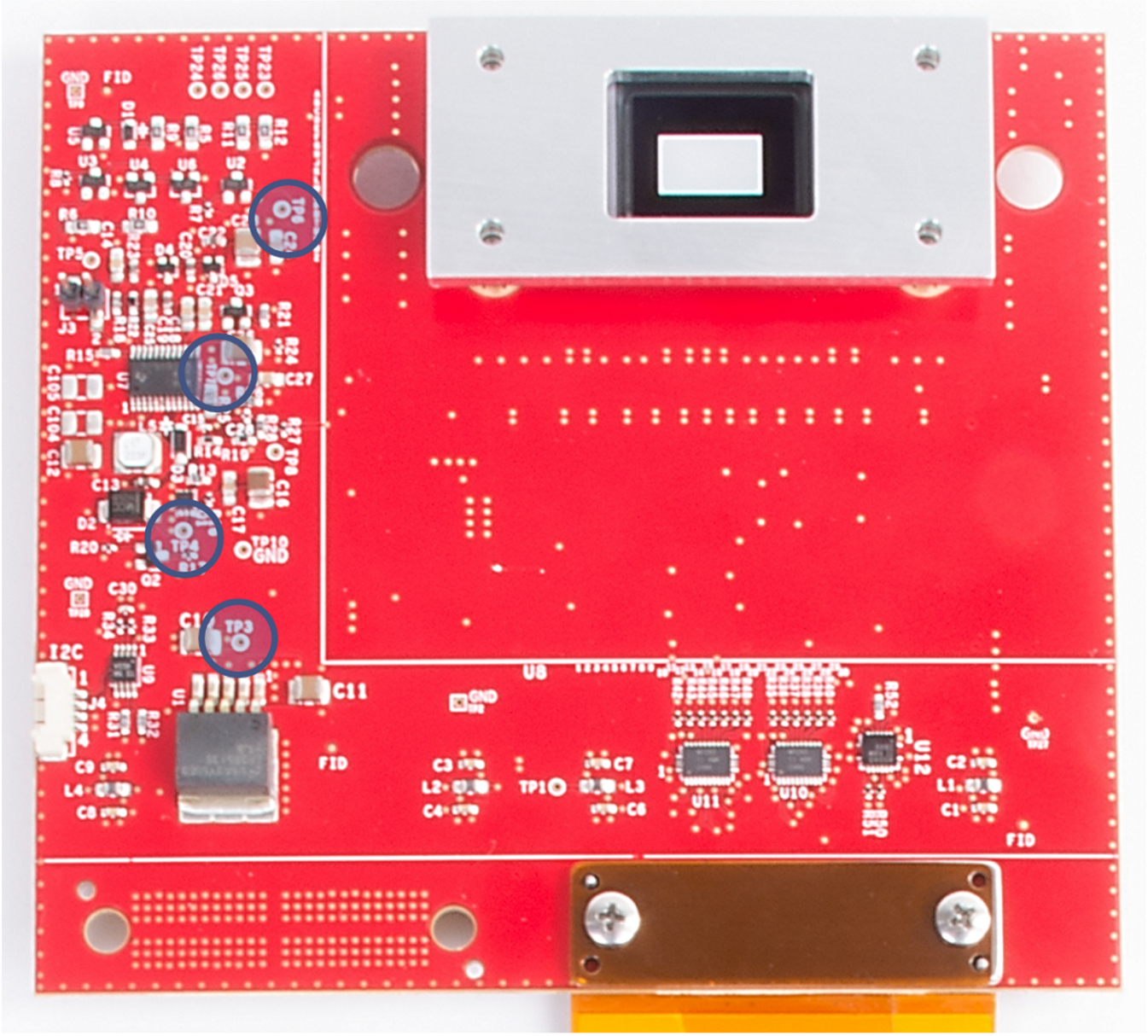


図 13. DMD Board Voltage Test Points

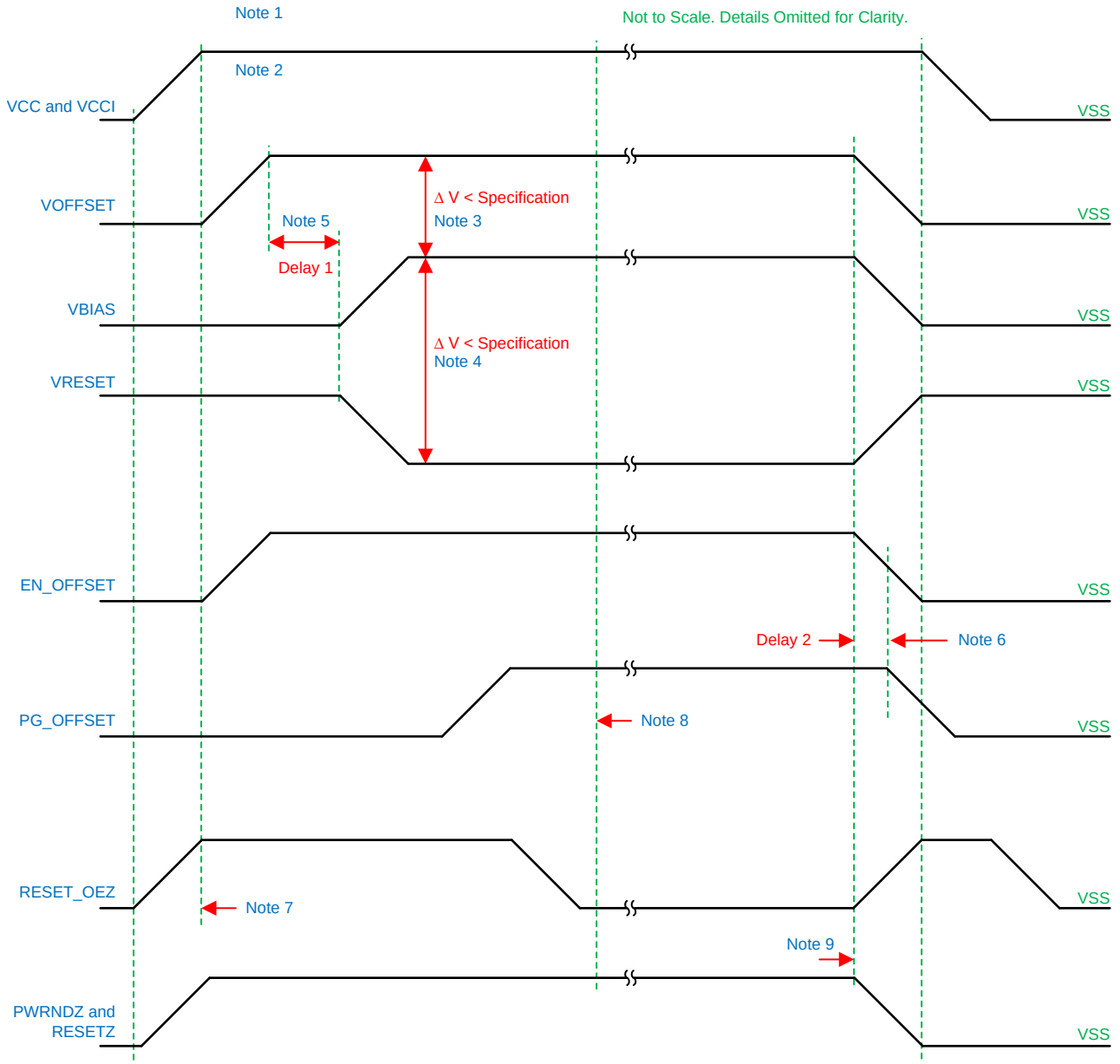


図 14. DMD Power Supply Timing Diagram

1. See the data sheet recommended operating conditions and pin functions.
2. To prevent excess current, the supply voltage delta |VCCI – VCC| must be less than specified limit in the data sheet.
3. To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified limit in the data sheet.
4. To prevent excess current, the supply voltage delta |VBIAS – VRESET| must be less than specified limit in the data sheet.
5. The VBIAS should power up after VOFFSET has powered up, per the Delay 1 specification in 図 14.
6. The PG_OFFSET should turn off after EN_OFFSET has turned off, per the Delay 2 specification in 図 14.
7. The DLP controller software enables the DMD power supplies to turn on after RESET_OEZ is at logic high.
8. The DLP controller software initiates the global VBIAS command.

9. After the DMD micromirror park sequence is complete, the DLP controller software initiates a hardware power-down that activates PWRDNZ and disables VBIAS, VRESET, and VOFFSET.

表 3. DMD Power Supply Requirements

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
Delay 1	Delay from VOFFSET settled at recommended operating voltage to VBIAS and VRESET power-up	1	2	—	ms
Delay 2	PG_OFFSET hold time after EN_OFFSET goes low	100	—	—	ms

4.2.1 DMD Power Supply Power-Up Procedure

- During power up, VCC and VCCI must always start and settle before VBIAS, VRESET, and VOFFSET plus Delay 1 as 図 14 shows.
- During power up, no requirement exists for the relative timing of VRESET with respect to VBIAS.
- Power supply slew rates during power up are flexible, provided that the transient voltage levels follow the requirements specified in the data sheet.
- During power up, LVCMOS input pins must not be driven high until after VCC and VCCI have settled at operating voltages listed in the data sheet.
- 図 15 shows the power supply power up.

4.2.2 DMD Power Supply Power-Down Procedure

- During power down, VCC and VCCI must be supplied until after VBIAS, VRESET, and VOFFSET are discharged to within the specified limit of ground.
- During power down, it is a strict requirement that the voltage delta (Δ) between VBIAS and VOFFSET must be within the specified limit that the data sheet shows.
- During power down, there is no requirement for the relative timing of VRESET with respect to VBIAS.
- Power supply slew rates during power down are flexible, provided that the transient voltage levels follow the requirements that the data sheet specifies.
- During power down, the LVCMOS input pins must be less than what the data sheet specifies.
- 図 16 shows the power supply power down.

4.2.3 Test Results

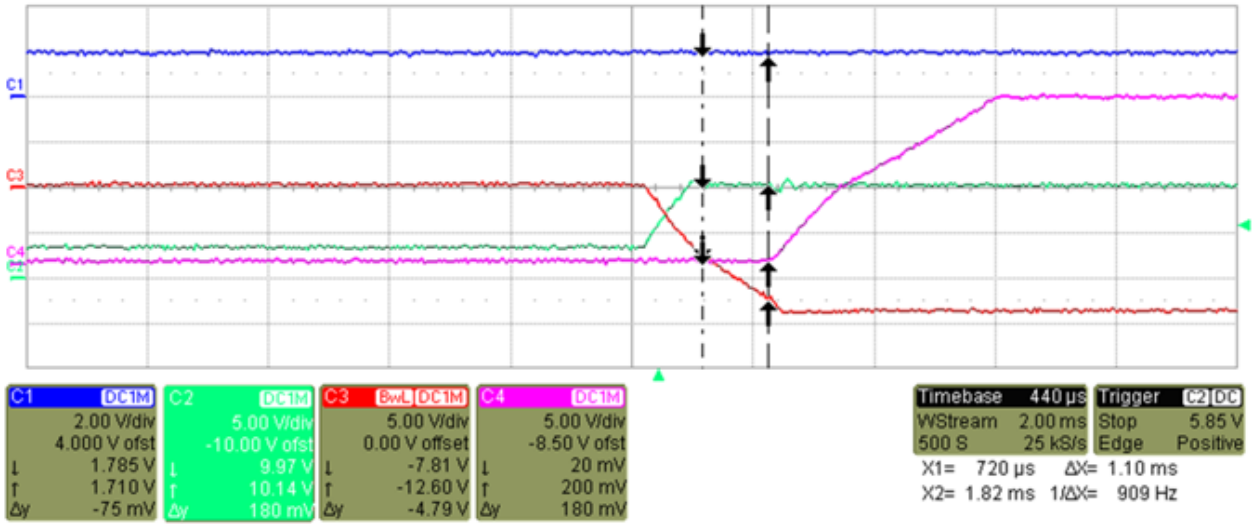


図 15. DMD Start-Up Power Sequencing

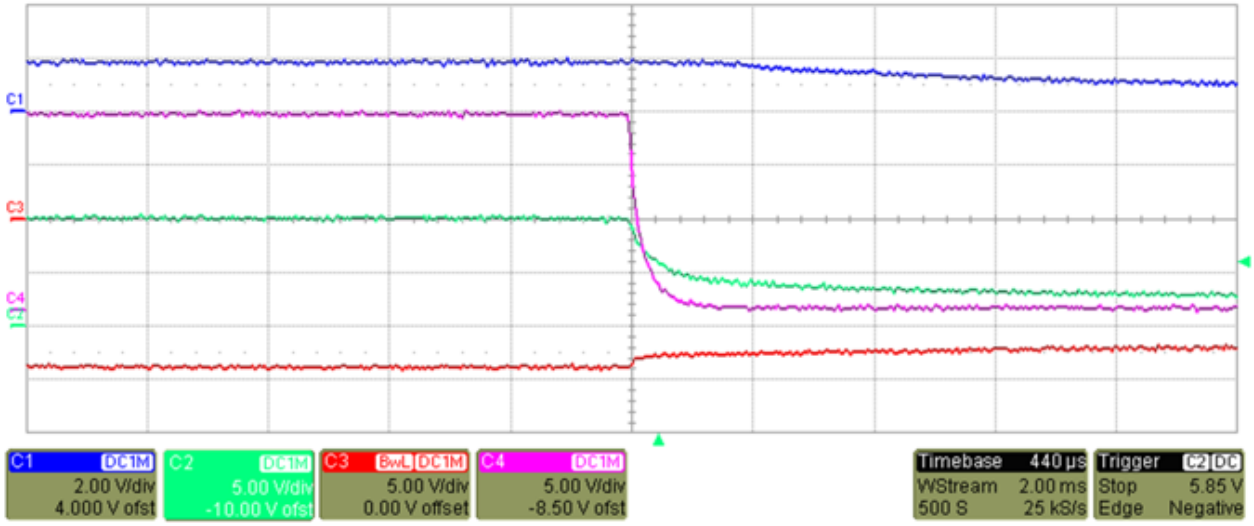


図 16. DMD Shutdown Power Sequencing

4.3 Frame Rate Measurements

To test the output frame rate of the projector, a source with a known output of 120 Hz is connected to the TIDA-01474 test set. The source was set to a solid red field and an optical sensor was placed in the projection path. The test probes were connected to the vertical sync (channel 1), data enable (channel 2), and the most significant bit for the red channel data input on the TIDA-01474 main board PCB (channel 3), and the optical sensor (channel 4). All four channels were active on the oscilloscope.

The oscilloscope capture shows that when the vertical sync first pulses (the dashed line with arrows on the left side), a time delay occurs before data enable goes high. This time delay is called the back porch. As soon as the back porch ends, the data enable goes high and the data bits begin to transmit on the red most significant bit. After the data for the frame has been transmitted, the data enable goes low again and another time delay occurs, which is called the front porch, before the vertical sync (the second white line) of the next frame. The oscilloscope cursors were used to measure the duration of a frame (from vertical sync to vertical sync) at 8.33 ms, corresponding to a 120-Hz video signal as 図 17 shows.

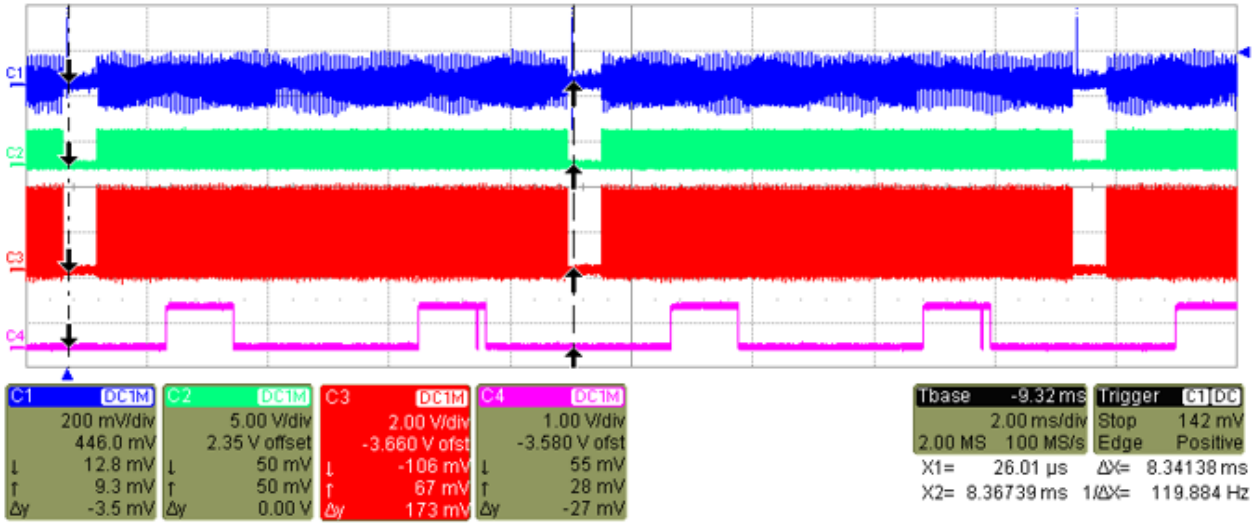


図 17. 120-Hz Frame Rate Measurement

4.4 Frame Delay Measurements

To test the frame delay in the TIDA-01474 subsystem from input data to projected image, a personal computer was connected to the TIDA-01474 test set as a video source. A slideshow presentation with a black slide and a red slide was queued up on the computer with the black slide set to display first. An optical sensor is placed in the projection path and an oscilloscope was set up with the optical sensor and one test probe functioning as the inputs. The test probe was connected to the input red channel most significant bit on the DLPC4422 ASIC. The oscilloscope was set to single capture mode and set to trigger on the rising edge of the red channel most significant bit input.

After preparing the test setup, the slideshow on the computer was changed from the black slide to the red slide manually. This slide transition caused the oscilloscope to trigger and capture the two input signals. In 図 18 and 図 19, the DLPC4422 was set to normal mode, which runs with a two- to three-frame delay. The oscilloscope capture shows two distinct frames of red channel data before any active data is shown on the optical sensor in the projection path.

The DLPC4422 was then set to low latency mode and the test was run again. 図 20 and 図 21 show only one frame of delay between the first input data to the DLPC4422 red channel most significant bit and the projection of the first data on the optical sensor. This test can be verified by measuring any input video data as long as the source displays the color being measured on the video input pin of the DLPC4422 device. In other words, a source displaying only green video data does not input any data on the blue channel input to the DLPC4422 ASIC, so none of the blue channel inputs can be used to trigger the oscilloscope.

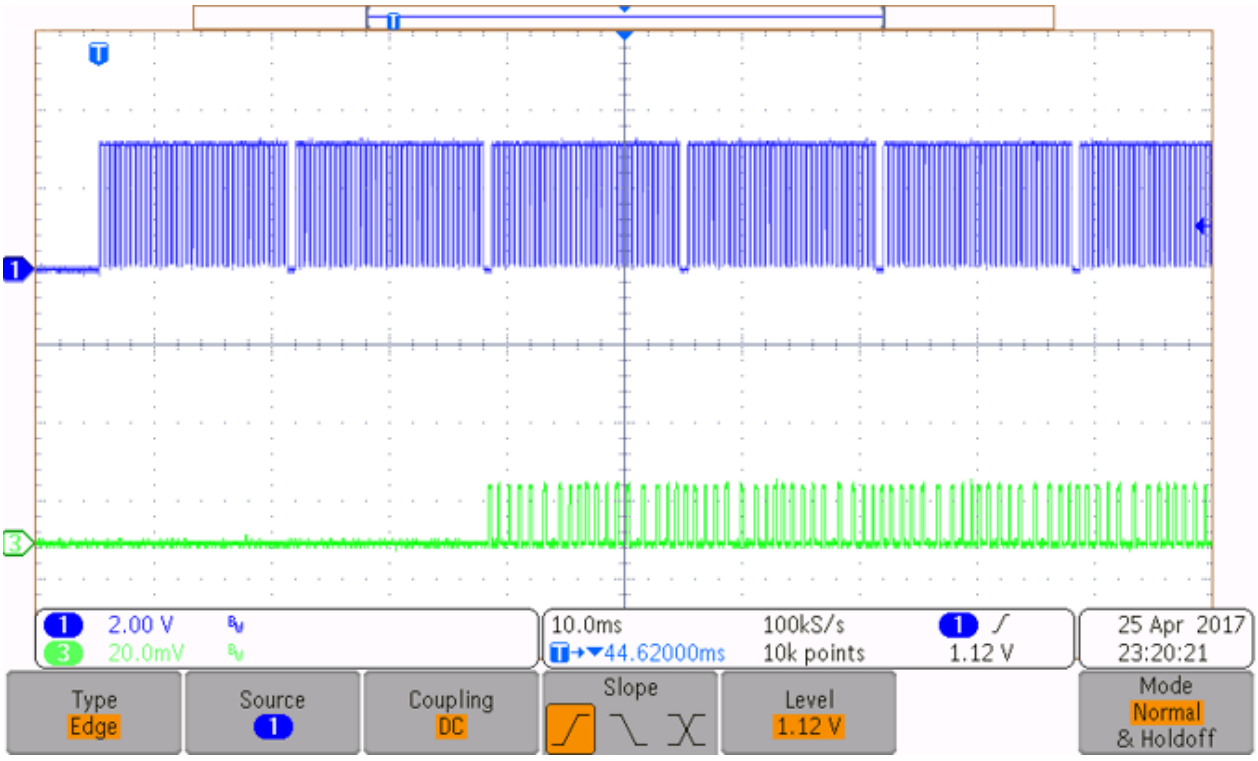


図 18. Two Frames of Delay at 60 Hz

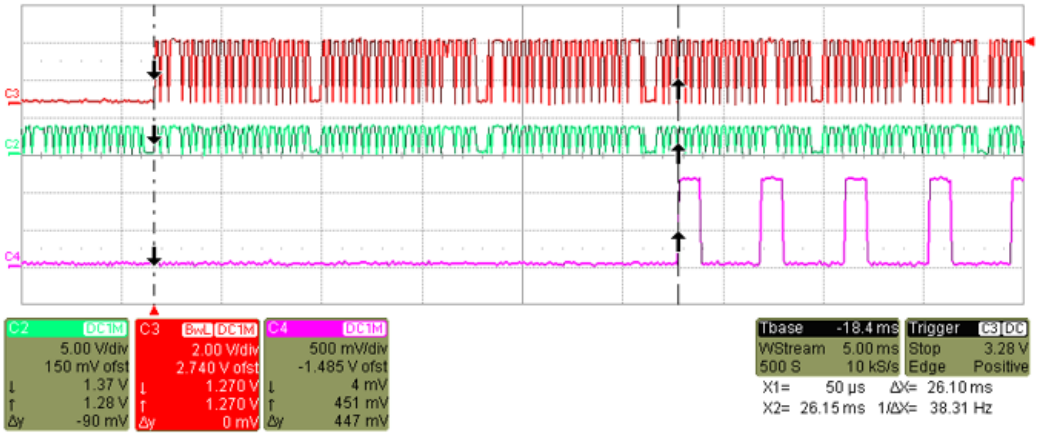


図 19. Three Frames of Delay at 120 Hz

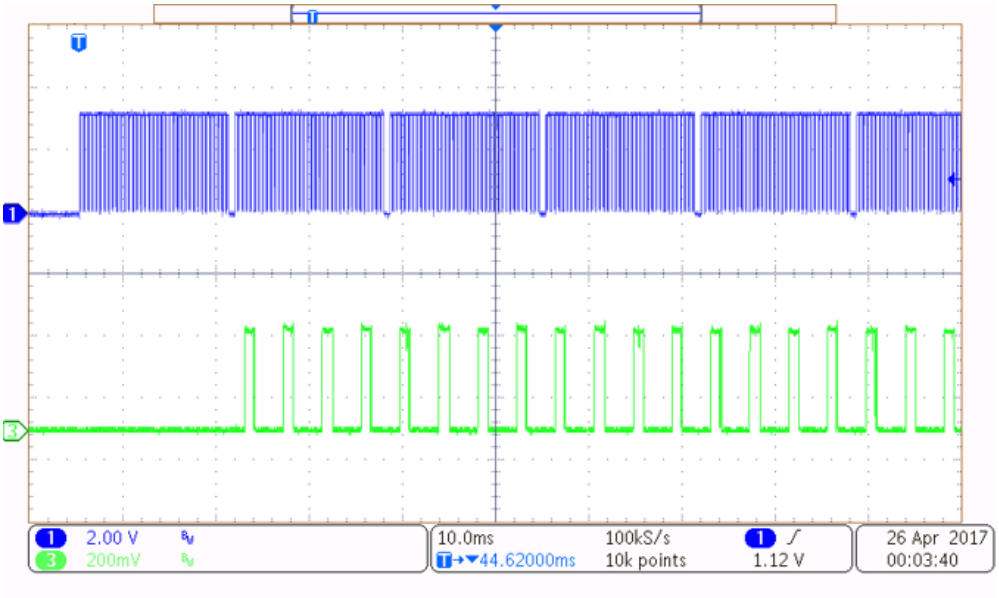


図 20. One Frame

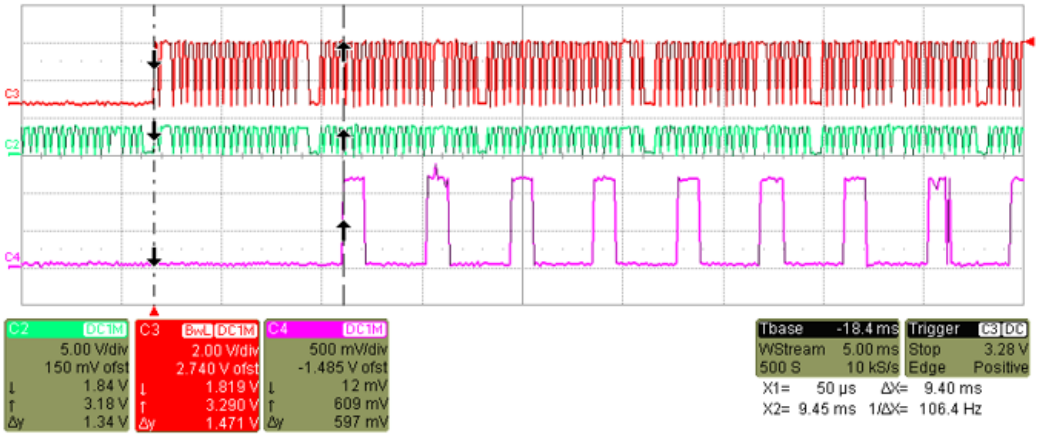


図 21. One Frame of Delay at 120 Hz

5 Design Files

5.1 Schematics

To download the schematics for each board, see the design files at TIDA-01474.

5.2 Bill of Materials

To download the bill of materials (BOM) for each board, see the design files at TIDA-01474.

5.3 PCB Layout Recommendations

5.3.1 Layout Recommendations

TI strongly recommends the PCB have solid ground planes and power planes with no splits if possible. If splits are unavoidable, no signals should be routed across the plane layer splits to avoid EMI compliance problems. Designers should avoid running signal traces on power and ground planes. Trace spacing and layer separation rules should be followed for all high-speed signals, especially the video data entering and leaving the DLPC4422 controller. See the layout guidelines sections of the DLPC4422, DLP470NE, and DLPA100 data sheets for specific layout requirements for these parts.

High-speed interfaces include:

- 400-MHz (DDR) LVDS interface from DLPC4422 ASIC to DLP470NE DMD
- Up to 170-MHz LVTTL interface from the front-end processor to the DLPC4422 ASIC and flash memory
- 143-MHz Arm trace port output (8-bit data bus shared with DLPC4422 test points)
- USB interface

The PCB requires a controlled impedance design for signal layers. The target impedance for the PCB should be 50 Ω with the LVDS traces being a 100-Ω differential.

The reference design layout files provided along with this reference design are only intended as evaluation modules. The reference design hardware was not optimized or tested for low EMI performance. Users of the information found in this reference design are responsible for ensuring that their products meet all applicable EMI regulations.

For more information, see *PCB Design Requirements for DLP® Standard TRP Digital Micromirror Devices*[5].

5.3.2 Layout Prints

To download the Layout Prints for each board, see the design files at TIDA-01474.

5.4 Allegro Cadence Project

To download the Allegro Cadence project files for each board, see the design files at TIDA-01474.

5.5 Gerber and CAD files

To download the Gerber and CAD files for each board, see the design files at TIDA-01474.

5.6 Assembly Drawings

To download the Assembly Drawings for each board, see the design files at TIDA-01474.

6 Software Files

To download the software files for this reference design, please see the link at TIDA-01474.

7 Related Documentation

1. Texas Instruments, *DLP470NE 0.47 1080P DMD* , DLP470NE Data Sheet (DLPS091)
2. Texas Instruments, *DLPC4422 DLP® Display Controller*, DLPC4422 Data Sheet (DLPS074)
3. Texas Instruments, *DLPC4422 Software Programmer's Guide*, DLPC4422 User's Guide (DLPU060)
4. Texas Instruments, *TI DLP® System Design: Brightness Requirements and Tradeoffs*, Application Report (DLPA068)
5. Texas Instruments, *PCB Design Requirements for DLP® Standard TRP Digital Micromirror Devices*, Application Report (DLPA080)
6. Texas Instruments, *TI DLP® technology for laser TV displays*, White Paper (DLPC105)
7. Texas Instruments, *Getting Started with TI DLP® Display Technology*, Application Report (DLPA059)

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