

# TI Designs: TIDA-01055

## 高性能DAQシステム用のADC基準電圧バッファ最適化のリファレンス・デザイン



### 概要

この高性能DAQシステム用リファレンス・デザインは、TI OPA837高速オペアンプによりADC基準バッファを最適化して、SNR性能を向上し、消費電力を削減します。このデバイスは複合バッファ構成で使用され、従来のオペアンプよりも22%の電力の改善を実現します。バッファを内蔵した基準電圧ソースには多くの場合に、チャンネル数の多いシステムで最適な性能を得るために必要な駆動力が不足しています。このリファレンス・デザインは、複数のADCを駆動し、18ビット、2MSPSのSAR ADCを使用して15.77ビットのシステムENOBを実現できます。

### リソース

- TIDA-01055
- LM53635-Q1
- LM5574, LM46001, TPS7A3001
- TPS7A47, LM7705
- SN74AHC1G04, SN74AUP1G80
- LMK61E2, LMK00804B
- OPA827, OPA625, THS4551, OPA837, OPA378
- REF6041, REF5040

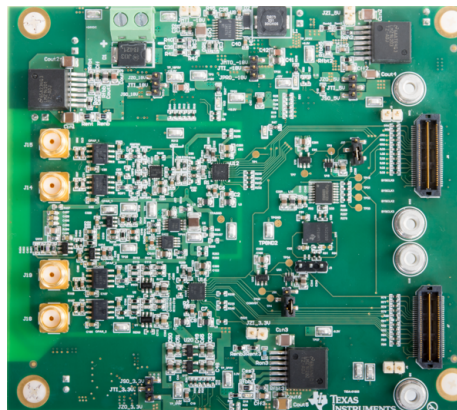
- デザイン・フォルダ
- プロダクト・フォルダ
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### 特長

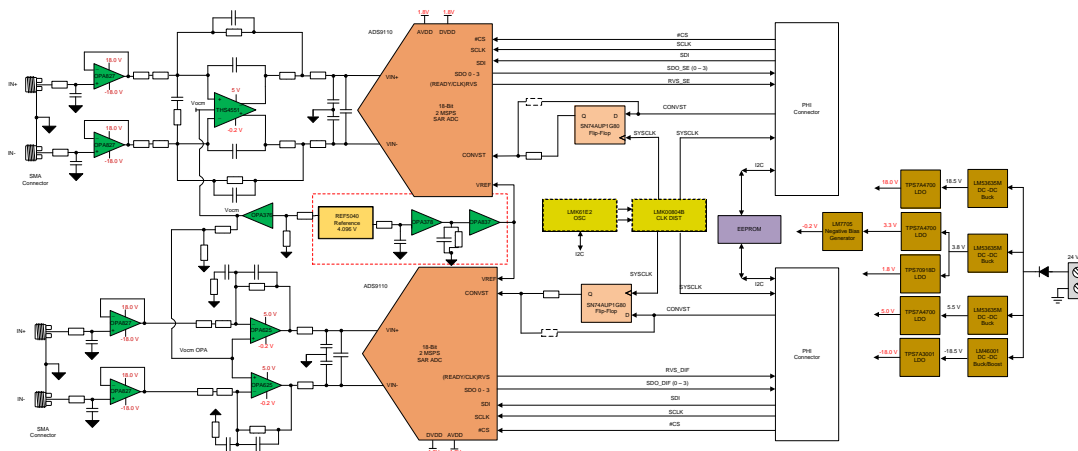
- 2段のバッファ設計により、基準電圧から発生するノイズを低減
- 2MSPSのSAR ADCを駆動できるスルー・レート能力を持つ、新しい低消費電力リファレンス・ドライバを実装

### アプリケーション

- データ収集(DAQ)
- 半導体試験用機器
- LCD試験用機器
- ラボ計測機器
- バッテリー試験装置



E2E™ エキスパートに質問



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## 1 System Description

Multi-input systems requiring the simultaneous or parallel sampling of many data channels present many design challenges to engineers developing data acquisition (DAQ) modules and automatic testers for applications such as semiconductor tests, memory tests, LCD tests, and battery tests. In these systems, sometimes hundreds or even thousands of data channels are required and thus maximizing SNR performance while minimizing power, component count, and cost are all key design criteria. One of the critical parts of these systems is the reference voltage circuit for the analog-to-digital converter (ADC). The reference pin of the ADC needs to be adequately driven to a precise voltage as to not add more noise to the system. Advanced buffering circuits are created to do this, but more components consume more power.

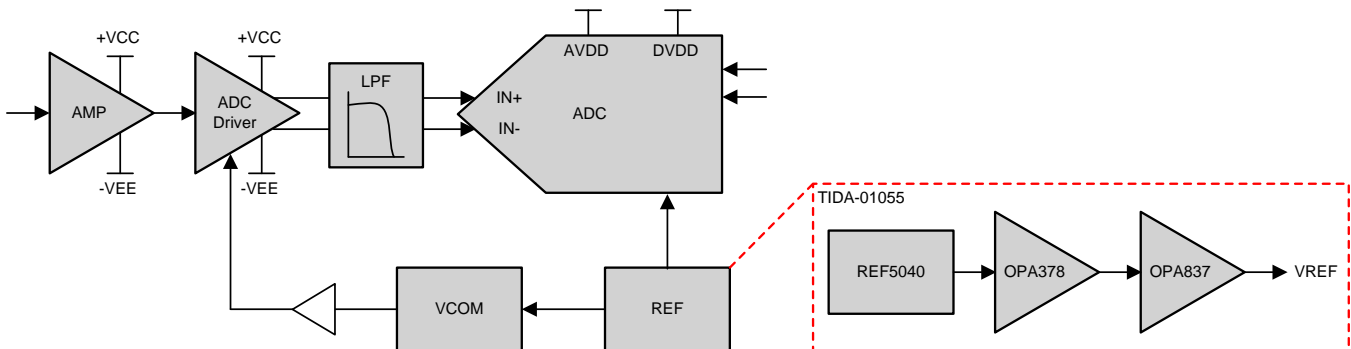


図 1. Generic Analog Front End

### 1.1 Key System Specifications

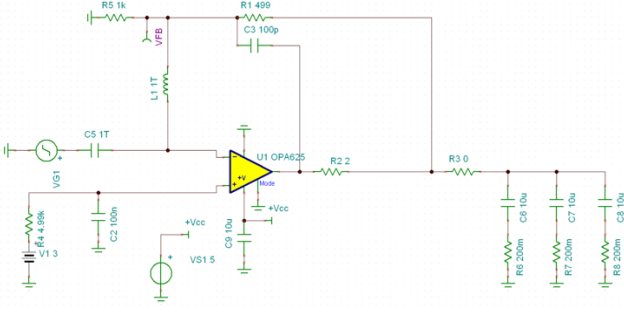
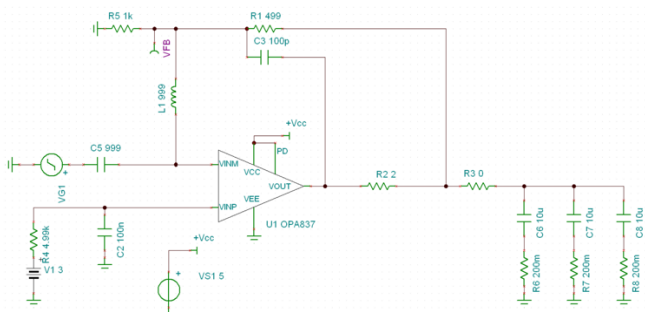
表 1. Key System Specifications

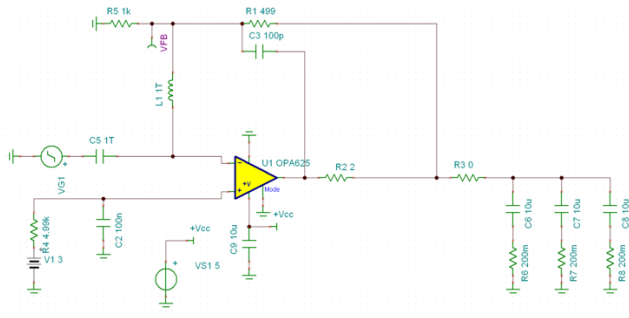
PARAMETER	SPECIFICATIONS	MEASURED
Number of channels	Dual	Dual
Input type	Differential	Differential
Input range	8- $V_{pp}$ fully differential	8- $V_{pp}$ fully differential
Resolution	18 bits	18 bits
SNR	> 96 dB	96.70 dB
THD	< -118 dB	-119.76 dB
ENOB	> 15 bit	15.77 bits
System power	< 2.5 W	1.94 W
Form factor (L x W)	120 x 100 mm	112.98 x 99.82 mm



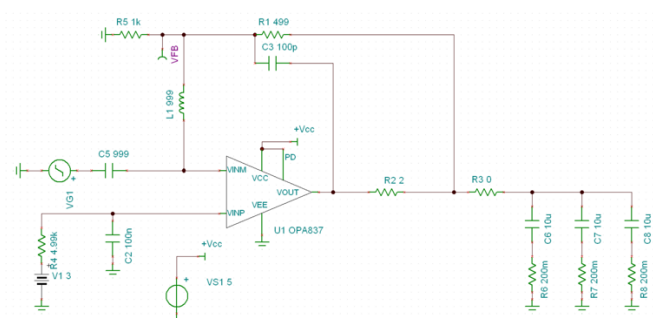
## 2.2 System Design Theory

### 2.2.1 Stability Analysis

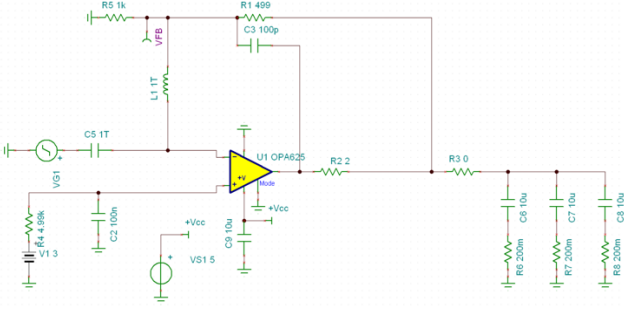
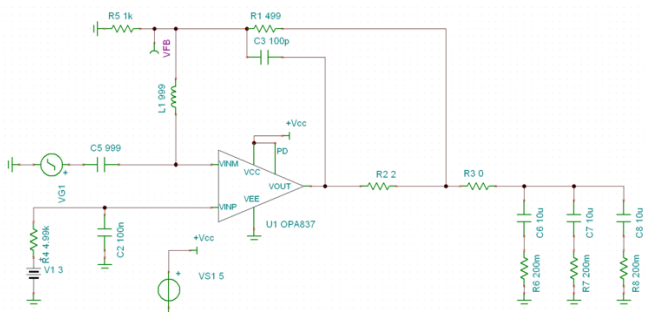
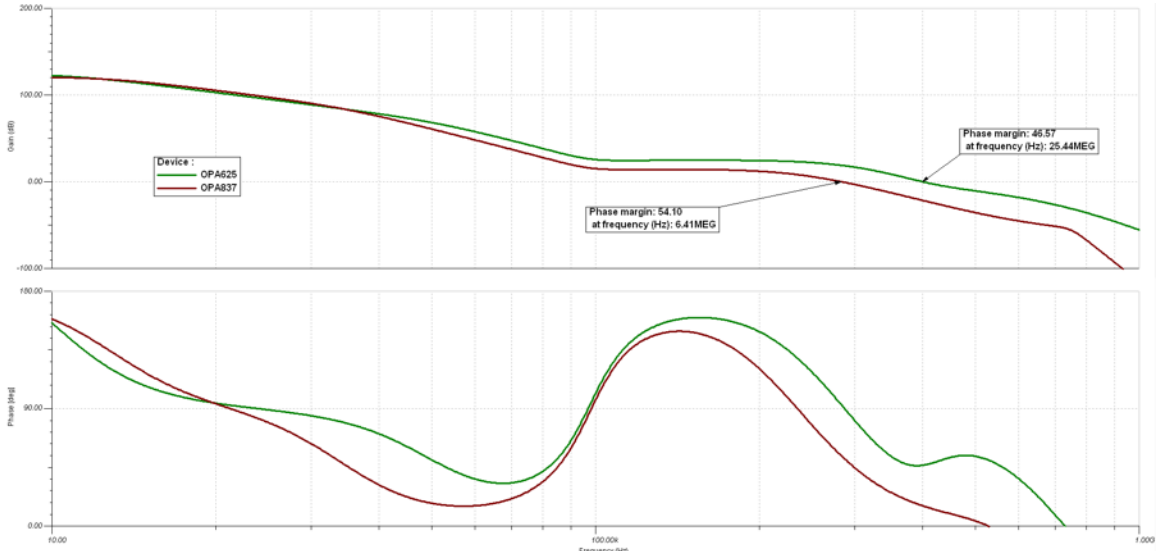
Both the OPA837 and the OPA625 are used in the reference buffer. To make sure that the devices function properly, a loop gain analysis is setup in TINA-TI™ to verify stability.  3 and  4 show the circuits set up in TINA-TI for both devices.

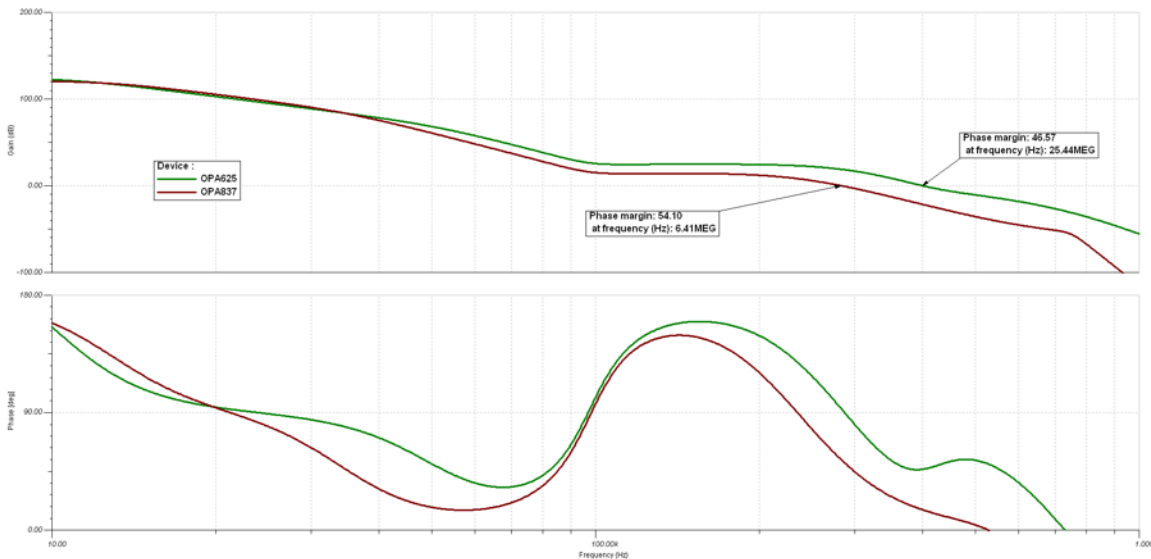


 3. OPA625 Stability Circuit



 4. OPA837 Stability Circuit

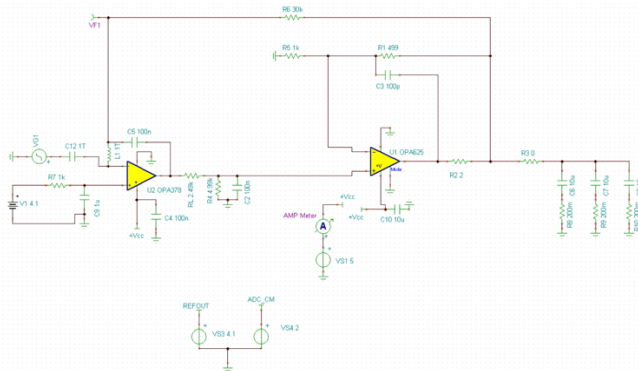
 3 shows the OPA625 circuit created to test stability.  4 shows the same setup with the OPA837 to test stability. Both devices are pin-to-pin compatible with the exception of the Mode and PD pin. This compatibility makes it easy to swap out each op amp during testing by using a 0-Ω resistor. An AC analysis is performed to verify stability with the results illustrated in  5.



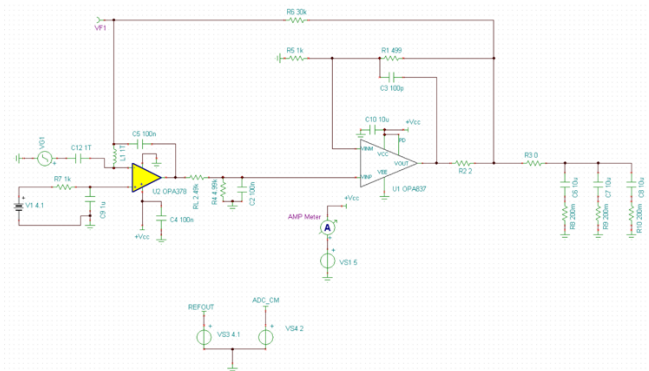
 5. AC Analysis Results for Both Op Amps

The rule of thumb for op-amp stability is to have a phase margin of at least 45 degrees or above. The OPA625 has a phase margin of 46.57 degrees, and the OPA837 has a phase margin of 54.10 degrees. Both op amps are stable in the same configuration, which is important as to not create additional variables for performance comparison.

With the stability for each op amp individually verified, the full dual-stage buffer system is created in TINA-TI to test the stability of the overall system. These circuits can be seen in [Figure 6](#) and [Figure 7](#).

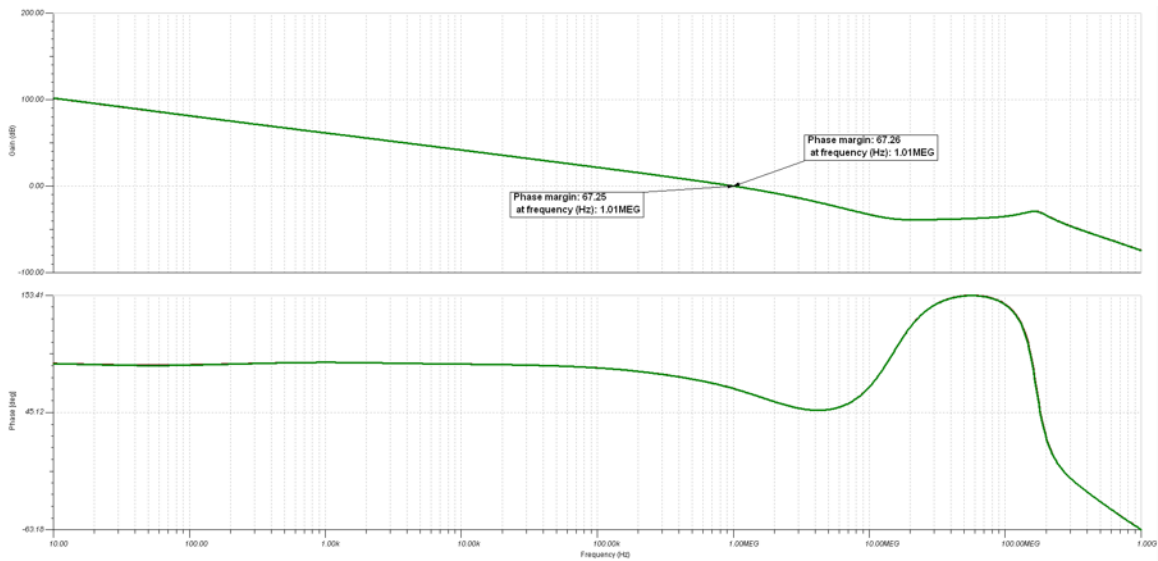


**Figure 6. OPA625 Full-Loop Stability Circuit**



**Figure 7. OPA837 Full-Loop Stability Circuit**

Both circuits are now simulated with the OPA378 added to the front end. The overall circuit is simulated with a 4.1-V input that emulates the output of the REF5040. Again, an AC analysis is performed for these two circuits to verify the stability. The results are illustrated in [Figure 8](#).

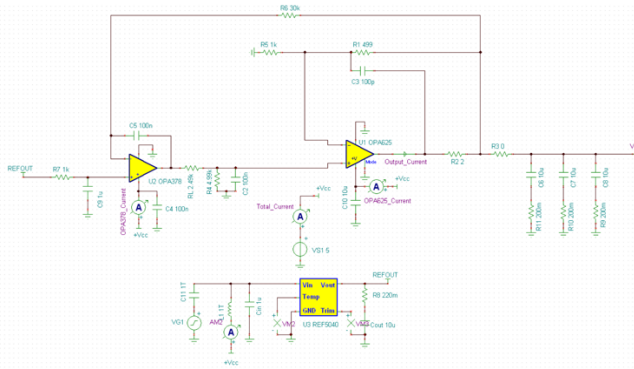


**Figure 8. Full-Loop AC Analysis Results for Both Op Amps**

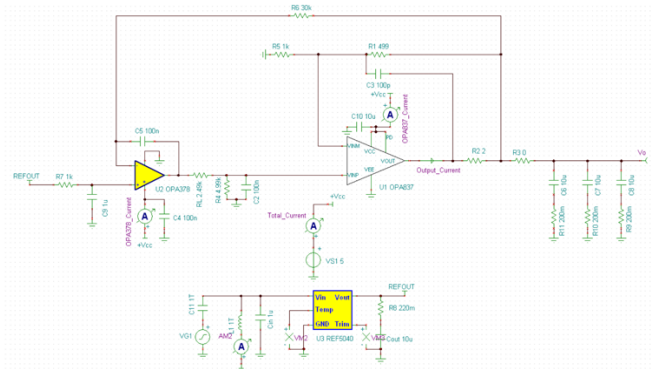
Both circuits have identical phase margin of 67.26 degrees, making both op amps stable in the whole buffer system. With circuit stability verified, more simulations are made to observe the noise and power performance of the buffer system.

### 2.2.2 Power and Noise Analysis

The main benefit of the OPA837 comes from its lower power consumption compared to the OPA625. A simulation is created in TINA-TI to verify that the overall power consumption of the buffer system implementing the OPA837 is indeed lower than that of the system implementing the OPA625. Two circuits are made in TINA-TI: one containing the OPA625 (see [Figure 9](#)) and the other containing the OPA837 (see [Figure 10](#)).



**Figure 9. OPA625 Power and Noise Optimization Circuit**



**Figure 10. OPA837 Power and Noise Optimization Circuit**

Both circuits contain current probes to observe the amount of current being drawn from the power source. A DC analysis is performed on both circuits in [Figure 9](#) (containing the OPA625) and [Figure 10](#) (containing the OPA837). The results are displayed in [Figure 11](#) and [Figure 12](#), respectively.

Measurement	Value
I_VG1[13.0]	0A
I_VS1[2.0]	-6.17mA
OPA378_Current	640.6uA
OPA625_Current	4.73mA
Output_Current	2.73mA
<b>Total_Current</b>	<b>6.17mA</b>
VM2	575.01mV
VM3	1.2V
Vo	4.1V

**Figure 11. OPA625 DC Analysis Results**

Measurement	Value
I_VG1[9.0]	0A
I_VS1[4.0]	-4.8mA
OPA378_Current	655.5uA
OPA837_Current	3.35mA
Output_Current	2.75mA
<b>Total_Current</b>	<b>4.8mA</b>
VM2	575.01mV
VM3	1.2V
Vo	4.1V

**Figure 12. OPA837 DC Analysis Results**

The current drawn for the OPA837 circuit is 1.37 mA less than that of the OPA625. This equates to a 6.85 mW power improvement. This result is expected by comparing the quiescent current values from the device datasheets.

The OPA837 is the better device when it comes to power efficiency, but it is also important to verify that the total noise on the output is comparable to the OPA625. To do this, the same two circuits are used from the power simulations to perform a noise analysis. The results of that analysis are illustrated in [Figure 13](#).

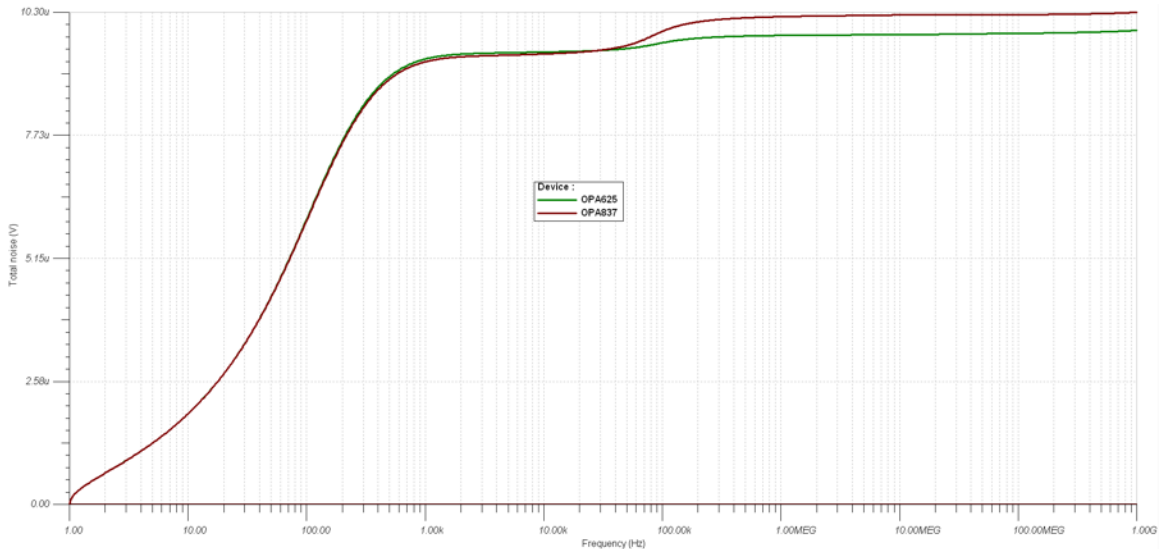


Figure 13. Noise Analysis Results for Both Op Amps

The total noise performance is similar with both op amps. The OPA625 has 300 nV less noise than the OPA837. To verify if the noise affects the performance of the ADC, it needs to be compared to the LSB value of the ADC. The value of 1 LSB for an 18-bit ADC with a 4.096-V reference voltage is 15.625  $\mu$ V. The results show that the noise reaches 10.3  $\mu$ V, which is not ideal because it exceeds half an LSB; however, this is done to achieve lowest power.

### 2.2.3 Transient Analysis

The ADS9110 is a high-performance successive approximation register (SAR) ADC with a sampling rate of 2 MSPS. With that, it takes a fast slew rate to charge the sampling capacitors before each sample occurs. To verify that the slew rates of both op amps are fast enough to recover after each sample of the ADC, a transient simulation is set up in TINA-TI. Both circuits for the OPA625 and OPA837 created in TINA-TI are shown in [Figure 14](#) and [Figure 15](#), respectively.

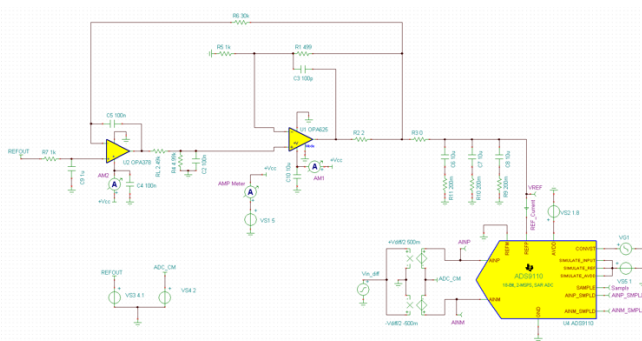


Figure 14. OPA625 Transient Circuit

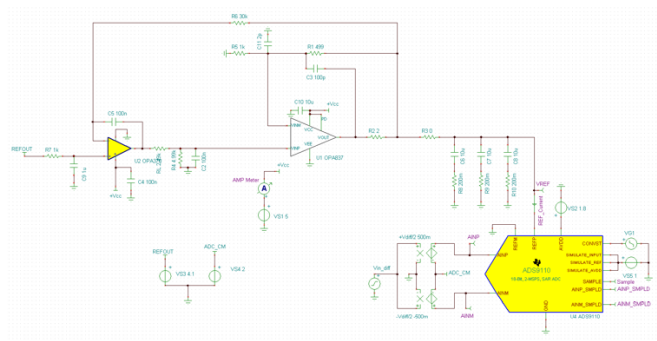
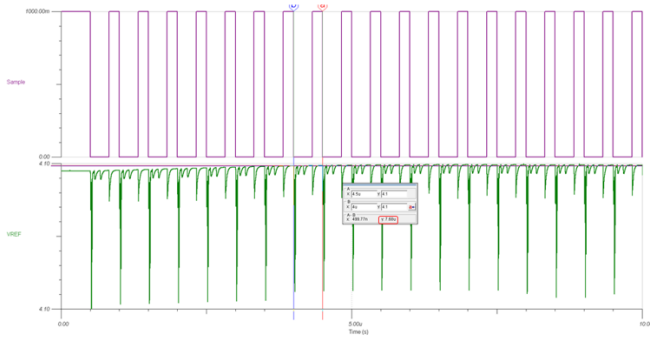
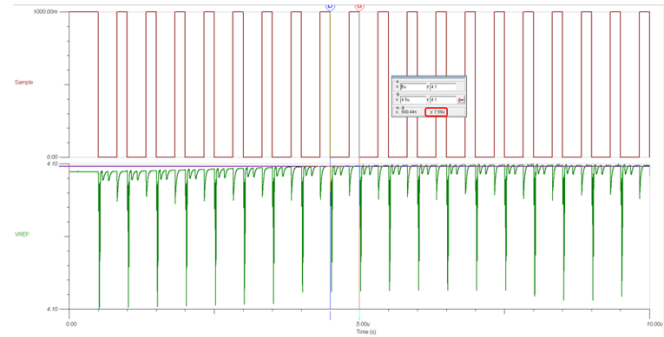


Figure 15. OPA837 Transient Circuit

The ADS9110 is simulated to mirror the physical test setup. A 10- $\mu$ s transient analysis is performed on both circuits, and the results are displayed in [Figure 16](#) and [Figure 17](#).



**Figure 16. OPA625 Transient Analysis Results**



**Figure 17. OPA837 Transient Analysis Results**

The top waveform named "Sample" is the simulated 2 MSPS for the ADS9110. Each sample occurs on the falling edge of the square wave. The waveform named "VREF" is the input of the REF pin of the ADS9110. Markers are placed at the beginning of two samples on the VREF waveform to measure the difference in voltage between them. The OPA625 has a voltage difference between samples of about 7.68  $\mu$ V, which is slightly above the 7.59  $\mu$ V of the OPA837. The transient performance for each op amp is very comparable.

## 2.3 Highlighted Products

### 2.3.1 OPA837

The OPA837 unity-gain stable, voltage feedback op amp provides among the highest MHz/mW of bandwidth versus power. Using only 600  $\mu$ A on a single 5-V supply, this 3.0-mW device delivers 105 MHz of bandwidth at a gain of 1 V/V. The very low-trimmed offset voltage of  $\pm 120$   $\mu$ V maximum comes with a typical drift of  $\pm 0.4$   $\mu$ V/ $^{\circ}$ C. The OPA837 provides one of the lowest input noise levels at 4.7 nV for its 3-mW quiescent power. The very high 50-MHz gain bandwidth product provides the low output impedance to high frequencies required to supply the fast charging currents in SAR driver application. This low dynamic output impedance also makes this a great reference buffer as it is used in this reference design.

### 2.3.2 REF5040

The REF5040 is a low-noise, low-drift, very high-precision voltage reference. This reference is capable of both sinking and sourcing current and has excellent line and load regulation. Excellent temperature drift (3 ppm/ $^{\circ}$ C) and high accuracy (0.05%) are achieved using proprietary design techniques. Combined with very low noise, these features make the REF5040 reference ideal for use in high-precision DAQ systems.



### 2.3.3 ADS9110

The ADS9110 is an 18-bit, 2-MSPS, SAR ADC with enhanced performance features. The high throughput enables developers to oversample the input signal to improve dynamic range and accuracy of the measurement. The ADS9120 is a pin-compatible, 16-bit, 2.5-MSPS variant of the ADS9110. The ADS9110 boosts analog performance while maintaining high-resolution data transfer by using TI's enhanced SPI feature. Enhanced SPI enables the ADS9110 to achieve high throughput at lower clock speeds, thereby simplifying board layout and lowering system cost.

### 2.3.4 OPA378

The OPA378 is a unity-gain stable, precision operational amplifier that is free from phase reversal. The use of proprietary Zero-Drift circuitry gives the benefit of low input offset voltage over time and temperature as well as lowering the 1/f noise component. These miniature, high-precision, low quiescent current amplifiers offer high-impedance inputs that have a common-mode range 100 mV beyond the supplies, excellent CMRR, and a rail-to-rail output that swings within 10 mV of the supplies. This design results in superior performance for driving ADCs without degradation of differential linearity.

### 3 Hardware, Testing Requirements, and Test Results

#### 3.1 Required Hardware

The ensuing section outlines the information for getting the board up and running as fast as possible. To learn about the PHI board or the onboard clocking and jitter cleaner, see the [TIDA-01052 reference design](#). Take care when moving jumper pins to avoid possible damage to the components.

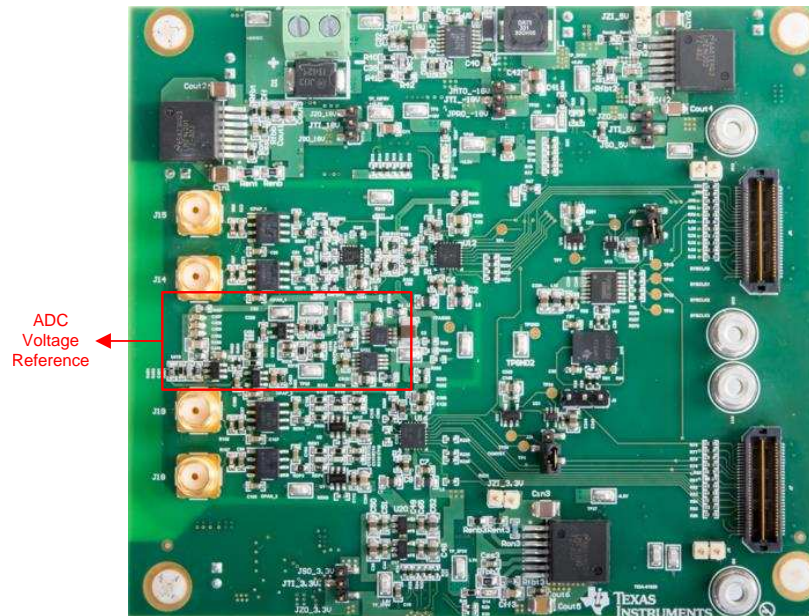


図 18. TIDA-01055 Hardware

### 3.1.1 Jumper Configuration

This system has several configurable power options. These options are selectable through the use of three-pin jumpers and two-pin jumpers. 表 2 highlights the purpose of each jumper and will assist in changing the configuration to fit the user's needs.

**表 2. Jumper Configuration**

JUMPER NAME	SHORT PINS 1 AND 2	SHORT PINS 2 AND 3	DEFAULT CONFIGURATION
JSI_18V	Power to LM53635 18-V rail	—	Short
JTI_18V	Connects LM53635 to TPS7A700 for 18-V rail	Connects LMZ14201 to TPS7A700 for 18-V rail	Short pins 1 and 2
JSI_5V	Power to LM53635 5-V rail	—	Short
JTI_5V	Connects LM53635 to TPS7A700 for 5-V rail	Connects LMZ14203 to TPS7A700 for 5-V rail	Short pins 1 and 2
JSI_3.3V	Power to LM53635 3.3-V rail	—	Short
JTI_3.3V	Connects LM53635 to TPS7A700 for 3.3-V rail	Connects LMZ14202 to TPS7A700 for 3.3-V rail	Short pins 1 and 2
JPRI_-18V	Power to LM46001 -18-V rail	—	Short
JTI_18V	Connects LM46001 to TPS7A3001 for -18-V rail	Connects LM5574 to TPS7A3001 for -18-V rail	Short pins 1 and 2
JMTI_-18V	Power to LM5574 -18-V rail	—	Open
JZI_18V	Power to LMZ14201 18-V rail	—	Open
JZI_3.3V	Power to LMZ14202 3.3-V rail	—	Open
JZI_5V	Power to LMZ14203 5-V rail	—	Open
J39	Connects -0.2-V rail to OPA625 and THS4551	Shorts -0.2-V rail to ground	Short pins 1 and 2



Figure 21 shows the reference settling analysis for both op amps. From the comparison, the OPA837 outperforms the OPA625 with its smaller voltage droop and quicker settling time. This helps solidify the OPA837 as the better option for the composite buffer.

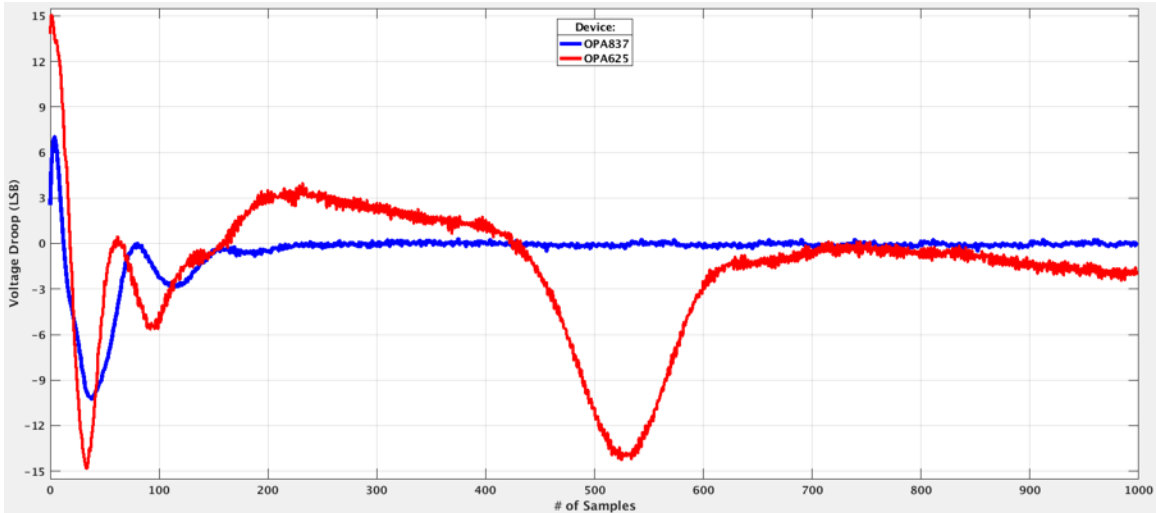


Figure 21. Reference Settling Analysis

### 3.2.2 Thick Trace versus Thin Trace Results

This design has two different trace options that connect the reference voltage to the REF pin of the ADS9110. This is to illustrate how a non-ideal layout can impact the system performance of a high-performance ADC. One of the traces is thick with a short length, and the other trace is thin with a long length. The long thin trace is not ideal because it has more resistance than the thick trace. Figure 22 and Figure 23 compare the performances of the thick trace and thin trace using the OPA837 in the buffer system.

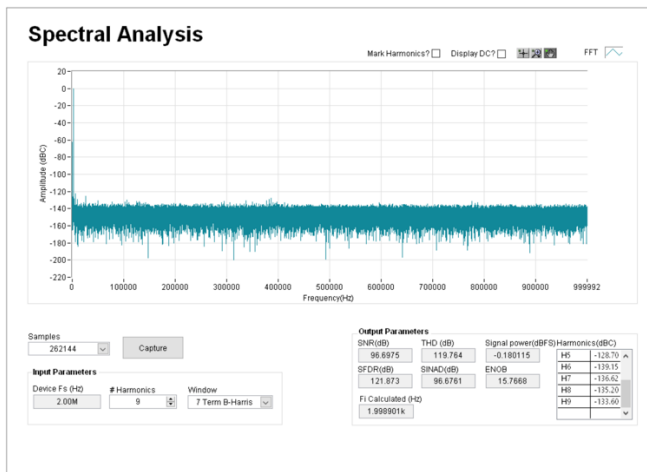


Figure 22. Spectral Analysis Using Thick Trace

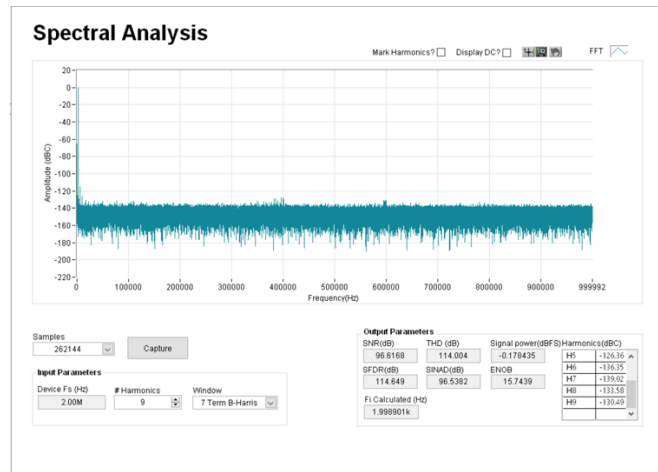


Figure 23. Spectral Analysis Using Thin Trace

From the comparison, the thin trace causes a large amount of performance degradation compared to the thick trace. Most of that degradation is attributed to the trace length, causing it to function as an antenna and coupling with the EMI from the power supplies. The higher resistance of the thin trace causes variations in the sampling capacitor charging time, which causes distortion adding to the THD. To see how the traces are laid out, see 4.3.

### 3.2.3 REF6041 Results

The REF6041 is another option for the ADC reference voltage that is included in this reference design. This device is put through the same simulations as the REF5040 and the dual stage composite buffer. In these simulations, the REF6041 performed similar to both op amps used in the buffer.

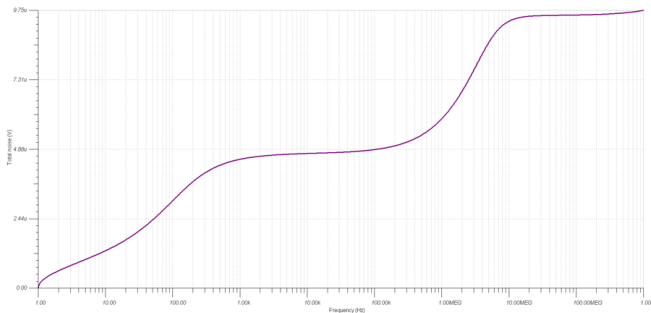


図 24. REF6041 Noise Analysis Results

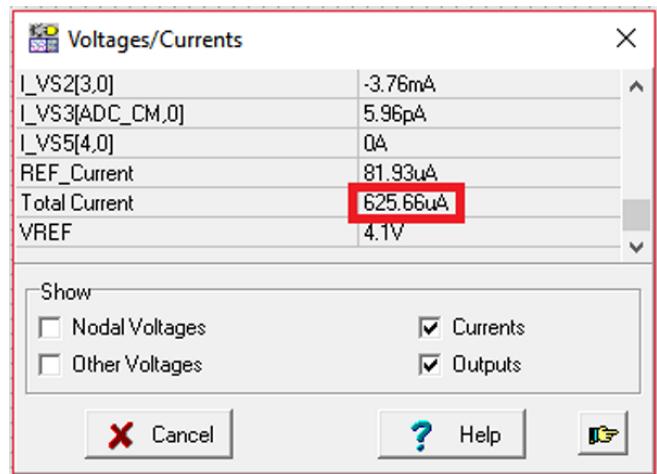


図 25. REF6041 DC Analysis

The noise performance of the REF6041 is comparable with both op-amps, but the power consumption is quite a bit lower. However, this device falls short in its current driving capability of only 4 mA. This is an important specifications to consider when using multiple ADCs in the system. The REF6041 is tested with the two ADCs in this design, and it is not able to successfully drive both. A TINA-TI simulation is made to verify results obtained from testing.

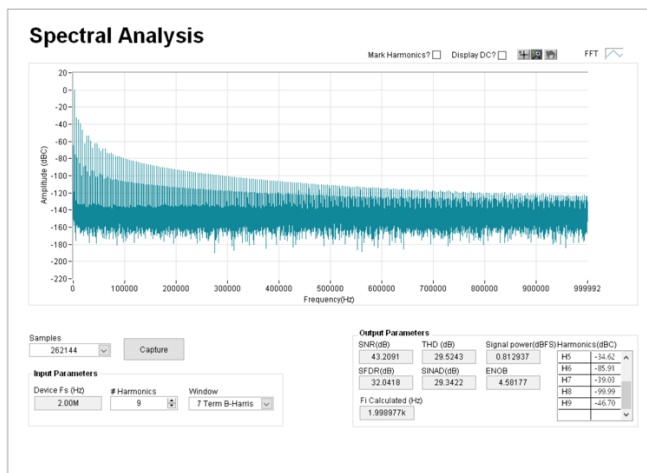


図 26. REF6041 Spectral Analysis

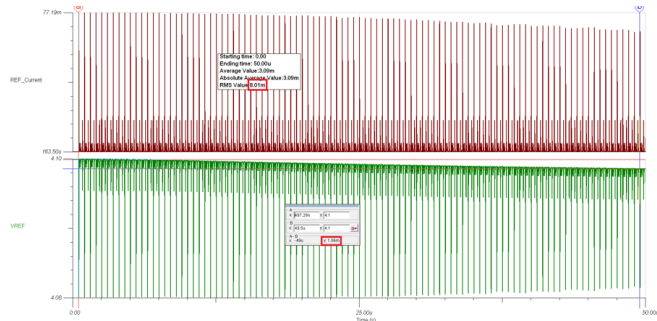


図 27. REF6041 Transient Analysis Results

Figure 26 shows the spectral analysis performed on the ADC output. The system performance is horrible when the REF6041 is used to drive two ADS9110 ADCs at 2 MSPS. The TINA-TI simulation results in Figure 27 show the voltage and current output of the REF6041. Notice how the voltage "VREF" slowly drops as more and more samples are being taken. Markers are set to measure the voltage drop of 1.06 mV from the first sample to the last in the 50- $\mu$ s window. The RMS value of the current "Iout" was taken to average out the current spikes from each sample. This RMS current value is 8 mA, which exceeds the drive capability of the REF6041. A good representation of how this affects the output of the ADC is displayed in Figure 28.

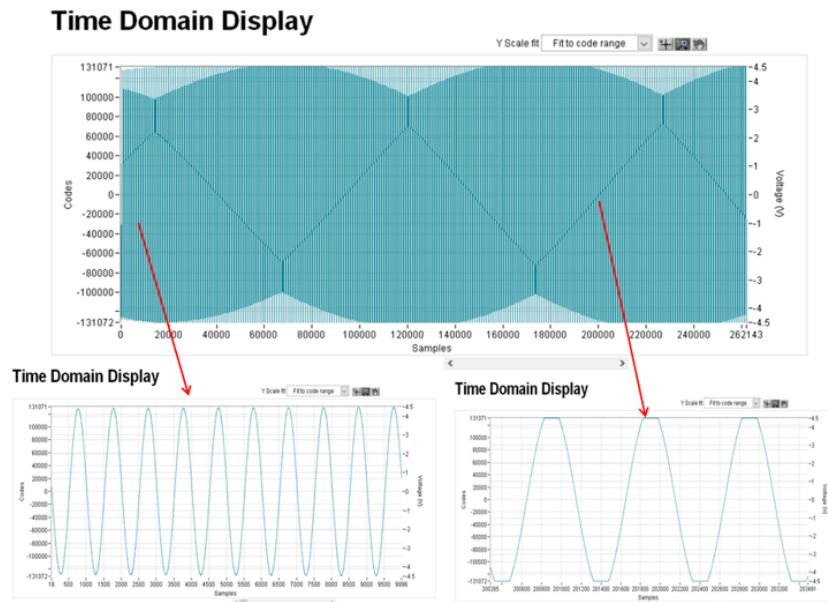


Figure 28. REF6041 Time Domain Waveform

Figure 28 displays the results from Figure 26 in the time domain. The waveforms magnitude begins to gradually increase as more samples are taken and then the waveform starts to clip after around 20,000 samples. The input signal amplitude is not actually increasing, but the REF6041 output voltage is not able to recover back to the 4.096 V as seen in the TINA-TI simulation. Therefore, the ADC samples with a lower reference voltage and the full-scale range is decreasing to a point below the input signal amplitude causing the clipping.

The results of all these tests help highlight the benefit of using the dual-stage composite buffer with the OPA837. The system performance is identical to the OPA625 and it accomplishes this at lower power consumption. The REF6041 is a great device for providing a reference voltage for a single 18-bit ADC sampling at 2 MSPS. However, this reference design is meant for end-equipment with a high number of channels containing ADCs. The REF5040 with the composite buffer is able to drive multiple ADCs with great performance. This coupled with the power consumption improvement of the OPA837, makes it the better option over using a REF6041 with each ADC in the system. Lastly, consider the layout of this reference driver as the system performance is greatly impacted by a non-ideal layout. The trace must be thick enough not to add additional resistance and short enough not to act as an antenna for any radiated signals to couple to. Table 3 highlights all of the results taken from each test to help observe the performance differences, including test results for the REF6041 driving only one ADC.

**表 3. Summary of Measured Results**

LAYOUT OPTION	BUFFER ARCHITECTURE	REFERENCE DEVICE	SNR (dB)	SINAD (dB)	THD (dB)	SFDR (dB)	ENOB (Bits)
Thick trace	OPA625	REF5040	96.66	96.64	-119.15	121.32	15.76
Thick trace	OPA837	REF5040	96.70	96.68	-119.76	121.87	15.77
Thin trace	OPA625	REF5040	96.50	96.39	-112.40	112.82	15.72
Thin trace	OPA837	REF5040	96.62	96.67	-114.00	114.65	15.74
Thick trace	—	REF6041	96.70	96.67	-117.87	118.99	15.77



## 4 Design Files

### 4.1 Schematics

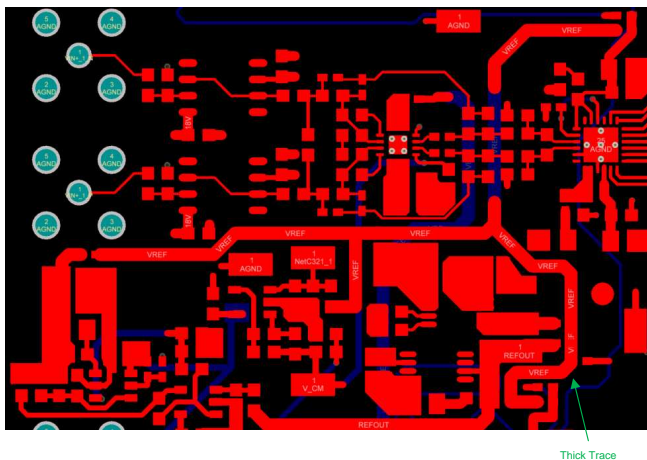
To download the schematics, see the design files at [TIDA-01055](#).

### 4.2 Bill of Materials

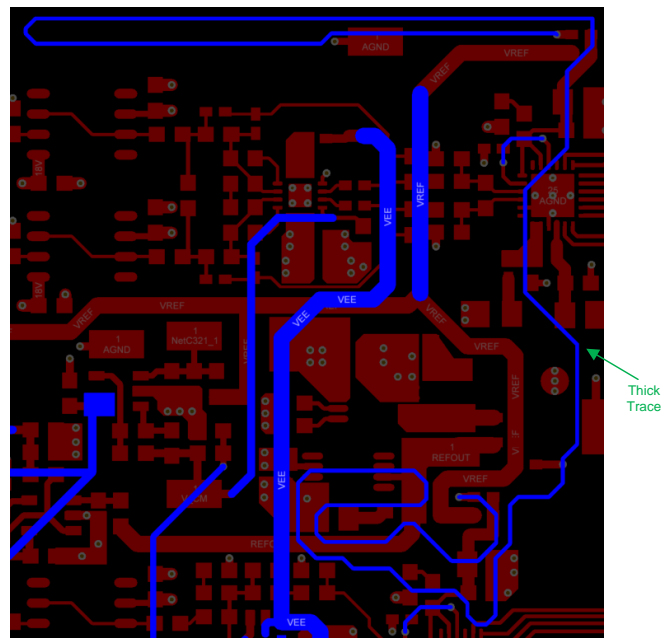
To download the bill of materials (BOM), see the design files at [TIDA-01055](#).

### 4.3 PCB Layout Recommendations

This reference design contains two layout options for the ADC reference voltage circuit. One is an ideal layout where the trace connected to the ADC REF pin is thick and has a short length. The non-ideal layout option has a long, thin trace connected to the ADC REF pin. [Figure 29](#) and [Figure 30](#) show these two different traces.



**Figure 29. Thick Trace Layout**



**Figure 30. Thin Trace Layout**

The thick trace is labeled VREF and the thin trace is labeled VREF1 though it cannot be seen due to the magnification. The thick trace is routed in a direct manner to the REF pin from the source, and the thin trace is routed to emulate the length of trace in a system with several of these channels. The thin trace is long and is routed by various power supplies making it susceptible to EMI coupling. For more layout recommendations regarding the AFE or the power design, see the [TIDA-01050](#) and [TIDA-01054](#) reference designs.

#### 4.3.1 Layout Prints

To download the layer plots, see the design files at [TIDA-01055](#).

### 4.4 Altium Project

To download the Altium project files, see the design files at [TIDA-01055](#).

## 4.5 Gerber Files

To download the Gerber files, see the design files at [TIDA-01055](#).

## 4.6 Assembly Drawings

To download the assembly drawings, see the design files at [TIDA-01055](#).

## 5 Software Files

To download the software files, see the design files at [TIDA-01055](#).

## 6 Related Documentation

1. Texas Instruments, [TIDA-01052 ADC Driver Reference Design Improving Full-Scale THD Using Negative Supply Design Guide](#)
2. Texas Instruments, [TIDA-01054 Multi-Rail Power Reference Design for Eliminating EMI Effects in High-Performance DAQ Systems Design Guide](#)
3. Texas Instruments, [TIPD113 18-Bit, 1-MSPS Data Acquisition \(DAQ\) Block Optimized for Lowest Power Design Guide](#)
4. Texas Instruments, [TIPD115 18-Bit, 1MSPS Data Acquisition Block \(DAQ\) Optimized for Lowest Distortion and Noise Design Guide](#)

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## 7 About the Authors

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## 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

### 2017年9月発行のものから更新

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