参考資料

# TI Designs: TIDA-01464
# 可変出力電圧対応、200W、92%効率、低THD、10%調光機能付きAC/DC LEDドライバのリファレンス・デザイン

TEXAS INSTRUMENTS

## 概要

このリファレンス・デザインは、100～200Vの範囲で出力電圧を調整できる、調光可能な低THDの200W AC/DC LED電源であり、街路照明や道路照明などの屋外照明アプリケーション向けに設計されています。UCC28180 CCM PFCコントローラを使用してフロントエンド力率補正(PFC)回路を設計し、UCC28740 CC-CVフライバック・コントローラを使用して疑似共振(QR)フライバック・コンバータを実装しており、出力LED電流/電圧の2次側レギュレーション(SSR)用に光カプラを用いた帰還回路を備えています。

0～10Vのアナログ電圧範囲での調光をサポートしており、IEC 61000-3-2クラスC照明機器の電流THD規格に基づくテストに合格しています。

## リソース

| | |
|---|---|
| TIDA-01464 | デザイン・フォルダ |
| UCC28180 | プロダクト・フォルダ |
| UCC28740 | プロダクト・フォルダ |
| INA180 | プロダクト・フォルダ |
| UCC28910 | プロダクト・フォルダ |
| LM358M | プロダクト・フォルダ |
| LM4040 | プロダクト・フォルダ |

TI E2E™ Community

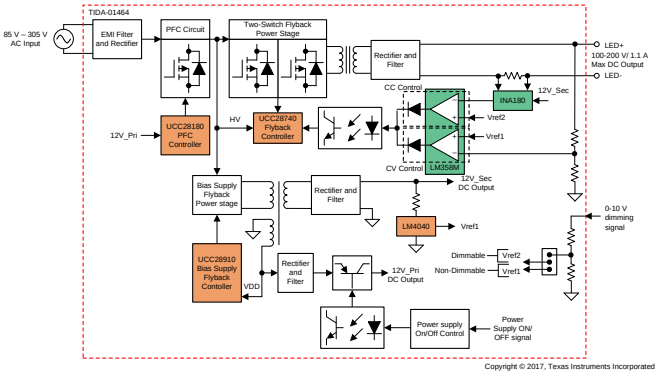
E2E™エキスパートに質問

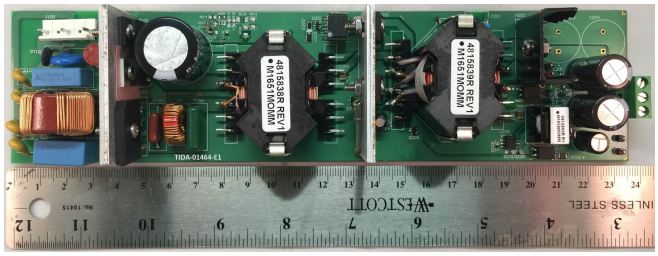
## 特長

- 85～305Vの汎用入力AC範囲と、230Vで350mW未満の極めて低いスタンバイ消費電力をサポート
- 196W負荷において120V ACでほぼ90%、230V、265V ACでほぼ92%の高効率を実現し、外部冷却は不要
- 196W負荷において120V、230V、265V ACで0.98を超える力率と5%未満のTHDを実現
- 0～10Vのアナログ調光範囲で10%未満の調光が可能
- 100～200Vの可変DC出力動作により、性能にさほど影響を与えることなく、さまざまなLED負荷のサポートを実現
- 22%以上の196V LED負荷、36%以上の102V LED負荷について、IEC 61000-3-2クラスCの電流THD規格に準拠

## アプリケーション

- 街路照明
- 道路照明
- 屋外照明



# 1 System Description

High-power LED lighting applications such as road lighting, street lighting, and Flood lighting may need power levels above 75 W to 200 W. For such requirements, generally two stage power supplies are used to get higher efficiency, lower mains ripple at the output, higher power factor, and low total harmonic distortion (THD). Two-stage architectures have a PFC stage as a front end, and power architecture like flyback or resonant convertors like LLC or LCC are used. While resonant converters can help achieving higher efficiency, generally they are tuned for specific load conditions. However, the LED power supplies that are sold as a separate unit needs to cater to different voltages of LED strings as the end user might use different numbers of LEDs or LED COBs in series. In such cases where the output voltage setting can change widely, the resonant converters efficiency are sacrificed. One of the architectures that can help to meet the cost, efficiency and design simplicity aspects of LED power supply with adjustable output voltage is the two switch flyback architecture. This 200-W LED power supply reference design has an output voltage that is adjustable from 100 V to 200 V. This design uses a CCM PFC front end to achieve low THD and high power factor. Following the PFC stage is a two-switch flyback architecture that converts DC/DC with isolation.

Due to its simplicity and low part count, flyback topology is often used in isolated switched-mode power supplies with an output power of 100 W or less. General operation principles of the flyback converter are used by power supply engineers for fast creation of new designs. Because of a low part count, designs can be made with low cost. Due to its versatility and simplicity, flyback topology can be called the 'work horse' of isolated topologies. Even though Flyback-topology is easily used with different applications, there are some drawbacks. The voltage stress of the primary-side transistor is high even in an ideal case, where the leakage effects of the transformer are not considered. When current flows on the secondary side, the drain voltage of the primary-side transistor rises to the sum of the input voltage and the reflected voltage.

When considering the parasitic ringing caused by transistor capacitances and the leakage inductance of the transformer, the voltage stress is even higher. Because the amplitude of the parasitic ringing is hard to predict, the designer must choose a transistor with a high voltage rating. High-voltage MOSFETs comes with higher on-state resistance compared to lower voltage MOSFETs. High on-state resistance increases conduction losses and leads to a reduction of efficiency. Different kinds of snubbers and clamping-circuits can reduce the transistor voltage stress. For voltage stress, snubbers and clamping-circuits are reasonable solutions, but the energy stored in the leakage inductance is dissipated in snubber and thus reducing efficiency.

The typical problems of flyback topology are overcome by using a two-switch flyback topology. When a second transistor is added between the input voltage and the transformer, the overall voltage stress is divided equally over both transistors. Instead of turning leakage energy into losses, it is now returned to the input supply through two diodes. Diodes also clamp drain-source voltages of both transistors to the input voltage, so the voltage rating of the transistors can be selected according to input voltage without a bigger margin. Due to these improvements, the two-switch flyback topology is an option over traditional flyback topology.

図 1 and 図 2 show examples of high-wattage AC/DC LED power supplies in outdoor lighting applications.

**図 1. Street Lighting**

**図 2. Flood Lighting**

## 1.1 Key System Specifications

**表 1. Key System Specifications**

| PARAMETER | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| **INPUT CONDITIONS** | | | | | |
| Input voltage ($V_{INAC}$) | | 85 | 120/230/265 | 305 | VAC |
| Frequency ($f_{LINE}$) | | 47 | 50 | 60 | Hz |
| Standby power | | | | 0.35 | W |
| No load power (PNL) | $V_{INAC}$ = 230 V, $I_{OUT}$ = 0 A | | | 1.3 | W |
| **OUTPUT CONDITIONS** | | | | | |
| Output voltage | | | 198 | | V |
| Output current | | | | 1.1 | A |
| Line regulation | | | | 0.5 | % |
| Load regulation | | | | 0.5 | % |
| Output voltage ripple | | | 20 | 50 | mV |
| Output power | | | | 200 | W |
| THD | $V_{INAC}$ = 85 - 305 V, $P_{OUT}$ > 25% of full load | | < 20 | | % |
| Hold-up time ($t_{HOLD}$) | $V_{INAC}$ = 120 V | | > 30 | | ms |
| | $V_{INAC}$ = 230 V | | > 50 | | ms |
| Primary-to-secondary insulation | | | | 4 | kV |
| **SYSTEM CHARACTERISTICS** | | | | | |
| Efficiency (η) | $V_{IN}$ = 265-V AC, $I_{OUT}$ = 1 A | | | > 92 | % |
| Protections | Output overvoltage (settable) | | | | |
| | Output overcurrent | | | | |
| | Thermal shutdown (temperature at the sense point) | | | | |
| | Output open loop protection | | | | |
| Operating ambient | Open frame | –40 | 25 | 60 | °C |
| Power line harmonics | As per IEC 61000-3-2 Class-C Lighting Equipment | | | | |
| Dimensions | Length × Breadth × Height | 120 × 82 × 35 | | | mm |

# 2 System Overview

## 2.1 Block Diagram

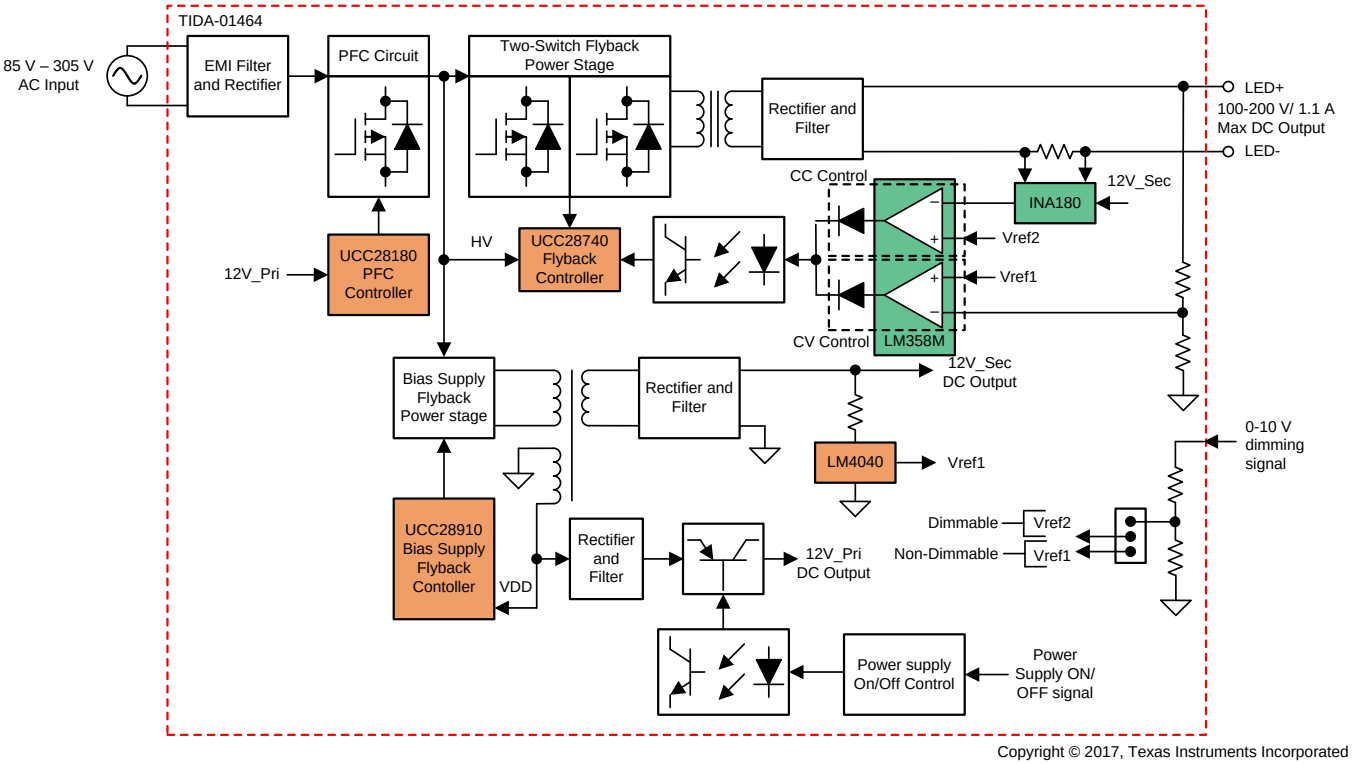





**図 3. TIDA-01464 Block Diagram**

## 2.2 Highlighted Products

This reference design uses the following highlighted products. Key features for selecting the devices for this reference design are given in the following sections. Find complete details of the highlighted devices in their respective product data sheets.

### 2.2.1 UCC28180

To implement the low-cost, small form factor, PFC design to meet THD requirements at 200-W power, the UCC28180 is the preferred controller because it offers series of benefits to meet IEC 61000-3-2 Class C THD norms and achieve high power factor for wide input voltage range of operation.

The UCC28180 is a flexible and easy-to-use, 8-pin, active PFC controller that operates under Continuous Conduction Mode (CCM) to achieve a high PF, low current distortion, and excellent voltage regulation of boost pre-regulators in AC/DC front ends. The controller is suitable for universal AC input systems operating in 100-W to few-kW range with the switching frequency programmable between 18 to 250 kHz. This switching frequency allows the device to support both power MOSFET and IGBT switches. An integrated 1.5-A and 2-A (SRC-SNK) peak gate drive output, clamped internally at 15.2 V (typical), enables fast turnon, turnoff, and easy management of the external power switch without the need for buffer circuits.

Low-distortion wave shaping of the input current using average current mode control is achieved without input line sensing, reducing the external component count. In addition, the controller features reduced current sense thresholds to facilitate the use of small-value shunt resistors for reduced power dissipation. This reduced dissipation is especially important in high-power systems. To enable low current distortion, the controller also features trimmed internal current loop regulation circuits for eliminating associated inaccuracies.

Key features that make this device unique are:

- 8-pin solution (no AC line sensing needed)
- Wide range programmable switching frequency (18 to 250 kHz for MOSFET and IGBT-based PFC converters)
- Trimmed current loop circuits for low iTHD
- Reduced current sense threshold (minimizes power dissipation in shunt)
- Average current-mode control
- Soft overcurrent and cycle-by-cycle peak current limit protection
- Output overvoltage protection with hysteresis recovery
- Audible noise minimization circuitry
- Open loop detection
- Enhance dynamic response during output overvoltage and undervoltage conditions
- Maximum duty cycle of 96% (typ)
- Burst mode for no load regulation
- VCC UVLO, low ICC start-up (< 75 µA)

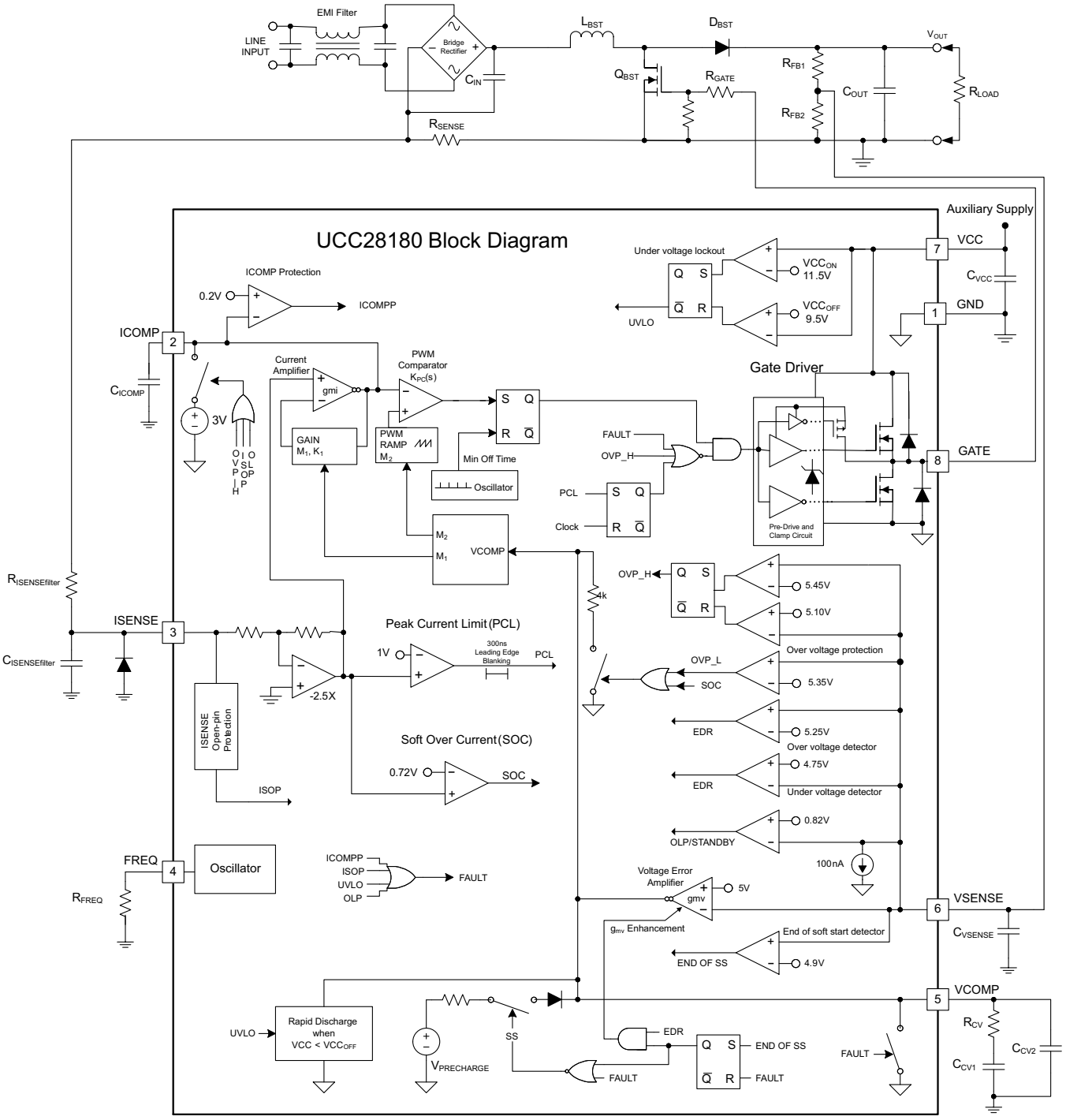





**図 4. UCC28180 Functional Block Diagram**

### 2.2.2 UCC28740

To implement the high-performance, small form factor, flyback design at 200-W power, the UCC28740 is preferred because it offers a series of benefits to address the needs of the next generation DIN rail power supply of low reduced feedback loops for precision current limit and power limit. This eliminates the need of external current sensing on the secondary side and multiple optocoupler feedback loops for open loop detection and power limiting.

The UCC28740 isolated-flyback power supply controller provides CV output regulation using an optical coupler to improve transient response to large load steps. CC regulation is accomplished through PSR techniques. This device processes information from optocoupled feedback and from an auxiliary flyback winding for precise high-performance control of output voltage and current. An internal 700-V startup switch, dynamically-controlled operating states, and a tailored modulation profile support ultra-low standby power without sacrificing startup time or output transient response. The drive output interfaces to a MOSFET power switch. Discontinuous conduction mode (DCM) with valley switching reduces switching losses. Modulating the switching frequency and primary current peak amplitude (FM and AM) keeps the conversion efficiency high across the entire load and line ranges.

Key features that make this device unique are:

- Optocoupled feedback regulation for CV and PSR for CC
- Enables ±1% voltage regulation and ±5% current regulation across line and load
- 100-kHz max switching frequency enables high power density charger designs
- QR valley switching operation for highest overall efficiency
- Frequency jitter scheme to ease EMI compliance
- Wide VDD range (35 V) allows small bias capacitor
- Drive output for MOSFET
- Enables <10-mW system standby and no load power
- Protection functions: Overvoltage, low line, and overcurrent
- SOIC-7 package

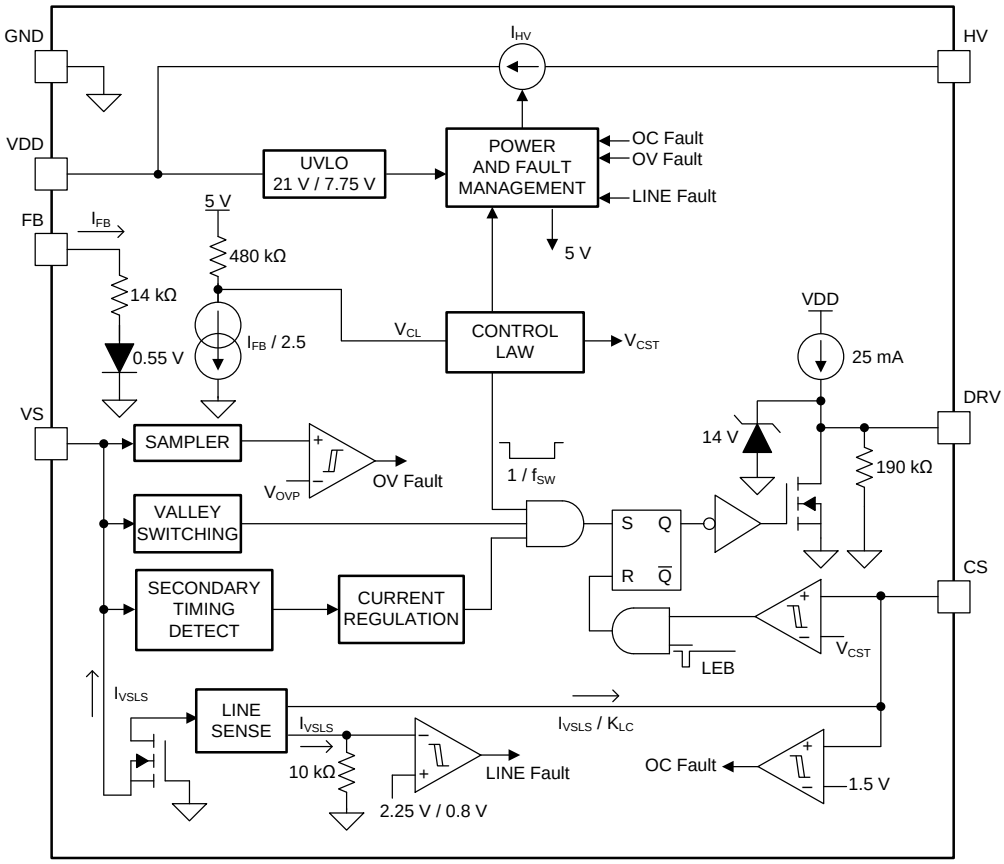





**図 5. UCC28740 Functional Block Diagram**

### 2.2.3 UCC28910

The UCC28910 is a high-voltage flyback switcher that provides output voltage and current regulation without the use of an optical coupler. This device incorporates a 700-V power FET and a controller that process operating information from the flyback auxiliary winding and power FET to provide a precise output voltage and current control. The integrated high-voltage current source for startup that is switched off during device operation, and the controller current consumption is dynamically adjusted with load. Both enable the very low standby power consumption.

Control algorithms in the UCC28910 that combining switching frequency and peak primary current modulation allow operating efficiencies to meet or exceed applicable standards. DCM with valley switching is used to reduce switching losses. Built-in protection features help to keep secondary and primary component stress levels in check across the operating range. The frequency jitter helps to reduce EMI filter cost.

Key features that make this device unique are:

- CV and CC output regulation without an optic coupler
- ±5% output voltage regulation accuracy
- ±5% output current regulation with AC line and primary inductance tolerance compensation
- 700-V start-up and smart power management enables <30-mW standby power

- 115-kHz maximum switching frequency design for high-power density
- Valley switching and frequency dithering to ease EMI compliance
- Thermal shutdown
- Low line and output overvoltage protection

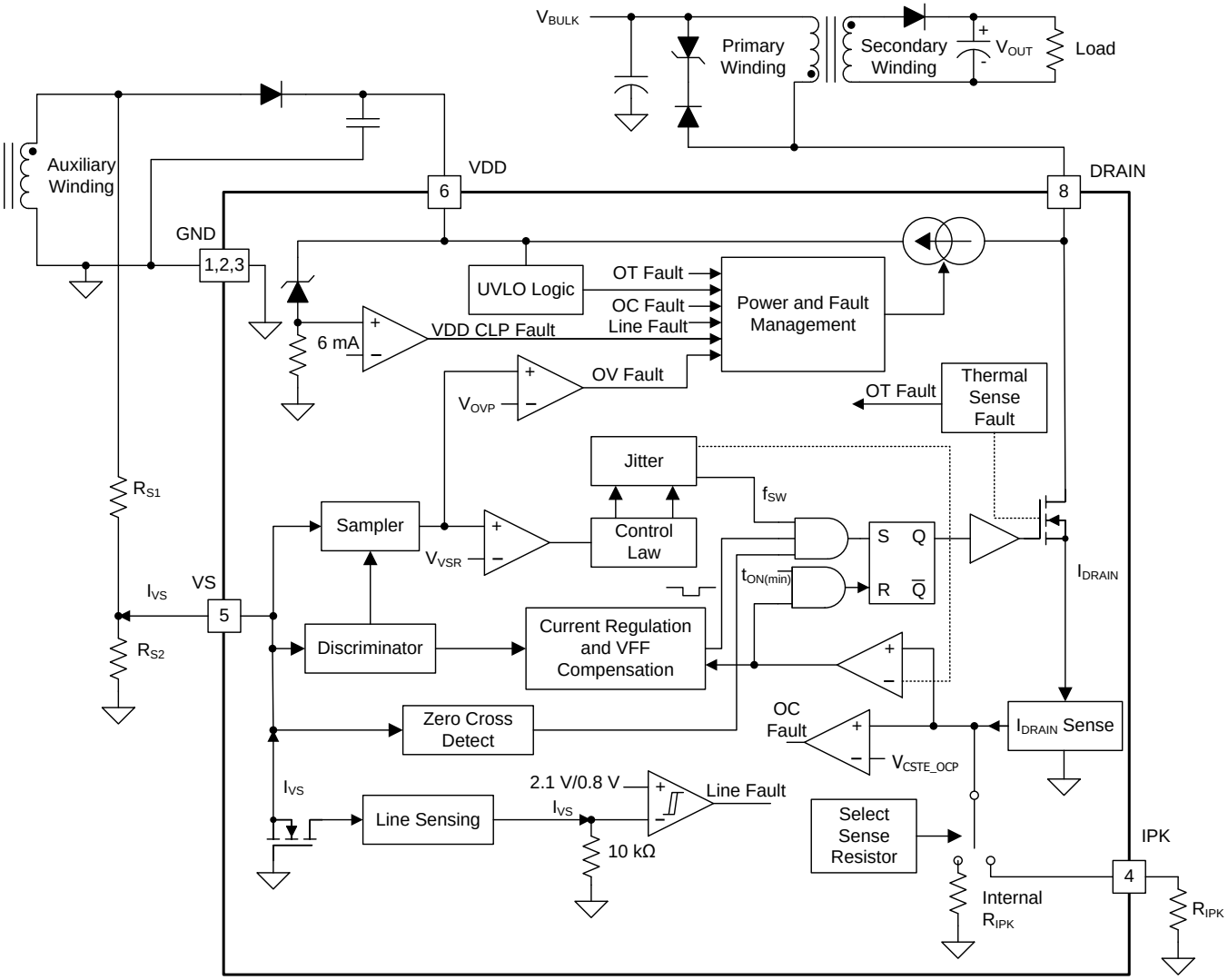



**図 6. UCC28910 Functional Block Diagram**

### 2.2.4 INA180

The INA180 is a family of cost-optimized current sense amplifiers (also called current-shunt monitors) that sense voltage drops across current-sense resistors at common-mode voltages from –0.2 to 26 V, independent of the supply voltage. The INA180 integrates a matched resistor gain network in four, fixed-gain device options: 20 V/V, 50 V/V, 100 V/V, or 200 V/V. This matched gain resistor network minimizes gain error and reduces the temperature drift.

The INA180 operates from a single 2.7- to 5.5-V power supply, drawing a maximum of 260 µA of supply current. All device options are specified over the extended operating temperature range of –40°C to +125°C and are available in a 5-pin, SOT-23 package with two different pin configurations.

Key features that make this device unique are:

- Common-mode range ($V_{CM}$): –0.2 to 26 V
- High bandwidth: 350 kHz
- Offset voltage:
  - ±150 µV (max) at $V_{CM}$ = 0 V
  - ±500 µV (max) at $V_{CM}$ = 12 V
- Output slew rate: 2 V/µs
- Accuracy:
  - ±1% gain error (max)
  - 1-µV/°C offset drift (max)
- Gain options:
  - 20 V/V (A1 devices)
  - 50 V/V (A2 devices)
  - 100 V/V (A3 devices)
  - 200 V/V (A4 devices)
- Quiescent current: 260 µA (max)

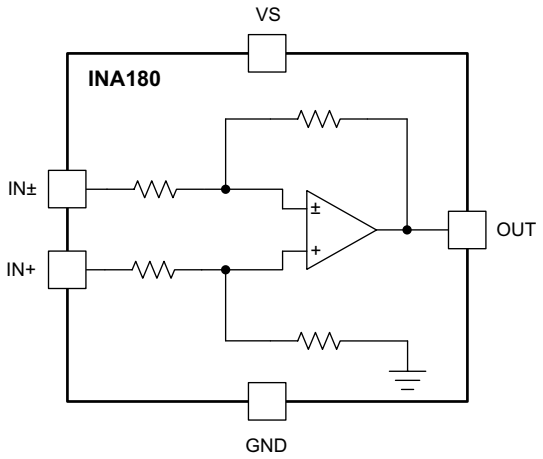





**図 7. INA180 Functional Block Diagram**

### 2.2.5 LM358

The LM358 device consist of two independent, high-gain, frequency-compensated operational amplifiers designed to operate from a single supply over a wide range of voltages. Operation from split supplies also is possible if the difference between the two supplies is 3 to 32 V (3 to 26 V for the LM2904 device), and VCC is at least 1.5 V more positive than the input common-mode voltage. The low supply-current drain is independent of the magnitude of the supply voltage.

Key features that make this device unique are:

- Wide supply ranges:
  - Single supply: 3 to 32 V
  - Dual supplies: ±1.5 to ±16 V
- Low supply-current drain, independent of supply voltage: 0.7 mA (typ)
- Wide unity gain bandwidth: 0.7 MHz
- Common-mode input voltage range includes ground, allowing direct sensing near ground
- Low input bias and offset parameters:
  - Input offset voltage: 3 mV (typ)
    A versions: 2 mV (typ)
  - Input offset current: 2 nA (typ)
  - Input bias current: 20 nA (typ)
    A versions: 15 nA (typ)
- Differential input voltage range equal to maximum-rated supply voltage: 32 V
- Open-loop differential voltage gain: 100 dB (typ)
- Internal frequency compensation
- On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

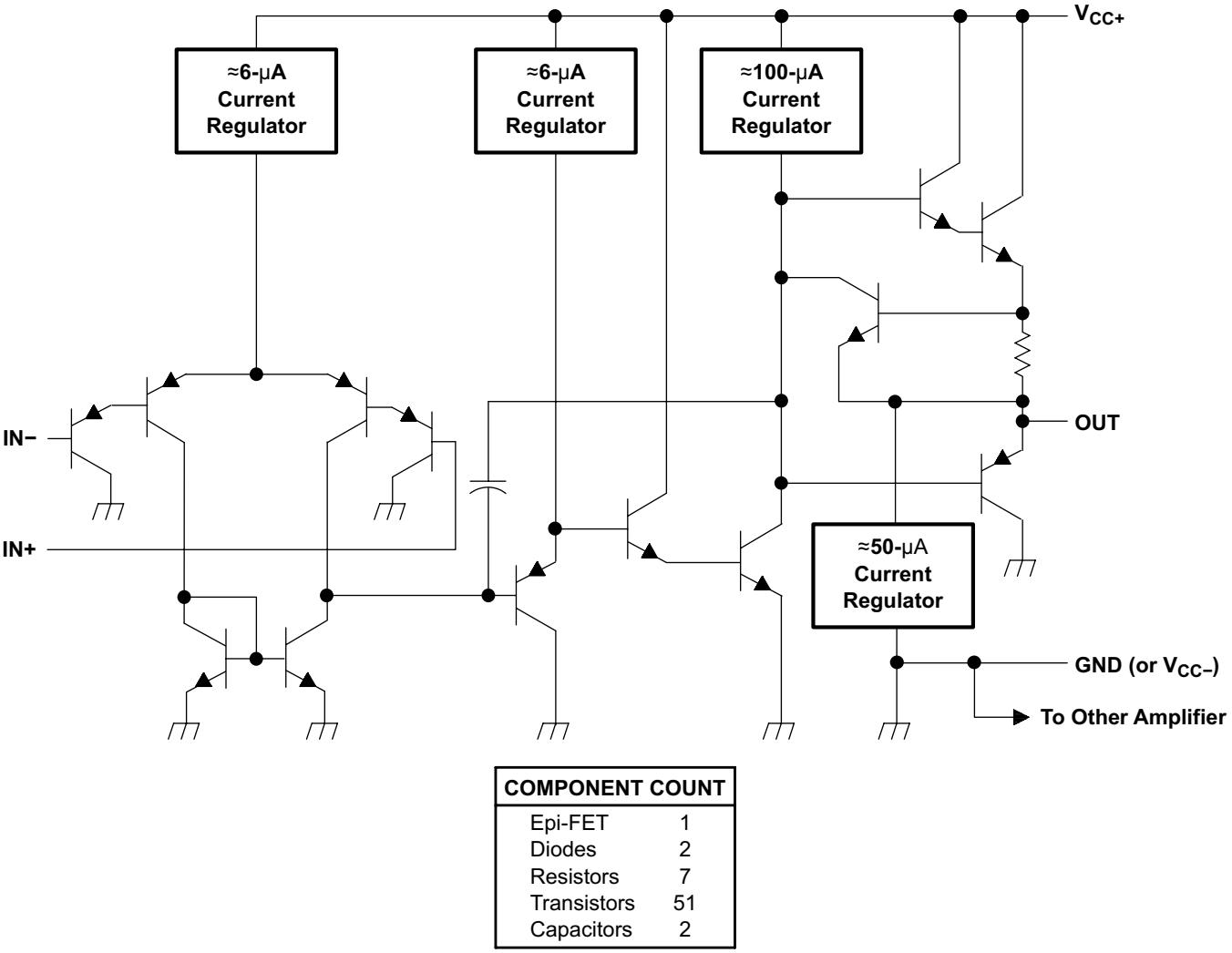



**図 8. LM358 Functional Block Diagram**

### 2.2.6 LM4040

The LM4040-N is a precision micropower, curvature-corrected, band-gap shunt voltage reference. For space critical applications, the LM4040-N is available in the sub-miniature SOT-23 and SC70 surface-mount package. The LM4040-N is designed for stable operation without the need of an external capacitor connected between the + pin and the − pin. If, however, a bypass capacitor is used, the LM4040-N remains stable. Reducing design effort is the availability of several fixed reverse breakdown voltages: 2.048 V, 2.5 V, 3 V, 4.096 V, 5 V, 8.192 V, and 10 V. The minimum operating current increases from 60 µA for the LM4040-N-2.048 and LM4040-N-2.5 to 100 µA for the 10-V LM4040-N. All versions have a maximum operating current of 15 mA.

Key features that make this device unique are:

- Fixed reverse breakdown voltages of 2.048 V, 2.5 V, 3 V, 4.096 V, 5 V, 8.192 V, and 10 V
- Wide operating current range: 45 µA (typ) to 15 mA
- Stable with all capacitive loads; no output capacitor required
- Available in extended temperature range: –40°C packages to +125°C

- Low output noise: 35 $\mu V_{RMS}$ (typ)
- Small packages: SOT-23, TO-92, and SC70

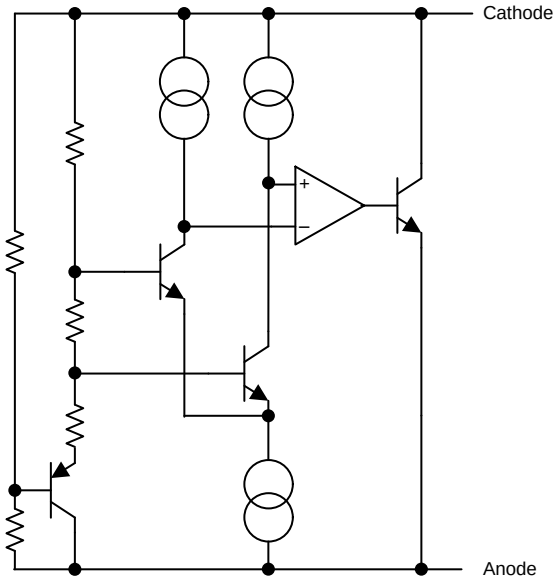



**図 9. LM4040 Functional Block Diagram**

## 2.3 System Design Theory

This reference design provides 200 W of continuous power over a wide AC input range from 85- to 305-V AC with power factor correction. The UCC28180 controls a PFC boost front-end power stage to generate DC output voltage, while the UCC28740 QR flyback controller converts the PFC output to isolated 198 V and 1.1 A. The total system efficiency is over 92% with a 265-V AC input and over 90% with a 120-V AC input under full load conditions. The design has a precise current limit and limits the power to less than 200 W under all fault conditions. In addition, several protections are embedded into this reference design, which includes output over-voltage and output over-current protection. High efficiency, high PF, low THD, and low standby power are the main focuses of this reference design.

### 2.3.1 PFC Circuit Component Design

**表 2. Design Goal Parameters for PFC**

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **INPUT CHARACTERISTICS** | | | | | | |
| $V_{IN}$ | Input voltage | | 85 | | 305 | VAC |
| $f_{LINE}$ | Input frequency | | 47 | | 63 | Hz |
| $I_{IN(peak)}$ | Peak input current | $V_{IN} = V_{IN(min)}$, $I_{OUT} = I_{OUT(max)}$ | | | 3.8 | A |
| **OUTPUT CHARACTERISTICS** | | | | | | |
| $V_{OUT}$ | Output voltage | $I_{OUT} \le I_{OUT(max)}$, $f_{LINE(min)} \le f_{LINE} \le f_{LINE(max)}$, $V_{IN(min)} \le V_{IN} \le V_{IN(max)}$ | 431 | 434 | 444 | VDC |
| | Line regulation | $I_{OUT} = I_{OUT(max)}$ $V_{IN(min)} \le V_{IN} \le V_{IN(max)}$ | | | 5 | |
| | Load regulation | $V_{IN}$ = 85-V AC, $f_{LINE}$ = 60 Hz, $I_{OUT(min)} \le I_{OUT} \le I_{OUT(max)}$ | | | 5 | % |
| | | $V_{IN}$ = 230-V AC, $f_{LINE}$ = 60 Hz, $I_{OUT(min)} \le I_{OUT} \le I_{OUT(max)}$ | | | 5 | % |
| $I_{OUT}$ | Output load current | $V_{IN(min)} \le V_{IN} \le V_{IN(max)}$ $f_{LINE(min)} \le f_{LINE} \le f_{LINE(max)}$ | 0 | | 0.507 | A |
| $P_{OUT}$ | Output power | $V_{IN(min)} \le V_{IN} \le V_{IN(max)}$ $f_{LINE(min)} \le f_{LINE} \le f_{LINE(max)}$ | 0 | | 220 | W |
| $V_{OUT(OVP)}$ | Output overvoltage protection | $V_{IN}$ = 85-V AC | | 477 | | VDC |
| $V_{OUT(UVP)}$ | Output undervoltage protection | | | 416 | | VDC |
| THD | $V_{INAC}$ = 85 to 305 V, $P_{OUT}$ > 25% of full load | | | < 20 | | % |
| **CONTROL LOOP CHARACTERISTICS** | | | | | | |
| $f_{SW}$ | Switching frequency | $T_J$ = 25°C | | 130 | | kHz |
| $f_{CO}$ | Voltage loop bandwidth | $V_{IN}$ = 162-V DC, $I_{OUT}$ = 0.466 A | | 8 | | Hz |
| | Voltage loop phase margin | $V_{IN}$ = 162-V DC, $I_{OUT}$ = 0.466 A | | 68 | | ° |
| PF | Power factor | $V_{IN}$ = 115-V AC, $I_{OUT} = I_{OUT(max)}$ | | 0.994 | | |
| η | Full load efficiency | $V_{IN}$ = 85-V AC, $f_{LINE}$ = 60 Hz, $I_{OUT} = I_{OUT(max)}$ | | 90 | | % |
| | Ambient temperature | | | 25 | | °C |

#### 2.3.1.1 Current Calculations

The input fuse, bridge rectifier, and input capacitor are selected based upon the input current calculations. First, determine the maximum average output current, $I_{OUT(max)}$:

$$I_{OUT(max)} = \frac{P_{OUT(max)}}{V_{OUT}}$$
$$I_{OUT(max)} = \frac{220\ W}{434\ V} = 0.507\ A \quad (1)$$

The maximum input RMS line current, $I_{IN\_RMS(max)}$, is calculated using the parameters from 表 2 such as the initial assumptions of efficiency and PF:

$$I_{IN\_RMS(max)} = \frac{P_{OUT(max)}}{\eta \times V_{IN(min)} \times PF}$$
$$I_{IN\_RMS(max)} = \frac{220}{0.9 \times 85 \times 0.994} = 2.893\ A \quad (2)$$

Based upon the calculated RMS value and assuming the waveform is sinusoidal, the maximum input current, $I_{IN\ (max)}$, and the maximum average input current, $I_{IN\_AVG(max)}$ can be determined.

$$I_{IN(max)} = \sqrt{2} \times I_{IN\_RMS(max)}$$
$$I_{IN(max)} = \sqrt{2} \times 2.893 = 4.09\ A$$
$$I_{IN\_AVG(max)} = \frac{2 \times I_{IN(max)}}{\pi}$$
$$I_{IN\_AVG(max)} = \frac{2 \times 4.09\ A}{3.14} = 2.60\ A \quad (3)$$

In this reference design, a fuse and bridge rectifier with a 4-A rating is used at the input.

#### 2.3.1.2 Switching Frequency

The UCC28180 switching frequency is user programmable with a single resistor on the FREQ pin (4th pin) to ground. For this reference design, the switching frequency, $f_{SW}$, is chosen to be 130 kHz. 図 10 can be used to select the suitable resistor to program the switching frequency, or the value can be calculated using constant scaling values of $f_{TYP}$ and $R_{TYP}$. In all cases, $f_{TYP}$ is a constant that is equal to 65 kHz, $R_{INT}$ is a constant that is equal to 1 MΩ, and $R_{TYP}$ is a constant that is equal to 32.7 kΩ. Simply applying these to 式 4 yields the appropriate resistor that must be placed between FREQ and GND:

$$R_{FREQ} = \frac{f_{TYP} \times R_{TYP} \times T_{INT}}{(f_{SW} \times R_{INT}) + (R_{TYP} \times f_{SW}) - (R_{TYP} \times f_{TYP})}$$
$$R_{FREQ} = \frac{65\ kHz \times 32.7\ k\Omega \times 1M\Omega}{(130\ kHz \times 1M\Omega) + (32.7\ k\Omega \times 130\ kHz) - (32.7\ k\Omega \times 65\ kHz)} = 16.2\ k\Omega \quad (4)$$

A standard resistor of 16.2 kΩ is used for setting a switching frequency around 130 kHz.

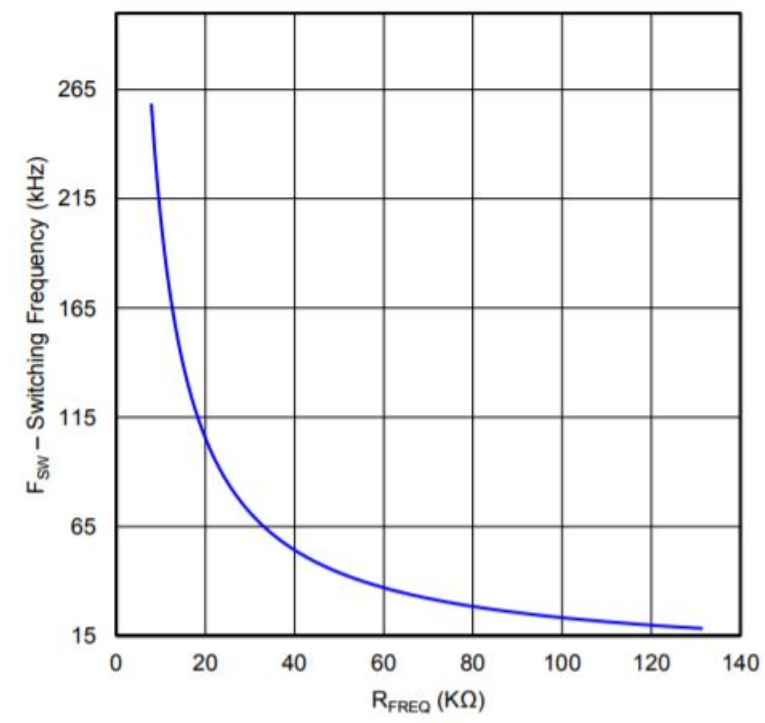



**図 10. Frequency versus $R_{FREQ}$**

#### 2.3.1.3 Bridge Rectifier

The input bridge rectifier must have an average current capability that exceeds the input average current. Assuming a forward voltage drop, $V_{F\_BRIDGE}$, of 1 V across the rectifier diodes, the power loss in the input bridge, $P_{BRIDGE}$, can be calculated as:

$$P_{BRIDGE} = 2 \times V_{F\_BRIDGE} \times I_{IN\_AVG(max)}$$

$$P_{BRIDGE} = 2 \times 1 \times 2.42 = 5.21 \text{ W}$$

Heat sinking is required to maintain operation within the safe operating area of the bridge rectifier.

#### 2.3.1.4 Inductor Ripple Current

The UCC28180 is a CCM controller, but if the chosen inductor allows relatively high-ripple current, the converter is forced to operate in DCM at light loads and at the higher input voltage range. High-inductor ripple current has an impact on the CCM and DCM boundary and results in higher light-load THD, and also affects the choices for the input capacitor, $R_{SENSE}$ and $C_{ICOMP}$ values. Allowing an inductor ripple current, $\Delta I_{RIPPLE}$, of 20% or less results in CCM operation over the majority of the operating range but requires a boost inductor that has a higher inductance value and the inductor itself will be physically large. As with all converter designs, decisions must be made at the onset to optimize performance with size and cost. For this reference design, inductor ripple current is chosen to be 20%.

#### 2.3.1.5 Input Capacitor

The input capacitor must be selected based upon the input ripple current and an acceptable high-frequency input voltage ripple. Allowing an inductor ripple current, $\Delta I_{RIPPLE}$, of 20% and a high-frequency voltage ripple factor, $\Delta V_{RIPPLE\_IN}$, of 7%, the maximum input capacitor value, $C_{IN}$, is calculated by first determining the input ripple current, $I_{RIPPLE}$, and the input voltage ripple, $V_{IN\_RIPPLE}$:

$I_{RIPPLE} = \Delta I_{RIPPLE} \times I_{IN(max)}$

$I_{RIPPLE} = 0.2 \times 4.09 = 0.818$ A

$V_{IN\_RIPPLE} = \Delta V_{RIPPLE\_IN} \times V_{IN\_RECTIFIED(min)}$

where:

- $V_{IN\_RECTIFIED(min)} = \sqrt{2} \times V_{IN(min)} = \sqrt{2} \times 85 = 120$ V
- $V_{IN\_RIPPLE} = 0.07 \times 120 = 8.415$ V

The recommended value for the input x-capacitor can now be calculated using 式 5:

$$C_{IN} = \frac{I_{RIPPLE}}{8 \times f_{SW} \times V_{IN\_RIPPLE}} \tag{5}$$

$$C_{IN} = \frac{0.818}{8 \times 130 \times 8.415} = 0.936\ \mu F$$

Two standard value 0.22-µF and 0.47-µF Y2/X2 film capacitors are used at the input of the PFC stage.

#### 2.3.1.6 Boost Inductor

Based upon the inductor ripple current allowed, the boost inductor, $L_{BST}$, is selected after determining the maximum inductor peak current, $I_{LPEAK}$:

$$I_{LPEAK(max)} = I_{IN(max)} + \frac{I_{RIPPLE}}{2} \tag{6}$$

$$I_{LPEAK(max)} = 4.09 + \frac{0.818}{2} = 4.499\ A$$

The minimum value of the boost inductor is calculated based upon the acceptable ripple current, $I_{RIPPLE}$, at a worst case duty cycle of 0.5:

$$L_{BST(min)} = \frac{V_{OUT} \times D \times (1 - D)}{f_{SW} \times I_{RIPPLE}} \tag{7}$$

$$L_{BST(min)} = \frac{434 \times 0.5 \times 0.5}{130\ kHz \times 0.818} = 1.02\ mH$$

The actual value of the boost inductor that will be used is 1.6 mH. With this actual value used, the actual resultant inductor current ripple will be:

$$I_{RIPPLE} = \frac{V_{OUT} \times D \times (1 - D)}{f_{SW} \times L_{BST}} \tag{8}$$

$$I_{RIPPLE} = \frac{V_{OUT} \times D \times (1 - D)}{f_{SW} \times L_{BST}} = 0.52\ A$$

$$I_{LPEAK(max)} = I_{IN(max)} + \frac{I_{RIPPLE}}{2} = 4.09 + \frac{0.52}{2} = 4.35\ A \tag{9}$$

The duty cycle is a function of the rectified input voltage and will be continuously changing over the half line cycle. The duty cycle, $D_{MAX}$, can be calculated at the peak of the minimum input voltage:

$$D_{MAX} = \frac{V_{OUT} - V_{IN\_RECTIFIED(min)}}{V_{OUT}}$$
$$D_{MAX} = \frac{434 - 120}{434} = 0.723 \quad (10)$$

#### 2.3.1.7 Boost Diode

The diode losses are estimated based upon the forward voltage drop, $V_F$, at 125°C and the reverse recovery charge, $Q_{RR}$, of the diode. Although the silicon carbide diode is more expensive, using this as a schottky diode essentially eliminates the reverse recovery losses and results in less power dissipation:

$$P_{DIODE} = V_{F\_125C} \times I_{OUT(max)} + 0.5 \times f_{SW} \times V_{OUT} \times Q_{RR} \quad (11)$$

where:

- $V_{F\_125C}$ = 1 V
- $Q_{RR}$ = 0 nC
- $P_{DIODE}$ = (1 × 0.507) = 0.507 W

This output diode must have a blocking voltage that exceeds the output overvoltage of the converter and be attached to an appropriately sized heat sink.

#### 2.3.1.8 Boost MOSFET Selection

The MOSFET switch is driven by a gate output that is clamped at 15.2 V for VCC bias voltages greater than 15.2 V. An external gate drive resistor is recommended to limit the rise time and to dampen any ringing caused by the parasitic inductances and capacitances of the gate drive circuit. This external resistor also helps in meeting any EMI requirements of the converter. This design example uses a 10-Ω as gate resistor. To facilitate a fast turnoff, a standard 100-V, 0.2-A Schottky diode is placed anti-parallel with the gate drive resistor. A 20-kΩ resistor is placed between the gate of the MOSFET and ground to discharge the gate capacitance and protect from inadvertent dV/dt triggered turnon.

For this reference design, a MOSFET with 600-V voltage and 13-A current rating is used. The conduction losses of the switch MOSFET in this reference design are estimated using the $R_{DS(on)}$ at 125°C, found in the device data sheet, and the calculated drain-to-source RMS current, $I_{DS\_RMS}$:

$$P_{COND} = I_{DS\_RMS}^2 \times R_{DS(on)125C}$$

where:

- $R_{DS(on)125C}$ = 0.346 Ω

$$I_{DS\_RMS} = \frac{P_{OUT(max)}}{V_{IN\_RECTIFIED(min)}} \times \sqrt{2 - \frac{16 \times V_{IN\_RECTIFIED(min)}}{3\pi \times V_{OUT}}} = \frac{220}{120} \times \sqrt{2 - \frac{16 \times 120}{3\pi \times 2.26\ A}} \quad (12)$$

$$P_{COND} = 2.267^2 \times 0.346 = 1.778\ W$$

The switching losses are estimated using the rise time, $t_r$, and fall time, $t_f$, of the MOSFET gate and the output capacitance losses using 式 13:

$$P_{SW} = f_{SW}\left(0.5 \times V_{OUT} \times I_{IN(max)}\left(t_r + t_f\right) + 0.5 \times C_{OSS} \times V_{OUT}^2\right) \quad (13)$$

where:

- $t_r$ = 7 ns
- $t_f$ = 6 ns

- $C_{OSS}$ = 34 pF

$$P_{SW} = 130\ \text{kHz}\left(0.5 \times 434\ \text{V} \times 4.09 \times (7\ \text{ns} + 6\ \text{ns}) + 0.5 \times 34\ \text{pF} \times 434^2\right) = 1.8\ \text{W} \quad (14)$$

Total FET losses = $P_{COND}$ + $P_{SW}$ = 1.778 + 1.8 W = 3.57 W

The MOSFET requires an appropriately sized heat sink.

#### 2.3.1.9 Sense Resistor

To accommodate the gain of the non-linear power limit, the sense resistor, $R_{SENSE}$, is sized such that it triggers the soft overcurrent at 10% higher than the maximum peak inductor current using the minimum soft overcurrent threshold of the $I_{SENSE}$ pin, $V_{SOC}$, of $I_{SENSE}$ equal to 0.265 V.

$$R_{SENSE} = \frac{V_{SOC(min)}}{I_{L\_PEAK(max)} \times 1.1}$$
$$R_{SENSE} = \frac{0.259}{4.35 \times 1.1} = 0.054\ \Omega \quad (15)$$

The peak current limit, PCL, protection feature is triggered when current through the sense resistor results in the voltage across $R_{SENSE}$ to be equal to the $V_{PCL}$ threshold. For a worst case analysis, the maximum $V_{PCL}$ threshold is used:

$$I_{PCL} = \frac{V_{PCL(max)}}{R_{SENSE}}$$
$$I_{PCL} = \frac{0.438}{0.054} = 8.11\ A \quad (16)$$

To protect the device from inrush current, a standard 221-Ω resistor, $R_{ISENSE}$, is placed in series with the $I_{SENSE}$ pin. A 1000-pF capacitor is placed close to the device to improve noise immunity on the $I_{SENSE}$ pin.

#### 2.3.1.10 Output Capacitor

The output capacitor, $C_{OUT}$, is sized to meet holdup requirements of the converter. Assuming the downstream converters require the output of the PFC stage to never fall below 300 V, $V_{OUT\_HOLDUP(min)}$, during one and half line cycle.

$$t_{HOLDUP} = \frac{0.5}{f_{LINE(min)}} = \frac{0.5}{47} = 10.6\ ms \quad (17)$$

The minimum calculated value for the capacitor is:

$$C_{OUT(min)} \geq \frac{2 \times P_{OUT(max)} \times t_{HOLDUP}}{V^2_{OUT} - V^2_{OUT\_HOLDUP(min)}}$$
$$C_{OUT(min)} \geq \frac{2 \times 220 \times 10.6\ ms}{434^2 - 300^2} \geq 44.7\ \mu F \quad (18)$$

De-rate this capacitor value by 10%; the actual capacitor used is 47 µF.

Verify that the maximum peak-to-peak output ripple voltage will be less than 5% of the output voltage. This ensures that the ripple voltage will not trigger the output overvoltage or output undervoltage protection features of the controller. If the output ripple voltage is greater than 5% of the regulated output voltage, a larger output capacitor is required. The maximum peak-to-peak ripple voltage, occurring at twice the line frequency, and the ripple current of the output capacitor is calculated:

$$V_{OUT\_RIPPLE(pp)} < 0.05 \times V_{OUT}$$
$$V_{OUT\_RIPPLE(pp)} < 0.05 \times 434\ V = 21.7\ V_{PP}$$
$$V_{OUT\_RIPPLE(pp)} = \frac{I_{OUT}}{2\pi \times 2 \times f_{LINE(min)} \times C_{OUT}}$$
$$V_{OUT\_RIPPLE(pp)} = \frac{0.507}{2\pi \times 2 \times 47 \times 47\ \mu F} = 18.27\ V \quad (19)$$

The required ripple current rating at twice the line frequency is equal to 式 20:

$$I_{COUT\_2fline} = \frac{I_{OUT(max)}}{\sqrt{2}}$$
$$I_{COUT\_2fline} = \frac{0.507}{\sqrt{2}} = 0.358\ A \quad (20)$$

There is a high-frequency ripple current through the output capacitor:

$$I_{COUT\_HF} = I_{OUT(max)} \times \sqrt{\frac{16 \times V_{OUT}}{3\pi \times V_{IN\_RECTIFIED(min)}} - 1.5}$$
$$I_{COUT\_HF} = 0.507 \times \sqrt{\frac{16 \times 434}{3\pi \times 120} - 1.5} = 1.09\ A \quad (21)$$

The total ripple current in the output capacitor is the combination of both, and the output capacitor must be selected accordingly:

$$I_{COUT\_RMS(total)} = \sqrt{I^2_{COUT\_2fline} + I^2_{COUT\_HF}}$$
$$I_{COUT\_RMS(total)} = \sqrt{0.358^2 + 1.09^2} = 1.14\ A \quad (22)$$

#### 2.3.1.11 Output Voltage Set Point

For low-power dissipation and minimal contribution to the voltage set point, it is recommended to use 1 MΩ for the top voltage feedback divider resistor, $R_{FB1}$. Multiple resistors in series are used due to the maximum allowable voltage across each. Using the internal 5-V reference, $V_{REF}$, the bottom divider resistor, $R_{FB2}$, is selected to meet the output voltage design goals.

$$R_{FB2} = \frac{V_{REF} \times R_{FB1}}{V_{OUT} - v_{REF}}$$
$$R_{FB2} = \frac{5\ V \times 0.996\ M\Omega}{434 - 5} = 11.6\ k\Omega \quad (23)$$

A standard value 11-kΩ resistor for $R_{FB2}$ results in a nominal output voltage set point of 434 V. A small capacitor on $V_{SENSE}$ must be added to filter out noise. Limit the value of the filter capacitor such that the RC time constant is limited to approximately 10 µs so as not to significantly reduce the control response time to output voltage deviations.

$$C_{VSENSE} = \frac{10\ \mu s}{R_{FB2}} = 909\ pF \quad (24)$$

The closest standard value of 820 pF is used on $V_{SENSE}$ for a time constant of 10.66 µs.

#### 2.3.1.12 Loop Compensation

The voltage error amplifier is compensated with a zero, $f_{ZERO}$, at the $f_{PWM\_PS}$ pole and a pole, $f_{POLE}$, placed at 20 Hz to reject high-frequency noise and roll off the gain amplitude. The overall voltage loop crossover, $f_V$, is desired to be at 10 Hz. The compensation components of the voltage error amplifier are selected accordingly. The design spreadsheet has all relevant equations for characterization of the compensation of the UCC28180 device (see 4.7).

### 2.3.2 Circuit Design of Dual Switch Flyback

The UCC28740 is a quasi-resonant flyback controller that provides CV mode control and CC mode control for precise output regulation. In this design, the controller uses an optocoupler for tight output voltage and current regulation and also for improved transient response to large load steps. The UCC28740 uses frequency modulation, peak primary current modulation, valley switching, and valley hopping in its control algorithm to maximize efficiency over the entire operating range.

**表 3. Design Goal Parameters for Dual Switch Flyback Stage**

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **INPUT** | | | | | |
| $V_{INDC}$ | DC input voltage range (from PFC output) | 300 | | 460 | VAC |
| **OUTPUT** | | | | | |
| $V_{OUT}$ | Output voltage | 199.6 | 200 | 201 | VDC |
| $I_{OUT}$ | Output current | | 1 | 1.1 | ADC |
| $I_{CCC}$ | Output overcurrent | | | 1.1 | ADC |
| $P_{OUT}$ | Output power (max) | | 200 | | W |
| | Line regulation | | | < 1% | |
| | Load regulation | | | < 1% | |
| $f_{MAX}$ | Maximum desired switching frequency | | | 60 | kHz |
| η | Targeted efficiency | | 90% | | |

#### *2.3.2.1 Input Bulk Capacitance and Minimum Bulk Voltage*

Because a PFC front-end is used in this reference design, the PFC output capacitor is the input capacitance for the flyback converter (C = 47 µF).

The minimum voltage operation of flyback is defined by the holdup voltage of the PFC converter during brownout conditions ($V_{HOLD\_UP(min)}$ = 300 V).

Considering a maximum of 20-V ripple voltage on the capacitor:

$V_{BULK(min)} = V_{HOLD\_UP(min)} – 20\ V = 280\ V$

#### *2.3.2.2 Transformer Parameter Calculations: Turns Ratio, Primary Inductance, and Peak Primary Current*

The target maximum switching frequency at full load, the minimum input-capacitor bulk voltage, and the estimated DCM $Q_R$ time determine the maximum primary-to-secondary turns ratio of the transformer. Initially determine the maximum-available total duty cycle of the on-time and secondary conduction time based on the target switching frequency, $f_{MAX}$, and DCM resonant time. For DCM resonant frequency, assume 500 kHz if an estimate from previous designs is not available. At the TM operation limit of DCM, the interval required from the end of secondary current conduction to the first valley of the $V_{DS}$ voltage is ½ of the DCM resonant period ($t_R$), or 1 µs assuming a 500-kHz resonant frequency. The maximum allowable MOSFET on-time $D_{MAX}$ is determined using 式 25.

$$D_{MAX} = 1 - D_{MAGCC} - f_{MAX} - \frac{t_R}{2} \quad (25)$$

where:

- $t_R$ is the estimated period of the LC resonant frequency at the switch node
- $D_{MAGCC}$ is defined as the duty cycle of the secondary-diode conduction during CC operation and is fixed

internally by the UCC28740 at 0.425

$$D_{MAX} = 1 - 0.425 - 60\,kHz \times \frac{2\,\mu s}{2} = 0.51$$

When $D_{MAX}$ is known, the maximum primary-to-secondary turns ratio is determined with 式 26. The total voltage on the secondary winding must be determined, which is the sum of $V_{OCV}$, $V_F$, and $V_{OCBC}$.

$$N_{PS(max)} = \frac{D_{MAX} \times V_{BULK(min)}}{D_{MAGCC} \times (V_{OCV} + V_F + V_{OCBC})} \quad (26)$$

$V_{OCBC}$ is the additional voltage drop of post filter inductor and any other target cable-compensation voltage added to $V_{OCV}$ (provided by an external adjustment circuit applied to the shunt regulator).

Assuming $V_{OCBC}$ = 0 and $V_F$ = 0.6 V:

$$N_{PS(max)} = \frac{0.51 \times 300}{0.425 \times (200 + 0.6)} = 1.794$$

A higher turns ratio generally improves efficiency, but may limit operation at a low input voltage. The transformer turns ratio selected affects the MOSFET $V_{DS}$ and secondary rectifier reverse voltage, so these must be reviewed. The UCC28740 controller requires a minimum on time of the MOSFET ($t_{ON(min)}$) and minimum secondary rectifier conduction time ($t_{DM(min)}$) in the high line and minimum load condition. The selection of $f_{MAX}$, $L_P$, and $R_{CS}$ affects $t_{ON(min)}$ and $t_{DM(min)}$. The secondary rectifier and MOSFET voltage stress can be determined by 式 27.

$$V_{REV} = \frac{V_{IN(max)} \times \sqrt{2}}{N_{PS}} + V_{OCV} + V_{OCBC} \quad (27)$$

For the MOSFET $V_{DS}$ voltage stress, include an estimated leakage inductance voltage spike ($V_{LK}$).

$$V_{DSPK} = \left(V_{IN(max)} \times \sqrt{2}\right) + (V_{OCV} + V_F + V_{OCBC}) \times N_{PS} + V_{LK} \quad (28)$$

式 29 determines if $t_{ON(min)}$ exceeds the minimum $t_{ON}$ target of 280 ns (maximum $t_{CSLEB}$). 式 30 verifies that $t_{DM(min)}$ exceeds the minimum $t_{DM}$ target of 1.2 μs.

$$t_{ON(min)} = \frac{L_P}{V_{IN(max)} \times \sqrt{2}} \times \frac{I_{PP(max)}}{K_{AM}} \quad (29)$$

$$T_{DM(min)} = \frac{t_{ON(min)} \times V_{IN(max)} \times \sqrt{2}}{N_{PS} \times (V_{OCV} + V_F)} \quad (30)$$

To determine the optimum turns ratio, $N_{PS}$, design iterations are generally necessary to optimize and evaluate system-level performance trade-offs and parameters mentioned in 式 27 to 式 30.

When the optimum turns ratio $N_{PS}$ is determined from a detailed transformer design, use this ratio for the following parameters. For this reference design, $N_{PS}$ = 1.5 is selected on optimization.

The UCC28740 CC regulation is achieved by maintaining $D_{MAGCC}$ at the maximum primary peak current setting. The product of $D_{MAGCC}$ and $V_{CST(max)}$ defines a CC-regulating voltage factor, $V_{CCR}$, which is used with $N_{PS}$ to determine the current-sense resistor value necessary to achieve the regulated CC target, $I_{OCC}$ (see 式 31).

$$I_{PP(max)} = \frac{0.81}{0.21} = 3.85 \text{ A} \quad (31)$$

Because a small portion of the energy stored in the transformer does not transfer to the output, a transformer efficiency term is included in 式 31. This efficiency number includes the core and winding losses, the leakage-inductance ratio, and a bias-power to maximum-output-power ratio. For example, an overall transformer efficiency of 0.9 is a good estimate based on 3.5% leakage inductance, 5% core and winding loss, and 0.5% bias power. Adjust these estimates appropriately based on each specific application.

$$I_{PP(nom)} = \frac{0.773}{0.21} = 3.68\ A$$

$V_{CCR(min)}$ is the minimum CC regulation factor and device parameter = 0.33 V. The standard value of current sense resistor selected is $R_{CS}$ = 0.21 Ω. Two parallel resistors to $R_{CS}$ are added in the schematic to adjust values easily.

To calculate primary inductance, first determine the transformer primary peak current using 式 32. Peak primary current is the maximum current-sense threshold divided by the current-sense resistance:

$$I_{PP(max)} = \frac{V_{CST(max)}}{R_{CS}} \tag{32}$$

$$R_{LED\_SNS} = \frac{V_{TH}}{I_{OUT(max)} \times INA_{gain}} = \frac{1}{1 \times 50} = 0.02\ \Omega$$

$$V_{TH} = \frac{V_{OUT} \times R_{FB2}}{R_{FB1} + R_{FB2}} \tag{33}$$

The primary transformer inductance is calculated using the standard energy storage equation for flyback transformers. Primary current, maximum switching frequency, output voltage and current targets, and transformer power losses are included in 式 34:

$$L_P = \frac{2 \times (V_{OCV} + V_F + V_{OCBC}) \times I_{OCC}}{\eta \times FMR \times I^2_{PP(max)} \times f_{MAX}} \tag{34}$$

$$L_P = \frac{2 \times (200 + 0.6) \times 1.1}{0.9 \times 3.85^2 \times 60\ kHz} = 551\ \mu H$$

The actual primary inductance selected is $L_P$ = 600 µH.

$N_{AS}$ is determined by the lowest target operating output voltage while in CC regulation and by the $V_{DD}$ UVLO turnoff threshold of the UCC28740. Additional energy is supplied to $V_{DD}$ from the transformer leakage-inductance, which allows a lower turns ratio to be used in many designs.

$$N_{AS} = \frac{V_{DD(off)} + V_{FA}}{V_{OCC} + V_F} = \frac{8.15 + 0.9}{8.5 + 0.4} = 0.925 \tag{35}$$

#### 2.3.2.3 Transformer Parameter Calculations: Primary and Secondary RMS Currents

With the primary inductance of 600 µH, the absolute maximum switching frequency is calculated from 式 36:

$$f_{MAX} = \frac{2 \times (200 + 0.6) \times 1.1}{0.9 \times 3.85^2 \times 600\ \mu H} = 55.1\ kHz \tag{36}$$

The maximum switching period is:

$$t_{SW} = \frac{1}{f_{MAX}} = \frac{1}{55.1\ kHz} = 18.14\ \mu s \tag{37}$$

The actual maximum on-time is given by 式 38:

$$t_{ON(max)} = \frac{I_{PP(nom)} \times L_P}{V_{BULK(min)}} = \frac{3.68 \times 600\ \mu H}{300} = 7.36\ \mu s \quad (38)$$

The maximum duty cycle of operation ($D_{MAX}$) is:

$$D_{MAX} = \frac{t_{ON(max)}}{t_{SW}} = \frac{7.36\ \mu s}{18.14\ \mu s} = 0.405 \quad (39)$$

The transformer primary RMS current ($I_{PRMS}$) is:

$$I_{PRMS} = I_{PP(nom)} \sqrt{\frac{D_{MAX}}{3}} = 3.68 \times \sqrt{\frac{0.405}{3}} = 1.35\ A \quad (40)$$

The transformer secondary peak current RMS current ($I_{SEC(max)}$) is:

$I_{SEC(max)} = I_{PP(max)} \times N_{PS} = 3.85 \times 1.5 = 5.77$ A

The transformer secondary RMS current ($I_{SEC\_RMS}$) is:

$$I_{SEC\_RMS} = I_{SEC(max)} \sqrt{\frac{D_{MAX}}{3}} = 5.77 \times \sqrt{\frac{0.425}{3}} = 2.17 \text{ A} \quad (41)$$

Based on these calculations, a Minntronix transformer was designed for this application (part number 4815839), which has the following specifications:

- $N_{PS}$ = 1.5
- $N_{PA}$ = 15
- $L_P$ = 600 µH
- $L_{LK}$ = 3.5 µH (which denotes the primary leakage inductance)

#### 2.3.2.4 Main Switching Power MOSFET Selection

The drain-to-source RMS current, $I_{DS\_RMS}$, through switching FET is calculated using 式 42:

$$I_{DS\_RMS} = I_{PP(max)} \times \sqrt{\frac{D_{MAX}}{3}} = 3.85 \times \sqrt{\frac{0.405}{3}} = 1.41 \text{ A} \quad (42)$$

Select a MOSFET with five times the $I_{DS\_RMS}$ calculated. The maximum voltage across the FET can be estimated using 式 28. Considering a de-rating of 25% and leakage spike of around 250 V, the voltage rating of the MOSFET in a dual switch flyback must be around 1200-V DC. Two STF18N65M2 MOSFETs of 650 V and 11 A at 25°C / 8 A at 100°C are selected for this reference design.

#### 2.3.2.5 Rectifying Diode Selection

Calculate the secondary output diode or synchronous rectifier FET reverse voltage or blocking voltage needed ($V_{DIODE\_BLOCKING}$):

$$V_{DIODE\_BLOCKING} = \frac{V_{IN\_DC(max)}}{N_{PS}} + V_{OUT\_OVP} + V_{OCBC} \quad (43)$$

$$V_{DIODE\_BLOCKING} = \frac{460}{1.5} + 200 = 506.6 \text{ V}$$

The required minimum average rectified output current is:

$I_{DOUT} = I_{SEC\_RMS} = 2.17$ A

A silicon carbide Schottky diode is recommended for low power loss and high-efficiency needs. For this reference design, the silicon carbide Schottky diode (C3D04060A) with a 600-V voltage and 4-A forward current rating is selected to optimize the on-state losses.

#### 2.3.2.6 Output Capacitor Selection

For this reference design, the output capacitor ($C_{OUT}$) for output is selected to prevent $V_{OUT}$ (= 200 V) from dropping below the minimum output voltage ($V_{OTRM}$) during transients up to 0.36 V and ripple voltage less than 100 mV.

$$C_{OUT} \geq \frac{\frac{I_{OUT}}{2} \times (t)}{V_{OUT} - V_{OTRM}} \tag{44}$$

where:

- $V_{OTRM}$ = 199.64 V

$$C_{OUT} \geq \frac{\frac{1.1}{2} \times (3.33\ \mu s)}{200 - 199.64} \geq 50.8\ \mu F$$

Considering the allowable output ripple voltage of 120 mV (5%), the ESR of the capacitor must be:

$$ESR = \frac{V_{OUT\_RIPPLE}}{I_{SEC(max)}} = \frac{120\ mV}{5.77\ A} = 20.7\ m\Omega \tag{45}$$

$$I_{COUT\_RMS} = \sqrt{\left(I_{SEC\_RMS}\right)^2 - \left(I_{OUT}\right)^2} = \sqrt{(2.17)^2 - (1.1)^2} = 1.87\ A \tag{46}$$

Two 47-µF, 250-V capacitors are selected for the output.

#### 2.3.2.7 Capacitance on VDD Pin

The capacitance on VDD needs to supply the device operating current until the output of the converter reaches the target minimum operating voltage in CC regulation.

The capacitance on VDD must supply the primary-side operating current used during startup and between low-frequency switching pulses. The largest result of two independent calculations denoted in 式 47 determines the value of $C_{VDD}$.

At start-up, when $V_{VDD(on)}$ is reached, $C_{VDD}$ alone supplies the device operating current and MOSFET gate current until the output of the converter reaches the target minimum operating voltage in CC regulation, $V_{OCC}$. Now the auxiliary winding sustains VDD for the UCC28740 above UVLO. The total output current available to the load and to charge the output capacitors is the CC-regulation target, $I_{OCC}$. 式 47 assumes that all of the output current of the converter is available to charge the output capacitance until $V_{OCC}$ is achieved. For typical applications, 式 47 includes an estimated $q_G \times f_{SW(max)}$ of average gate drive current and a 1-V margin added to $V_{VDD}$.

$$C_{VDD} \geq \frac{\left(I_{RUN} + q_G \times f_{SW(max)}\right) \times \frac{C_{OUT} \times V_{OCC}}{I_{OCC}}}{V_{DD(on)} - \left(V_{DD(off)} + 1\,V\right)} \tag{47}$$

$$C_{VDD} \geq \frac{\left(2\ mA + 9.9\ nC \times 60\ kHz\right) \times \frac{94\ \mu F \times 201\,V}{1.1}}{21 - \left(8.5 + 1\,V\right)} \geq 3.87\ \mu F$$

During a worst-case un-load transient event from full load to no load, $C_{OUT}$ overcharges above the normal regulation level for a duration of $t_{OV}$ until the output shunt regulator loading is able to drain $V_{OUT}$ back to regulation. During $t_{OV}$, the voltage feedback loop and optocoupler are saturated, driving maximum $I_{FB}$ and temporarily switching at $f_{SW(min)}$. The auxiliary bias current expended during this situation exceeds that normally required during the steady-state no-load condition.

The current design uses 10-µF and 2.2-µF capacitors.

#### 2.3.2.8 Open-Loop Voltage Regulation versus Pin Resistor Divider, Line Compensation Resistor

The resistor divider at the $V_S$ pin determines the output voltage regulation point of the flyback converter. Also, the high-side divider resistor ($R_{S1}$) determines the line voltage at which the controller enables continuous DRV operation. $R_{S1}$ is initially determined based on transformer auxiliary-to-primary turns ratio and desired input voltage operating threshold.

$$R_{S1} = \frac{V_{IN(run)} \times \sqrt{2}}{N_{PA} \times I_{VSL(min)}} \tag{48}$$

where:

- $N_{PA}$ is the transformer primary-to-auxiliary turns ratio
- $V_{IN(run)}$ is the AC RMS voltage to enable turnon of the controller (run); in case of DC input, leave out the $\sqrt{2}$ term in the equation
- $I_{VSL(run)}$ is the run threshold for the current pulled out of the VS pin during the switch on-time (see the Electrical Characteristics section of the UCC28740 data sheet)

$$R_{S1} = \frac{390\ V}{15 \times 275\ \mu A} = 110\ k\Omega$$

A standard resistor of 110 kΩ is selected.

The low-side VS pin resistor is selected based on the desired $V_{OUT}$ regulation voltage in open-loop conditions and sets maximum allowable voltage during open-loop conditions.

$$R_{S2} = \frac{R_{S1} \times V_{OVPTH}}{N_{AS} \times (V_{OV} - V_F) - V_{OVPTH}} \tag{49}$$

where:

- $V_{OV}$ is the maximum allowable peak voltage at the converter output
- $V_F$ is the output-rectifier forward drop at near-zero current
- $N_{AS}$ is the transformer auxiliary-to-secondary turns ratio
- $R_{S1}$ is the VS divider high-side resistance
- $V_{OVPTH}$ is the overvoltage detection threshold at the VS input (see the Electrical Characteristics section of the UCC28740 data sheet)

$$R_{S2} = \frac{110\ k\Omega \times 4.6}{0.1 \times (201 - 0.6) - 4.6} = 32.77\ k\Omega$$

A standard resistor of 33.2 kΩ is selected.

The UCC28740 maintains tight CC regulation over varying input line by using the line-compensation feature. The line-compensation resistor ($R_{LC}$) value is determined by current flowing in $R_{S1}$ and the total internal gate drive and external MOSFET turnoff delay. Assuming an internal delay of 50 ns in the UCC28740:

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times t_D \times N_{PA}}{L_P} \tag{50}$$

where:

- $R_{CS}$ is the current-sense resistor value

- $t_D$ is the current-sense delay including MOSFET turnoff delay
- $N_{PA}$ is the transformer primary-to-auxiliary turns ratio
- $L_P$ is the transformer primary inductance
- $K_{LC}$ is a current-scaling constant (see the Electrical Characteristics section of the UCC28740 data sheet)

$$R_{LC} = \frac{25 \times 71.5\ k\Omega \times 0.21 \times 46\ ns \times 15}{600\ \mu H} = 720\ \Omega$$

A standard resistor of 590 Ω is selected.

#### 2.3.2.9 Feedback Elements

In this reference design, the secondary side CC-CV control is implemented using two op amps where LED current regulation is achieved using the INA180, which is used for sensing output LED current through sensing voltage across sense resistor. Output voltage regulation is achieved using feedback based on the resistor divider (R221, R223, and R225). The value of the LED current sensing resistor can be calculated using 式 51 based on INA180 gain (50 V/V), reference voltage setting (1 V), and full-load LED current (1 A).

$$R_{LED\_SNS} = \frac{V_{TH}}{I_{OUT(max)} \times INA_{GAIN}} = \frac{1}{1 \times 50} = 0.02\ \Omega \quad (51)$$

The output voltage is set through the sense network resistors $R_{FB1}$ and $R_{FB2}$. The value of feedback resistor can be chosen based on desired output voltage by 式 52.

$$V_{TH} = \frac{V_{OUT} \times R_{FB2}}{R_{FB1} + R_{FB2}} \quad (52)$$

where:

- $V_{TH}$ = 1 V

Assuming $R_{FB1}$ = 224 kΩ and setting $V_{OUT}$ = 200 V, the value of $R_{FB2}$ as calculated per 式 52 is 1.23 kΩ.

The op amp compensation network, $Z_{FB}$, is determined using well-established design techniques for control-loop stability. Typically, a type-II compensation network is used.

# 3 Hardware, Testing Requirements, and Test Results

## 3.1 Required Hardware

- Isolated AC source (0- to 305-V AC / 3 A)
- Single-phase power analyzer
- DC power supply (0- to 10-V DC / 0.3 A)
- Digital oscilloscope
- Digital multimeter
- High-wattage LED load

## 3.2 Testing and Results

### 3.2.1 Test Setup

#### 3.2.1.1 Test Conditions

- Input voltage range: The AC source must be capable of varying a $V_{INAC}$ between 85- and 305-V AC. Set input current limit to 3 A.
- Output: Connect an LED load capable of 200 V and a load variable in range from 0 to 1 A.
- External DC input voltage: External DC signal up to 10 V is required to turn on or off the PFC stage in the power supply reference design.

#### 3.2.1.2 Test Procedure

図 11 shows the flow followed to test the reference design PCB and perform 0- to 10-V dimming.

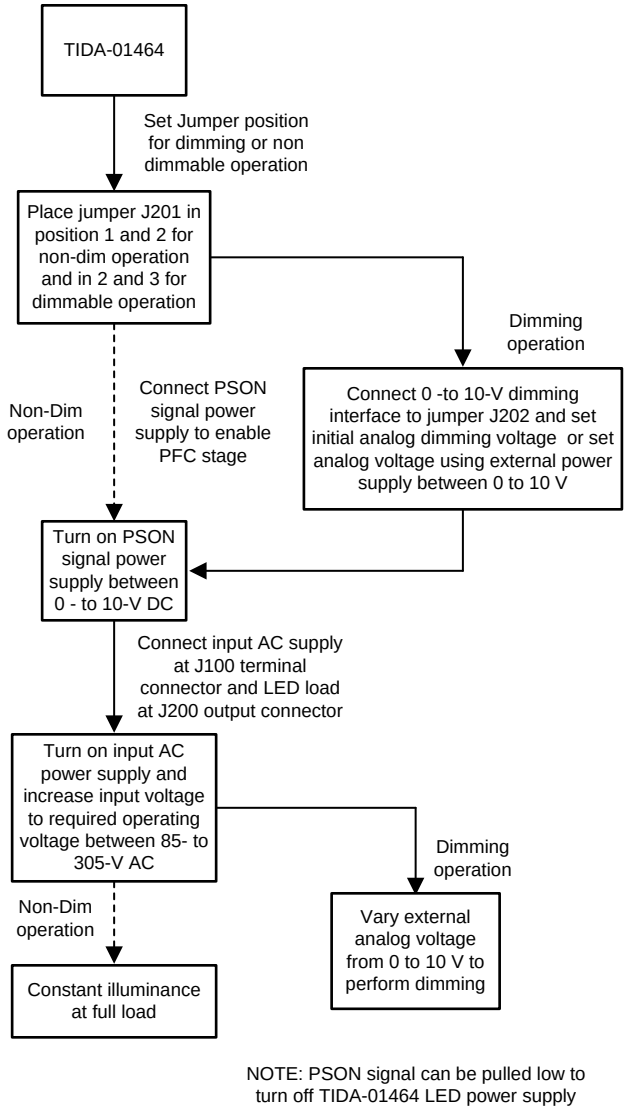





**図 11. Test Flow for TIDA-01464**

### 3.2.2 Test Results

The test results are divided into multiple sections that cover the steady state performance measurements, current harmonics measurements, functional performance waveforms and test data, transient performance waveforms, and thermal measurements.

#### *3.2.2.1 Performance Data With 196-V and 102-V LED Loads With Input Line Voltage Variation at Full Load*

**表 4. Test Data With 102-V LED Load at Full Load**

| $V_{IN}$ (V) | FREQ (Hz) | $V_{RMS}$ (V) | $I_{RMS}$ (A) | $P_{IN}$ (W) | PF | $A_{THD}$ | $V_{OUT}$ (V) | $I_{LED}$ (A) | $P_{OUT}$ (W) | EFFICIENCY |
|---|---|---|---|---|---|---|---|---|---|---|
| 85 | 50 | 84.07 | 1.39 | 116.9 | 0.998 | 3.36% | 102 | 1 | 102 | 87.25% |
| 100 | 50 | 109.09 | 1.06 | 115.8 | 0.997 | 3.40% | 102 | 1 | 102 | 88.08% |
| 120 | 50 | 120 | 0.964 | 114.9 | 0.997 | 3.60% | 102 | 1 | 102 | 88.77% |
| 180 | 50 | 179.5 | 0.636 | 112.8 | 0.989 | 4.31% | 102 | 1 | 102 | 90.43% |
| 230 | 50 | 230.05 | 0.502 | 113.2 | 0.976 | 4.47% | 102.1 | 1.01 | 103.121 | 91.10% |
| 265 | 50 | 265.61 | 0.443 | 112.7 | 0.963 | 4.53% | 102.2 | 1.01 | 103.222 | 91.59% |

**表 5. Test Data With 196-V LED Load at Full Load**

| $V_{IN}$ (V) | FREQ (Hz) | $V_{RMS}$ (V) | $I_{RMS}$ (A) | $P_{IN}$ (W) | PF | $A_{THD}$ | $V_{OUT}$ (V) | $I_{LED}$ (A) | $P_{OUT}$ (W) | EFFICIENCY |
|---|---|---|---|---|---|---|---|---|---|---|
| 85 | 50 | 83.92 | 2.69 | 225.2 | 0.995 | 11.18% | 195.9 | 1 | 195.9 | 86.99% |
| 100 | 50 | 98.9 | 2.23 | 220.8 | 0.997 | 7.20% | 196 | 1 | 196 | 88.77% |
| 120 | 50 | 118.97 | 1.86 | 218.5 | 0.998 | 4.30% | 196 | 1 | 196 | 89.70% |
| 180 | 50 | 179.5 | 1.19 | 214.8 | 0.995 | 3.50% | 196 | 1 | 196 | 91.25% |
| 230 | 50 | 230.1 | 0.936 | 213.2 | 0.991 | 3.80% | 196 | 1 | 196 | 91.93% |
| 265 | 50 | 265 | 0.811 | 212.5 | 0.986 | 3.90% | 196.2 | 1 | 196.2 | 92.33% |

#### *3.2.2.1.1 Functional Performance Graphs With Input Line Voltage Variation at Full Load*

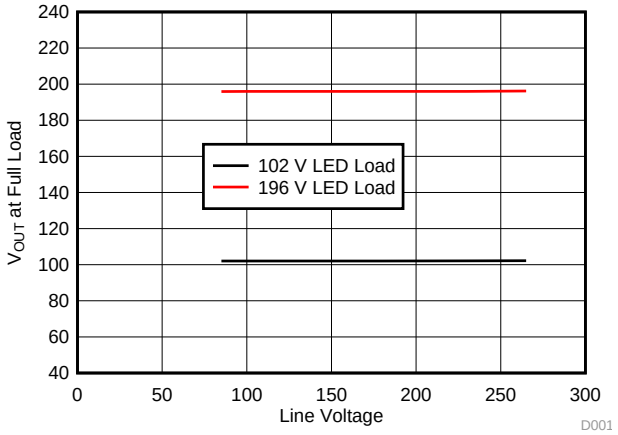



**図 12. Line Voltage versus $V_{OUT}$ at Full Load**

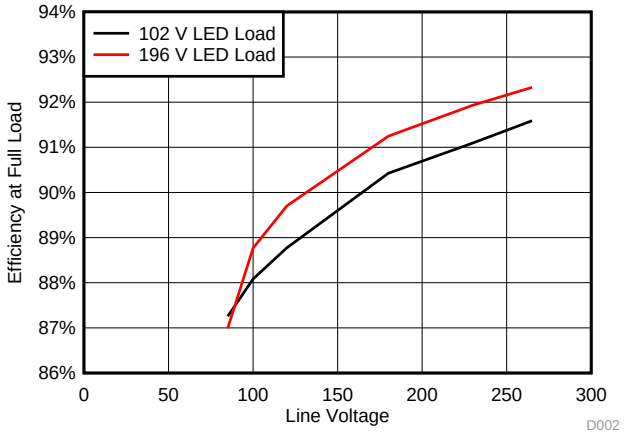



**図 13. Line Voltage versus Efficiency at Full Load**

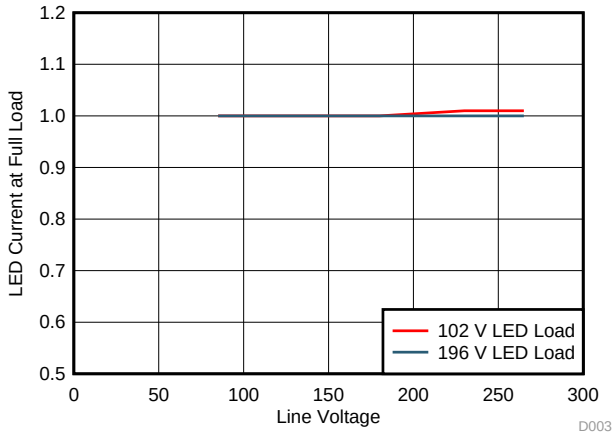



図 14. Line Voltage versus LED Current at Full Load

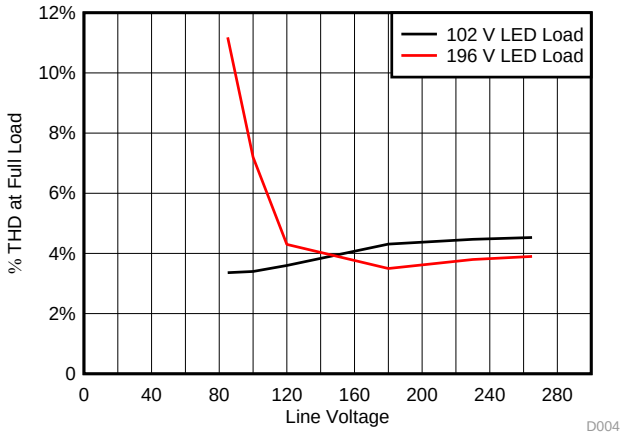



図 15. Line Voltage versus THD at Full Load

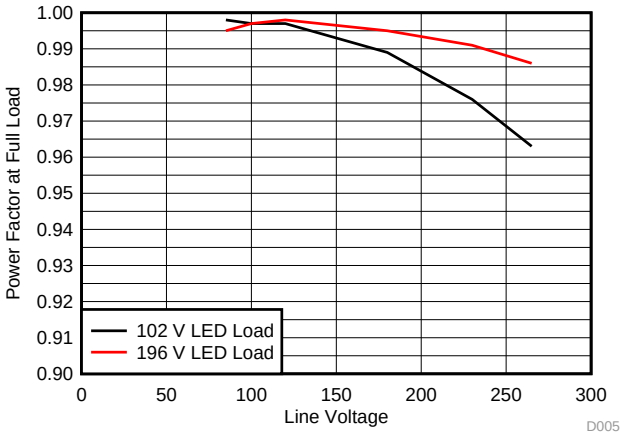



図 16. Line Voltage versus Power Factor at Full Load

### 3.2.2.2 Dimming Data for 196-V and 102-V LED Loads

#### 3.2.2.2.1 Dimming Data With 196-V LED Load at Different Operating Line Voltages

表 6. Performance Data With Dimming at 120-V/50-Hz Input AC Voltage

| $I_{ADJ}$ (V) | $I_{RMS}$ (A) | $P_{IN}$ (W) | PF | $A_{THD}$ | $V_{OUT}$ (V) | $I_{OUT}$ (A) | $P_{OUT}$ (W) | EFFICIENCY |
|---|---|---|---|---|---|---|---|---|
| 10 | 1.848 | 218.5 | 0.997 | 4.26 | 196 | 1 | 196 | 89.70% |
| 9 | 1.62 | 192.6 | 0.997 | 3.69 | 193.9 | 0.891 | 172.7649 | 89.70% |
| 8 | 1.425 | 169.3 | 0.997 | 3.36 | 192.3 | 0.79 | 151.917 | 89.73% |
| 7 | 1.236 | 146.8 | 0.997 | 3.26 | 190.6 | 0.691 | 131.7046 | 89.72% |
| 6 | 1.05 | 125.1 | 0.997 | 3.45 | 188.7 | 0.594 | 112.0878 | 89.60% |
| 5 | 0.874 | 103.8 | 0.996 | 4.03 | 186.7 | 0.496 | 92.6032 | 89.21% |
| 4 | 0.698 | 82.9 | 0.995 | 4.8 | 184.2 | 0.399 | 73.4958 | 88.66% |
| 3 | 0.525 | 62.25 | 0.991 | 6.87 | 181.1 | 0.301 | 54.5111 | 87.57% |
| 2 | 0.356 | 41.9 | 0.983 | 9.87 | 176.8 | 0.202 | 35.7136 | 85.24% |
| 1 | 0.193 | 21.96 | 0.951 | 15.88 | 170.7 | 0.101 | 17.2407 | 78.51% |
| 0.8 | 0.158 | 17.74 | 0.935 | 16 | 169.1 | 0.081 | 13.6971 | 77.21% |

**表 7. Performance Data With Dimming at 230-V/50-Hz Input AC Voltage**

| $I_{ADJ}$ (V) | $I_{RMS}$ (mA) | $P_{IN}$ (W) | PF | $A_{THD}$ | $V_{OUT}$ (V) | $I_{OUT}$ (A) | $P_{OUT}$ (W) | EFFICIENCY |
|---|---|---|---|---|---|---|---|---|
| 10 | 937.8 | 213.2 | 0.99 | 3.87 | 196 | 1 | 196 | 91.93% |
| 9 | 826.4 | 187.9 | 0.989 | 3.76 | 194.1 | 0.889 | 172.5549 | 91.83% |
| 8 | 729.2 | 165.5 | 0.987 | 3.76 | 192.5 | 0.789 | 151.8825 | 91.77% |
| 7 | 635.9 | 143.9 | 0.984 | 3.92 | 190.8 | 0.691 | 131.8428 | 91.62% |
| 6 | 545.4 | 122.9 | 0.979 | 4.29 | 189 | 0.593 | 112.077 | 91.19% |
| 5 | 456.6 | 102.2 | 0.972 | 4.86 | 186.9 | 0.496 | 92.7024 | 90.71% |
| 4 | 369.9 | 81.76 | 0.96 | 5.86 | 184.4 | 0.399 | 73.5756 | 89.99% |
| 3 | 284.2 | 61.42 | 0.935 | 7.22 | 181.2 | 0.301 | 54.5412 | 88.80% |
| 2 | 198.8 | 41.8 | 0.891 | 11.36 | 177.1 | 0.203 | 35.9513 | 86.01% |
| 1 | 126.1 | 21.3 | 0.733 | 20.5 | 170.9 | 0.101 | 17.2609 | 81.04% |
| 0.8 | 109.1 | 17.33 | 0.689 | 20.75 | 169.2 | 0.081 | 13.7052 | 79.08% |

**表 8. Performance Data With Dimming at 265-V/50-Hz Input AC Voltage**

| $I_{ADJ}$ (V) | $I_{RMS}$ (mA) | $P_{IN}$ (W) | PF | $A_{THD}$ | $V_{OUT}$ (V) | $I_{OUT}$ (A) | $P_{OUT}$ (W) | EFFICIENCY |
|---|---|---|---|---|---|---|---|---|
| 10 | 802.2 | 212.5 | 0.985 | 3.96 | 196.2 | 1 | 196.2 | 92.33% |
| 9 | 711.2 | 185.6 | 0.982 | 3.85 | 193.5 | 0.885 | 171.2475 | 92.27% |
| 8 | 629.6 | 163.7 | 0.979 | 3.86 | 191.9 | 0.786 | 150.8334 | 92.14% |
| 7 | 550.8 | 142.5 | 0.974 | 4.02 | 190.2 | 0.689 | 131.0478 | 91.96% |
| 6 | 474 | 121.8 | 0.966 | 4.36 | 188.4 | 0.592 | 111.5328 | 91.57% |
| 5 | 399.2 | 101.3 | 0.955 | 4.97 | 186.4 | 0.495 | 92.268 | 91.08% |
| 4 | 326.1 | 81 | 0.935 | 5.7 | 183.9 | 0.398 | 73.1922 | 90.36% |
| 3 | 252.5 | 60.7 | 0.904 | 8.77 | 180.9 | 0.301 | 54.4509 | 89.70% |
| 2 | 182.8 | 40.4 | 0.832 | 16.24 | 176.6 | 0.202 | 35.6732 | 88.30% |
| 1 | 118.3 | 20.8 | 0.665 | 23.4 | 170.4 | 0.101 | 17.2104 | 82.74% |
| 0.8 | 106.6 | 17.1 | 0.604 | 28.4 | 168.8 | 0.081 | 13.6728 | 79.96% |

#### *3.2.2.2.1.1 Performance Graphs With 196-V LED Load*

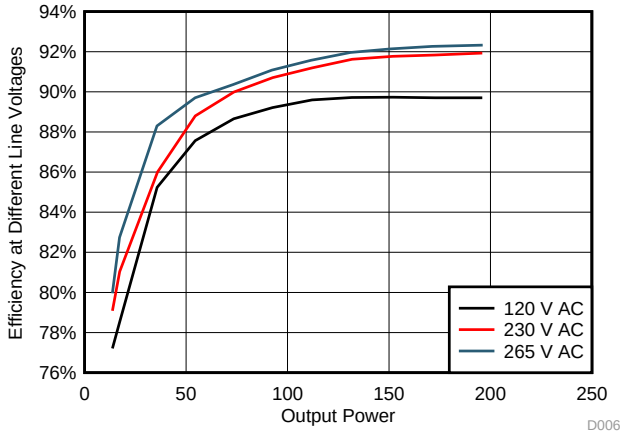



**図 17. Output Power versus Efficiency at Different Line Voltages**

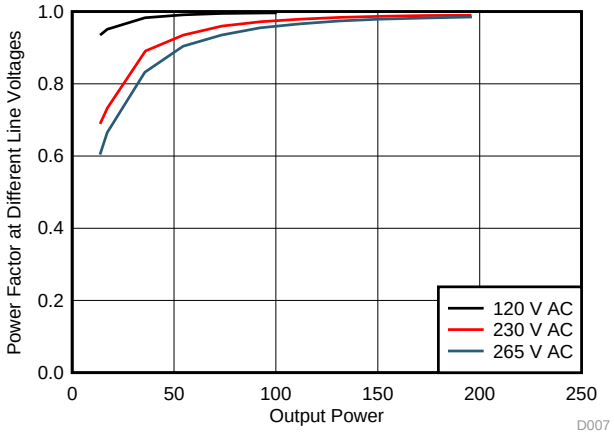



**図 18. Output Power versus Power Factor at Different Line Voltages**

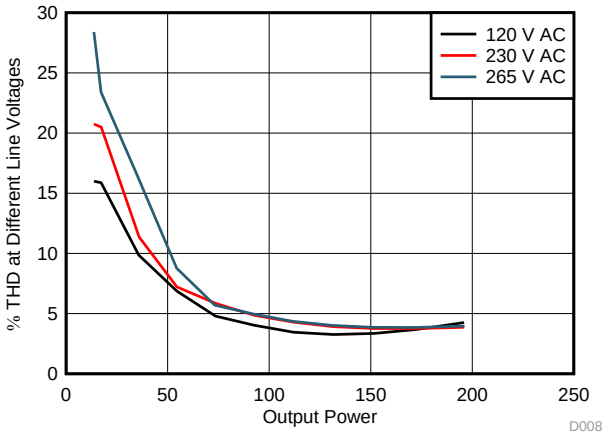



**図 19. Output Power versus THD at Different Line Voltages**

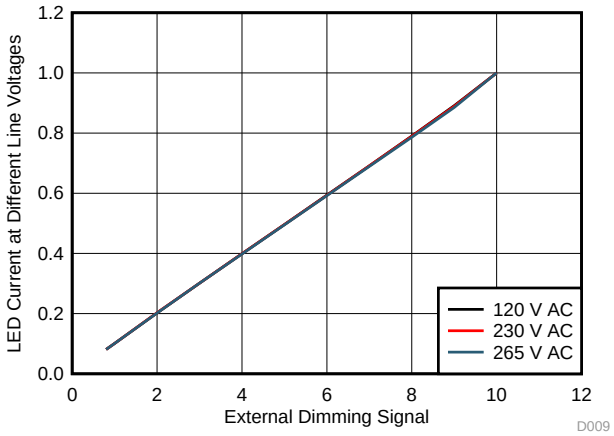



**図 20. External Dimming Signal versus LED Current at Different Line Voltages**

#### *3.2.2.2.2 Dimming Data With 102-V LED Load at Different Operating Line Voltages*

**表 9. Performance Data With Dimming at 120-V/50-Hz Input AC Voltage**

| $I_{ADJ}$ (V) | $I_{RMS}$ (mA) | $P_{IN}$ (W) | PF | $A_{THD}$ | $V_{OUT}$ (V) | $I_{OUT}$ (A) | $P_{OUT}$ (W) | EFFICIENCY |
|---|---|---|---|---|---|---|---|---|
| 10 | 964 | 114.9 | 0.997 | 3.60% | 102 | 1 | 102 | 88.77% |
| 9 | 857.6 | 101.8 | 0.996 | 4.02% | 101.3 | 0.891 | 90.2583 | 88.66% |
| 8 | 753.4 | 89.4 | 0.995 | 4.61% | 100.4 | 0.785 | 78.814 | 88.16% |
| 7 | 655.7 | 77.7 | 0.994 | 5.35% | 99.5 | 0.686 | 68.257 | 87.85% |
| 6 | 561.8 | 66.5 | 0.992 | 6.32% | 98.6 | 0.59 | 58.174 | 87.48% |
| 5 | 470.6 | 55.5 | 0.989 | 7.59% | 97.6 | 0.494 | 48.2144 | 86.87% |
| 4 | 380.9 | 44.7 | 0.985 | 9.23% | 96.4 | 0.398 | 38.3672 | 85.83% |
| 3 | 292.7 | 34.1 | 0.976 | 11.50% | 95.08 | 0.301 | 28.61908 | 83.93% |
| 2 | 205.4 | 23.4 | 0.956 | 15.10% | 93.24 | 0.203 | 18.92772 | 80.89% |
| 1 | 104.6 | 12.4 | 0.913 | 18.70% | 90.62 | 0.101 | 9.15262 | 73.81% |
| 0.8 | 91 | 9.6 | 0.888 | 20.18% | 89.9 | 0.082 | 7.3718 | 76.79% |

**表 10. Performance Data With Dimming at 230-V/50-Hz Input AC Voltage**

| $I_{ADJ}$ (V) | $I_{RMS}$ (mA) | $P_{IN}$ (W) | PF | $A_{THD}$ | $V_{OUT}$ (V) | $I_{OUT}$ (A) | $P_{OUT}$ (W) | EFFICIENCY |
|---|---|---|---|---|---|---|---|---|
| 10 | 502 | 113.2 | 0.976 | 4.47% | 102.1 | 1.01 | 103.121 | 91.10% |
| 9 | 449.5 | 100.5 | 0.971 | 4.88% | 101.4 | 0.893 | 90.5502 | 90.10% |
| 8 | 397.4 | 88.2 | 0.965 | 5.47% | 100.5 | 0.786 | 78.993 | 89.56% |
| 7 | 348.8 | 76.7 | 0.955 | 6.04% | 99.6 | 0.686 | 68.3256 | 89.08% |
| 6 | 302.3 | 65.6 | 0.942 | 6.85% | 98.6 | 0.589 | 58.0754 | 88.53% |
| 5 | 257.5 | 54.6 | 0.922 | 7.17% | 97.6 | 0.494 | 48.2144 | 88.30% |
| 4 | 210.9 | 43.6 | 0.899 | 9.69% | 96.5 | 0.397 | 38.3105 | 87.87% |
| 3 | 166.4 | 32.6 | 0.851 | 15.50% | 95.1 | 0.301 | 28.6251 | 87.81% |
| 2 | 131 | 22.6 | 0.752 | 20.20% | 93.28 | 0.203 | 18.93584 | 83.79% |
| 1 | 89.7 | 11.8 | 0.573 | 25.20% | 90.6 | 0.101 | 9.1506 | 77.55% |
| 0.8 | 79.4 | 9.7 | 0.531 | 31.80% | 89.96 | 0.081 | 7.28676 | 75.12% |

**表 11. Performance Data With Dimming at 265-V/50-Hz Input AC Voltage**

| $I_{ADJ}$ (V) | $I_{RMS}$ (mA) | $P_{IN}$ (W) | PF | $A_{THD}$ | $V_{OUT}$ (V) | $I_{OUT}$ (A) | $P_{OUT}$ (W) | EFFICIENCY |
|---|---|---|---|---|---|---|---|---|
| 10 | 443 | 112.7 | 0.963 | 4.53% | 102.2 | 1.01 | 103.222 | 91.59% |
| 9 | 397 | 100.68 | 0.954 | 4.97% | 101.2 | 0.897 | 90.7764 | 90.16% |
| 8 | 348 | 87.33 | 0.942 | 5.49% | 100.2 | 0.783 | 78.4566 | 89.84% |
| 7 | 308.1 | 75.9 | 0.927 | 5.85% | 99.39 | 0.685 | 68.08215 | 89.70% |
| 6 | 268 | 64.8 | 0.91 | 6.69% | 98.47 | 0.588 | 57.90036 | 89.35% |
| 5 | 228.5 | 53.9 | 0.888 | 9.68% | 97.48 | 0.493 | 48.05764 | 89.16% |
| 4 | 191.5 | 43.2 | 0.849 | 16.60% | 96.34 | 0.397 | 38.24698 | 88.53% |
| 3 | 160 | 32.9 | 0.775 | 20.80% | 95 | 0.301 | 28.595 | 86.91% |
| 2 | 123.7 | 22.5 | 0.684 | 25.40% | 93.2 | 0.203 | 18.9196 | 84.09% |
| 1 | 89.1 | 11.6 | 0.494 | 38.60% | 90.57 | 0.101 | 9.14757 | 78.86% |
| 0.8 | 84 | 9.5 | 0.425 | 45.00% | 89.89 | 0.081 | 7.28109 | 76.64% |

#### *3.2.2.2.2.1 Performance Graphs With 102-V LED Load*

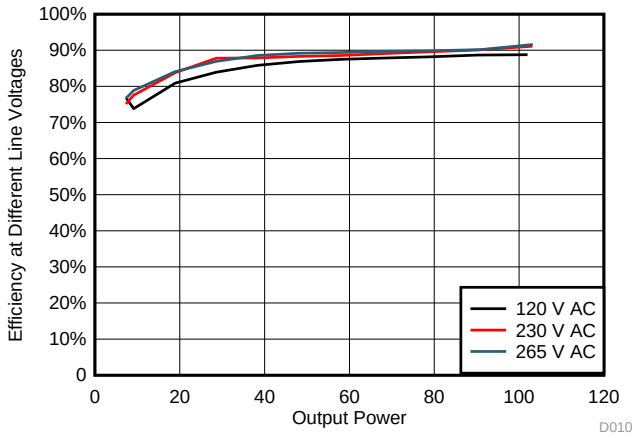



**図 21. Output Power versus Efficiency at Different Line Voltages**

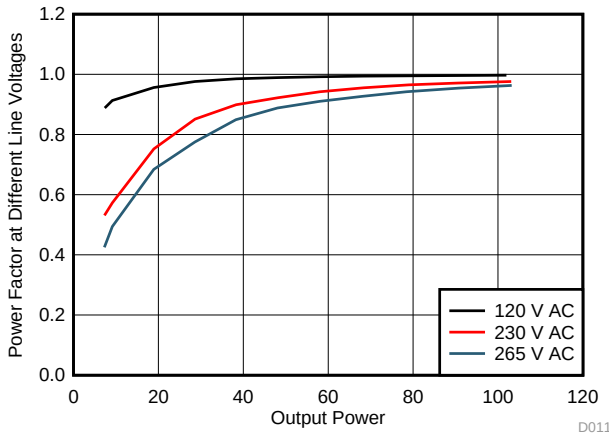



**図 22. Output Power versus Power Factor at Different Line Voltages**

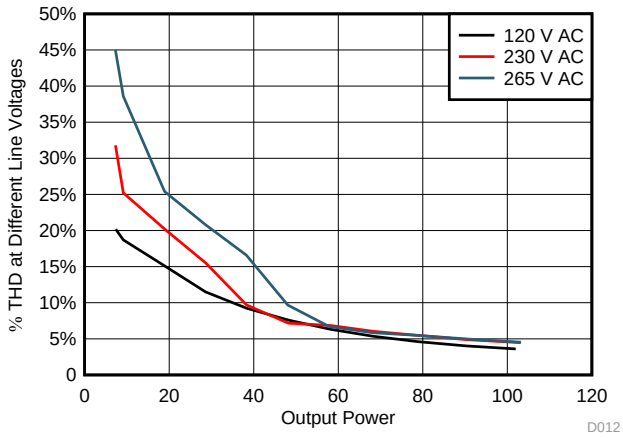



**図 23. Output Power versus THD at Different Line Voltages**

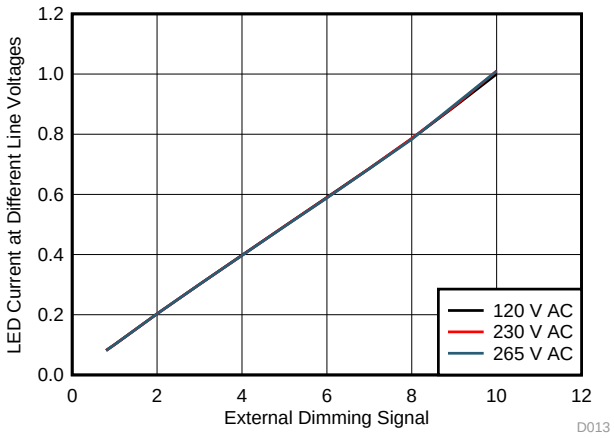



**図 24. External Dimming Signal versus LED Current at Different Line Voltages**

### 3.2.2.3 Input Harmonic Currents Tested as per IEC 6100-3-2

**表 12. EN 61000-3-2 Class C Limits for System Power > 25 W**

| HARMONICS ORDER n | MAXIMUM VALUE EXPRESSED AS A PERCENTAGE OF THE FUNDAMENTAL INPUT CURRENT |
|---|---|
| 2 | < 2% |
| 3 | < 30 λ%(1) |
| 5 | 10% |
| 7 | < 7% |
| 9 | < 5% |
| 11 ≤ n ≤ 39 | < 3% |

(1) λ = Power factor

#### 3.2.2.3.1 Input Current Harmonics Tested at 22% Load With 196-V LED Load

**表 13. Test Conditions for 22% Load With 196-V LED Load**

| $I_{ADJ}$ (V) | $V_{IN}$ (V) | FREQ (Hz) | $I_{IN}$ (mA) | $P_{IN}$ (W) | PF | $A_{THD}$ | $P_{OUT}$ (W) |
|---|---|---|---|---|---|---|---|
| 2.2 | 230 | 50 | 216.79 | 45.043 | 0.902 | 8.10% | 39.54 |

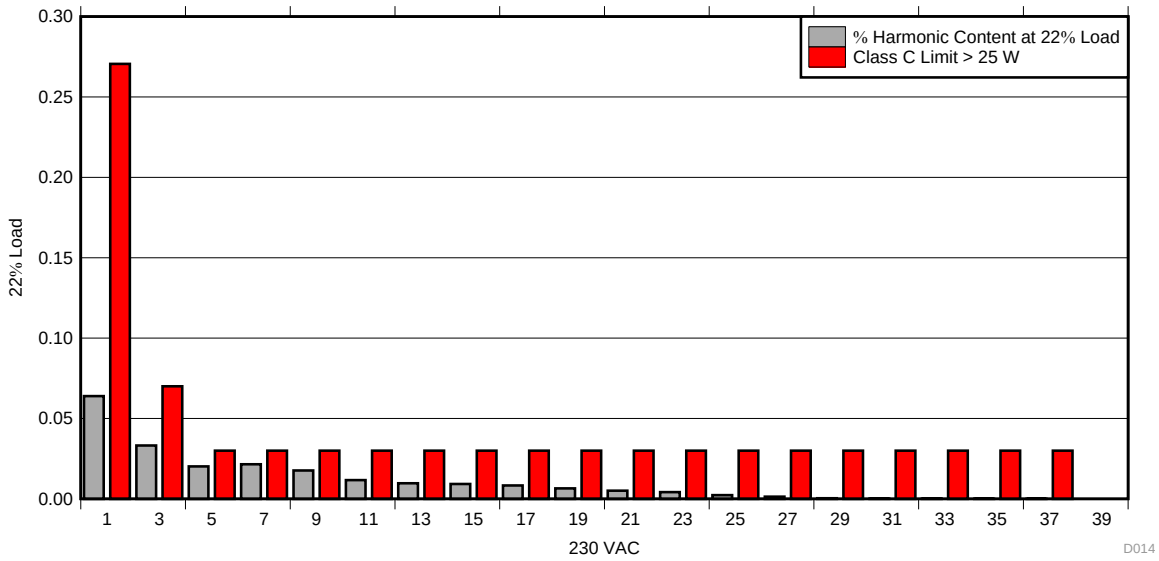



**図 25. Harmonic Test Results at 230-V AC and 22% Load**

#### 3.2.2.3.2 Input Current Harmonics Tested at 100% Load With 196-V LED Load

**表 14. Test Conditions for 100% Load With 196-V LED Load**

| $I_{ADJ}$ (V) | $V_{IN}$ (V) | FREQ (Hz) | $I_{IN}$ (mA) | $P_{IN}$ (W) | PF | $A_{THD}$ | $P_{OUT}$ (W) |
|---|---|---|---|---|---|---|---|
| 10 | 230 | 50 | 936.71 | 213.2 | 0.99 | 3.87% | 196 |

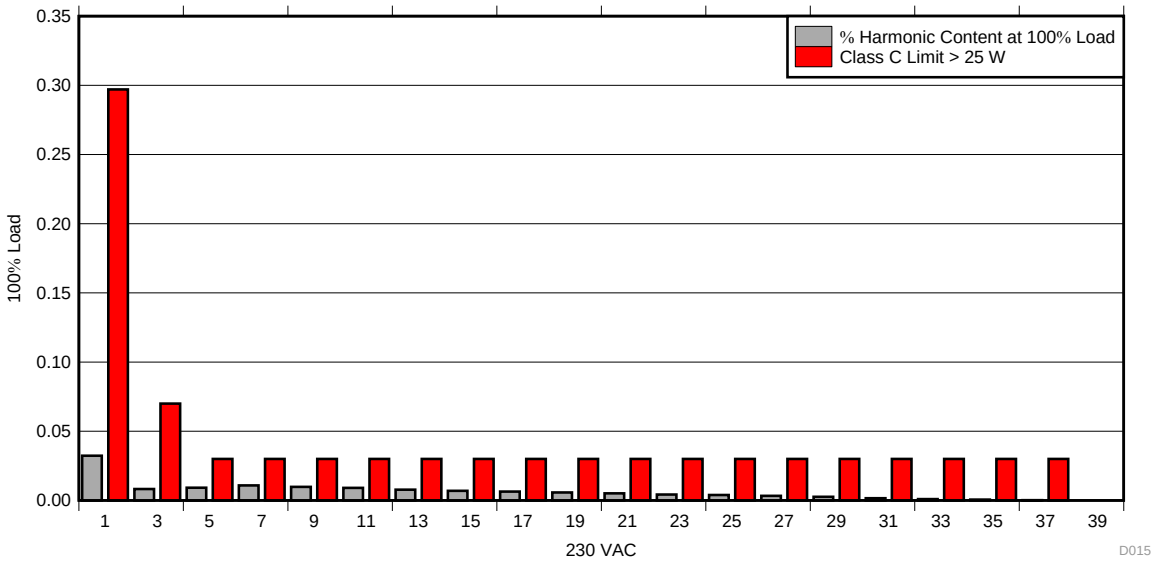



**図 26. Harmonic Test Results at 230-V AC and 100% Load**

#### 3.2.2.3.3 Input Current Harmonics Tested at 36% Load With 102-V LED Load

**表 15. Test Conditions for 36% Load With 102-V LED Load**

| $I_{ADJ}$ (V) | $V_{IN}$ (V) | FREQ (Hz) | $I_{IN}$ (mA) | $P_{IN}$ (W) | PF | $A_{THD}$ | $P_{OUT}$ (W) |
|---|---|---|---|---|---|---|---|
| 3.8 | 230 | 50 | 202.68 | 41.65 | 0.893 | 9.62% | 36.56 |

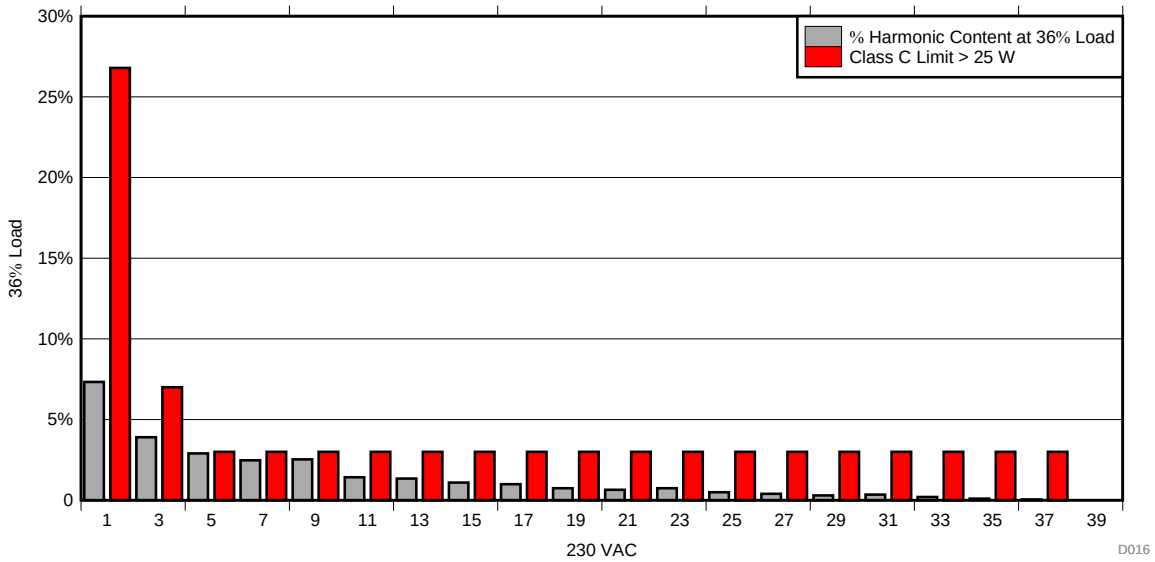



**図 27. Harmonic Test Results at 230-V AC and 36% Load**

#### 3.2.2.4 Functional Waveforms

This section comprises of various functional waveforms such as the PFC output ripple, output current, and voltage ripple waveforms at various input line voltages.

##### 3.2.2.4.1 PFC Output Ripple

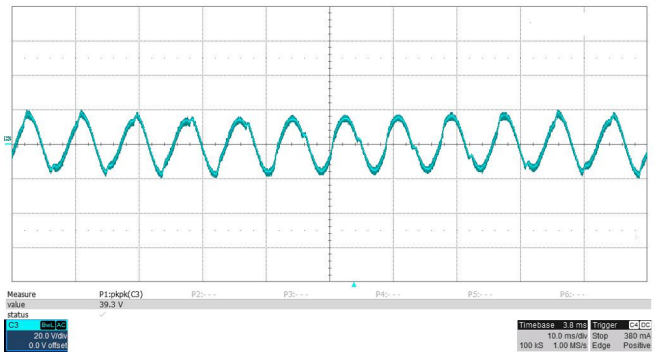


図 28. PFC Output Ripple at 120-V AC With 196-W LED Load

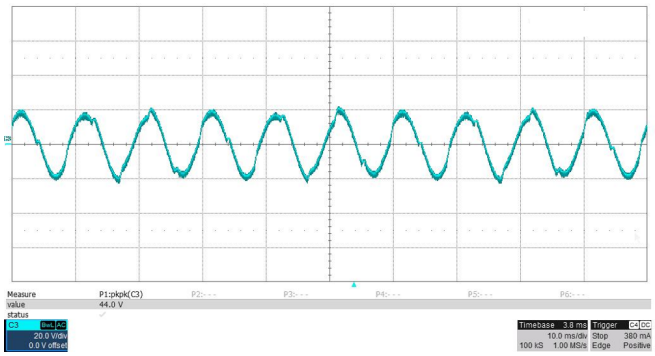


図 29. PFC Output Ripple at 120-V AC With 196-W LED Load

##### 3.2.2.4.2 Output Voltage and Current Ripple

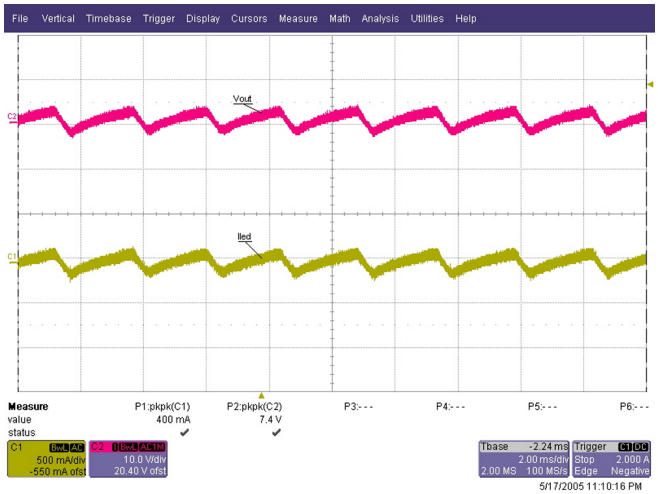



図 30. Output Voltage and Current Ripple With 196-W LED Load at 120-V AC

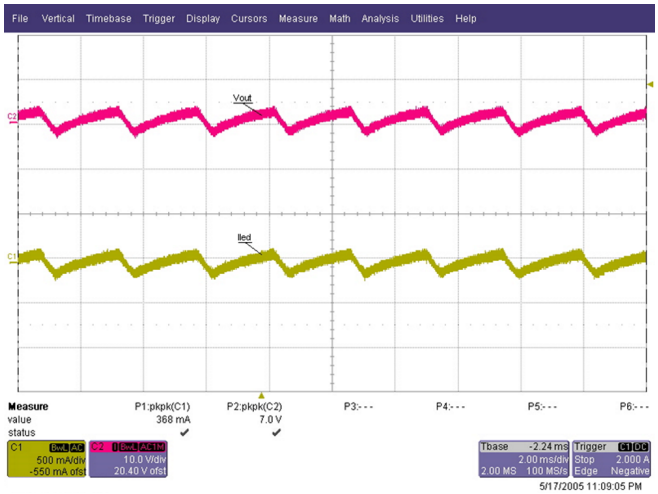



図 31. Output Voltage and Current Ripple With 196-W LED Load at 230-V AC

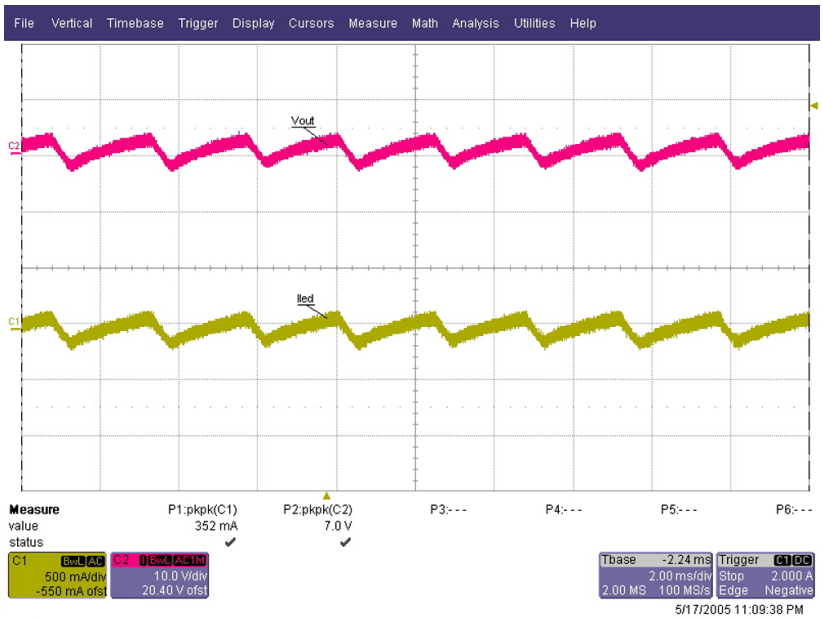



**図 32. Output Voltage and Current Ripple With 196-W LED Load at 265-V AC**

### 3.2.2.5 Transient Waveforms

This section presents transient waveforms such as start-up and turnoff waveforms at various input line voltages.

#### 3.2.2.5.1 Start-up Waveforms at No Load and Full Load

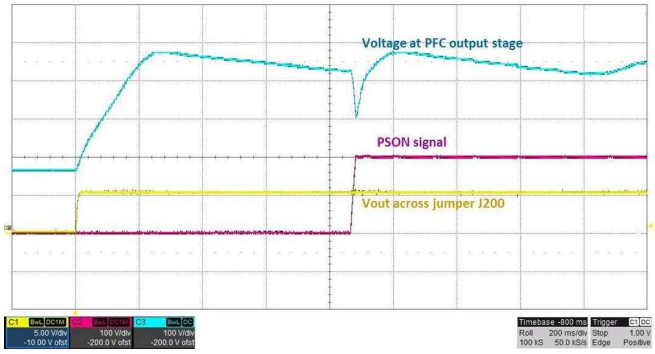



**図 33. Start-up at 120-V AC With No Load at Output**

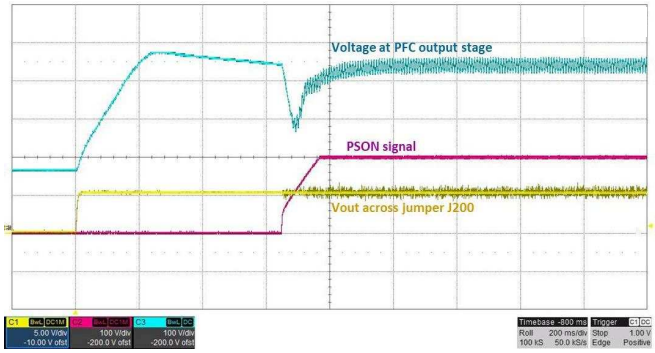



**図 34. Start-up at 120-V AC With 196-W LED Load at Output**

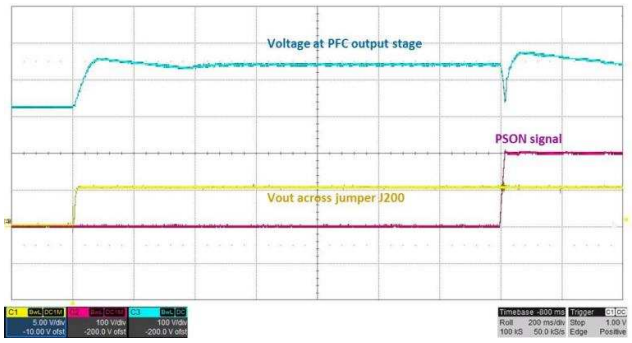



**図 35. Start-up at 230-V AC With No Load at Output**

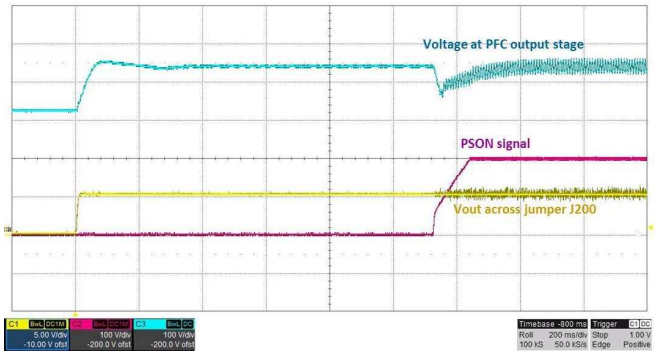



**図 36. Start-up at 230-V AC With 196-W LED Load at Output**

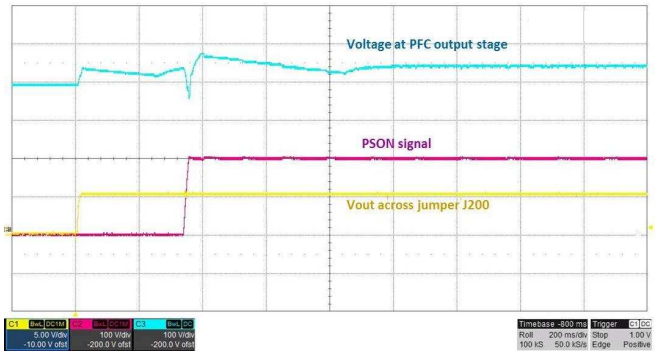



**図 37. Start-up at 265-V AC With No Load at Output**

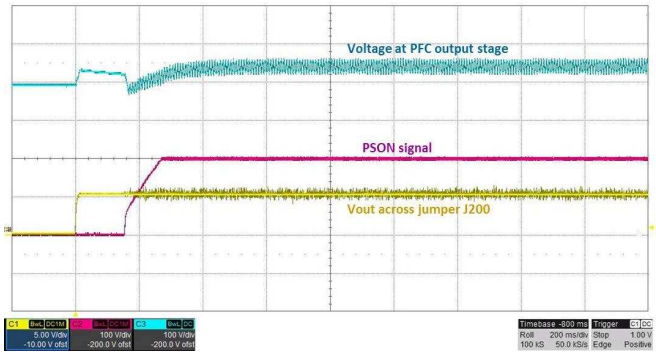



**図 38. Start-up at 265-V AC With 196-W LED Load at Output**

#### 3.2.2.5.2 Turnoff Waveforms

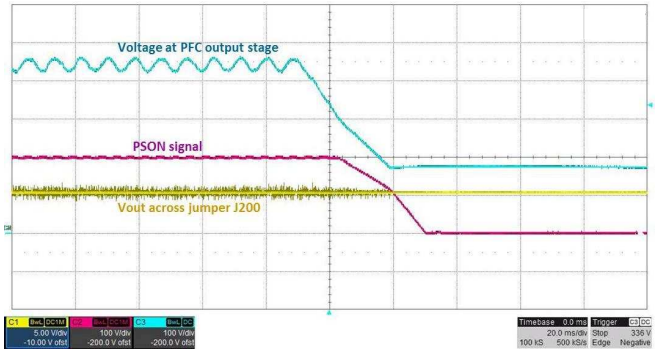



図 39. Turnoff at 120-V AC With 196-W LED Load at Output

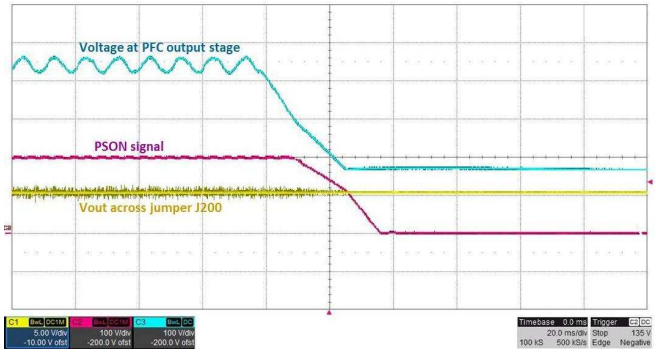



図 40. Turnoff at 230-V AC With 196-W LED Load at Output

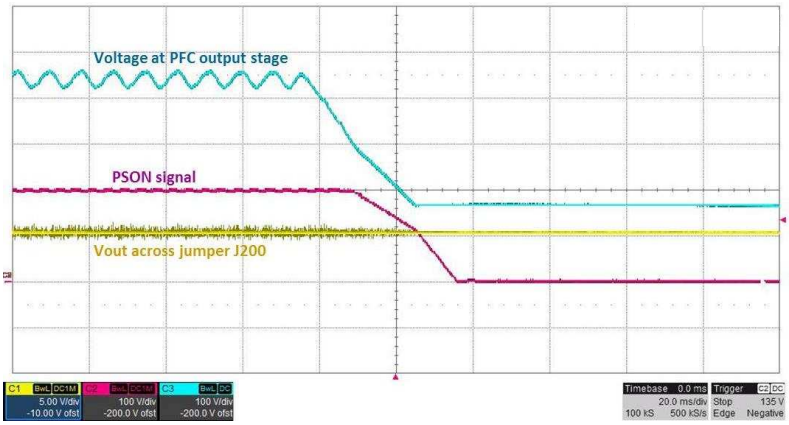



図 41. Turnoff at 265-V AC With 196-W LED Load at Output

### 3.2.2.6 Thermal Images at Full Load

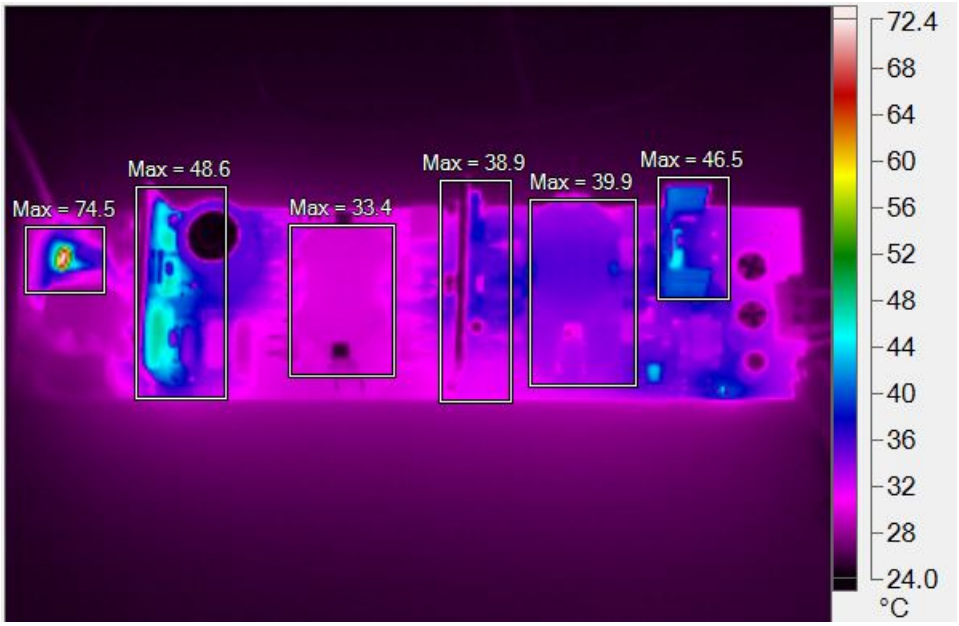



**図 42. Thermal Image of Top View of TIDA-01464 PCB With 196-W Load at 230-V Input AC Voltage**

**表 16. Max Temperature for PCB Components Highlighted in 図 42**

| MAX TEMPERATURE (°C) | DEVICE NAME |
|---|---|
| 74.5 | NTC at the input (RT100) |
| 48.6 | Bridge rectifier, PFC MOSFET, and diode (D102, Q100, and D100) |
| 33.4 | PFC inductor |
| 38.9 | Two-switch flyback MOSFETs |
| 39.9 | Flyback transformer |
| 46.5 | Secondary-side rectifier diode |

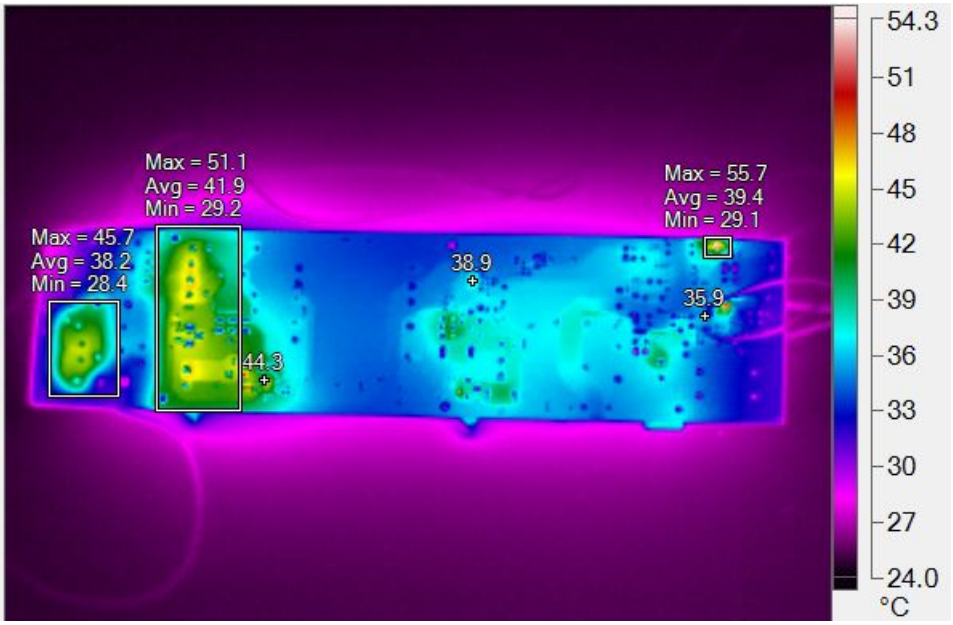



**図 43. Thermal Image of Bottom View of TIDA-01464 PCB With 196-W Load at 230-V Input AC Voltage**

**表 17. Max Temperature for PCB Components Highlighted in 図 43**

| MAX TEMPERATURE (°C) | DEVICE NAME |
|---|---|
| 45.7 | RT100 bottom |
| 51.1 | D102 bottom |
| 44.3 | UCC28180 |
| 38.9 | UCC28740 |
| 35.9 | LM358 |
| 55.7 | Q207 |

# 4 Design Files

## 4.1 Schematics

To download the schematics, see the design files at TIDA-01464.

## 4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01464.

## 4.3 PCB Layout Recommendations

### 4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01464.

## 4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01464.

## 4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01464.

## 4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01464.

## 4.7 Design Calculator Spreadsheet

To download the design calculator spreadsheet for PFC stage, see the design files at TIDA-01464.

# 5 Related Documentation

1. Texas Instruments, *Improving the Performance of Traditional Flyback Topology With Two-Switch –Approach Application Report*

## 5.1 商標

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# 6 About the Authors

**SEETHARAMAN DEVENDRAN** is a systems architect at Texas Instruments, where he is responsible for developing reference design solutions for the industrial segment. Seetharaman brings to this role his extensive experience in analog and mixed signal system-level design expertise. Seetharaman earned his bachelor's degree in electrical engineering (BE, EEE) from Thiagarajar College of Engineering, Madurai, India

**SHENG-YANG YU** is an application engineer at Texas Instruments where he is responsible for developing power supply reference design solutions for strategic customers. Sheng-Yang earned his PhD degree from The University of Texas at Austin.

**SURYA MISHRA** is a systems designer at Texas Instruments, where he is responsible for developing reference design solutions for the Lighting, Industrial Segment. Surya earned his bachelor of electronics and communication engineering from the Motilal Nehru National Institute of Technology (MNNIT), Allahabad.

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