参考資料

TI Designs

25W PLCコントローラ・ユニット用の入力保護およびバックアップ電源のリファレンス・デザイン

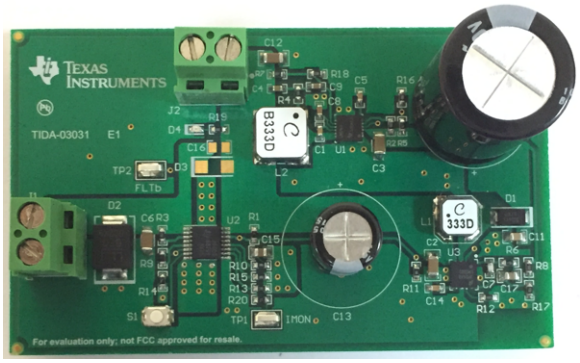
概要

このTI Designは、一般的なPLCコントローラ・ユニットの入力電源パス保護およびバックアップ電源設計用のソリューションです。従来使用されてきたディスクリート回路による実装を、完全に統合された保護回路に置き換えています。

リソース

TIDA-03031	デザイン・フォルダ
TPS2660	プロダクト・フォルダ
LM5002	プロダクト・フォルダ
LM5160	プロダクト・フォルダ

TI E2E™ Community　E2Eエキスパートに質問

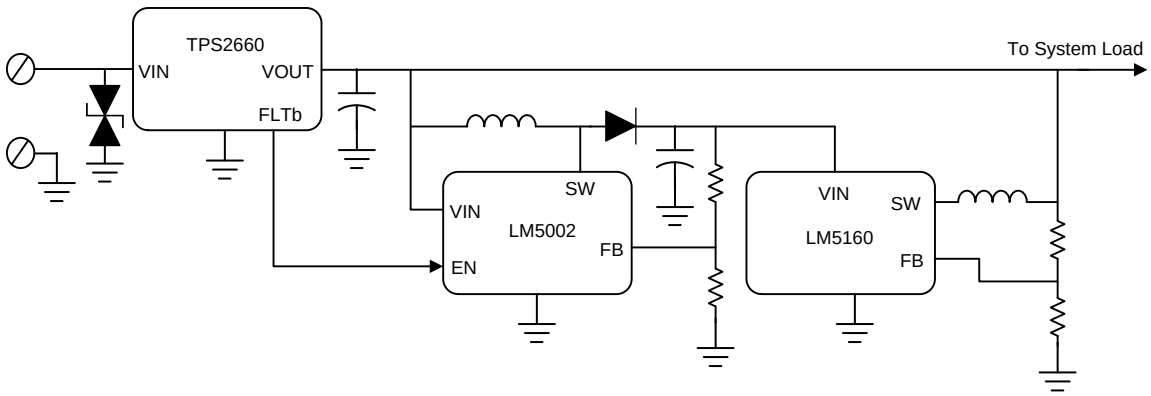


特長

- 19.2～28.8V入力、25Wの出力電力
- 過負荷、過電圧、低電圧、逆電流保護
- 現場での誤配線や逆極性から保護
- ±500V、2Ω (8/20µs)サージ、基準Aの性能に準拠(IEC 61000-4-5)
- ±2kV、50Ω EFT、基準Aの性能に準拠(IEC 61000-4-4)
- 全負荷出力時に10msの電源障害で中断なし(IEC 61000-4-29)
- 高効率降圧および昇圧レギュレータにより、7W出力で120msのバックアップ時間

アプリケーション

- PLC、DCS、PAC
  - CPU
  - I/Oモジュール
  - 通信モジュール
- CNC自動化
  - コントローラ・ユニット
- バックアップ電源アプリケーション



1 System Overview

1.1 System Description

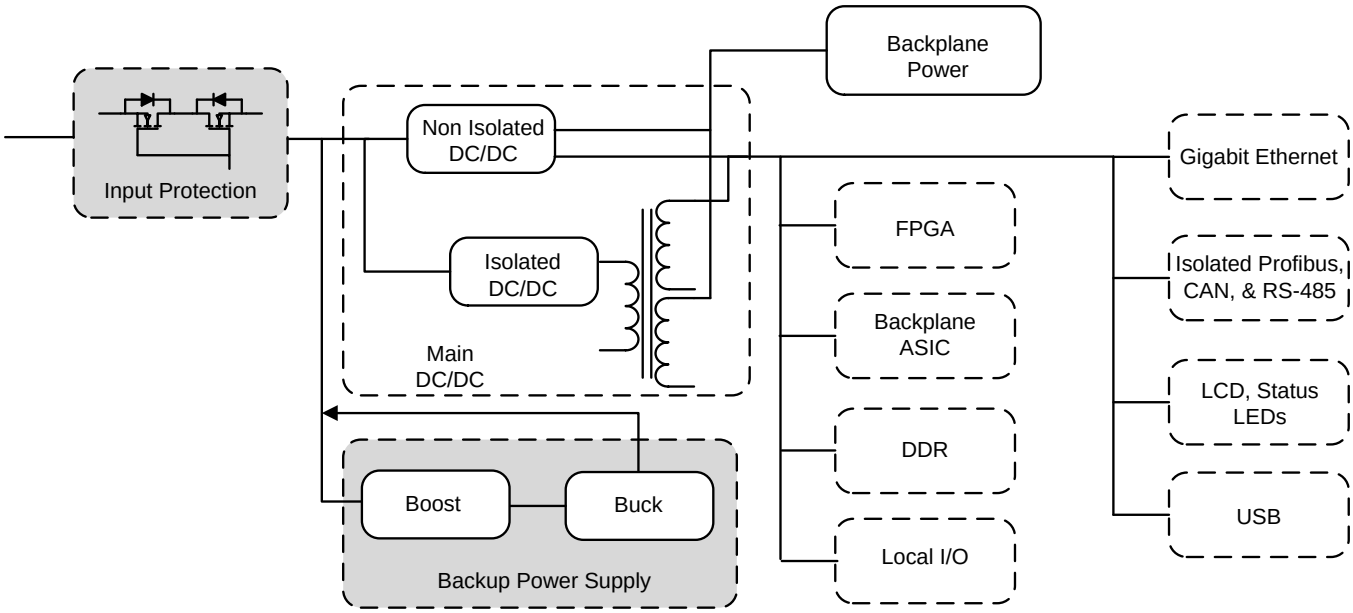


図 1. Typical PLC Controller Unit Power Architecture (TI Design Highlighted)

The PLC system is usually connected to an external 24-V DC power supply to provide power to the controller unit, backplane, and I/O modules. Input protection circuits are required to protect the PLC from faults such as overvoltage, undervoltage, and overload. Because input supply connectors are screw type, there can always be a possibility of reverse supply connections. Protection circuits should block the reverse polarity to protect the PLC from possible negative voltages. At the same time, every PLC is tested for electrostatic discharge (ESD) according to IEC 61000-4-2, burst pulses (EFT) according to IEC 61000-4-4, energy single pulse (surge) according to IEC 61000-4-5, and voltage drops and interruptions according to IEC 61000-4-29. The input side protection circuits must also be capable of withstanding all the protection needs specified by each standard. Traditionally, discrete or semi-integrated circuits have been the solution for designing these protection circuits.

This TI Design focuses on the design of the PLC input protection circuit using the TPS2660 and backup supply design using the LM5002 boost and the LM5160 integrated buck regulators. It provides backup supply for 10 ms at full load and an additional 120 ms duration at ¼th of the full load power at a 17-V regulated voltage. The TPS2660 integrates all protection circuits to provide a single-chip solution for all protection needs.

1.2 Key System Specifications

表 1. Key System Specifications

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	Normal operation	19.2	24	28.8	V
		Reverse Polarity	–28.8			
V_{OUT}	Output voltage	Normal operation	19.2		28.8	V
I_{OUT}	Load current	Normal operation		1.5		A
$V_{IN(UVLO)}$	Input undervoltage lockout	V_{IN} rising		18		V
$V_{IN(OVP)}$	Input overvoltage lockout	V_{IN} rising		30		V
$V_{OUT(BACKUP)}$	Backup supply regulation voltage			17		V
t_{BACKUP}	Backup time	V_{OUT} = 17 V, R_{LOAD} = 40 Ω		150		ms
t_{PFAIL}	Power fail time without interruption (IEC 61000-4-29)	V_{OUT} = 24 V, R_{LOAD} = 16 Ω		10		ms
$V_{IN(SURGE)}$	Input surge voltage (IEC61000-4-5)	V_{OUT} = 24 V, R_{LOAD} = 16 Ω	–500		500	V
$V_{IN(EFT)}$	Input EFT voltage (IEC61000-4-4)	V_{OUT} = 24 V, R_{LOAD} = 16 Ω	–2		2	kV
$V_{IN(ESD)}$	Input system ESD voltage (IEC 61000-4-2)	Contact discharge	–8		8	kV
		Air discharge	–15		15	kV

1.3 Block Diagram

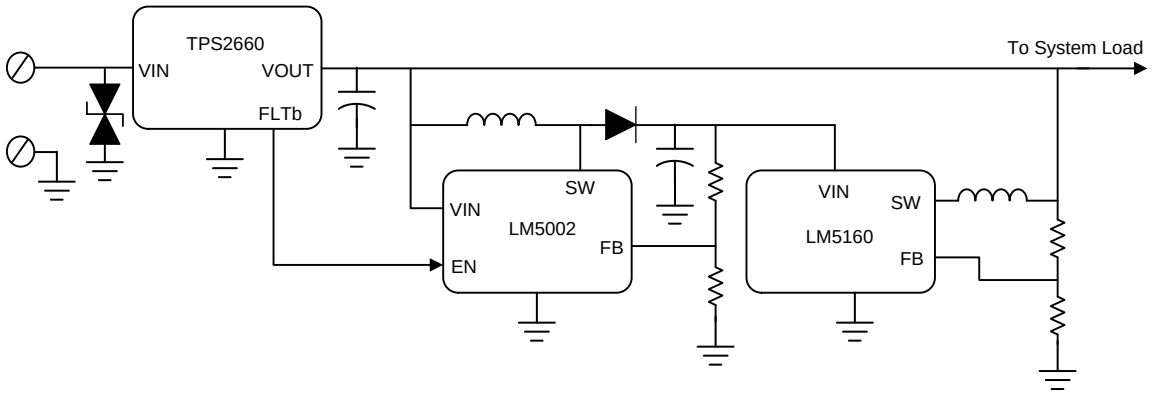


図 2. Block Diagram of TIDA-03031

図 2 shows the block diagram of the input protection and backup supply TI Design. The TPS2660 provides front-end protection features such as overvoltage, undervoltage, overload, inrush current control, reverse current, and reverse polarity. The device also provides monitor functions like fault status and load current monitor output. A 28-V bidirectional TVS along with the TPS2660 provides protection against ±500-V power supply surges, ±2-kV EFT pulses and system ESD.

The LM5002 is configured as a discontinuous mode (DCM) boost converter to charge bulk output capacitor to a higher voltage. It takes around 0.4 seconds to fully charge the bulk output capacitor. Due to the nature of DCM, the boost converter skips switching cycles once the output capacitor fully charges. Output of the bulk capacitor is stepped down to 17 V and fed back to system bus through a high-voltage LM5160 integrated buck regulator. Under normal operation with a 19.2- to 28.8-V input, the buck regulator output is always higher than the regulation voltage, and hence the switching is disabled. The device remains in non-switching state until the input supply voltage drops below the buck regulation voltage.

When power fails, the TPS2660 de-asserts FLTb signal and disables switching of the boost converter. The output capacitor at the TPS2660 supplies full load current momentarily before buck regulator starts regulating the system bus voltage. During backup time, the buck regulator draws power from bulk capacitor and provides backup supply for 120 ms at ¼th of full load power and a 17-V regulated output voltage. The FLTb signal indicates PLC CPU that power-fail event happened in the system. The CPU can initiate backup operation if the power fail signal persists for a longer duration.

1.4 Highlighted Products

1.4.1 TPS2660

The TPS2660x devices are compact, high-voltage eFuses with a full suite of protection features. The wide supply input range of 4.2 to 55 V allows control of many popular DC bus voltages. The device can withstand and protect the loads from positive and negative supply voltages up to ±60 V. Integrated back-to-back FETs provide reverse current blocking feature making the device suitable for systems with output voltage holdup requirements during power fail and brownout conditions. Load, source, and device protection are provided with many adjustable features including overcurrent, output slew rate, and overvoltage and undervoltage thresholds. The internal robust protection control blocks along with the high-voltage rating of the TPS2660x helps to simplify the system designs for surge protection.

1.4.2 LM5002

The LM5002 high-voltage switch mode regulator features all the functions necessary to implement efficient high-voltage boost, flyback, SEPIC and forward converters, using few external components. This easy-to-use regulator integrates a 75-V N-channel MOSFET with a 0.5-A peak current limit. Current mode control provides inherently simple loop compensation and line-voltage feed-forward for superior rejection of input transients. The switching frequency is set with a single resistor and is programmable up to 1.5 MHz. Additional protection features include: current limit, thermal shutdown, undervoltage lockout (UVLO), and remote shutdown capability.

1.4.3 LM5160

The LM5160 is a 65-V, 2-A synchronous step-down converter with integrated high-side and low-side MOSFETs. The constant ON-time control scheme requires no loop compensation and supports high step-down ratios with a fast transient response. An internal feedback amplifier maintains ±1% output voltage regulation over the entire operating temperature range. The ON-time varies inversely with input voltage resulting in nearly constant switching frequency. Peak and valley current limit circuits protect against overload conditions. The undervoltage lockout (EN/UVLO) circuit provides independently adjustable input undervoltage threshold and hysteresis. The LM5160 is programmed through the FPWM pin to operate in continuous conduction mode (CCM) from no load to full load or to automatically switch to discontinuous conduction mode (DCM) at light load for higher efficiency.

2 System Design Theory

The following key specifications are required to start the system design:

- Input undervoltage (V_{UV}) and overvoltage (V_{OV})
- Output full-load current (I_{OUT})
- UVLO of downstream DC/DC converter ($V_{OUT(UVLO)}$)
- Backup time (t_{BACKUP})
- Average load current during back time (I_{BACKUP})

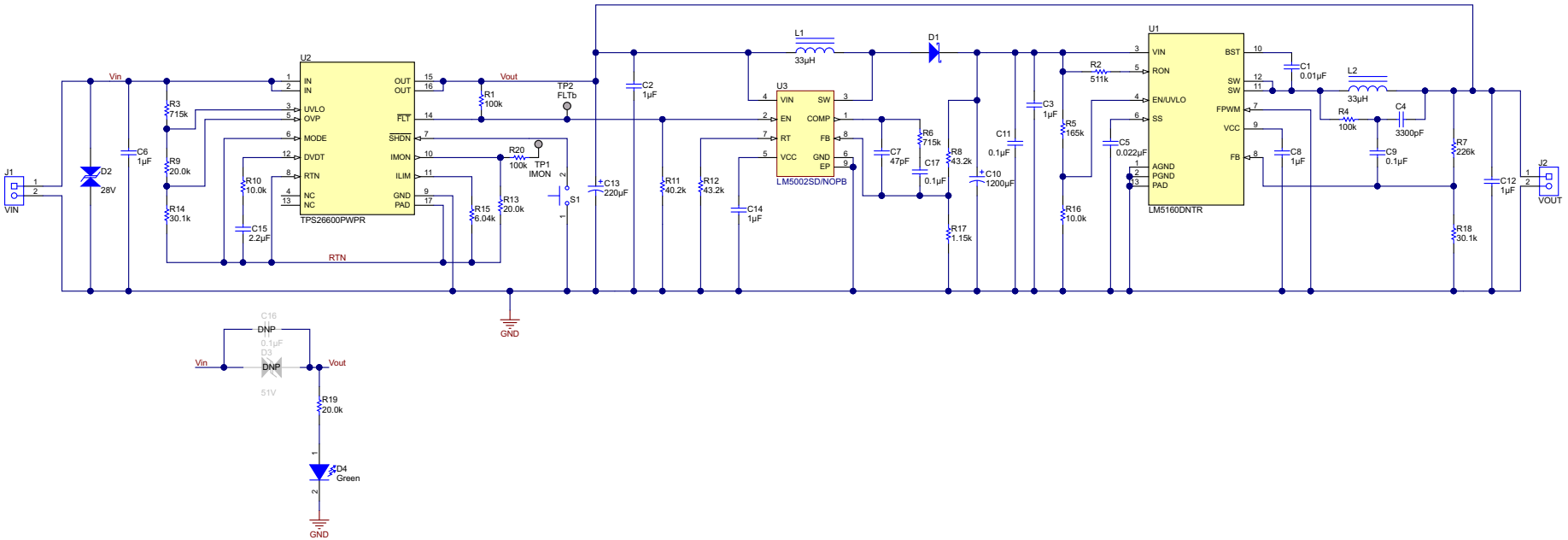


図 3. Schematic Circuit

2.1 Backup Capacitor (C10) Selection

The backup bulk capacitor charges to 48 V to store the energy at higher voltage. During backup time, the buck regulator steps down the capacitor voltage to a regulated DC voltage and supplies to the downstream DC/DC converters. Regulation voltage of the buck regulator is chosen to be higher than the undervoltage lockout $V_{OUT(UVLO)}$ of the downstream converters. Assuming 16V $V_{OUT(UVLO)}$, the buck regulation voltage is given by 式 1.

$$V_{OUT(REG)} = V_{OUT(UVLO)} + 1\,V = 16 + 1 = 17\,V \quad (1)$$

The bulk output capacitor is allowed to discharge until the falling UVLO of the buck regulator. The falling UVLO threshold is selected based on maximum duty ratio of the buck regulator. Assuming D_{MAX} = 0.9, the buck regulator UVLO falling is calculated as given by 式 2.

$$V_{BUCK(UVLO)} = \frac{V_{OUT(REG)}}{D_{MAX}} = \frac{17}{0.9} = 19\,V \quad (2)$$

The bulk capacitor value is calculated using 式 3.

$$C_{BOOST} = \frac{V_{OUT(REG)} \times \left[\left(I_{OUT} \times t_{PFAIL} \right) + \left(I_{BACKUP} \times t_{BACKUP} \right) \right]}{0.5 \times \left(V_{BOOST}^{2} - V_{BUCK(UVLO)}^{2} \right) \times \eta} \quad (3)$$

$$C_{BOOST} = \frac{17 \times \left[\left(1.5 \times 10\,m \right) + \left(0.375 \times 100\,m \right) \right]}{0.5 \times \left(48^{2} - 19^{2} \right) \times 0.9} = 1021\,\mu F$$

where:

- V_{BOOST} is the boost capacitor voltage
- t_{PFAIL} is the time for which the PLC should not see power interruption; typically 10 ms as per IEC 61000-4-29 specifications
- t_{BACKUP} is the time required by the CPU module to complete backup operation
- η is the power conversion efficiency of the buck regulator

Considering ±20% tolerance, the 1200-µF/50-V Nichicon capacitor is selected for this application.

注: For any other backup supply voltage, the buck regulator feedback and EN/UVLO resistor divider values should be updated according to equations given in the LM5160 datasheet.

2.2 TPS2660 Protection Circuit Design

The TPS2660 is a high-voltage eFuse or integrated hot swap controller, designed to protect the loads from various system faults such as overvoltage, undervoltage, input reverse polarity, reverse current, overload, and output short circuit. Its wide 4.2- to 60-V input voltage range and programmable 0.1- to 2.2-A current limit capability makes this device ideal for protecting the loads operating from many popular DC bus voltages.

Integrated back-to-back connected FETs along with programmable inrush current control and reverse current blocking features make the device suitable for the systems with output voltage holdup requirements during power fail and brownout conditions. Load current monitor, fault reporting, and shutdown control features provide ease of control with an external microprocessor. The block diagram of the TPS2660 is shown in 図 4.

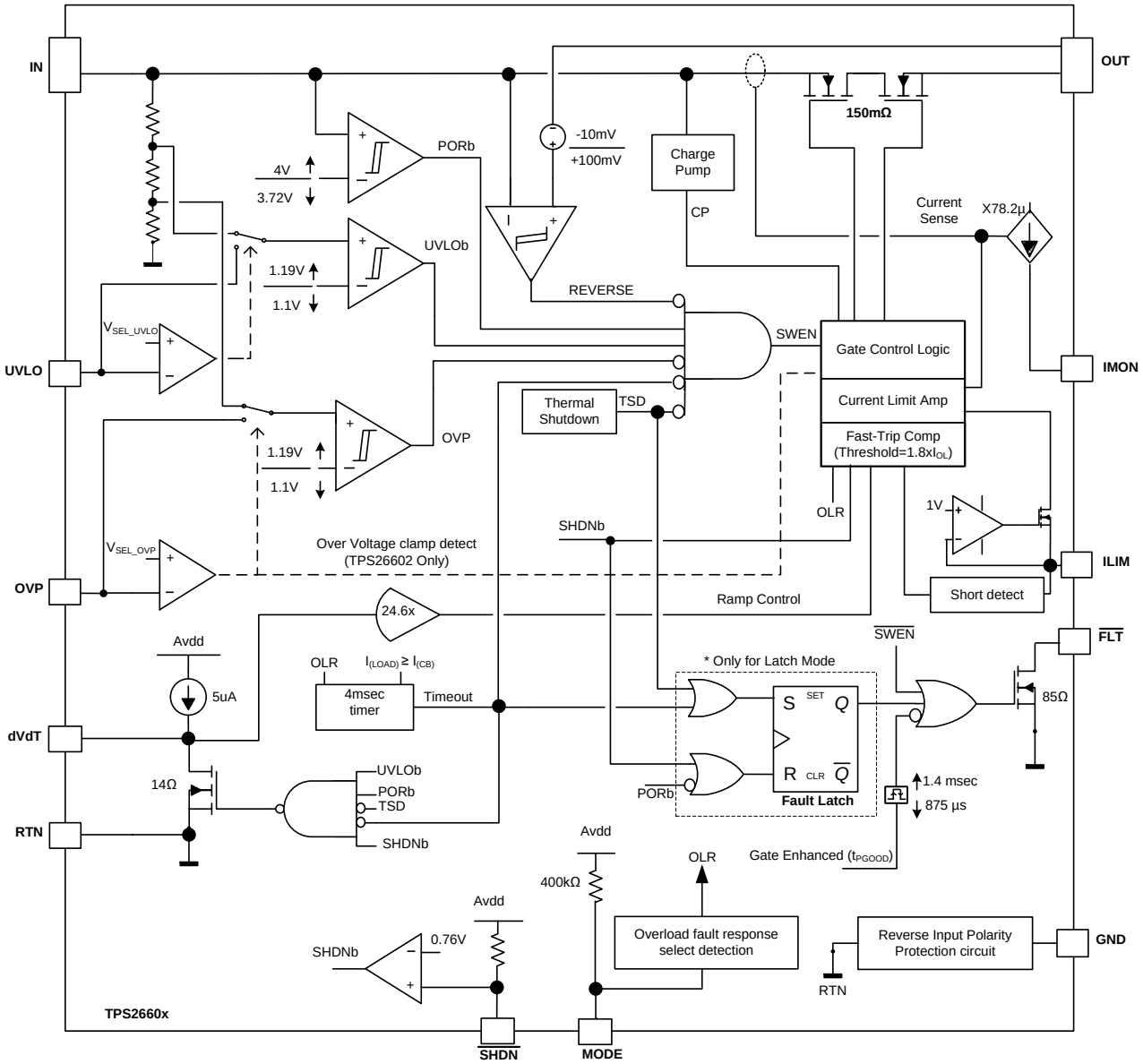


図 4. Block Diagram of TPS2660

2.2.1 Output Capacitor (C13) Selection

The eFuse output capacitor is selected to support the 0.25-ms backup time before the buck regulator starts regulating the bus voltage. Under worst case power fail conditions, the eFuse output capacitor discharges from $V_{IN(MIN)}$ to $V_{OUT(REG)}$. The eFuse output capacitor value is calculated using 式 4

$$C_{OUT} = \frac{I_{OUT} \times t_{eFUSE}}{\left(V_{IN(MIN)} - V_{OUT(REG)}\right)} = \frac{1.5 \times 0.25\ m}{(19.2 - 17)} = 170\ \mu F \quad (4)$$

where:

- t_{eFUSE} is the backup time provided by the eFuse
- $V_{IN(MIN)}$ is the minimum operating input voltage of the PLC
- $V_{OUT(REG)}$ is the regulation voltage of the buck regulator

Considering ±20% tolerance, the 220-µF/35-V electrolytic capacitor is selected for this application.

2.2.2 C_{dVdT} (C15) and R_{dVdT} (R10) Selection

Soft start capacitor (C_{dVdT}) controls inrush current and reduces peak current drawn from the power supply during start-up. Effective capacitance at output of the eFuse is sum of C_{OUT} and C_{BOOST}. Assuming the capacitor charging current to be 1/10th of full load current, the start-up time required is calculated using 式 5.

$$t_{dVdT} = \frac{\left(C_{OUT} + C_{BOOST}\right) \times V_{IN(MAX)}}{I_{CHARGE}} = \frac{(220\ \mu + 1200\ \mu) \times 30}{0.15} = 0.28\ s \quad (5)$$

where:

- I_{CHARGE} is the inrush current to charge the output capacitors; typically 1/10th of full load current
- $V_{IN(MAX)}$ is the maximum operating input voltage of the PLC

For a given start-up time, C_{dVdT} capacitance value is calculated using 式 6.

$$C_{dVdT} = \frac{t_{dVdT}}{8000 \times V_{IN(MAX)}} = \frac{0.28}{8000 \times 30} = 1.2\ \mu F \quad (6)$$

A 2.2-µF/16-V ceramic capacitor is selected as start-up control capacitor.

If the power-fail duration is less than 10 ms, to restart the TPS2660 quickly without much discharging backup capacitor, a series resistor is required to hold the C_{dVdT} capacitor charge during transient power fail conditions. For a 10-ms power fail, R_{dVdT} is calculated using 式 7.

$$R_{dVdT} = \frac{t_{FAIL(TR)}}{\ln(3.6) \times C_{dVdT}} = \frac{10\ m}{\ln(3.6) \times 2.2\ \mu} = 3.54\ k\Omega \quad (7)$$

where:

- t_{FAIL_TR} is the transient power fail time; typically 4 to 10 ms

注: Power dissipated in the device during start-up must be kept well below the maximum allowable power dissipation for a given start-up time to prevent entering into thermal shutdown. Use the TPS2660 design calculator to verify the margin available for the glitch free start-up. A minimum 30% margin at 85°C ambient is recommended for a successful design.

2.2.3 UVLO, OVP Resistors Selection

UVLO and OVP resistors selected based on input operating voltage range of the PLC. R14 in chosen in the range from 10k to 49.9k. R9 and R3 are calculated using 式 8 and 式 9, respectively.

$$R9 = R14 \times \left(\frac{V_{UV(LOR)} \times V_{OV}}{V_{OV(PR)} \times V_{UV}} - 1 \right) = 30.1\,k\Omega \times \left(\frac{1.19 \times 30}{1.19 \times 18} - 1 \right) = 20\,k\Omega \quad (8)$$

$$R3 = R14 \times \left(\frac{V_{OV}}{V_{OV(PR)}} \right) \times \left(1 - \frac{V_{UV(LOR)}}{V_{UV}} \right) = 30.1\,k\Omega \times \left(\frac{30}{1.19} \right) \times \left(1 - \frac{1.19}{18} \right) = 708\,k\Omega \quad (9)$$

where:

- V_{UVLOR} and V_{OVPR} are UVLO and OVP rising thresholds of the device, 1.19 V typical
- V_{UV} and V_{OV} are undervoltage and overvoltage input voltage levels

R14 selected as 30.1 kΩ, R9 selected as 20 kΩ, and R3 selected as 715 kΩ.

2.2.4 Current Limit Resistor (R15) Selection

The current limit is selected based on the power rating of the PLC module. This TI Design assumes 25-W power rating at the output of the downstream DC/DC converters. The maximum input current at a minimum supply voltage is calculated using 式 10.

$$I_{IN(MAX)} = \frac{P_{OUT}}{\eta \times V_{IN(MIN)}} = \frac{25}{0.9 \times 19} = 1.46\ A \quad (10)$$

Additional current to charge the boost output capacitor is added to the maximum input current during start-up. The current limit is set at 5% higher than the maximum expected input current, and the corresponding current limit resistor is calculated using equation式 11.

$$R15 = \frac{12}{1.05 \times \left(I_{IN(MAX)} + I_{BOOST} \right)} = \frac{12}{1.05 \times (1.46 + 0.25)} = 6.6\,k\Omega \quad (11)$$

R15 selected as 6.04 kΩ.

2.3 Overload or Short-Circuit Protection

Accurate overload control in each PLC unit is essential to avoid oversizing of the field power supply. The TPS2660 can control overload within ±5% over temperature. When the overload is present, the device indefinitely regulates load current at set current limit. If the overload is severe, output voltage drops and increases power dissipation in the device. If the device hits thermal limit, it turns off and attempts restart after 512 ms. This operation continues until the overload is removed from the system. The current monitor output (IMON) can be used to determine overload status of the system.

注: Other modes of current limit responses are available based on the MODE pin status. See the TPS2660 datasheet for a detailed description (SLVSDG2).

If a faulty module causes short circuit in the system, the fast trip comparator detects the short-circuit condition at 1.8 times the set current limit and immediately isolates the module from the power supply.

2.4 Surge Protection

The TPS2660 is designed to handle the fastest supply slew rates that occur due to the application of the surge pulse. It does not require additional circuits to smoothen the surge pulse. A bidirectional TVS in SMC package along with the TPS2660 is sufficient to give a criteria-A performance with a ±500-V, 2-Ω surge pulse (8/20-µs) according to IEC 61000-4-5. A proprietary high-speed protection algorithm immediately disconnects the output from the input and prevents surge passing from the input to the output.

2.4.1 Input TVS Diode (D2) Selection

A bidirectional TVS is needed at input to clamp the surge pulse in both positive and negative directions. The reverse standoff voltage (V_{RWM}) of the TVS must be higher than the maximum operating input voltage. The clamping voltage of the TVS is calculated using 式 12 and 式 13.

$$V_{CL} = V_{IN} + \left(R_D \times I_{SURGE}\right) \quad (12)$$

$$I_{SURGE} = \frac{V_{SURGE}}{R_C} \quad (13)$$

where:

- R_D is the dynamic resistance of the TVS
- R_C is the coupling impedance of the surge pulse generator
- V_{SURGE} is the applied surge voltage

IEC 61000-4-5 specifies ±500 V as a level-1 surge pulse voltage with a 2-Ω coupling impedance for the power path. A single 28-V TVS (SMCJ28CA) is selected, which clamps the surge voltage to ±44 V at 24 V input voltage. The sum of the clamp voltage and the nominal test input voltage must be below the ±70-V transient abs max of the TPS2660. Multiple TVS diodes connected in series can be used to support higher voltage surge compliance.

2.5 Power Fail, Reverse Current Protection

When power fails, the reverse current protection circuit in the TPS2660 immediately turns off the internal FETs to prevent discharge of the output capacitance from the output to the input. When the input supply voltage drops below the UVLO threshold, the device shuts down and the back-to-back connected FETs completely isolate the output and input. During power fail event, the eFuse output capacitor momentarily supplies power to the downstream DC/DC converters. When system bus voltage starts falling, the buck converter starts switching and regulates the system bus voltage to 17 V. The FLTb signal pulls low and disables boost converter operation during backup time and indicates the CPU that power fail happened in the system.

If the CPU detects a longer power fail duration, it can start the backup operation. Bulk capacitor supports 10 ms of backup time with full load and 120 ms of backup time with ¼th of the full load. If power resumes before the CPU starts backup operation, the TPS2660 starts in current limit mode to quickly ramp up the system bus voltage to the input voltage level. Once the system bus voltage is close to the input voltage, the FLTb pin releases pulldown and allows the boost converter to charge the output bulk capacitor.

2.6 Electrical Fast Transients Protection

EFT burst pulses contain lower energy than a single surge pulse. A 1-µF input capacitor along with TVS diode can effectively suppress these pulses. This TI Design can withstand ±2-kV burst pulses and provides criteria-A performance.

2.7 Reverse Polarity or Field Miswiring Protection

Reverse polarity or field miswiring is not unlikely due to screw-type power supply connections in the PLC. Negative input voltages are also generated while performing the surge test. The TPS2660 integrates reverse polarity protection to disconnect downstream when the power supply polarity is negative. Traditionally, either a series diode or a PFET is used to solve this problem.

3 Getting Started Hardware

3.1 Hardware

No additional jumper settings are required to test the hardware. 表 2 describes accessible terminals and test points available on the board. The general hardware connection test setup is shown in 図 5.

表 2. Placeholder

REFERENCE	LABEL	DESCRIPTION
J1	VIN	Input supply terminal
J2	VOUT	Output voltage or load terminal
TP1	FLTb	Fault status output
TP2	IMON	Load current monitor output

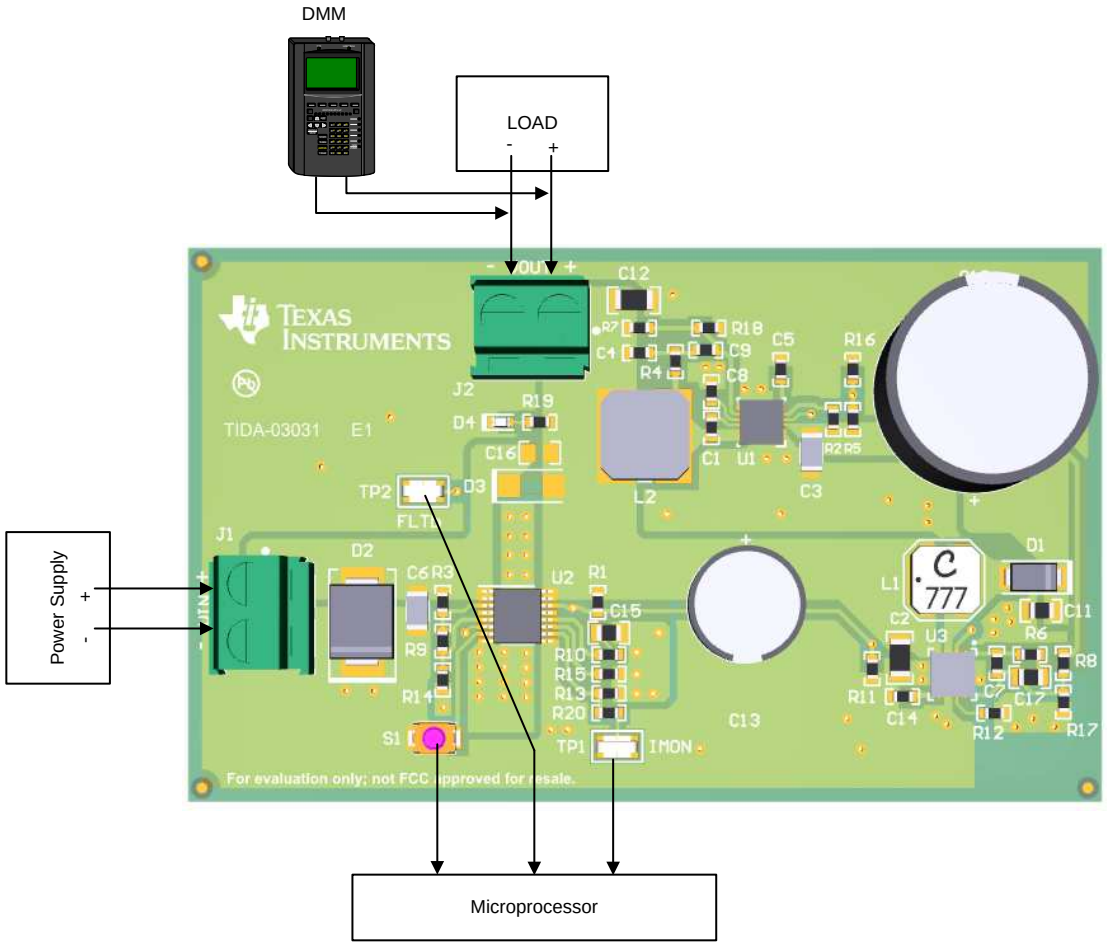


図 5. Hardware Connection Setup

4 Testing and Results

4.1 Test Setup

図 6. Test Setup

4.2 Start-up Tests

The following scope shots show how the reference design responds to different start up and reverse polarity conditions.

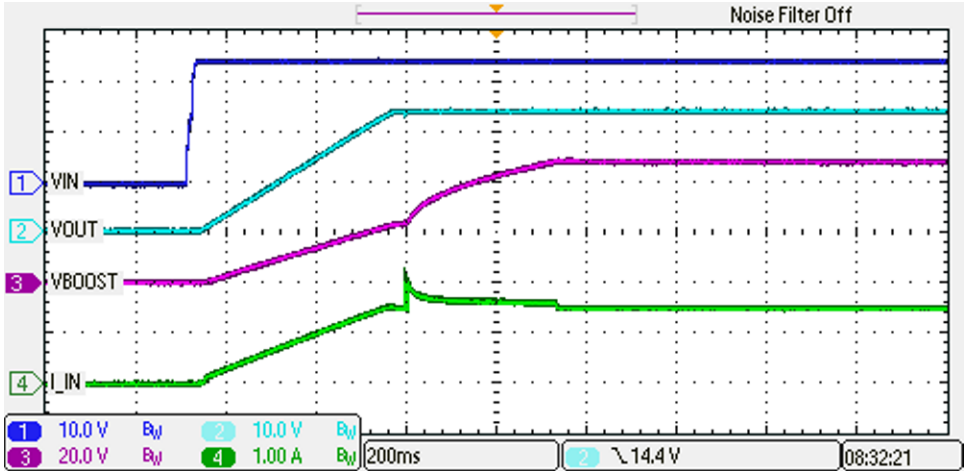


図 7. Output Voltage Start-up and Boost Capacitor Charging With V_{IN} = 24 V, Load = 16 Ω

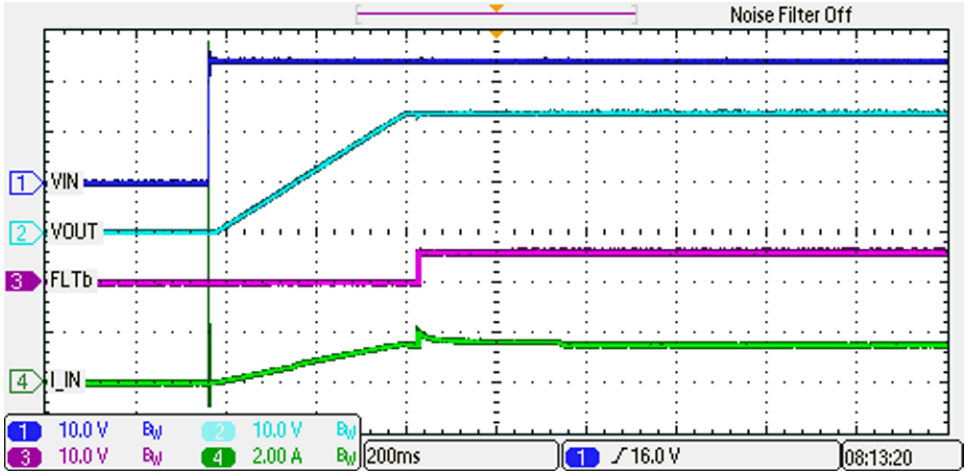


図 8. Hot Plug With V_{IN} = 24 V, Load = 16 Ω

4.3 Reverse Polarity Test

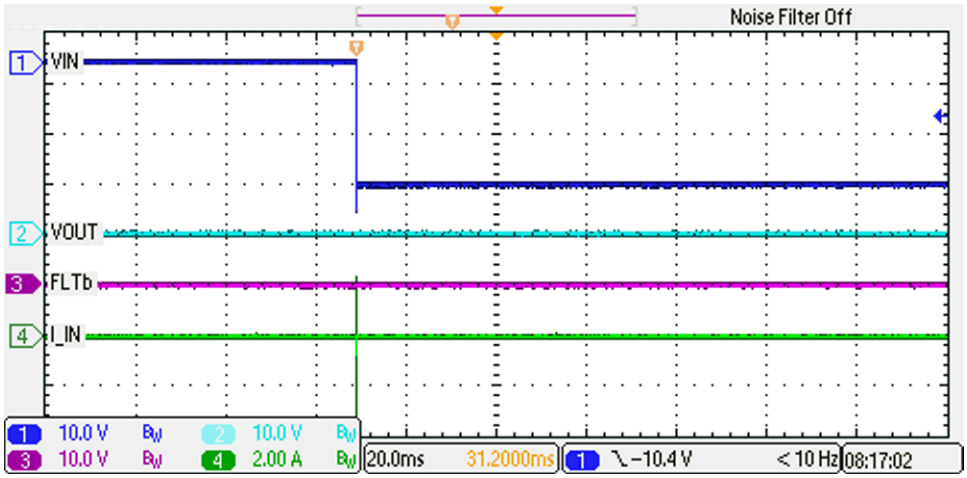


図 9. Reverse Polarity Hot Plug With V_{IN} = 24 V

4.4 Overload Test

図 10 shows the output short circuit response of the reference design.

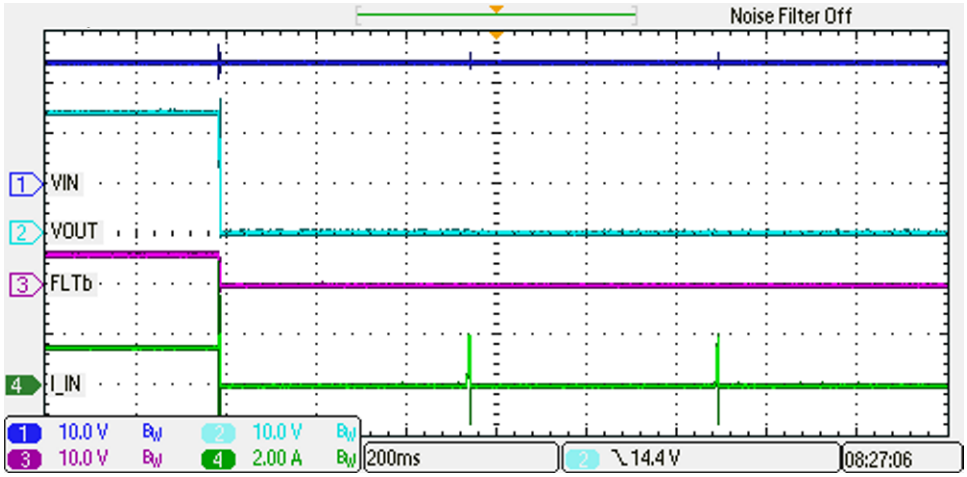


図 10. Output Short-Circuit With V_{IN} = 24 V, Load = 16 Ω

4.5 Power Fail Tests

図 11 to 図 14 show the reference design backup supply duration at different load conditions for indefinite power fail and 図 15 shows the performance for 10 ms power fail duration.

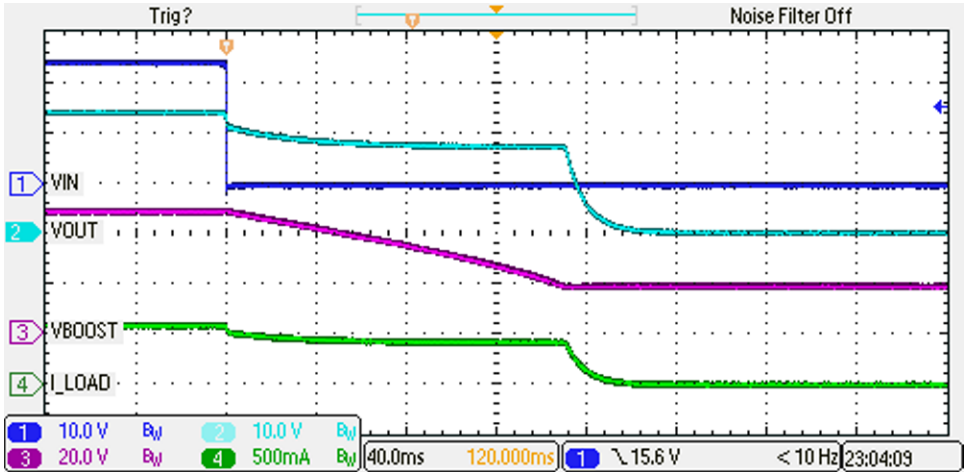


図 11. Input Power-Fail With V_{IN} = 24 V, Load = 40 Ω, Backup Time = 150 ms

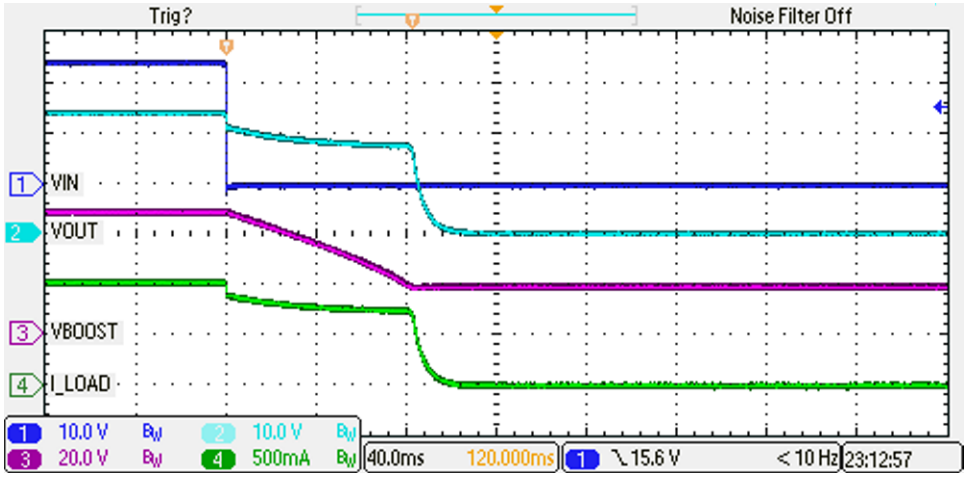


図 12. Input Power-Fail With V_{IN} = 24 V, Load = 24 Ω, Backup Time = 85 ms

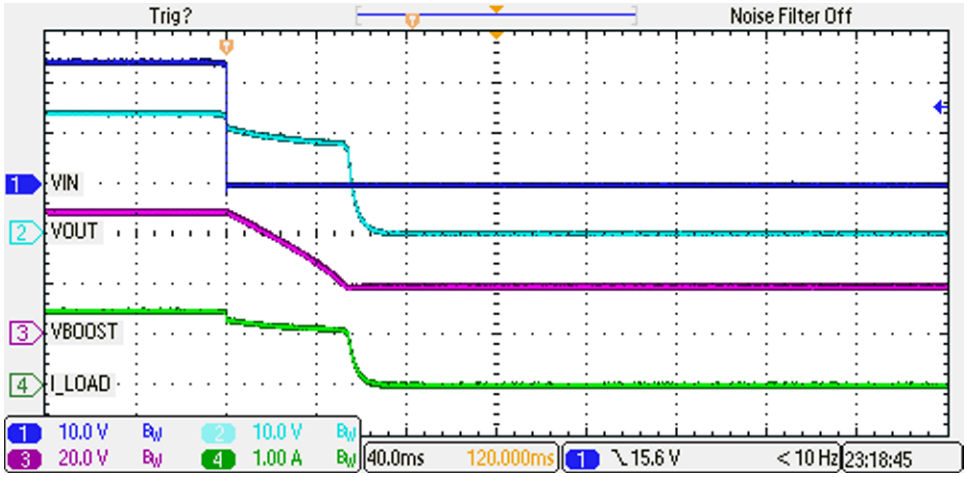


図 13. Input Power-Fail With V_{IN} = 24 V, Load = 16 Ω, Backup Time = 50 ms

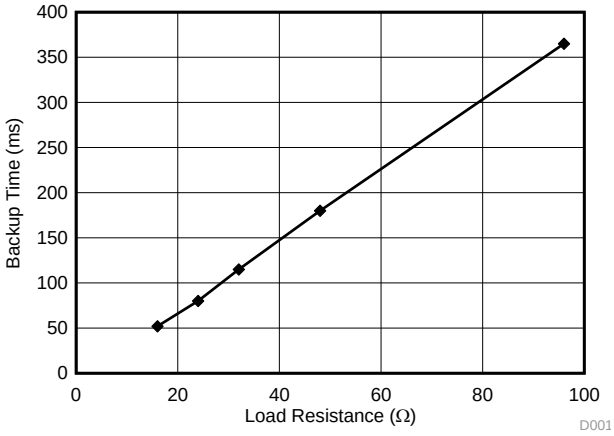


図 14. Backup Time versus Load Resistance

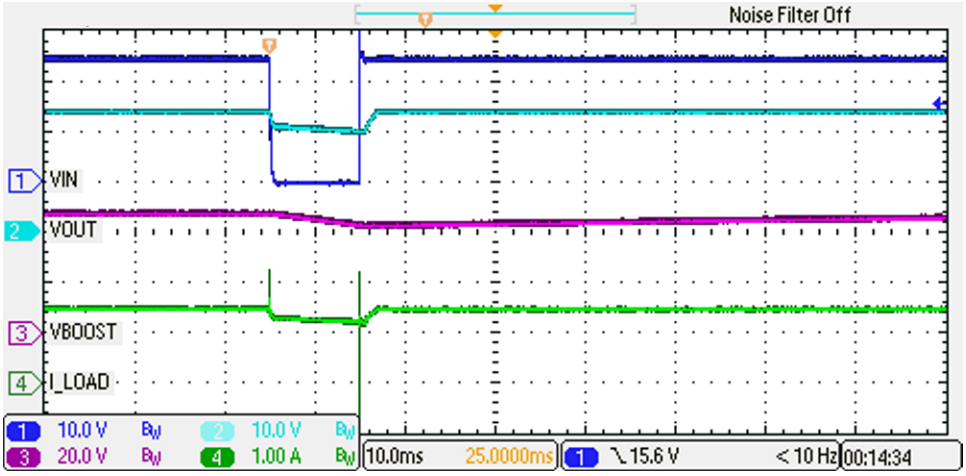


図 15. 10-ms Input Power-Fail With V_{IN} = 24 V, Load = 16 Ω (IEC 61000-4-29 Level 1)

4.6 Surge Tests

図 16 to 図 19 show the performance of the reference design for positive and negative 500 V, 2Ω, 8/20 μs (IEC 61000-4-5) surge pulses. The backup supply voltage is available during the surge event and provides criteria A performance.

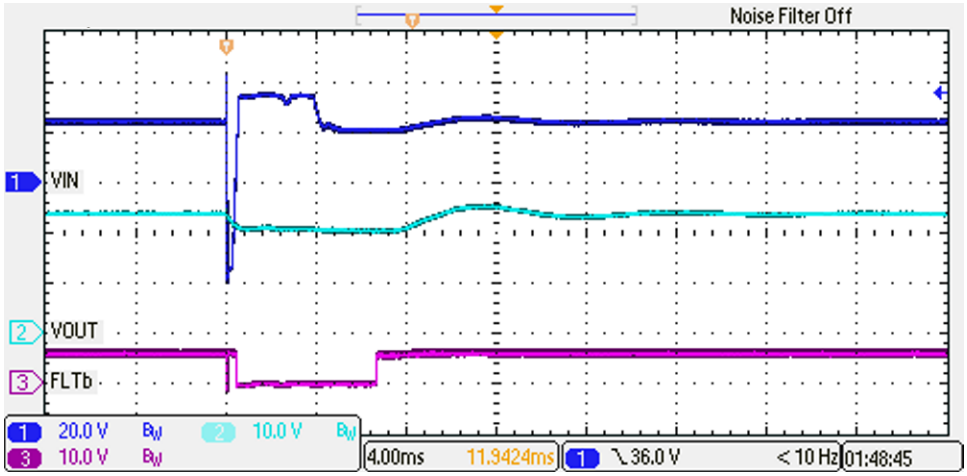


図 16. 500-V, 2-Ω, 8/20-µs Surge Response With V_{IN} = 24 V, Load = 16 Ω (IEC 61000-4-5 Level 1, L-N Coupling)

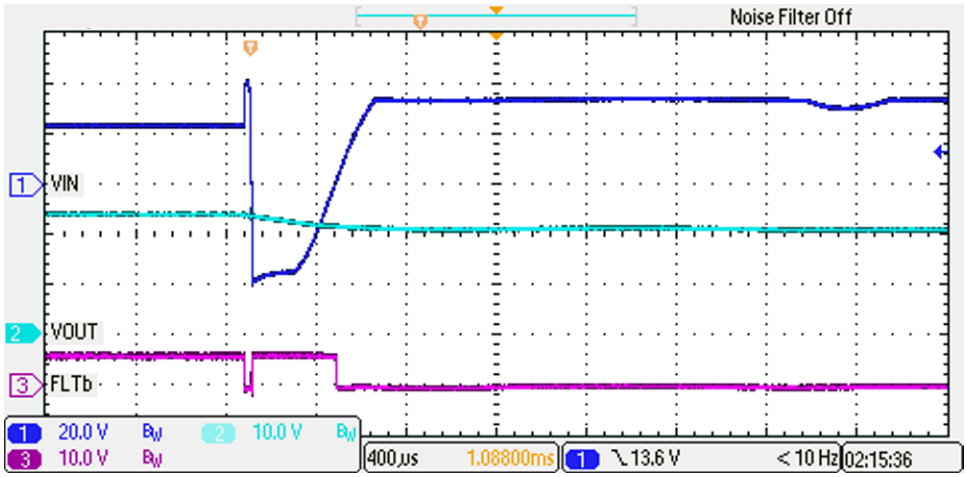


図 17. Zoom at the Instance of Surge

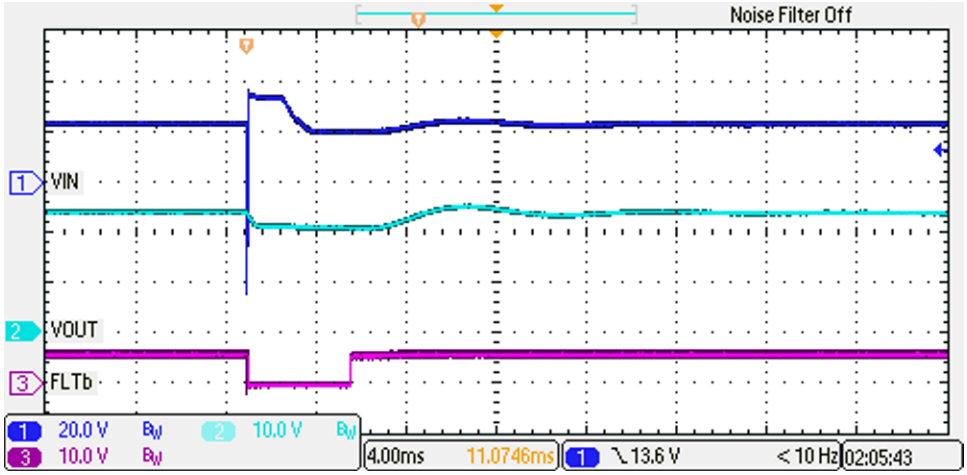


図 18. –500-V, 2-Ω, 8/20-µs Surge Response With V_{IN} = 24 V, Load = 16 Ω (IEC 61000-4-5 Level 1, L-N Coupling)

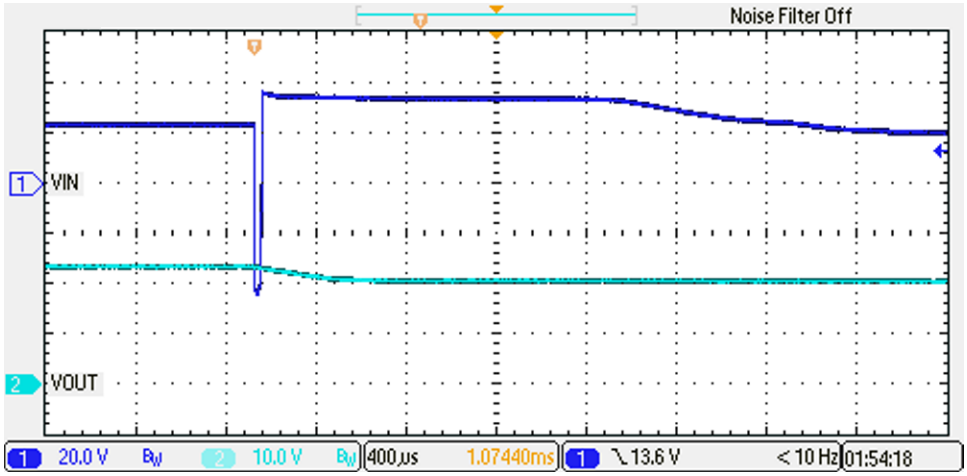


図 19. Zoom at the Instance of Surge

4.7 EFT and ESD Tests

表 3. Summary of the EFT (IEC 61000-4-4 Level 3, 5 kHz) Test Results

BURST MAGNITUDE AND POLARITY	COUPLING MODE	RESULT	PERFORMANCE
2 kV	L	Pass	Criteria A
–2 kV	L	Pass	Criteria A
2 kV	N	Pass	Criteria A
–2 kV	N	Pass	Criteria A
2 kV	L N	Pass	Criteria A
–2 kV	L N	Pass	Criteria A
2 kV	L PE	Pass	Criteria A
–2 kV	L PE	Pass	Criteria A
2 kV	N PE	Pass	Criteria A
–2 kV	N PE	Pass	Criteria A
2 kV	L N PE	Pass	Criteria A
–2 kV	L N PE	Pass	Criteria A

表 4. Summary of the ESD (IEC 61000-4-2 Level 4) Test Results

ESD ON POWER PORTS	MAGNITUDE	RESULT
Contact discharge	±8 kV	Pass
Air discharge	±15 kV	Pass

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-03031.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-03031.

表 5. TIDA-03031 BOM

ITEM	DESIGNATOR	QTY	VALUE	PARTNUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
1	!PCB1	1		TIDA-03031	Any	Printed Circuit Board	
2	C1	1	0.01uF	GRM188R72A103KA01D	MuRata	CAP, CERM, 0.01 µF, 100 V, +/- 10%, X7R, 0603	0603
3	C2, C12	2	1uF	GRM31MR71H105KA88L	MuRata	CAP, CERM, 1 µF, 50 V, +/- 10%, X7R, 1206	1206
4	C3, C6	2	1uF	GRM31CR72A105KA01L	MuRata	CAP, CERM, 1 µF, 100 V, +/- 10%, X7R, 1206	1206
5	C4	1	3300pF	GRM188R72A332KA01D	MuRata	CAP, CERM, 3300 pF, 100 V, +/- 10%, X7R, 0603	0603
6	C5	1	0.022uF	GRM188R71C223KA01D	MuRata	CAP, CERM, 0.022 µF, 16 V, +/- 10%, X7R, 0603	0603
7	C7	1	47pF	GRM1885C1H470JA01D	MuRata	CAP, CERM, 47 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603
8	C8, C14	2	1uF	GRM188R71C105KA12D	MuRata	CAP, CERM, 1 µF, 16 V, +/- 10%, X7R, 0603	0603
9	C9	1	0.1uF	GRM188R72A104KA35D	MuRata	CAP, CERM, 0.1 µF, 100 V, +/- 10%, X7R, 0603	0603
10	C10	1	1200uF	UHE1H122MHD6	Nichicon	CAP, AL, 1200 µF, 50 V, +/- 20%, TH	D18xL25mm
11	C11	1	0.1uF	GRM21BR72A104KAC4L	MuRata	CAP, CERM, 0.1 µF, 100 V, +/- 10%, X7R, 0805	0805
12	C13	1	220uF	UHE1V221MPD6	Nichicon	CAP, AL, 220 µF, 35 V, +/- 20%, TH	D10xL12.5mm
13	C15	1	2.2uF	GRM219R71C225KE15	MuRata	CAP, CERM, 2.2 µF, 16 V, +/- 10%, X7R, 0805	0805
14	C17	1	0.1uF	GRM219R71C104KA01D	MuRata	CAP, CERM, 0.1 µF, 16 V, +/- 10%, X7R, 0805	0805
15	D1	1	60V	B160-13-F	Diodes Inc.	Diode, Schottky, 60 V, 1 A, SMA	SMA

表 5. TIDA-03031 BOM (continued)

ITEM	DESIGNATOR	QTY	VALUE	PARTNUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
16	D2	1	28V	SMCJ28CA	Littelfuse	Diode, TVS, Bi, 28 V, 45.4 Vc, SMC	SMC
17	D4	1	Green	LTST-C190GKT	Lite-On	LED, Green, SMD	1.6x0.8x0.8mm
18	H1, H2, H3, H4	4		SJ-5303 (CLEAR)	3M	Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon
19	J1, J2	2		282841-2	TE Connectivity	Terminal Block, 2x1, 5.08mm, TH	10.16x15.2x9mm
20	L1	1	33uH	LPS6235-333MLB	Coilcraft	Inductor, Shielded Drum Core, Ferrite, 33 µH, 1.3 A, 0.18 ohm, SMD	LPS6235
21	L2	1	33uH	LPS8045B-333MRB	Coilcraft	Inductor, Shielded, Ferrite, 33 µH, 1.2 A, 0.121 ohm, SMD	8x4.5x8mm
22	R1, R4, R20	3	100k	CRCW0603100KFKEA	Vishay-Dale	RES, 100 k, 1%, 0.1 W, 0603	0603
23	R2	1	511k	CRCW0603511KFKEA	Vishay-Dale	RES, 511 k, 1%, 0.1 W, 0603	0603
24	R3, R6	2	715k	CRCW0603715KFKEA	Vishay-Dale	RES, 715 k, 1%, 0.1 W, 0603	0603
25	R5	1	165k	CRCW0603165KFKEA	Vishay-Dale	RES, 165 k, 1%, 0.1 W, 0603	0603
26	R7	1	226k	CRCW0603226KFKEA	Vishay-Dale	RES, 226 k, 1%, 0.1 W, 0603	0603
27	R8, R12	2	43.2k	CRCW060343K2FKEA	Vishay-Dale	RES, 43.2 k, 1%, 0.1 W, 0603	0603
28	R9, R13, R19	3	20.0k	CRCW060320K0FKEA	Vishay-Dale	RES, 20.0 k, 1%, 0.1 W, 0603	0603
29	R10, R16	2	10.0k	CRCW060310K0FKEA	Vishay-Dale	RES, 10.0 k, 1%, 0.1 W, 0603	0603
30	R11	1	40.2k	CRCW060340K2FKEA	Vishay-Dale	RES, 40.2 k, 1%, 0.1 W, 0603	0603
31	R14, R18	2	30.1k	CRCW060330K1FKEA	Vishay-Dale	RES, 30.1 k, 1%, 0.1 W, 0603	0603
32	R15	1	6.04k	CRCW06036K04FKEA	Vishay-Dale	RES, 6.04 k, 1%, 0.1 W, 0603	0603
33	R17	1	1.15k	CRCW06031K15FKEA	Vishay-Dale	RES, 1.15 k, 1%, 0.1 W, 0603	0603
34	S1	1		SKRKAEE010	Alps	Switch, Push Button, SMD	2.9x2x3.9mm SMD
35	TP1, TP2	2		5019	Keystone	Test Point, Miniature, SMT	Test Point, Miniature, SMT
36	U1	1		LM5160DNTR	Texas Instruments	Wide Input 65V, 1.5A Synchronous Step-Down DC-DC Converter, DNT0012B	DNT0012B
37	U2	1		TPS26600PWPR	Texas Instruments	4.5V-55V, 0.15A-2A, 150mOhm Industrial eFuse, PWP0016D	PWP0016D
38	U3	1		LM5002SD/NOPB	Texas Instruments	High Voltage Switch Mode Regulator, 8-pin LLP, Pb-Free	SDC08A
39	C16	0	0.1uF	GRM21BR72A104KAC4L	MuRata	CAP, CERM, 0.1 µF, 100 V, +/-10%, X7R, 0805	0805
40	D3	0	51V	SMAJ51CA	Littelfuse	Diode, TVS, Bi, 51 V, 400 W, SMA	SMA

表 5. TIDA-03031 BOM (continued)

ITEM	DESIGNATOR	QTY	VALUE	PARTNUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
41	FID1, FID2, FID3	0		N/A	N/A	Fiducial mark. There is nothing to buy or mount.	Fiducial

5.3 PCB Layout Recommendations

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-03031.

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-03031.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-03031.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-03031.

5.7 商標

6 About the Author

VENKATA NANDAM is systems application engineer at Texas Instruments, where he is responsible for supporting eFuse system solutions. He has eight years of broad experience in power management products development and application support. He earned his master's degree in electrical engineering from the Indian Institute of Technology, Kharagpur, INDIA.

TIの設計情報およびリソースに関する重要な注意事項

Texas Instruments Incorporated ("TI")の技術、アプリケーションその他設計に関する助言、サービスまたは情報は、TI製品を組み込んだアプリケーションを開発する設計者に役立つことを目的として提供するものです。これにはリファレンス設計や、評価モジュールに関係する資料が含まれますが、これらに限られません。以下、これらを総称して「TIリソース」と呼びます。いかなる方法であっても、TIリソースのいずれかをダウンロード、アクセス、または使用した場合、お客様(個人、または会社を代表している場合にはお客様の会社)は、これらのリソースをここに記載された目的にのみ使用し、この注意事項の条項に従うことに合意したものとします。

TIによるTIリソースの提供は、TI製品に対する該当の発行済み保証事項または免責事項を拡張またはいかなる形でも変更するものではなく、これらのTIリソースを提供することによって、TIにはいかなる追加義務も責任も発生しないものとします。TIは、自社のTIリソースに訂正、拡張、改良、およびその他の変更を加える権利を留保します。

お客様は、自らのアプリケーションの設計において、ご自身が独自に分析、評価、判断を行う責任がお客様にあり、お客様のアプリケーション(および、お客様のアプリケーションに使用されるすべてのTI製品)の安全性、および該当するすべての規制、法、その他適用される要件への遵守を保証するすべての責任をお客様のみが負うことを理解し、合意するものとします。お客様は、自身のアプリケーションに関して、(1) 故障による危険な結果を予測し、(2) 障害とその結果を監視し、および、(3) 損害を引き起こす障害の可能性を減らし、適切な対策を行う目的での、安全策を開発し実装するために必要な、すべての技術を保持していることを表明するものとします。お客様は、TI製品を含むアプリケーションを使用または配布する前に、それらのアプリケーション、およびアプリケーションに使用されているTI製品の機能性を完全にテストすることに合意するものとします。TIは、特定のTIリソース用に発行されたドキュメントで明示的に記載されているもの以外のテストを実行していません。

お客様は、個別のTIリソースにつき、当該TIリソースに記載されているTI製品を含むアプリケーションの開発に関連する目的でのみ、使用、コピー、変更することが許可されています。明示的または黙示的を問わず、禁反言の法理その他どのような理由でも、他のTIの知的所有権に対するその他のライセンスは付与されません。また、TIまたは他のいかなる第三者のテクノロジまたは知的所有権についても、いかなるライセンスも付与されるものではありません。付与されないものには、TI製品またはサービスが使用される組み合わせ、機械、プロセスに関連する特許権、著作権、回路配置利用権、その他の知的所有権が含まれますが、これらに限られません。第三者の製品やサービスに関する、またはそれらを参照する情報は、そのような製品またはサービスを利用するライセンスを構成するものではなく、それらに対する保証または推奨を意味するものでもありません。TIリソースを使用するため、第三者の特許または他の知的所有権に基づく第三者からのライセンス、もしくは、TIの特許または他の知的所有権に基づくTIからのライセンスが必要な場合があります。

TIのリソースは、それに含まれるあらゆる欠陥も含めて、「現状のまま」提供されます。TIは、TIリソースまたはその仕様に関して、明示的か暗黙的かにかかわらず、他のいかなる保証または表明も行いません。これには、正確性または完全性、権原、続発性の障害に関する保証、および商品性、特定目的への適合性、第三者の知的所有権の非侵害に対する黙示の保証が含まれますが、これらに限られません。

TIは、いかなる苦情に対しても、お客様への弁護または補償を行う義務はなく、行わないものとします。これには、任意の製品の組み合わせに関連する、またはそれらに基づく侵害の請求も含まれますが、これらに限られず、またその事実についてTIリソースまたは他の場所に記載されているか否かを問わないものとします。いかなる場合も、TIリソースまたはその使用に関連して、またはそれらにより発生した、実際的、直接的、特別、付随的、間接的、懲罰的、偶発的、または、結果的な損害について、そのような損害の可能性についてTIが知らされていたかどうかにかかわらず、TIは責任を負わないものとします。

お客様は、この注意事項の条件および条項に従わなかったために発生した、いかなる損害、コスト、損失、責任からも、TIおよびその代表者を完全に免責するものとします。

この注意事項はTIリソースに適用されます。特定の種類の資料、TI製品、およびサービスの使用および購入については、追加条項が適用されます。これには、半導体製品(http://www.ti.com/sc/docs/stdterms.htm)、評価モジュール、およびサンプル(http://www.ti.com/sc/docs/sampterms.htm)についてのTIの標準条項が含まれますが、これらに限られません。