参考資料

TI Designs: TIDA-01495
480W、薄型(17mm未満)、94%効率、高速過渡応答のAC/DC SMPSのリファレンス・デザイン

TEXAS INSTRUMENTS

概要

この薄型で、高速過渡応答のAC/DC SMPSのリファレンス・デザインは、UCC28063Aをベースとするフロントエンド、2フェーズのインターリーブ遷移モード(TM)力率補正(PFC)によって構成され、PFCインダクタの寸法を最小化できるほか、電磁気干渉(EMI)フィルタの要件を低減できます。UCC256303ヒステリシス制御ハイブリッドLLCコントローラは、HB-LLC絶縁DC/DC段を制御し、高速な過渡応答を保証するため、PFCバルクおよび出力コンデンサを小型化できます。PFC段での位相シェディングと、LLC段での高度なバースト・モード最適化機能により、5%負荷で高効率を実現できます(230V AC)。UCC24612マルチモード同期整流コントローラは、比例ゲート駆動を確立し、LLC段の出力整流器における伝導損失を減らすことで、高効率のデザインを実現します。

リソース

TIDA-01495	デザイン・フォルダ
UCC28063A	プロダクト・フォルダ
UCC256303	プロダクト・フォルダ
UCC24612	プロダクト・フォルダ
CSD19501KCS	プロダクト・フォルダ
TL431A	プロダクト・フォルダ
UCC28880	プロダクト・フォルダ
UCC27524	プロダクト・フォルダ

TI E2E™ Community

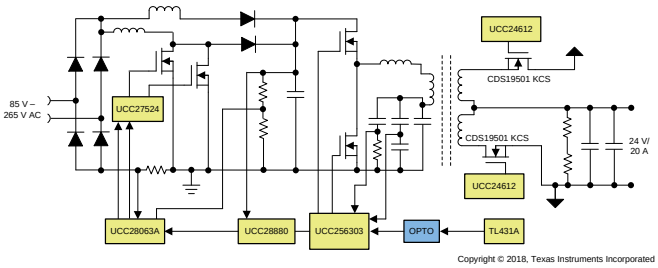
E2E™エキスパートに質問

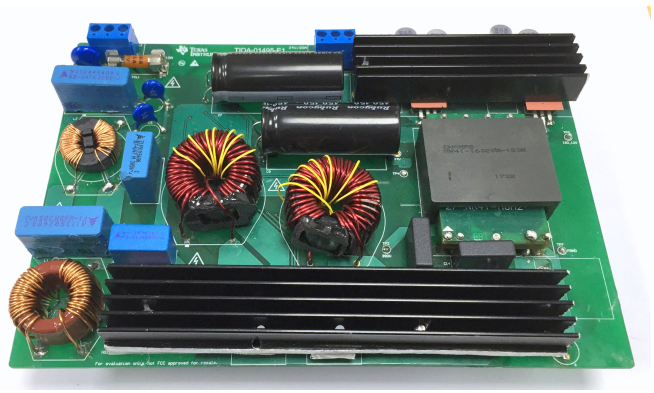
特長

- 薄型(高さ17mm未満)、PCBの外形185mm×110mmで、容積の制限されるアプリケーションに適切
- 全負荷効率93.3%超(230V AC)、91.1%超(115V AC)、ピーク効率94.1% (230V AC)および92% (115V AC)により、80+ Platinum標準に準拠
- PFC段の位相シェディング機能と、LLC段の高度なバースト・モード機能により、軽負荷状況で高効率を実現: 5%負荷で84%超(230V AC)、82%超(115V AC)
- LLCコントローラのZCS回避機能とOVPセンシング機能により堅牢性が向上し、システムを過電流、短絡、過電圧から保護して安全性を保証
- 0.99を上回る高い力率で、PFC規制およびIEC 61000-3-2 Class Aの電流THD規格に準拠
- EN55011 Class B伝導放射標準を満たす設計

アプリケーション

- 産業用AC/DC
- コンシューマ用AC/DC
- DINレール用の電源
- 医療用電源
- バッテリ充電器





1 System Description

This reference design is a thin-profile, 480-W, high-efficiency AC/DC power supply for use in space-constrained, high-power-density applications. The design consists of a two-phase-interleaved, critical conduction mode (CrCM) PFC converter, which operates from an input voltage range of 85-V to 265-V AC_{RMS} and generates a 390-V DC bus. The second stage comprises an isolated half-bridge (HB) LLC stage, which generates a 24-V, 20-A nominal output. This design demonstrates high-efficiency operation in a small form factor (185 × 110 × 17 mm) and delivers a continuous 480 W of power over the entire input operating voltage range from 85-V to 265-V AC. The design shows an efficiency greater than 93% for 230-V AC nominal operation and 91% for 115-V AC nominal operation.

The UCC28063A PFC integrated circuit (IC) controls the interleaved CrCM PFC stage. Interleaved critical conduction mode (CrCM) and continuous conduction mode (CCM) are the two popular topologies for PFC applications with greater than 300-W output power. CrCM PFC has the advantage of minimizing the turnon losses on the PFC MOSFET and eliminates the reverse recovery on the boost diode to reduce losses. CrCM PFC also has a much smaller inductor value than the CCM PFC. The reduced boost inductor value helps to develop the low-profile magnetics necessary for meeting the thin-profile requirement in the design. By interleaving two CrCM power stages, the effective input ripple current is reduced and helps to minimize the EMI filter requirement. The HB-LLC power stage is controlled through the stage of the art UCC256303 resonant controller which implements current mode control for increased control bandwidth. This increased control bandwidth reduces the PFC bulk and output capacitors required to suppress the AC ripple on the output. To achieve high efficiency, the output of the LLC stage uses synchronous rectification based on the UCC24612 device and the CSD19501KCS MOSFET.

The design has low standby power of < 400 mW and meets ENERGY STAR rating requirements as well as 2013 EU eco-design directive ErP Lot 6. The EMI filter is designed to meet EN55011 class-B conducted emission levels. The design is fully tested and validated for various parameters such as regulation, efficiency, EMI signature, output ripple, start-up, and switching stresses. Overall, the design meets the key challenges of industrial power supplies to provide safe and reliable power with all protections built-in, while delivering high performance with low power consumption and low bill-of-material (BOM) cost.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CONDITIONS						
Input voltage	V_{INAC}		85	230	265	V AC
Frequency	f_{LINE}		47	50	63	Hz
No load power	PSB			400		mW
OUTPUT CONDITIONS						
Output voltage				24		V
Output current				20		A
Line regulation		Both current and voltage			0.5%	
Load regulation		Both current and voltage			1%	
Output voltage ripple		Peak to peak		200		mV
Output power (nominal)	P_O				480	W
SYSTEM CHARACTERISTICS						
Efficiency	H	V_{IN} = 230-V AC_{RMS} and full load at 24-V output		93.5%		
		V_{IN} = 115 AC_{RMS} and 230-W load at 24-V output		91.4%		
Protections	Output overcurrent			25		A
	Output overvoltage			30		V
Operating ambient	Open frame	–10	25		55	C
Standards and norms	Power line harmonics	As per EN55011 / EN55022 Class B				
	Conducted emissions	EN55022 Class B				
	EFT	As per IEC-61000-4-4				
	Surge	As per IEC-61000-4-5				
Board form factor (FR4 material, two-layer)	Length × breadth × height	180 mm × 110 mm × 17 mm				mm

2 System Overview

2.1 Block Diagram

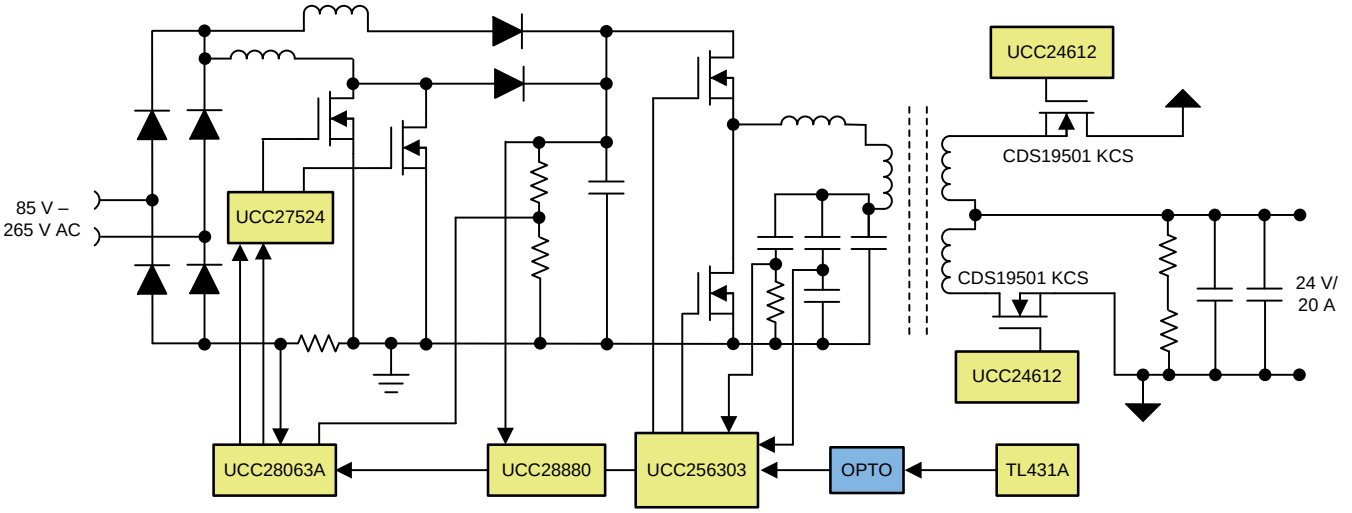


図 1. TIDA-01495 Block Diagram

2.2 Highlighted Products

2.2.1 UCC28063A

The UCC28063A is a two-phase, naturally-interleaved, transient-mode power factor correction (PFC) controller for implementing a high-efficiency, low-component-count, front-end AC/DC PFC stage. The two-phase interleaved power stage reduces the filter requirements for input current ripple electromagnetic interference (EMI).

The natural interleaving technique of the UCC28063A ensures that both phases operate at high efficiency while synchronized to the same switching frequency. The integrated brownout and dropout handling feature, the inrush-safe current limiting feature combined with the overvoltage protection, and the overcurrent protection feature increase the robustness of the PFC stage.

2.2.2 UCC256303

Series resonant converters like LLC are one of the most widely used topologies for implementing medium-to-high power isolated DC/DC power stages in consumer and industrial power supplies. LLC resonant converters are quite popular due to their ability to achieve soft-switching (ZVS turnon) for high-voltage MOSFETs, thereby improving the overall efficiency of a system.

The UCC256303 has a unique, hybrid hysteretic control that provides excellent line and load transient response, minimizing the requirement for output filter capacitors. The wide frequency range of the device can be used to reduce the PFC bulk capacitor required to meet the holdup time requirement in the industrial power supplies. With the integrated high-voltage gate drive, X-Cap discharge function, and additional output overvoltage protection, the UCC256303 reduces the amount of external discreet components required to implement a high-efficiency industrial power supply.

2.2.3 UCC24612-2

The UCC24612-2 is a multi-mode synchronous rectifier controller for active clamp flyback and LLC applications. Along with its 4-A sink and 1-A source capability, this device has a proportional gate drive, which helps when using this synchronous rectifier in LLC applications where the system can operate far above the resonant frequency. The adaptive off-time feature adds robustness to the synchronous rectifier by preventing false triggering.

2.2.4 CSD19501KCS

The CSD19501KCS is an 80-V NexFET™ power MOSFET, with 5.5-mΩ resistance and 38-nC gate charge. In this reference design, the CSD19501KCS is used as the synchronous field-effect transistor (FET) to lower the losses in the output stage of the LLC converter.

2.3 System Design Theory

This reference design provides a universal AC mains-powered, 480-W nominal output at 24 V and 20 A. This design comprises a front-end AC/DC PFC power stage followed by an isolated DC/DC LLC power stage.

2.3.1 PFC Regulator Stage Design

For high power levels such as 500 W, either the single-phase CCM PFC or interleaved CrCM PFC is the preferred topology for implementing PFC. Interleaved CrCM PFC offers certain advantages at these power levels because it ensures valley switching for the PFC MOSFET and ZCS turnoff diode, which reduces the losses in the PFC stage. Cheaper diodes can be used because the PFC diode does not have a hard turnoff. CrCM PFC requires a smaller PFC inductor. By interleaving two CrCM power stages, the overall input ripple current is also reduced. Alternatively, CCM PFC requires a larger inductor and is not very effective in low-profile designs.

This reference design uses the UCC28063A-based interleaved CrCM PFC. The following subsections detail the design process and component selection.

2.3.1.1 Design Parameters

表 2. Design Parameters for PFC Power Stage Design

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
INPUT					
V_{IN}	Input voltage	85		265	V AC
f_{LINE}	Input frequency	47		63	Hz
OUTPUT					
V_{OUT}	Output voltage		397		V DC
$P_{OUT(nom)}$	Output power			500	W
	Line regulation			5%	
	Load regulation			5%	
PF	Targeted power factor		0.99		
η	Targeted efficiency		97.3%		
iTHD	Targeted input current THD		5%		

2.3.1.2 Input Current Calculations

The input fuse, bridge rectifier, and input capacitor are selected based on the input current calculations. First, determine the maximum average output current, $I_{OUT(max)}$:

$$I_{OUT(max)} = \frac{P_{OUT(max)}}{V_{OUT(max)}} \quad (1)$$

$$I_{OUT(max)} = \frac{500}{390} = 1.28\ A \quad (2)$$

Calculate the maximum input root mean square (RMS) for the line current, $I_{INrms(max)}$, using the parameters from the *Key System Specifications* and the initial assumptions of the efficiency and power factor:

$$I_{INrms(max)} = \frac{P_{OUT(max)}}{\eta \times V_{IN(min)} \times PF} \quad (3)$$

$$I_{INrms(max)} = \frac{500}{0.94 \times 85 \times 0.99} = 6.32\ A \quad (4)$$

2.3.1.3 Boost Inductor

Calculate the boost inductor using the minimum input voltage and the minimum desired frequency of operation. First calculate the duty cycle, $DUTY_{(max)}$, at the peak of the minimum input voltage:

$$DUTY_{(max)} = \frac{\left(V_{OUT(nom)} - V_{INrms(min)} \times \sqrt{2}\right)}{V_{OUT(nom)}} \quad (5)$$

$$DUTY_{(max)} = \frac{390 - (1.414 \times 85)}{390} = 0.691 \quad (6)$$

式 7 calculates the boost inductor value.

$$L1 = L2 = \frac{\left(\eta \times \left(V_{INrms(min)}\right)^2 \times DUTY_{(max)}\right)}{\left(P_{OUT(max)} \times F_{MIN}\right)} \quad (7)$$

$$L1 = L2 = \frac{0.95 \times 85^2 \times 0.69}{500 \times 50000} = 195\ \mu H \quad (8)$$

The actual value of the boost inductor used is 210 µH. Calculate the required saturation current for the boost inductor is calculated using 式 9 for the minimum input voltage and under the assumption that both phases equally share the load.

$$I_{L(max)} = \left(\sqrt{2} \times \frac{P_{OUT(max)}}{V_{INrms(min)}}\right) = 8.3\ A \quad (9)$$

2.3.1.4 Output Capacitor

For this application, choose the output capacitor such that the output ripple is kept below 25 V_{PK-PK}. 式 10 calculates the output capacitor.

$$C_{OUT} \geq 2 \times P_{OUT(max)} \times \frac{1}{V_{OUT} \times 4 \times \pi \times F_{LINE} \times V_{PFCRipple}} \quad (10)$$

$$C_{OUT} \geq 2 \times 500 \times \frac{1}{390 \times 4 \times \pi \times 47 \times 25} = 182.4\ \mu F \quad (11)$$

In this reference design, two low-profile 100-µF capacitors are connected in parallel to form the PFC bulk capacitor.

2.3.1.5 Current Sense Resistor

The current sense resistor detects the sum of the inductor currents through both phases. The overcurrent protection limit in UCC28063A is 200 mV. The required value of the current sense resistor is calculated for the lowest input voltage and a 25% overload condition. Estimate the peak current first (式 12) before calculating the current sense resistor:

$$I_{PEAK_{CS}} = \frac{2 \times \sqrt{2} \times P_{OUT(max)} \times 1.25}{\eta \times V_{INrms(min)}} \quad (12)$$

$$I_{PEAK_{CS}} = \frac{2 \times \sqrt{2} \times 500 \times 1.25}{0.95 \times 85} = 21\,A \quad (13)$$

This result gives the value of the current sense resistor as:

$$Rcs = \frac{200\,mV}{21\,A} \cong 9\,m\Omega \quad (14)$$

This reference design uses two 18-mΩ resistors in parallel.

2.3.1.6 PFC MOSFET

式 15 calculates the RMS current through the PFC MOSFET.

$$IDS_{rms} = \left(\frac{I_{PEAK_{CS}}}{2}\right) \times \sqrt{\frac{\frac{1}{6} - \left(4\sqrt{2} \times V_{INrms(min)}\right)}{9\pi \times V_{OUT_{PFC}}}} \quad (15)$$

$$IDS_{rms} = 3.715\,A \quad (16)$$

Select a MOSFET with a low figure of merit for this application. To maintain the overall height of the design to less than 17 mm, the PFC stage has been designed to switch at high frequency. The key MOSFET specifications that are important for minimizing losses in this design are:

- Low R_{DSon}, for reducing the conduction losses in the MOSFET
- Low Q_G, for fast turnoff

2.3.1.7 PFC Diode

式 17 calculates the RMS current through the boost diode.

$$ID_{rms} = \left(\frac{I_{PEAK_{CS}}}{2}\right) \times \sqrt{\frac{\left(4\sqrt{2} \times V_{INrms(min)}\right)}{9\pi \times V_{OUT_{PFC}}}} = 2.26\,A \quad (17)$$

2.3.1.8 Brownout Protection Configuration

The brownout voltage in UCC28063A can be set through the potential divider on the VINAC pin. In this reference design, the brownout voltage is set to 70 V with a hysteresis of 12 V. The following equations determine the value of the resistors in the potential divider network. R_A refers to the top three resistors in the potential divider (式 18) and R_B refers to the bottom resistor in the potential divider (式 19).

$$R_A = 12 \times \frac{1.414}{I_{BOHYS}} = \frac{17}{2 \times 10^{-6}} = 8.5\,M\Omega \quad (18)$$

Three resistors of 2.87 MΩ are connected in series to form R_A, with the bottom resistor using 式 19.

$$R_B = \frac{1.4 \times R_A}{70\sqrt{2} - 1.414} = 123.5\ K \tag{19}$$

A standard value of 123 k is chosen for RB.

2.3.1.9 Control Loop Compensation

This design uses a type-2 compensator for the voltage loop compensation. Resistor R67 and capacitors C63 and C65 form the compensator. Start with a value of 7.5 K for R67. Place a zero close to 10 Hz to give a phase boost close to the gain crossover frequency. This zero is formed by R67 and C63.

$$C63 = \frac{1}{2\pi \times 10 \times 7500} = 2.12\ \mu F \tag{20}$$

Choose a 2.2-µF capacitor for the C63 capacitor.

Place a pole at a frequency much lower than the lowest switching frequency, around 20 KHz, to attenuate the switching noise. This pole is formed by R67 and C65.

$$C65 = \frac{1}{2\pi \times 20000 \times 7500} = 1.06\ nF \tag{21}$$

Choose a 1-nF capacitor for C65.

2.3.1.10 Programming VOUT and HVSEN

The VOUT pin sets the output voltage regulation point. To minimize the no-load losses, use high-value resistances to construct this potential divider network. Use three 3.01-MΩ resistors to form the top resistor (R_C) in the potential divider. Calculate the bottom resistor (R_D) using 式 22.

$$R_D = V_{REF} \times \frac{R_C}{V_{OUT(nom)} - V_{REF}} = \frac{6 \times 9 \times 10^6}{390 - 6} = 140.6\ k\Omega \tag{22}$$

Use a value of 142 kΩ for R_D.

This reference design uses the HVSEN pin to set the fail-safe output overvoltage protection (OVP). Three 3.01-MΩ resistors form the top resistor (R_E) in the potential divider. Calculate the bottom resistor (R_F) using 式 23.

$$R_F = \frac{4.87 \times R_E}{V_{OUT(pk)} - 4.87} = \frac{4.87 \times 9 \times 10^6}{450 - 4.87} = 98.46\ k\Omega \tag{23}$$

Use a value of 97.6 kΩ for R_F.

2.3.2 LLC Converter Stage Design

Increased demands for high-power-density power supplies have resulted in the increase in switching frequency of the converters designed. While component sizes tend to decrease with an increase in the switching frequency, device switching losses (which are proportional to frequency) have significantly increased contributing to resulting in significant efficiency loss. Resonant converters use soft-switching techniques to alleviate switching loss problems and attain high efficiencies. Further, soft-switching helps attain low losses during light load conditions, very-low device stress, and reduced EMI.

The LLC resonant converter is based on the series resonant converter (SRC). By utilizing the transformer magnetizing inductor, zero-voltage switching can be achieved over a wide range of input voltage and load. As a result of multiple resonances, zero-voltage switching can be maintained even when the switching frequency is higher or lower than the resonant frequency.

In this design, the LLC converter operates at a high nominal switching frequency of around 180 kHz. This allows to minimize the dimension of the LLC transformer to meet the low profile requirements. The converter achieves the best efficiency when operated close to its resonant frequency at a nominal input voltage. As the switching frequency is lowered, the voltage gain is significantly increased. This allows the converter to maintain regulation when the input voltage falls low. These features make the converter ideally suited to operate from the output of a high-voltage boost PFC pre-regulator, allowing it to hold up through brief periods of AC line-voltage dropout.

With its hybrid hysteretic control and ZCS avoidance feature, the UCC256303 LLC controller enables safe operation of the LLC power stage while minimizing the dimension of the output capacitors. In addition, the controller delivers complete system protection functions including overcurrent, undervoltage lockout (UVLO), and overvoltage protection (OVP).

表 3 lists the design parameters for the LLC power stage design.

表 3. Design Parameters for LLC Power Stage Design

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
INPUT					
V_{INDC}	Input voltage	250	397	410	V DC
OUTPUT					
V_{OUT}	Output voltage		24		V DC
P_{OUT}	Max output power		480		W
f_{SW_nom}	Nominal switching frequency		180		kHz
	Line regulation		1		%
	Load regulation		1		%
η	Targeted efficiency		0.965		

2.3.2.1 Determine LLC Transformer Turns Ratio N

The LLC tank is designed to have a nominal gain, M_g, of 1 at the resonant frequency. Use 式 24 to estimate the required turns ratio.

$$n = M_g \times \frac{\frac{V_{DCIN(nom)}}{2}}{V_O + V_F} : M_g = 1 \quad (24)$$

where

- M_g is the voltage gain,
- $V_{DCIN(nom)}$ is the nominal PFC output,
- V_O is the output voltage,
- V_F is the voltage drop across the synchronous rectifier.

From the specifications, the nominal values for input voltage and output voltage are 390 V and 24 V, respectively. Assuming an average drop of 100 mV on the synchronous rectifier, the turns-ratio can be calculated as:

$$n = 1 \times \left(\frac{390}{24 + 0.1} \right) = 8.07 \tag{25}$$

The transformer turns ratio is set to 8.

2.3.2.2 Determine M_{g_min} and M_{g_max}

Determine M_{g_min} and M_{g_max} using 式 26 and 式 27, respectively.

$$M_{g\_min} = n \times \frac{(V_O + V_F)}{\frac{V_{DCIN(max)}}{2}}$$

$$M_{g\_min} = 8.0 \times \left(\frac{24.1\,V}{\frac{410\,V}{2}} \right) = 0.94 \tag{26}$$

$$M_{g\_max} = n \times \left(\frac{V_{0(nom)} + V_F}{\frac{V_{DCIN(min)}}{2}} \right)$$

$$M_{g\_max} = 8.0 \times \left(\frac{24.1\,V}{\frac{310\,V}{2}} \right) = 1.285 \tag{27}$$

The dimensioned M_{g_max} is increased to 1.1 times the required value to have some margin = M_{g_max} = 1.1 × 1.28543 ≈ 1.426.

2.3.2.3 Determine Equivalent Load Resistance (R_e) of Resonant Network

式 28 calculates the equivalent load resistance at nominal and peak load under nominal output voltage and peak output voltage.

$$R_e = \frac{8 \times n^2}{\pi^2} \times \left(\frac{V_{O\_nom}}{I_{O\_nom}} \right) \tag{28}$$

$$R_{e\_nom} = \frac{8 \times 8^2}{\pi^2} \times \left(\frac{24}{20} \right) = 62.31\,\Omega \tag{29}$$

2.3.2.4 Select Lm and Lr ratio (Ln) and Qe

Set the resonance point for the LLC converter close to 180 kHz to minimize the dimension of the LLC transformer set. The operating point of the LLC power stage is close to this frequency during a full load condition. Choose a value of Lr = 15 µH and Cr = 66 nF to calculate the value of the resonant frequency as follows:

$$Fr = \frac{1}{2 \times \pi \times \sqrt{(Lr \times Cr)}} = 176\ kHz \tag{30}$$

The magnetizing inductance to resonant inductance ratio is chosen as 6:10.5 to develop a sufficient Q while simultaneously minimizing the magnetizing current in the LLC transformer. A planar core has been used to realize the LLC transformer. The required leakage inductance is provided through an additional shim inductor.

図 2 shows the Q curves for this design at full load conditions.

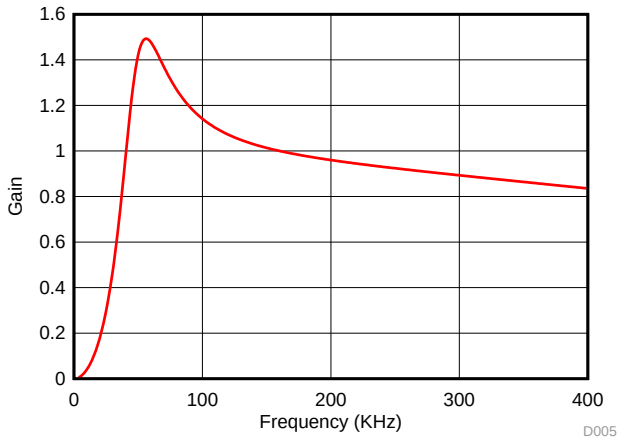


図 2. Q Curve at Full Load and Nominal Output Voltage

2.3.2.5 Determine Primary-Side Currents

Use 式 31 to calculate the primary-side RMS load current (I_{pri}) at a full load condition:

$$I_{pri} = \frac{\pi}{2\sqrt{2}} \times \left(\frac{I_{O(nom)}}{n} \right) \tag{31}$$

$$I_{pri} = 1.11 \times \left(\frac{20}{8.0} \right) = 2.775\,A \tag{32}$$

As calculated in 式 33, the RMS magnetizing current (I_m) at f_{SW_min} = 100 kHz is:

$$I_m = \left(\frac{2\sqrt{2}}{\pi} \right) \times \left(n \times \frac{V_{O(nom)} + V_f}{2 \times \pi \times f_{SW\_min} \times L_M} \right) \tag{33}$$

$$I_m = \left(\frac{2\sqrt{2}}{\pi} \right) \times \left(\frac{8.0 \times 24}{2 \times \pi \times 100\,kHz \times 150\,\mu H} \right) = 1.84\ A \tag{34}$$

式 35 calculates the resonant circuit current (I_r):

$$I_r = \sqrt{I_m^2 + I_{pri}^2} \tag{35}$$

$$I_r = \sqrt{2.775^2 + 1.84^2} = 3.373\ A \tag{36}$$

This value is also equal to the transformer primary winding current at f_{SW_min}.

2.3.2.6 Determine Secondary-Side Currents

The secondary-side RMS currents can be calculated from the average load current. Assuming the LLC power stage is operating close to its second resonant frequency, the RMS current through each rectifier in the secondary-side push-pull output is calculated in 式 37:

$$I_{sec\_rms} = I_{sec} \times \frac{\pi}{4} = 15.7\ A \tag{37}$$

where,

- I_{sec} is the full-load, secondary-side output current (equal to 20 A).

2.3.2.7 Primary Side MOSFETs

Consider each MOSFET to have an input voltage equal to its maximum applied voltage. A MOSFET with a maximum drain source voltage greater than 500 V is feasible for this design. The turnon losses can be neglected for an LLC power stage working in ZVS. Choose the MOSFET based on the values for R_{DSon} and C_{OSS}. Optimizing the C_{OSS} helps to minimize the dead time required for achieving ZVS, thereby minimizing the duty cycle loss. This reference design uses the STP24N60M2 MOSFET. The adaptive dead-time optimization feature of the UCC256303 helps to maximize the duty cycle, which improves the efficiency.

2.3.2.8 Secondary-Side Synchronous MOSFETs

式 38 calculates the synchronous rectifier maximum voltage rating.

$$V_{DSmax\_sec} = 1.2 \times 2 \times V_{O(nom)} = 57.6\ V \tag{38}$$

The current rating of the MOSFET is determined as I_{sec_Mrms} = 15.7 A.

This reference design uses TI's CSD19501KCS with its low R_{DSon} (< 5.5 mΩ) and Q_g (< 38 nC). The very-low R_{DSon} of the device helps to reduces the overall loss in the synchronous rectifier.

2.3.2.9 Soft Start—UCC256303

The UCC256303 is configured to provide a maximum 400-ms soft-start period. During start-up the soft-start capacitor charges using the internal 25-µA current source. The UCC256303 exits soft start when the closed-loop control takes over or when the voltage on the soft-start capacitor reaches 7 V. Select the value of the soft-start capacitor using 式 39.

$$C_{SS} = C31 = 400\ mS \times \frac{25\ \mu A}{7\ V} = 1.5\ \mu F \tag{39}$$

2.3.2.10 Current Sense Circuit (ISNS Pin)—UCC256303

The overcurrent limit OCP3 is set to trigger at 1.2 times the peak overload capability of the system.

$$V_{ISNSFullload} = \frac{OCP3}{1.2} = \frac{0.6}{1.2} = 0.5\ V \tag{40}$$

The current sense ratio is then calculated as:

$$K_{ISNS} = \frac{V_{ISNSFullload}}{\left(\frac{P_{OUT(max)}}{\eta}\right) \times \left(\frac{1}{V_{DCIN(nom)}}\right)} = \frac{0.5}{(500) \times \left(\frac{1}{390}\right)} = 0.39\ \Omega \tag{41}$$

Select the current sense capacitor C_{ISNS} = C39 = 150 pF. 式 42 calculates the current sense resistor R_{ISNS}.

$$R_{ISNS} = R14 = K_{ISNS} \times \frac{C_r}{C_{ISNS}} = 0.39 \times \frac{66 \times 10^{-9}}{150 \times 10^{-12}} = 171\ \Omega \tag{42}$$

Use a 169-Ω resistor for R14.

2.3.2.11 Overvoltage Protection (BW Pin)—UCC256303

The BW pin senses the output voltage through the bias winding mounted on the LLC transformer. This pin can be used to provide an additional OVP in the system. In this reference design, the bias winding has the same number of turns as the secondary winding. When the OVP voltage is set to 32 V, the bias winding voltage will be 32 V. After implementing this setting, the BW pin potential divider is configured in such a way that it acknowledges the 4 V at the 32-V output.

Select $R_{BWLOWER}$ = R18 = 10 kΩ. 式 43 then calculates the $R_{BWUPPER}$ as follows.

$$R_{BWUPPER} = R20 = R18 \times \frac{32\ V - 4\ V}{4\ V} = 70\ k \tag{43}$$

Use a 69.8-kΩ resistor for R18.

3 Hardware, Testing Requirements, and Test Results

3.1 Requirement for Testing

3.1.1 Test Conditions

- Input conditions:
  - V_{IN}: 85-V to 265-V AC
  - I_{IN}: Current limit to 8 A
- Output conditions:
  - V_{OUT}: 24 V
  - I_{OUT}: 0 A to 20 A

3.1.2 Required Equipment

- Isolated AC source
- Single-phase power analyzer
- Digital oscilloscope
- Multimeters
- Electronic load
- 12-V DC fan

3.1.3 Procedure

1. Turn on the 12-V DC fan and set the current to obtain approximately 200 LFM airflow on the board.
2. Connect the input terminals (connector J3) of the reference board to the AC power source.
3. Connect the output terminals (connector J2) to the electronic load, maintaining correct polarity.
4. Set a minimum load of approximately 50 mA.
5. Gradually increase the input voltage from 0 V to turn on a voltage of 85-V AC. As the voltage across the PFC bulk capacitor crosses 90 V, the LLC section begins working and supplies the auxiliary power to the PFC controller. At this point, the PFC starts and boosts the PFC stage output voltage to 390-V DC.
6. Observe the start-up conditions for smooth switching waveforms.
7. Apply a load and perform tests to determine the efficiency, obtain regulation data, and observe steady-state operating conditions.

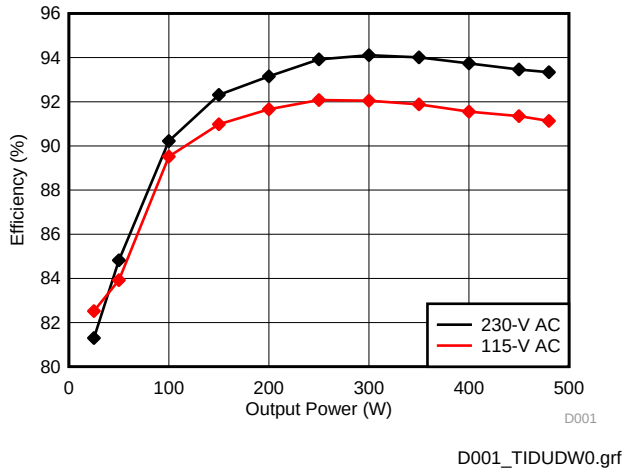
3.2 Test Results

3.2.1 Efficiency, Regulation, PF, and iTHD

This section shows the efficiency, power factor, regulation, and iTHD results at 115-V AC and 230-V AC input. 表 4 gives the test data.

表 4. Test Results for 115-V AC and 230-V AC Input

P_{OUT} (W)	EFFICIENCY (%) AT 115-V AC	EFFICIENCY (%) AT 230-V AC	PF AT 115-V AC	PF AT 230-V AC	iTHD (%) AT 115-V AC	iTHD (%) AT 230-V AC	% REGULATION AT 115-V AC	% REGULATION AT 230-V AC
25	82.51507128	81.29950053	0.9481	0.7	23.09	33	0.57	0.62
50	83.9242486	84.81680385	0.9727	0.866	17.2	27.2	0.54	0.55
100	89.52061765	90.22170067	0.9884	0.964	11.19	16.8	0.05	0.38
150	90.97905138	92.31231215	0.992	0.9755	8.7	15.7	0	–0.05
200	91.65701754	93.15128193	0.995	0.981	7.27	14.06	–0.08	–0.1
250	92.07668415	93.92470822	0.996	0.985	6.37	12.5	–0.1	–0.06
300	92.04876775	94.11389092	0.997	0.988	5.75	11.3	–0.14	–0.12
350	91.87753864	94.01469237	0.997	0.9899	5.53	10.88	–0.25	–0.22
400	91.55421377	93.74407263	0.997	0.991	5.39	9.67	–0.39	–0.35
450	91.35421377	93.45708653	0.998	0.992	5.42	9.06	–0.44	–0.4
480	91.12785237	93.34447384	0.998	0.992	5.31	8.97	–0.44	–0.42



D001_TIDUDW0.grf

図 3. Efficiency Data

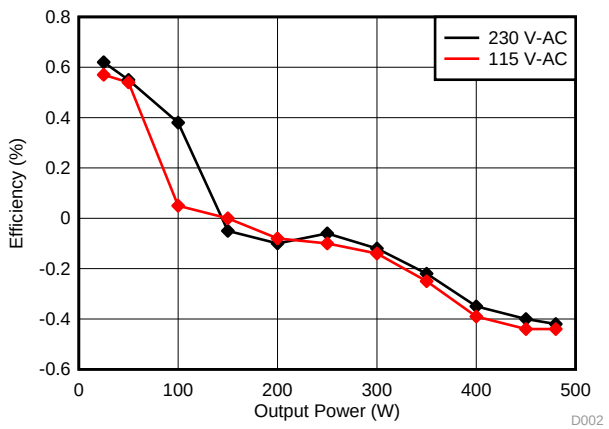


図 4. Load Regulation Data

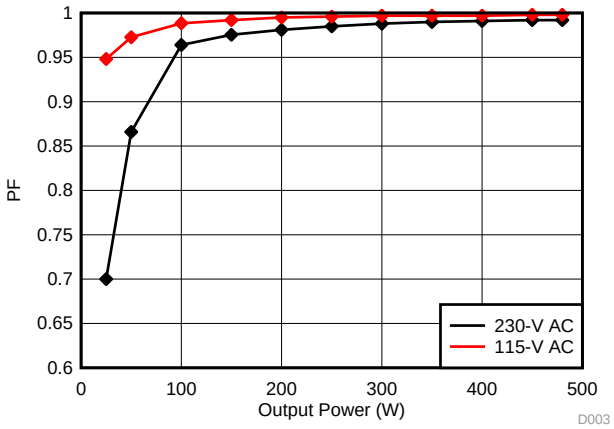


図 5. Power Factor Data

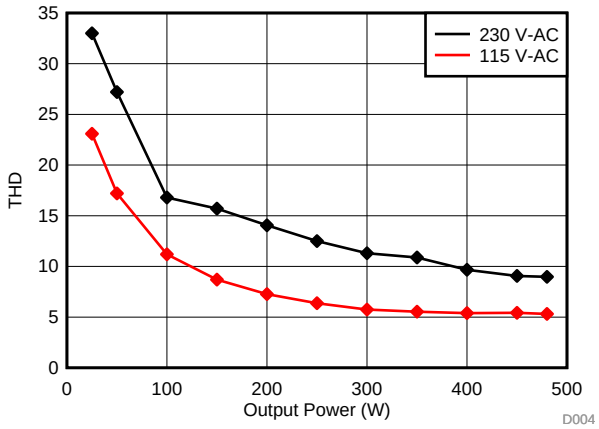


図 6. iTHD Data

3.2.2 Inrush Current Limiting at Start-Up

図 7 shows the inrush current at start-up. The inrush current is limited through an active inrush limiter circuit in series with the bulk capacitor.

図 7. Inrush Current Limiting at Start-Up

3.2.3 PFC Start-Up Waveform

図 8 shows the full-load start-up waveform. The input current reaches the steady-state value in the first few cycles.

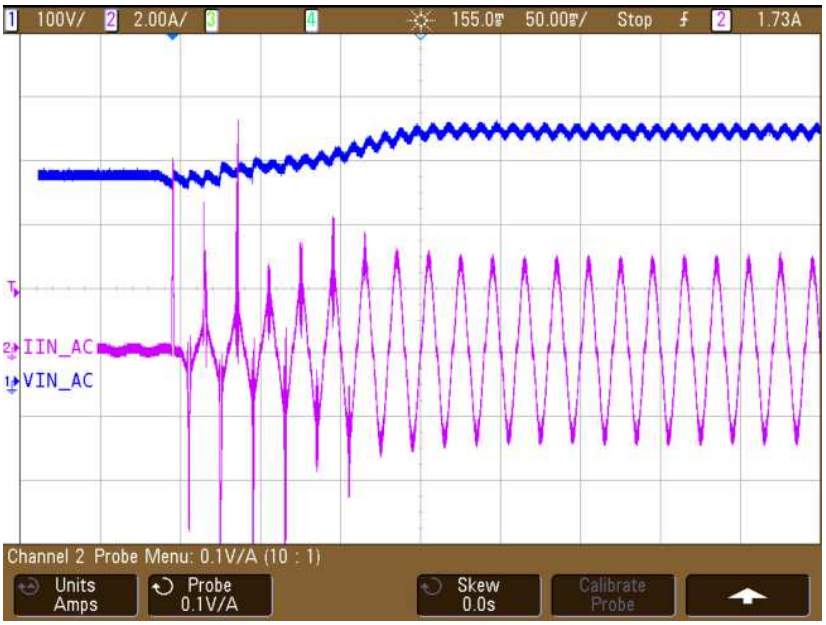


図 8. Full Load Start-Up Waveform at 230-V AC Input

3.2.4 Load Transient Response

図 9 shows the load transient response of the system when the 24-V output load current step changes from 20% to 100% with a slew rate of 500 mA/µs.

図 9. Load Transient Response

3.2.5 Output Voltage Ripple

図 10 shows the output voltage ripple at the 24-V output at full load.

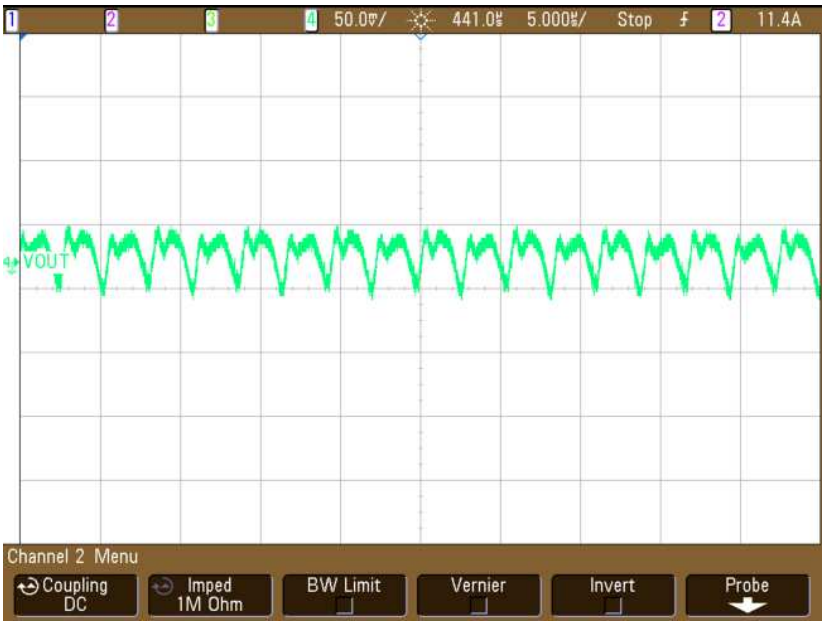


図 10. Output Voltage Ripple at Full Load

3.2.6 PFC Working Waveforms

This subsection shows the PFC input and switching waveforms. 図 11 shows the input voltage and input current at a 230-V AC input and full-load output.

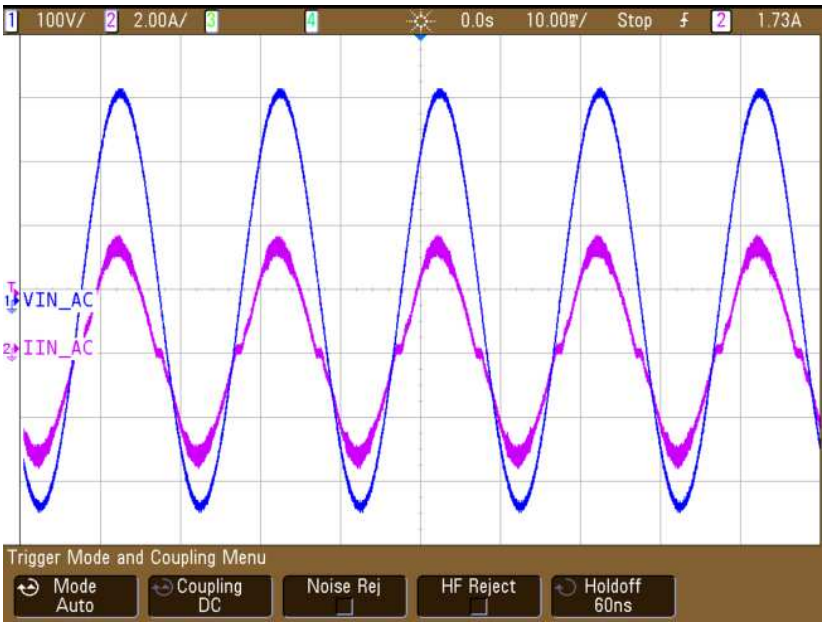


図 11. PFC Input Voltage and Current Waveform

図 12 shows the PFC switching waveform for phase 1. The MOSFET drain source voltage, gate source voltage, and the ZCD winding voltage has been captured. Note how the PFC MOSFET turns at the valley point, thus ensuring the lowest turnon loss.

図 12. PFC MOSFET Switching Waveform

3.2.7 LLC Working Waveform

図 13 shows the LLC switching waveforms. The primary high-voltage MOSFET drain source voltage, gate source voltage, and the resonant tank current have been captured.

図 13. LLC Stage MOSFET Switching Waveform

3.2.8 Synchronous Rectifier Waveform

This subsection shows the UCC24612 synchronous rectifiers drive output along with the current through the synchronous rectifier MOSFET. When the current begins to flow through the body diode of the synchronous MOSFET, the synchronous rectifier turns on the channel within 170 ns; 図 14 shows this result.

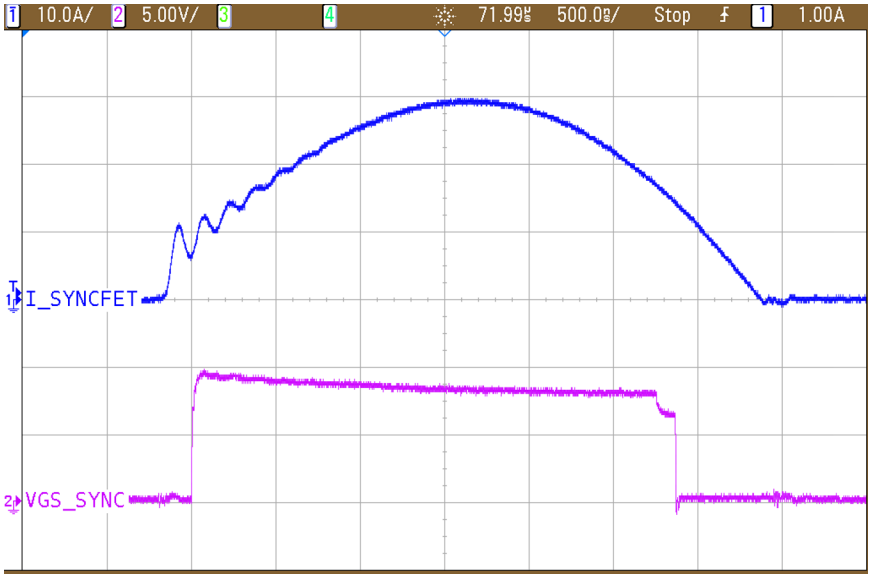


図 14. Synchronous Rectifier Working Waveform

3.2.9 Full-Load Thermal Image

図 15 and 図 16 show the full-load thermal image at a 230-V AC input. The thermal image was recorded after running the board for 20 minutes. This thermal image was recorded using forced air cooling with a 200-LFM airflow.

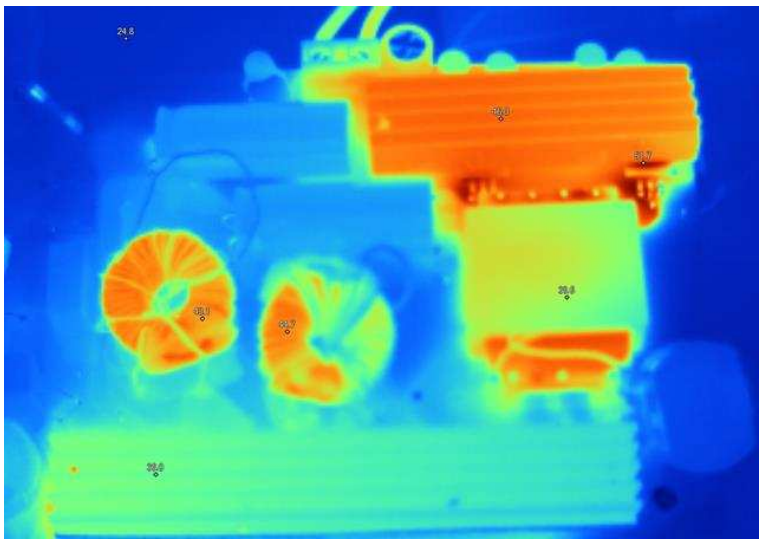


図 15. Thermal Image Captured at 230-V AC Input and Full Load Output (Top View)

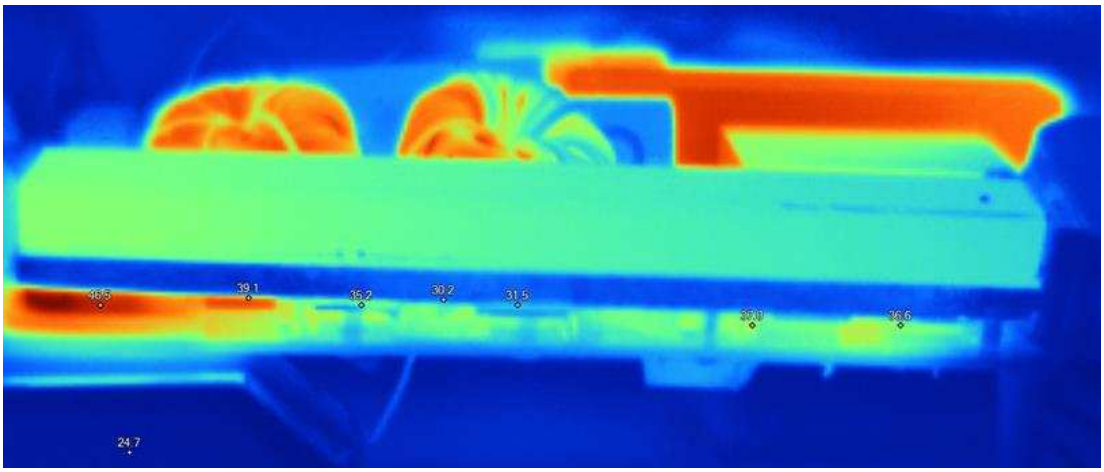


図 16. Thermal Image Captured at 230-V AC Input and Full Load Output (Side View)

表 5 lists the temperatures at different points on the board.

表 5. Temperature of Various Components on Board

COMPONENT	TEMPERATURE
Diode bridge	46.8°C
PFC MOSFET	39.1°C, 35.2°C
PFC diode	31.5°C, 30.2°C
PFC inductor	48.1°C, 46.7°C
LLC MOSFET	46.2°C, 46.4°C
LLC synchronous rectifier	56.9°C, 52.5°C

表 5. Temperature of Various Components on Board (continued)

COMPONENT	TEMPERATURE
LLC transformer	38.8°C

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01495.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01495.

4.3 PCB Layout Recommendations

Refer to the UCC256303, UCC28063A, and UCC24612-2 data sheets for detailed layout recommendations.

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01495.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01495.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01495.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01495.

5 商標

6 About the Author

RAMKUMAR S is a systems engineer at Texas Instruments, where he is responsible for developing reference design solutions for the industrial segment. Ramkumar brings his diverse experience in analog and digital power supplies design to this role. Ramkumar earned his master of technology (M.Tech) from the Indian Institute of Technology in Delhi.

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