参考資料

TI Designs: TIDA-01610
車載オーディオ・アンプ用トラッキング電源のリファレンスデザイン

TEXAS INSTRUMENTS

概要

このリファレンス・デザインは、10Aの2相昇圧コンバータを実装します。出力電圧は、16V～40V DCの範囲で動的に設定可能です。この出力電圧範囲により、PWM信号または電圧により供給されるオーディオ信号をトラッキングできます。

リソース

TIDA-01610	デザイン・フォルダ
LM25122-Q1	プロダクト・フォルダ

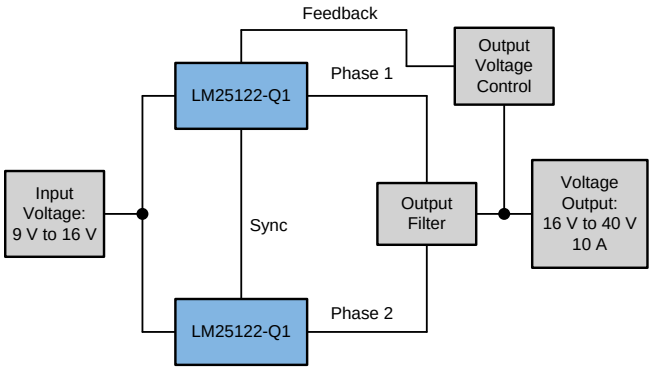
TI E2E™ Community　E2E™エキスパートに質問

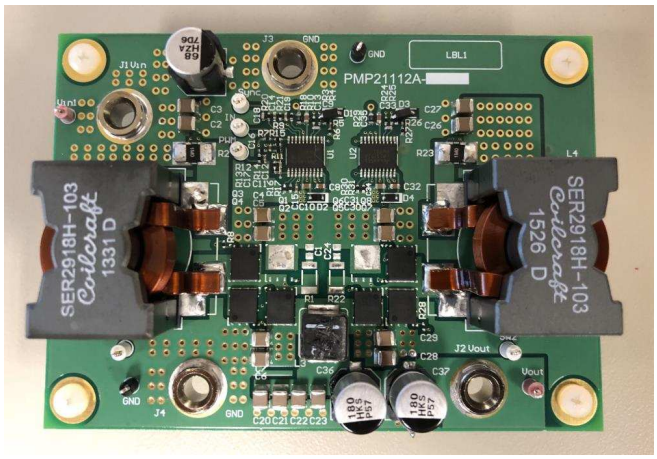
特長

- 入力電圧範囲: 9V～16V
- 出力電圧範囲: 16V～40V
- 10Aの連続出力
- PWMまたはDC制御の出力電圧
- オーディオ・アンプ電源を信号の条件に合わせて調整可能

アプリケーション

- 車載用外部アンプ





1 System Description

This reference design is a dual-phase boost using the LM25112-Q1 boost controller for automotive audio applications. This design can operate from 9 V to 16 V. The design has an adjustable output of 16 V to 40 V and is capable of sourcing a 10-A continuous current, suitable for powering a power audio amplifier. The LM25112-Q1 boost controller has a bypass function. When V_{IN} is equal to or greater than the set output voltage, the device will bypass V_{IN} using the high-side sync FET. Output adjustment is achieved by applying a 3.3-V PWM signal to the adjustment input. Adjusting the duty cycle of the PWM signal from 10% to 90% adjusts the output from 40 V to 16 V, respectively.

This design is also capable of tracking a sine wave up to 500 Hz without distortion and achieves a delay time of less than 300 µs between sine wave and the output voltage. The switching frequency is set to 150 kHz and a four-layer PCB is used. When used with an audio processor system capable of supplying the PWM signal, the reference design can be used to track an audio signal, adjusting the output voltage based on the audio signal conditions. An audio amplifier powered by this circuit can provide high-power output when the boost output voltage is set high. A lower power supply voltage is used when less volume is required, allowing the audio amplifier to dissipate less heat than it would if the boost supply was left set to the maximum voltage.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Input voltage	9-V to 16-V DC
Output voltage	16-V to 40-V DC
Output current	10 A
Tracking input voltage	0 V min, 3.3 V max
	0.33 V to 3 V to meet output voltage range
Tracking input frequency	500 Hz, max
Tracking PWM frequency	100 kHz, minimum

2 System Overview

2.1 Block Diagram

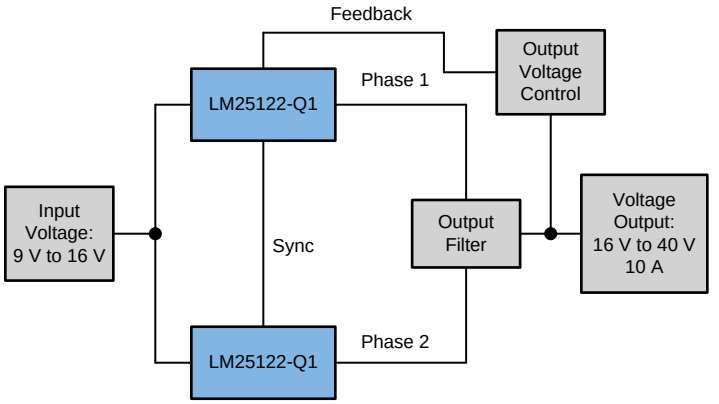


図 1. TIDA-01610 Block Diagram

2.2 Highlighted Products

2.2.1 LM25122-Q1 Wide-Input Synchronous Boost Controller With Multiple Phase Capability

The LM25122 is a multiphase capable synchronous boost controller intended for high-efficiency synchronous boost regulator applications. The control method is based upon peak current mode control.

Current mode control provides inherent line feedforward, cycle-by-cycle current limiting and ease of loop compensation.

The switching frequency is programmable up to 600 kHz. Higher efficiency is achieved by two robust N-channel MOSFET gate drivers with adaptive dead-time control. A user-selectable diode emulation mode also enables discontinuous mode operation for improved efficiency at light load conditions.

An internal charge pump allows 100% duty cycle for high-side synchronous switch (bypass operation). A 180º phase shifted clock output enables easy multiphase interleaved configuration. Additional features include thermal shutdown, frequency synchronization, hiccup mode current limit and adjustable line undervoltage lockout.

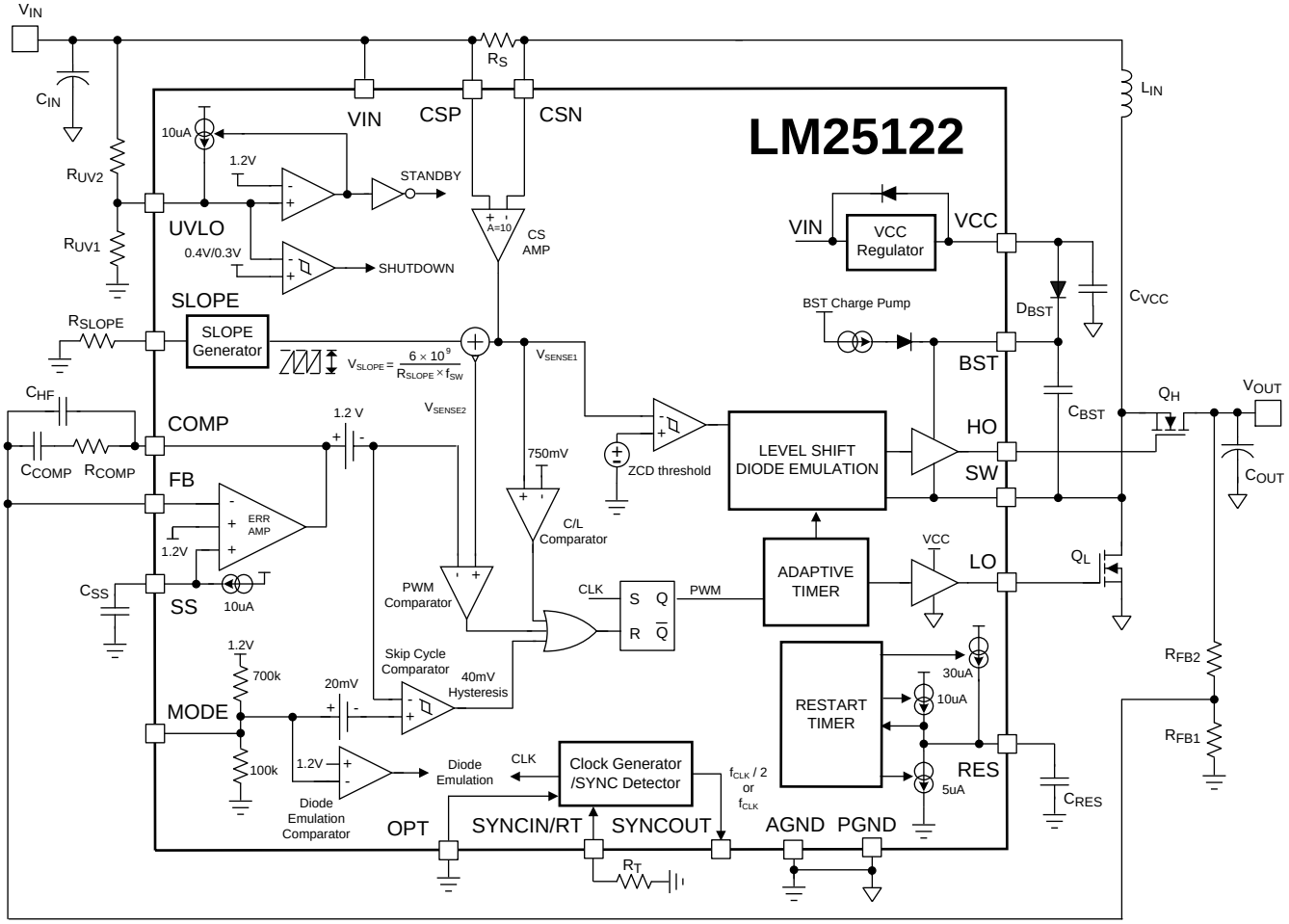


図 2. LM25122-Q1 Block Diagram

2.3 System Design Theory

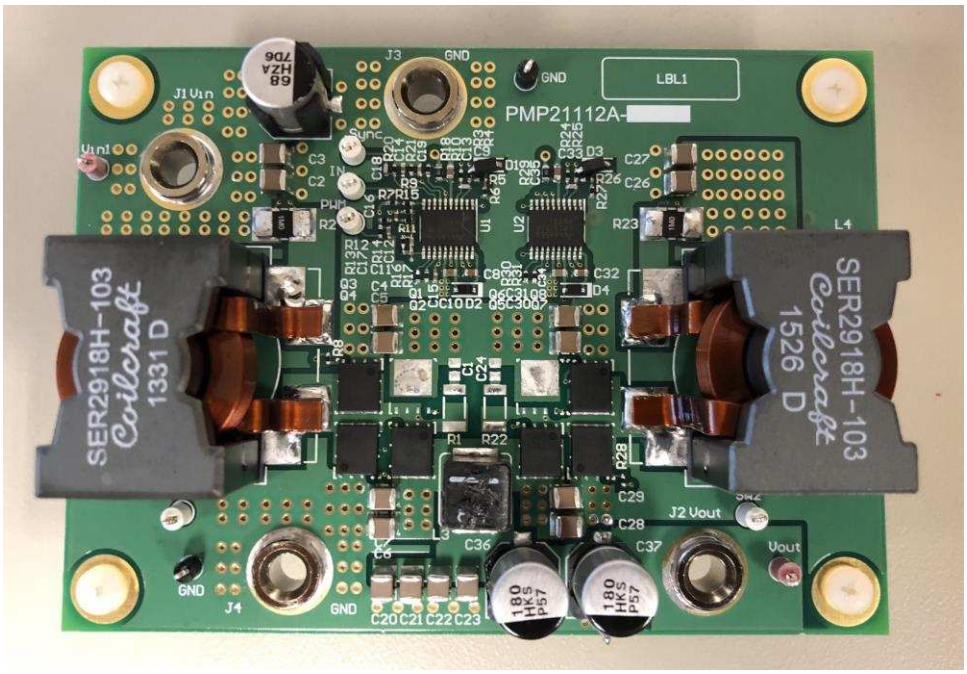


図 3. PCB Top View

2.3.1 Boost Design

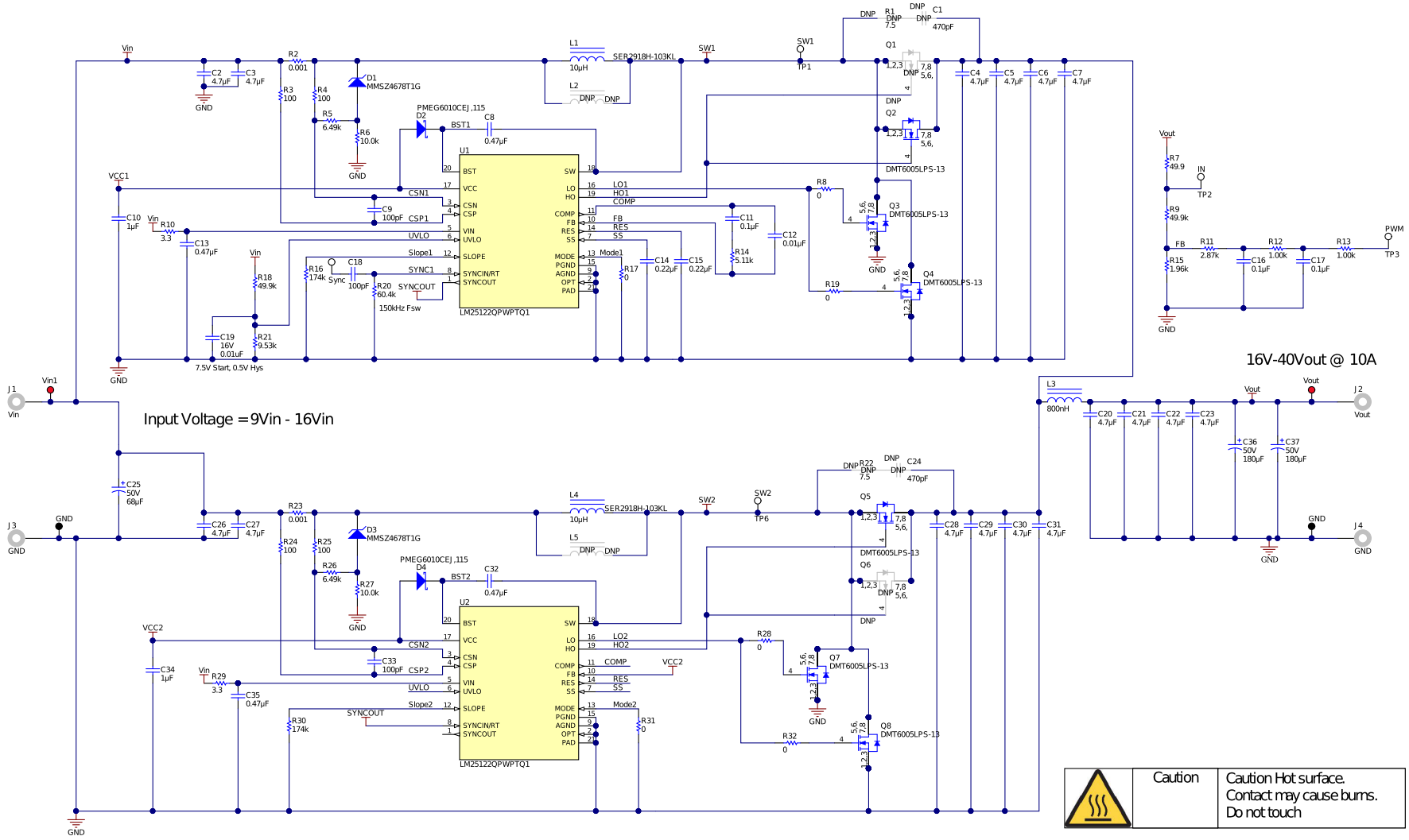


図 4. TIDA-01610 Schematic

To ensure a continuous 10-A delivery to the load, a two-phase boost topology is used for this reference design. A two-phase implementation allows reduction in the size of filter capacitors and inductors while simultaneously lowering power dissipation in the main boost switch transistor. The filter inductor can shrink because the average current is divided between two inductors. The LM25122-Q1 is ideal for this design because it provides SYNCOUT and SYNC in pins for use in creating multi-phase designs. In the reference design, U1 provides the master timing to U2. The feedback pin on U2 is tied to U2's VCC input to set the device for slave operation. Other than the interconnection for synchronization, the circuits around U1 and U2 are identical. The undervoltage lockout (UVLO) and compensation network are shared by the two boost circuits.

Each phase is designed as a 5-A output boost. The designer must make trade-offs because the voltage can be set anywhere in the range of 16 V to 40 V. The same constraints apply to both phases.

The switching frequency is set for 150 kHz by R20. The frequency setting and load requirements determine the necessary filter component values for inductance and total capacitance. 150 kHz is chosen to ensure minimum switching losses and heat dissipation. The value of inductors L1 and L4 is 10 µH. The peak inductor current is almost 26 A, so the inductor must have a high current rating. Large inductor ripple current results in large core loss in the inductor. The selected inductance provides a 20% to 30% inductor ripple current ratio to the average inductor current across entire input and output operating voltages with a 10-A load current. The selected SER2918H-103 is suitable for high-power applications like this design. The SER2918H-103 has DCR to reduce DC loss. Its core design reduces core loss.

Ceramic capacitors are chosen for the input and output filters closest to U1. C25, C2, C3, C26, and C27 are the input capacitors. The input capacitors in a boost topology see continuous current. Therefore, the input capacitor’s RMS current is low. The worst case RMS current in the input capacitors is 2.6 A, so a single electrolytic capacitor with moderate ESR in addition to four ceramic capacitors ensures proper RMS current split as well as damping some amount of wiring inductance from the supply. C25 is shared by both boost phases.

The output capacitors in a boost topology see discontinuous, pulsating current. The worst case RMS current in the output capacitor is 20 A. One job of the output capacitors is to maintain the output voltage in a load transient event. A second stage filter is added to attenuate the RMS current going into the large value electrolytic capacitors at the final output. This filter is necessary because the DC voltage of a ceramic capacitor must be derated and because the boost topology has a slow loop response due to the presence of a right-half-plane zero in the boost transfer function. In this reference design, C4 through C7 are the first stage output capacitors in the U1 phase, and C28 through C31 are the output capacitors for the second phase. These are all 4.7-µF, 80-V capacitors. The high voltage rating ensures the total capacitance value does not drop significantly when the output is set to 40 V. The second low-pass filter consists of L3, C20 through C23, C36, and C37.

The switch and synchronous rectifier transistors chosen are automotive rated and have low $R_{DS(on)}$. Due to the high peak current, two transistors are paralleled to reduce heat dissipation in the switch transistors. The synchronous rectifier does not dissipate as much power, so only one transistor is needed; however, this reference design provides enough space for two.

The output voltage can track a 500-Hz sine wave signal with little distortion. Consequently, the LM25122-Q1 has to charge and discharge the output capacitors from 16 V to 40 V then back to 16 V at a rate of 500 Hz. During the discharging event, the synchronous FET is discharging current from the output and returning the current back to the input, which creates a negative voltage across the current sense amplifier. The differential current sense amplifier on the LM25122-Q1 does not support negative current

sense. Therefore, a level shift circuit must be implemented to bias the no-load current sense value to the middle of the dynamic range. The bias circuit consists of D1, R5, and R6 in phase 1 and D3, R26, and R27 in phase 2. This implementation allows the amplifier to transition between the current limit threshold and zero, which ensures regulation during a tracking event. Due to the level shift implementation, a 1-mΩ current sense resistor is used to ensure full load delivery of the charging current during the tracking event.

The operation mode is set for diode emulation mode by tying U1, pin 13 to ground through R17. In FPWM mode, with a pre-biased output at no load, a large reverse current upon start-up is potentially destructive. Selecting diode emulation mode prevents potential large reverse currents. The offset provided to the current sense amplifier forces continuous conduction mode during all conditions of operation, even with the mode pin set to diode emulation mode.

UVLO is set so the regulator starts operating when the input voltage is above 7.5 V. The input voltage is filtered by R10 and C13. R10 provides U1's V_{IN} connection with some isolation from the switching transients on V_{IN}.

2.3.2 Tracking Control

The tracking control circuit is part of the output voltage feedback network for the power supply. The tracking control point is TP3, which is also labeled PWM on the schematic. Resistors R7, R9, and R15 form the normal part of the output voltage feedback network. Resistors R11, R12, and R13 along with capacitors C16 and C17 form an input filter for the PWM signal. R13, C17, R12, and C16 form a low-pass filter that filters a PWM signal. The PWM signal need not be PWM. This signal can also be a sine wave of 500 Hz or less, or a DC voltage can be applied to control the boost output voltage.

The boost regulator drives the output voltage to maintain 1.2 V at the feedback pin on U1. Changing the voltage at TP3 can therefore control the output voltage. V_{OUT} is inversely proportional to the voltage at TP3. The PWM input design works with a 3.3-V PWM output from a microprocessor. The resistor values of the PWM input network are chosen so the boost regulator provides a 40-V output when a 3.3-V PWM signal with a 10% duty cycle is present. If the PWM signal has a 90% duty cycle, the boost output is 16 V.

The PWM signal must be at least 100 kHz. Otherwise, the filter network cannot filter the noise from the PWM signal well and the noise will appear in the output of the boost converter. If the values of C16 and C17 are increased, more filtering would be provided to the control signal. However, it would take longer for the boost output voltage to respond to changes in the control signal, which lowers the frequency that the power supply output responds to. In an actual system, the control signal varies based on the level, or volume, setting of an audio signal.

3 Hardware Setup, Testing Requirements, and Test Results

3.1 Hardware Setup

In addition to the setup defined in 図 5, three 6.8-mF, 65-V rated electrolytic capacitors are used to damp the wiring inductance of the input supply for all test data taken on this design guide.

3.2 Testing and Results

3.2.1 Test Setup

図 5 shows the setup for the efficiency test.

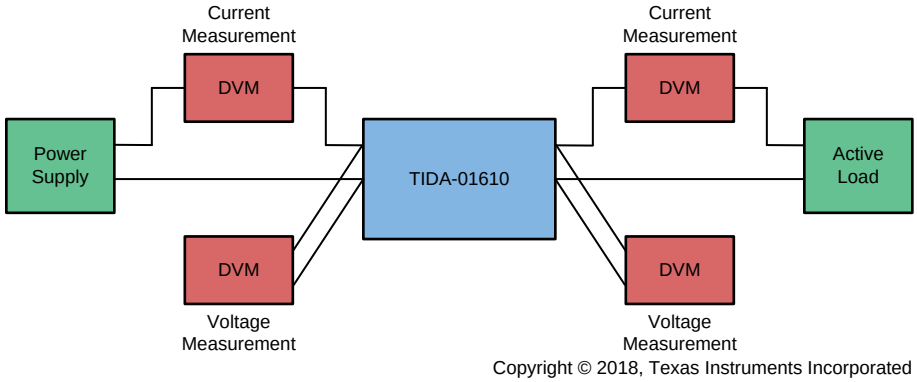


図 5. Efficiency Test Setup Diagram

3.2.2 Test Results

3.2.2.1 Efficiency

The power output efficiency is plotted in 図 6, 図 7, 図 8, and 図 9. In all cases, the efficiency is above 90% for loads above 0.5 A and above 95% for loads above 2 A.

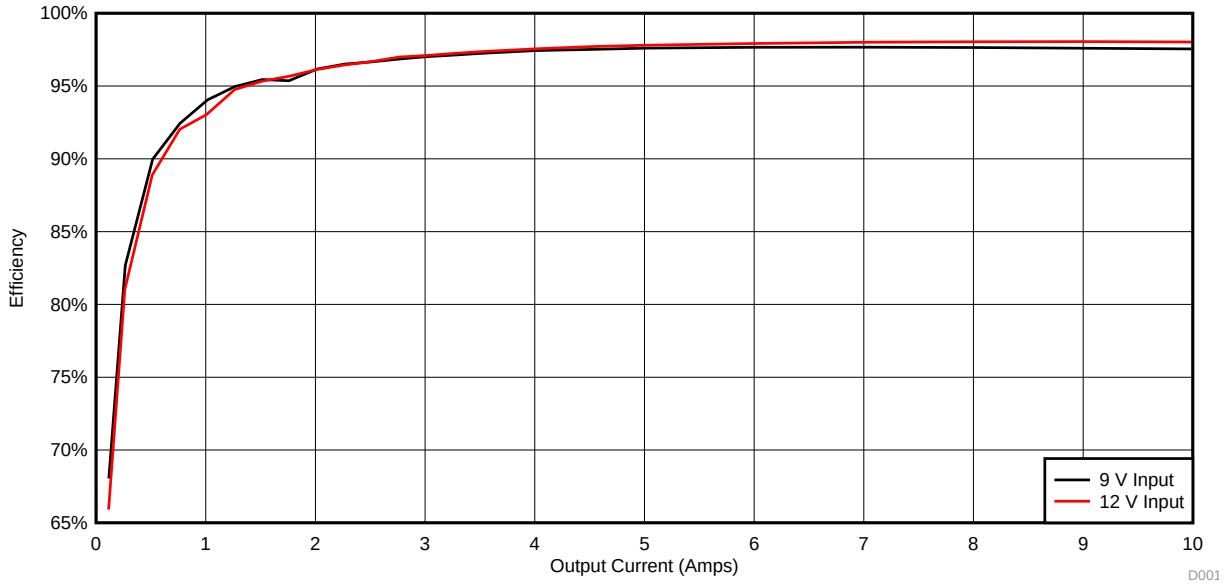


図 6. 16-V Output Efficiency

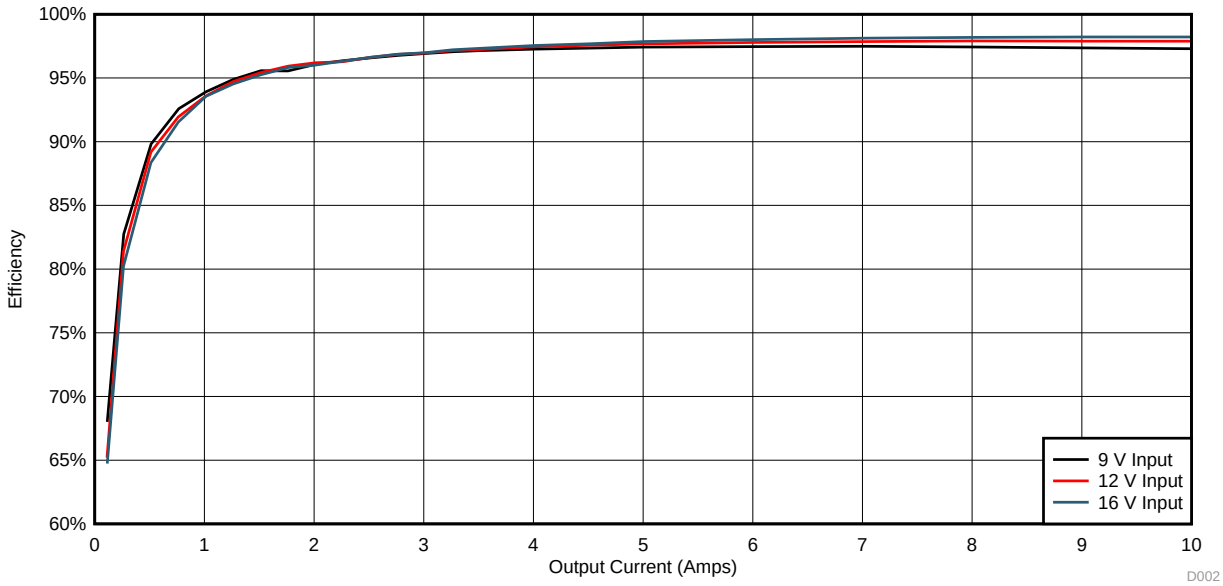


図 7. 20-V Output Efficiency

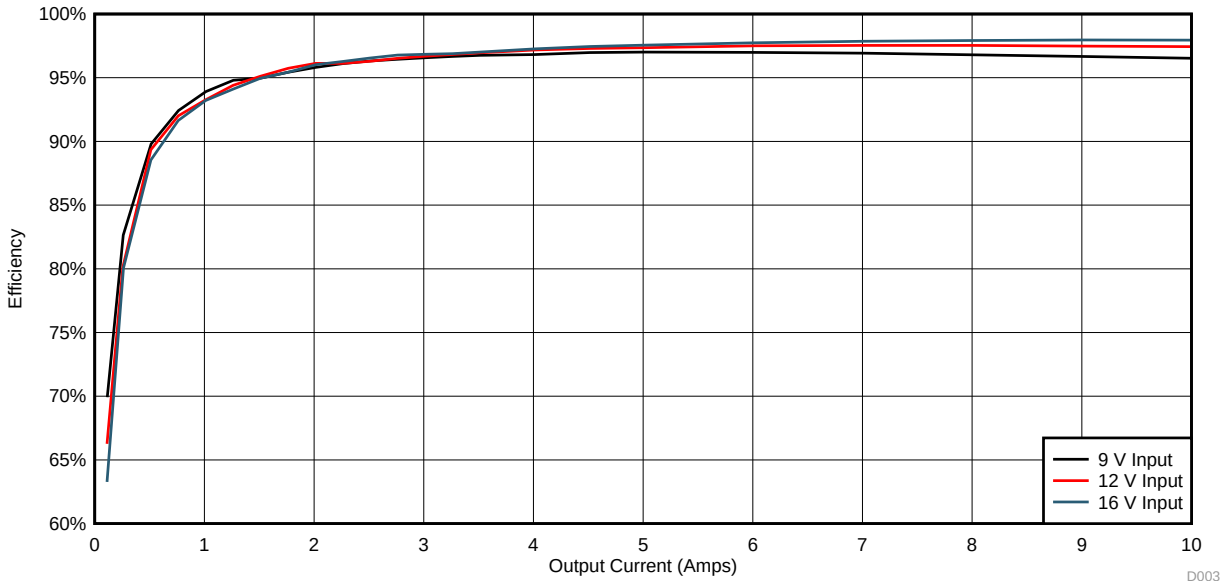


図 8. 30-V Output Efficiency

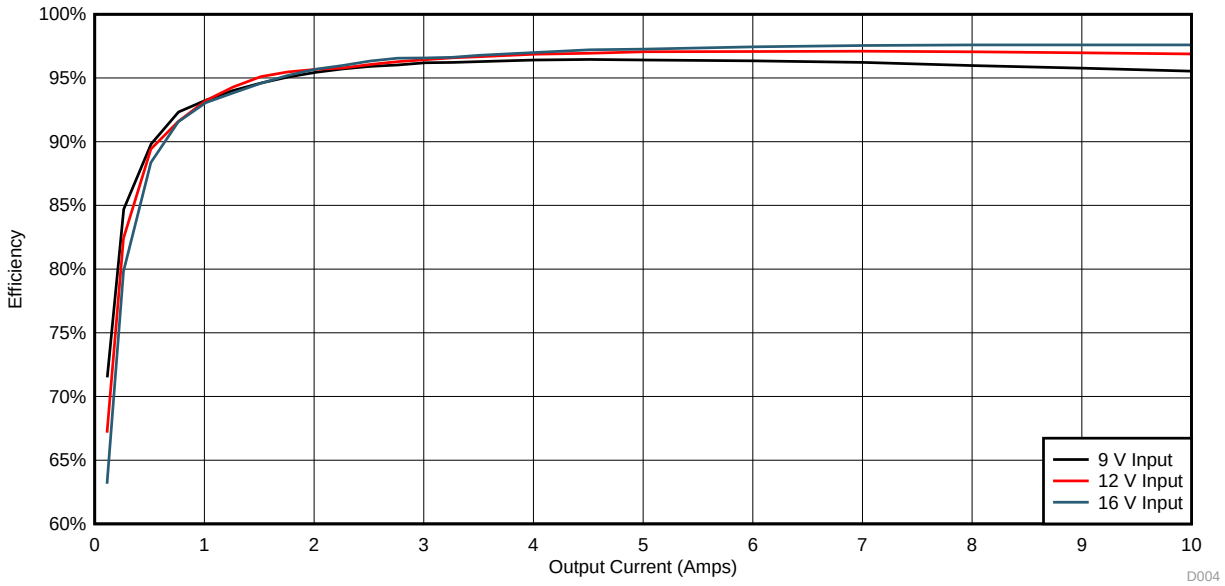


図 9. 40-V Output Efficiency

3.2.2.2 Switching Waveforms and Output Ripple

The switching waveforms and output ripple are measured with oscilloscope probes connected to TP1 (SW1), TP2 (SW2), and the V_{OUT} test points shown in 図 4. In the oscilloscope traces in 図 10, the yellow trace is the switch node for the master LM25122-Q1, the blue trace is the slave switch node, and the pink trace is the output ripple and noise. The worst cast output ripple is about 180 mVp-p with a 9-V input and a 40-V output, as shown in 図 18.

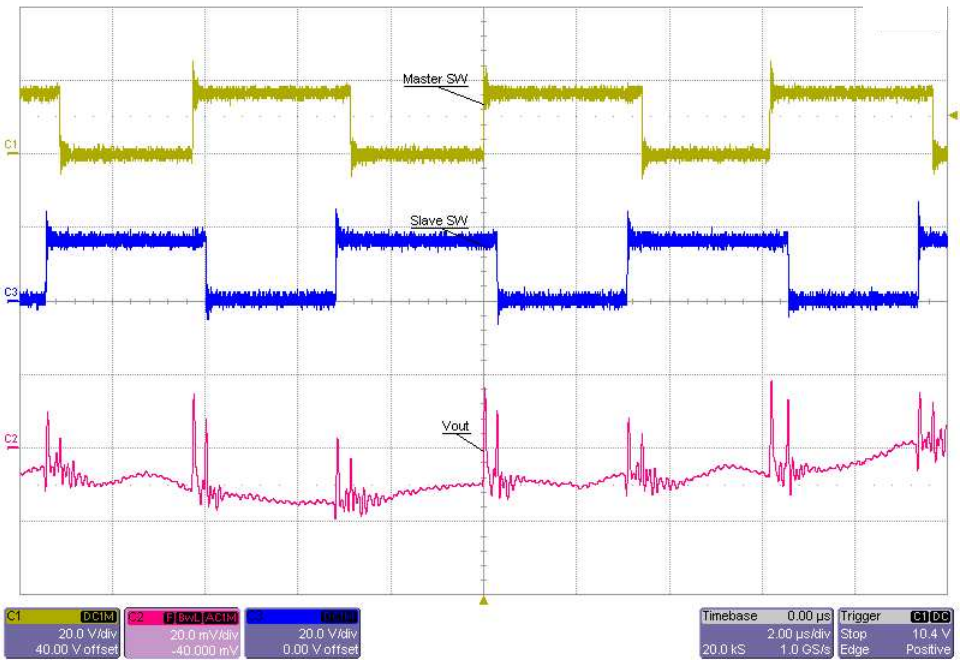


図 10. 9-V Input, 16-V Output, Full Load

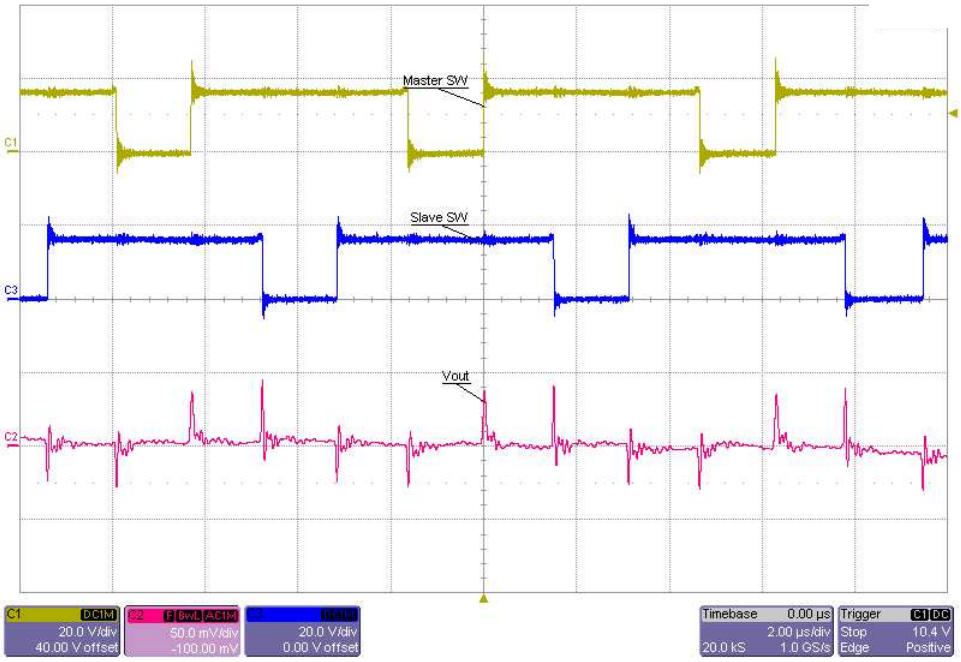


図 11. 12-V Input, 16-V Output, Full Load

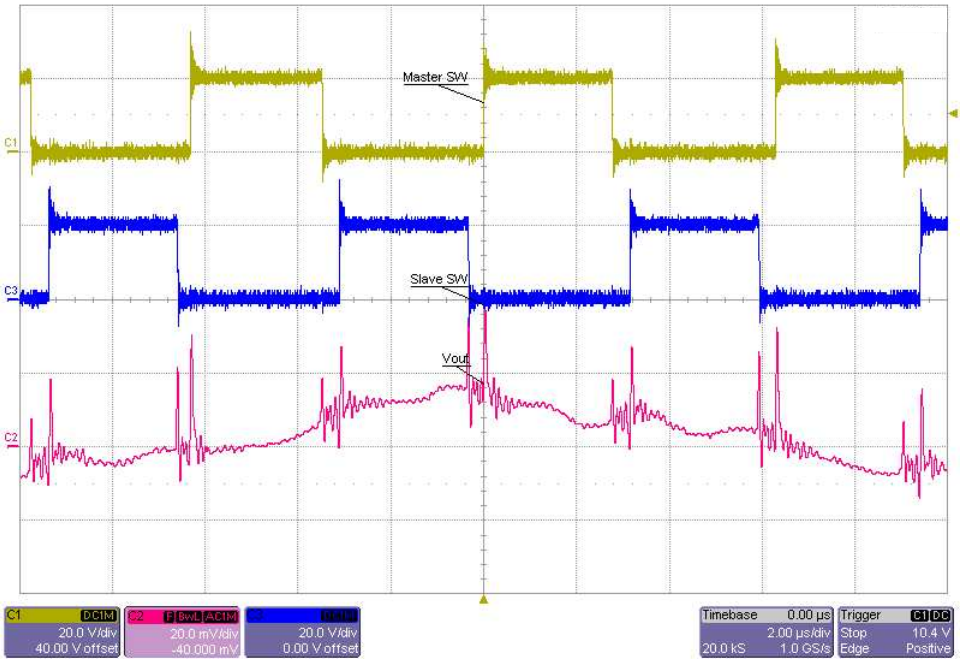


図 12. 9-V Input, 20-V Output, Full Load

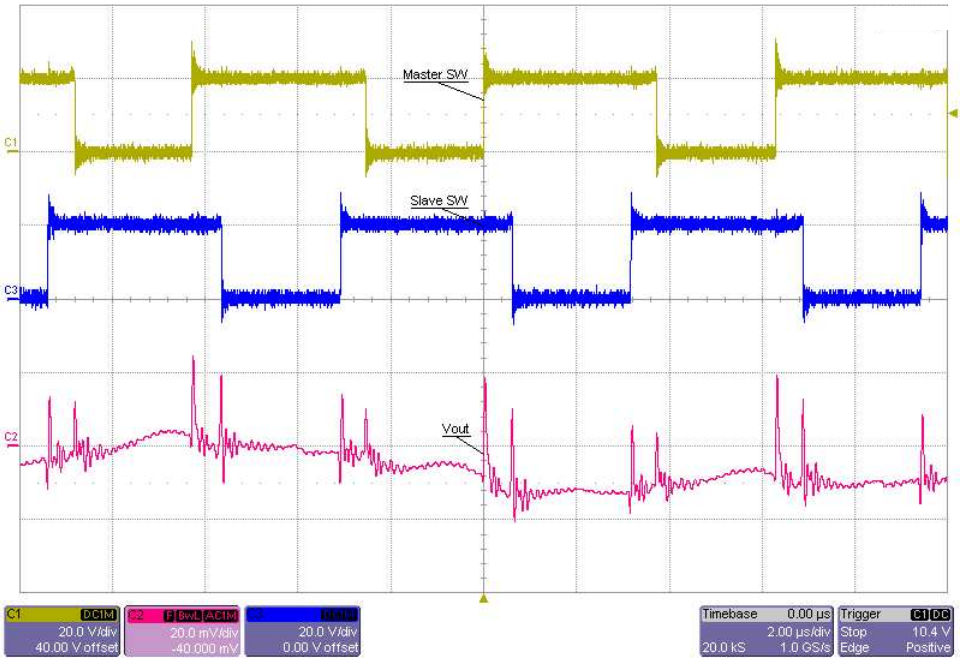


図 13. 12-V Input, 20-V Output, Full Load

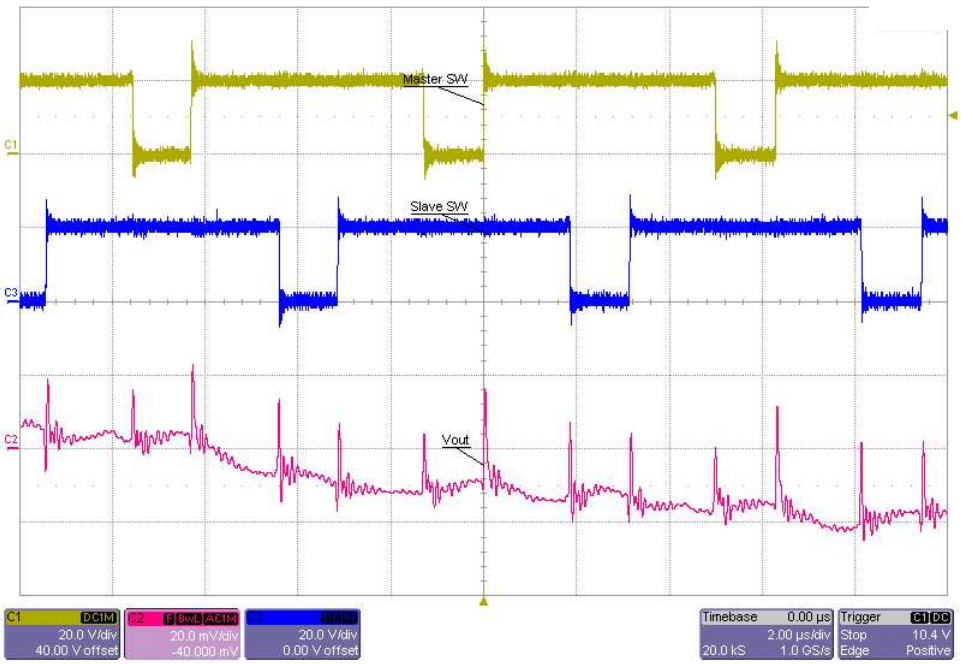


図 14. 16-V Input, 20-V Output, Full Load

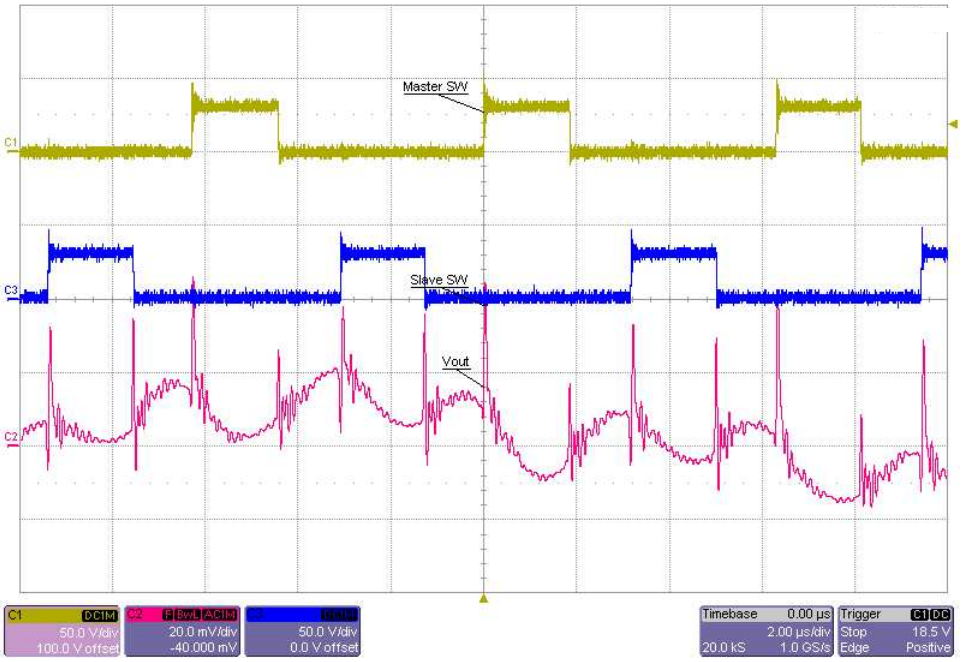


図 15. 9-V Input, 30-V Output, Full Load

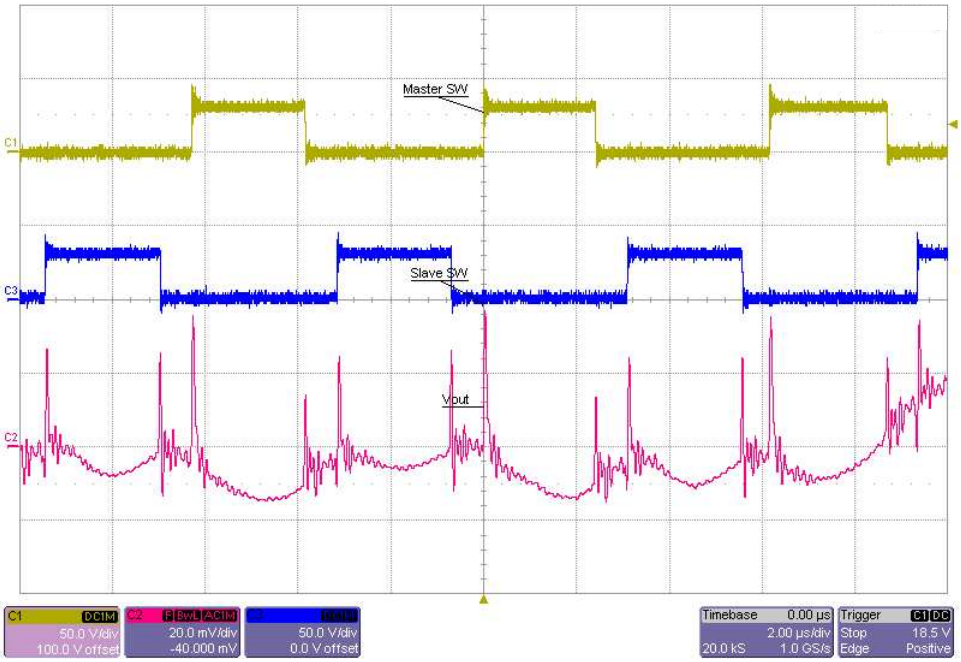


図 16. 12-V Input, 30-V Output, Full Load

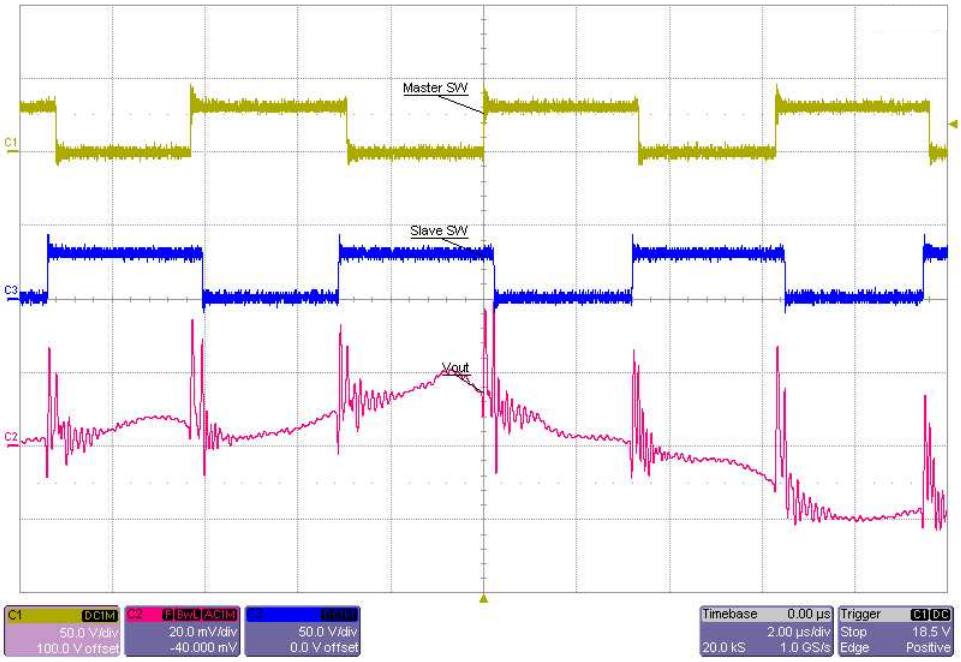


図 17. 16-V Input, 30-V Output, Full Load

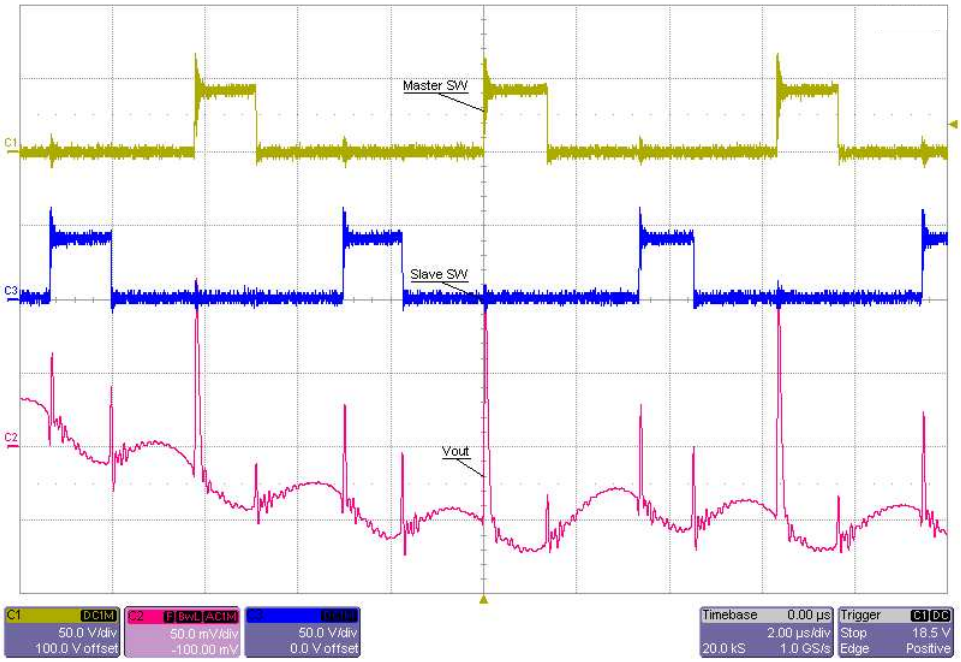


図 18. 9-V Input, 40-V Output, Full Load

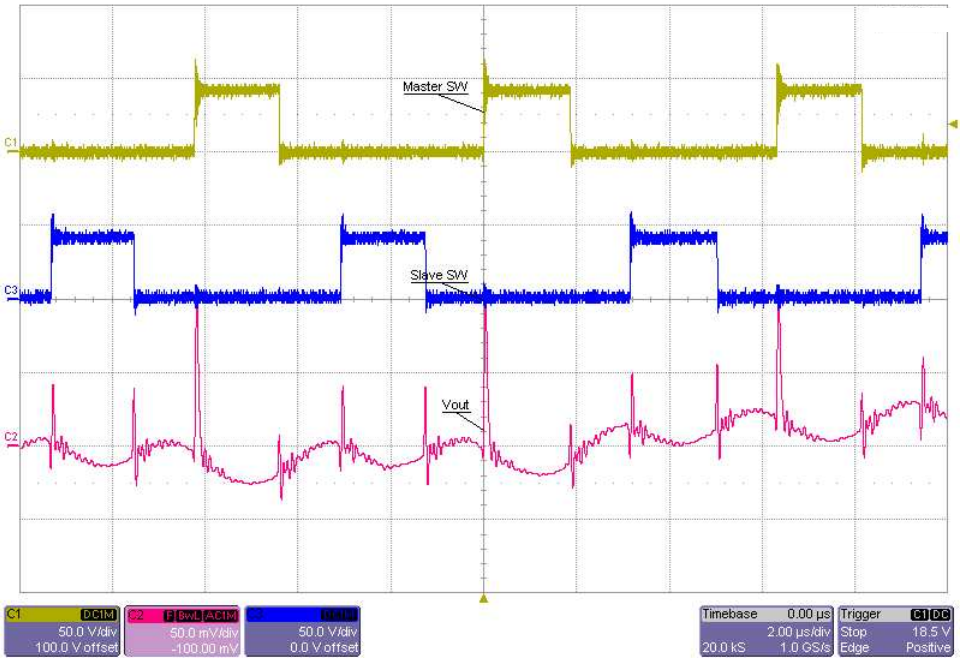


図 19. 12-V Input, 40-V Output, Full Load

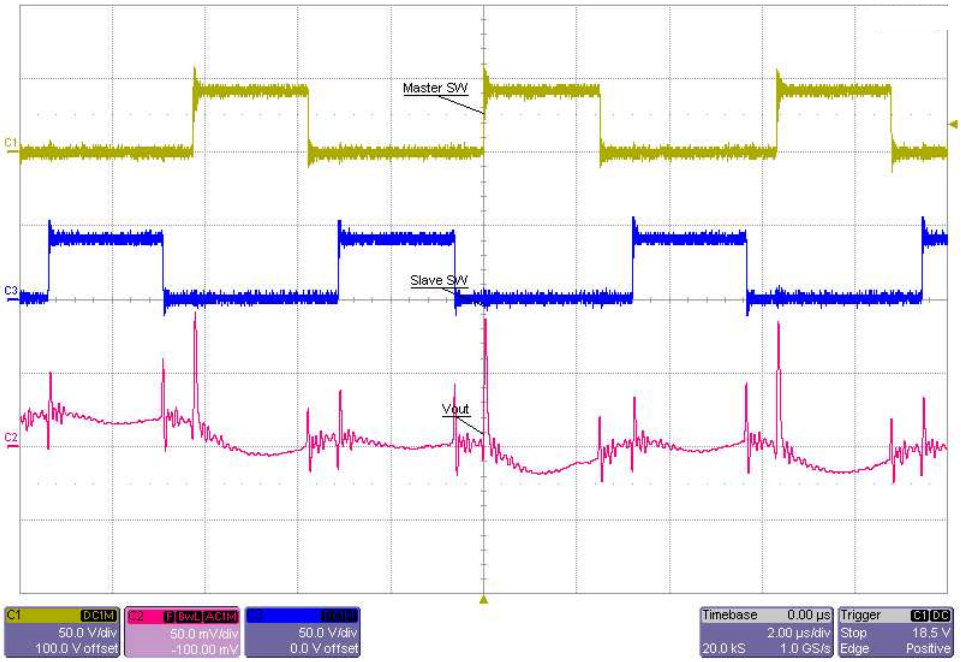


図 20. 16-V Input, 40-V Output, Full Load

3.2.2.3 Start-Up Transient

The start-up transient behavior is measured with oscilloscope probes connected to the input and output voltages and an inductive current probe to measure the output current to the load. In the oscilloscope traces in this section, the yellow trace is the input voltage, the blue trace is the output voltage, and the green trace is the output current. At start-up, the output reaches 40 V in about 22 ms for input voltages of 12 V and 16 V and 23 ms for an input voltage of 9 V.

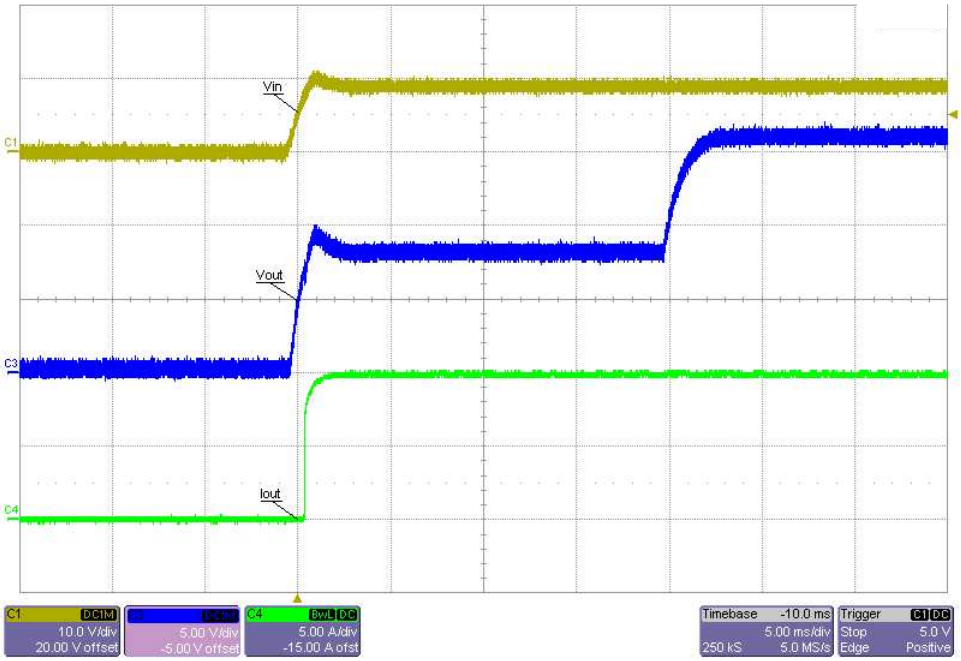


図 21. 9-V Input, 16-V Output, 10-A Load Start-up

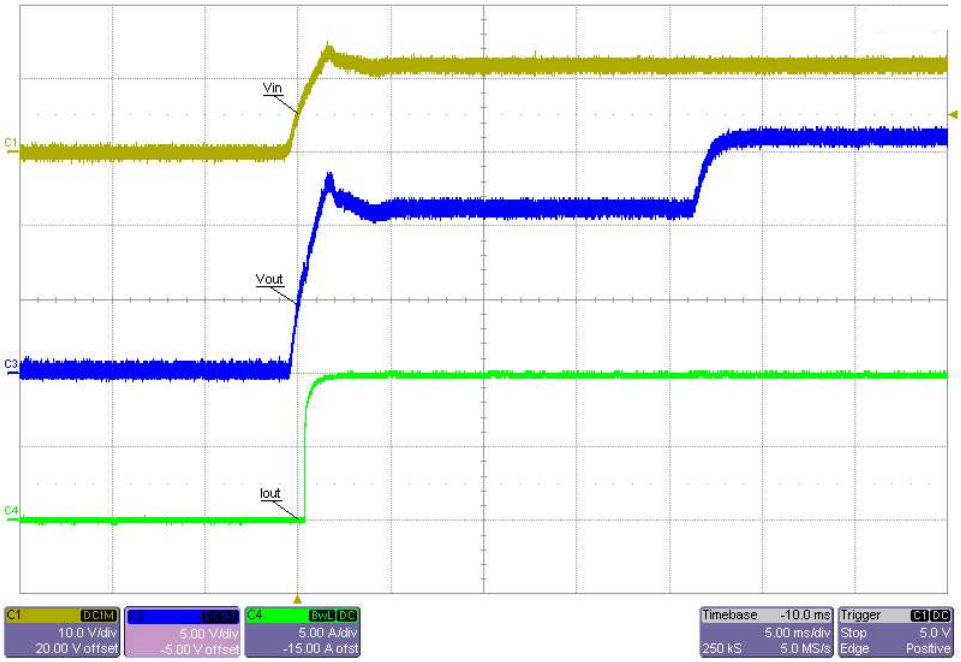


図 22. 12-V Input, 16-V Output, 10-A Load Start-up

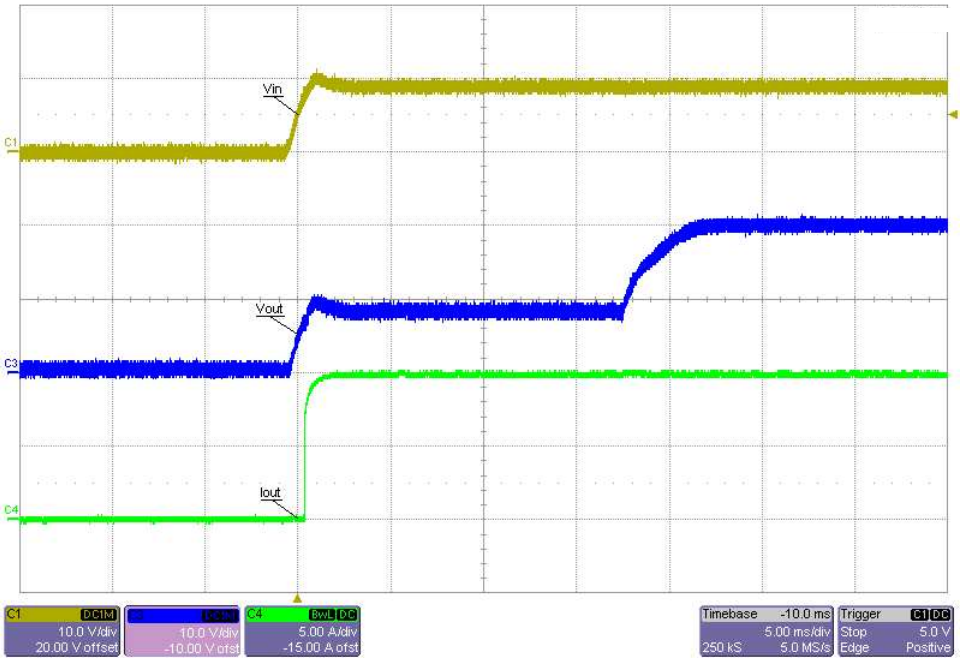


図 23. 9-V Input, 20-V Output, 10-A Load Start-up

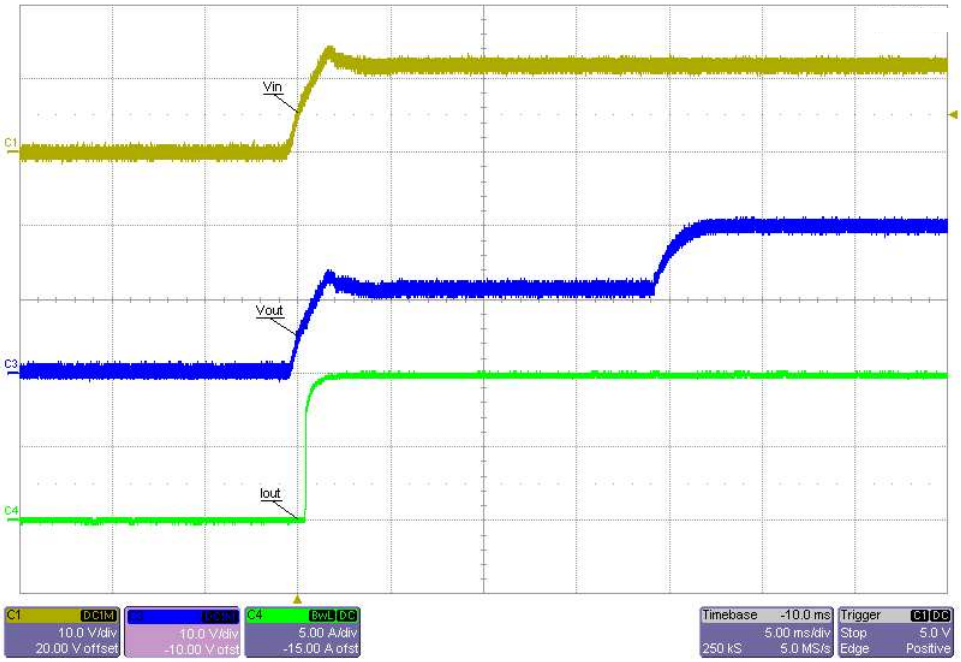


図 24. 12-V Input, 20-V Output, 10-A Load Start-up

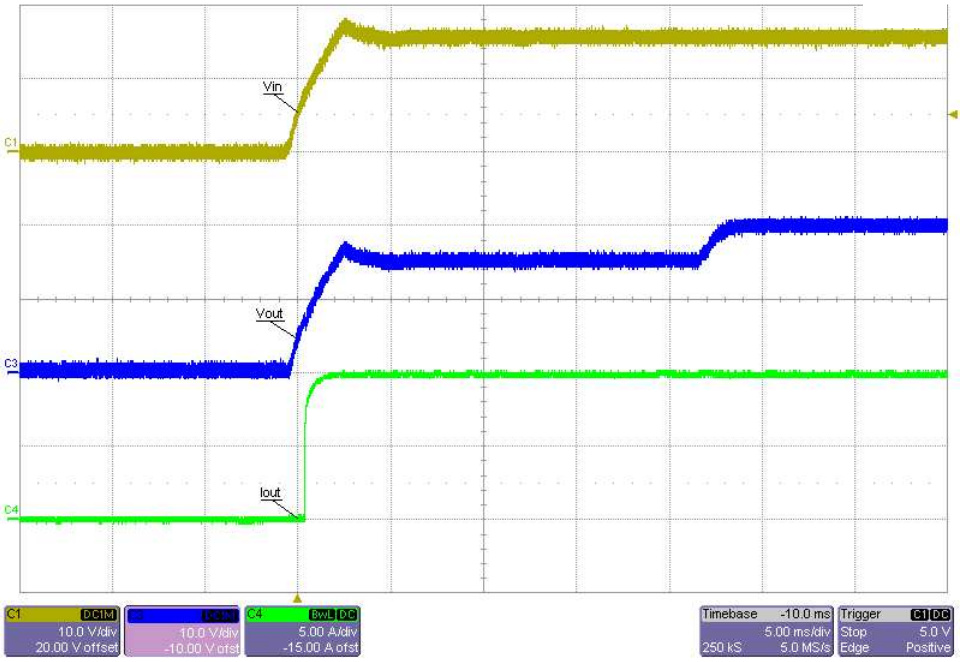


図 25. 16-V Input, 20-V Output, 10-A Load Start-up

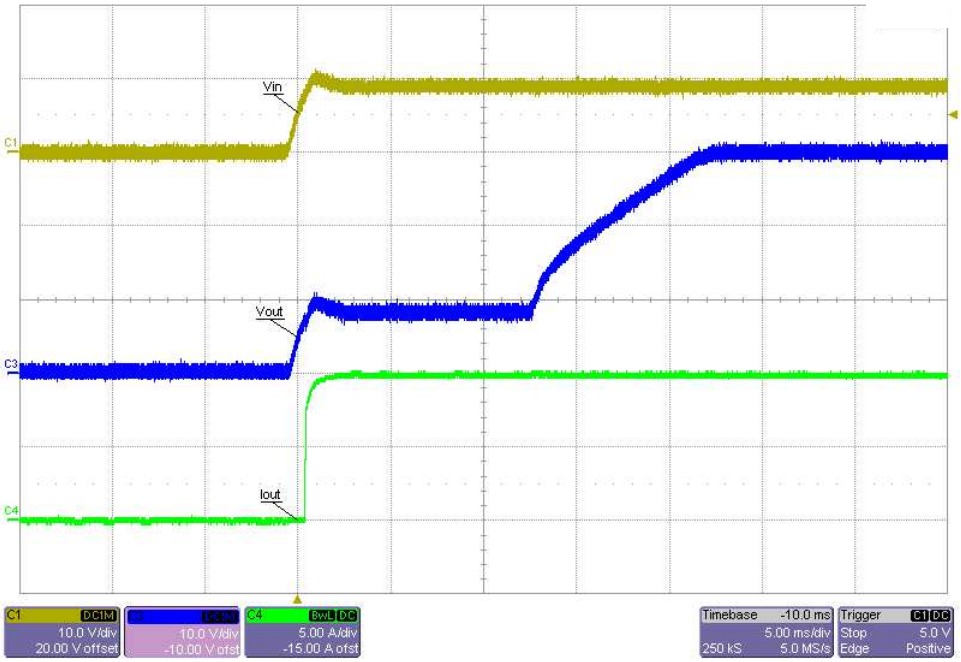


図 26. 9-V Input, 30-V Output, 10-A Load Start-up

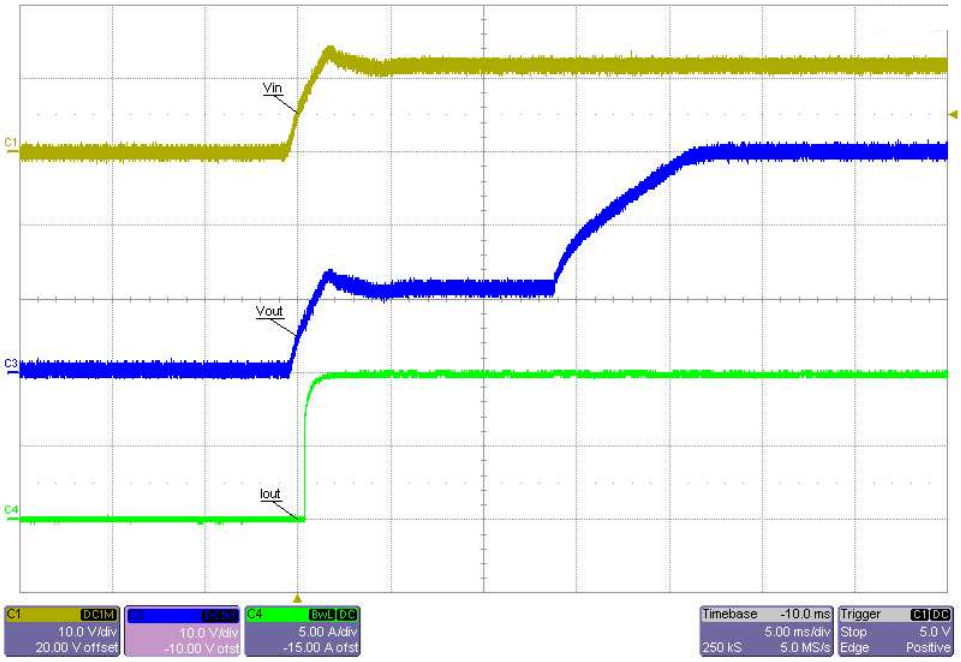


図 27. 12-V Input, 30-V Output, 10-A Load Start-up

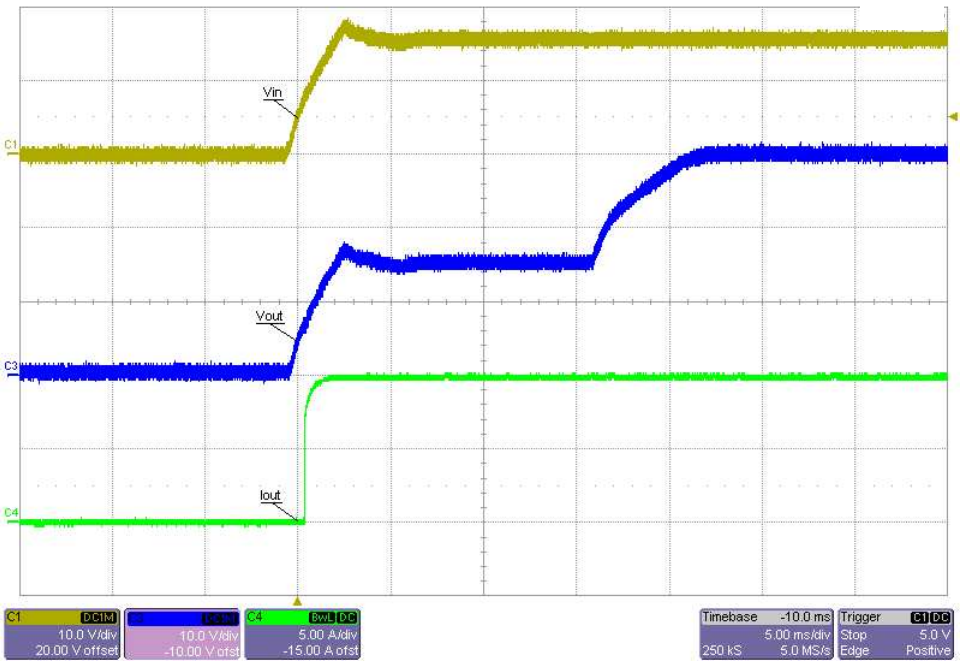


図 28. 16-V Input, 30-V Output, 10-A Load Start-up

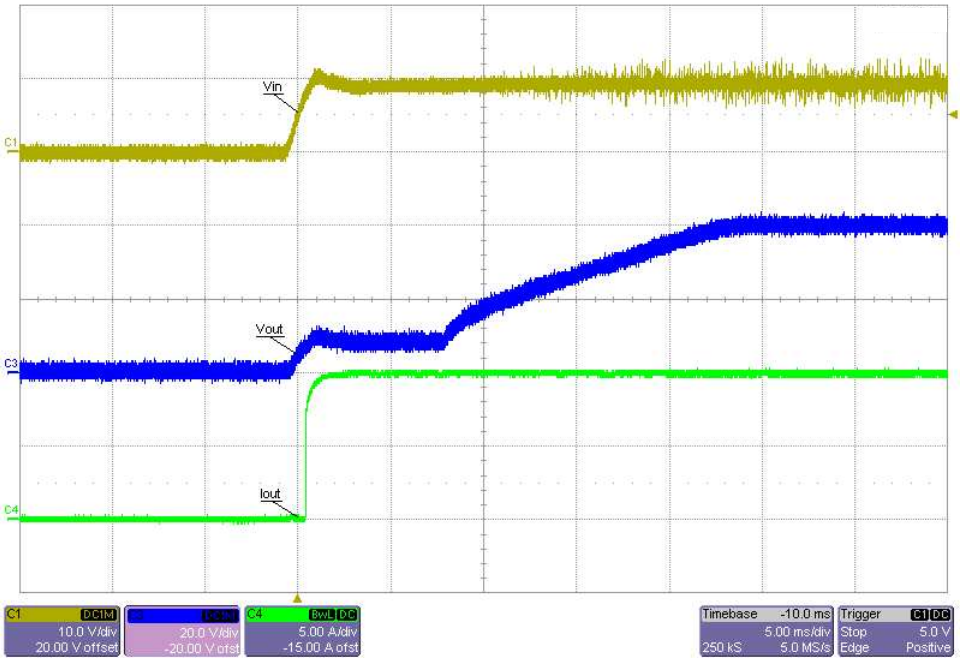


図 29. 9-V Input, 40-V Output, 10-A Load Start-up

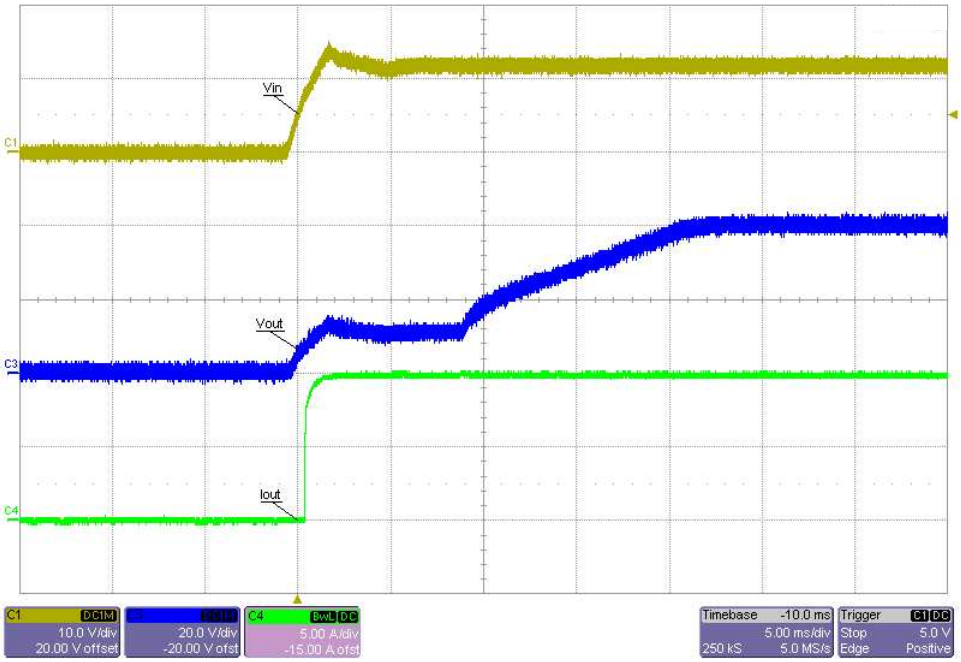


図 30. 12-V Input, 40-V Output, 10-A Load Start-up

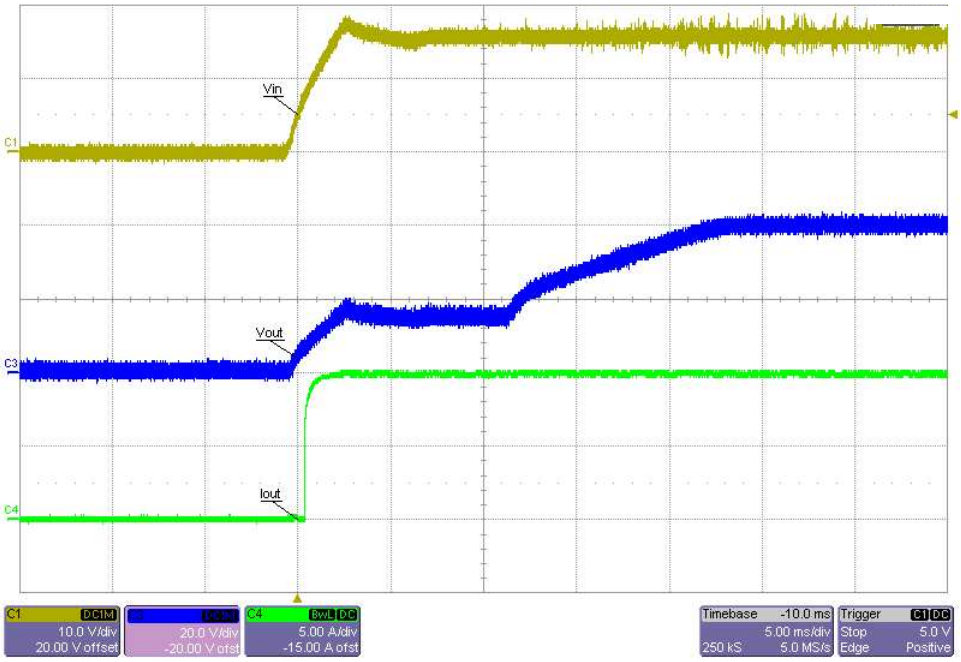


図 31. 16-V Input, 40-V Output, 10-A Load Start-up

3.2.2.4 Transient Response

The load step transient response is measured with an oscilloscope probe on the output voltage and an inductive current probe measuring the output current. In the following plots, the pink trace is the output voltage and the green trace is the output current. The load step response is measured with a load step of 5 A to 10 A with input voltages of 9 V, 12 V, and 16 V. Output voltage is set for 40 V because this is the worst case condition. The worst case droop and overshoot occurs when the input voltage is 49 V, as shown in 図 32. The maximum voltage droop is 1.4 V, and the maximum overshoot is 1.2 V.

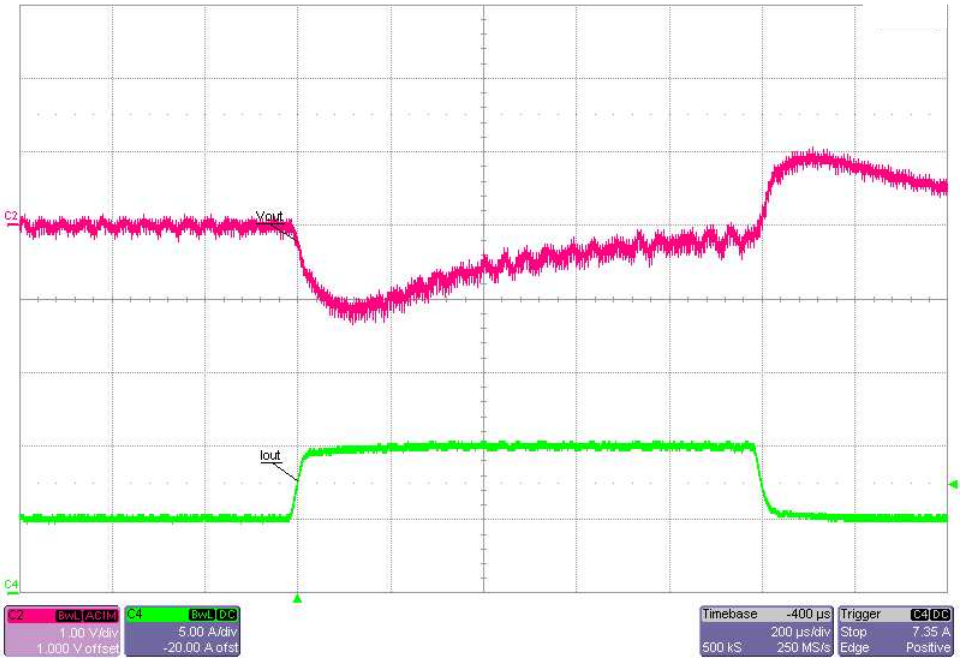


図 32. 9-V Input, 40-V Output, 5-A to 10-A Load Transient

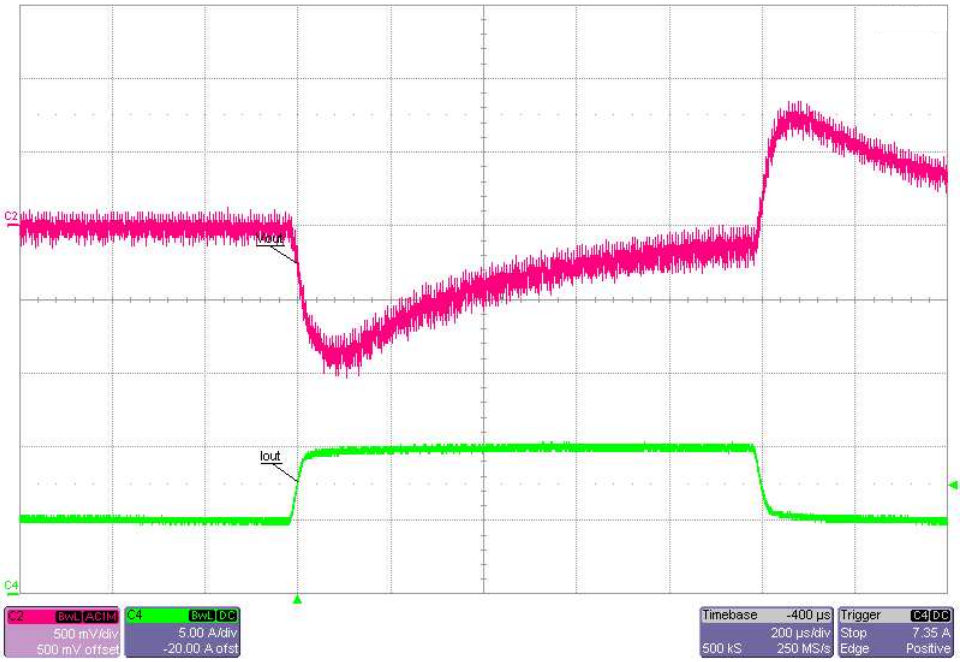


図 33. 12-V Input, 40-V Output, 5-A to 10-A Load Transient

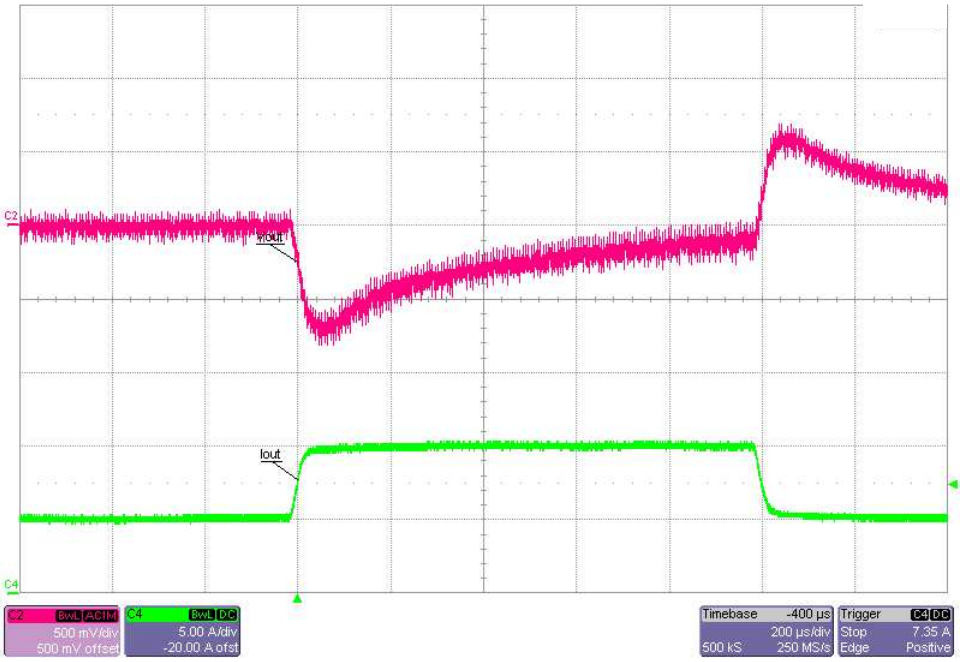


図 34. 16-V Input, 40-V Output, 5-A to 10-A Load Transient

3.2.2.5 Envelope Tracking

図 35 shows the response of the output voltage to a 500-Hz tracking signal. The tracking signal varies from 0.3 V to 3 V. In the following plots, the yellow trace is the tracking signal, the pink track is the output voltage, the blue trace measures the compensation voltage, and the green trace measures the input current. The input voltage is 12 V in both cases. Note that the output voltage is delayed by 285 µs from the tracking voltage.

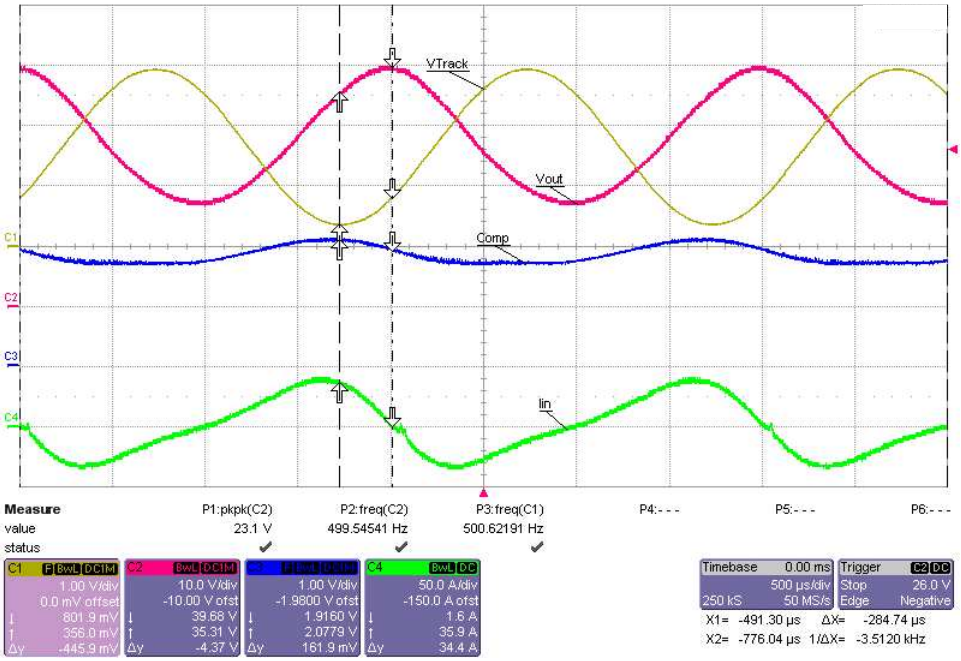


図 35. Tracking Response, 12-V Input, No Load, 500-Hz Tracking Signal

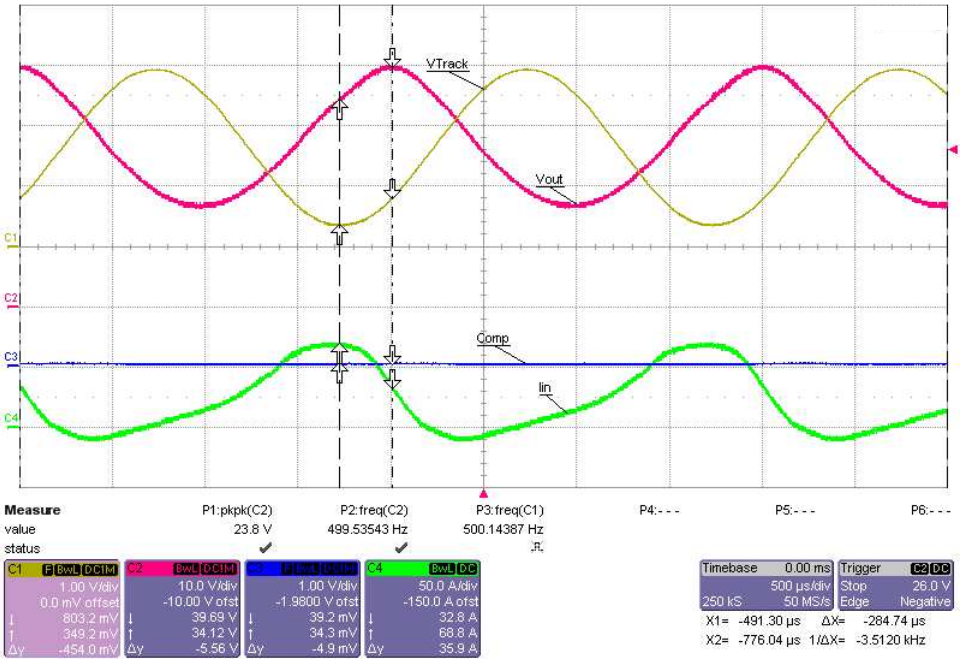


図 36. Tracking Response, 12-V Input, 10-A Load, 500-Hz Tracking Signal

3.2.2.6 Frequency Response

This section shows the gain and phase margin for a 10-A output with the input voltage set to 9 V, 12 V, or 16 V and the output voltage set to 16 V, 24 V, 30 V, or 40 V.

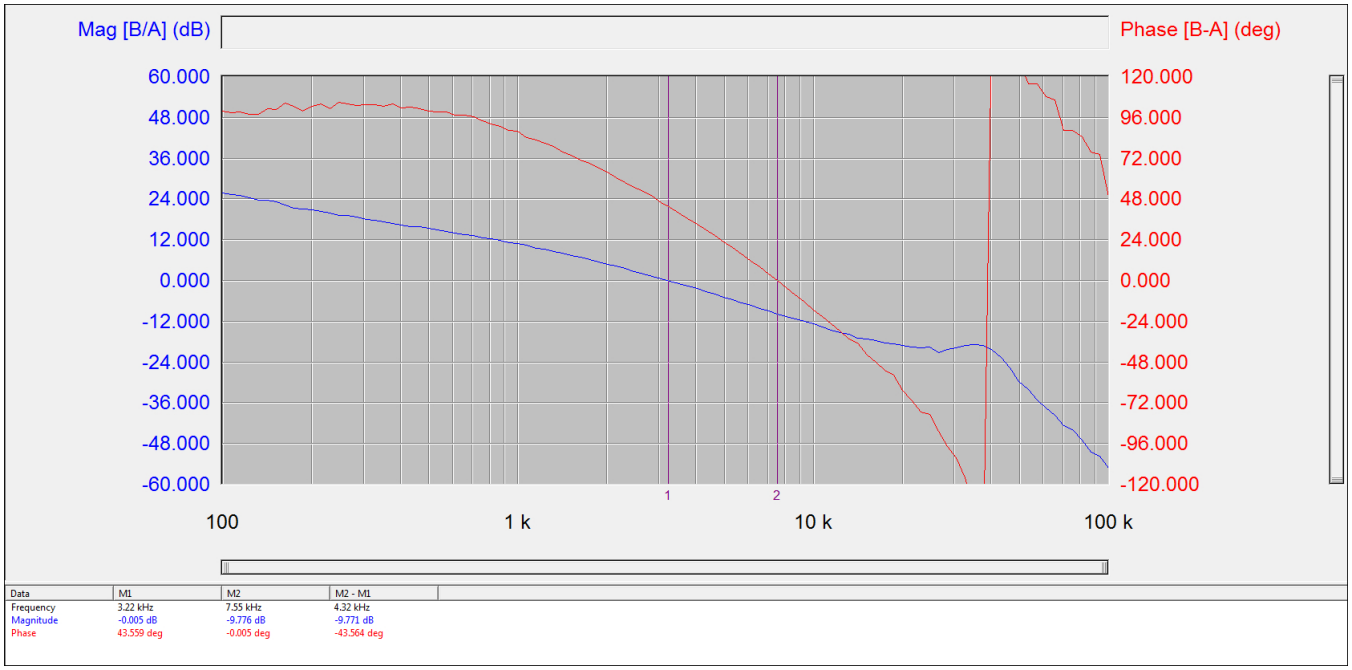


図 37. 9-V Input, 16-V Output, 10-A load: 43.56-Degree Phase Margin, –9.78-dB Gain Margin

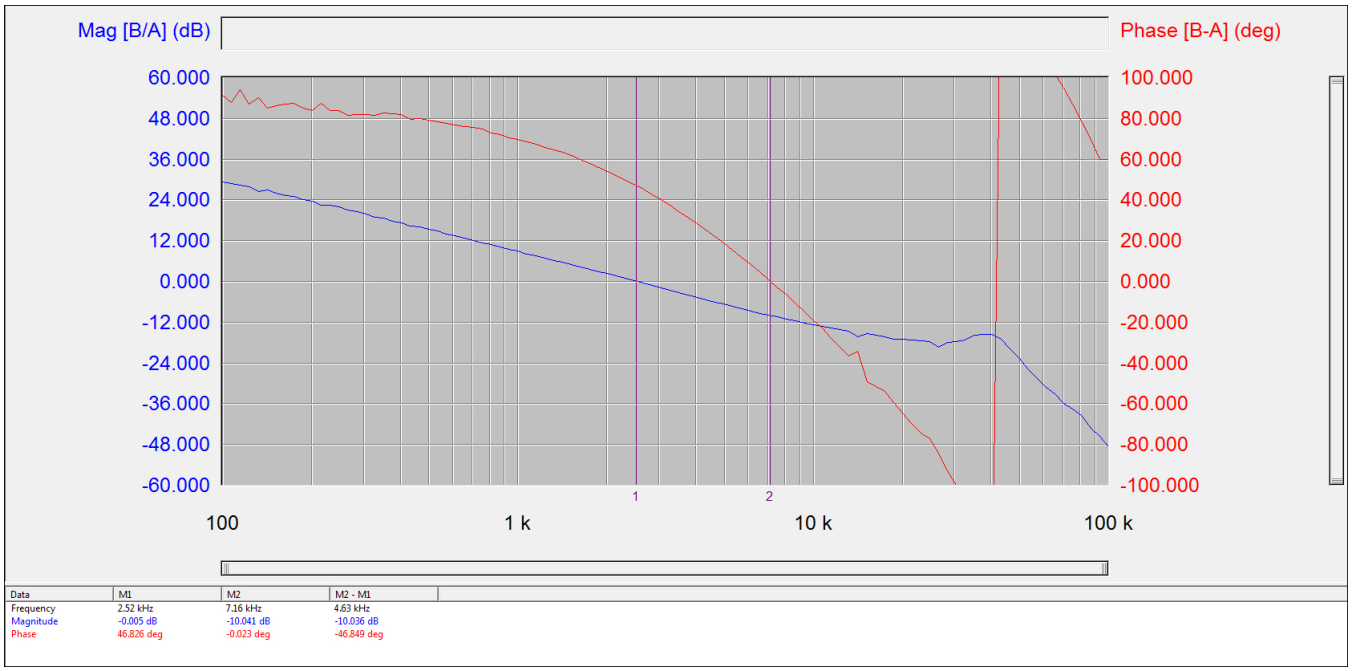


図 38. 9-V Input, 24-V Output, 10-A Load: 46.83-Degree Phase Margin, –10.04-dB Gain Margin

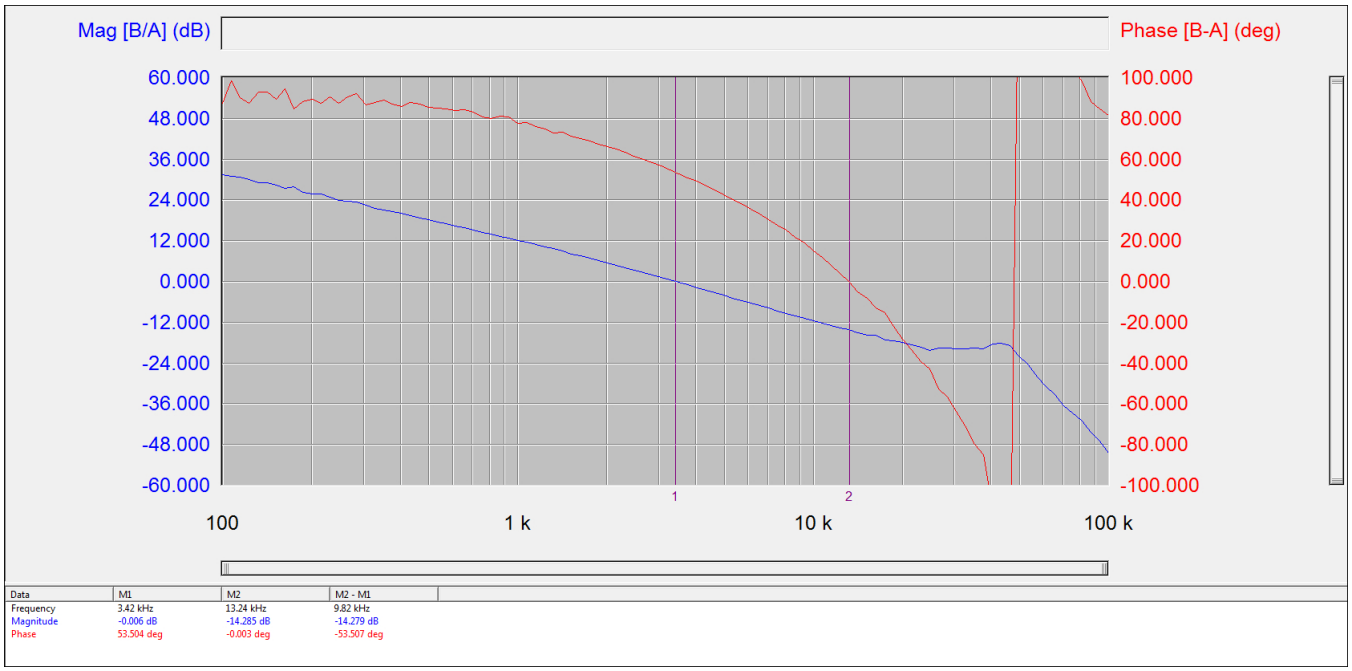


図 39. 9-V Input, 30-V Output, 10-A Load: 48.94-Degree Phase Margin, –10.36-dB Gain Margin

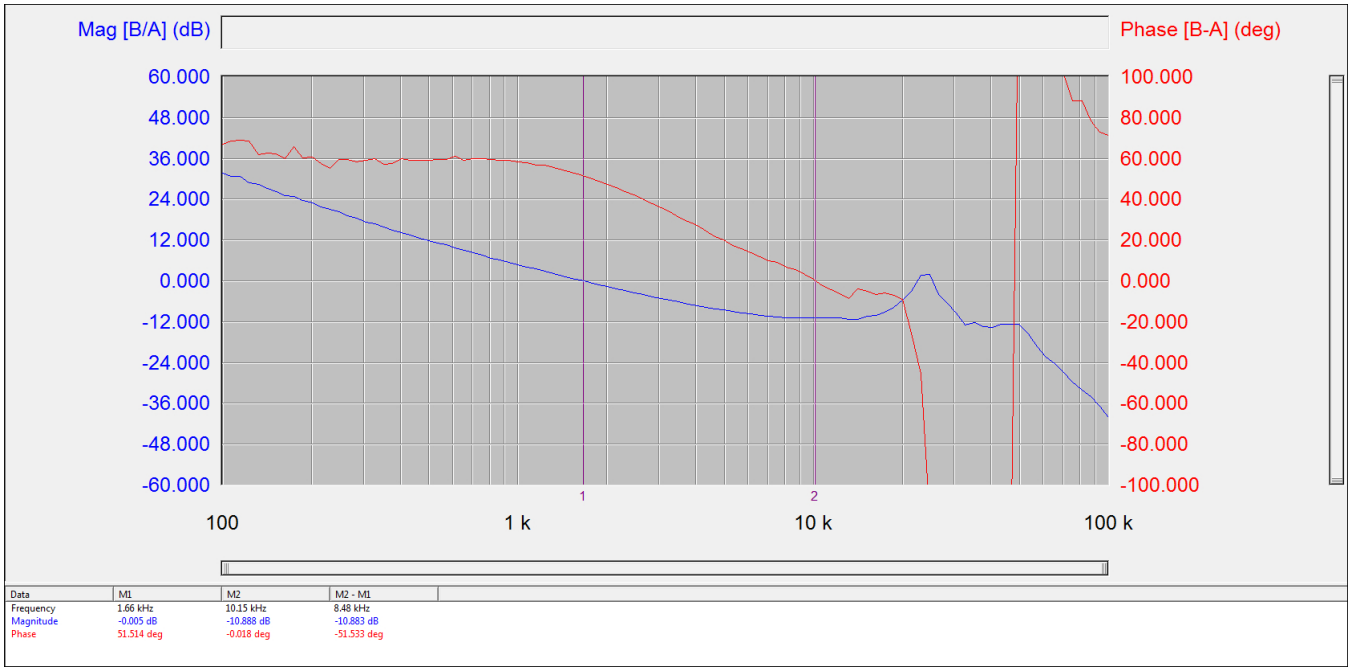


図 40. 9-V Input, 40-V Output, 10-A Load: 51.51-Degree Phase Margin, –10.89-dB Gain Margin

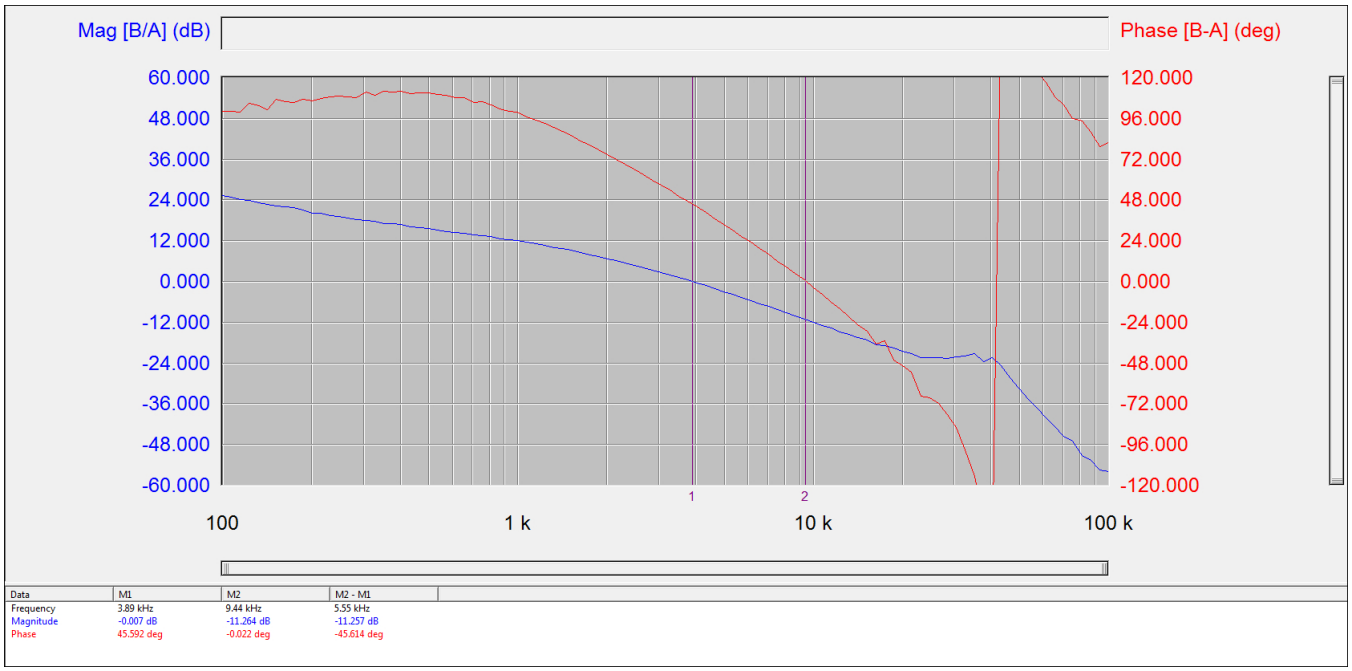


図 41. 12-V Input, 16-V Output, 10-A load: 45.6-Degree Phase Margin, –11.26-dB Gain Margin

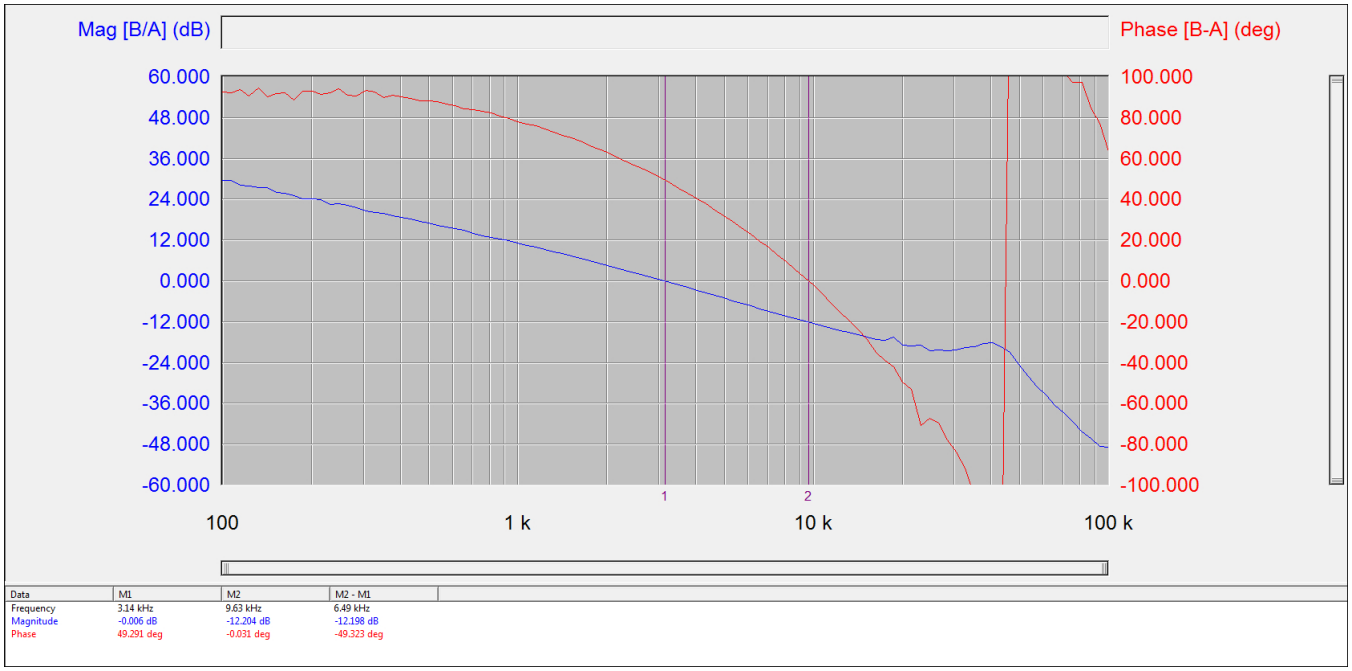


図 42. 12-V Input, 24-V Output, 10-A Load: 49.29-Degree Phase Margin, –12.204-dB Gain Margin

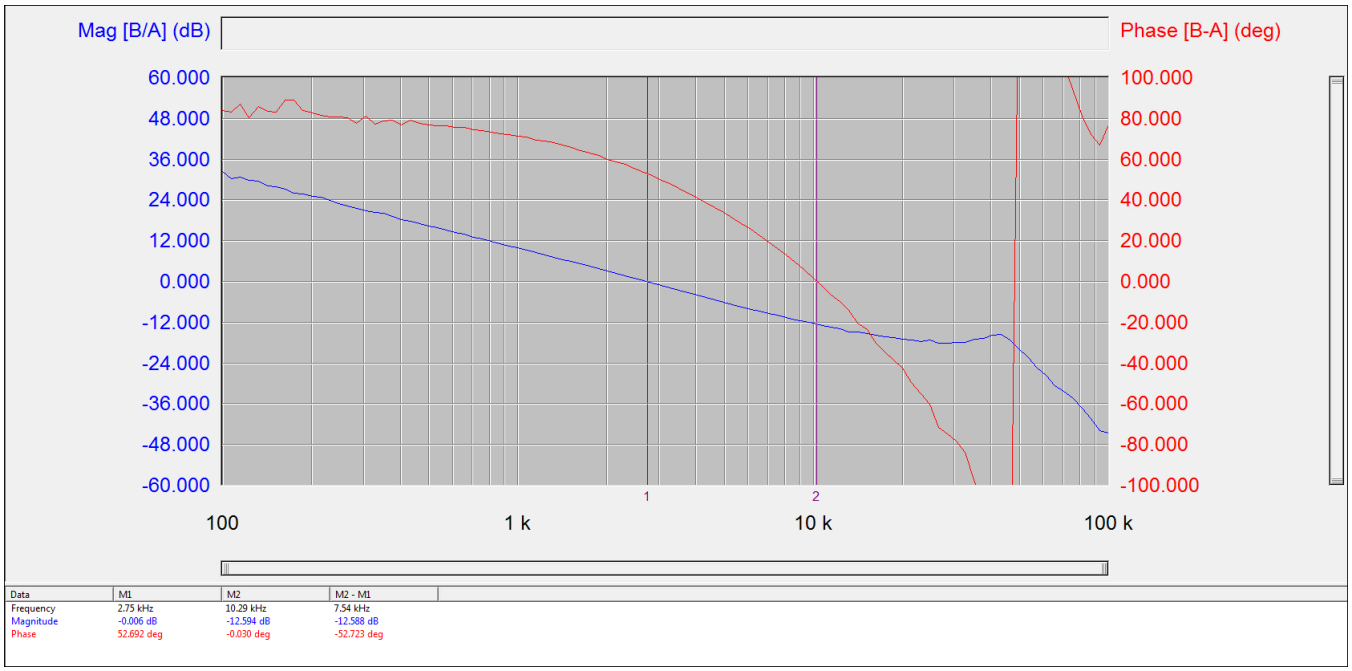


図 43. 12-V Input, 30-V Output, 10-A Load: 52.69-Degree Phase Margin, –12.59-dB Gain Margin

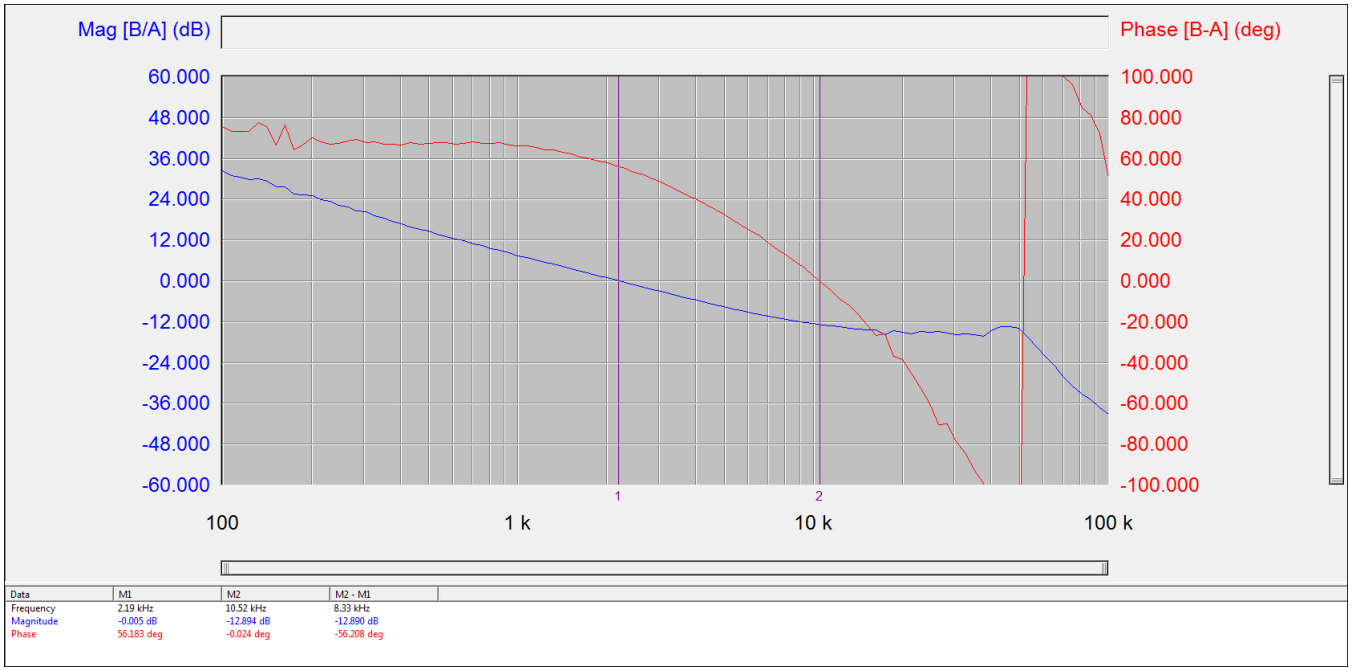


図 44. 12-V Input, 40-V Output, 10-A Load: 56.18-Degree Phase Margin, –12.89-dB Gain Margin

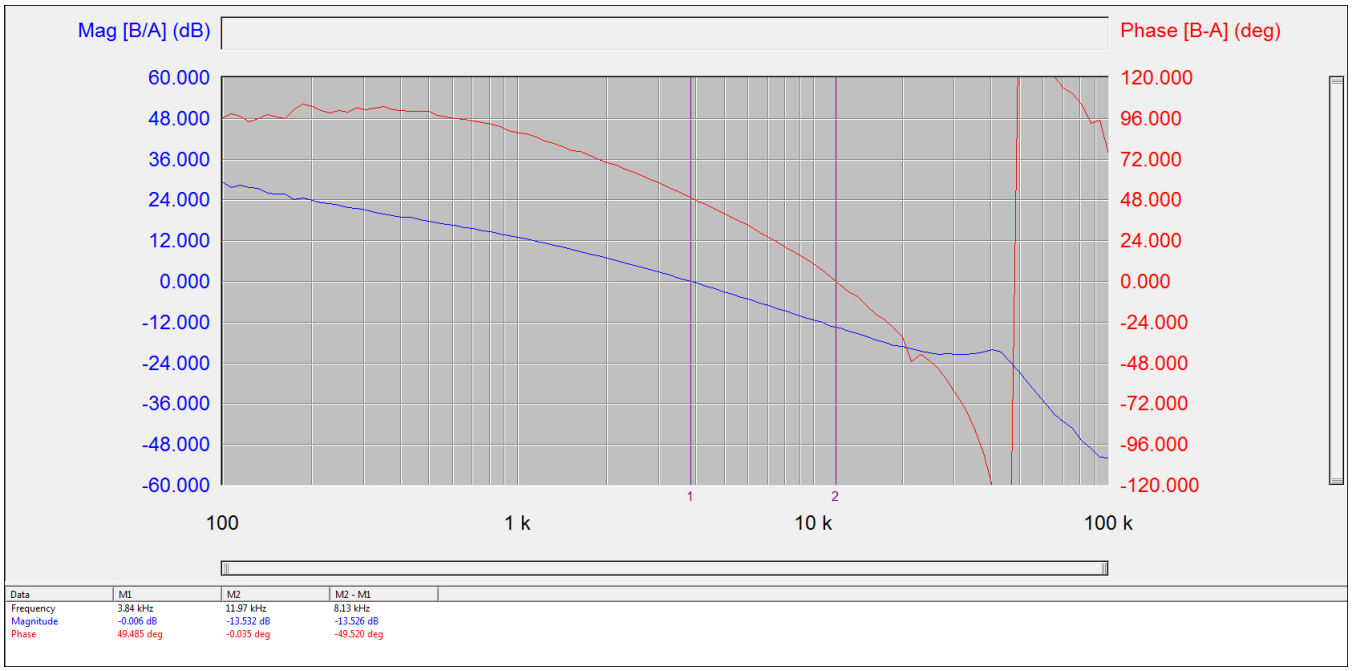


図 45. 16-V Input, 24-V Output, 10-A Load: 49.49-Degree Phase Margin, –13.53-dB Gain Margin

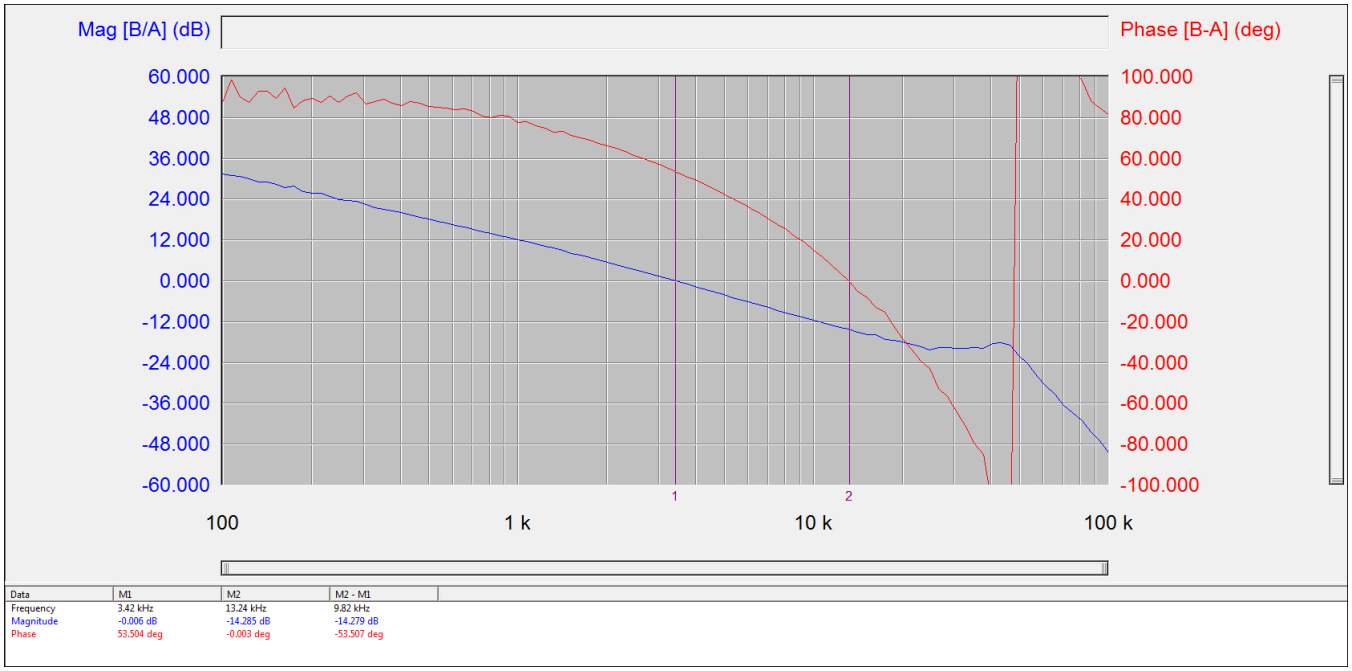


図 46. 16-V Input, 30-V Output, 10-A Load: 53.51-Degree Phase Margin, –14.29-dB Gain Margin

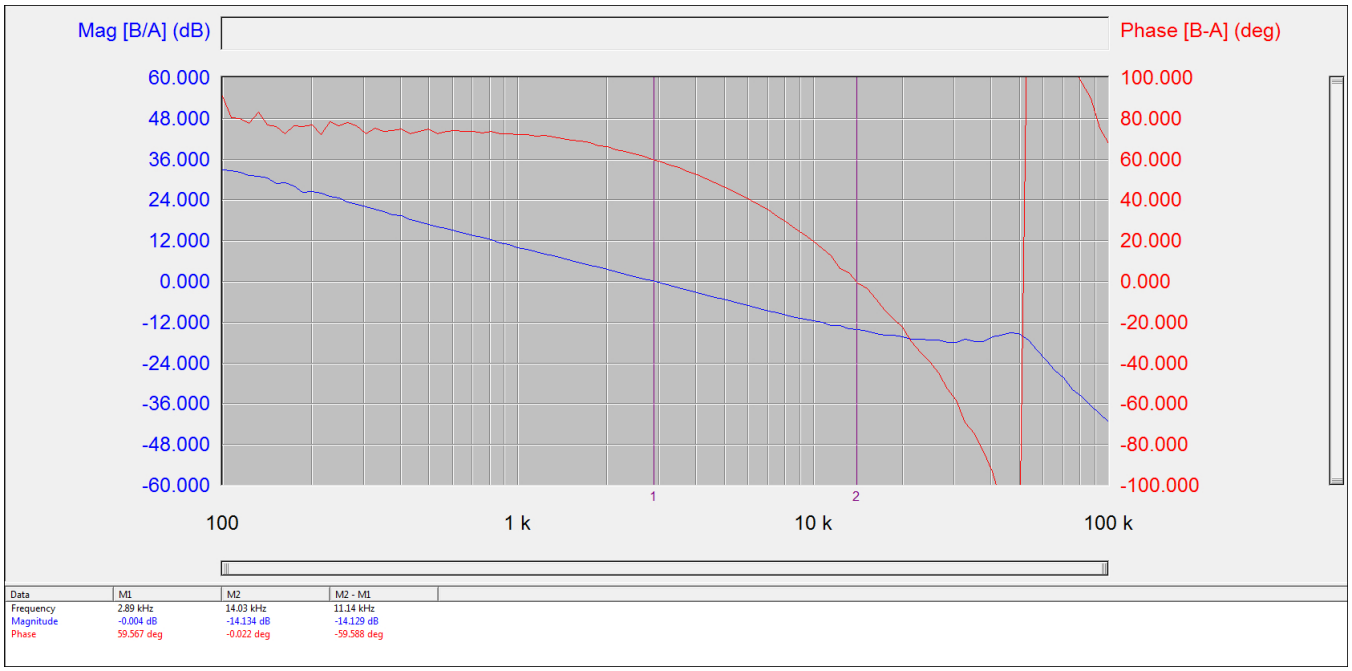


図 47. 16-V Input, 40-V Output, 10-A Load: 59.57-Degree Phase Margin, –14.13-dB Gain Margin

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01610.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01610.

4.3 PCB Layout Recommendations

The PCB is a four-layer board with routing on all four layers. All components are placed on the top layer. The input caps, current sense resistors R2 and R23, inductors L1 and L2, the synchronous rectifier transistors, and the output capacitors are placed so that the copper traces are as short as possible and the current loop from the input capacitor ground to the output capacitor ground is short. Multiple large vias are used to ensure low impedance where high current nets change layers on the PCB. The switch transistors also form a short path from the input inductor to ground between the input and output capacitors. Because the LM25122-Q1 boost controllers are not in the high current path, they are placed away from the main current loop. All high current paths have large copper areas to minimize impedance. V_{OUT} is connected to the output filter on this layer.

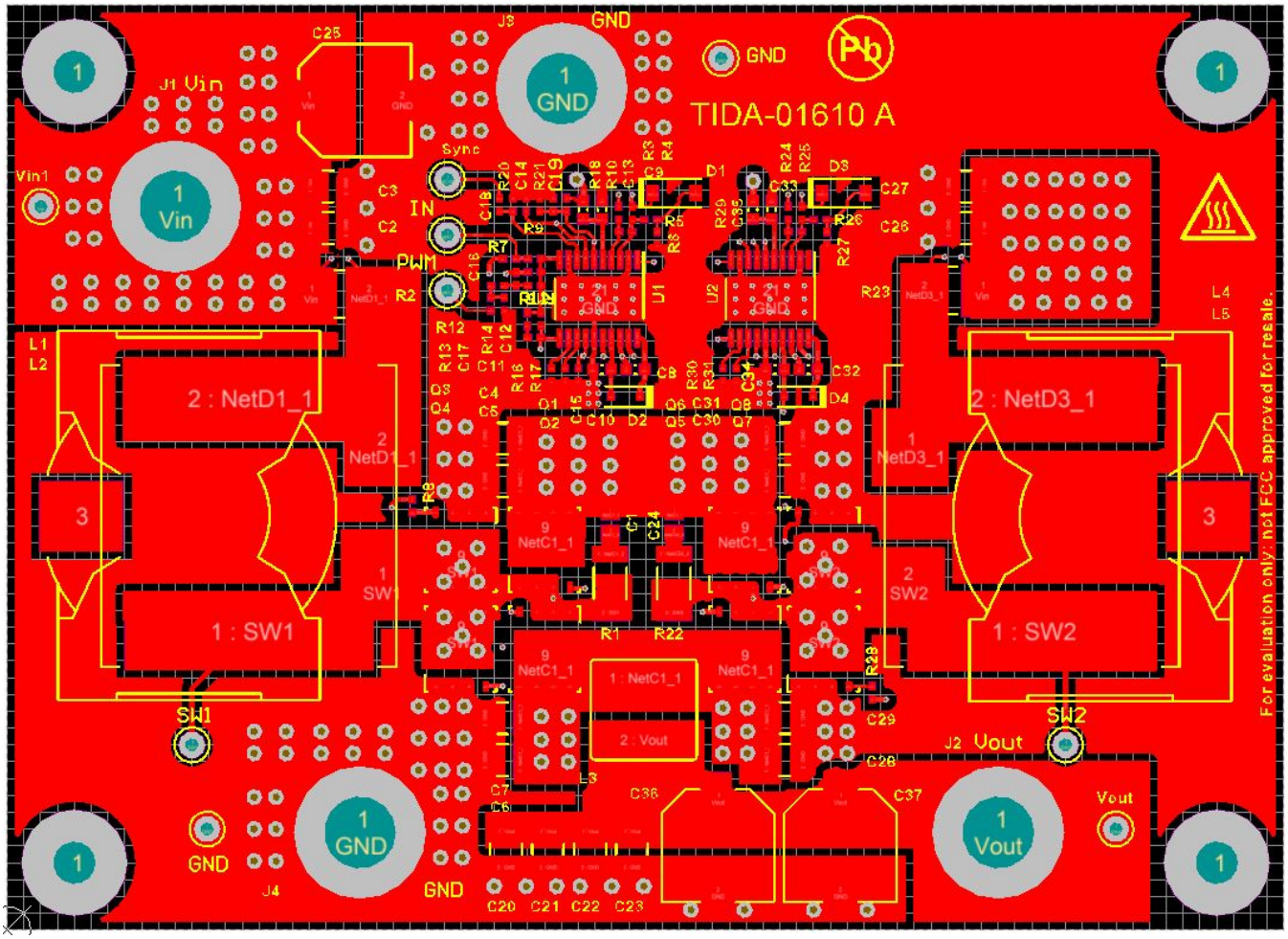


図 48. PCB Top Layer

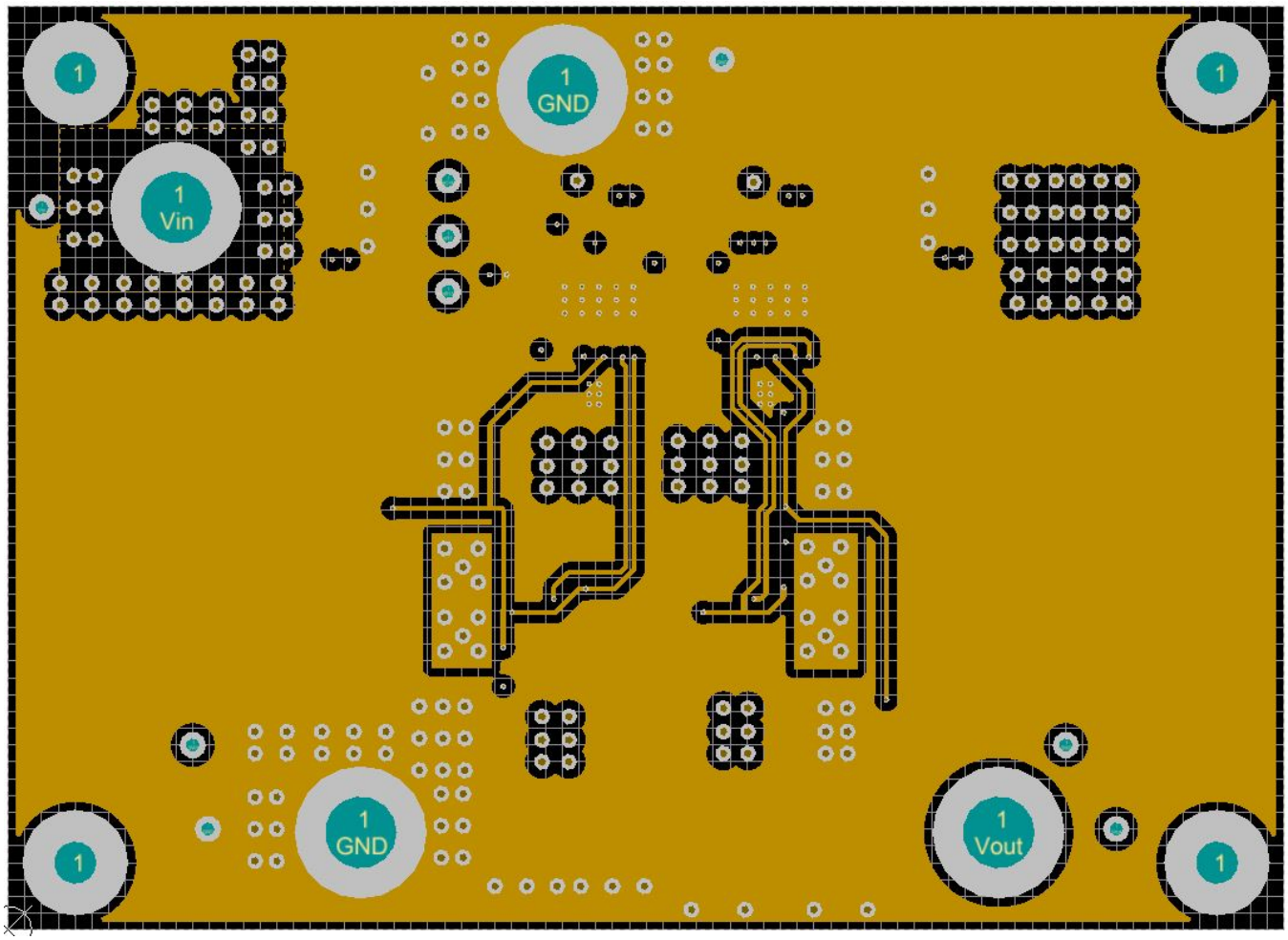


図 49. PCB Layer 2

On layer 2, HO1 is routed next to the part of SW1 that connects from U1 to Q1 and Q2, and HO2 and SW2 are routed in a similar manner from U2 to Q5 and Q6. LO1 and LO 2 are also routed on this layer. The large copper pour on this layer is ground.

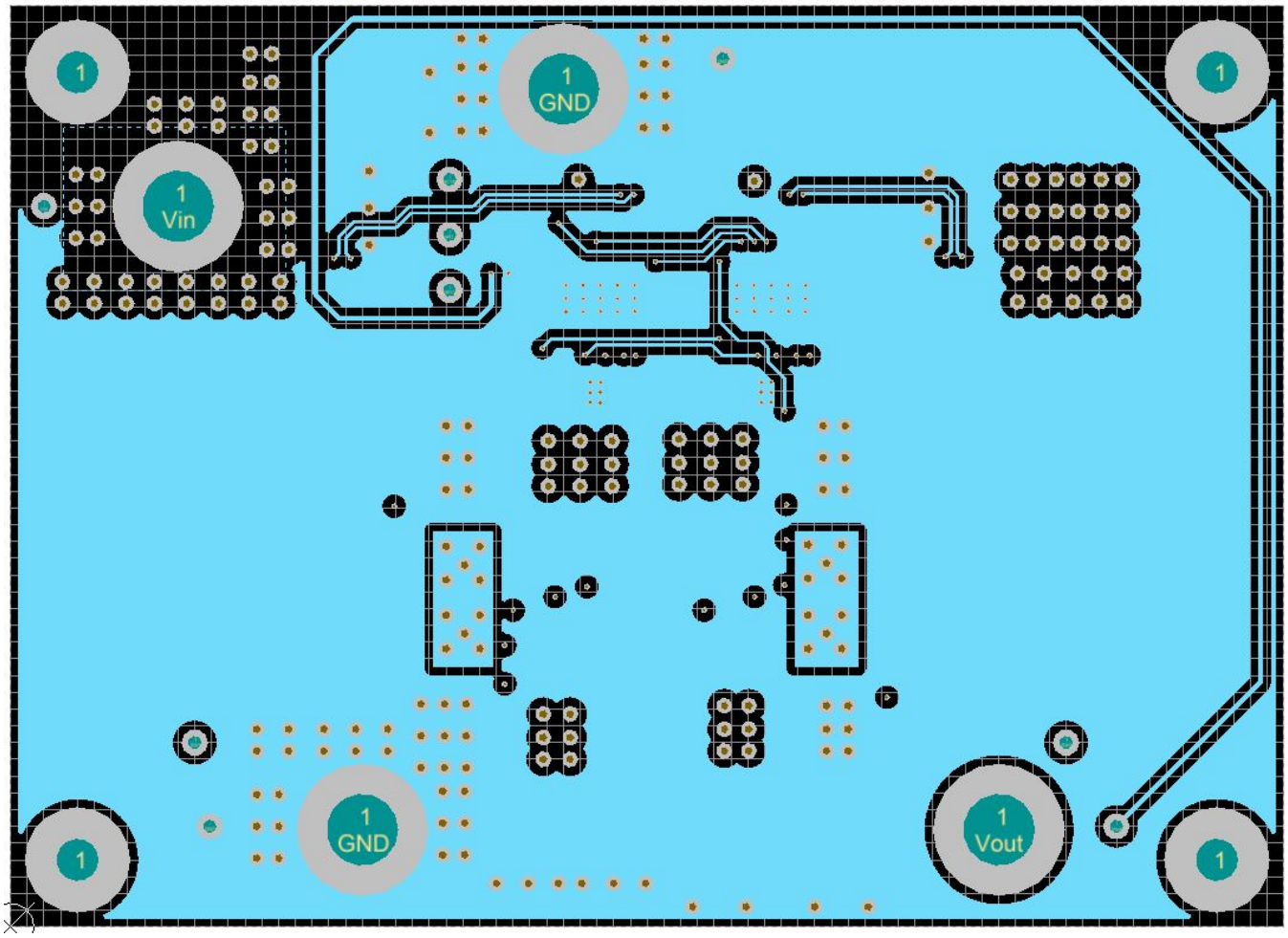


図 50. PCB Layer 3

PCB layer 3 contains the signals shared by U1 and U2. The pairs of nets toward the top are the Kelvin connections from current sense resistors R2 and R23. One connection in each pair is connected to V_{IN}. The vias for these connections fall inside of a V_{IN} plane that is on the bottom layer. Because of this, cutouts are placed around the four vias so that they do not connect to the plane. If they did, the current measurement would not be accurate due to the voltage not being sensed right at the resistors. Most of layer 3 is ground. The bottom has a plane for V_{IN}, a plane for net C1-1 (which is the connection point of the two output phases), and a ground plane.

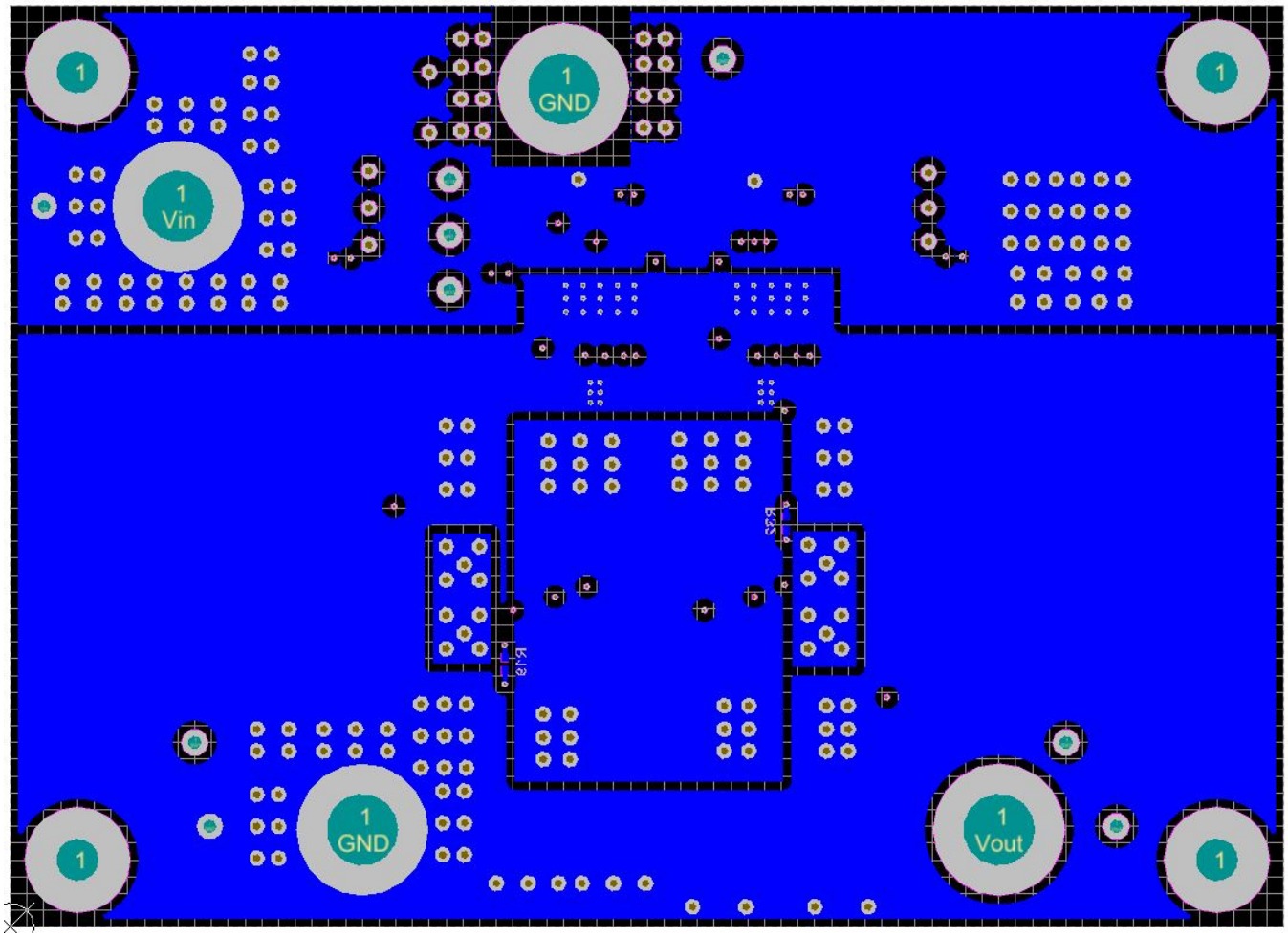


図 51. PCB Bottom Layer

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01610.

4.4 Altium Project Files

To download the Altium project files, see the design files at TIDA-01610.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01610.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01610.

5 商標

E2E is a trademark of Texas Instruments.
すべての商標および登録商標はそれぞれの所有者に帰属します。

6 About the Authors

MARK KNAPP is a systems architect at Texas Instruments Incorporated who specializes in automotive premium audio systems and instrument clusters. He also has an extensive background in video camera systems and infrared imaging systems for military, automotive, and industrial applications. Mark earned his BSEE at the University of Michigan-Dearborn and his MSEE at the University of Texas at Dallas.

XINYU DAI has a system application role at Texas Instruments Incorporated and specializes in designing various power supply topologies for industrial, consumer, and automotive applications. His background includes kilowatt multi-phase designs, compact designs for personal electronics, and EMI optimized designs for automotive applications. Xinyu earned his BSEE at the Georgia Institute of Technology with high honor.

TIの設計情報およびリソースに関する重要な注意事項

Texas Instruments Incorporated ("TI")の技術、アプリケーションその他設計に関する助言、サービスまたは情報は、TI製品を組み込んだアプリケーションを開発する設計者に役立つことを目的として提供するものです。これにはリファレンス設計や、評価モジュールに関係する資料が含まれますが、これらに限られません。以下、これらを総称して「TIリソース」と呼びます。いかなる方法であっても、TIリソースのいずれかをダウンロード、アクセス、または使用した場合、お客様(個人、または会社を代表している場合にはお客様の会社)は、これらのリソースをここに記載された目的にのみ使用し、この注意事項の条項に従うことに合意したものとします。

TIによるTIリソースの提供は、TI製品に対する該当の発行済み保証事項または免責事項を拡張またはいかなる形でも変更するものではなく、これらのTIリソースを提供することによって、TIにはいかなる追加義務も責任も発生しないものとします。TIは、自社のTIリソースに訂正、拡張、改良、およびその他の変更を加える権利を留保します。

お客様は、自らのアプリケーションの設計において、ご自身が独自に分析、評価、判断を行う責任がお客様にあり、お客様のアプリケーション(および、お客様のアプリケーションに使用されるすべてのTI製品)の安全性、および該当するすべての規制、法、その他適用される要件への遵守を保証するすべての責任をお客様のみが負うことを理解し、合意するものとします。お客様は、自身のアプリケーションに関して、(1) 故障による危険な結果を予測し、(2) 障害とその結果を監視し、および、(3) 損害を引き起こす障害の可能性を減らし、適切な対策を行う目的での、安全策を開発し実装するために必要な、すべての技術を保持していることを表明するものとします。お客様は、TI製品を含むアプリケーションを使用または配布する前に、それらのアプリケーション、およびアプリケーションに使用されているTI製品の機能性を完全にテストすることに合意するものとします。TIは、特定のTIリソース用に発行されたドキュメントで明示的に記載されているもの以外のテストを実行していません。

お客様は、個別のTIリソースにつき、当該TIリソースに記載されているTI製品を含むアプリケーションの開発に関連する目的でのみ、使用、コピー、変更することが許可されています。明示的または黙示的を問わず、禁反言の法理その他どのような理由でも、他のTIの知的所有権に対するその他のライセンスは付与されません。また、TIまたは他のいかなる第三者のテクノロジまたは知的所有権についても、いかなるライセンスも付与されるものではありません。付与されないものには、TI製品またはサービスが使用される組み合わせ、機械、プロセスに関連する特許権、著作権、回路配置利用権、その他の知的所有権が含まれますが、これらに限られません。第三者の製品やサービスに関する、またはそれらを参照する情報は、そのような製品またはサービスを利用するライセンスを構成するものではなく、それらに対する保証または推奨を意味するものでもありません。TIリソースを使用するため、第三者の特許または他の知的所有権に基づく第三者からのライセンス、もしくは、TIの特許または他の知的所有権に基づくTIからのライセンスが必要な場合があります。

TIのリソースは、それに含まれるあらゆる欠陥も含めて、「現状のまま」提供されます。TIは、TIリソースまたはその仕様に関して、明示的か暗黙的かにかかわらず、他のいかなる保証または表明も行いません。これには、正確性または完全性、権原、続発性の障害に関する保証、および商品性、特定目的への適合性、第三者の知的所有権の非侵害に対する黙示の保証が含まれますが、これらに限られません。

TIは、いかなる苦情に対しても、お客様への弁護または補償を行う義務はなく、行わないものとします。これには、任意の製品の組み合わせに関連する、またはそれらに基づく侵害の請求も含まれますが、これらに限られず、またその事実についてTIリソースまたは他の場所に記載されているか否かを問わないものとします。いかなる場合も、TIリソースまたはその使用に関連して、またはそれらにより発生した、実際的、直接的、特別、付随的、間接的、懲罰的、偶発的、または、結果的な損害について、そのような損害の可能性についてTIが知らされていたかどうかにかかわらず、TIは責任を負わないものとします。

お客様は、この注意事項の条件および条項に従わなかったために発生した、いかなる損害、コスト、損失、責任からも、TIおよびその代表者を完全に免責するものとします。

この注意事項はTIリソースに適用されます。特定の種類の資料、TI製品、およびサービスの使用および購入については、追加条項が適用されます。これには、半導体製品(http://www.ti.com/sc/docs/stdterms.htm)、評価モジュール、およびサンプル(http://www.ti.com/sc/docs/sampterms.htm)についてのTIの標準条項が含まれますが、これらに限られません。