参考資料

TI Designs: TIDA-080002
ウルトラ・モバイル、低消費電力DLP Pico qHDディスプレイのリファレンス・デザイン

概要

この0.23 qHD DLPチップセットは、組み込みホスト・プロセッサとともにDLPテクノロジを使用するための安価なプラットフォームです。 このチップセットにより、各種のアプリケーション向けにオンデマンド、フリー・フォームの低消費電力サブシステム・ディスプレイを実現できます。

リソース

TIDA-080002	デザイン・フォルダ
DLP230GP (DMD)	プロダクト・フォルダ
DLPC3432	プロダクト・フォルダ
DLPA3000	プロダクト・フォルダ

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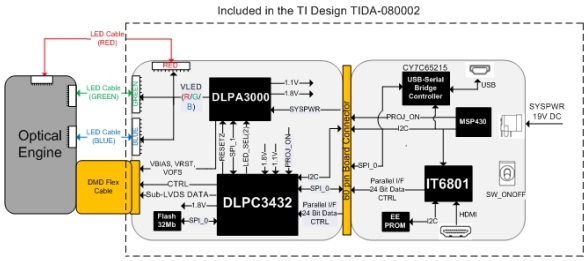
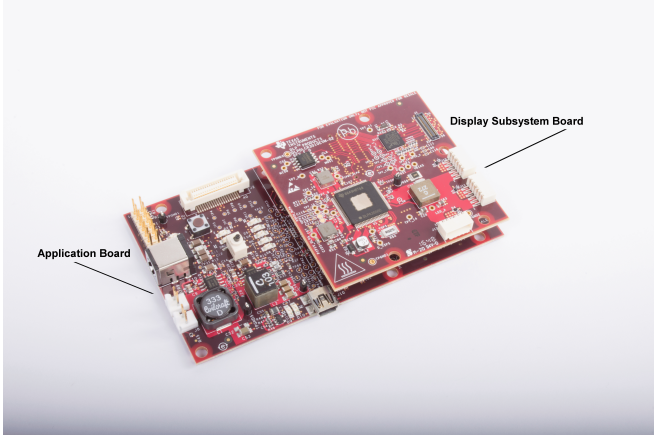
特長

- ディスプレイ・サブシステムDLP230GP (qHD解像度)
- コンパクトなPCBレイアウトでqHD (DLP230GP)光学エンジンをサポートし、HDMIおよびUSB接続機能を搭載
- 19V入力と、最大6AのLED駆動電流

アプリケーション

- パーソナル・エレクトロニクス:
  - スマートフォンおよびタブレット
  - バッテリ駆動のモバイル・アクセサリ
  - ウェアラブル(ニアアイ)ディスプレイ
  - スマート・スピーカー
- 産業用:
  - 家電製品





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1 System Description

The 0.3-inch TRP HD 720p display chipset enables the use of DLP technology in a variety of applications that require HD resolution, low power, and small form factors. This reference design provides developers with the ability to quickly implement HD display subsystems at higher brightness levels using the DLPA3000 PMIC and LED driver.

1.1 Applications for Mobile Smart TVs and Mobile Projectors

Smart home is a broad category of products and services that bring automation and interconnectivity to a variety of devices in the home, such as lighting, thermostats, appliances, and entertainment devices.

Bringing smart displays based on DLP Pico™ technology into the home can offer many benefits such as interactive, adaptive, and reconfigurable interfaces that can replace buttons, tablets, LCD panels, and mechanical knobs in virtually every room of the house. DLP technology-based smart displays offer advantages in brightness, resolution, small form factor, low power consumption, throw ratio, and interactivity.

Find more about smart home displays using DLP technology in the white paper *TI DLP Pico technology for smart home applications* (DLPC101).

表 1. DLP Features and Design Benefits for Smart Home Applications

DLP FEATURE	DESIGN BENEFIT
Displays of any shape on virtually any surface	Smart displays using DLP chips can project directly onto existing surfaces in the home, delivering convenient information just about anywhere.
On-demand display	Smart home projection can instantly provide a display without the intrusion of a permanent display panel. In addition, DLP Pico technology enables small optical module designs that can be tucked out of sight or be integrated into existing home devices.
High optical efficiency	Digital micromirror devices (DMDs) incorporate highly reflective and polarization agnostic aluminum micromirrors, which enable bright, power-efficient, compact smart home display systems.
High resolution	DLP Pico DMDs enable high-resolution projected images—up to full HD 1080p resolution.
Solid-state illumination compatible	DLP chips are compatible with solid-state illumination, such as LEDs and lasers, which further enables compact sizes and long illumination lifetimes.

1.2 Applications for Wearable Displays

Wearable displays are devices that are worn as a helmet, headset, or glasses by the user and create an image in the user's field of view. The display can either be see-through (augmented reality) or opaque (immersive or virtual reality). Products in this category include head-mounted displays (HMDs) and near-eye displays.

The DLP Pico chip is a reflective microdisplay technology used in the optical module in a wearable display. It is typically illuminated by RGB LEDs, and intelligently reflects light through pupil forming optics into a final optical element, such as a waveguide or curved combiner, which relays the image into the eye. DLP Pico technology enables bright, high contrast, low power HMDs with fast refresh rates.

表 2. DLP Features and Design Benefits for Wearable Displays

DLP FEATURE	DESIGN BENEFIT
High contrast	Optical modules designed with DLP Pico chips can achieve full on/off contrast ratios of over 1000:1, depending on the system design. In an augmented reality wearable display, high contrast ratios enable a highly transparent display background even at high brightness levels.

表 2. DLP Features and Design Benefits for Wearable Displays (continued)

DLP FEATURE	DESIGN BENEFIT
High optical efficiency	Digital micromirror devices (DMDs) incorporate highly reflective and polarization agnostic aluminum micromirrors, which enable bright, power efficient wearable displays. DLP Pico technology is a particularly good fit for wearable displays that demand high brightness over a medium to large field of view.
High speed: Fast refresh rates, low latency	DLP Pico chipsets support frame rates up to 240 Hz, depending on the input resolution, and enable low latency display systems. The high switching speed of DLP micromirrors reduces motion blur.
Low power consumption	The DLP2010 and DLP3010 have total chipset (DMD + controller) power consumption of under 350 mW. In addition, the chips' high optical efficiency decreases the illumination power required to reach a desired brightness level.
Small size, high resolution	With micromirrors as small as 5.4µm, DLP Pico chips deliver resolutions up to 1080p while enabling very compact optical engine designs that meet the space-constrained demands of wearable displays.

1.3 Applications for Pico Projector Accessory and Mobile Attachments

Accessory and mobile-attached pico projectors can be used as a portable big-screen display for any device with video output, such as laptops, smartphones, tablets, and gaming consoles. They can offer users an easy and lightweight means to project large and colorful video in a variety of settings.

表 3. DLP Features and Design Benefits for Pico Projector Accessory and Mobile Attachments

DLP FEATURE	DESIGN BENEFIT
Small size, high resolution	With micromirrors as small as 5.4 µm, DLP Pico chips deliver high resolution projected images (up to full HD 1080p) while enabling very compact projection designs.
High optical efficiency	Digital micromirror devices (DMDs) contain highly reflective and polarization agnostic aluminum micromirrors, which enable bright, battery-powered pico projection systems.
High contrast	Optical modules designed with DLP Pico DMDs can achieve full on/off contrast ratios of over 1000:1, depending on system optical design. Higher contrast translates to more vivid colors and darker blacks.
DLP IntelliBright(TM) algorithms	A suite of image processing algorithms designed to help optimize image brightness, contrast, and power consumption. DLP IntelliBright algorithms can boost brightness by up to 50% without increasing power consumption. For more information, read the DLP IntelliBright application note.
Mature ecosystem	A mature global ecosystem of established optical module manufactures eases the design process and allows product developers to go to market faster by utilizing an existing, off-the-shelf optical engine that is already in production.

2 System Overview

2.1 Block Diagram

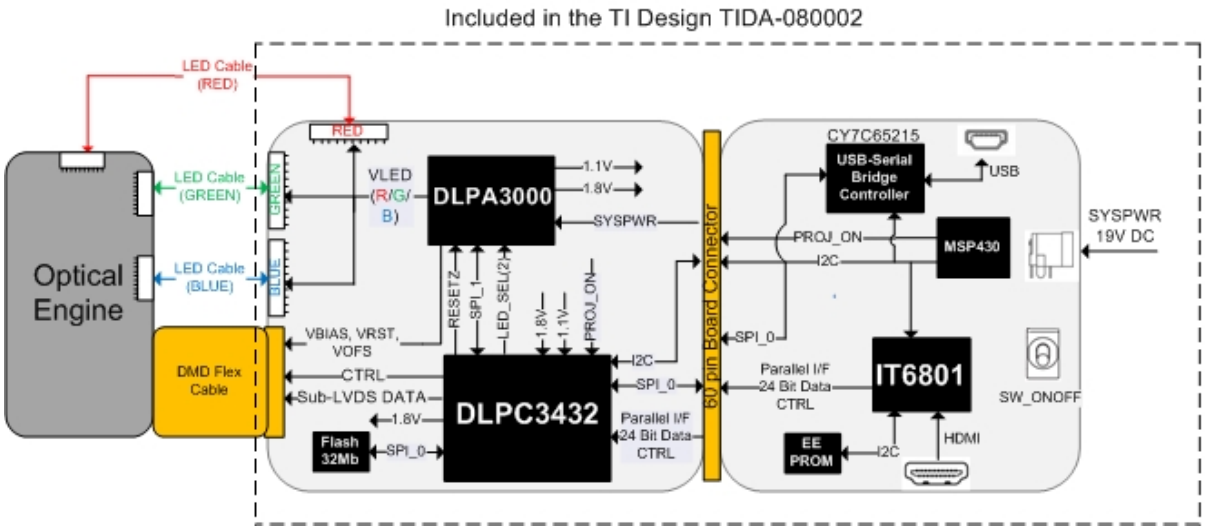


図 1. TIDA-080002 Block Diagram

2.2 Design Considerations

See the following documents for considerations in DLP system design:

- *TI DLP® Pico™ System Design: Optical Module Specifications*
- *TI DLP® System Design: Brightness Requirements and Tradeoffs*

2.3 Highlighted Products

This chipset reference design guide draws upon figures and content from several other published documents related to the 0.23-in qHD DLP chipset. For a list of these documents, see 6.

3 Hardware, Software and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

This design requires the connection of an optical engine with a DLP230GP DMD and LEDs. The hardware in this TI Design cannot be operated otherwise. Ensure that the flex cable of the optical engine is compatible to the flex cable connector J1 on the PCB. For a list of optical module manufacturers visit our Optical modules page.

The p23 qHD PCB design is based on the DLPDLCR3010EVM-G2. The DLPDLCR3010EVM-G2 can be used with the p23 qHD DMD by replacing the DLPC3433 display controller with the DLPC3432 display controller. The correct firmware has to be used for each system.

1. After connecting the optical engine, power up the p23 qHD PCB by applying an external DC power supply (19-V DC, 4.75 A) to the J9 connector.
   External power supply requirements:
   - Nominal output voltage: 19-V DC
   - Minimum output current: 2.5 A; max output current: 4.74 A
   - Efficiency level: VI

   注: TI recommends using an external power supply that complies with applicable regional safety standards such as UL, CSA, VDE, CCC, PSE, and so on.

   注: The system is designed to operate also with an external 12-V DC power supply. The P5V_VIN (D9) and P3P3V_SB (D10) LED will turn on to indicate that 5-V and 3.3-V standby power is applied.
2. Move SW2 switch to the ON position to turn on the p23 qHD DLP chipset. When the p23 qHD chipset is turned on, the PROJ_ON LED (D4) will turn on.
3. After the p23 qHD chipset is turned on, the projector will default to displaying a DLP display splash image.
4. When turning off the projector, turn off the SW2 switch prior to removing the power cable.

   注: To avoid potential damage to the DMD, it is recommended to turn off the projector with the SW2 switch before disconnecting the power.

There are ten indicator LEDs on the p23 qHD PCB and they are defined in 表 4:

表 4. LEDs on the TIDA-080002 Hardware

LED REFERENCE	SIGNAL INDICATION	DESCRIPTION
D1	MSP_LED2_ON	ON when HDMI cable is plugged in and external video is detected, OFF when external video is not detected.
D2	HOST_IRQ	ON during DLPC3432 boot, OFF when projector is running. Indication of DLPC3432 boot-up completed and ready to receive commands
D3	RESETZ	OFF when projector is turned on through SW_ONOFF
D4	PROJ_ON	ON when projector is turned on through SW_ONOFF
D5	GPIO1	Blinking when PC is communicating to flash over SPI
D6	GPIO0	Blinking when PC is communicating to DLPC3432 over I^2C
D7	MSP430_ACK	ON when Cypress CY3420 is I^2C master. OFF when the MSP430™ MCU is I^2C master
D8	MSP430_REQ	ON when Cypress CY3420 requests the MSP430 MCU to give Cypress master control of the I^2C bus
D9	P5V_VIN	Regulated 5-V power on
D10	P3P3V_SB	Regulated 3.3-V power on

3.1.2 Software

The software required for this reference design is available for download on the TIDA-080002. It includes the firmware for the DLPC3432 and the MSP430F5529. The MSP430 controls proj-on and sets up the DLPC3432 for HDMI. The firmware provided for the DLPC3432 sets the LED current by default to 3 A. It has to be ensured that the LEDs connected to this design are rated for this current setting.

3.2 Testing and Results

The results of a successful test of this system is the appearance on the display of the splash screen, as shown in 図 2.

図 2. 0.23-qHD Board Splash Screen

The chipset enables a low power and high optical efficiency. The optical efficiency can vary up to 10-25 lumens/watt based on the optical engine design and LEDs used in the system. Power consumption numbers can be found in the DLP chipset datasheets as specified in 6.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-080002.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-080002.

4.3 PCB Layout Recommendations

The layout guidelines listed in this design guide are subsets of the guidelines included in the component data sheets. For more information, refer to the DLPC3432, DLP230GP, and DLPA3000 data sheets.

4.3.1 DLPC3432 Layout Guidelines

4.3.1.1 Internal ASIC PLL Power

The following guidelines are recommended to achieve desired ASIC performance relative to the internal PLL. The DLPC3432 contains two internal PLLs, which have dedicated analog supplies (VDD_PLLM, VSS_PLLM, VDD_PLLD, VSS_PLLD). As a minimum, VDD_PLLx power and VSS_PLLx ground pins must be isolated using a simple passive filter consisting of two series ferrites and two shunt capacitors (to widen the spectrum of noise absorption). It is recommended that one capacitor be a 0.1-µF capacitor and the other be a 0.01-µF capacitor. Place all four components as close to the ASIC as possible; however, it is especially important to keep the leads of the high-frequency capacitors as short as possible. Note that both capacitors must be connected across VDD_PLLM and VSS_PLLM or VDD_PLLD and VSS_PLLD respectively on the ASIC side of the ferrites.

For the ferrite beads used, their respective characteristics should be as follows:

- DC resistance less than 0.40 Ω
- Impedance at 10 MHz equal to or greater than 180 Ω
- Impedance at 100 MHz equal to or greater than 600 Ω

The PCB layout is critical to PLL performance. It is vital that the quiet ground and power are treated like analog signals. Therefore, VDD_PLLM and VDD_PLLD must be a single trace from the DLPC3432 to both capacitors and then through the series ferrites to the power source. The power and ground traces should be as short as possible, parallel to each other, and as close as possible to each other.

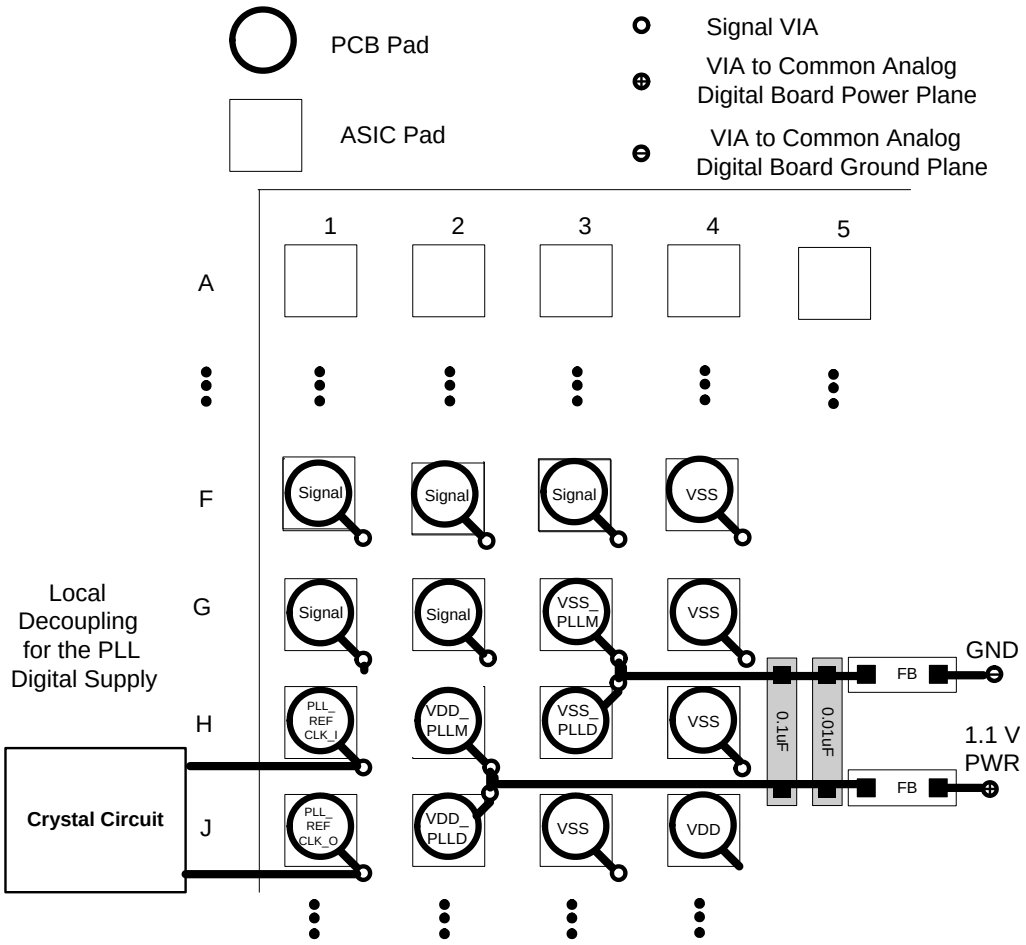


図 3. PLL Filter Layout

4.3.1.2 I²C Interface Performance

Both DLPC3432 I²C interface ports support a 100-kHz baud rate. By definition, I²C transactions operate at the speed of the slowest device on the bus, thus there is no requirement to match the speed grade of all devices in the system.

4.3.1.3 DMD Interface Considerations

The sub-LVDS HS interface waveform quality and timing on the DLPC3432 ASIC is dependent on the total length of the interconnect system, the spacing between traces, the characteristic impedance, etch losses, and how well matched the lengths are across the interface. Thus, ensuring positive timing margin requires attention to many factors.

As an example, DMD interface system timing margin can be calculated as follows:

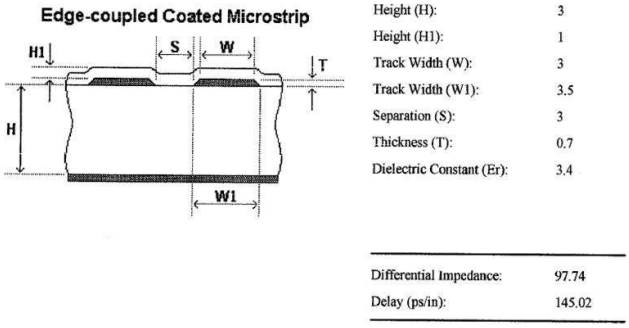
Setup Margin = (DLPC3432 output setup) – (DMD input setup) – (PCB routing mismatch) – (PCB SI degradation) (1)

Hold-time Margin = (DLPC3432 output hold) – (DMD input hold) – (PCB routing mismatch) – (PCB SI degradation)

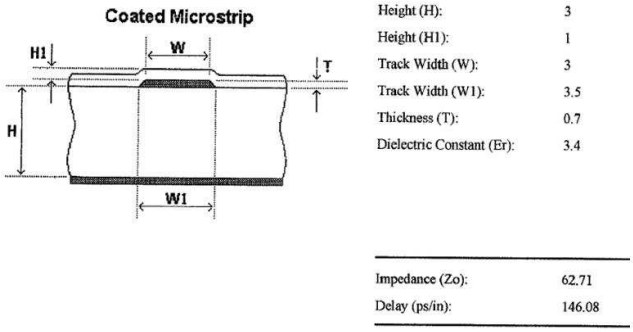
where PCB SI degradation is signal integrity degradation due to PCB effects, which includes such things as simultaneously switching output (SSO) noise, crosstalk, and inter-symbol interference (ISI) noise. (2)

DLPC3432 I/O timing parameters as well as DMD I/O timing parameters can be found in their corresponding data sheets. Similarly, PCB routing mismatch can be budgeted and met through controlled PCB routing. However, PCB SI degradation is a more complicated adjustment.

In an attempt to minimize the signal integrity analysis that would otherwise be required, the following PCB design guidelines are provided as a reference of an interconnect system that satisfy both waveform quality and timing requirements (accounting for both PCB routing mismatch and PCB SI degradation). Variation from these recommendations can also work, but must be confirmed with PCB signal integrity analysis or lab measurements.



DMD_HS Differential Signals



DMD_LS Signals

図 4. DMD Interface Board Stack-Up Details

4.3.1.4 General Handling Guidelines for Unused CMOS-Type Pins

To avoid potentially damaging current caused by floating CMOS input-only pins, TI recommends that the user tie unused ASIC input pins through a pullup resistor to their associated power supply or a pulldown resistor to ground. For ASIC inputs with internal pullup or pulldown resistors, do not add an external pullup or pulldown resistor unless specifically recommended.

注: Internal pullup and pulldown resistors are weak and must not be expected to drive the external line. The DLPC3432 device implements very few internal resistors, and these are noted in the pin list. When external pullup or pulldown resistors are needed for pins that have built-in weak pullups or pulldowns, use the value 8 kΩ (max).

Never tie unused output-only pins directly to power or ground. These pins can be left open.

When possible, TI recommends that unused bidirectional I/O pins be configured to their output state such that the pin can be left open. If this control is not available and the pins can become an input, then the pins must be pulled up (or pulled down) using an appropriate, dedicated resistor.

4.3.1.5 Maximum Pin-to-Pin, PCB Interconnects Etch Lengths

表 5. Max Pin-to-Pin PCB Interconnect Recommendations(1)(2)

DMD BUS SIGNAL	SIGNAL INTERCONNECT TOPOLOGY		UNIT
	SINGLE BOARD SIGNAL ROUTING LENGTH	MULTI-BOARD SIGNAL ROUTING LENGTH	
DMD_HS_CLK_P DMD_HS_CLK_N	6.0 152.4	See (3)	inch (mm)
DMD_HS_WDATA_A_P DMD_HS_WDATA_A_N	6.0 152.4	See (3)	inch (mm)
DMD_HS_WDATA_B_P DMD_HS_WDATA_B_N			
DMD_HS_WDATA_C_P DMD_HS_WDATA_C_N			
DMD_HS_WDATA_D_P DMD_HS_WDATA_D_N			
DMD_HS_WDATA_E_P DMD_HS_WDATA_E_N			
DMD_HS_WDATA_F_P DMD_HS_WDATA_F_N			
DMD_HS_WDATA_G_P DMD_HS_WDATA_G_N			
DMD_HS_WDATA_H_P DMD_HS_WDATA_H_N			
DMD_LS_CLK	6.5 165.1	See (3)	inch (mm)
DMD_LS_WDATA	6.5 165.1	See (3)	inch (mm)
DMD_LS_RDATA	6.5 165.1	See (3)	inch (mm)
DMD_DEN_ARSTZ	7.0 177.8	See (3)	inch (mm)

(1) Max signal routing length includes escape routing.
(2) Multi-board DMD routing length is more restricted due to the impact of the connector.
(3) Due to board variations, these are impossible to define. Any board designs should SPICE simulate with the ASIC IBIS models to ensure single routing lengths do not exceed requirements.

表 6. High-Speed PCB Signal Routing Matching Requirements(1)(2)(3)(4)

INTERFACE	SIGNAL GROUP	REFERENCE SIGNAL	MAX MISMATCH(5)	UNIT
DMD	DMD_HS_WDATA_A_P DMD_HS_WDATA_A_N	DMD_HS_CLK_P DMD_HS_CLK_N	±1.0 (±25.4)	inch (mm)
	DMD_HS_WDATA_B_P DMD_HS_WDATA_B_N			
	DMD_HS_WDATA_C_P DMD_HS_WDATA_C_N			
	DMD_HS_WDATA_D_P DMD_HS_WDATA_D_N			
	DMD_HS_WDATA_E_P DMD_HS_WDATA_E_N			
	DMD_HS_WDATA_F_P DMD_HS_WDATA_F_N			
	DMD_HS_WDATA_G_P DMD_HS_WDATA_G_N			
	DMD_HS_WDATA_H_P DMD_HS_WDATA_H_N			
DMD	DMD_LS_WDATA DMD_LS_RDATA	DMD_LS_CLK	±0.2 (±5.08)	inch (mm)
DMD	DMD_DEN_ARSTZ	N/A	N/A	inch (mm)

(1) These values apply to PCB routing only and do not include any internal package routing mismatch associated with the DLPC3432, the DMD.
(2) DMD HS data lines are differential, thus these specifications are pair-to-pair.
(3) Training is applied to DMD HS data lines, so defined matching requirements are slightly relaxed.
(4) DMD LS signals are single-ended.
(5) Mismatch variance applies to high-speed data pairs. For all high-speed data pairs, the maximum mismatch between pairs must be 1 mm or less.

4.3.1.6 *Number of Layer Changes*

- Single-ended signals: Minimize the number of layer changes.
- Differential signals: Individual differential pairs can be routed on different layers, but the signals of a given pair must not change layers.

4.3.1.7 *Stubs*

- Avoid stubs.

4.3.1.8 *Terminations*

- No external termination resistors are required on DMD_HS differential signals.
- The DMD_LS_CLK and DMD_LS_WDATA signal paths must include a 43-Ω series termination resistor located as close as possible to the corresponding ASIC pins.
- The DMD_LS_RDATA signal path must include a 43-Ω series termination resistor located as close as possible to the corresponding DMD pin.
- DMD_DEN_ARSTZ does not require a series resistor.

4.3.1.9 *Routing Vias*

- Minimize the number of vias on DMD_HS, DMD_LS_CLK, and DMD_LS_WDATA signals to not exceed two.
- Any and all vias on these signals must be located as close to the ASIC as possible.

4.3.2 DLPA3000 Layout Guidelines

4.3.2.1 Layout Guidelines

For switching power supplies, the layout is an important step in the design process, especially when it concerns high-peak currents and high-switching frequencies. If the layout is not carefully done, the regulator could show stability issues and EMI problems. Therefore, it is recommended to use wide- and short-traces for high-current paths and for their return power ground paths. The input capacitor, output capacitor, and inductor must be placed as near as possible to the device. To minimize ground noise coupling between different buck converters, separate their grounds and connect them together at a central point under the part.

The high currents of the buck converters concentrate around pins V_{IN}, SWITCH, and P_{GND} (see 図 5). The voltage at the pins V_{IN}, P_{GND}, and FB are DC voltages while the pin SWITCH has a switching voltage between V_{IN} and P_{GND}. In case the FET between pins 52 and 53 is closed, the red line indicates the current flow while the blue line indicates the current flow when the FET between pins 53 and 54 is closed. These paths carry the highest currents and must be kept as short as possible.

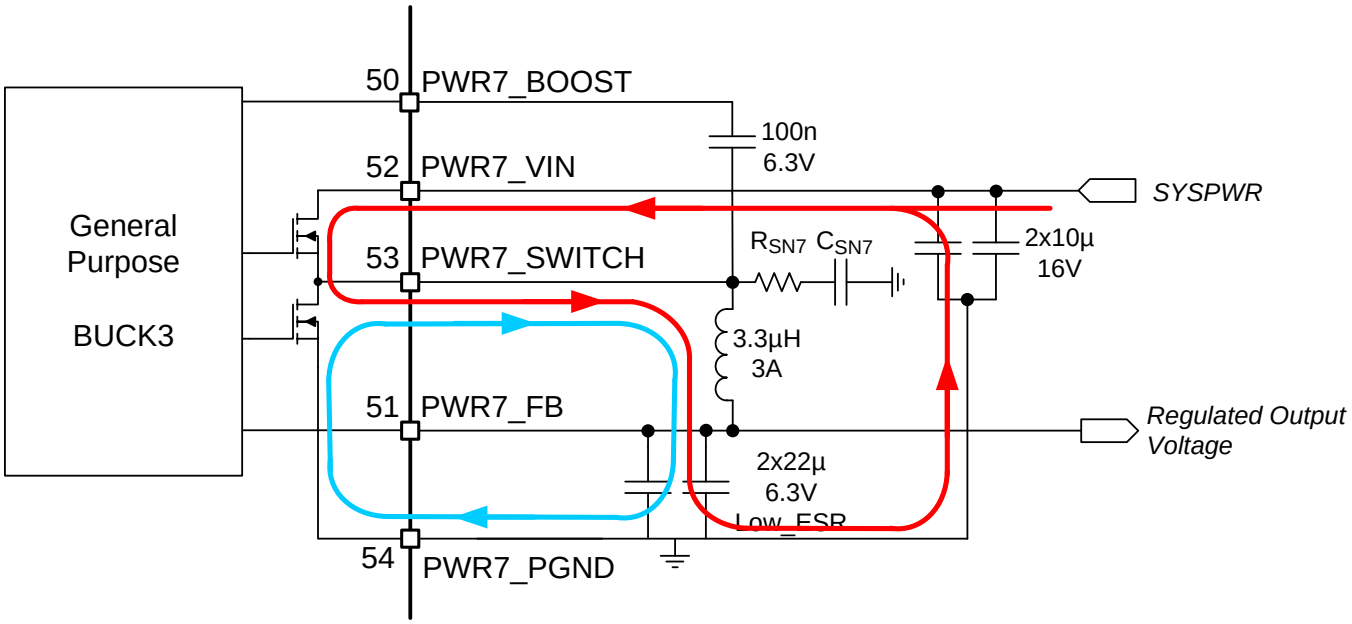


図 5. High AC Current Paths in a Buck Converter

The trace to the V_{IN} pin carries high AC currents. Therefore, the trace must be low-resistive to prevent voltage drop across the trace. Additionally, the decoupling capacitors must be placed as near to the V_{IN} pin as possible.

The SWITCH pin is connected alternatingly to the V_{IN} or GND. This means a square wave voltage is present on the SWITCH pin with an amplitude of V_{IN} and containing high frequencies. This condition can lead to EMI problems if not properly handled. To reduce EMI problems, a snubber network (RSN7 and CSN7) is placed at the SWITCH pin to prevent or suppress unwanted high-frequency ringing at the moment of switching.

The P_{GND} pin sinks high current and must be connected to a star ground point such that it does not interfere with other ground connections.

The FB pin is the sense connection for the regulated output voltage, which is a DC voltage; no current is flowing through this pin. The voltage on the FB pin is compared with the internal reference voltage to control the loop. The FB connection must be made at the load such that the I•R drop is not affecting the sensed voltage.

4.3.2.2 SPI Connections

The SPI consists of several digital lines and the SPI supply. If routing of the interface lines is not done properly, communication errors can occur. SPI lines must not pick up noise and keep possible interfering sources away from the interface.

Pickup of noise can be prevented by ensuring that the SPI ground line is routed together with the digital lines as much as possible to the respective pins. The SPI must be connected by a separate own ground connection to the DGND of the DLPA3000 (see 図 6). This prevents ground noise between SPI ground references of the DLPA3000 and DLPC due to the high current in the system.

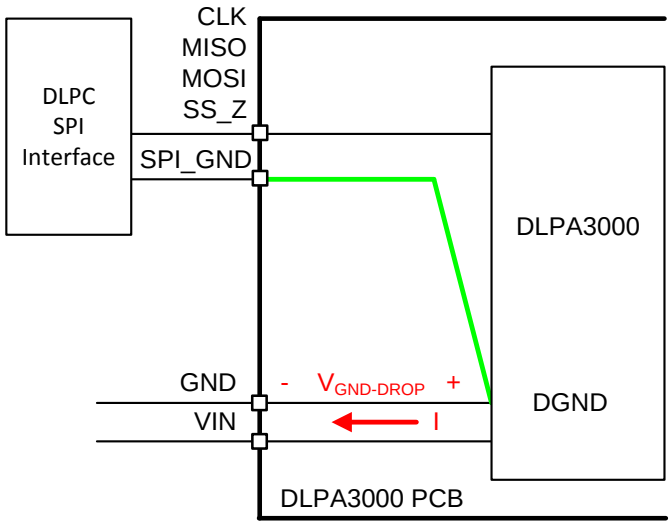


図 6. SPI Connections

Keep interfering sources away from the interface lines as much as possible. High-current lines such as neighboring PWR_7 must especially be routed carefully. If PWR 7 is routed too close to SPI_CLK, for example, it could lead to false clock pulses and thus communication errors.

4.3.2.3 R_{LIM} Routing

R_{LIM} is used to sense the LED current. To accurately measure the LED current, the RLIM_K_1,2 lines must be connected close to the top side of measurement resistor R_{LIM}, while RLIM_BOT_K_1,2 must be connected close to the bottom side of R_{LIM}.

The switched LED current is running through R_{LIM}. Therefore, a low-ohmic ground connection for R_{LIM} is strongly advised.

4.3.2.4 LED Connection

Switched large currents are running through the wiring from the DLPA3000 to the LEDs. Therefore, special attention needs to be paid here. Two perspectives apply to the LED-to-DLPA3000 wiring:

1. The resistance of the wiring, R_{series}
2. The inductance of the wiring, L_{series}

図 7 shows the location of the parasitic series impedances.

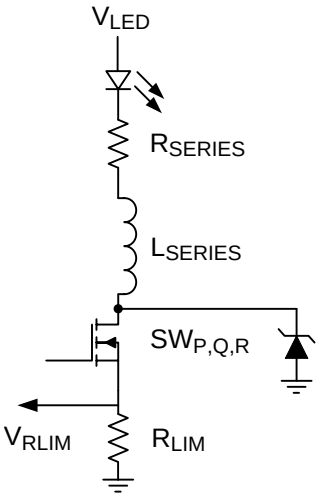


図 7. Parasitic Inductance (L_{series}) and Resistance (R_{series}) in Series With LED

Currents up to 6 A can run through the wires connecting the LEDs to the DLPA3000. Some noticeable dissipation can easily be caused. Every 10 mΩ of series resistances implies for a 6-A average LED current a parasitic power dissipation of 0.36 W. This dissipation can cause PCB heating, but more importantly, the overall system efficiency is deteriorated.

Additionally, the resistance of the wiring might impact the control dynamics of the LED current. The routing resistance is part of the LED current control loop. The LED current is controlled by V_{LED}. For a small change in V_{LED} (ΔV_{LED}), the resulting LED current variation (ΔI_{LED}) is given by the total differential resistance in that path:

$$\Delta I_{LED} = \frac{\Delta V_{LED}}{r_{LED} + R_{series} + R_{on\_SW\_P,Q,R} + R_{LIM}} \quad (3)$$

in which r_{LED} is the differential resistance of the LED and $R_{on\_SW\_P,Q,R}$ the on-resistance of the strobe decoder switch. In this expression, L_{series} is ignored since realistic values are usually sufficiently low to cause any noticeable impact on the dynamics.

All the comprising differential resistances are in the range of 25 mΩ to several 100s mΩ. Without paying special attention, a series resistance of 100 mΩ can easily be obtained. It is advised to keep this series resistance sufficiently low (for example, < 50 mΩ).

The series inductance plays an important role when considering the switched nature of the LED current. While cycling through R, G, and B LEDs, the current through these branches is turned on and turned off in short-time duration. Specifically, turnoff is fast. A current of 6 A goes to 0 A in a matter of 50 ns, which implies a voltage spike of about 1 V for every 10 nH of parasitic inductance. It is recommended to minimize the series inductance of the LED wiring by:

- Short wires
- Thick wires or multiple parallel wires
- Small enclosed area of the forward and return current path

If the inductance cannot be made sufficiently low, a Zener diode needs to be used to clamp the drain voltage of the RGB switch, such it does not surpass the absolute maximum rating. The clamping voltage needs to be chosen between the maximum expected V_{LED} and the absolute maximum rating. Take care of sufficient margin of the clamping voltage relative to the mentioned minimum and maximum voltage.

4.3.3 DMD Flex Cable Interface Layout Guidelines

The 5496-203BKDLP230GPFQP5496-213BK DMD is connected to a PCB or a flex circuit using an interposer. For additional layout guidelines regarding length matching, impedance, etc. see the DLPC3432/DLPC3472 controller datasheet.

Some layout guidelines for routing to the 5496-203BKDLP230GPFQP5496-213BK DMD are:

- Match lengths for the LS_WDATA and LS_CLK signals.
- Minimize vias, layer changes, and turns for the HS bus signals. Refer to 図 8.
- Minimum of two 100-nF (25 V) capacitors - one close to V_{BIAS} pin. Capacitors C4 and C8 in 図 8.
- Minimum of two 100-nF (25 V) capacitors - one close to each V_{RST} pin. Capacitors C3 and C7 in 図 8.
- Minimum of two 220-nF (25 V) capacitors - one close to each V_{OFS} pin. Capacitors C5 and C6 in 図 8.
- Minimum of four 100-nF (6.3 V) capacitors - two close to each side of the DMD. Capacitors C1, C2, C9 and C10 in 図 8.

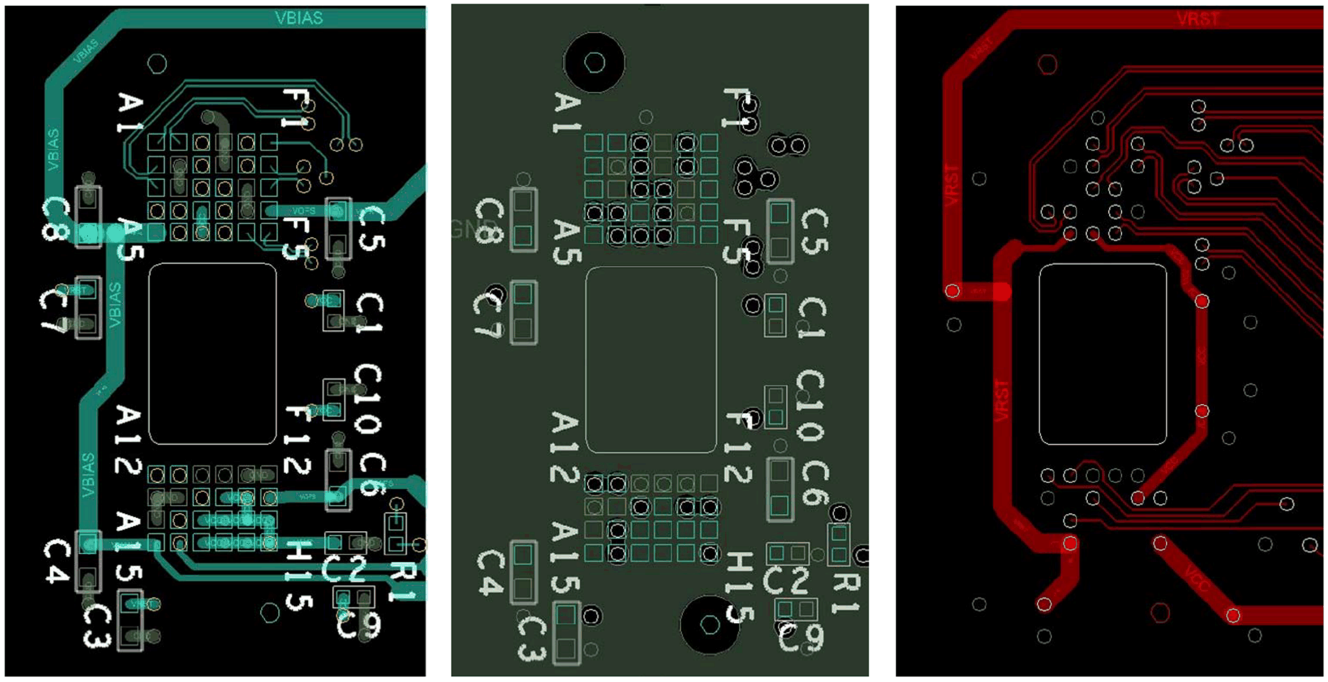


図 8. Power Supply Connections

4.3.4 Layout Prints

To download the layer plots, see the design files at TIDA-080002.

4.4 Cadence Project

To download the Cadence project files, see the design files at TIDA-080002.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-080002.

5 Software Files

To download the software files, see the design files at TIDA-080002.

6 Related Documentation

1. Texas Instruments, *DLPC3432 Display Controller Data Sheet*
2. Texas Instruments, *DLP230GP (p23 qHD DMD) Data Sheet*
3. Texas Instruments, *DLPA3000 PMIC and High-Current LED Driver IC Data Sheet*

6.1 商標

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