参考資料

TI Designs: TIDA-050001
HDMI® 2.0 ESD保護デバイスのリファレンス・デザイン

概要

このリファレンス・デザインでは、HDMI®2.0ドライバおよびリタイマのTMDSラインを静電放電(ESD)から保護する2つの方法を示します。HDMI規格は、セットトップ・ボックスからノートブックPC、テレビまで、多くのアプリケーションに採用されています。このポートはたいてい外付けになるため、ESD事象の影響を受けやすくなっています。高速のHDMI 2.0信号の場合、ドライバで適切なESD保護機能をICに内蔵できないため、ディスクリートのESD保護デバイスが必要とされます。また、HDMIドライバは一般に極めて高感度であることから、ESD保護デバイスには極めて低いクランプ電圧が要求されます。このリファレンス・デザインは、2つの設定で初期HDMI 2.0コンプライアンス・データを処理し、各基板でESDテストを行い、テスト後に最終的なHDMI 2.0コンプライアンス・データを示します。HDMIコネクタの他の5本のピンの保護については、TI TechNotes『HDMIアプリケーションのESD保護』を参照してください。

特長

- HDMI 2.0準拠を支援
- IEC 61000-4-2 Level 4 (±8kV接触)
- 高感度HDMIドライバの保護に必要とされる超低クランプ電圧を実現
- DP159とTMDS181の両方に対応

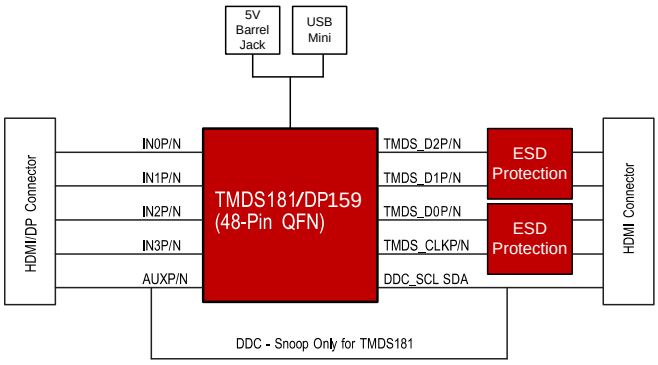
アプリケーション

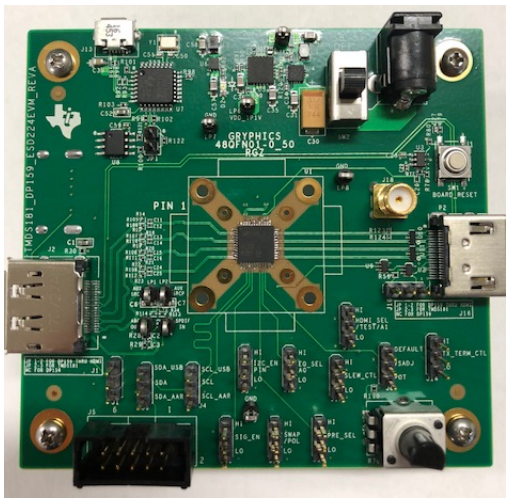
- セットトップ・ボックス
- ノートブックPC
- テレビ

リソース

TIDA-050001	デザイン・フォルダ
ESD224	プロダクト・フォルダ
TMDS181RGZEVM	プロダクト・フォルダ
SN65DP159	プロダクト・フォルダ

TI E2E™ Community　E2E™エキスパートに質問





1 System Description

This reference 'standalone' design will showcase two ways to protect the HDMI 2.0 driver and redriver TMDS lines. First using the ultra low clamping ESD224 and second using the ESD224 with a common mode choke for applications with electromagnetic interference (EMI) concerns. This design specifically targets the TMDS clock and data lines for ESD protection. This guide will go through the initial HDMI 2.0 compliance testing showing that the protection stage allows HDMI compliance. Then showcase an ESD strike on the TMDS lines with the clamping voltage during the event. Then show the post test HDMI compliance data to show the protection stage has worked as intended.

The HDMI 2.0 specification has a TMDS differential clock signal and is rated for 18 Gbps between three differential data pairs, data line 0 (D0±), data line 1 (D1±), data line 2 (D2±), with each pair at 6 Gbps. These HDMI signals are usually routed to a connector which then runs through a cable to another driver on the receiving end. The connector cable interface is exposed to the outside world and therefore susceptible to the ESD event. With the data rates so high in this application, care must be taken so that the protection stage will not interrupt normal operation of the data but will also protect during the ESD event. Furthermore, the protection stage is required to clamp the voltage to an acceptable level for the HDMI driver.

For each of these schemes the ESD224 will be used because of its ultra low clamping performance and low capacitance value. The difference in the two protection schemes covered in this design are based on whether EMI is an issue. If EMI is not a concern the first strategy can be used of only the ESD224. However, for applications in noisy environment or ones that require extremely low noise, designers will typically use a common mode choke in the protection stage that will eliminate the common mode noise and let the differential signal pass uninhibited. However, the trade off is that the CMC will take most of the bandwidth of the HDMI 2.0 signal. Therefore care must be taken in design to not have much more parasitics in the system so that the ESD224 with the CMC can have enough bandwidth while providing robust protection.

2 System Overview

2.1 Block Diagram

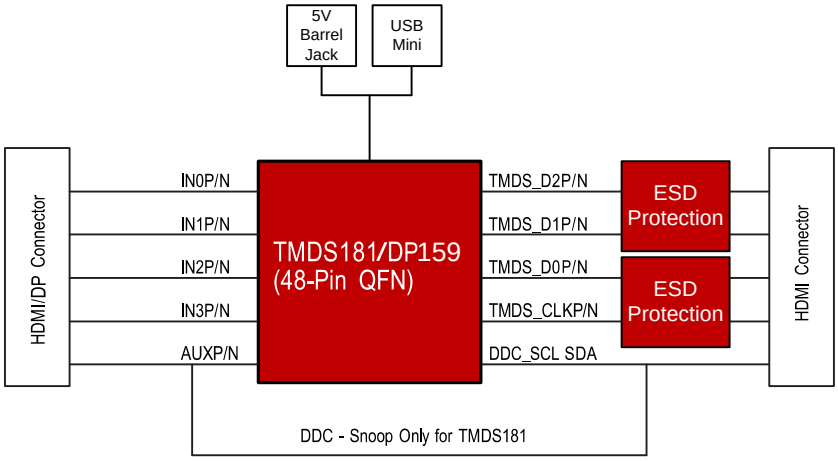


図 1. TIDA-05001 Block Diagram

2.2 Design Considerations

Protecting HDMI drivers or systems on chip (SoC) from ESD, requires that the protection stage be as close as possible to the source of the ESD, in this case the HDMI output connector. This ensures the least amount of parasitics between the pulse and the protection path. When routing the TMDS lines care must be taken that each pair is differentially routed 100 Ω differential impedance. The ESD224 is non-flow through routing so the traces have an input and an output in the device. This is discussed more in 2.4.3

2.3 Highlighted Products

2.3.1 ESD224

The ESD224 is a bidirectional TVS ESD protection diode array for high speed applications such as USB 3.0 and HDMI 2.0. The ESD224 is rated to dissipate ESD strikes at the maximum level specified in the IEC 61000-4-2 international standard (Level 4). The ESD224 employs on-chip differentially matched series elements to enhance down-stream ESD clamping performance while maintaining the signal compliance for high speed interfaces. The ultra-low clamping performance and high differential bandwidth provided by the ESD224 on-chip ESD protection network enables the device to be HDMI 2.0 compliant while providing robust protection to downstream HDMI devices. For more information see ESD224 HDMI 2.0 Compliance and Protection.

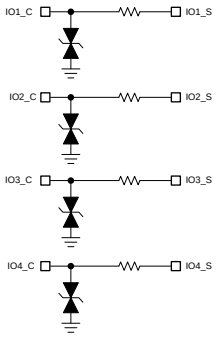


図 2. ESD224 Functional Block Diagram

2.3.2 TMDS181

The TMDS181 is a digital video interface (DVI) or high-definition multimedia interface (HDMI) retimer. The TMDS181 support four TMDS channels, audio return channel (SPDIF_IN/ARC_OUT), and digital display control (DDC) interfaces. The TMDS181 supports signaling rates up to 6 Gbps to allow for the highest resolutions of 4k2k60p 24 bits per pixel and up to WUXGA 16-bit color depth or 1080 p with higher refresh rates. The TMDS181 can be configured to support the HDMI2.0a standard. The TMDS181 automatically configures itself as a redriver at low data rate (<1.0 Gbps) or as a retimer above this data rate. Redriver mode supports HDMI1.4b with data rates up to 3.4 Gbps.

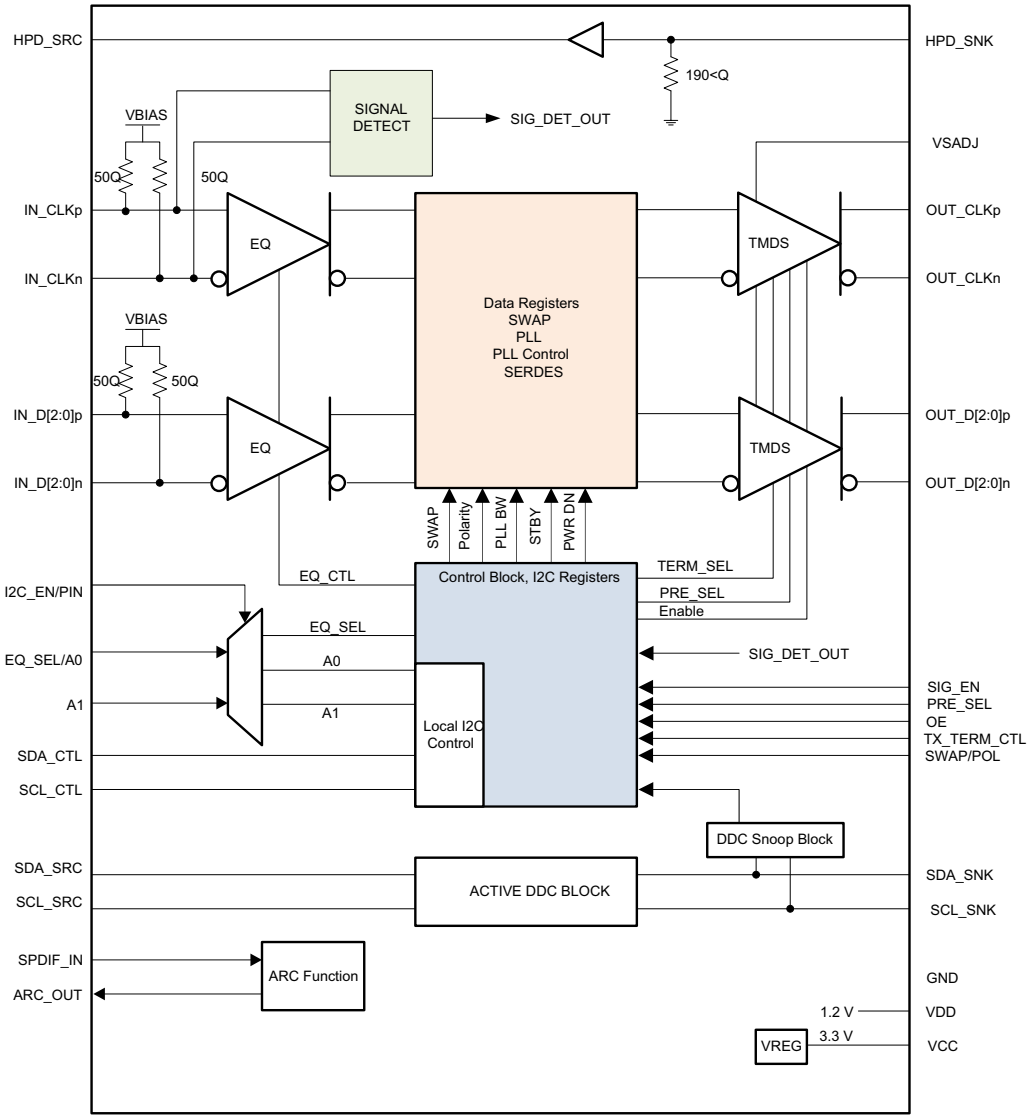


図 3. TMDS181 Functional Block Diagram

2.3.3 SN65DP159

The SN65DP159 device is a dual mode DisplayPort to transition-minimized differential signal (TMDS) retimer supporting digital video interface (DVI) 1.0 and high-definition multimedia interface (HDMI) 1.4 b and 2.0 output signals. The SN65Dp159 device supports the dual mode standard version 1.1 type 1 and type 2 through the DDC link or AUX channel. The SN65DP159 device supports data rate up to 6-Gbps per data lane to support Ultra HD (4k × 2k / 60-Hz) 8-bits per color high-resolution video and HDTV with 16-bit color depth at 1080p (1920 × 1080 / 60-Hz). The SN65DP159 device can automatically configure itself as a re-driver at data rates <1 Gbps, or as a retimer at more than this data rate. This feature can be turned off through I^2C programming.

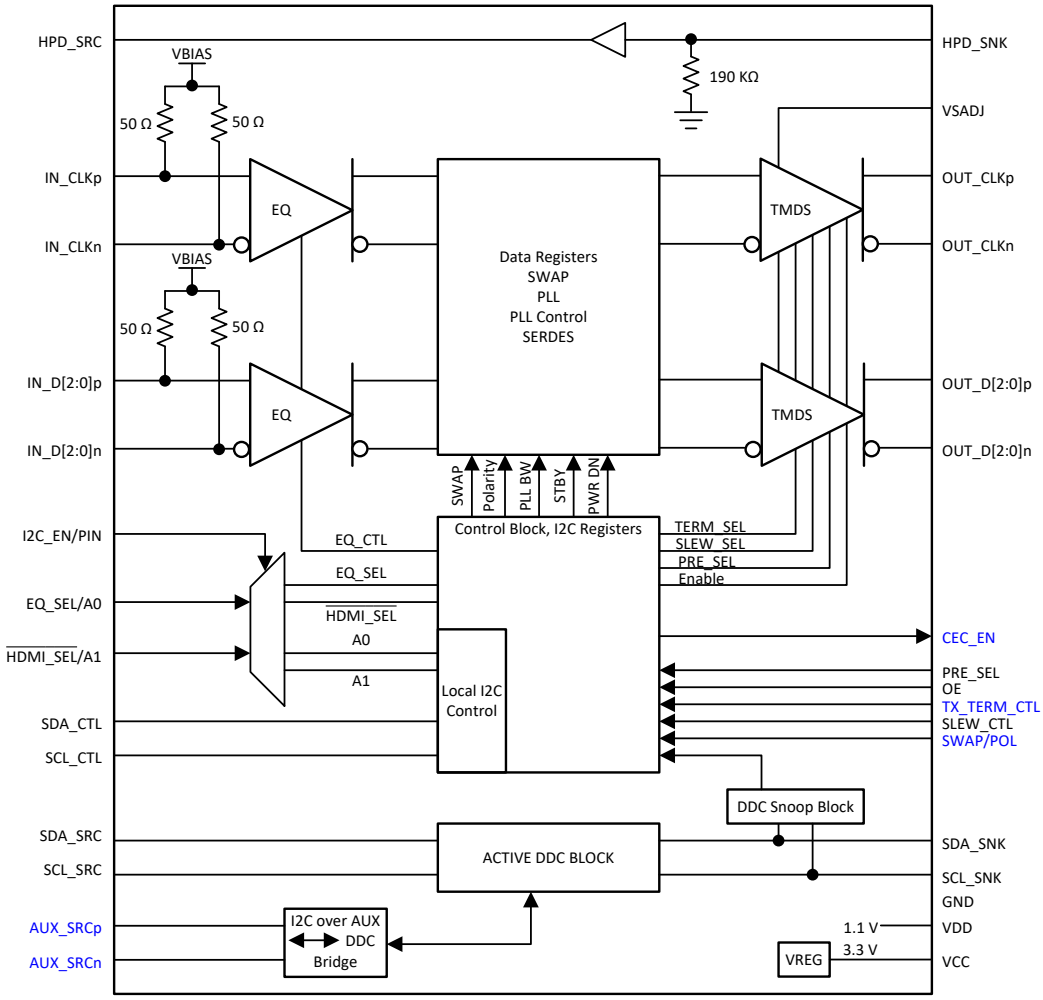


図 4. SN65DP159 Functional Block Diagram

2.4 System Design Theory

2.4.1 TMDS181RGZEVM

This board is built off the existing TMDS181RGZEVM with minor modifications allowing for both the TMDS181 and the DP159 to be tested. The major changes are the addition of the display port connector for the DP159 testing and the addition of a protection stage at the output of the main device. R123 was added to D2P to be able to connect a cable to measure the ESD waveform seen on the system side of the ESD strike. For symmetry, the R124 footprint was added to D2N to make sure there was not additional skew added to the signal. During the HDMI testing and normal ESD testing R123 was depopulated and therefore not inhibiting the waveforms. For a full schematic of the TMDS181RGZEVM see the TMDS181RGZEVM User's Guide.

2.4.2 Choosing the Right Protection

ESD pulses are very high energy and very short durations. To protect from damage, often times a discrete protection stage is used at the input of the where the ESD discharge is likely to occur. When choosing the ESD protection there are several aspects that can make the process more straight forward. The different parameters and concerns are discussed in TI's training series ESD Essentials. This six part series walks through the process of understanding the ESD pulse to selecting correct protection. It is also worth noting that doing the transmission line pulse, TLP, testing of the DP159 and the TMDS181 gives a clear answer to what clamping voltage will most likely protect that IC.

The TLP results will give an indication of what the clamping voltage must be, the IEC61000-4-2 should be at 30 ns. The rule of thumb is that 2 A TLP is equivalent to 1 kV ESD. Shown below are the TLP results from each device. It can be seen that the TMDS181 has a maximum value of approximately 9 V at 4 A on the positive side and approximately –6 V at 5 A on the negative side before device failure. Likewise the DP159's maximum clamping value is approximately 8.5 V at 4.5 A on the positive side and approximately –6 V at 5 A on the negative side before device failure. The clamping voltage of the ESD224 found in the datasheet is at 8 kV is 8 V and –5 V at –8 kV, therefore the clamping voltage our protection stage is enough to protect these HDMI devices.

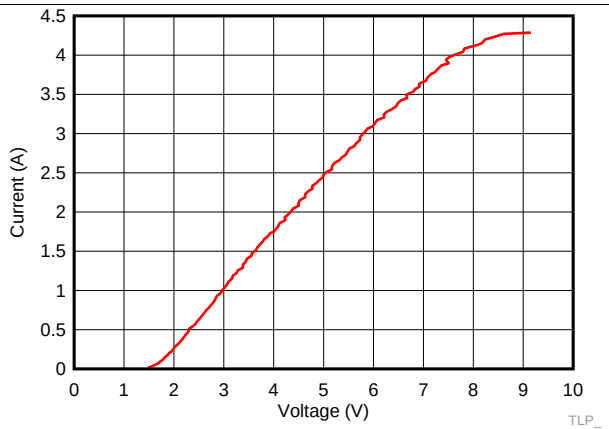


図 5. TMDS181 TLP Clamping Waveform

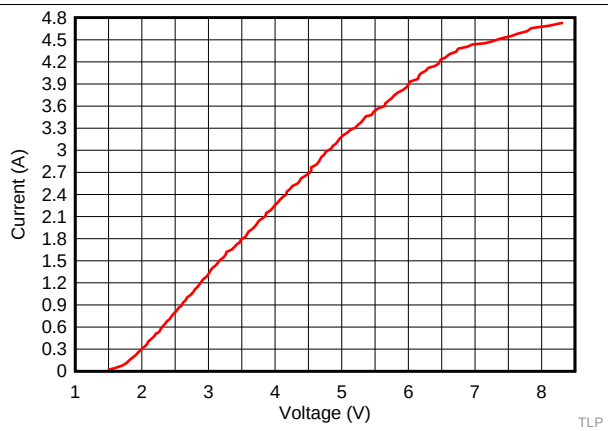


図 6. DP159 TLP Clamping Waveform

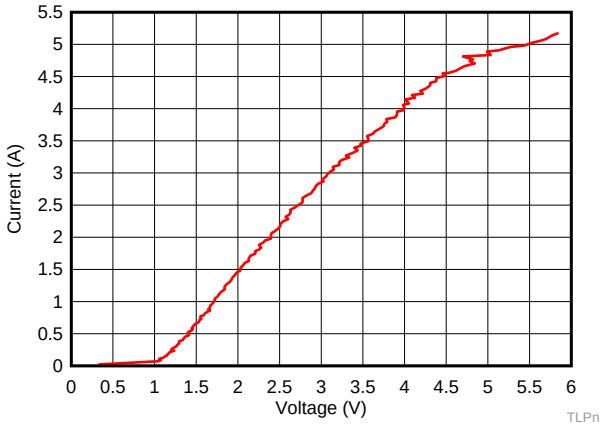


図 7. TMDS181 Negative TLP Clamping Waveform

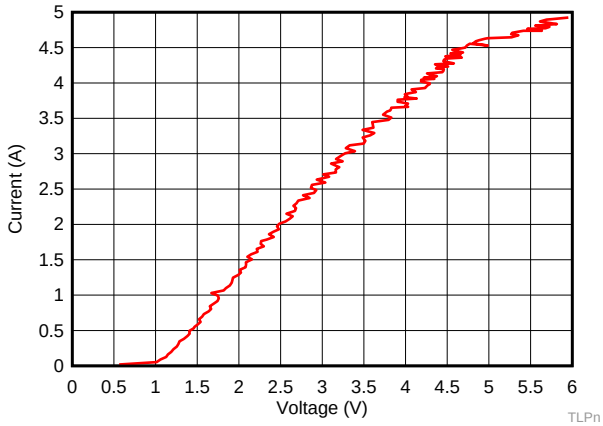


図 8. DP159 Negative TLP Clamping Waveform

2.4.3 Protection Stages

Since the TLP of the TMDS181 and DP159 show how low the clamping voltage must be and how little current the device can take before breaking, the protection stage must be robust. The dynamic resistance (R_{DYN}) of many ESD devices is not sufficient to keep the clamping voltage so low. This means the addition of a series element in the circuit is necessary to drop the voltage low enough to provide adequate protection shown in 図 9.

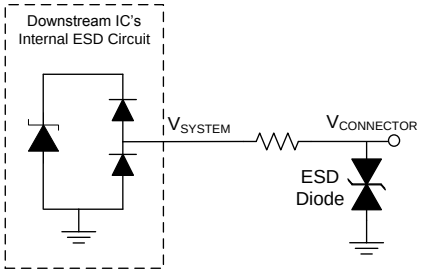


図 9. Low Clamping ESD Protection

$V_{CONNECTOR}$ is the voltage seen on the connector side where the ESD strike is originating. V_{SYSTEM} is the voltage seen by the downstream IC. Picturing the protection stage like this it is easy to see the voltage drop since the series element will by nature have a resistance to it. The key concern beyond that is to make sure that the resistance of the series component does not interfere with the HDMI 2.0 signal. This series component must be differentially matched as to not cause skew in the signal as well as be a low enough value to meet the differential voltage swing requirement of HDMI 2.0.

This design covers two distinct types of protection for the HDMI 2.0 TMDS signal lines. The first is the ESD224 which is a 4-channel ultra-low clamping ESD device shown in 図 10. This fits in applications that have lower noise concerns and can save considerably by not having to include a CMC but still provides robust protection because of the series element introduced in the design. This clamping voltage on the system side is specified in the datasheet to indicate that it can protect the ESD sensitive HDMI drivers.

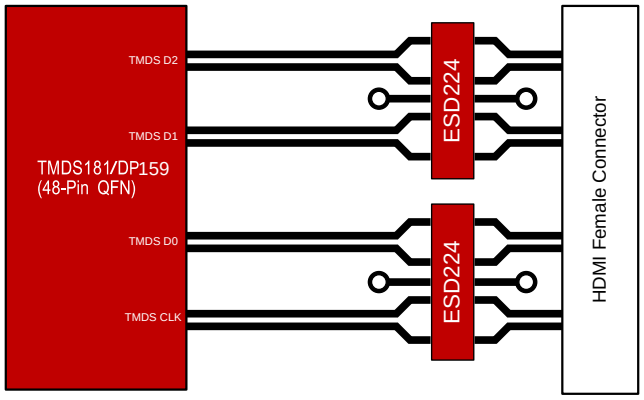


図 10. ESD224 Protection Schematic

The other protection stage covered in this design use a discrete ESD diode, ESD224, and a CMC for EMI reduction. The CMC is useful to reduce the common mode noise on each differential pair in noisy environments. The CMC will also make the traces discontinuous again, adding more series resistance to further reduce the clamping voltage on the system side. Using the CMC in conjuncture with the ESD224 means that the signal integrity will be affected more as they are both taking up significant bandwidth. However, as can be seen in the 3.2, the combination of ESD224 plus a high speed CMC can meet the HDMI 2.0 requirement. The protection stage with ESD diode and CMC can be seen in 図 11.

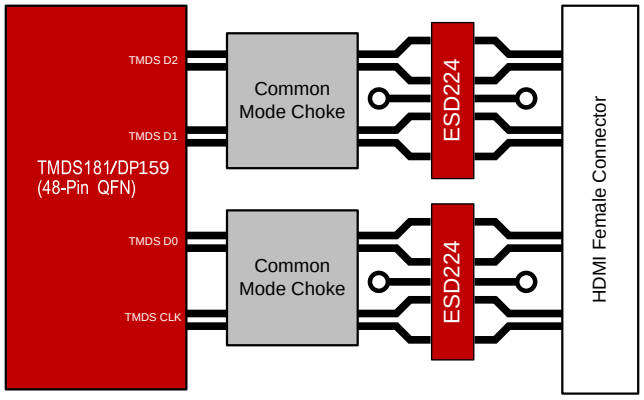


図 11. ESD224 and CMC Protection Schematic

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

The board was made to be interchangeable from the TMD181 to the DP159. It was also made to take in DisplayPort++ (DP++) input as well as HDMI. However in order to do this there are several components need to be changed to enable operation of the other device.

3.1.1.1 Input Signal

To use either the HDMI or DP++ input connector there are zero Ohm resistors that have to be either populated or depopulated. For the HDMI connector, R15, R15, R18, R19, R20, R21, R22 and R23 should be populated while R105, R106, R107, R108, R109, R110, R111, R112 should be depopulated. For the DP+ connector it is the opposite. This can be seen in 図 12.

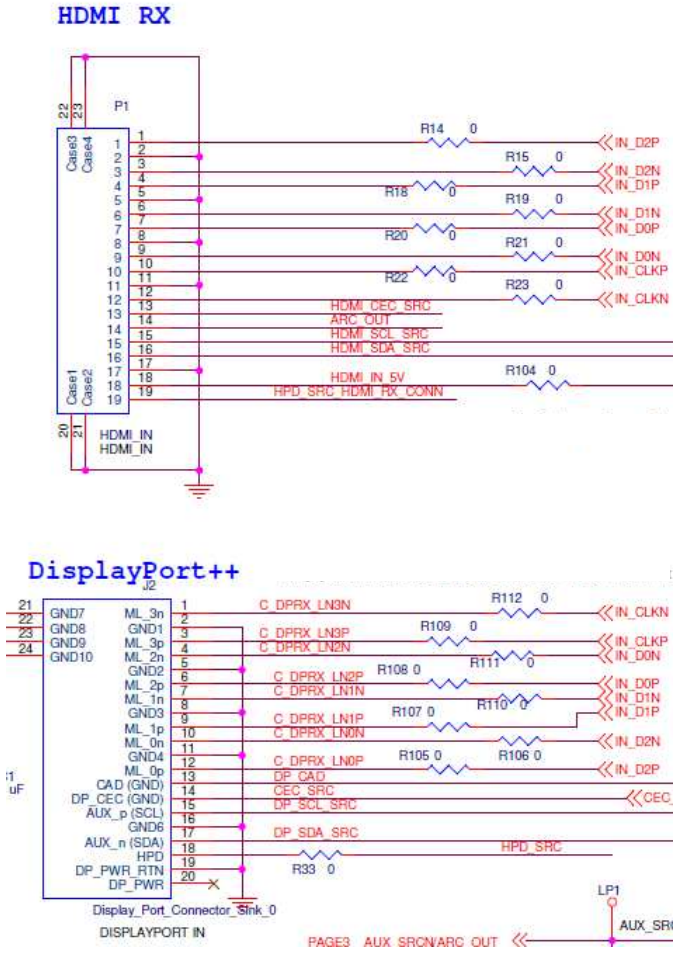


図 12. HDMI or DP++ Input Connector

3.1.1.2 SN65DP159

The SN65DP159 implementation is shown in 図 13. AC coupling capacitors are used on the TMDS input lines. This is taken from the SN65DP159 datasheet so it does not show the ESD protection on the output TMDS lines.

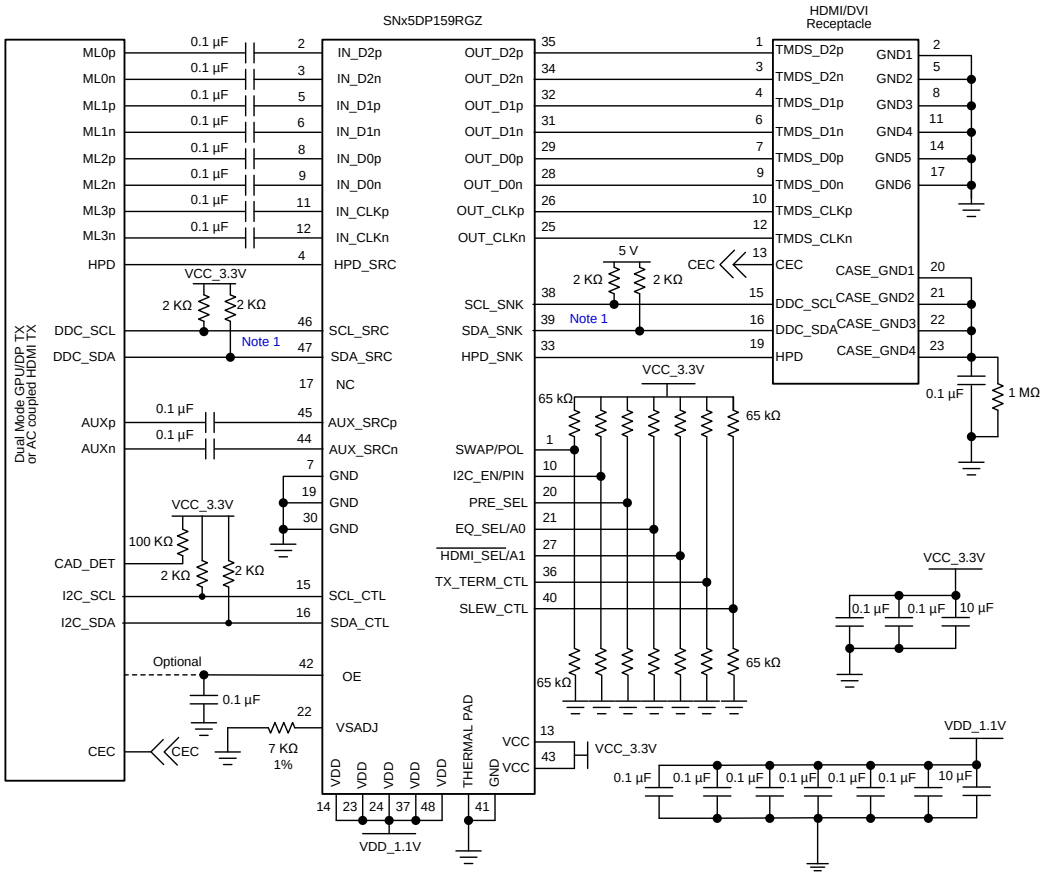


図 13. SN65DP159 Implementation

3.1.1.3 TMDS181

In order to run TMDS181 in 6-Gbps mode, DDC snoop must be implemented as shown in 図 14. This is taken from the TMDS181 datasheet so it does not show the ESD protection on the output TMDS lines.

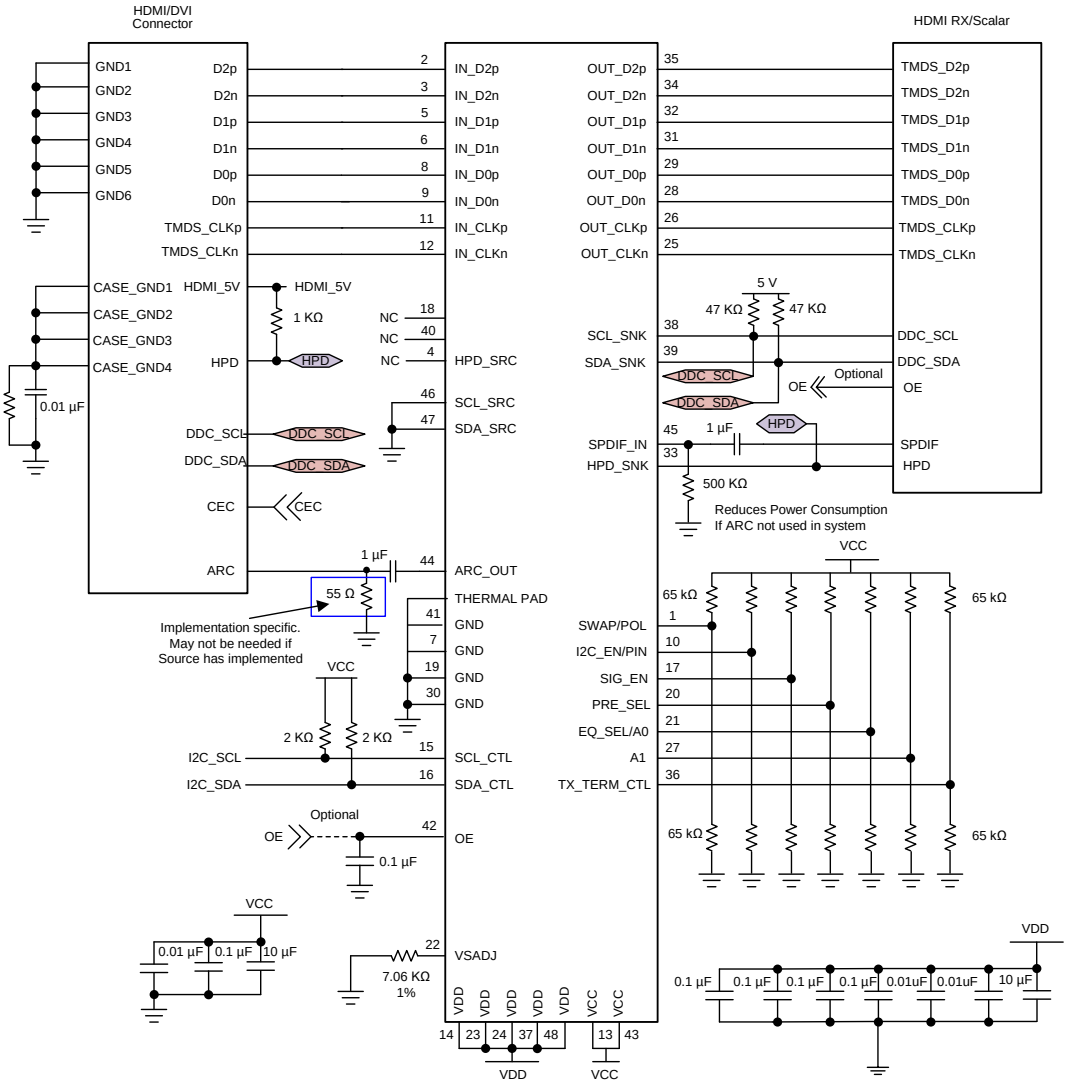


図 14. TMDS181 in Sink Side Application

It is important to notice that the TMDS lines are connected directly from the input connector to the TMDS181 device. This means C11, C12, C13, C14, C15, C16, C24, and C25 all need to be changed to 0 Ω resistors because the TMDS181 can take bias voltages on the input side. Also the SCL and SDA source pins are shorted to ground while the SCL and SDA sink side is connected to both the input connector SCL and SDA pins as well as the output connector SCL and SDA pins.

Also seen on page 2 of the schematic C2 and C3 should be not populated for TMDS181.

3.1.1.4 Switches and Jumper Orientation

The board can be powered two different ways, either from the USB Micro connector, J13, or barrel jack with 5 V, J9. SW2 allows the option to choose between. Moving the switch to position 1 allows the board to be powered off of a 5-V barrel jack connector, J9. Moving the switch to position 3 allows the board to be powered from the USB mini connector, J13. Position 2 on the switch means that the board is not powered.

表 1 explains the jumpers orientation to use either DP159 or TMDS181.

表 1. Jumpers

Jumper	Description	Jumper Settings	
J1 and J16	HDMI driver selection	For **DP159** jump pins 1-2 or NC	For **TMDS181** jump pins 2-3
J3	I^2C Enable	To **enable** jump pins 1-2	To **disable** jump pins 1-2
J4 and J6	Select between writing I^2C with USB-micro or Aardvark	For **USB** jump pins 1-2	For **Aardvark** jump pins 2-3
J8	Adjust TMDS-compliant voltage swing control nominal resistor to GND, or V_{sadj} pin	For use of **potentiometer** jump pins 1-2	For **default** 6.98kΩ jump 2-3 or NC

3.1.2 Software

Both devices must be set up in 6-Gbps mode in a sink application. Refer to TMDS181 Datasheet and SNx5DP159 Datasheet for more information about the register settings needed to set each device up to send HDMI 2.0 signals.

3.2 Testing and Results

The testing of the design was to check the initial HDMI 2.0 compliance using Keysight's HDMI Compliance Software, then strike the board according to the IEC 61000-4-2 standard at ±12 kV to show the full range of the ESD224 protection, then retest the board for HDMI 2.0 compliance to observe there are no shifts.

3.2.1 Test Setup - HDMI 2.0 Compliance Software

Using Keysight's HDMI Compliance Software on an oscilloscope and a simulator for the TMDS data and clock lines, HDMI 2.0 compliance could be established. This setup can be seen in 図 15. This design's main concern is with the ESD protection provided by the two stages, to see a more in-depth look at the device compliance and protection see the ESD224 HDMI ® 2.0 Compliance and Protection application report.

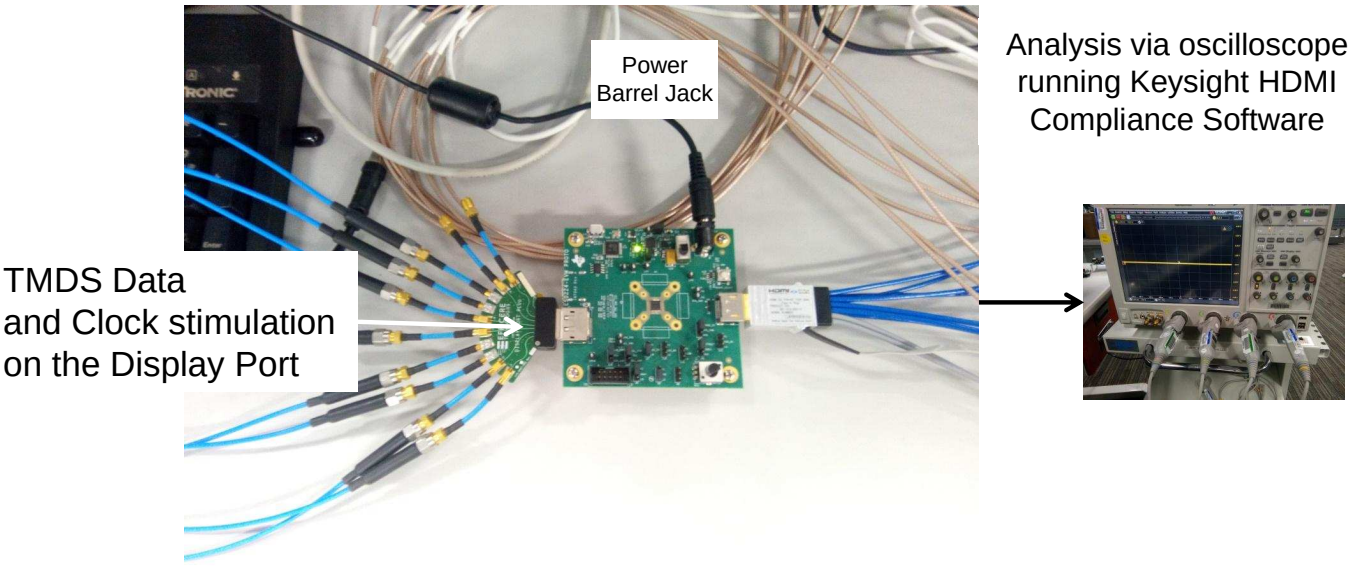


図 15. HDMI Test Setup for DP159

The specific HDMI 2.0 compliance tests run were the rise and fall times for each data lane including clock, the maximum and minimum for each data lane and the inter-pair skew for between each data lane. Once these tests were run, the boards would then go to be struck with ESD and then return to rerun the same HDMI 2.0 testing to see any shifts in performance.

3.2.2 Test Setup - ESD Striking

The board was placed in the setup as defined by the IEC 61000-4-2 standard. It was then powered by a USB cable and an adapter was attached to the output HDMI connector to provide a striking point as seen in 図 16. All of the TMDS pins have the same protection stage attached to them so therefore the results of the pin being struck are the same for each of the protected pins. The pin being stuck in 図 16 is D2P. This pin was chosen specifically because it is an outer most pin so an SMA connector could be connected to the line to see the clamping voltage that the system side sees. It is important to note that the waveform does look different than the IEC61000-4-2 standard waveform because of the reflections caused by the stub of the SMA connector. However for the full IEC 61000-4-2 ±8 kV and ±12 kV contact test, this stub was removed by depopulating R123.

図 16. ESD Test Setup

For more information about the IEC 61000-4-2 standard see the application report IEC 61000-4-x Tests for TI's Protection Devices. It is important to note that while the protection stage between the two cases is different, the same method with the resistor to SMA connector is used.

3.2.3 Test Results

3.2.3.1 TMDS181 with ESD224

The results show the pretest differential Keysight HDMI 2.0 compliance test passes with margin as seen in 表 2.

The eye diagram for the D2 TMDS line is shown in 図 17.

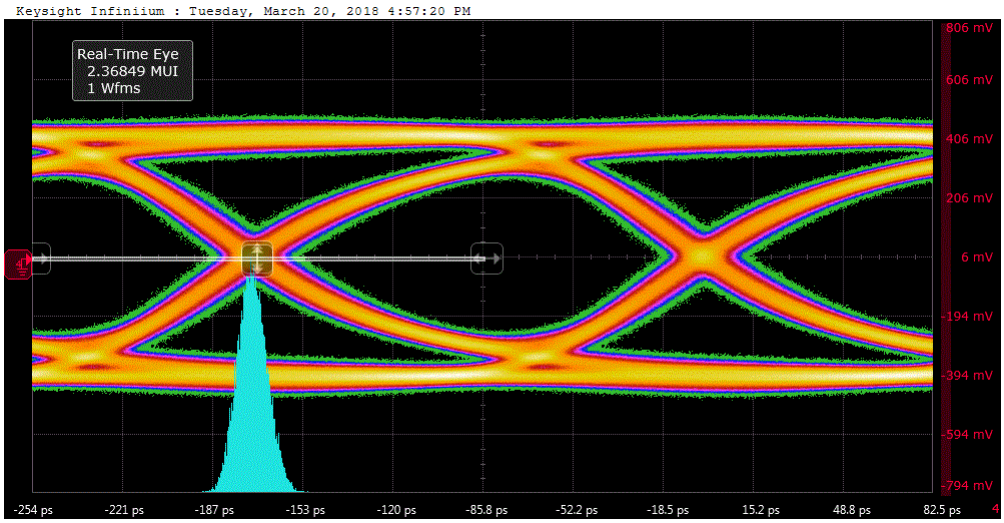


図 17. D2 TMDS181 with ESD224 Eye Diagram Pretest

The board was taken and struck with the IEC 61000-4-2 ESD waveform using the method described in 3.2.2. The clamping waveform for +8 kV and –8 kV can be seen in 図 18 and 図 19. The leakage remained the same as the pretest showing that the driver has not been damaged.

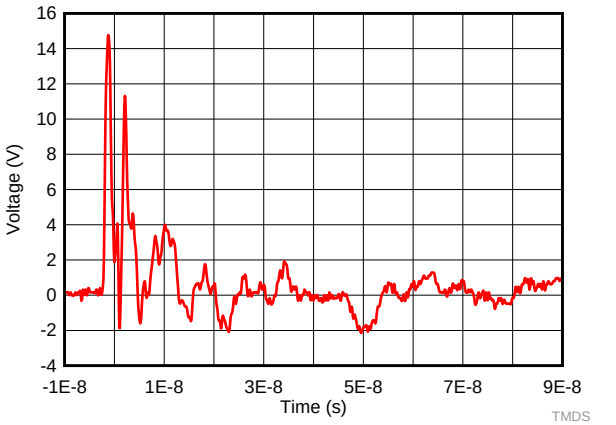


図 18. +8 kV Clamping Waveform TMDS181 with ESD224

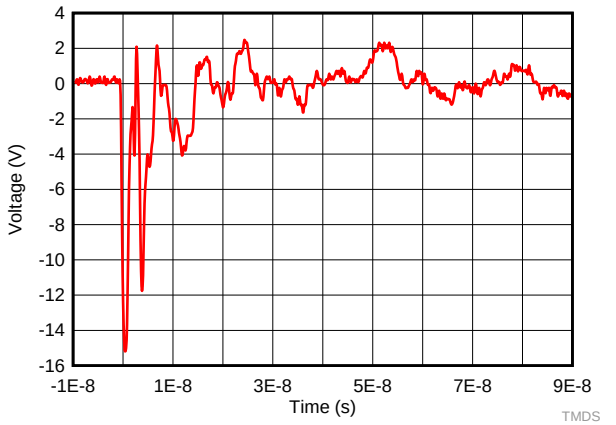


図 19. –8 kV Clamping Waveform TMDS181 with ESD224

The clamping voltage at 30 ns as can be seen in the waveform is much lower than the required voltage shown in 図 5. The board was then struck 10 times per the IEC61000-4-2 standard at one second intervals with ±12 kV ESD to show the full protection of the ESD224. Afterwards it was ran back through the HDMI compliance shown in 表 3.

The post test eye diagram for D2 TMDS line is shown in 図 20.

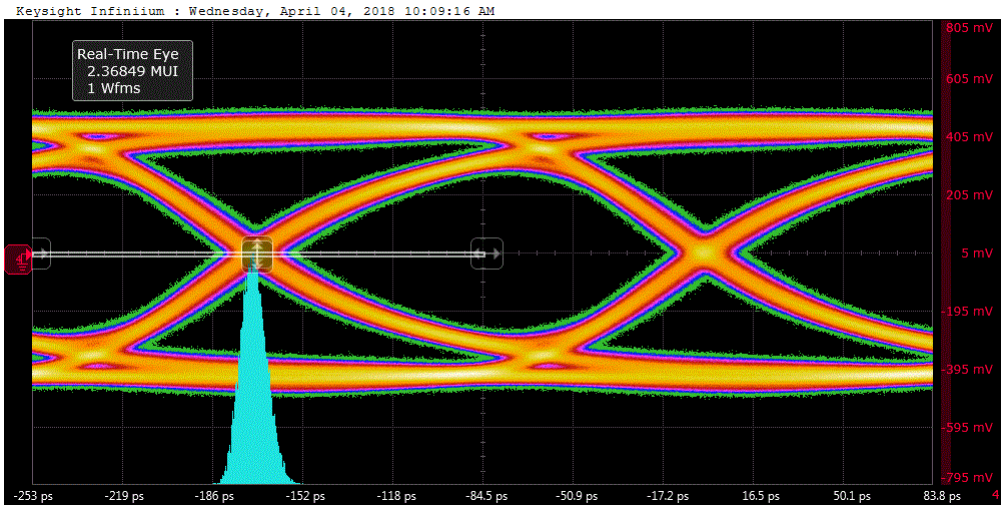


図 20. ±12 kV TMDS181 with ESD224 Post-test Eye Diagram

As shown in 図 20 there is no change in the eye diagram from the pretest. Refer to the 5 to compare pre and post tests results.

3.2.3.2 DP159 with ESD224 and CMC

Next testing the ESD224 plus CMC with the DP159 and with the same HDMI2.0 compliance pretests yields the results below.

The pretest eye diagram for D2 TMDS line is shown in 図 21.

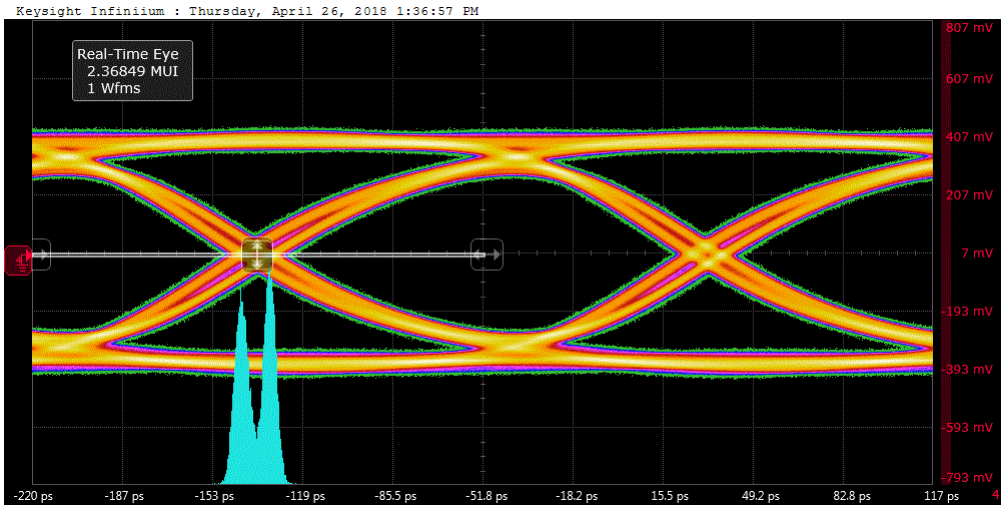
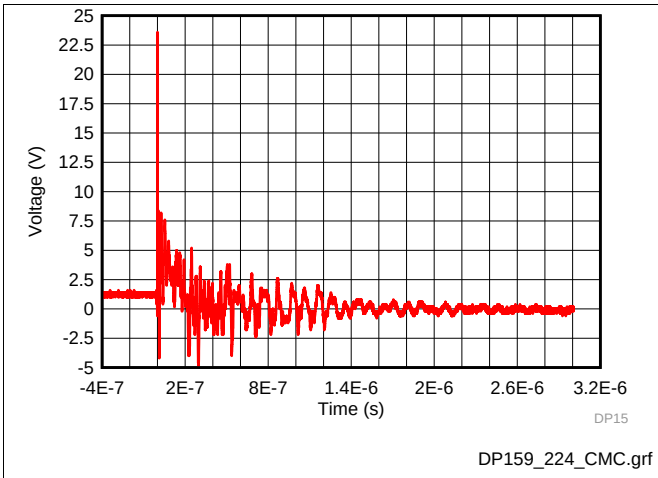


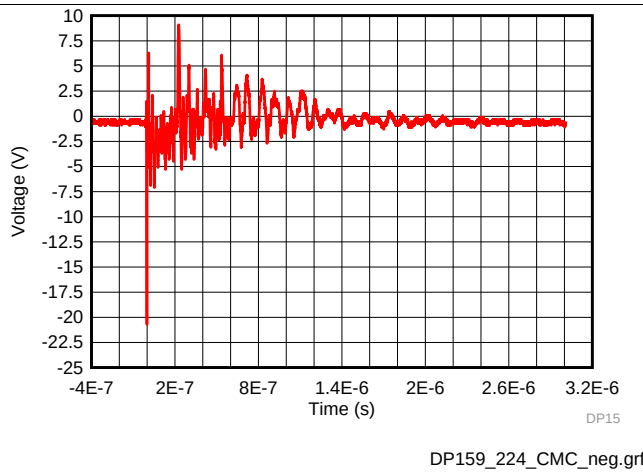
図 21. D2 DP159 with ESD224 and CMC Eye Diagram Pretest

The board was taken and struck with the IEC61000-4-2 ESD waveform using the method described in 3.2.2. The clamping waveform for +8 kV and –8 kV can be seen in 図 22 and 図 23. The leakage remained the same as the pretest showing that the driver has not been damaged



DP159_224_CMC.grf

図 22. +8 kV Clamping Waveform DP159 with ESD224 and CMC



DP159_224_CMC_neg.grf

図 23. –8 kV Clamping Waveform DP159 with ESD224 and CMC

It is important to note that the reason the waveform seems more noisy than just with the ESD224 is because the CMC is acting like an inductor in the circuit. However, the clamping voltage at 30 ns shown in the waveform is still lower than the required voltage shown in 図 5. The board was then struck 10 times per the IEC61000-4-2 standard at one second intervals with ±12 kV ESD to show the full protection of the ESD224. Afterwards it was ran back through the HDMI compliance shown in 表 5.

The post test eye diagram for D2 TMDS line is shown in 図 24 .

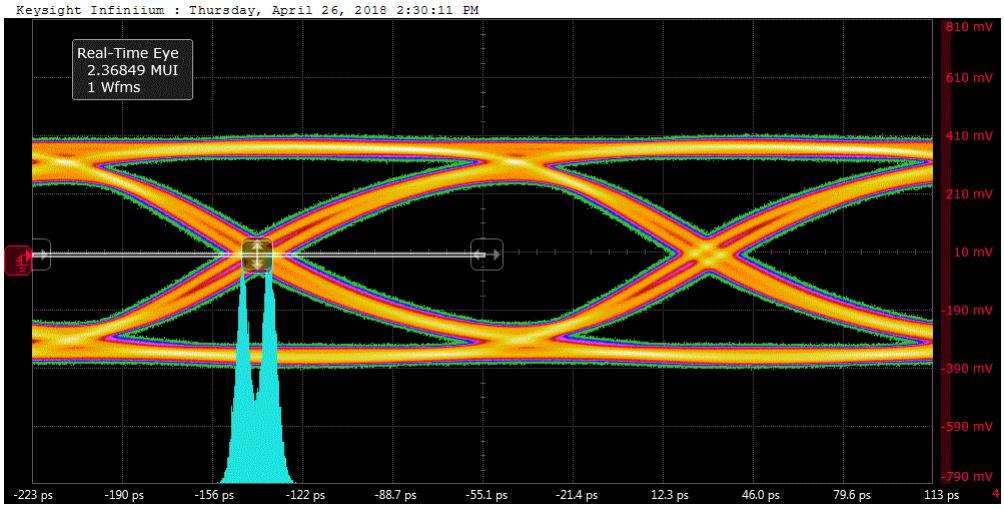


図 24. ±12 kV DP158 with ESD224 and CMC Post-test Eye Diagram

As can be seen there is no change in the eye diagram from the pretest. Refer to the 5 to compare pre and post tests results.

In conclusion, the ESD224 is capable of protecting sensitive HDMI drivers while not interfering normal operation. The ultra low clamping voltage on the system side allows HDMI drivers to not require such robust internal ESD designs. The 0.5 pF capacitance is low enough that with good layout it will easily pass the HDMI 2.0 data rates. Even with the introduction of a high speed CMC the ESD224 can still be used.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-05001 .

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-05001 .

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-05001 .

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-05001 .

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-05001 .

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-05001 .

5 Full Test Results

表 2 through 表 5 shows the full results from each of the Keysight's HDMI 2.0 Compliance tests.

表 2. Pretest HDMI 2.0 Compliance Results for TMDS181 with ESD224

PASS	Test Name	Actual Value	Margin	Pass Limits
Yes	HF1-2: Clock Rise Time	121.982 ps	62.60%	VALUE >= 75.000 ps
Yes	HF1-2: Clock Fall Time	115.296 ps	53.70%	VALUE >= 75.000 ps
Yes	HF1-6: Clock Duty Cycle(Minimum)	49.77	24.40%	>=40%
Yes	HF1-6: Clock Duty Cycle(Maximum)	49.99	16.70%	<=60%
Yes	HF1-6: Clock Rate	148.499900000 MHz	2.30%	85.000000000 MHz <= VALUE <= 150.000000000 MHz
Yes	HF1-7: Differential Clock Voltage Swing, Vs (TP1)	703 mV	37.90%	400 mV < VALUE < 1.200 V
Yes	HF1-5: D0 Maximum Differential Voltage	499	36.00%	VALUE <= 780 m
Yes	HF1-5: D0 Minimum Differential Voltage	-521	33.2 %	VALUE >= -780 m
Yes	HF1-2: D0 Rise Time	104.360 ps	145.60%	VALUE >= 42.500 ps
Yes	HF1-2: D0 Fall Time	96.940 ps	128.10%	VALUE >= 42.500 ps
Yes	HF1-5: D1 Maximum Differential Voltage	477	38.80%	VALUE <= 780 m
Yes	HF1-5: D1 Minimum Differential Voltage	-449	42.4 %	VALUE >= -780 m
Yes	HF1-2: D1 Rise Time	101.531 ps	138.90%	VALUE >= 42.500 ps

表 2. Pretest HDMI 2.0 Compliance Results for TMDS181 with ESD224 (continued)

Yes	HF1-2: D1 Fall Time	87.482 ps	105.80%	VALUE >= 42.500 ps
Yes	HF1-5: D2 Maximum Differential Voltage	491	37.10%	VALUE <= 780 m
Yes	HF1-5: D2 Minimum Differential Voltage	-480	38.5 %	VALUE >= -780 m
Yes	HF1-2: D2 Rise Time	98.313 ps	131.30%	VALUE >= 42.500 ps

表 3. Post Test HDMI 2.0 Compliance Results for TMDS181 with ESD224

PASS	Test Name	Actual Value	Margin	Pass Limits
Yes	HF1-5: D0 Maximum Differential Voltage	501 m	35.80%	VALUE <= 780 m
Yes	HF1-5: D0 Minimum Differential Voltage	-516 m	33.8 %	VALUE >= -780 m
Yes	HF1-2: D0 Rise Time	106.899 ps	151.50%	VALUE >= 42.500 ps
Yes	HF1-2: D0 Fall Time	102.079 ps	140.20%	VALUE >= 42.500 ps
Yes	HF1-5: D1 Maximum Differential Voltage	478 m	38.70%	VALUE <= 780 m
Yes	HF1-5: D1 Minimum Differential Voltage	-451 m	42.2 %	VALUE >= -780 m
Yes	HF1-2: D1 Rise Time	105.920 ps	149.20%	VALUE >= 42.500 ps
Yes	HF1-2: D1 Fall Time	92.138 ps	116.80%	VALUE >= 42.500 ps
Yes	HF1-5: D2 Maximum Differential Voltage	489 m	37.30%	VALUE <= 780 m
Yes	HF1-5: D2 Minimum Differential Voltage	-467 m	40.1 %	VALUE >= -780 m
Yes	HF1-2: D2 Rise Time	103.204 ps	142.80%	VALUE >= 42.500 ps
Yes	HF1-2: D2 Fall Time	100.198 ps	135.80%	VALUE >= 42.500 ps
Yes	HF1-3: Inter-Pair Skew - D0/D1	-6 mTpixel	48.5 %	-200 mTpixel <= VALUE <= 200 mTpixel
Yes	HF1-3: Inter-Pair Skew - D0/D2	-28 mTpixel	43.0 %	-200 mTpixel <= VALUE <= 200 mTpixel
Yes	HF1-3: Inter-Pair Skew - D1/D2	-23 mTpixel	44.3 %	-200 mTpixel <= VALUE <= 200 mTpixel

表 4. Pretest HDMI 2.0 Compliance Results for DP159 with ESD224 and CMC

Pass	Test Name	Actual Value	Margin	Pass Limits
Yes	HF1-2: Clock Rise Time	125.299 ps	67.10%	VALUE >= 75.000 ps
Yes	HF1-2: Clock Fall Time	122.345 ps	63.10%	VALUE >= 75.000 ps
Yes	HF1-6: Clock Duty Cycle(Minimum)	49.77	24.40%	>=40%
Yes	HF1-6: Clock Duty Cycle(Maximum)	49.99	16.70%	<=60%
Yes	HF1-6: Clock Rate	148.499500000 MHz	2.30%	85.000000000 MHz <= VALUE <= 150.000000000 MHz
Yes	HF1-7: Differential Clock Voltage Swing, Vs (TP1)	813 mV	48.40%	400 mV < VALUE < 1.200 V
Yes	HF1-5: D0 Maximum Differential Voltage	485 m	37.80%	VALUE <= 780 m
Yes	HF1-5: D0 Minimum Differential Voltage	-502 m	35.6 %	VALUE >= -780 m
Yes	HF1-2: D0 Rise Time	83.125 ps	95.60%	VALUE >= 42.500 ps

表 4. Pretest HDMI 2.0 Compliance Results for DP159 with ESD224 and CMC (continued)

Yes	HF1-2: D0 Fall Time	76.774 ps	80.60%	VALUE >= 42.500 ps
Yes	HF1-5: D1 Maximum Differential Voltage	426 m	45.40%	VALUE <= 780 m
Yes	HF1-5: D1 Minimum Differential Voltage	-401 m	48.6 %	VALUE >= -780 m
Yes	HF1-2: D1 Rise Time	95.263 ps	124.10%	VALUE >= 42.500 ps
Yes	HF1-2: D1 Fall Time	89.026 ps	109.50%	VALUE >= 42.500 ps
Yes	HF1-5: D2 Maximum Differential Voltage	446 m	42.80%	VALUE <= 780 m
Yes	HF1-5: D2 Minimum Differential Voltage	-430 m	44.9 %	VALUE >= -780 m
Yes	HF1-2: D2 Rise Time	90.850 ps	113.80%	VALUE >= 42.500 ps
Yes	HF1-2: D2 Fall Time	91.757 ps	115.90%	VALUE >= 42.500 ps

表 5. Post Test HDMI 2.0 Compliance Results for DP159 with ESD224 and CMC

Pass	Test Name	Actual Value	Margin	Pass Limits
Yes	HF1-2: Clock Rise Time	125.817 ps	67.80%	VALUE >= 75.000 ps
Yes	HF1-2: Clock Fall Time	122.366 ps	63.20%	VALUE >= 75.000 ps
Yes	HF1-6: Clock Duty Cycle(Minimum)	49.77	24.40%	>=40%
Yes	HF1-6: Clock Duty Cycle(Maximum)	49.99	16.70%	<=60%
Yes	HF1-6: Clock Rate	148.499400000 MHz	2.30%	85.000000000 MHz <= VALUE <= 150.000000000 MHz
Yes	HF1-7: Differential Clock Voltage Swing, Vs (TP1)	813 mV	48.40%	400 mV < VALUE < 1.200 V
Yes	HF1-5: D0 Maximum Differential Voltage	492 m	36.90%	VALUE <= 780 m
Yes	HF1-5: D0 Minimum Differential Voltage	-494 m	36.7 %	VALUE >= -780 m
Yes	HF1-2: D0 Rise Time	86.678 ps	103.90%	VALUE >= 42.500 ps
Yes	HF1-2: D0 Fall Time	79.564 ps	87.20%	VALUE >= 42.500 ps
Yes	HF1-5: D1 Maximum Differential Voltage	424 m	45.60%	VALUE <= 780 m
Yes	HF1-5: D1 Minimum Differential Voltage	-398 m	49.0 %	VALUE >= -780 m
Yes	HF1-2: D1 Rise Time	102.296 ps	140.70%	VALUE >= 42.500 ps
Yes	HF1-2: D1 Fall Time	90.565 ps	113.10%	VALUE >= 42.500 ps
Yes	HF1-5: D2 Maximum Differential Voltage	451 m	42.20%	VALUE <= 780 m
Yes	HF1-5: D2 Minimum Differential Voltage	-429 m	45.0 %	VALUE >= -780 m
Yes	HF1-2: D2 Rise Time	90.854 ps	113.80%	VALUE >= 42.500 ps
Yes	HF1-2: D2 Fall Time	90.391 ps	112.70%	VALUE >= 42.500 ps

6 Related Documentation

1. *ESD224 Datasheet*
2. *TMDS181RGZ Evaluation Module*
3. *TMDS181 Datasheet*
4. *DP159 Datasheet*
5. *IEC 61000-4-x Tests for TI's Protection Devices*
6. *TI ESD Protection Devices and the HDMI CTS*
7. *ESD Protection for HDMI Applications*

6.1 商標

7 About the Author

CAMERON PHILLIPS is an applications engineer at Texas Instruments where he is responsible for developing reference designs for TI's ESD and Surge portfolio. Cameron earned his bachelor of science in electrical engineering from Texas A&M University.

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