参考資料

TI Designs: TIDA-01633
コンパクトでプログラム可能な4mA～20mA、±10VのAC/サーボ・ドライブ用アナログ出力のリファレンス・デザイン

TEXAS INSTRUMENTS

概要

このリファレンス・デザインでは、ACインバータおよびサーボ・ドライブ用の、小さな外形で2チャネルの構成可能なアナログ電圧および電流出力モジュールを実現します。統合された産業用出力ドライバのXTR305により、複数のオペアンプとパッシブ部品を使用した場合と比べてサイズが小さくなります。出力は C2000™MCUなどのホストMCUにより、またはジャンパーでの手動構成により、±10Vまたは4mA～20mAにプログラム可能です。エラー・フラグと出力負荷監視機能により、堅牢な設計が可能になります。同じチャネルを、±10Vまたは4mA～20mAのアナログ入力としても構成可能です。インターフェイスは、C2000 Launchpadに適合します。

リソース

TIDA-01633	デザイン・フォルダ
XTR305	プロダクト・フォルダ
TVS1400	プロダクト・フォルダ
TLV431A	プロダクト・フォルダ
LMZM23601	プロダクト・フォルダ

TI E2E™ Community

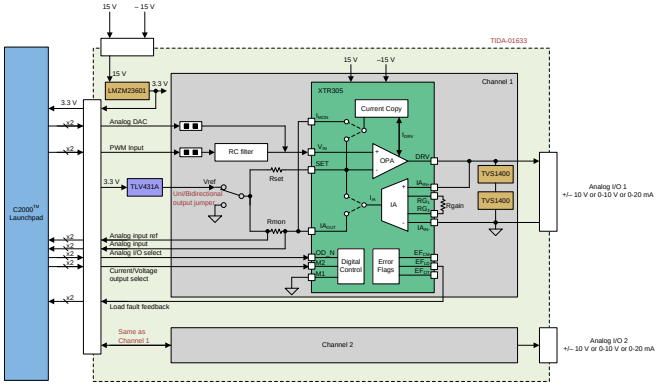
E2E™エキスパートに質問

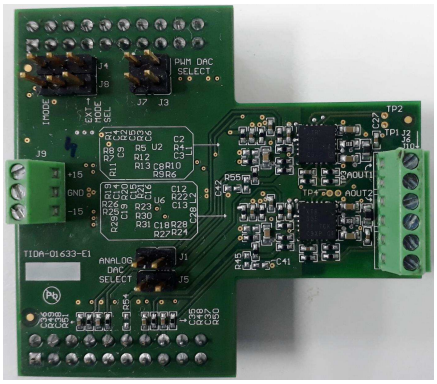
特長

- 2つのシングル・エンドのプログラム可能アナログ電圧および電流出力、または電圧入力
- 正確な±10V電圧および0mA～20mA電流出力、温度範囲-40℃～+85℃において、較正後の標準誤差0.1%未満
- ±10Vのアナログ入力、較正後の標準誤差1%未満。4mA～20mAの電流入力は、外付けの500Ω抵抗を使用して電圧に変換する必要あり
- 保護、診断、監視機能
  - 堅牢な短絡電流制限付きの出力と、短絡および開放負荷障害の検出とMCUフィードバック
  - 出力負荷監視により予知保全が可能
- 高いEMC耐性: 基準Aにおいて4kV ESD、2kV EFT、1kVサージのIEC61800-3 EMC耐性要件に合格
- ホストMCUインターフェイスはアナログDAC入力信号とPWM入力信号の両方に対応

アプリケーション

- ACインバータおよびVFドライブ
- サーボ、CNC、ロボティクス
- PLCアナログ出力モジュール
- 産業用ロボットのIOモジュール
- 混合IOモジュール





1 System Description

図 1 shows the components for a generic, analog output use-case. The motor is coupled to a load setup which requires an application specific torque speed profile. The application can be a fan, compressor, pump, conveyor system, machine tool, elevator system, and so forth. The variable frequency drive (VFD) controls the motor whose torque speed output has to match the load requirement. The VFD continuously monitors the speed and torque of the motor and provides feedback to the programmable logic controller (PLC). The PLC then closes the control loop by providing control set points to the VFD. This communication between the VFD and PLC occurs through analog signals. The analog output from the drive is connected to the analog input terminals of the PLC. Typically in a VFD, the analog output is either a 0-V to 10-V, ±10 V, or 4-mA to 20-mA signal. The connection is generally created by using shielded, twisted pair cables. The VFD analog output can also be programmed to transmit parameters such as motor phase current, DC-link voltage, motor shaft position, and so forth.

In an industrial environment the analog output cables run in close proximity to the motor power cables, high-voltage switchgear, and other electrical noise generating equipment. Opening and closing of contactors, startup of motors, short circuit failures, arc faults, and lightning strike surges can cause transient noise (EFT, Surge) to get coupled into the analog output cables. Handling cables, such as connecting and disconnecting cables from the analog output connectors, can cause ESD strikes. The analog output interface must be robust and capable of handling the noise transients.

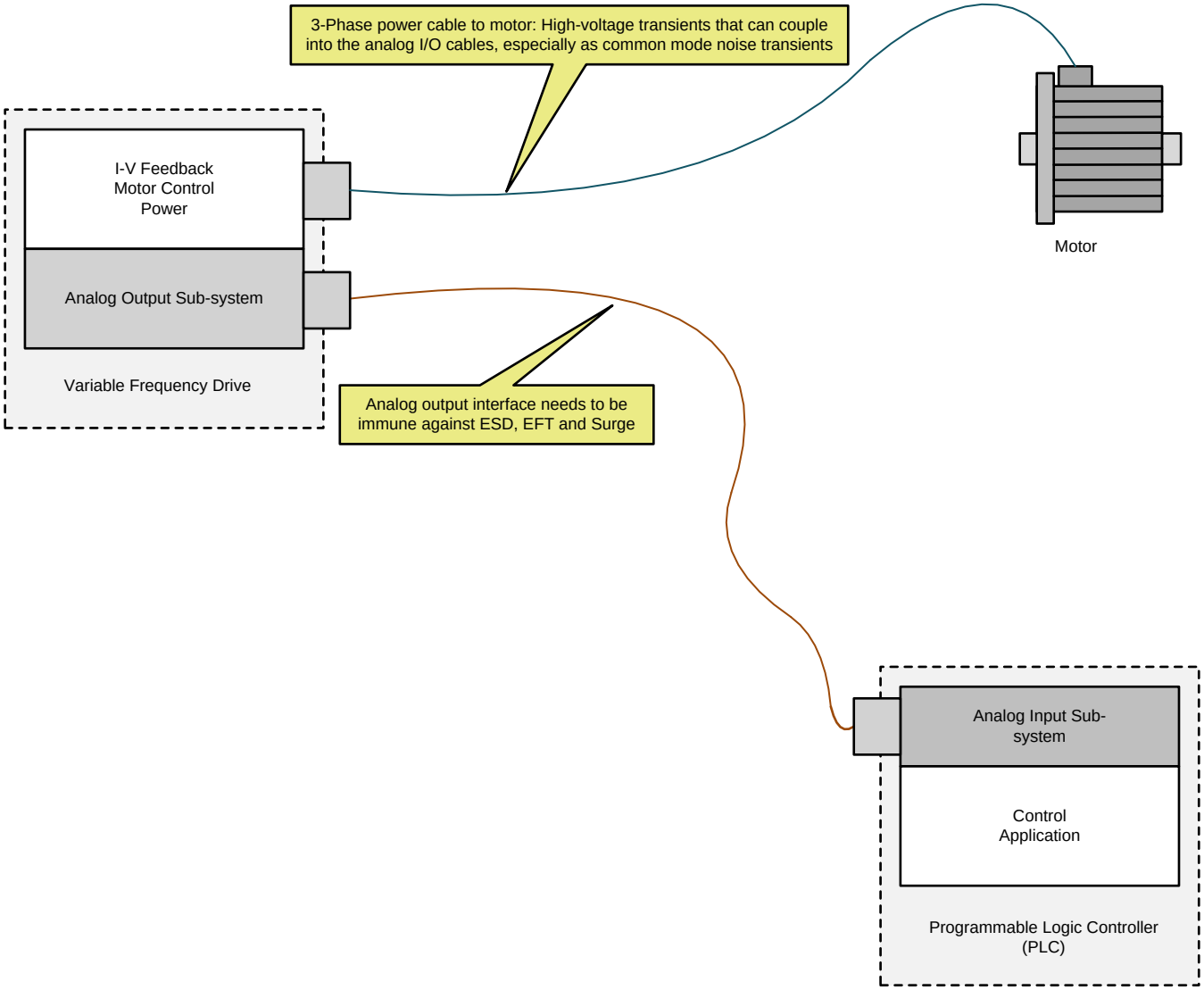


図 1. Analog Output Use Case in Motor Drives

図 2 shows a typical example of discrete and partially discrete implementations of the analog output. Op amp based circuits are used for voltage output and a current mirror circuit is used for current output. The outputs are then connected to the output pin either through an analog multiplexer or through a manual jumper configuration.

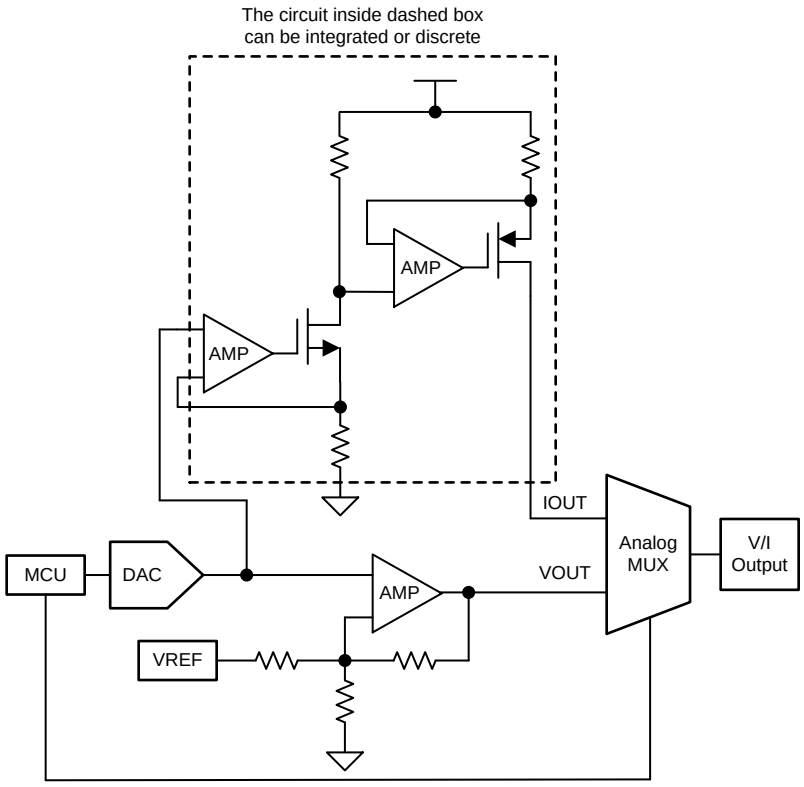


図 2. Discrete and Partially Discrete Analog Output Implementation Example

This TI Design implements a fully integrated solution using XTR305 analog output driver as shown in 図 3. The integrated solution enables a smaller solution form factor and reduced bill of material (BOM) size. There is no need for precise current sensing shunt resistors and shunt voltage measurement with high common-mode rejection amplifiers for the current output. The same analog output pin can be software programmed to current or voltage output without additional analog multiplexers. The inbuilt over-current limit protection and advanced diagnostic features enable detection of short circuit and open load faults which increases the drive reliability. It is also possible to use the same channel as analog input instead of output by disabling the XTR305 output drive stage and using the feedback channel of the device, which increases the functional flexibility of a single pin.

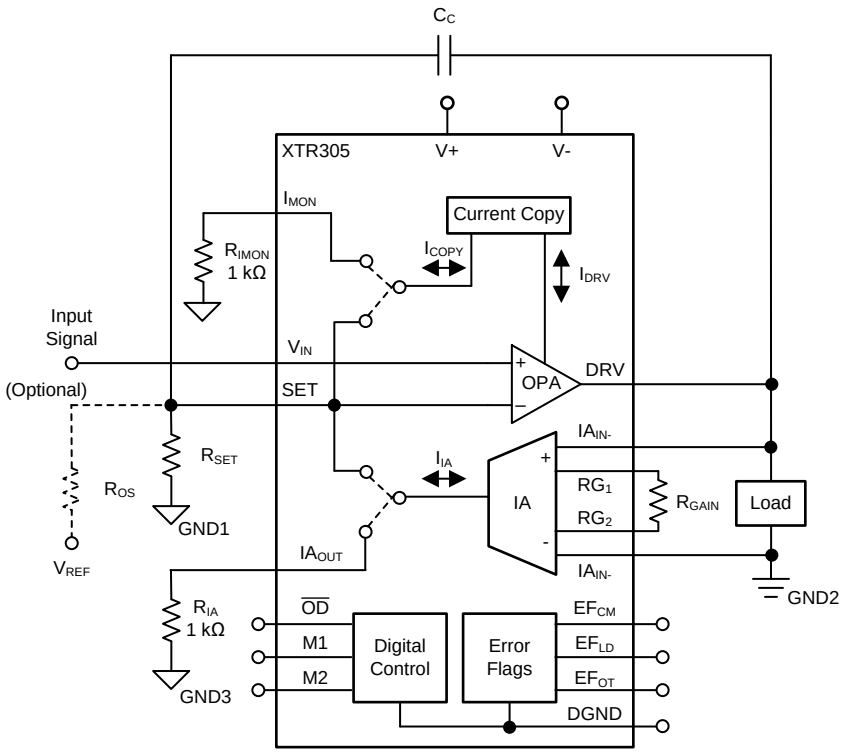


図 3. XTR305 Based Fully Integrated Solution

This reference design demonstrates the following:

- Small form factor and reduced BOM
- Programmable analog voltage or current output
- Accurate output performance over temperature range
- High EMC immunity: Meets IEC61000-4-2 (ESD), IEC61000-4-4 (EFT) and IEC61000-4-5 (Surge) according to IEC61800-3
- Protection and diagnostic features

1.1 Key System Specifications

表 1. TIDA-01633 Specifications

SUB-SECTION	PARAMETER	SPECIFICATIONS	COMMENT
Pin Mode Selection	Programmable	Voltage or Current Output or Input	Using 3.3-V CMOS/TTL interface to host MCU or via jumpers (2.3.4)
Voltage Output	Voltage Range	±10 V (図 23)	Corresponds to input control voltage of 0.4 V to 2.9 V with gain of 8 V/V
	% FSR Error	< 0.1% typical calibrated (図 25)	At 25°C
	Temperature Drift	< 175 ppm/K	Mainly dominated by 1.65-V reference setting resistors. Selection of 25-ppm resistors will reduce drift to <100 ppm/K
	Bandwidth	800 Hz (図 31)	
	Rise Time	~ 1 ms (図 28)	Faster rise time is possible by changing compensation capacitor and feedback capacitor
Current Output	Current Range	0 mA to 20 mA (図 36)	Corresponds to input control voltage of 1.65 V to 2.9 V with a gain of 16 mA/V
	%FSR Error	< 0.1% typical calibrated (図 38)	At 25°C
	Temperature Drift	<175 ppm/K	Mainly dominated by 1.65-V reference setting resistors. Selection of 25-ppm resistors reduces the drift to <100 ppm/K
	Bandwidth	800 Hz (図 44)	
	Rise Time	~ 1 ms (図 41)	Faster rise time is possible by changing compensation capacitor and feedback capacitor
Voltage Input	Voltage Range	±10 V (図 53)	
	% FSR Error	< 1% typical calibrated (図 55)	
Power Supply	Voltage	±15 V Nominal	Can use ±12 V. Ensure that the maximum output voltage swing is within the compliance voltage swing range for the operating conditions
Feedback	Output Current Monitor Feedback	±1.238 V corresponding to ±20-mA load current	During voltage output mode
	Output Voltage Monitor Feedback	0 V to +1.238 V corresponding to 0 V to 10 V across the load	During current output mode
Interface to Controller	C2000 Launchpad Interface	表 4 and 表 5 for pin assignments	LAUNCHXL-F28379D used for EMC testing
Operating Conditions	Temperature Range	–40 to +85°C	The XTR305 is specified over the –40°C to +85°C industrial temperature range and is operational over the extended industrial temperature range of –55°C to +125°C
Protection Features	Short Circuit Detection Threshold	±20 mA nominal	During voltage output mode
	Open Load Detection	Output saturation into supply rails	During current output mode
	Load Monitoring	Output current and voltage feedback enables load monitoring for predictive maintenance	
EMC (Shielded Cable)	ESD	4 kV CD (3.2.5.1)	Tested according to IEC61000-4-2
	EFT	2 kV (3.2.5.2)	Tested according to IEC61000-4-4
	Surge	1 kV (3.2.5.3)	Tested according to IEC61000-4-5
Printed-Circuit Board (PCB) Information	PCB Layer Stack	4 layer, 1-oz copper	
	Laminate	FR4, high Tg	
	PCB Thickness	1.6 mm	
	PCB Size	25.4 mm × 24.13 mm	Solution size - Area of PCB containing XTR305 circuit. Not including launchpad interface connectors

2 System Overview

2.1 Block Diagram

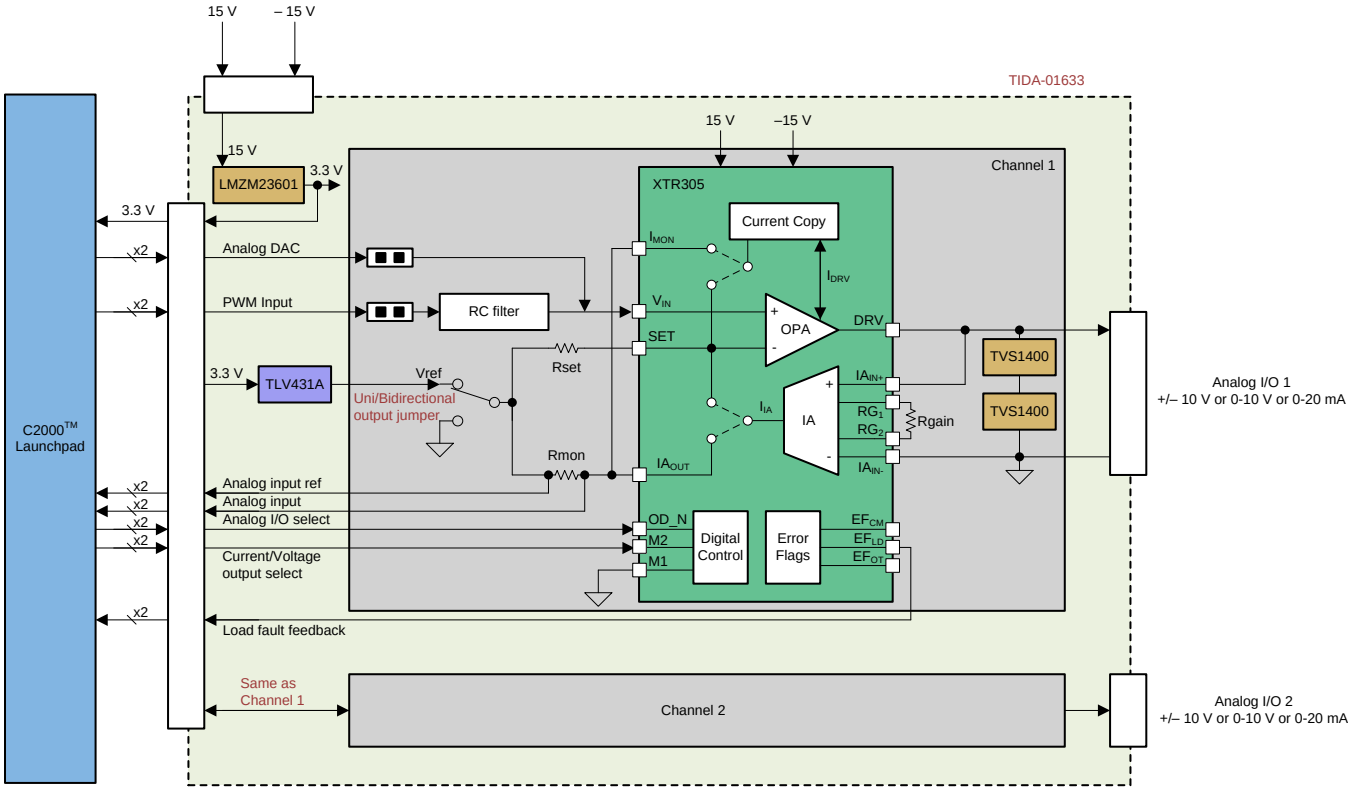


図 4. TIDA-01633 Block Diagram

This reference design is a two-channel configurable current and voltage analog output. 図 4 shows channel 1 in detail and channel 2 with minimal detail, however, it is the same as channel 1. The key part is the XTR305, which is an industrial analog current or voltage output driver. The XTR305 takes an analog input control signal and drives a proportional analog output. The output is configured as current output if M2 is high, M1 is low, and voltage output if M2, M1 are low. In this design M1 is hardwired to ground and M2 can be driven either digitally through a C2000 Launchpad GPIO or is manual jumper configurable. The input to output gain of the XTR305 is set by Rset and Rgain. The gain components in this design are selected for ±10-V or ±20-mA output. Two TVS1400 transient voltage suppressor diodes are used in bidirectional configuration for protecting the analog output from surge and ESD strikes.

The input control voltage to the XTR305 can be an analog DAC or a PWM signal which can be selected through jumpers. If a PWM signal is selected it is converted to a DC signal by passing through a 3rd order RC filter before connecting to the device. An unipolar input signal drives a bipolar analog output, this requires the input stage of the XTR305 to be biased to an intermediate reference voltage Vref. This is generated by shunt regulator TLV431A from a 3.3-V input.

The load fault monitor output of the XTR305 is routed to the connector. This signal indicates a short-circuit fault on the output during current and voltage modes and an open-load fault during current output mode. The XTR305 is also capable of monitoring analog output load. The output current can be sensed on the analog feedback signal during voltage output mode and the output voltage is sensed during the current output mode.

If one of the analog output channels is not used, then it can be configured as an analog input channel. This is done by pulling the output disable pin OD_N low which disables the XTR305 output drive and puts it in high-impedance mode. The M2 pin is made high to connect the instrumentation amplifier output IAout to the analog feedback channel. Analog voltage inputs (±10 V) can be sensed directly but the analog current inputs need to be converted to voltage by adding an external burden resistor. This feature improves the flexibility of a single analog I/O pin.

The pin allocation of the connectors is compatible with a C2000 Launchpad. The board requires an external ±15-V supply for powering the XTR305, which drives the analog outputs. An LMZM23601 DC/DC converter module is used to generate 3.3 V from 15 V. This 3.3 V is used for powering the Launchpad, if used, and for interfacing the open collector fault monitor signals to the Launchpad GPIO's.

2.2 Highlighted Products

2.2.1 XTR305

The XTR305 is a complete output driver for cost-sensitive industrial and process control applications. The output can be configured as current or voltage by the digital I/V select pin. No external shunt resistor is required. Only external gain-setting resistors and a loop compensation capacitor are required.

The separate driver and receiver channels provide flexibility. The instrumentation amplifier can be used for remote voltage sense or as a high-voltage, high-impedance measurement channel. In voltage output mode, a copy of the output current is provided, allowing calculation of load resistance.

The digital output-selection capability, error flags, and monitor pins make remote configuration and troubleshooting possible. Fault conditions on the output and on the IA input, as well as over-temperature conditions are indicated by error flags. The monitoring pins provide continuous feedback about load power or impedance. For additional protection, the maximum output current is limited and thermal protection is provided.

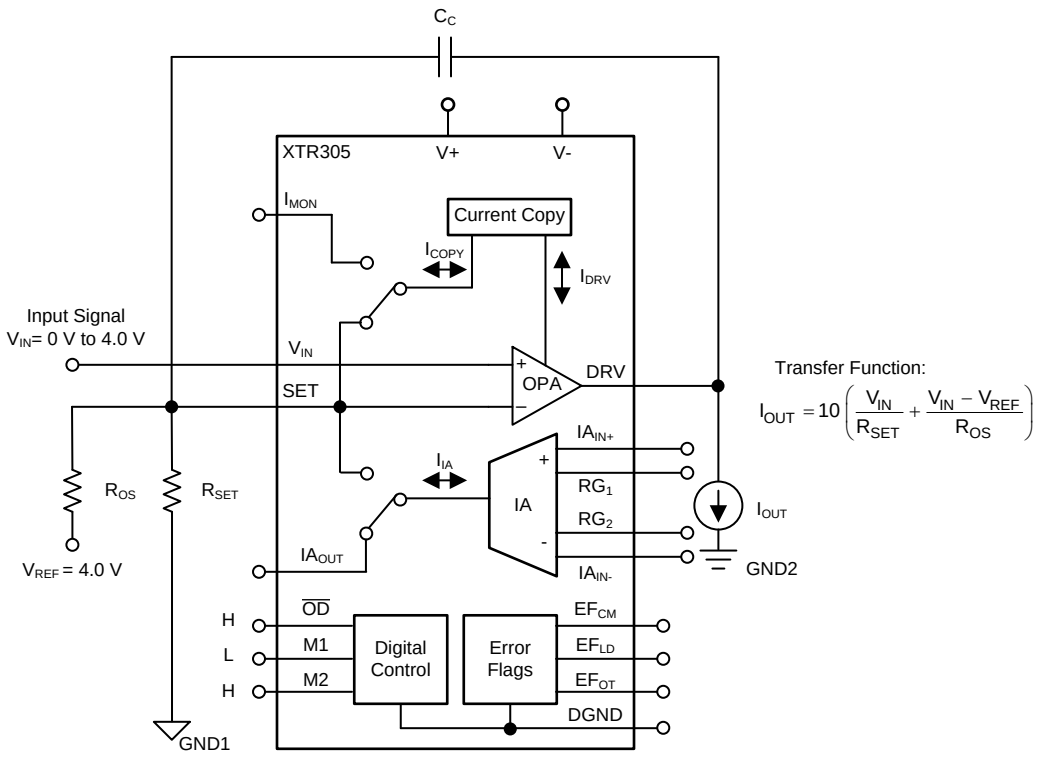


図 5. Functional Block of XTR305

2.2.2 TVS1400

The TVS1400 robustly shunts up to 43 A of IEC 61000-4-5 fault current to protect systems from high-power transients or lightning strikes. The device offers a solution to the common industrial signal line EMC requirement to survive up to ±2 kV IEC61000-4-5 open circuit voltage coupled through 42-Ω impedance. The TVS1400 uses a unique feedback mechanism to ensure precise flat clamping during a fault, assuring system exposure below 20 V. The tight voltage regulation allows designers to confidently select system components with a lower voltage tolerance, lowering system costs and complexity without sacrificing robustness.

The TVS1400 is available in a small 2 mm × 2 mm SON footprint which is designed for space constrained applications offering a 70% reduction in size compared to industry standard SMA and SMB packages. The extremely low device leakage and capacitance has a minimal effect on the protected line.

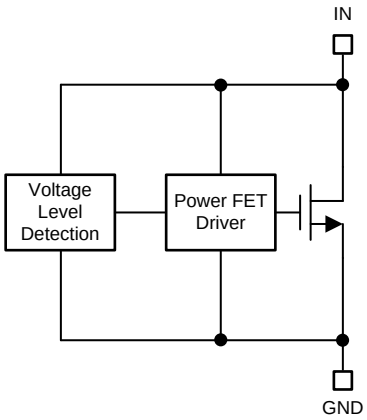


図 6. Functional Block of TVS1400

2.2.3 TLV431A

The TLV431A device is a low-voltage, 3-terminal adjustable voltage reference with specified thermal stability over applicable industrial and commercial temperature ranges. The typical output impedance is 0.25 Ω, and the output voltage can be set to any value between Vref (1.24 V) and 6 V with two external resistors. The devices are excellent replacements for low-voltage Zener diodes in many applications, including on-board regulation and adjustable power supplies, because of its active output circuitry, which provides a sharp turn-on characteristic.

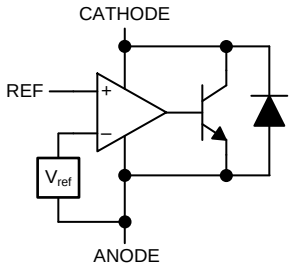


図 7. Functional Block of TLV431A

2.2.4 LMZM23601

This device is a nano module specifically designed for space-constrained industrial applications and is available in fixed output voltage options of 5 V and 3.3 V or an adjustable output voltage option with a range of 2.5 V to 15 V. The LMZM23601 supports an input voltage range of 4 V to 36 V and can deliver up to 1000 mA of output current. This nano module is extremely easy to use, requiring only two external components for a 5-V or 3.3-V output design. All aspects of the LMZM23601 are optimized for performance driven industrial applications with space constrained needs. An open drain, Power Good option provides a true indication of the system status. This feature negates the requirement for an additional supervisory component, saving cost and board space. Seamless transition between PWM and PFM modes along with a no-load supply current of only 30 µA ensures high efficiency and superior transient response for the entire load current range.

The device in this design powers the TLV431A based reference generation circuit, the pullups for XTR305 open collector signals, and the launchpad which can be used to control the analog output card.

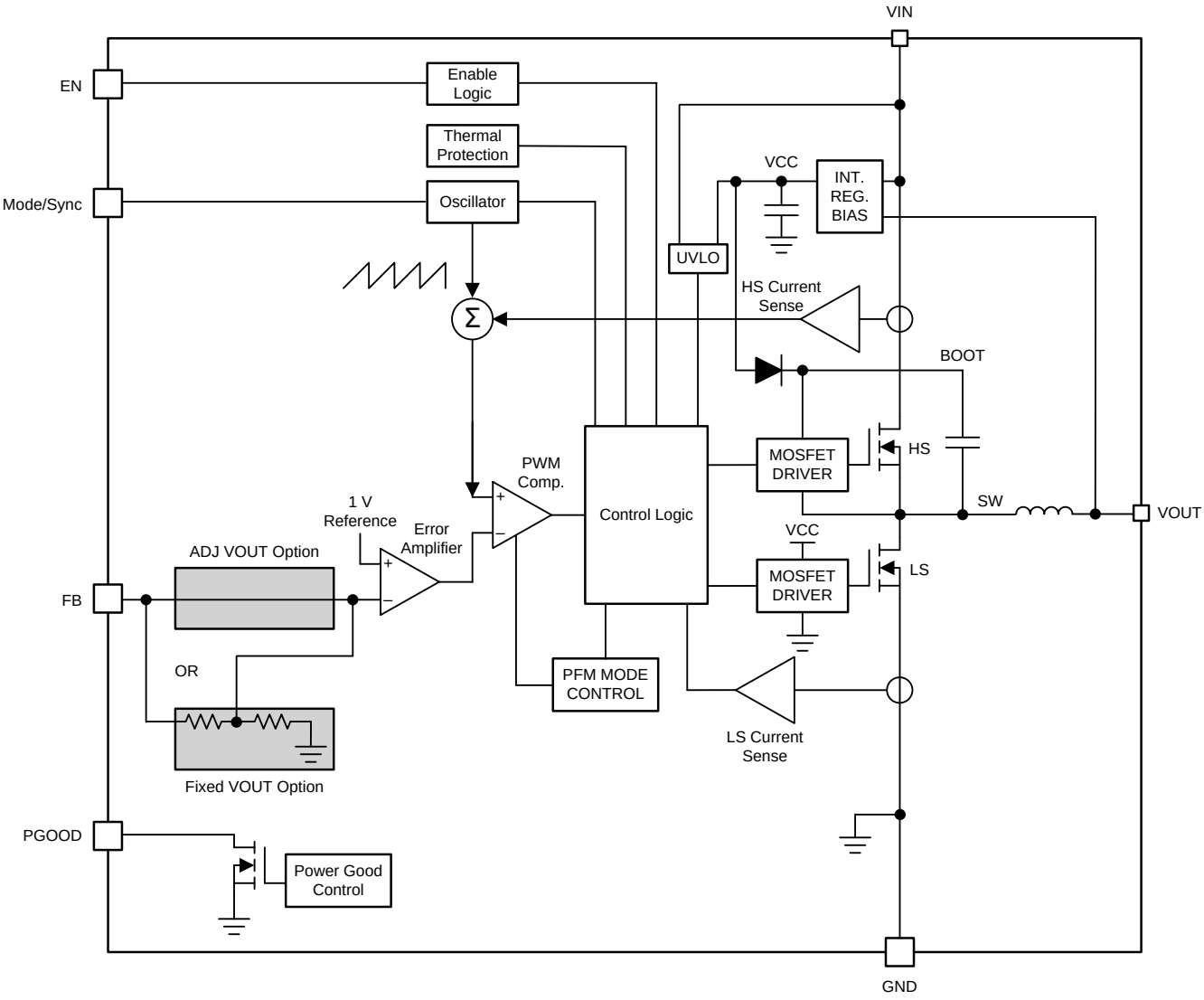


図 8. Functional Block of LMZM23601

2.3 System Design Theory

The XTR305 provides two basic functional blocks: an instrumentation amplifier (IA) and a driver that is a unique operational amplifier (OPA) for current or voltage output. During the current output mode a precision current mirror generates an exact 1/10th copy of the output current and this current is routed to the summing junction of the OPA to close the feedback loop. In the voltage output mode the IA amplifier senses the output voltage and feedback a current equal to 2 Vout/Rgain to the summing junction of the OPA to close the feedback loop.

図 9 shows the circuit for one analog output channel designed using XTR305. The second channel is designed in exactly the same way. The design steps are as follows:

- Select R5 for current output transfer function
- Select R10 for the voltage output transfer function
- Select EMC protection components

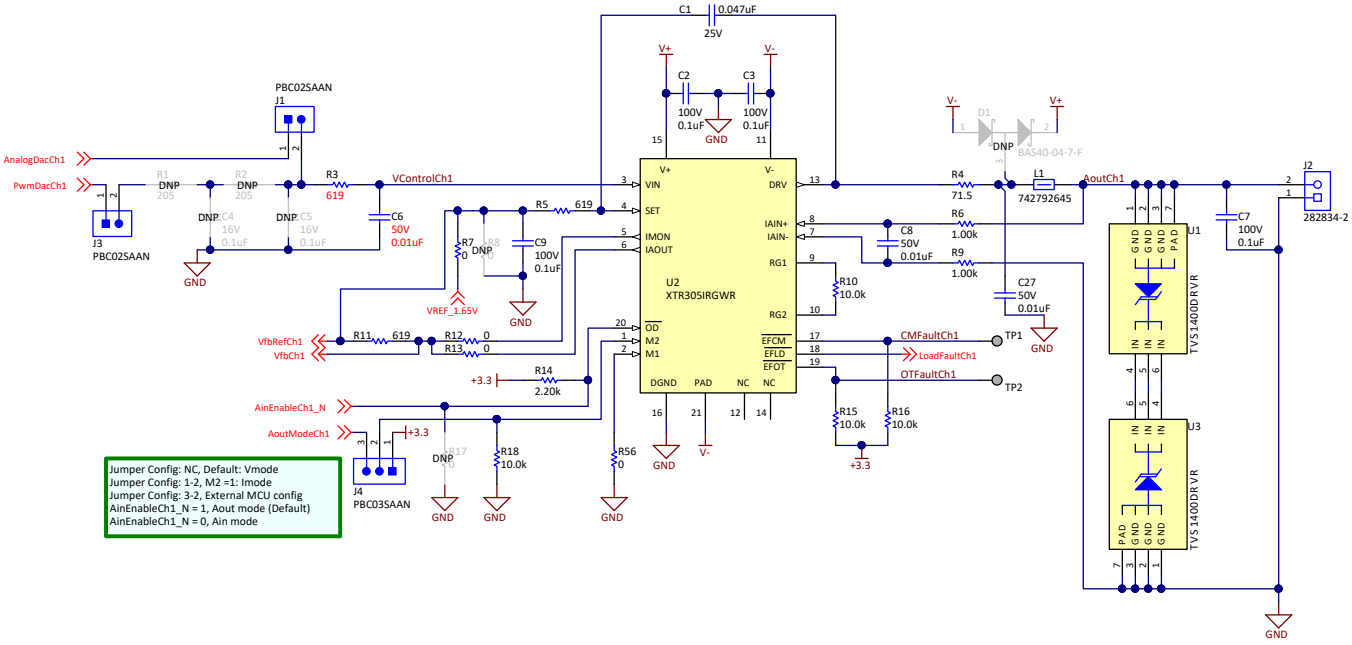


図 9. Analog Output Circuit

2.3.1 Current Output Mode

For this design a 0.4-V to 2.9-V control input is converted to a ±20-mA current output. As the output is bipolar and the input is unipolar, a reference bias voltage Vref is required on the input stage of the XTR305. The bias voltage selected is 1.65 V which means that ±1.25 V around 1.65 V translates to a ±20-mA current output.

The transconductance gain is set by R5 according to Equation 1

$$R5 = \left(\frac{10}{I_{outFSR}}\right) \times V_{inFSR} = \left(\frac{10}{40\ mA}\right) \times 2.5 = 625\ \Omega \quad (1)$$

Select R5 = 619 Ω which gives an IoutFSR of 40.38 mA (±20.19 mA)

The transfer function is given by equation: Iout = (10/R5) × (Vin-Vref)

$$Iout = \left(\frac{10}{R5}\right) \times (Vin - Vref) \quad (2)$$

During the current output mode it is possible to monitor the output load voltage, see 2.3.7.

2.3.2 Voltage Output Mode

A 0.4-V to 2.9-V control input is translated to a ±10-V voltage output. For unipolar to bipolar translation a 1.65-V bias voltage has been selected. This means that ±1.25 V around 1.65 V translates to a ±10-V output

The gain is set by R5 and R10 as per Equation 3

$$R10 = \frac{2 \times V_{outFSR} \times R5}{V_{inFSR}} = \frac{2 \times 20 \times 619}{2.5} = 9904\ \Omega \quad (3)$$

Select R10 = 10 kΩ which gives an VoutFSR of 20.19 V (±10.10 V)

The transfer function is given by Equation 4

$$Vout = \frac{R10 \times (Vin - Vref)}{(2 \times R5)} \quad (4)$$

During the voltage output mode it is possible to monitor the output load current, see 2.3.7.

2.3.3 EMC Protection Components

A drive analog output is typically connected to a PLC or motion controller using long cables in an industrial environment. These cables run along motor power cables and other noise generating sources like electrical contactors. The analog output has to be immune to transient noise signals like ESD, EFT and surge events which get coupled into the cable. The immunity to these noise transients can be quantified by passing tests as prescribed in IEC61800-3 (*Adjustable Speed Electrical Power Drive Systems – Part 3: EMC requirements and specific test methods*). IEC61800-3 points to IEC61000-4 for EMC test methods.

During each of these IEC61800-4 tests, the equipment under test (EUT) is monitored for performance deviations or total failure. Results are assigned to one of the four classes, see 表 2.

表 2. EMC Test Performance Criterion

GRADE	DESCRIPTION
Class A	The EUT must continue to operate as intended. No loss of function or performance even during the test.
Class B	Temporary degradation in performance during the test. The EUT continues to operate as expected after the test is complete.
Class C	Temporary degradation in performance during the test. The EUT needs to be manually restarted or put through a power off-on cycle to operate as expected after the test is complete.
Class D	Loss of function due to destruction of hardware.

The IEC61000-4 transients have two main components:

- High frequency component (ESD, EFT) – ESD events are typically caused by a person or insulator touching the connector terminals or the cable. These are temporary fast transients and the energy content is very low. EFT events are caused by sparks in the air due to the contactor closing and opening; other sources are VFD motor power cables in which the voltage switches rapidly between ±DC bus voltage. These are typically a burst of fast transient pulses with low energy content which get coupled into the cable.
- High energy component (Surge) – Surge strikes get coupled into the cable during motor startup, lightning strikes, and so forth. These are slower transients with high energy content.

The goal of protection components is to attenuate and divert the transients from damaging the sensitive electronic components. This design uses a combination of transient energy attenuation and diversion, see 図 10.

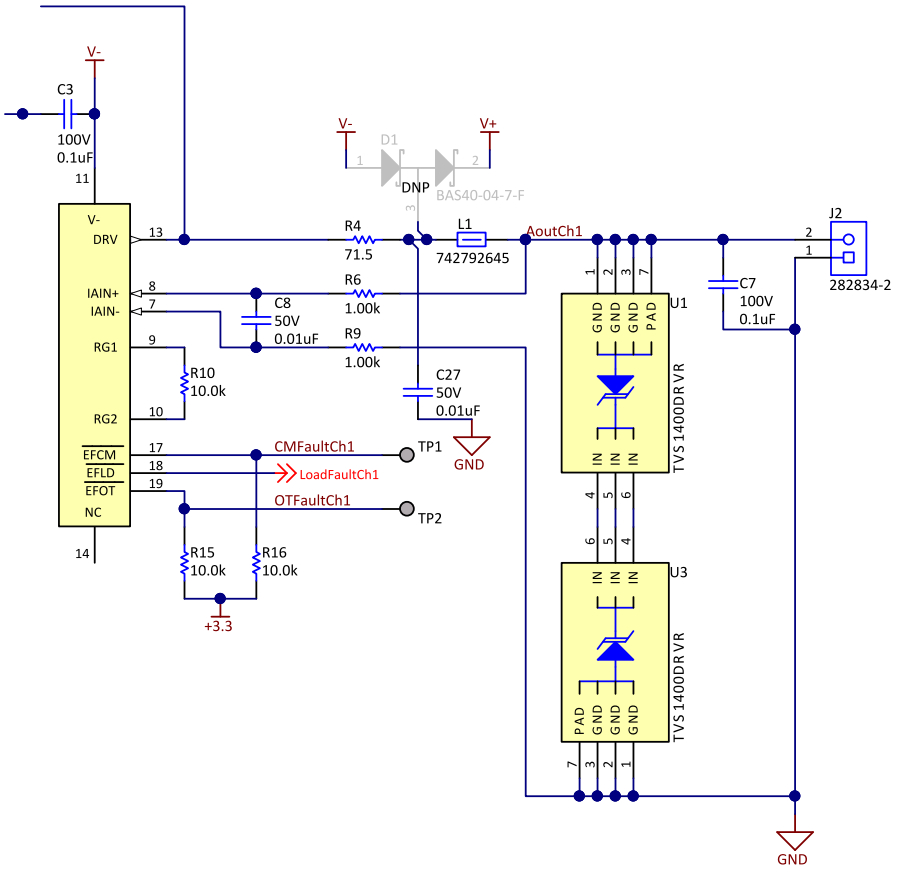


図 10. Output EMC Protection Components

- Capacitor C7 – 0.1 µF capacitor is placed on the output terminal. This capacitor is the first line of defense which attenuates and slows down the transient noise signals entering the PCB in combination with the transient generators source impedance.
- TVS U1, U3 – A bidirectional TVS diode is used to divert high voltage transients to earth. This design uses a symmetrical ±15-V supply voltage for the analog output driver. Therefore, two unidirectional TVS1400 diodes are placed back to back with opposite polarity. The working voltage of this diode is 14 V and the clamping voltage is ~18.4 V. A working voltage of 14 V means that during normal ±10-V operation the TVS diode does not interfere with the output. The output voltage increases to > 14 V only during fault conditions and this only increases the output leakage current into the TVS diode without deteriorating the TVS or reducing its reliability. The leakage current returns back to normal once the fault condition is removed. Increase in leakage current during fault conditions is not an issue with the analog output performance. The advantage of using TVS1400 is that it offers ~ 70% reduction in size when compared to standard SMB, SMA packages. The small size allows the device to be kept close to the input connector lowering the length of path fault current will take through the system when compared to larger protection solutions. It has extremely low leakage and capacitance which ensures minimal interference during normal operation. The clamping performance is extremely flat when compared to standard TVS diodes. The flat clamping voltage ensures that the downstream components are stressed to a lower extent which increases the system reliability. The TVS1400 clamping voltage has better stability across temperature when compared to standard TVS diodes. The TVS1400 has an IEC61000-4-2 contact discharge rating of ±21 kV and IEC61000-4-5 (8/20 us) surge rating of 43 A

- Ferrite bead L1 – It has a DC resistance of 0.2 Ω and an impedance of 470 Ω at 100 Mhz. The ferrite bead does not interfere in the normal analog output operating frequency region, which is typically <1 kHz, but provides a high impedance to high-frequency transients.
- Capacitor C27 – This 10 nF capacitor along with the ferrite bead further filters the noise transients.
- Resistor R4 – If even after attenuation and diversion of transient energy there remains some residual energy this can be handled by the internal rail to rail clamp diodes on the DRV pin of XTR305. R4 limits the current into the clamping diodes. The clamping diodes can take a peak current of 50 mA. Therefore this resistor is selected to be (18.5 – 15.7)/50 mA = 56 Ω. A 71.5-Ω resistor is selected to provide sufficient margin.
- Schottky diode D1 – This external rail-to-rail clamping schottky diode is not populated in this design. It can be used if harsher EMC requirements are to met than tested in this design.
- Resistors R6 and R9 – The instrumentation amplifier inputs are also connected directly to the output connector. The inputs have rail-to-rail clamping diodes inside the device. In case of overvoltage transients, the diodes clamp to the ±15-V power rails. The current is limited by external 1-kΩ resistors R6 and R9. Equal values cancel the offset due to instrumentation amplifier input bias currents.
- Capacitor C8 – This additional 10-nF capacitor filters transient noise in the input signal to the instrumentation amplifier.
- R47, C33 and C34 are connected in parallel between the PCB ground and Earth terminals. These components provide a low-impedance path for the high frequency transient currents to flow into the earth but act as high impedance for the analog output operating frequency region.

2.3.4 Mode Selection

The analog output channel can be configured either digitally through MCU control or manually using jumpers according to 表 3. In this design, M1 is hardwired to GND and M2 is configurable.

表 3. Analog Output Mode Selection

M2	M1	MODE	DESCRIPTION
L	L	Vout	Voltage output mode, Isc = 20 mA
H	L	Iout	Current output mode, Isc = 32 mA
L	H	Ext	IA and IMON on external pins, Isc = 20 mA
H	H	Ext	IA and IMON on external pins, ISC = 32 mA

Manual configuration: By default the output is in voltage output mode as R18 pulls down M2 low. Connect J4 pins 1 and 2 for connecting M2 to 3.3 V, which changes output to current mode.

MCU configuration: Connect J4 pins 3 and 2 together. The mode is now controlled by signal AoutModeCh1, which is connected to Launchpad GPIO.

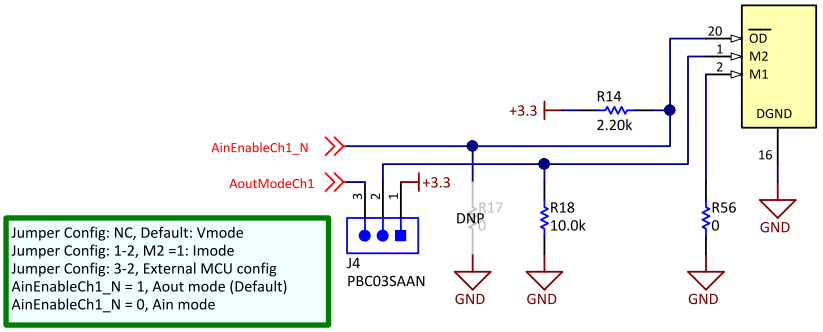


図 11. Analog Output Pin Mode Selection

2.3.5 Analog Output Control Methods

The analog output magnitude can be controlled either by analog input control signal or a PWM signal. The default use case in this design is through analog control signal for which the pins 1 and 2 of connector J1 have to be jumpered together. The AnalogDacCh1 signal gets connected to the Vin pin of XTR305 through RC filter comprising of R3 and C6. R3 is selected to be equal to R5 to cancel out offsets due to input bias current of the XTR305 device.

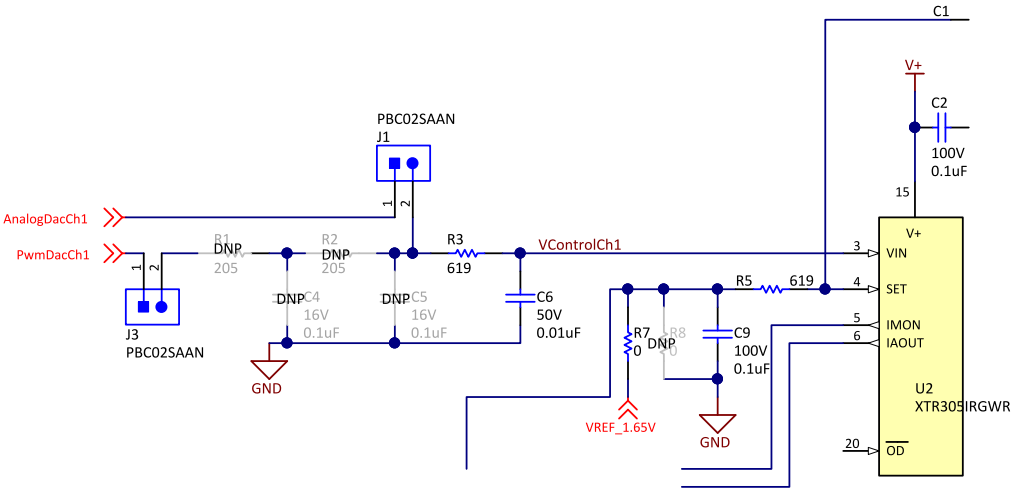


図 12. Analog DAC Based Control of Analog Output

If the use case is PWM control then pins 1 and 2 of connector J3 have to be jumpered together. The PwmDacCh1 gets connected to the Vin pin of XTR305 through a third order cascaded RC filter comprising of (R1, C4), (R2, C5) and (R3, C6). In this case select R1 = R2 = R3 = R5/3 and C4 = C5 = C6 = 100 nF. The PWM frequency is 100 kHz. A duty cycle variation from 12.12% to 87.87% corresponds to 0.4 V to 2.9 V at the Vin pin.

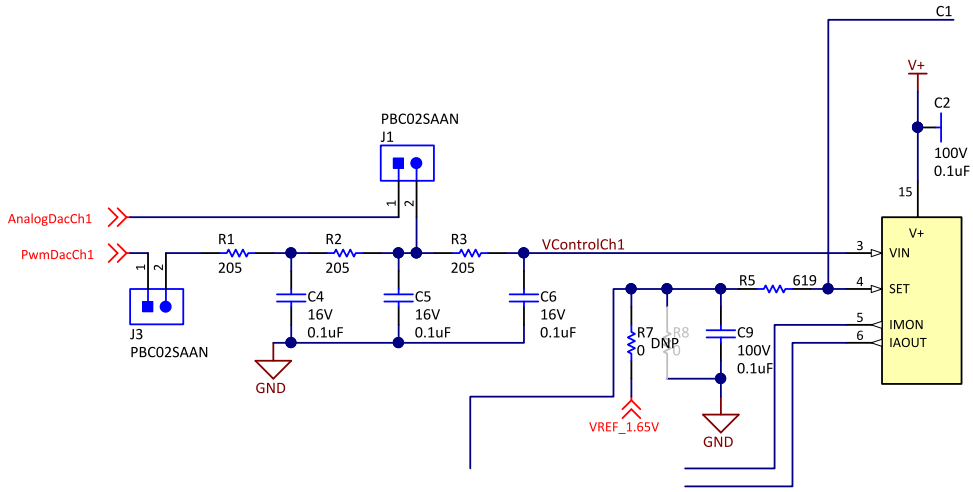


図 13. PWM Control of Analog Output

2.3.6 Analog Input

If an analog output channel is not used in the system it is possible to configure it as analog input. To do this pull down OD_N control pin to low and make M2 low. This disables the output DRV pin and connects the instrumentation amplifier output IAout to R11. The voltage across R11 is sensed by a pseudo differential ADC.

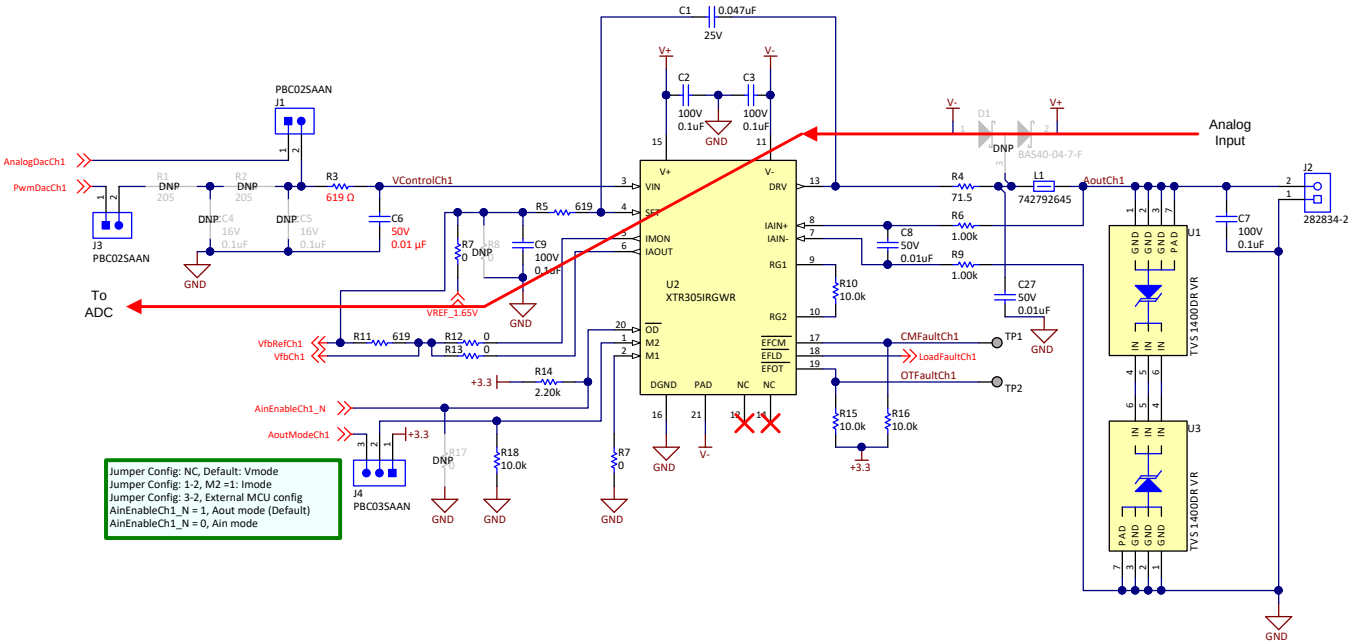


図 14. Analog Input Circuit

If the analog input is voltage it can be directly sensed through J2. If the input is current then it has to be converted into voltage by using an external burden resistor connected across J2. A 500-Ω resistor will convert the 0-mA to 20-mA current input to 0 V to 10 V.

The transfer function for the analog input is given by Equation 5

$$(\text{VfbCh1} - \text{VfbRefCh1}) = \left(\frac{2 \times \text{Voltage across J2 pins}}{\text{R10}}\right) \times \text{R11} \quad (5)$$

Which means that a ±10-V analog input translates to ±1.238 V at the ADC around the 1.65-V reference.

RC filters comprising of R51, C38 and R49, C36 are used on the ADC inputs. The capacitance is selected to be 100 times the input parasitic capacitance of the ADC. In this design the LAUNCHXL-F28379D ADC pins ADCINB5 and ADCINC5 are used, which have an input parasitic capacitance of ~5 pF. C38 and C36 are selected to be 820 pF. As the XTR305 is powered by ±15-V rails, it is possible that the IAout can become more than 3.3 V during fault conditions. The rail-to-rail clamping diodes D4 and D6 are used to clamp the ADC input to 3.3 V and GND.

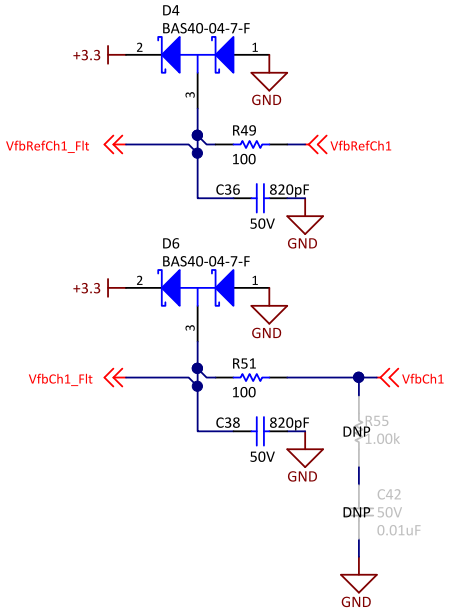


図 15. RC Filters on ADC Input

Note: By default the OD_N pin is pulled up to 3.3 V through R14, which configures the XTR305 device in analog output mode.

2.3.7 Diagnostic Features

Fault detection: The XTR305 device has inbuilt diagnostic features to detect overload, short-circuit load, over temperature of IC, and common-mode over voltage range on the instrumentation amplifier inputs.

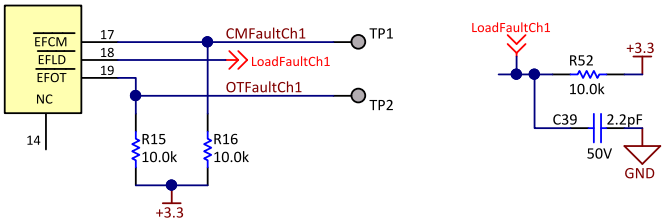


図 16. Error Flags

IA Common-Mode Over Voltage Range (EFcm): This flag goes low as soon as the input of the IA reach the limits of the linear operation for the input voltage. This can be monitored on test point TP1.

Over temperature Flag (Efot): This flag goes low if the chip temperature reaches 140°C and resets as soon as it cools down to 125°C. The flag can be monitored on test point TP2.

Load error (EFld): Indicates fault conditions driving voltage or current into the load. In voltage output mode, it monitors the voltage limits of the output swing and the current limit condition caused from short or low load resistance. In current output mode, it indicates a saturation into the supply rails from a high-load resistance or open load. In this design, this fault flag is connected to the Launchpad GPIO. The fault flag helps in detecting if the analog output wire is broken or shorted. This improves the reliability of the analog output function. In case of short-circuit load, the output current is limited to ±20 mA in the voltage output mode and ±32 mA in the current output mode.

All three fault flags are open collector and therefore need pullup resistors. Pullup resistors R15, R16 and R52 = 10 kΩ. C39 = 2.2 pF is a noise filter placed on the output for connecting to Launchpad.

Analog output monitor: During the current output mode IA output is connected to R11 through IAOUT pin and IMON is internally disconnected. IAOUT is proportional to the output voltage given by Equation 6. This current is converted into voltage across R11 which is sensed by a pseudo differential ADC. This enables to monitor the output power delivered to the load. If the load resistance is known then the output current can be calculated inside the Launchpad and compared with the commanded value.

$$IAout = \frac{2 \times Vout}{R10} \tag{6}$$

During the voltage output mode 1/10th of the output drive current is mirrored onto the IMON pin and IAOUT is internally disconnected. The IMON pin is connected to R11. The voltage across R11 is sensed by a pseudo differential ADC. If the output load is known, then the output voltage can be calculated and compared with the commanded value. The output power delivered to the load can also be calculated.

Output monitor functions helps detect load changes enabling predictive maintenance which increase reliability of the Aout function

2.3.8 Power Supplies and Reference

The XTR305 is powered from ±15-V supplies which have to be provided externally to the PCB through connector J9. C21 and C24 are local bulk capacitors on the PCB and C22, C23, C25 and C26 are noise decoupling capacitors.

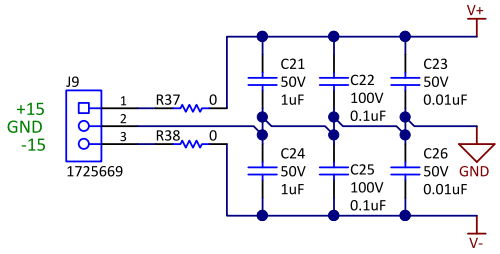


図 17. ±15-V External Supply

A C2000 launchpad can be used to control the TIDA-01633 PCB. In this case, a 3.3-V supply is required to power the Launchpad. This 3.3-V supply is generated from a 15-V supply using LMZM23601 DC/DC converter module. The output voltage is configured by R42 and R43 using Equation 7

$$Vout = \frac{Vfb \times (R43 + R42)}{R43}$$

- Where reference voltage, Vfb = 1 V (7)

R42 is selected as 10 kΩ. For 3.3-V output, R43 is calculated to be 4.34 kΩ. Select R43 = 4.32 kΩ

Low ESR ceramic capacitors are required on the output. For 3.3-V output, the LMZM23601 data sheet recommends a minimum value of 22 µF. C30 = 22 µF and C31 = 10 µF are used in this design. A 10-µF capacitor: C29 is used on the device input. The device is always enabled by connecting enable pin (EN) to VIN. The control mode is set to forced PWM mode by connecting MODE pin to VIN. In this mode the device switches at the internal clock frequency. The pad of the device is connected to GND plane for good heat sinking.

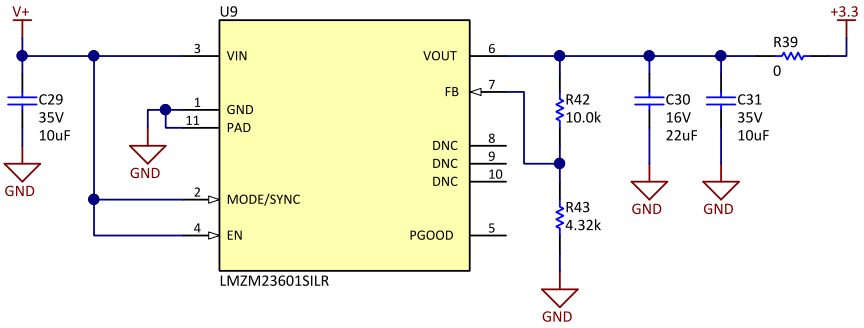


図 18. 15-V to 3.3-V Conversion

A 1.65-V reference bias Vref is required on the XTR305 input stage. This is to ensure bipolar output with a unipolar input. TLV431A adjustable precision shunt regulator is used in this design to generate the reference from a 3.3-V input. The reference voltage is set by R44 and R46 according to Equation 8

$$Vref = \frac{V1 \times (R46 + R44)}{R46}$$

- Where V1 = 1.24 V is the device internal reference voltage at pin 1 (8)

R46 is selected as 10 kΩ. For 1.65 V reference, R44 is calculated to be 3.306 kΩ. Select R44 = 3.32 kΩ

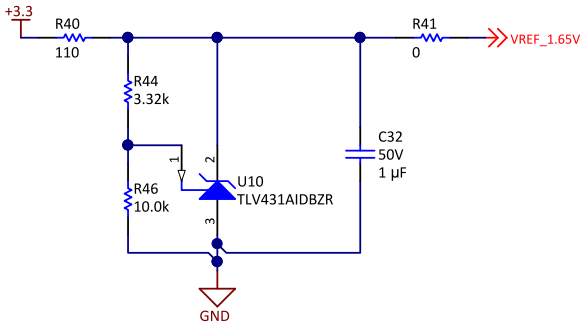


図 19. 1.65-V Reference Generation

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware

3.1.1 TIDA-01633 PCB Overview

The ±15-V DC supply and the analog outputs are connected to the TIDA-01633 PCB as shown in 図 20. J4 and J8 are used to configure the analog output mode of operation. By default the output is in voltage mode. To manually change to current output mode, a jumper has to be placed between the center pin and the right side pin. If MCU control of the output is required then a jumper is placed between the center pin and the left side pin. Jumper J3, J7, J1 and J5 are used to select the control input signal source. Placing jumpers on J1 and J5 enables output control using analog DAC signals. Placing jumpers on J7 and J3 enables output control using PWM signal. Note that for PWM control component changes are required, see schematic file in design tool folder.

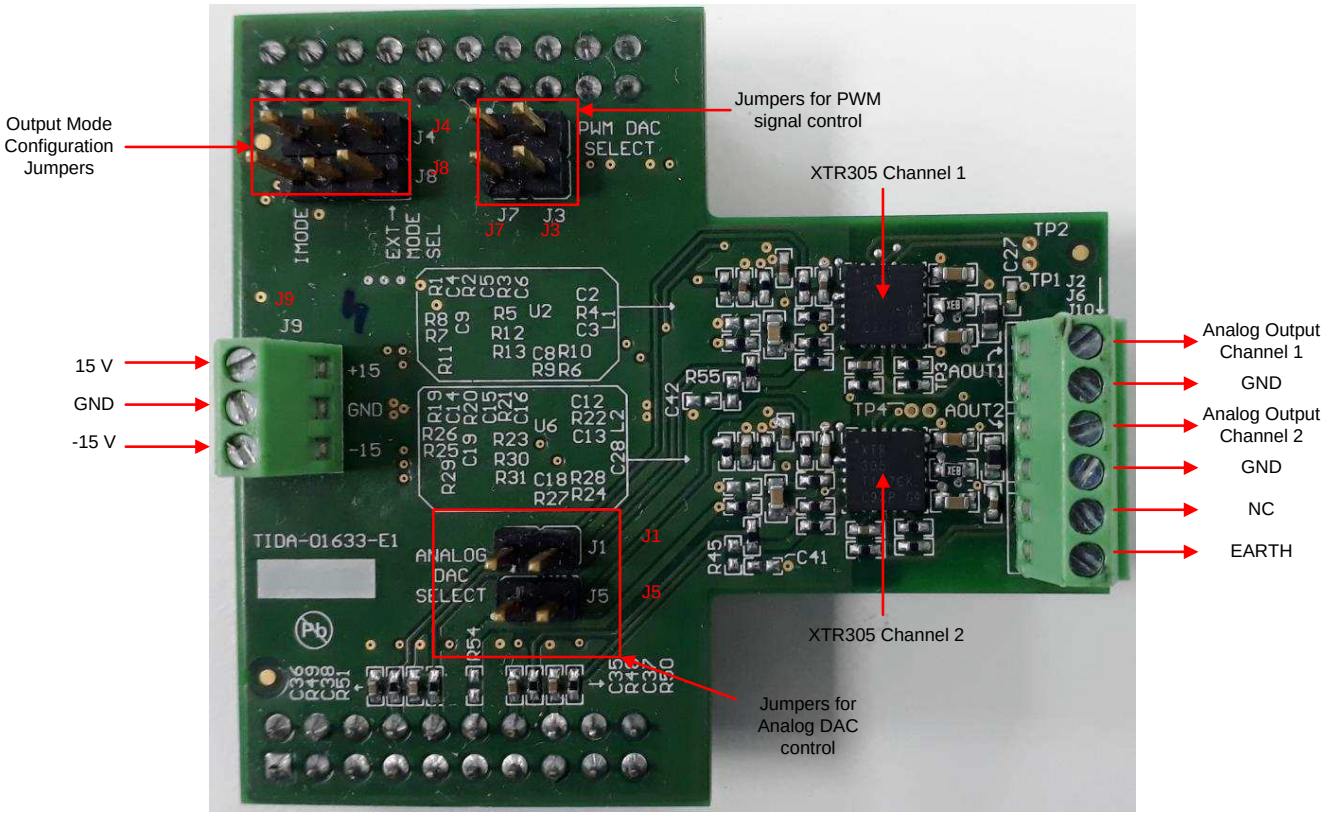


図 20. Top View of TIDA-01633

3.1.2 Controller Interface

TIDA-01633 can be interfaced with the LAUNCHXL-F28379D Launchpad as shown in 図 21. The pin functions assigned are shown in 表 4 and 表 5.

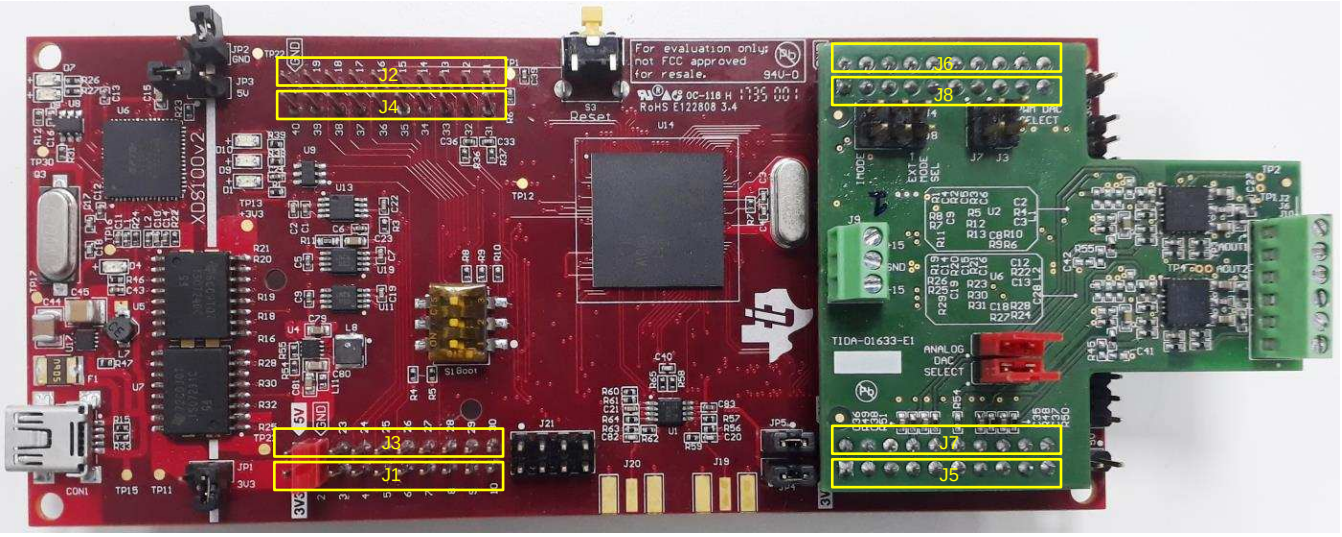


図 21. Launchpad Interface to TIDA-01633

表 4. TIDA-01633 J11 Interface to Launchpad J5, J7

TIDA-01633 FUNCTION	LAUNCHPAD FUNCTION USED	J5 PIN	J7 PIN	LAUNCHPAD FUNCTION USED	TIDA-01633 FUNCTION
3.3 V	3.3 V	41	61		
		42	62	GND	GND
		43	63		
		44	64	ADCINC5	VfbRefCh1_Flt
		45	65	ADCINB5	VfbCh1_Flt
		46	66		ExtRef
RESERVED	SPICLKB	47	67	ADCINC4	VfbRefCh2_Flt
AinEnableCh2_N	GPIO52	48	68	ADCINB4	VfbCh2_Flt
		49	69		AnalogDacCh2
		50	70	DACOUTB	AnalogDacCh1

表 5. TIDA-01633 J13 Interface to Launchpad J8, J6

TIDA-01633 FUNCTION	LAUNCHPAD FUNCTION USED	J8 PIN	J6 PIN	LAUNCHPAD FUNCTION USED	TIDA-01633 FUNCTION
		41	61	GND	GND
		42	62	SPISTEB_N	Reserved
		43	63	GPIO131	AoutModeCh2
		44	64	GPIO130	AoutModeCh1
		45	65		
PwmDacCh2	EPWM8A	46	66	SPISIMOB	Reserved
PwmDacCh1	EPWM8B	47	67	SPISOMIB	Reserved
		48	68	GPIO26	AinEnableCh1_N
		49	69	GPIO27	LoadFaultCh2
		50	70	GPIO25	LoadFaultCh1

For more information on C2000 launchpads go to: C2000 Tools and Software

For further technical support on C2000 go to e2e forum: https://e2e.ti.com/support/microcontrollers/c2000/

3.2 Testing and Results

The focus of the tests is to evaluate the functionality and performance of the XTR305 based analog output module. The accuracy of the circuit, diagnostic features, and EMC immunity performance are characterized.

3.2.1 Voltage Output Mode

The TIDA-01633 is configured in the voltage output mode. A ±15-V external supply powers the board. The control input voltage is provided by a source meter. A resistive load is connected on the voltage output. A multimeter connected in parallel to the load measures the output voltage.

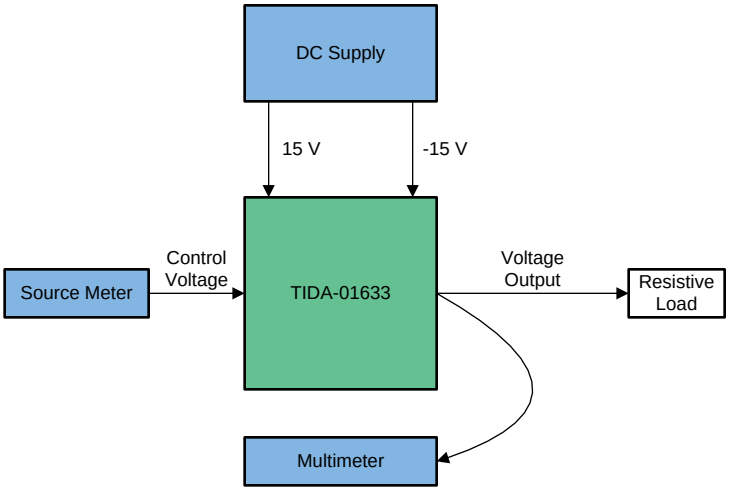


図 22. Test Setup for Voltage Output Mode

3.2.1.1 Transfer Function

A 0.4-V to 2.9-V input voltage (±1.25 V around 1.65-V reference) provides a –10-V to +10-V output voltage. The transfer functions for both analog output channels are plotted in 図 23.

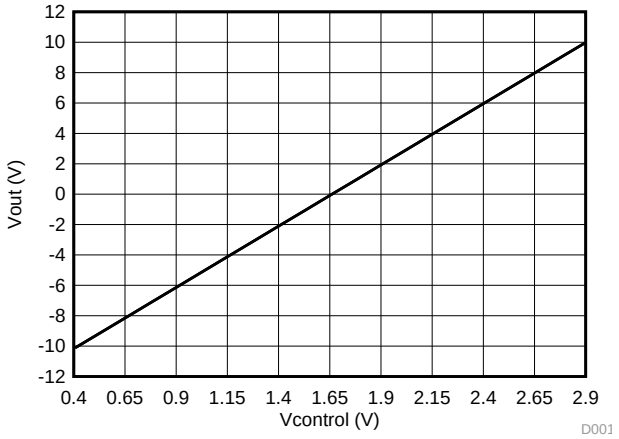


図 23. Voltage Output Transfer Function

3.2.1.2 Output Voltage Accuracy

The deviation from the expected output value is plotted for 10 kΩ, 1 kΩ and no load case for both channel 1 and 2 in 図 24.

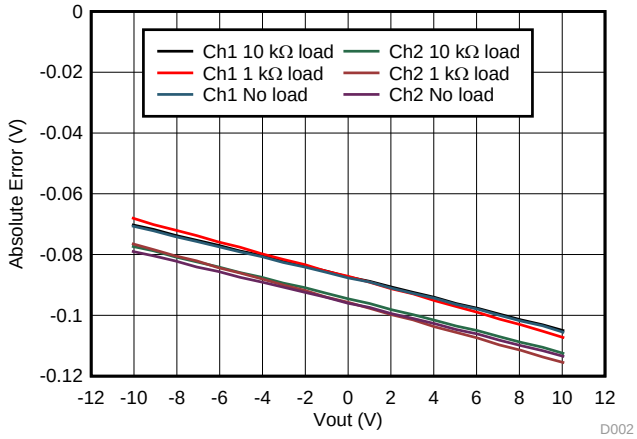


図 24. Uncalibrated Measurement Error vs Output Voltage at Different Loads

The values plotted in 図 24 are calibrated using a 2 point calibration method at 25°C with 10-kΩ load. Calibration eliminates the offset and gain errors. The same correction factors are applied for 1 kΩ load and no load. The calibrated results are plotted in 図 25.

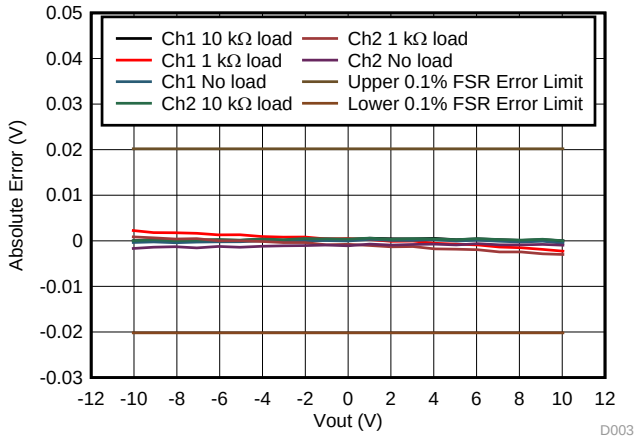


図 25. 2-Point Calibrated Measurement Error vs Output Voltage at Different Loads

The measurement error drift at different temperatures is plotted in 図 26. This measurement is done with a 10-kΩ load and the temperature is set at 0°C, 25°C, 55°C, and 85°C.

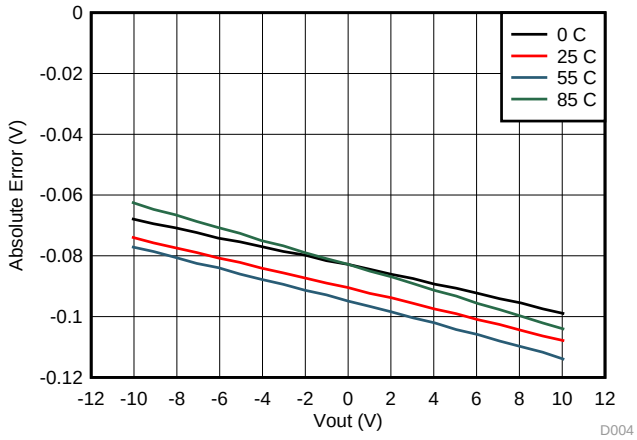


図 26. Measurement Error vs Output Voltage at Different Temperatures

The plots in 図 26 are 2-point calibrated at 25°C and the correction factor applied to all the temperatures. The result is shown in 図 27.

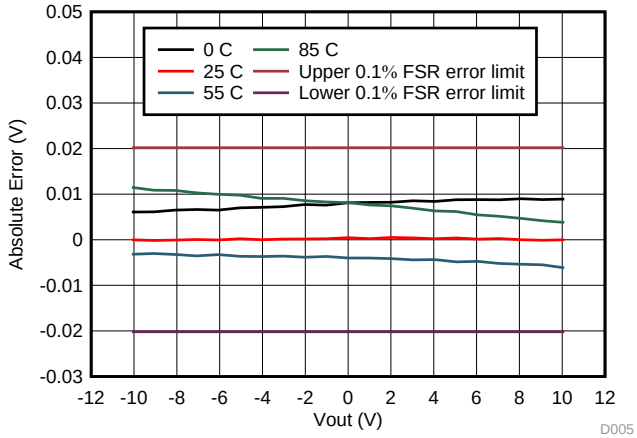


図 27. 2-Point Calibrated Measurement Error vs Output Voltage at Different Temperatures

3.2.1.3 Step Response

A small signal step of ±12 mV around 1.65 V is applied to the input of channel 1 using a function generator. The resulting small signal step response is plotted in 図 28. The rise and fall time is ~1 ms. The load used for this test is 10 kΩ.

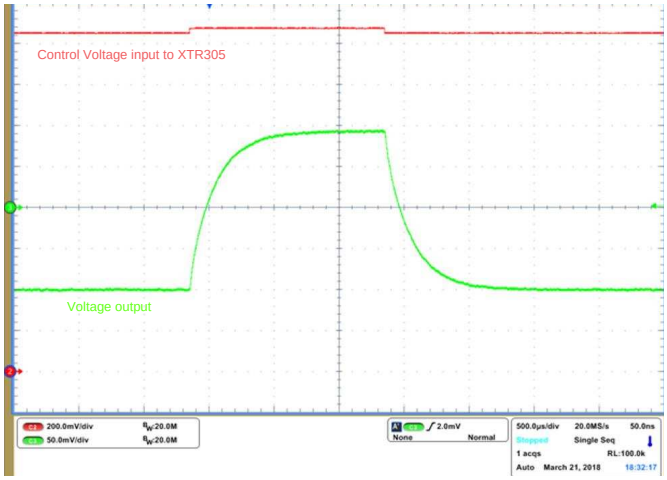


図 28. Small Signal Step Response

A 0.4-V to 2.9-V input step is applied to the input and the resulting ±10-V output step is plotted in 図 29.

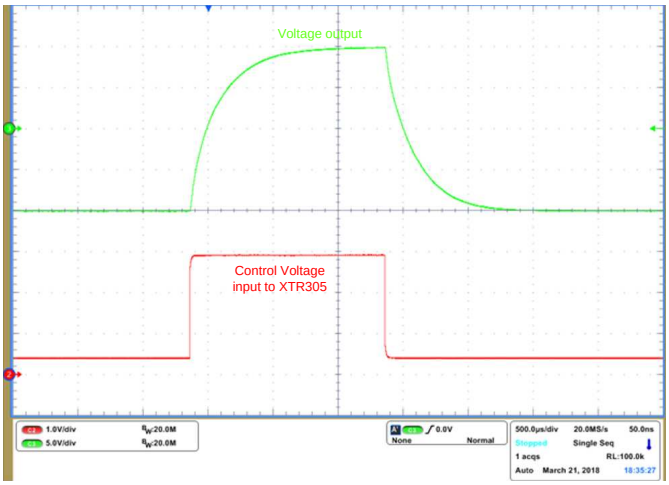


図 29. Large Signal Step Response

A 10-Hz sine input is applied at the input and the resulting output sine wave is plotted in 図 30. Both waveforms are AC coupled scope captures.

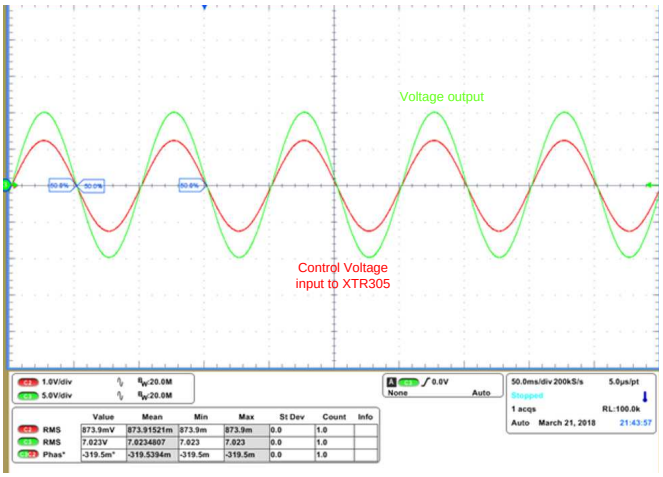


図 30. Input and Output Sine Voltages at 10 Hz

3.2.1.4 Bandwidth

The gain vs frequency plot for the voltage output was measured using a sine wave input of constant amplitude and varying frequency. The output voltage magnitude was measured with a multimeter. Values were plotted at 10, 100, 1000, 10 khz, and 100 khz. From 図 31, the bandwidth is ~800 Hz.

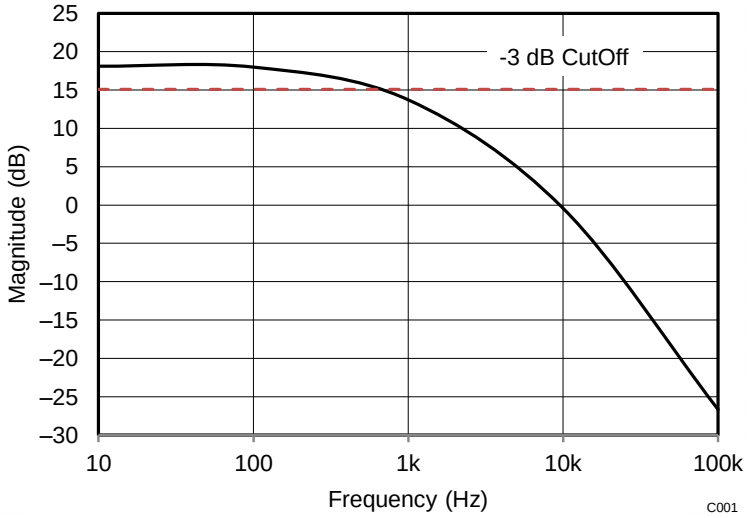


図 31. Bode Plot for Voltage Output

3.2.1.5 PWM Input Signal Control of Voltage Output

The voltage output can be controlled by a PWM input signal. For PWM control variant of TIDA-01633 and BOM changes refer schematic and CAD files. A 100-kHz PWM signal is used for testing the board. Changing the PWM duty cycle from 12.12% to 87.87% corresponds to full scale swing of the voltage output as shown in 図 32 to 図 34.

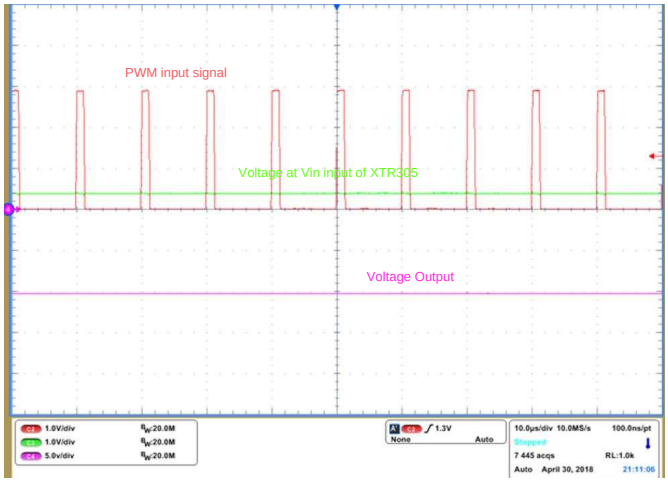


図 32. Voltage Output at 12.12% Duty Cycle

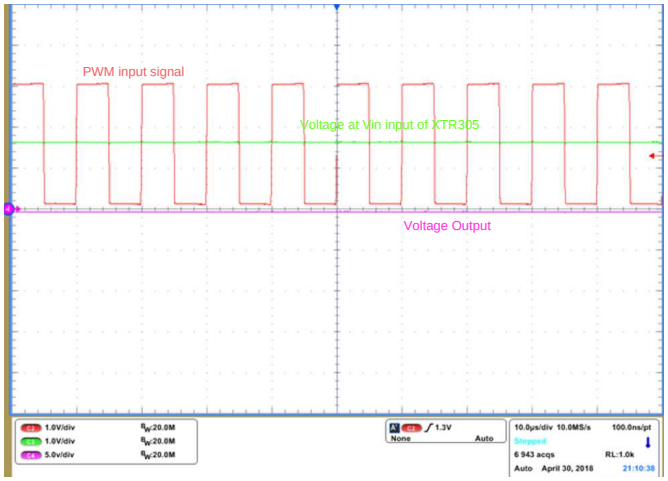


図 33. Voltage Output at 50% Duty Cycle

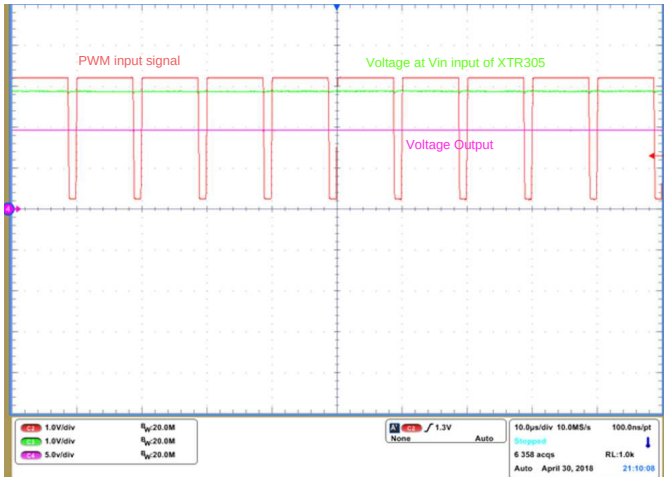


図 34. Voltage Output at 87.87% Duty Cycle

3.2.2 Current Output Mode

The TIDA-01633 is configured in the current output mode. A ±15-V supply powers the board. The control input voltage is provided by a source meter. A resistive load is connected on the voltage output. A multimeter connected in series with the load measures the output current.

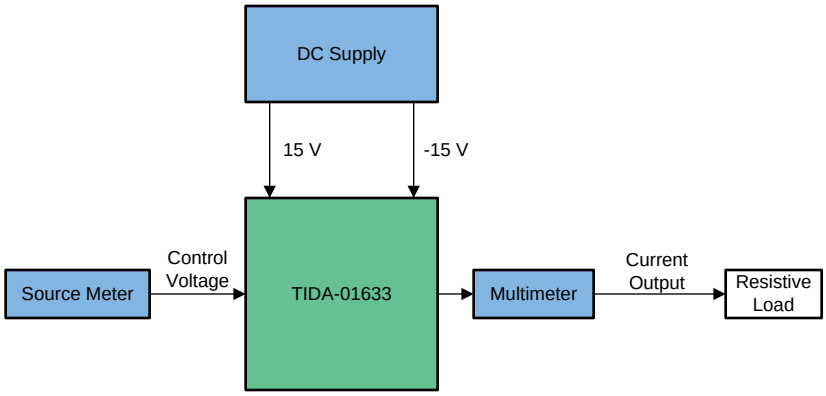


図 35. Test Setup for Current Output Mode

3.2.2.1 Transfer Function

A 0.4-V to 2.9-V input voltage (±1.25 V around 1.65-V reference) provides a –20 mA to +20-mA output current. The transfer functions for both analog output channels are plotted in 図 36

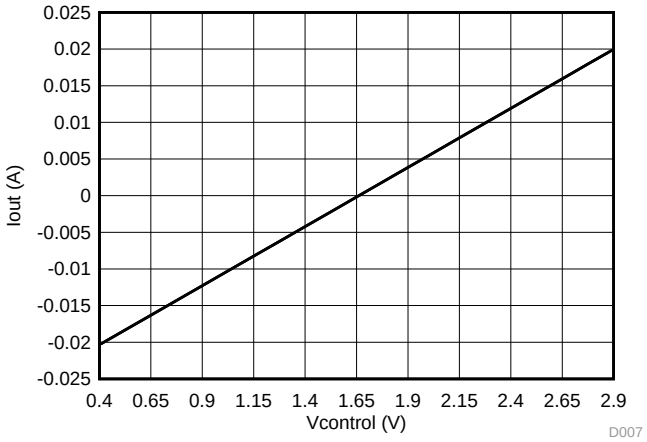


図 36. Current Output Transfer Function

3.2.2.2 Output Current Accuracy

The deviation from the expected output value is plotted for 250-Ω, 500-Ω and 100-Ω loads for both channel 1 and 2 in 図 37.

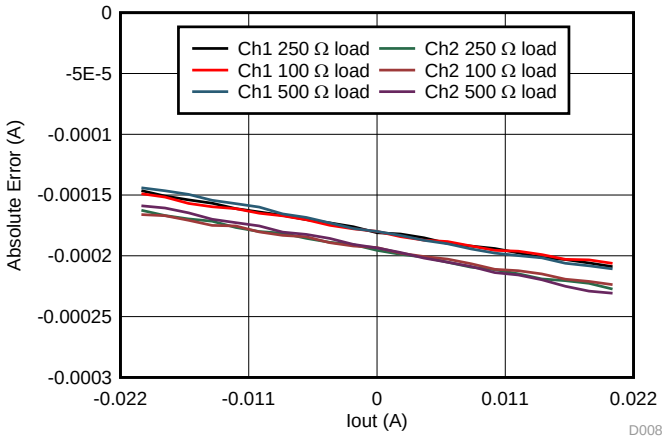


図 37. Uncalibrated Measurement Error vs Output Current at Different Loads

The values plotted in 図 37 are calibrated using a 2-point calibration method at 25°C with 250-Ω load. Calibration eliminates the offset and gain errors. The same correction factors are applied for 100-Ω load and 500-Ω load. The calibrated results are plotted in 図 38.

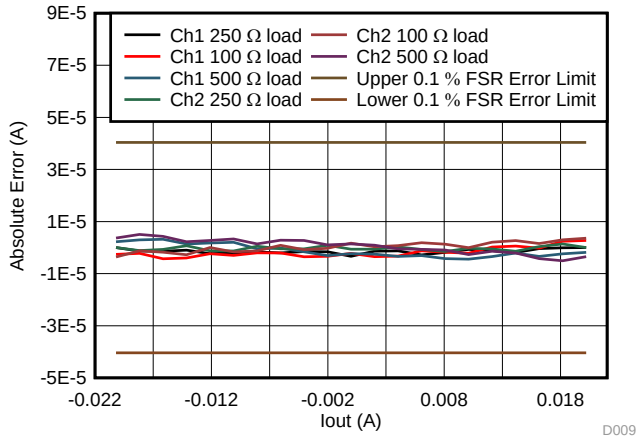


図 38. 2-Point Calibrated Measurement Error vs Output Current at Different Loads

The measurement error drift at different temperatures is plotted in 図 39. This measurement is done with a 250–Ω load and the temperature is set at 0°C, 25°C, 55°C, and 85°C.

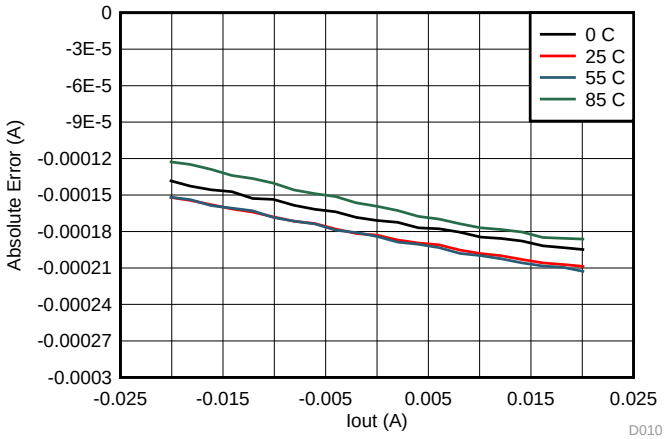


図 39. Measurement Error vs Output Current at Different Temperatures

The plots in 図 39 are 2-point calibrated at 25°C and the correction factor applied to all the temperatures. The result is shown in 図 40.

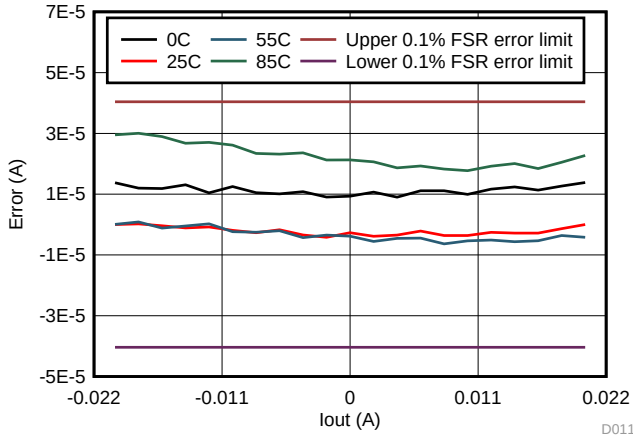


図 40. 2-Point Calibrated Measurement Error vs Output Current at Different Temperatures

3.2.2.3 Step Response

A small signal step of 0 mV to 20 mV is applied to the input of channel 1 using a function generator. The resulting small signal output step response of 0 µA to 320 µA is plotted in 図 41 (Note: The output current is measured across 250-Ω load, 0 mV to 80 mV corresponds to 0 µA to 320 µA). The rise and fall time is ~1 ms.

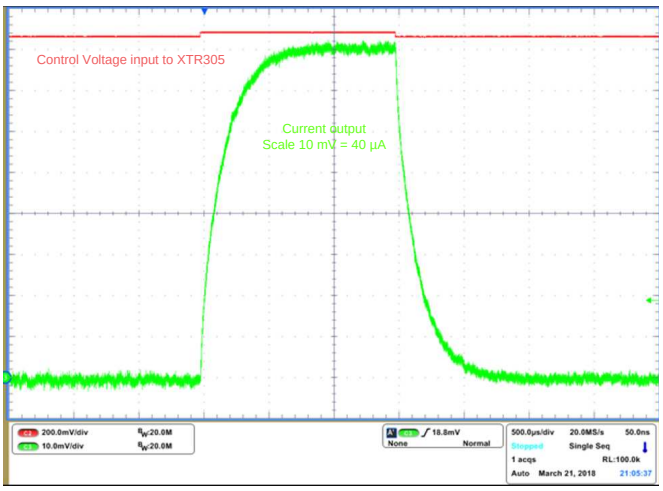


図 41. Small Signal Step Response

A 1.65-V to 2.9-V input step is applied to the input and the resulting 0-mA to 20-mA output step is plotted in 図 42.

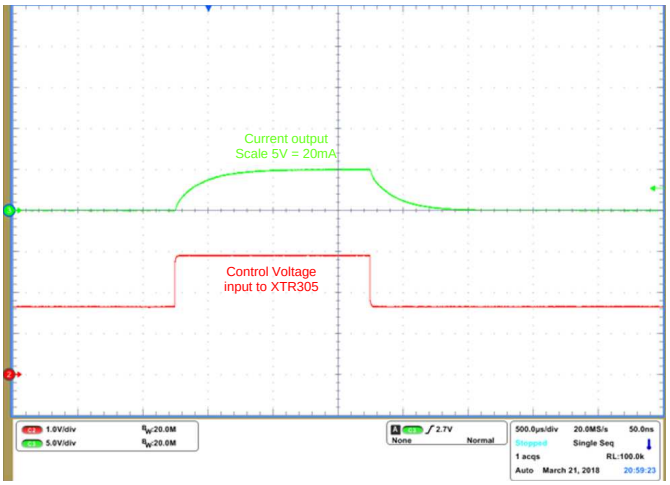


図 42. Large Signal Step Response

The 10-Hz sine signal is applied on the input and the resulting sine wave output is plotted in 図 43. Both waveforms are AC coupled scope captures.

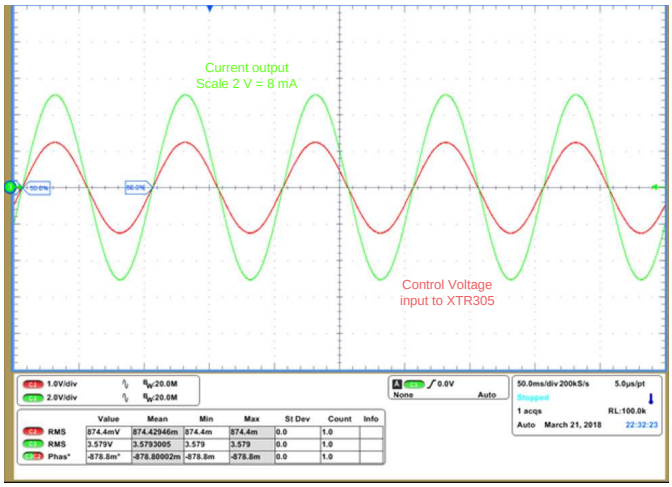


図 43. Input Sine Voltage and Output Sine Current at 10 Hz

3.2.2.4 Bandwidth

The gain vs frequency plot for the current output was measured using a sine wave input of constant amplitude and varying frequency. The output current magnitude was measured with a multimeter. Values were plotted at 10, 100, 1000, 10 khz and 100 khz. From the plot the bandwidth is ~800 Hz.

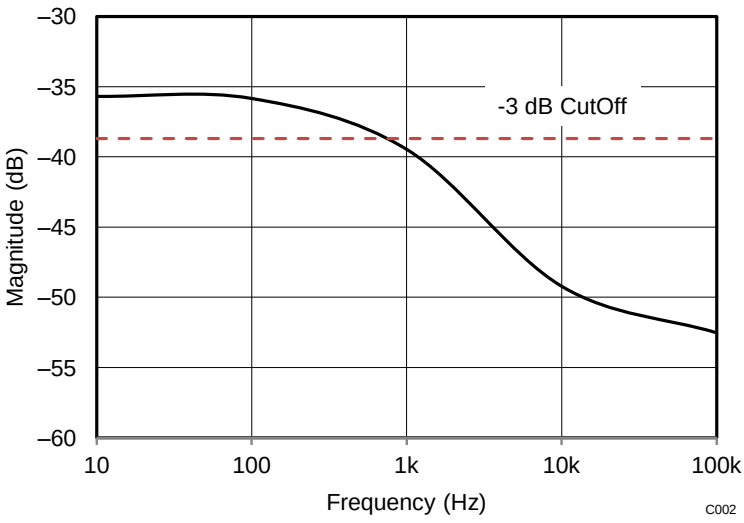


図 44. Bode Plot Current Output Mode

3.2.2.5 PWM Input Signal Control of Current Output

The current output can be controlled by a PWM input signal. For PWM control variant of TIDA-01633 and BOM changes see the schematic and CAD files. For testing the board a 100-kHz PWM signal is used. Changing the PWM duty cycle from 12.12% to 87.87% corresponds to full scale swing of the current output as shown in 図 45 to 図 47. The actual current polarity is inverse of the current polarity shown in the graphs as the current probe was connected in the reverse direction.

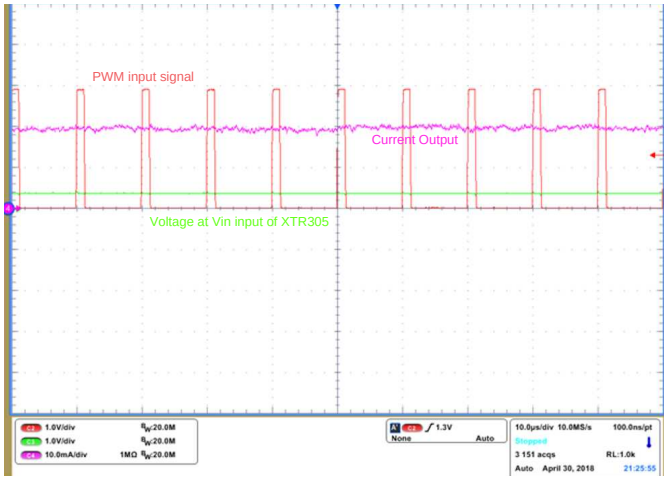


図 45. Current Output at 12.12% Duty Cycle

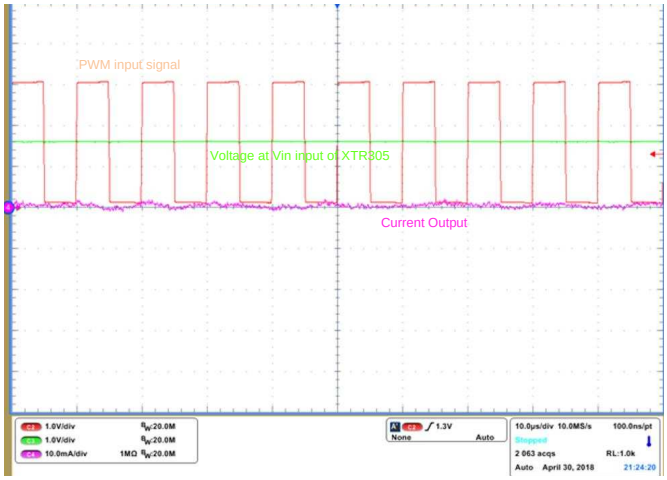


図 46. Current Output at 50% Duty Cycle

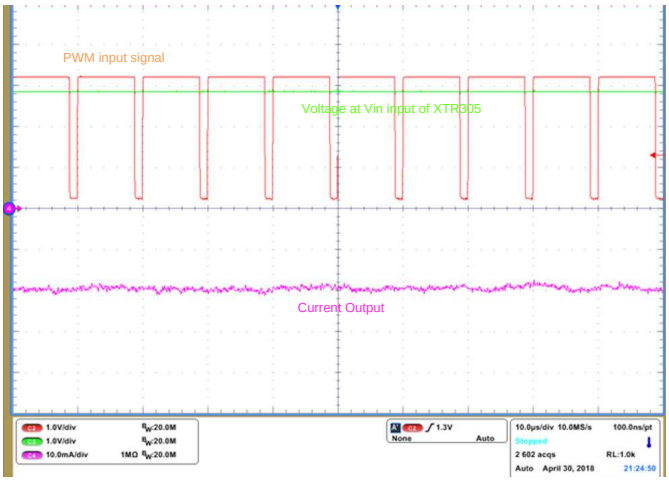


図 47. Current Output at 87.87% Duty Cycle

3.2.3 Output Protection

The XTR305 faulty load detection function is tested in *3.2.3* .

3.2.3.1 Short-Circuit Detection

During the voltage output mode if the output gets shorted because of a faulty load connected, the XTR305 limits the output current to 20 mA and pulls the load fault output flag low. The microcontroller can then take appropriate action based on the fault flag.

In 図 48 a 10-V output is connected to a 1-kΩ load which drives 10 mA into the load initially. The load is then shorted. When the short event occurs the XTR305 pulls down the output voltage to ~0 V and limits the output current to 20 mA. Simultaneously the load fault flag is pulled low.

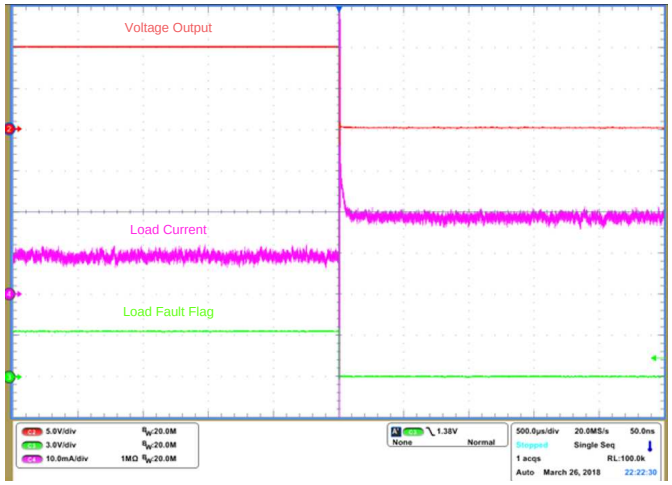


図 48. Load Short Detection - Initial Vout is +10 V

In 図 49 a –10-V output is connected to a 1-kΩ load with –10 mA driven into the load initially. In this case on load short the output current is limited to –20 mA.

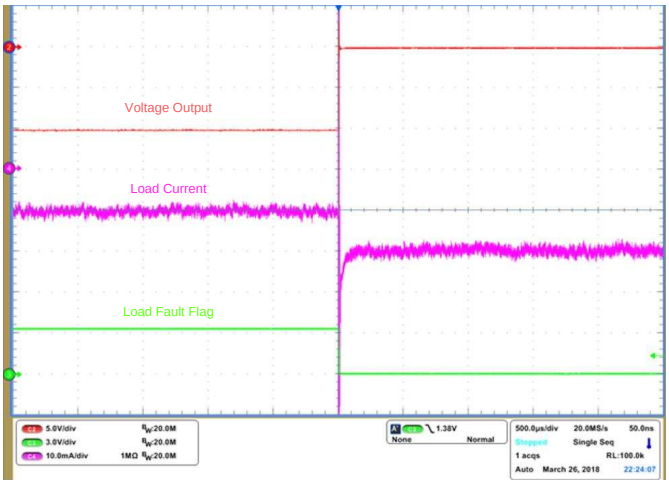


図 49. Load Short Detection - Initial Vout is –10 V

3.2.3.2 Open Load Detection

In the current output mode if the output opens due to faulty wiring, the XTR305 output rises to the compliance voltage limit and once this is reached it pulls the load fault output flag low. The controller can then take appropriate action based on the fault flag.

In 図 50 a 20-mA output is connected to a 250-Ω load which is suddenly opened. The output current becomes 0 immediately and the output voltage rises towards the positive rail. As soon as the compliance output voltage limit is reached the load fault flag is pulled low.

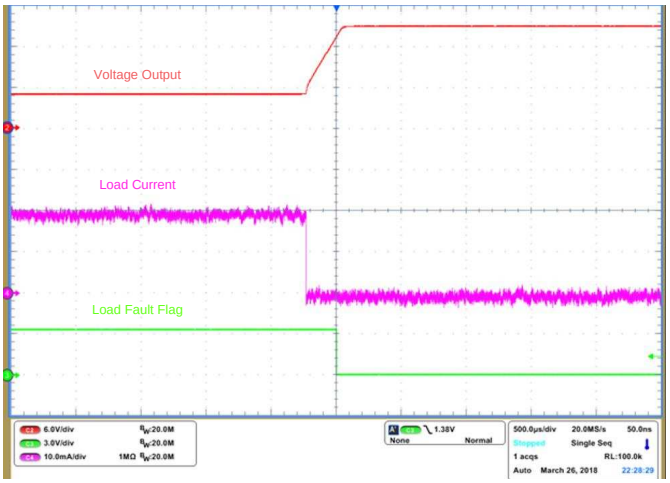


図 50. Open Load Fault Detection - Initial Iout is +20 mA

In 図 51 a –20-mA initial output current is driven into a 250-Ω load before the output open event. In this case the output voltage is driven towards the negative rail.

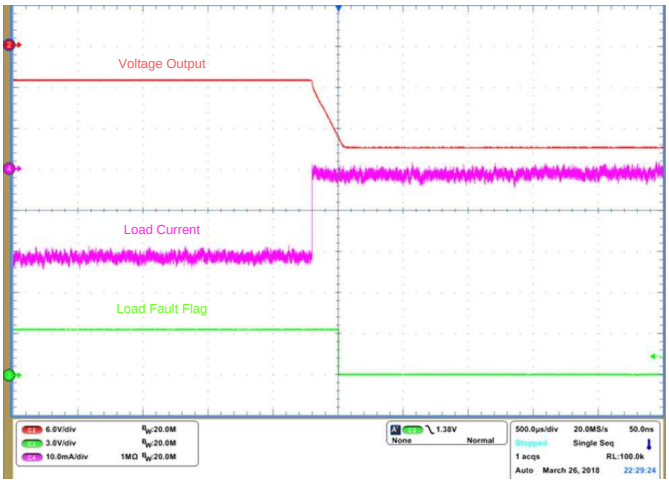


図 51. Open Load Fault Detection - Initial Iout is –20 mA

3.2.4 Analog Input

The TIDA-01633 can also be configured as an analog input. For testing this configuration a source meter is connected on the terminal connectors and a multimeter is connected on the analog feedback channels. The analog feedback channel is measured with respect to the 1.65-V reference.

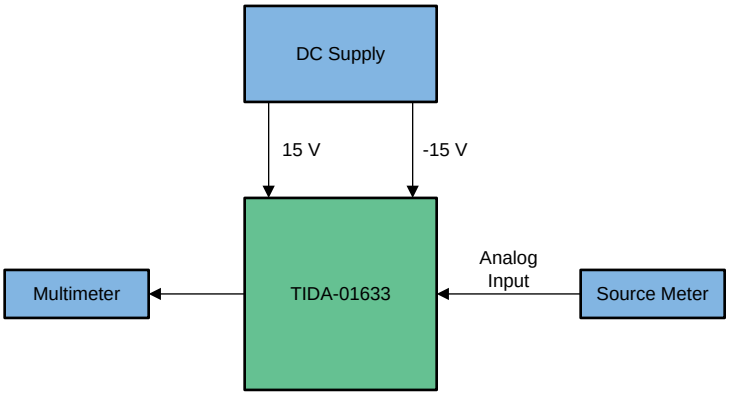


図 52. Test Setup for Analog Input Mode

3.2.4.1 Transfer Function

A –10-V to +10-V analog input voltage provides ±1.238 V across 1.65-V reference. The transfer function is plotted in 図 53.

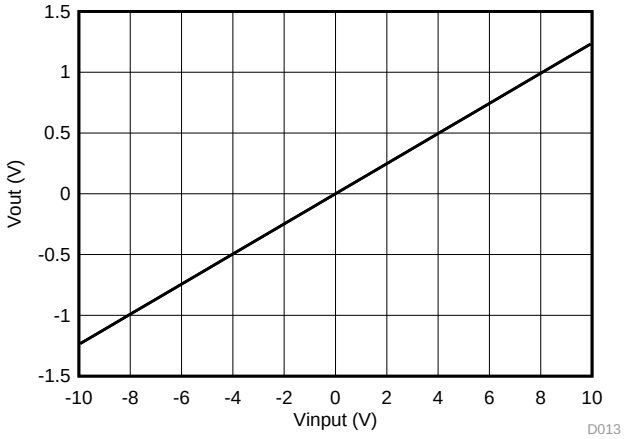


図 53. Analog Input Transfer Function

3.2.4.2 Analog Input Accuracy

The deviation from the expected measurement values is plotted in 図 54. An external burden resistor has to be used for using current as an analog input.

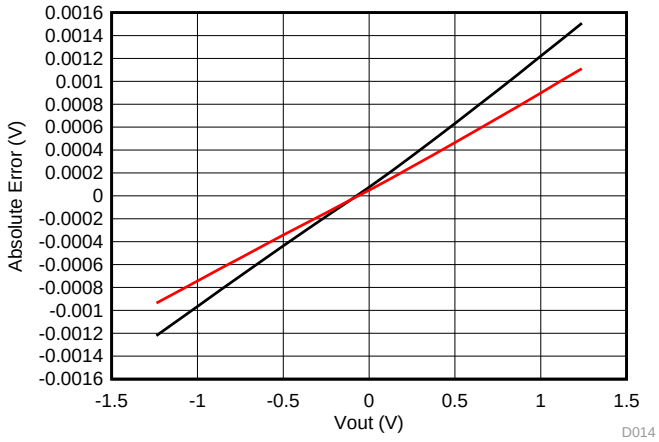


図 54. Uncalibrated Measurement Error vs Analog Input Voltage

The values plotted in 図 54 are calibrated using a 2-point calibration method. Calibration eliminates the offset and gain errors. The calibrated results are plotted in 図 55.

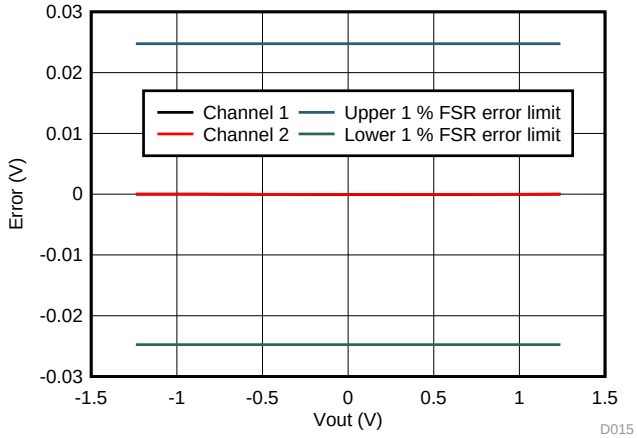


図 55. 2-Point Calibrated Measurement Error vs Analog Input Voltage

3.2.4.3 Step Response

A small signal step of –100 mV to +100 mV is applied using a function generator. The resulting small signal step response is plotted in 図 56.

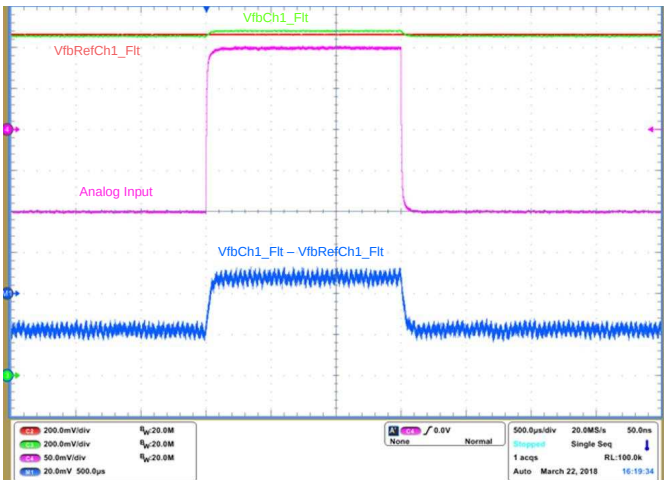


図 56. Small Signal Step Response

A –10-V to +10-V input step is applied and the resulting large signal step response is plotted in 図 57.

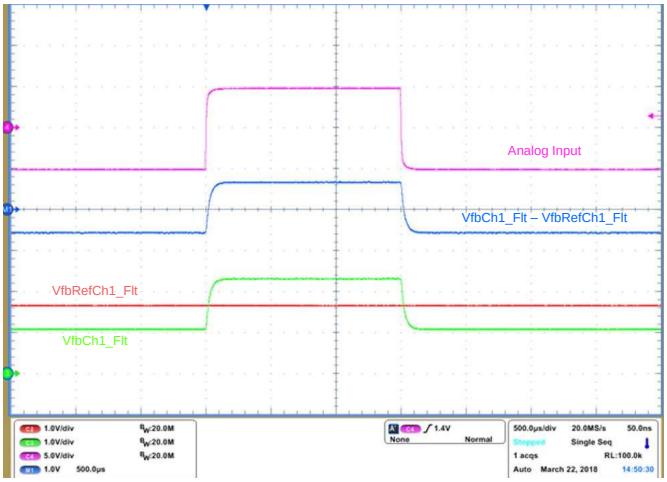


図 57. Large Signal Step Response

The sine analog input (10 Hz) and its response is plotted in 図 58.

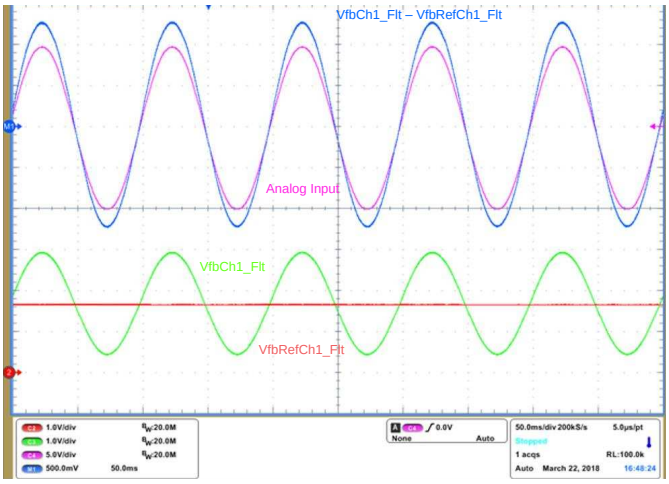


図 58. Sine Input and Output at 10 Hz

3.2.5 EMC Immunity Tests

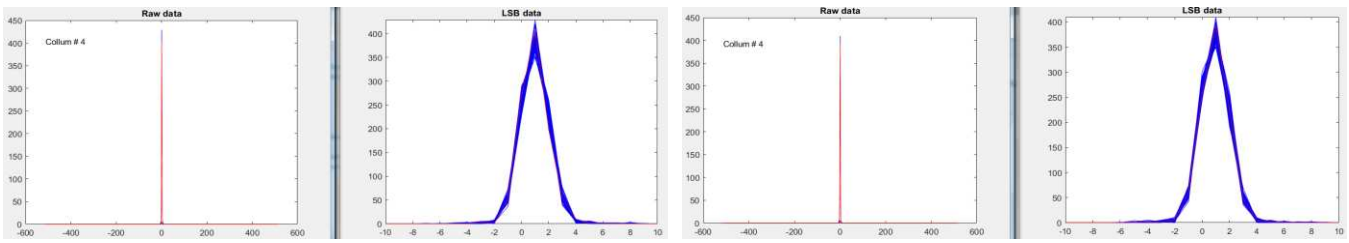
The TIDA-01633 has been tested as per IEC61000-4-2, IEC61000-4-4 and IEC61000-4-5 (ESD, EFT and Surge) with the test levels and performance criterion specified in the standard IEC61800-3: *EMC Immunity Requirements and Specific Test Method Applicable in Adjustable Speed, Electrical Power Drive Systems*.

The performance criterion is defined in 表 2

General Test procedure:

- Set up the EMC test equipment and EUT as shown in corresponding section for each of the tests
- Measure histogram before EMC test
- Apply transient noise and measure histogram during the test
- Compare both the histograms to determine the test class

Capturing Histograms: The analog output is monitored using the analog feedback channel. For channel 1 the analog feedback channel comprises of the signals VfbCh1 and VfbRefCh1. VfbRefCh1 is the 1.65-V reference and VfbCh1 is proportional to the analog output. Both of these signals are connected to simultaneous sampling channels of ADC. The difference (VfbCh1 - VfbRefCh1) is then stored in memory. For creating the histogram sampling is done at 1 ksps for 2 minutes. For each sample the error from the initial reference measurement is calculated and sorted into LSB bins. This is now plotted in a graph with the LSB bins on the X-axis and the number of samples with error falling into LSB bins plotted on the Y-axis. The EMC transients have to be applied within this 2-minute interval. An example histogram for voltage output before EMC and during EMC is shown in 図 59.



Histogram for Voltage output without any transient Noise

Histogram for Voltage output measured during +1 kV Surge

図 59. Histogram Before EMC Transients and During EMC Transient

The performance criterion A is often customer specific and the expected accuracy is depending system requirements. In TIDA-01633 the performance criterion is class A if the measurement accuracy remains within the maximum worst case 0.2% FSR accuracy range. The EMC test results are summarized in 表 6.

表 6. IEC61800-3 EMC Immunity Requirements

IEC61800-3 EMC IMMUNITY REQUIREMENTS FOR SECOND ENVIRONMENT AND MEASURED VOLTAGE LEVELS AND CLASS					TIDA-01633 MEASUREMENTS (STANDARD TEST VOLTAGE LEVELS)			TIDA-01633 MEASUREMENTS (EXTENDED TEST VOLTAGE LEVELS)	
PORT	**PHENOMENON**	**BASIC STANDARD**	**LEVEL**	**PERFORMANCE CRITERION**	**LEVEL**	**PERFORMANCE CRITERION**	**TEST**	**LEVEL**	**PERFORMANCE CRITERION**
Enclosure Ports	ESD	IEC61000-4-2	±4 kV CD	B	±4 kV CD	A	Pass	±8 kV CD	B
Ports for control lines and DC auxiliary supplies (<60 V)	Fast transient burst (EFT)	IEC61000-4-4	±2 kV/5 khz capacitive clamp	B	±2 kV	A	Pass	±4 kV	B
	Surge 1.2/50 us, 8/20 us	IEC61000-4-5	±1 kV; because shielded cable >20 m direct coupling to shield (2 Ω/500 A)	B	±1 kV	A	Pass	±2 kV	A

3.2.5.1 ESD Test Results

図 60 shows the test setup for ESD immunity testing and 図 61 shows the lab setup. The TIDA-01633 is mounted onto the LAUNCHXL-F28379D and placed on an insulation sheet which is kept on the table reference. The table reference is connected to the ground reference through two 470-kΩ resistors in series. The ESD gun is referenced to the ground reference. ESD strikes are applied on the TIDA-01633 Earth connector pin which is connected to the shield of the cable as shown in 図 63. The shield of the cable is connected to ground reference. 10 pulses with positive polarity with 1-s interval between pulses is applied for each test followed by 10 pulses with negative polarity.

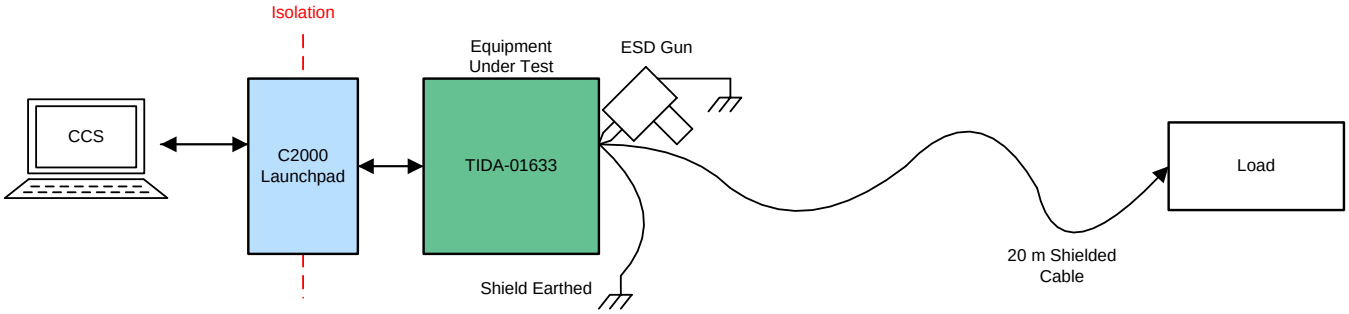


図 60. ESD Test Setup Diagram

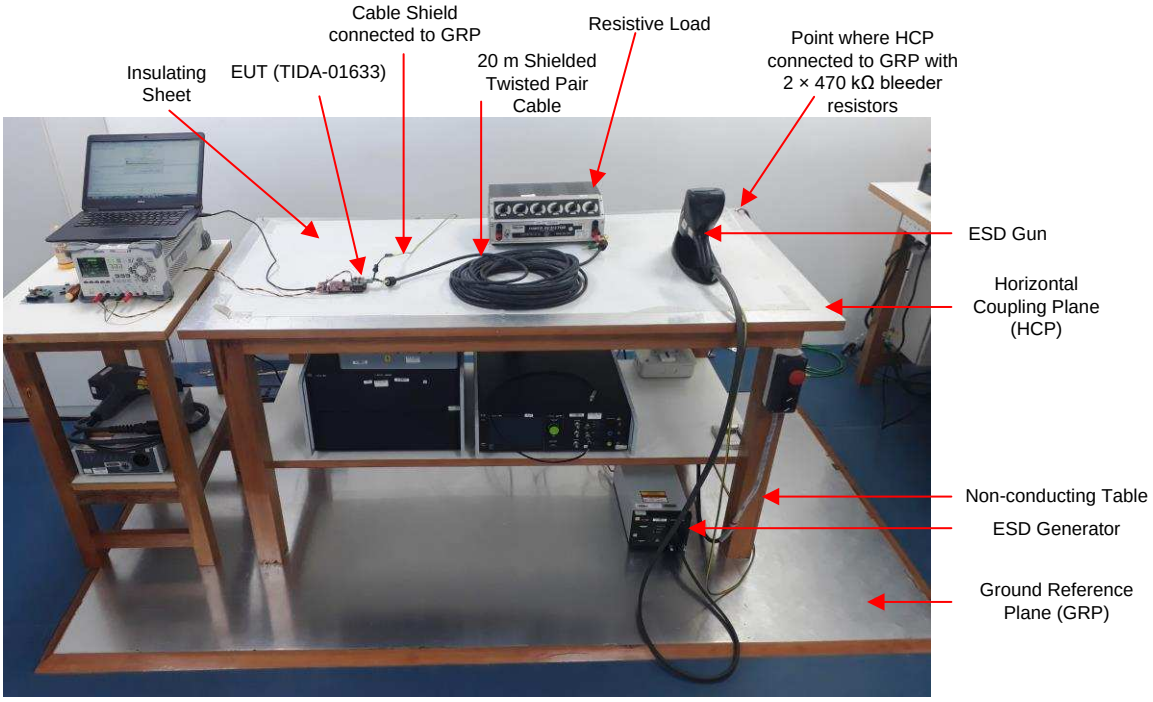


図 61. Lab Test Setup

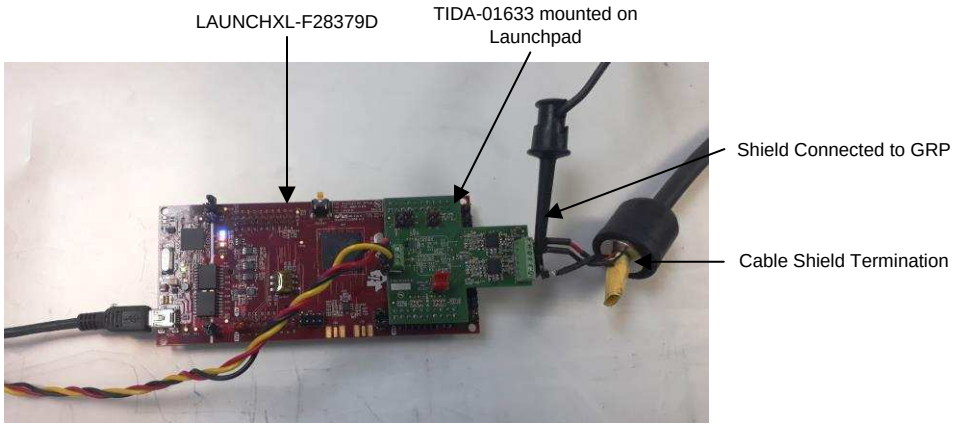


図 62. EUT (TIDA-01633) Connections

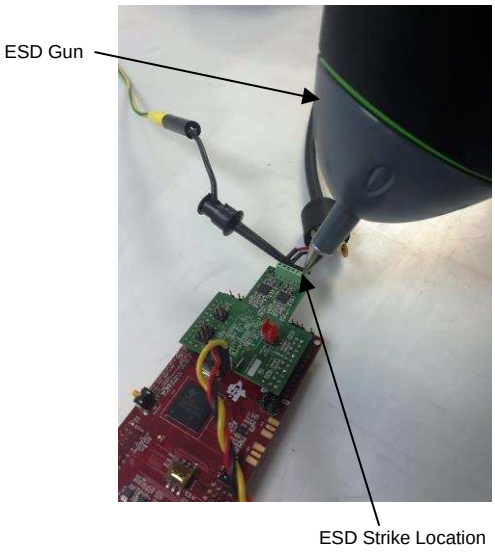


図 63. ESD Strike Location

表 7. ESD Test Results

ESD PULSES	PERFORMANCE ACHIEVED	
	VOLTAGE OUTPUT	CURRENT OUTPUT
+4 kV	Class A	Class A
–4 kV	Class A	Class A
+6 kV	Class A	Class B
–6 kV	Class A	Class A
+8 kV	Class A	Class B
–8 kV	Class A	Class B

3.2.5.2 EFT

The TIDA-01633 is connected to a resistive load through a 20-m shielded twisted pair cable. EFT is coupled into this cable through a capacitive clamp as shown in 図 65. For the EFT test the table reference and the ground reference are shorted to each other.

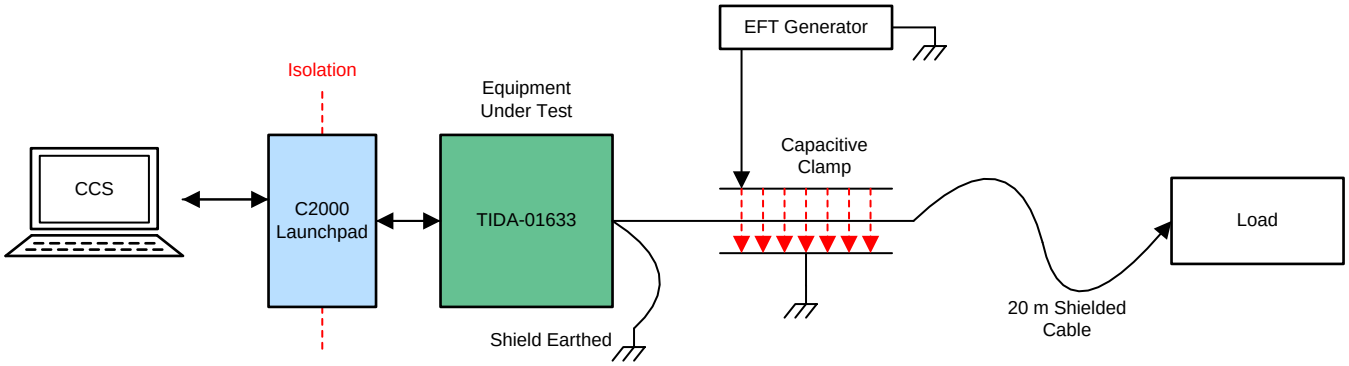


図 64. EFT Test Setup Diagram

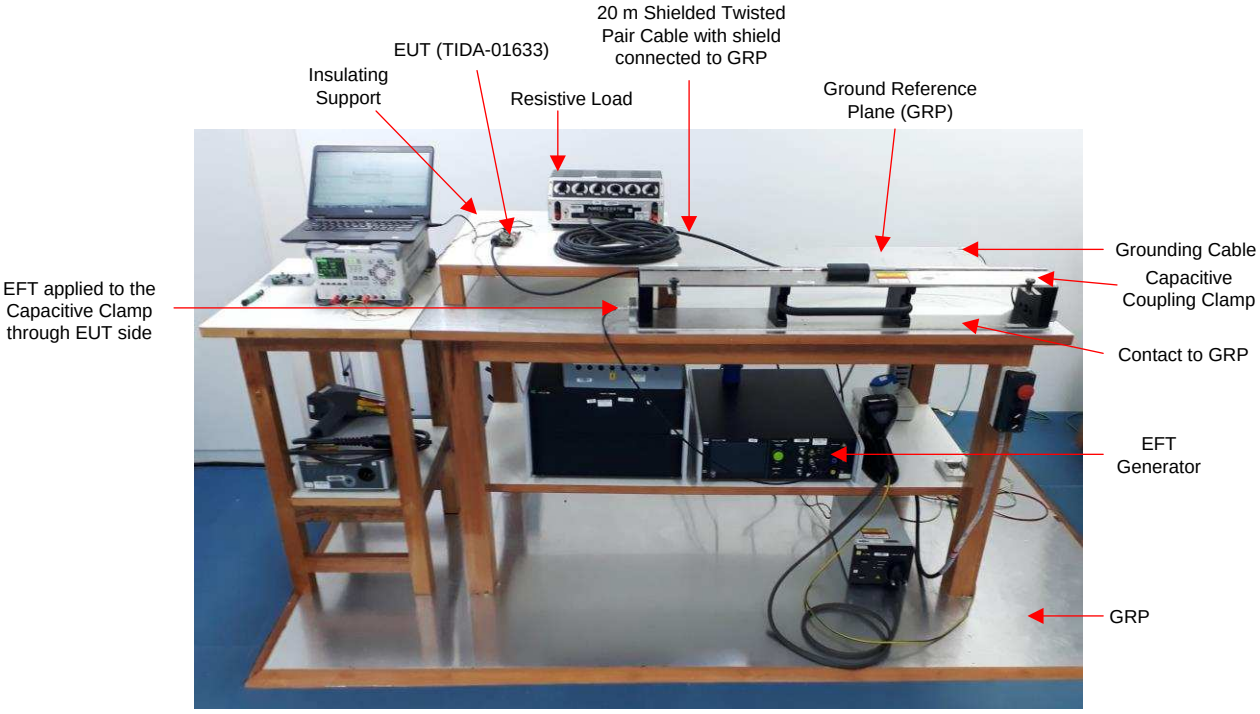


図 65. Lab EFT Test Setup

表 8. EFT Test Results

EFT PULSES	PERFORMANCE ACHIEVED	
	VOLTAGE OUTPUT	CURRENT OUTPUT
+2 kV	Class A	Class A
–2 kV	Class A	Class A
+4 kV	Class B	Class B
–4 kV	Class B	Class B

3.2.5.3 Surge

For surge testing the surge is directly inserted into the shield of the cable at the EUT end.

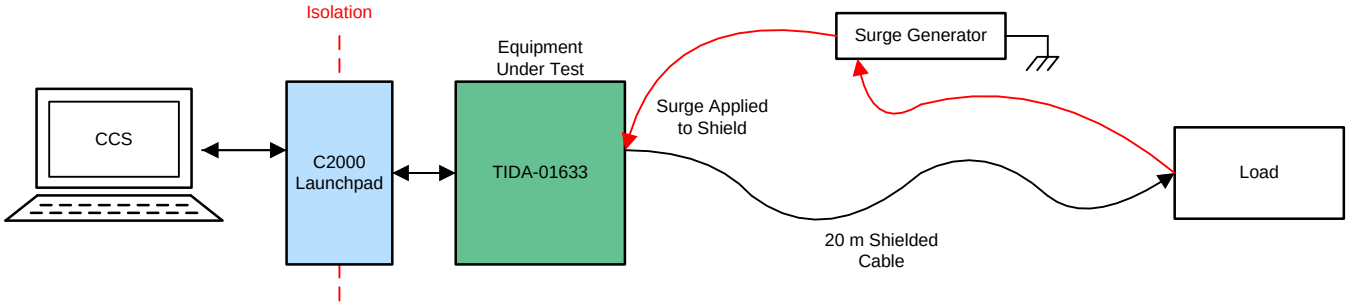


図 66. Surge Test Setup Diagram

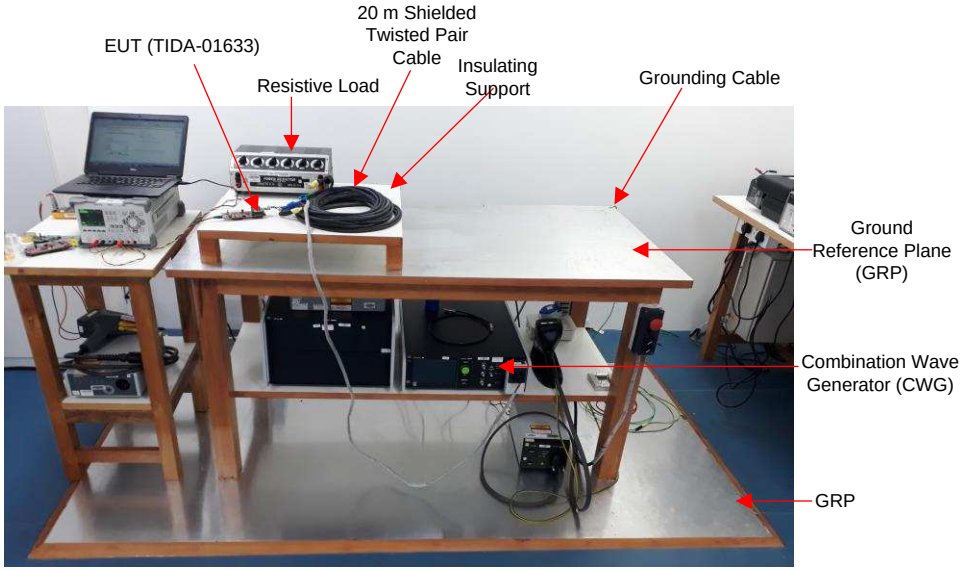


図 67. Lab Surge Test Setup

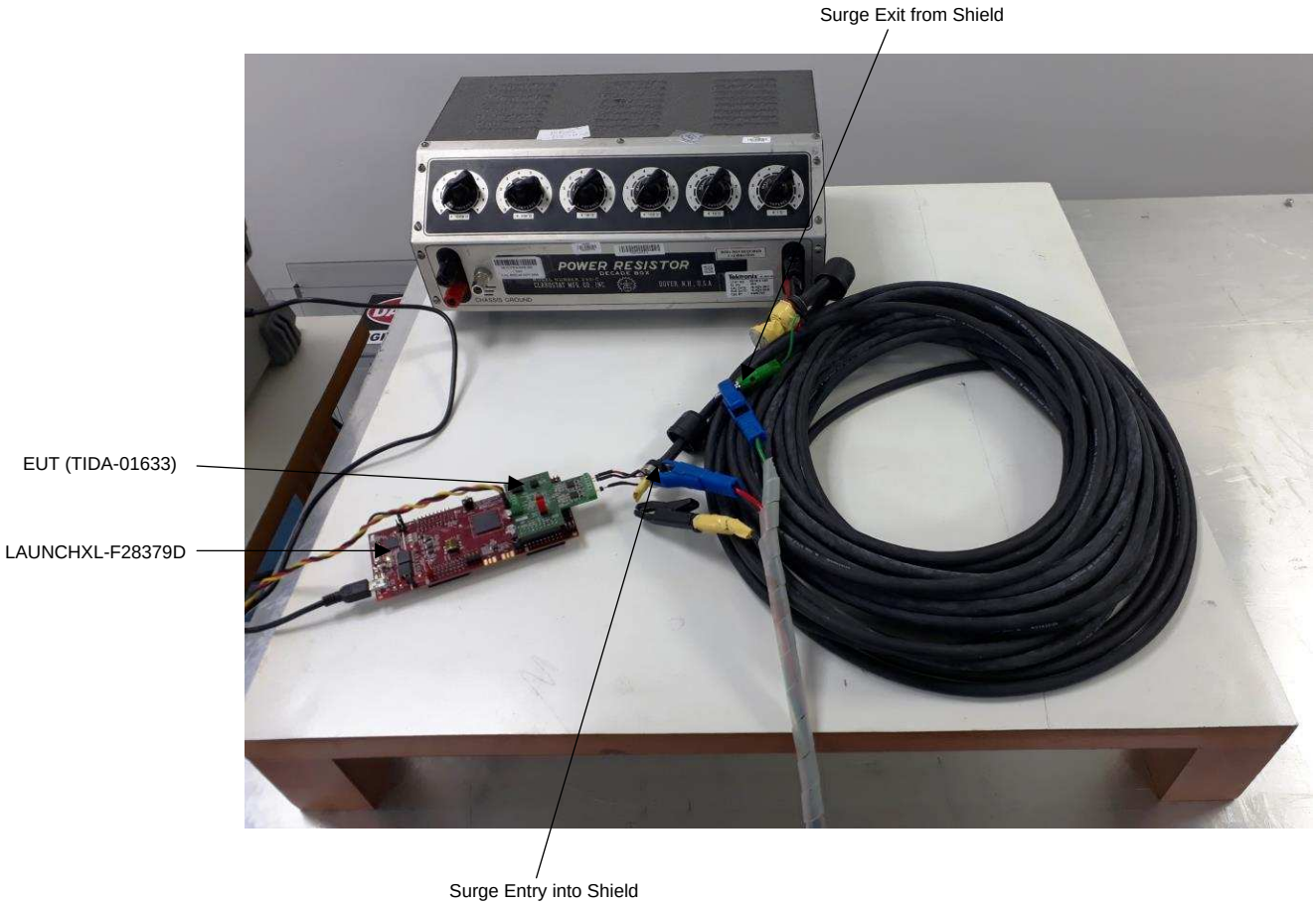


図 68. Surge Application Into Shield

表 9. Surge Test Results

SURGE	PERFORMANCE ACHIEVED	
	VOLTAGE OUTPUT	CURRENT OUTPUT
+1 kV	Class A	Class A
–1 kV	Class A	Class A
+2 kV	Class A	Class A
–2 kV	Class A	Class A

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01633.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01633.

4.3 PCB Layout Recommendations

4.3.1 XTR305

- Place supply bypass capacitors C2, C3 close to device supply pins
- R5, C1, R3 and C6 are placed at the input of the OPA inside XTR305. The trace length should be minimized to avoid noise coupling into the input
- R6, R9, C8 and R10 are placed at the input of the IA inside XTR305. Trace lengths should be minimized to avoid noise coupling
- The instrumentation amplifier ground connection from R9 resistor must be at the connector pins
- The power pad of the XTR305 is connected to the internal ground planes through multiple vias for good thermal performance

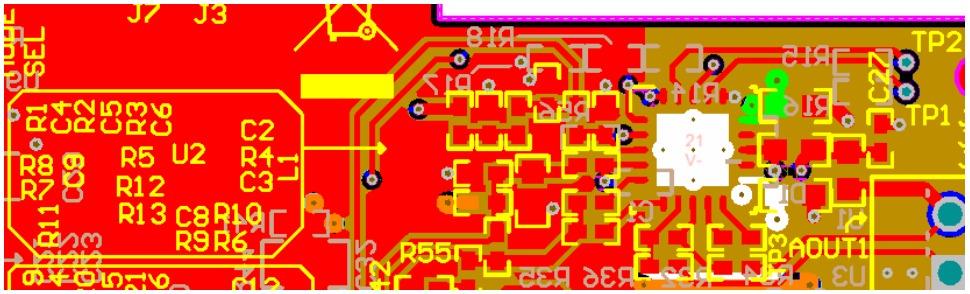


図 69. XTR305 Layout guidelines

4.3.2 TVS1400

- The small form factor of the TVS1400 device enables placement below the connector close to the terminal pins when compared to standard SMA and SMB packages
- Close placement with short traces shunts the transient noise right at the connector without coupling into other net connections

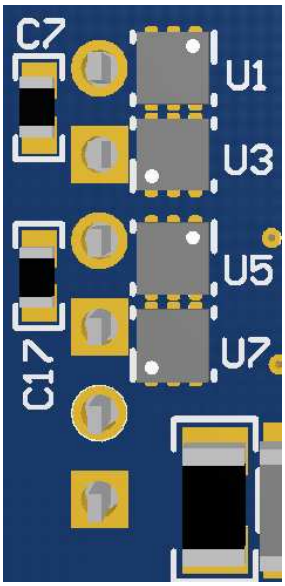


図 70. Placement of TVS1400

4.3.3 Layout Prints

To download the layer plots, see the design files at TIDA-01633.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-01633.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01633.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01633.

5 Related Documentation

1. Texas Instruments, *Single-Channel Industrial Voltage and Current Output Driver, Isolated, EMC/EMI Tested*
2. Texas Instruments, *LAUNCHXL-F28379D OVerview User's Guide*
3. IEC61800-3 Edition 2.0 (2004-08) Adjustable Speed Electrical Power Drive Systems - Part 3: *EMC Requirements and Specific Test Methods*
4. IEC61000-4-2 Edition 2.0 (2008-12) Electromagnetic compatibility (EMC) - Part 4-2 : *Testing and Measurement Techniques - Electrostatic Discharge Immunity Test*
5. IEC61000-4-4 Edition 3.0 (2012-04) Electromagnetic compatibility (EMC) - Part 4-4 : *Testing and Measurement Techniques - Electrical Fast Transient/burst Immunity Test*
6. IEC61000-4-5 Edition 3.0 (2014-05) Electromagnetic compatibility (EMC) - Part 4-5 : *Testing and Measurement Techniques - Surge Immunity Test*

5.1 Trademarks

6 About the Author

Pawan Nayak is a System Engineer at Texas Instruments, where he is responsible for developing reference design solutions for the Motor Drive segment within Industrial Systems.

Martin Staebler is a System Architect in the Industrial Systems Motor Drive team at Texas Instruments, responsible for specifying and developing reference designs for industrial drives.

6.1 Recognition

The author would like to recognize excellent contributions from **Kristen Mogensen** during the test of the design.

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お客様は、自らのアプリケーションの設計において、ご自身が独自に分析、評価、判断を行う責任がお客様にあり、お客様のアプリケーション(および、お客様のアプリケーションに使用されるすべてのTI製品)の安全性、および該当するすべての規制、法、その他適用される要件への遵守を保証するすべての責任をお客様のみが負うことを理解し、合意するものとします。お客様は、自身のアプリケーションに関して、(1) 故障による危険な結果を予測し、(2) 障害とその結果を監視し、および、(3) 損害を引き起こす障害の可能性を減らし、適切な対策を行う目的での、安全策を開発し実装するために必要な、すべての技術を保持していることを表明するものとします。お客様は、TI製品を含むアプリケーションを使用または配布する前に、それらのアプリケーション、およびアプリケーションに使用されているTI製品の機能性を完全にテストすることに合意するものとします。TIは、特定のTIリソース用に発行されたドキュメントで明示的に記載されているもの以外のテストを実行していません。

お客様は、個別のTIリソースにつき、当該TIリソースに記載されているTI製品を含むアプリケーションの開発に関連する目的でのみ、使用、コピー、変更することが許可されています。明示的または黙示的を問わず、禁反言の法理その他どのような理由でも、他のTIの知的所有権に対するその他のライセンスは付与されません。また、TIまたは他のいかなる第三者のテクノロジまたは知的所有権についても、いかなるライセンスも付与されるものではありません。付与されないものには、TI製品またはサービスが使用される組み合わせ、機械、プロセスに関連する特許権、著作権、回路配置利用権、その他の知的所有権が含まれますが、これらに限られません。第三者の製品やサービスに関する、またはそれらを参照する情報は、そのような製品またはサービスを利用するライセンスを構成するものではなく、それらに対する保証または推奨を意味するものでもありません。TIリソースを使用するため、第三者の特許または他の知的所有権に基づく第三者からのライセンス、もしくは、TIの特許または他の知的所有権に基づくTIからのライセンスが必要な場合があります。

TIのリソースは、それに含まれるあらゆる欠陥も含めて、「現状のまま」提供されます。TIは、TIリソースまたはその仕様に関して、明示的か暗黙的かにかかわらず、他のいかなる保証または表明も行いません。これには、正確性または完全性、権原、続発性の障害に関する保証、および商品性、特定目的への適合性、第三者の知的所有権の非侵害に対する黙示の保証が含まれますが、これらに限られません。

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お客様は、この注意事項の条件および条項に従わなかったために発生した、いかなる損害、コスト、損失、責任からも、TIおよびその代表者を完全に免責するものとします。

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