参考資料

TI Designs: TIDA-050014
パワーDUOシンク、200W USB-C PDのリファレンス・デザイン

概要

このUSB電力供給(PD)のリファレンス・デザインは、動作に100W以上を必要とするシステムをユーザーが実装するためのもので、同時に業界で最も低いRDS_{on}のソリューションも示しています。このデザインは、4つの標準ソース電圧(5V、9V、15V、20V)をすべてシンクできます。標準のType-C PD動作で、最大20V/5Aまでシンク可能です。テキサス・インスツルメンツのパワーPower DUO代替モードで動作しているとき、このデザインは最大20V/10Aを出力でき、同時にRDS_{on}を1/2に減らすことができます。

リソース

TIDA-050012	デザイン・フォルダ
TIDA-050014	デザイン・フォルダ
TPS65987D	プロダクト・フォルダ
TPS768	プロダクト・フォルダ
TPD2E009	プロダクト・フォルダ

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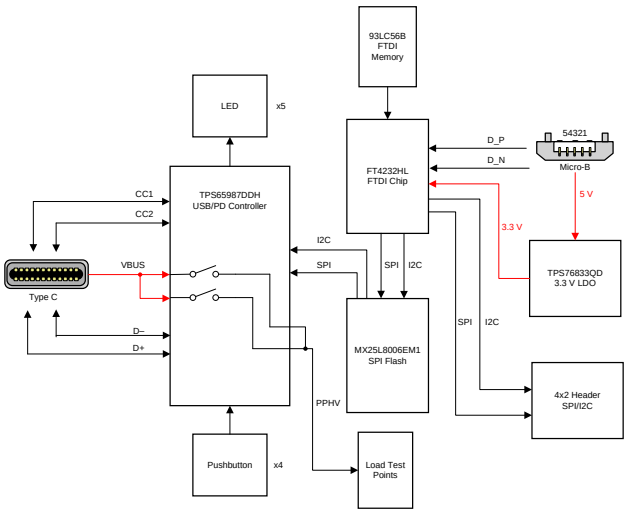
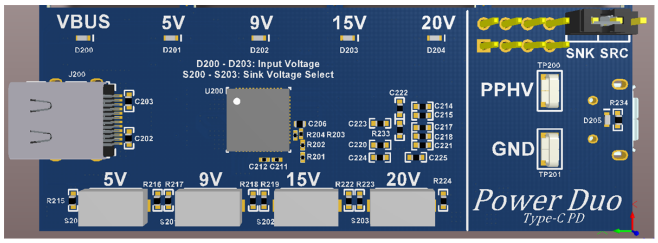
- システム負荷をシミュレートするためのテスト・ポイント
- プログラミングおよび構成用のFTDI

アプリケーション

- ノートブックおよびラップトップ
- パーソナル・エレクトロニクス
- 高電圧のパワー・バンク
- PDコントローラの統合電源パス





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1 System Description

This design highlights how to implement a high power USB Type-C PD sink device. This design can be referenced for various different end equipments, from Notebooks, TV's and monitors, power banks, and any other system that sinks power from a source charger. Through the use of a Texas Instruments USB PD Alternate Mode, the TPS65987D PD adapter will close both of it's load switches in parallel to double the current carrying capability and reduce the effective RDS_{on} by a factor of two. The design also highlights a feature of the TPS65987D called App Config by allowing users to select their Type-C PD input voltage through push button switches.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Input Power Source	20 V USB Type-C PD (200 W recommended for full feature use)
System Quescent Current	3.4 mA
Typical Load Switch RDS_{on}	29 mOhm
Power DUO Alternate Mode RDS_{on}	14.5 mOhm

2 System Overview

2.1 Block Diagram

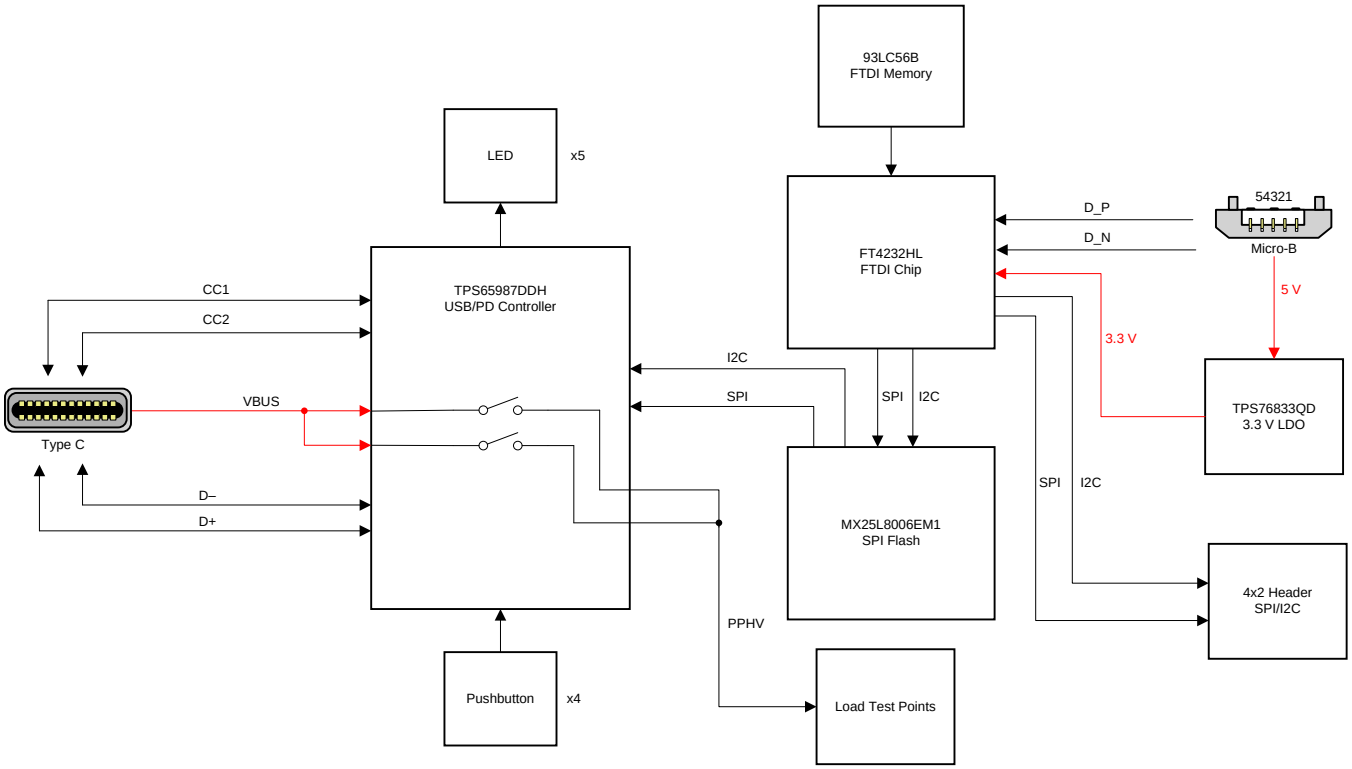

図 1. TIDA-050014 Block Diagram

2.2 Design Considerations

TIDA-050014 gives an example of how to implement a USB Type-C PD system that is capable of handling high current. This design can be used in monitors, dongles, power banks, and any other system that would benefit from having more than 100 W of power sourced to it. If the end user will exceed 5 A of current, it is recommended to use a tethered cable instead of a Type-C receptacle. This would allow the user to develop their own high current cable and not be limited by the cables and connectors in the design.

2.3 Highlighted Products

2.3.1 TPS65987D

The TPS65987D is a stand-alone USB Type-C and Power Delivery (PD) controller providing cable plug and orientation detection for a single USB Type-C connector. Upon cable detection, the TPS65987D communicates on the CC wire using the USB PD protocol. When cable detection and USB PD negotiation are complete, the TPS65987D enables the appropriate power path and configures alternate mode settings for external multiplexers.

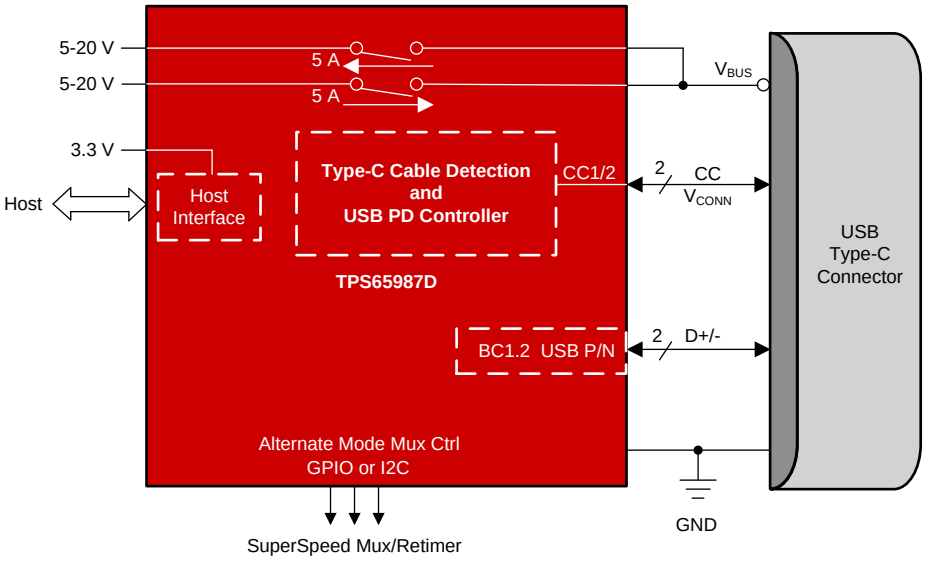

図 2. TPS65987D Simplified Schematic

2.3.2 TPS768xx

This device is designed to have a fast transient response and be stable with 10 mF capacitors. This combination provides high performance at a reasonable cost.

Since the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 230 mV at an output current of 1 A for the TPS76850) and is directly proportional to the output current. Additionally, because the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 85 mA over the full range of output current, 0 mA to 1 A). These two key specifications yield a significant improvement in operating life for battery-powered systems. This LDO family also features a shutdown mode; applying a TTL high signal to EN (enable) shuts down the regulator, reducing the quiescent current to less than 1 mA at T_J = 25°C.

Power good (PG) is an active high output, which can be used to implement a power-on reset or a low-battery indicator.

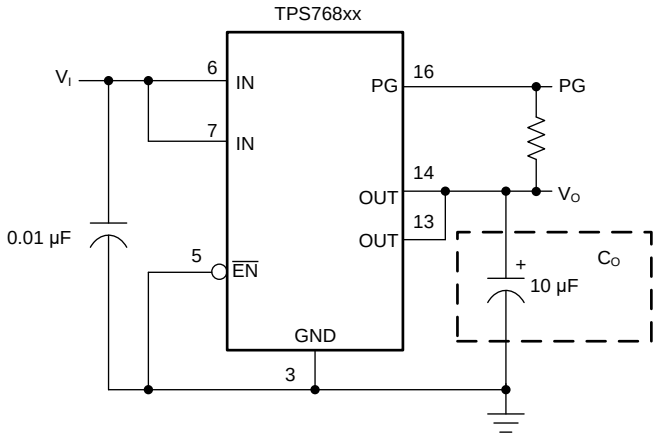

図 3. TPS768xx Simplified Schematic

2.3.3 TPD2E009

The TPD2E009 device provides two ESD protection diodes with flow-through pin mapping for ease of board layout. This device has been designed to protect sensitive components which are connected to ultra high-speed data and transmission lines. The TPD2E009 offers transient voltage suppression for Level 4 of IEC 61000-4-2 Contact ESD protection. TVS protection up to a 5-A (8/20 μs) peak pulse-current rating per the IEC 61000-4-5 (lightning) specification is also provided.

The monolithic silicon technology allows matching between the differential signal pairs. The less than 0.05-pF differential capacitance ensures that the differential signal distortion due to added ESD circuit protection remains minimal. The low capacitance (0.7-pF) is suitable for high-speed data rates up to 6 Gbps.

Typical applications for the TPD2E009 line of ESD protection products are: HDMI, USB, eSATA, and ethernet interfaces in notebooks, DVD and media players, set-top boxes, and portable computers.

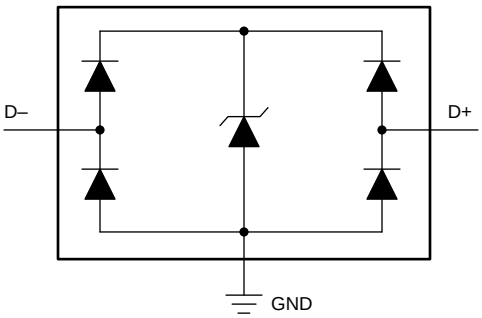

図 4. TPD2E009 Simplified Schematic

2.4 System Design Theory

2.4.1 TPS65987D PD Controller

The TPS65987D has two internal power paths that are capable of handling 5 A each. This design is intended to allow for loads larger than 5 A to be applied, which is why the two power paths are connected to one another. VBUS_SINK is connected to the Type-C connector, while PP_HV_Sink is connected to what would be the system load.

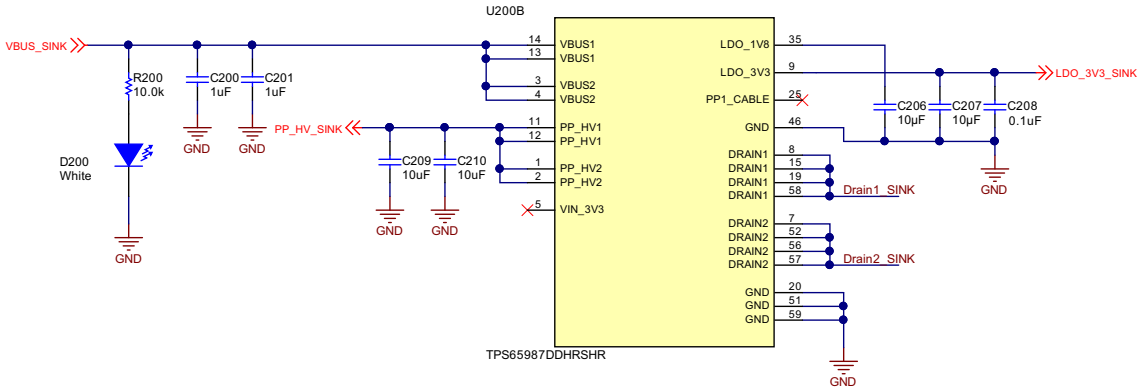

図 5. TPS65987D Power Path

A total of eight GPIO's are used from the TPS65987D. Four are connected to an external FET, and the other three are connected to pushbuttons. Their intended use case and functionality are explained within 2.4.3. The TPS65987D has the ability to change its corresponding I2C address and start function via an external resistor divider network connected to ADCIN1 and ADCIN2. In this resistor divider configuration, the TPS65987D will have an I2C address of 1 with a BP_NoWait boot mode.

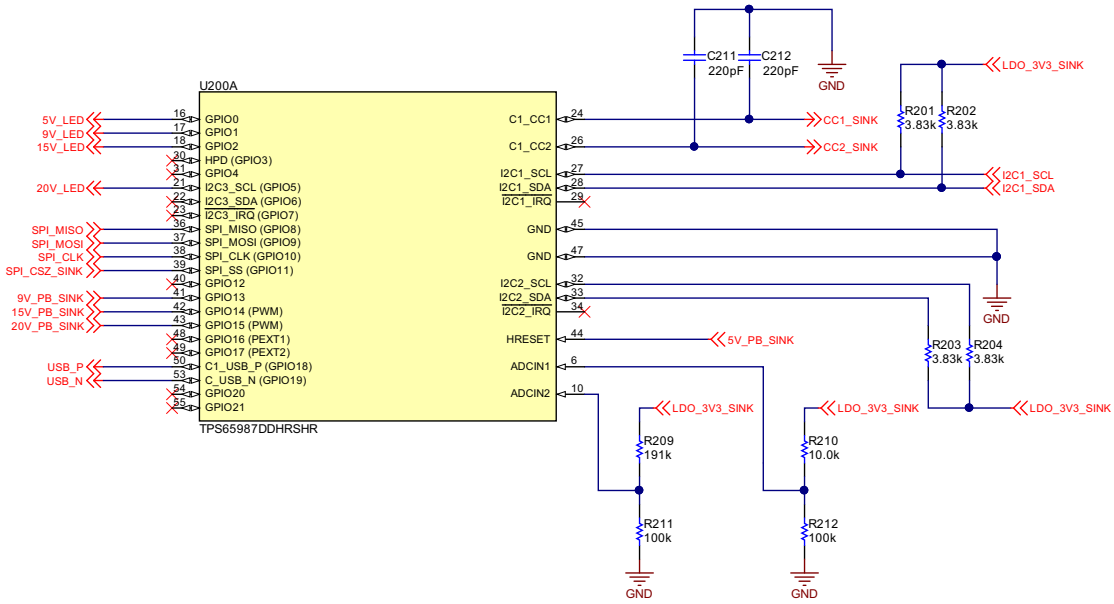

図 6. TPS65987D USB PD Controller Schematic

An external SPI-Flash is used for holding the application that is written onto the board from the app confugration tool. Upon booting, the TPS65987D will read back the application code from the SPI-Flash. The SPI-Flash is only accessed upon initial boot up and power on reset events.

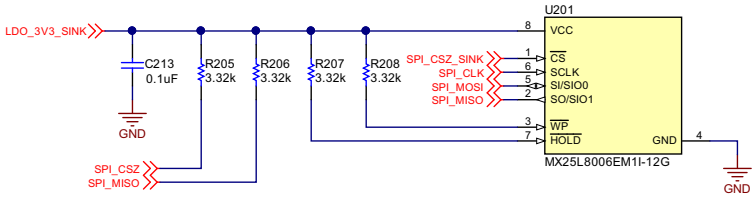

図 7. SPI Flash Schematic

2.4.2 FTDI

Located on the TIDA-050014 is the FT4232HL, which is an FTDI chip. This allows for the board to be programmed by a Type-B cable connected to a laptop, as the FT4232HL is able to convert the DP/DM data lines from a USB cable to SPI and I2C. The I2C lines from the FT4232HL go straight to the TPS65987D, while the SPI connections go to both the TPS65987D as well as the SPI flash. The FT4232HL needs an external source of memory, which is what the 93LC56B is used for.

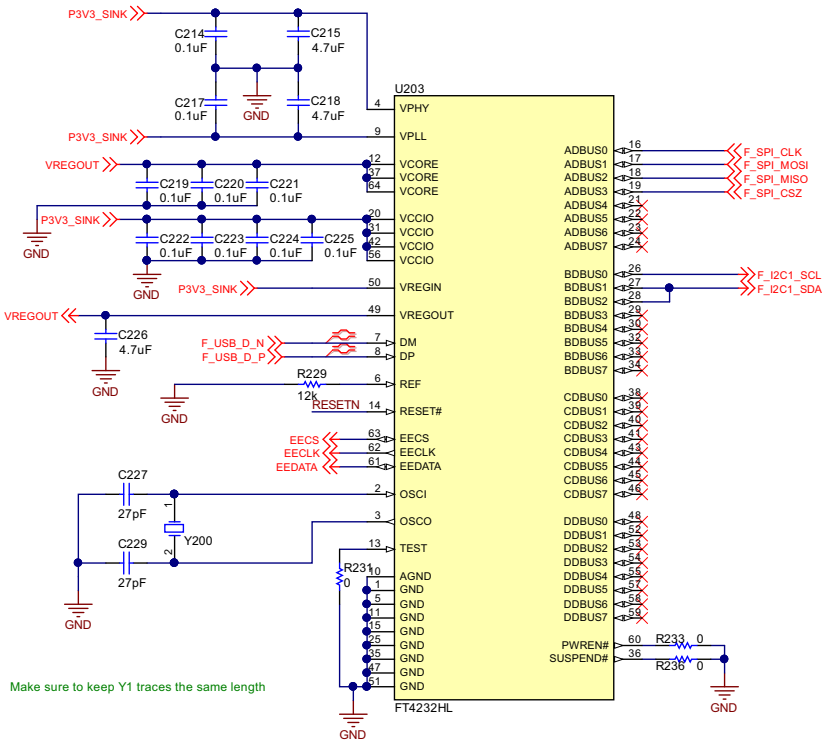

図 8. FTDI Chip Schematic FT4232HL

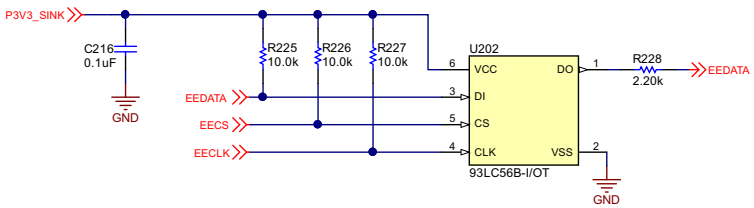

図 9. FTDI Memory Schematic 93LC56B

The USB Type-B cable will supply 5 V to the TIDA-050014 via VBUS. The TPS76833QD is used to regulate the 5 V from VBUs to 3.3 V, which is then used to power the FTDI.

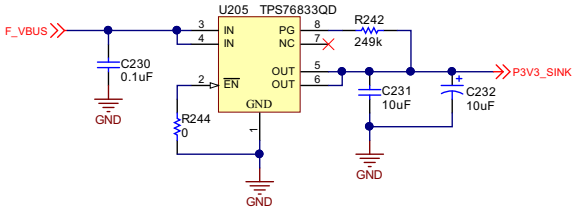

図 10. LDO Schematic TPS76833QD

2.4.3 Buttons and LEDs

TIDA-050014 is designed to request four different PDO's depending on what the customer is wanting to test. 9V_PB_SINK, 15V_PB_SINK, and 20V_PB_SINK are connected to three individual GPIO pins on the TPS65987D. 5V_PB_SINK will be connected to HRESET. When the push buttons are not pressed, each of the GPIO's will be pulled low. Upon initial startup, each GPIO will be pulled low and the TPS65987D will go in its default state of requesting 5 V. When a push button is pressed, its corresponding GPIO will be pulled high, and then that sink voltage will be requested by the TPS65987D.

For example, a USB Type-C PD source controller, capable of supplying up to 20 V, is connected to the TIDA-050014. The TIDA-050014 will go into its default state, and request 5 V from the source controller. If the user wants the sink voltage to change to 20 V, they would then press the pushbutton labeled "20 V". This will pull 20V_PB_SINK and it's corresponding GPIO high. The TPS65987D would then request a 20 V PDO from the source controller, and the voltage on VBUS would then rise to 20 V. If they wish to return back to 5 V, press the button labeled "5 V". This will pull 5V_PB_SINK and HRESET high, and the TPD65987D will reset. When the TPS65987D comes back on, it will then request it's default voltage of 5 V.

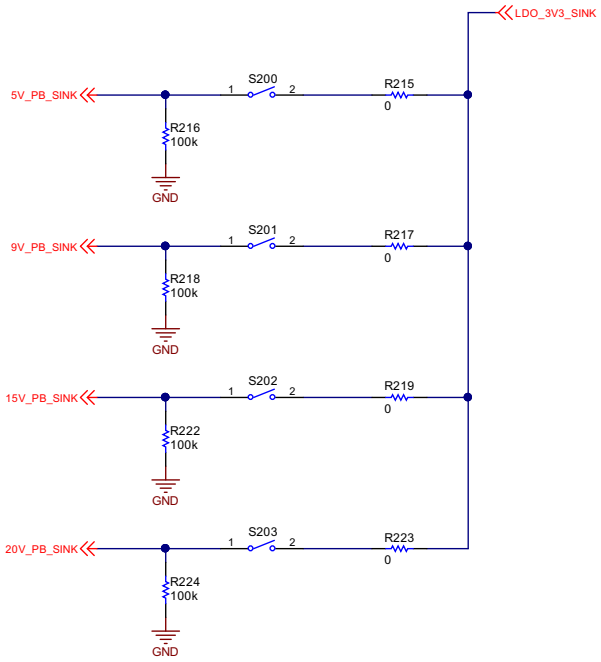

図 11. Push Buttons

5V_LED, 9V_LED, 15V_LED, and 20V_LED are all connected to their own individual GPIO from the TPS65987D. These LED's signify what the TPS65987D is currently sinking from the source PD controller. For example, if 20 V is negotiated between the sink and the source PD controllers and applied on VBUS, the GPIO connected to the 20 V LED will drive the gat on the BSS138W high, allowing for current to flow turning on the LED.

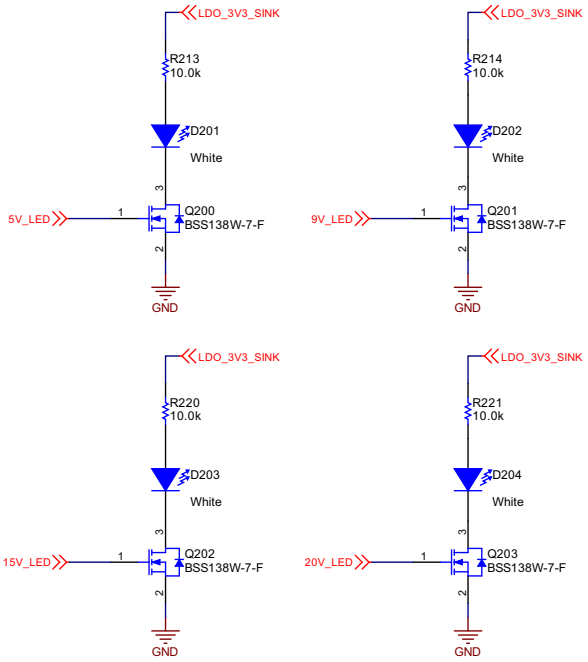

図 12. Voltage LEDs

2.4.4 Hardware

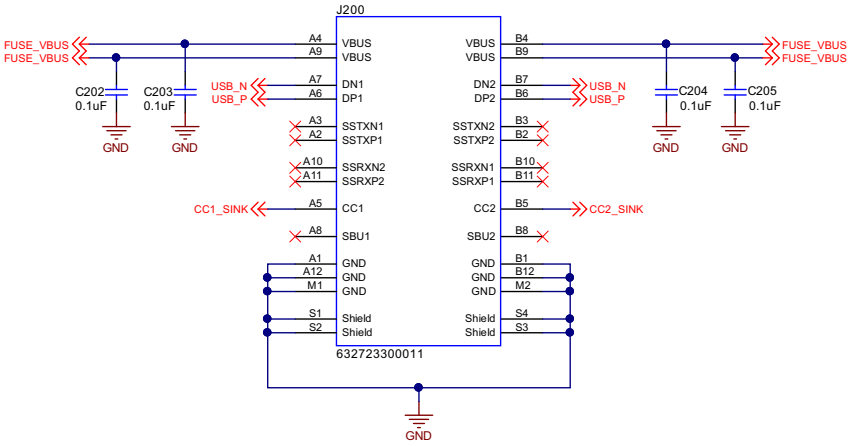

図 13. Type-C Connector and Fuse

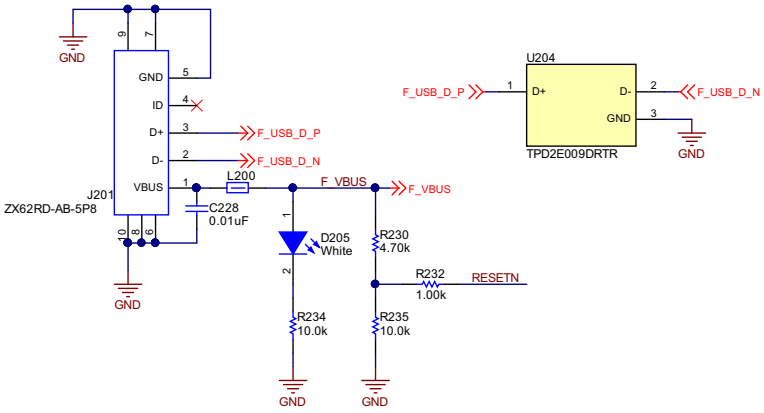

図 14. USB Type-B Connector

図 15. SPI and I2C Resistors

図 16. SPI CS Header

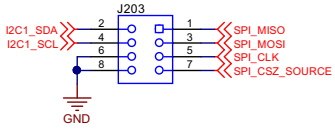

図 17. Programming Header

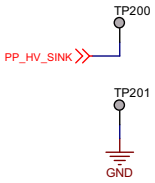

図 18. PPHV Test Points

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

To fully test the TIDA-050014 board, the following items are required:

1. Windows PC with TPS6598x Application Customization Tool installed
2. TIDA-050012 Companion TI-Design board
3. High Current Type-C Cable
4. 230 W Barrel Jack Connector or High Powered Bench Supply capable of sourcing 20 V at 10 A
5. E-load or resistive load

3.1.1 Hardware

For use of this design, a high powered power source is required. The power source must be able to source at least 20 V at 10 A.

3.1.2 Software

The TPS6598x Application Customization Tool must be installed on the Windows PC used to interface with this design.

3.2 Testing and Results

3.2.1 Test Setup

The effective RDS_{on} was measured using Power Duo mode and in normal operation. The results are highlighted in 表 2 and 表 3. Each measurement was taken with various currents going through VBUS. The boards were left for 5 minutes before the voltage drop across the power path was measured to allow for the drop to reach a steady state.

3.2.2 Test Results

表 2. RDS_{on} Power Duo Mode Measurments

VBUS Voltage (V)	VBYS Current (A)	Voltage Drop across Power Path (mV)	Effective RDS_{on} (mOhm)
20	1.5	21.48	14.32
20	2	28.16	14.08
20	3	44.42	14.81
20	4	58.12	14.53
20	5	76.32	15.26
20	6	97.32	16.24
20	7	120.36	17.19
20	8	145.32	18.17
20	9	175.76	19.53
20	10	216.78	21.68

表 3. RDS_{on} Single Power Path Measurements

VBUS Voltage (V)	VBYS Current (A)	Voltage Drop Across Power Path (mV)	Effective RDS_{on} (mOhm)
20	1.5	44.2	29.48
20	2	56.89	28.45
20	3	86.12	28.71
20	4	119.78	29.95
20	5	158.74	31.75

From the results above, it can be seen that the Power DUO Mode RDS_{on} is about half of the single power path RDS_{on}. This can be modeled as two FETs in parallel. The effective RDS_{on} when two of the same FETs are in parallel will be roughly half RDS_{on} of a single one.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-050014.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-050014.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-050014.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA050014.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-050014.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-050014.

5 Software Files

To download the software files, see the design files at TIDA-050014.

6 Related Documentation

1. *TPS65987DDH Power Path Performance and Documentation*

6.1 商標

7 Terminology

The terminology used in this design guide is all related to the USB Type-C and PD specifications. These specifications can be downloaded from the USB-IF website.

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