参考資料

TI Designs: TIDA-01629
サーボ・ドライブ向け、スマート・ゲート・ドライバ搭載48V、500W、3相インバータのリファレンス・デザイン

概要

効率、保護機能、統合は、最大60VDCの小型DC入力ドライバの重要な設計要素です。このリファレンス・デザインは、公称48VのDC入力と10A_{RMS}の出力電流に対応する3相インバータを紹介します。降圧型コンバータを内蔵するインテリジェントな100V 3相ゲート・ドライバDRV8350Rと、全ゲート電荷量が極めて小さい6個の100V NexFET™パワーMOSFETが、高効率の電力段を実現します。DRV8350Rの内蔵保護機能を使って、過熱、過電流、モータ端子間およびモータ端子-グランド間の短絡から電力段を保護します。INA240により高精度の位相電流検出を実現する一方、3.3V I/Oのインターフェイスによりブラシレス ACモータ制御用 C2000™MCUなどのホストMCUと接続できます。

リソース

TIDA-01629	デザイン・フォルダ
DRV8350R	プロダクト・フォルダ
INA240	プロダクト・フォルダ
CSD19532Q5B	プロダクト・フォルダ
TMP235	プロダクト・フォルダ
TPS62162	プロダクト・フォルダ
LAUNCHXL-F28379D	ツール・フォルダ

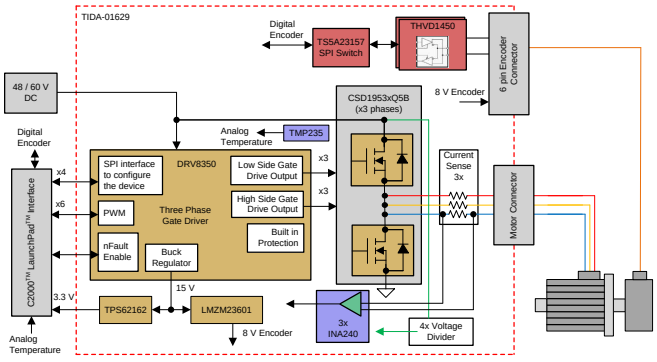
TI E2E™ Community　E2E™ エキスパートに質問

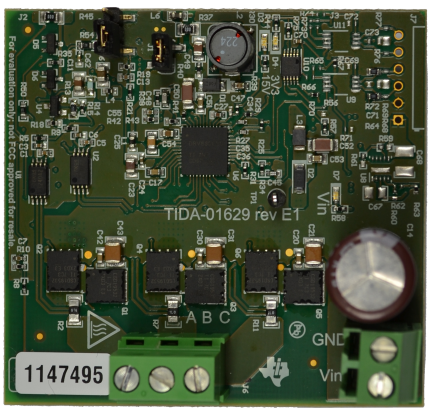
特長

- 24～60VDC入力、10A_{RMS}の連続位相電流に対応した、サーボ・ドライブ用3相インバータ
- ピーク効率が極めて高いため(99.0%)、ヒートシンクや冷却ファンは不要
- ハードウェア保護機能とゲート駆動電源用DC/DC降圧コンバータを内蔵したインテリジェントな3相ゲート・ドライバDRV8350R
- 電力段を完全保護：貫通電流、過電流、短絡、低電圧、および過熱保護
- ゲート・ドライバのソース/シンク電流を50mA～2Aで設定可能なため、効率とEMI性能の最適化が容易であり、V_{GS}ハンドシェイクおよび最小デッドタイム挿入により貫通電流を回避
- 同相除去比の高いゼロ・ドリフト電流のセンス・アンプINA240による同相シャント測定（1mΩ）に基づく電流検出

アプリケーション

- サーボCNCおよびロボティクス
- 産業用ロボット
- ACインバータおよびVFドライブ





1 System Description

Low-voltage DC-fed 3-phase inverter for voltages from 12 VDC to 60 VDC and power ratings of less than 1 kW, typically use shunt-based current sensing and non-isolated gate drivers along with power FETs. The inverter might be motor integrated or standalone.

An important design criteria is a robust power stage which is protected against shoot-through, overcurrent, and short-circuit as well as overtemperature.

Another aspect is efficiency to reduce cost for the heatsink and emissions (EMI) versus the switching speed. To implement these features with single- or half-bridge FET gate drivers, additional active and passive components are required, which increase BOM and PCB size, while often reducing the flexibility to modify parameters like the strength of the gate drive.

A three-phase gate-driver incorporates three discrete half-bridge gate drivers. A smart three-phase gate-driver architecture further reduces system cost, board size, as well as the BOM by saving up to 24 passive components. The integrated programmable Vds sensing and soft-shutdown allow the smart gate driver to detect any overcurrent or short-circuit event without the need for current sensing. To prevent shoot-through, the gate driver also implements V_{GS} handshake for each half-bridge with automatic dead time insertion. The ability to program the gate driver source and sink currents simplifies tuning, minimizing EMI, switch-node ringing, and switching losses. A serial interface increases flexibility and diagnostics, including fault reporting through the host microcontroller. An integrated DC buck regulator to create an intermediate rail from the DC input to supply the gate driver and signal chain further reduces BOM and system cost.

To allow for continuous and accurate phase current sensing with minimum losses, 1-mΩ inline shunts are used. A major challenge for non-isolated amplifiers is the huge common-mode voltage, which is a factor of 100 to 1000 times higher than the shunt full-scale voltage. Therefore, a current sense amplifier with a large common mode voltage range and very high DC and AC common mode rejection is required. Due to the low shunt impedance, an amplifier with additional integrated fixed gain and zero offset further helps reduce system cost while ensuring highly-accurate current measurements.

1.1 Design Considerations

This TI Design implements a 48-V, 500-W three-phase inverter with smart gate driver for low-voltage servo motors, the design is being fully tested at 48 V.

The major building blocks of this TI Design can be split into six different sub systems.

The Design sub systems are:

- Three-phase power stage including gate drivers and FETs
- Voltage and in-phase current sensing
- Host processor interface
- Diagnostic measurements
- System power supply
- Encoder interface

図 1 shows the block diagram.

The host processor to control the motor is not part of this design.

The focus of this design is to test the three-phase power stage including gate drivers and FETs, functional tests of the In-phase current sensing will also be done. The encoder interface and diagnostic measurements are not being tested in this design.

1.2 Key System Specifications

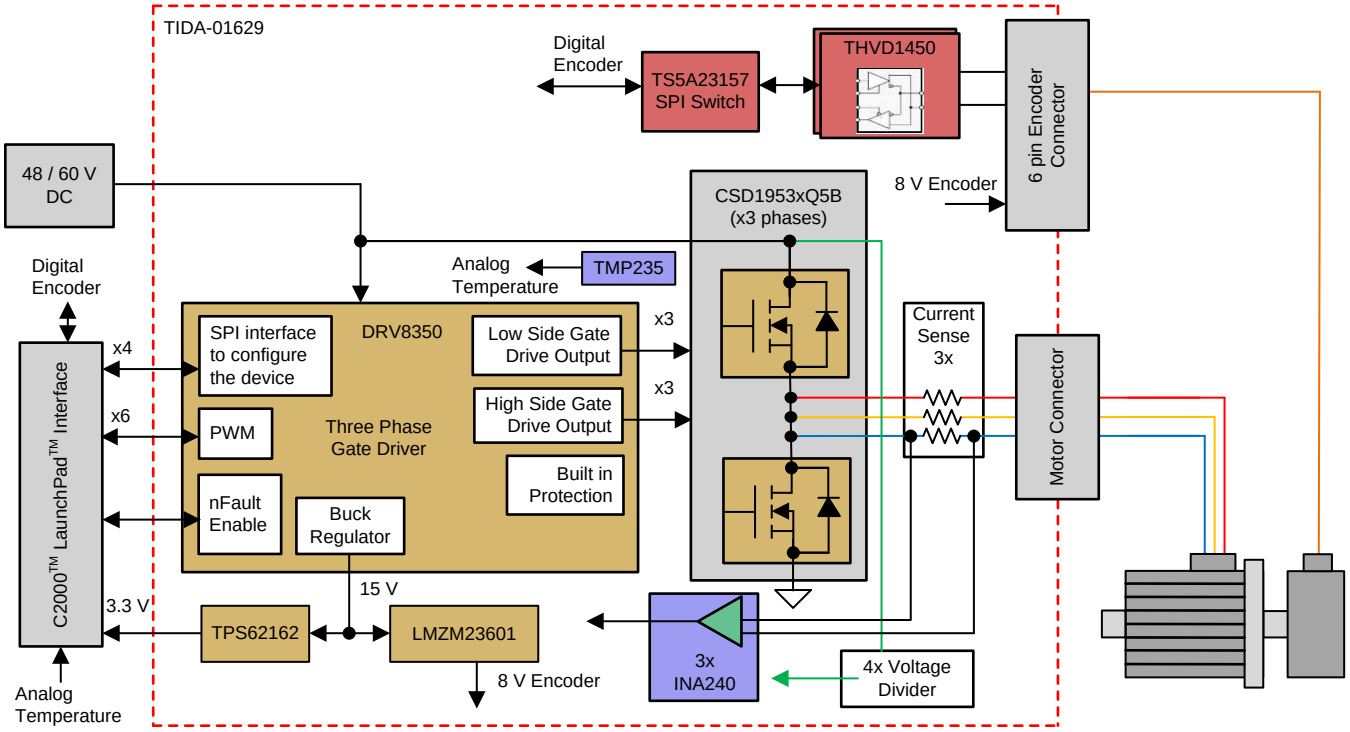
表 1. TIDA-01629 System Specifications

PARAMETER	VALUE (TYPICAL)	COMMENT
DC input voltage	24 V to 60 V	Absolute maximum 95 V DC
Output phase current	±10 A_{RMS} (continuous)	
Phase Current measurement range on all three phases	±30 A	Scaled from 0 V to 3.0 V, inverted with 1.5-V bias. Limited of the 3.0-V reference voltage chosen on the LaunchPad™
In-Phase Current Shunt	1 mΩ	Differential, non-isolated current sense amplifier with 50 V/V and enhanced PWM rejection (INA240)
PWM Switching Frequency	16 kHz	Up to 40 kHz
PWM Dead time	Automatic or user defined	DRV8350R offers an automatic dead time with handshake typical 180 ns to 350 ns, user defined typical 200 ns
Efficiency at 16 kHz	99% (peak)	Estimated at maximum output power see 3.2.3.1
Temperature range	–40ºC to 85°C	See 図 36 for the safe operating area
Protection	Short-circuit protection	Overcurrent protection using Vds sensing see 2.2.1.1
	Shoot through protection	Automatic Dead time insertion handshake
	Temperature protection	Temperature sensor to indicated overtemperature mounted to PCB
	UVLO	Integrated at 8.3 V
PCB temperature measurement range and accuracy	–40°C to 150ºC at 2ºC accuracy	TMP235A2
Interface signals	3.3 V I/O for PWM, I-V Sensing, Fault, …	TI BoosterPack™ compatible supporting 3.3-V signal levels see pin assignment in 表 7
Absolute Encoder Interface	RS485	Not tested or populated in this design
Indicator LEDs	Power rails	3.3-V, 15-V and DC input voltage
PCB layer stack	Four-layer, 70-µm copper	2 oz - No heat sink
Form Factor	65 mm x 60 mm	2560 Mil × 2352 Mil

2 System Overview

2.1 Block Diagram

図 1. TIDA-01629 System Block Diagram



2.2 Design Considerations

2.2.1 Hardware Design

2.2.1.1 Power Stage Gate Driver

Gate Driver

For the DRV8350R with the SPI control the gate drive and source strength can be programmed for best performance. This has been used during the testing to find the optimum configuration for the switch node. The DRV8350R also has an automatic dead time insertion between the high side and low side FET. This is done using the V_{GS} voltage monitoring and enables the driver to adjust for temperature drift and different FETs used in the system. For more details, see the *TDRIVE: MOSFET Gate Drive Control* section in *DRV835x 100-V Three-Phase Smart Gate Driver*.

Protection features

The overcurrent trip on the gate driver is tripping on the Vds voltage drop. The overcurrent trip threshold of the DRV8350R can be programmed over SPI. There are several options. These values are found in the *Electrical Characteristics* table using the variable VVDS_OCP. The minimum is 48 mV–72 mV and the maximum is 1.8 V–2.2 V. With this feature, a blanking time is also available to ensure no overshoots are being detected during switching of the FETs. For more information on this see the 表 2 which explains how the FET is used for over current protection.

V_{GS} definition

V_{GS} from the DRV835x is defined on which V_{VM} voltage is used on the DRV in this case the V_{GS}. Gate driver supply voltage (VM) is 15 V or above V_{GS} between 9 to 12.5 gate driver supply voltage (VM) is 12 V or above V_{GS} between 7 to 11.5 Typically, if VM is above 15 V, the V_{GS} is 10 V. These values are found in the *Electrical Characteristics* using the variable VGSH and VGSL. When picking the FETs is it important to know the V_{GS} to know the $R_{DS(on)}$ of the FET, this will have a big impact on the efficiency of the overall system.

SPI communication

For details on how to use the SPI communication of the DRV8350R, see *SPI Communication* in *DRV835x 100-V Three-Phase Smart Gate Driver*. The SPI format (protocol) is described which explains how to setup the SPI communication.

2.2.1.2 Power Stage FETs

With the V_{GS} sensing of the DRV8350R it is important to choose a FET which can fit the current requirements of the system. This means that it is needed to calculate the overcurrent trip level with respect to the FETs $R_{DS(on)}$ which is changing with V_{GS} and temperature.

V_{GS} vs $R_{DS(on)}$

V_{GS} from the DRV835xR is defined on which V_{VM} voltage is used on the DRV in this case the V_{GS}.

This voltage can be used to see the $R_{DS(on)}$ of the FET at the given voltage. The $R_{DS(on)}$ is needed to know how to define the overcurrent trip level of the DRV8350R, this can be found in the graph $R_{DS(on)}$ vs VDS on the front page of *DRV835x 100-V Three-Phase Smart Gate Driver*.

With these considerations, 表 2 shows the calculation of the FET chosen. The calculation is done using Ohms law.

表 2. DRV8350R Overcurrent Trip With Regards to CSD19532Q5B

DRV8350R V_{DS} OVERCURRENT TRIP VOLTAGE	CSD19532Q5B		
	Id	17 A	
	Idm	40 A	
	Temperature	25°C	125°C
VDS_LVL(0011b)	$R_{DS(on)}$(V_{GS} = 10 V)	4.0 mΩ	7.3 mΩ
0.090	A Peak	22.50	12.33
0.110	A Peak	27.50	15.07

To ensure fast switching of FETs, a RC snubber network was chosen on the half bridges. For more details on the snubber network see 2.2.1.4.

2.2.1.3 Phase Current and Voltage Sensing

The ADC converter accepts an input voltage of maximum 3.3 V or the device might be damaged. Therefore, it is important to scale the voltage measurements to fit the ADC used.

Phase Current

The amplifier with shunt needs to scale the voltage range which can fit the chosen ADC converter, in this design the currents measured is bidirectional, due to this the voltage range calculated is scaled by 2.

This design is specified to support a maximum current up to 30 A. With this specification, a 1-mΩ shunt resistor and an amplifier with a gain of 50 are selected.

Use 式 1 to calculate the voltage range of the output of the amplifier:

$$V_{Scale} = I_{ph} \times R_{Shunt} \times G_{amp} \times 2 = 30\ A \times 1\ m\Omega \times 50 \times 2 = 3.0\ V \quad (1)$$

The voltage scale of 3.0 V is chosen to fit the LaunchPad HW used to test the design, with usage of other HW a voltage scale of 3.3 V could be used.

With the scale set to 3.0 V it is important to set the voltage reference of the amplifier to ensure that 0 A is the center point of the voltage scale.

Also it is important to ensure that the power loss of the sense resistor can sustain the current of the system.

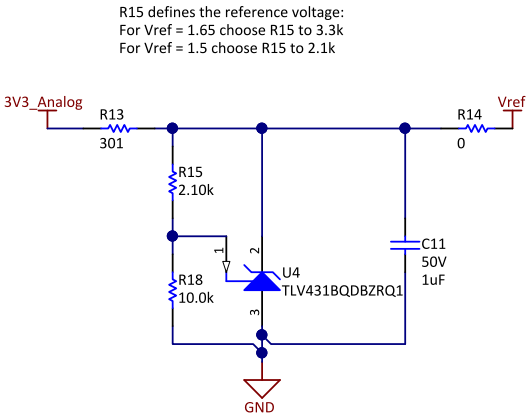
$$P_{loss} = I_{RMS}^2 \times R_{Shunt} = 30\ A^2 \times 1\ m\Omega = 0.9\ W \quad (2)$$

The 30 A is only in case of a fault condition nominal current would be 10 A_{RMS}, which would give a power of 0.1 W. The shunt resistor for this design has a rated power of 1 W.

Phase Current – Bias voltage reference

Since the design is built to scale to 3.0 V, due to the use of the Launchxl-f28379d board, the following considerations were made. For this design, a voltage reference which can support both the 3.0-V and 3.3-V reference voltage was selected. This is done using the TLV431. 図 2 shows the TLV431 schematic.

図 2. TLV431 Schematic From TIDA-01629



Using this reference, it is important to control how much current is flowing into the device with R_{13}, this defines if the device has a stable output. Here a 300-Ω resistor is used.

The second step is to pick the correct voltage divider. R15 and R18 are selected, R18 is always fixed to 10.0 kΩ.

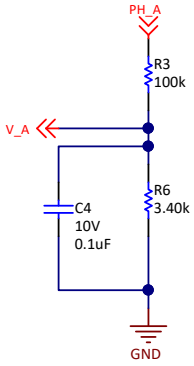
Choose R_{15} as 2.1 kΩ for 1.5 V, or as 3.3 kΩ for 1.65-V bias reference of the INA240.

Voltage

Two different voltage rails must be measured by the ADC converter. There are two different voltages which must be measured. One voltage is the 15-V rail which supplies the gate driver and the PoL power supply. Here, the PoL device supports up to maximum 20-V input. The other voltage is the V_{IN} voltage and motor phase voltage. This voltage can be maximum of 100 V before the device gets damaged; therefore, the voltage divider is chosen to support up to 100 V.

図 3 shows a schematic view of a 100-V phase voltage measurement.

図 3. Phase Voltage A Schematic From TIDA-01629



The calculation used the following formula:

$$R_6 = \frac{R_3 \times V_{OUT}}{V_{IN} - V_{OUT}} = \frac{100\ k\Omega \times 3.3\ V}{100\ V \times 3.3\ V} = 3{,}413\ \Omega \quad (3)$$

R_3 is chosen as 100 kΩ, for the specific voltage divider a low pass filter is added – this is done with C_4.

Hence, the resistor divider equation gives the following results and R_6 is chosen to be as explained in the following for both measurements:

For the 15-V rail, the following is entered into 式 3: V_{IN} 22 V, V_{OUT} = 3.3 V, R21 = 100 kΩ this results in R17 = 17647 Ω. The closest 1% value below this calculated value is 17400 Ω.

For the motor voltage and the V_{IN} voltage measurements, the following is entered into 式 3: V_{IN} 100 V, V_{OUT} = 3.3 V, R1 = 100 kΩ, this gives R2 = 3413 Ω. The closest 1% value below this calculated value is 3400 Ω.

2.2.1.4 Power Stage System Considerations

Snubber

The main consideration on this is what size of resistor package to dissipate the current over the snubber circuit. To calculate this current the following formula is used as a worst case scenario how this design is specified:

$$P = C_{(x)} \times V^2 \times f_{(s)} = 2.2\ nF \times 60\ V^2 \times 40\ kHz = 0.3168\ W \quad (4)$$

where

- C(x) is the snubber capacitor
- V is the DC link voltage
- 40 kHz is the maximum PWM frequency of the DRV8350R

When choosing a resistor – here a pulse proof resistor is chosen – this gives a higher power rating, it is evident that it is important to know how much power the resistor needs to dissipate.

- Pulse Proof 0603-sized resistors have a typical power rating of 0.25 W and an operating voltage of 75 V
- Pulse Proof 0805-sized resistors have a typical power rating of 0.5 W and an operating voltage of 150 V

See e2e.ti.com for good way of defining the snubber values:

https://e2e.ti.com/blogs_/b/powerhouse/archive/2016/05/05/calculate-an-r-c-snubber-in-seven-steps

Using this blog, the RC-snubber is chosen for the best performance for a 48-V input voltage.

LED

For the LED calculation it is assumed that the LED gets a forward diode current of 0.65 mA and has a forward diode voltage of 2.5 V.

This means that the LED resistor can be calculated with the following equation:

$$R_{LED} = \frac{V_{IN} - V_{doide}}{I_{LED}} = \frac{3.3\ V - 2.5\ V}{0.65\ mA} \approx 1{,}230\ \Omega \quad (5)$$

2.2.1.5 Host Processor Interface

The processor interface is selected to work for the Launchxl-f28379d. Here it is chosen to run the system from header J1 to J4. For more details on the interface, see 表 7 in the design guide.

2.2.1.6 System Diagnostic Measurements

Temperature measurement

A temperature sensor is added to the design to provide a turn off option when the temperature of the PCB is too high compared to the maximum temperature at which the ICs can operate.

Gate voltage measurement

This option is given to ensure a proper voltage is provided to the gate drive of the DRV8350R, this measurement can be used to diagnose if the DRV8350R can provide proper gate drive for the FETs.

2.2.1.7 System Power Supply

To reduce the power consumption of the DRV8350R, two supply rails for the DRV8350R are chosen, one V_{VM} for the gate driver supply voltage and one V_{IN} for the integrated buck controller. For details, read *Dual Supply Power Dissipation* in *DRV835x 100-V Three-Phase Smart Gate Driver*.

This configuration also gives the best flexibility for voltage level use of the DRV8350 as the Vin pin is limited to 95 V and the VM pin is limited to 80 V. Using the output of the regulated Buck to supply the VM pin means that the maximum input voltage of the system increases by 15 V.

To get the highest V_{GS} voltage of the DRV8350R but still keep the power consumption of the gate driver low, a 15-V rail was generated from the buck controller which can be used to supply the DRV8350R gate drivers.

15-V rail

To generate the 15-V output of the DRV8350R buck controller, the data sheet references *LM5008A 100-V 350-mA Constant On-Time Buck Switching Regulator*. In this data sheet, the section 8.2.2 is used to design the rail.

The buck is configured in a way that it will run with as high frequency as possible.

The DRV8350R has an integrated buck controller which provides a 15-V rail which will be used for the gate driver power supply input of the DRV8350R and the external voltage rails needed. In this case the PoL is 3.3 V, this 3.3-V rail need to provide the C2000 processor and the additional system components.

The 15-V rail can provide 350 mA, 表 3 calculates a power budget of the buck controller to ensure the current provided is enough for the system.

表 3. Power Budget of the 350-mA Buck at 15 V

PART NUMBER	VOLTAGE RAIL	CURRENT CONSUMPTION DATA SHEET	WATT	CURRENT ON 15 V WITH 80 EFFICIENCY
DRV8350R	15 V	15 mA (Ivm)	0.225 W	15 mA
F28379d	3.3 V	540 mA	2.145 W	119 mA
Total				**134 mA**

The buck has a maximum current of 350 mA which means that there is still 216 mA for additional circuitry.

3.3-V rail

The 3.3-V rail has a power requirement of around 1 A, this includes the sensing, diagnostic, encoder section and the option of powering the LaunchPad from the 3.3-V rail. The second requirement is what input voltage range is used.

Looking at the VM pin it has a minimum supply voltage of 8 V and with the choice of 15 V. Previously it was learned that this means the input voltage of the 3.3-V rail is between 8 V and 15 V, due to the supply of the DRV8350 gate driver.

The TPS62162 has an input voltage range of 3 V to 17 V providing 1-A current. This device comes in a fixed output voltage or adjustable output voltage range, a fixed output voltage is chosen to minimize external components and PCB size.

The *1-A Power Supply* section of *TPS6216x 3-V to 17-V, 1-A Step-Down Converters with DCS-Control™* has a schematic example for building a 3.3-V rail. The schematic shows that 1 input capacitor 1 output capacitor and an inductor is needed as external components. 表 3 shows the already-tested inductors. For the two capacitors, X5R or X7R ceramic capacitors are recommend.

2.2.1.8 Encoder Interface

The *Encoder Interface* is added to enable a servo driver power stage, this encoder interface is built to work with Endat2.2 and BiSS-C. For more details, see the TIDA-1401 tool folder:

www.ti.com/tool/tida-01401

2.2.2 Optional Layout Updates

Route the signals GHx and SHx and the signals GLx and SLx as close as possible to each other to reduce the inductance on the traces this will minimize the ringing on the gate voltage. Increase the trace width when possible to minimize Inductance on the traces this will minimize ringing on the gate voltage.

2.2.3 Software Design

The software for testing this design is based on the *DesignDRIVE Development Kit IDDK* example and the TIDM-SERVO-LAUNCHXS example in controlSUITE™. This example is updated to work with the TIDA-01629 design.

Here it is needed to ensure that the PWM from the C2000 are configured correctly for the High Side and Low Side FET and that the ADC channels are configured correctly for the LaunchPad used.

Secondly, the design is tested using built level 2 which means that board is used in an open loop configuration.

Download controlSUITE (www.ti.com/ControlSuite) for the IDDK example.

Some other things to add is the SPI communication to the DRV8350R and the GPIO enable pin of the DRV8350R, example software for this type of features can be found in the example TIDM-SERVO-LAUNCHXS.

For questions on software or controlSUITE, visit the e2e forum:

https://e2e.ti.com/support/microcontrollers/c2000/

See the *DesignDRIVE Development Kit IDDK v2.2 User's Guide* for documentation of the IDDK example for the C2000 MCU.

For documentation of the TIDM-SERVO-LAUNCHXS example, download controlSUITE and go to the folder: \controlSUITE\development_kits\TIDM-SERVO-LAUNCHXS\ .

2.3 Highlighted Products

2.3.1 DRV8350R

The DRV835x family of devices is highly integrated gate drivers for three-phase brushless DC (BLDC) motor applications. These applications include field-oriented control (FOC), sinusoidal current control, and trapezoidal current control of BLDC motors. The device variants provide optional integrated current shunt amplifiers to support different motor control schemes and a buck regulator to power the gate driver or external controller.

The DRV835x is based on a smart gate drive (SGD) architecture to minimize the number of externally required components typically required for MOSFET slew rate control and protection circuits. The SGD architecture also optimizes dead time to avoid any shoot-through conditions, provides flexibility in decreasing electromagnetic interference (EMI) by MOSFET slew rate control, and protects against any gate short circuit conditions through VGS monitors. A strong gate pulldown circuit helps prevent any unwanted dV/dt parasitic gate turn on events.

2.3.2 CSD19532Q5B

This 100-V, 4.0-mΩ, SON 5-mm×6-mm NexFET power MOSFET is designed to minimize losses in power conversion applications.

The main features of this device are:

- Ultra-low Q_g and Q_{gd}
- Very-low Q_{rr}
- Low thermal resistance
- Avalanche rated
- Pb-free terminal plating
- RoHS compliant
- Halogen free

注: Depending on the needs, a different FET could suit better for performance, like the CSD19531Q5A or CSD19533Q5A (pin-to-pin compatible).

2.3.3 INA240

The INA240 is a voltage-output, current-sense amplifier with enhanced PWM rejection that can sense drops across shunt resistors over a wide common-mode voltage range from –4 V to 80 V, independent of the supply voltage. Enhanced PWM rejection provides high levels of suppression for large common-mode transients (ΔV/Δt) in systems that use pulse width modulation (PWM) signals such as three-phase inverters in motor drives. This feature allows for accurate current measurements without large transients and associated recovery ripple on the output voltage. This device operates from a single 2.7-V to 5.5-V power supply, drawing a maximum of 2.4 mA of supply current. Four fixed gains are available: 20 V/V, 50 V/V, 100 V/V, and 200 V/V. The low offset of the zero-drift architecture enables current sensing with maximum drops across the shunt as low as 10-mV full-scale. All versions are specified over the extended operating temperature range (–40°C to +125°C), and are offered in an 8-pin TSSOP package.

図 4. INA240 Functional Block Diagram

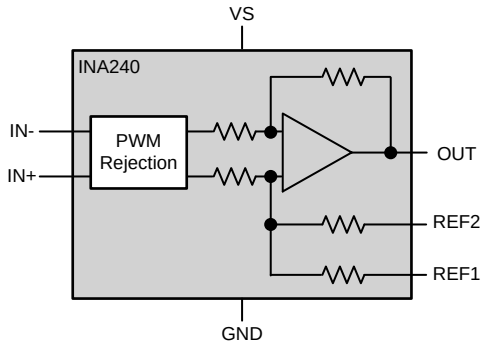


表 4. INA240 Features and Benefits

FEATURE	BENEFIT
Fast-transient common-mode voltage input filtering (Enhanced PWM Rejection) and high AC CMRR: 93-dB @ 50 kHz and 132-dB DC CMRR	Enables non-isolated shunt based precision phase current measurement with three-phase inverters with high switching frequency of 40-kHz and above
Wide common-mode input voltage range: -4 V to 80 V	Provides sufficient headroom for transient overvoltage and undervoltage in three-phase inverters with 48-V to 60-V DC link voltage
Low offset voltage (V_{OS} = ±25 µV) and low gain error (0.2%)	Low offset and gain error enables accurate current sensing without calibration
Low offset voltage drift (0.25 µV/°C) and gain error drift (2.5 ppm/°C)	Ultra-low offset and gain error drift allows high accurate current sensing over entire temperature range without temperature dependent calibration
400-kHz signal bandwidth	High signal bandwidth supports low latency phase current measurement of high-speed motors as well as low latency detection of high-current transients such as during a short-circuit event
Integrated output mid-point voltage reference voltage divider	Allows using an external ADC reference to set the INA240 mid-point voltage to half of the ADC reference voltage. This eliminates any offset generated by the ADC reference voltage drift.
Integrated precision gain setting resistors	Easier PCB layout and reduced BOM cost

2.3.4 TPS62162

The TPS6216x device family is easy to use synchronous step-down DC/DC converters optimized for applications with high power density. A high switching frequency of typically 2.25 MHz allows the use of small inductors and provides fast transient response as well as high output voltage accuracy by utilization of the DCS-Control™ topology.

With its wide operating input voltage range of 3 V to 17 V, the devices are ideally suited for systems powered from either a Li-Ion or other battery as well as from 12-V intermediate power rails. It supports up to 1-A continuous output current at output voltages between 0.9 V and 6 V (with 100% duty cycle mode).

Power sequencing is also possible by configuring the enable and open-drain power good pins.

In power save mode, the devices show quiescent current of about 17 µA from VIN. Power save mode, entered automatically and seamlessly if the load is small, maintains high efficiency over the entire load range. In shutdown mode, the device is turned off and shutdown current consumption is less than 2 µA.

The device, available in adjustable and fixed output voltage versions, is packaged in an 8-pin WSON package measuring 2.00 mm × 2.00 mm (DSG) or 8-pin VSSOP package measuring 3.00 mm x 3.00 mm (DGK).

2.3.5 TMP235

The TMP23x devices are a family of precision CMOS integrated-circuit linear analog temperature sensors with an output voltage proportional to temperature, making the series suitable for multiple analog temperature sensing applications. These temperature sensors are more accurate than similar pin-compatible devices on the market, featuring accuracy from 0°C to +70°C of ±1°C and ±2°C. The increased accuracy of the series is designed for many analog temperature sensing applications. The TMP235 device provides a positive slope output of 10 mV/°C over the full –40°C to +150°C temperature range and a supply range from 2.3 V to 5.5 V. The higher gain TMP236 sensor provides a positive slope output of 19.5 mV/°C from –10°C to +125°C and a supply range from 3.1 V to 5.5 V.

The 9-µA typical quiescent current and 800-µs typical power-on time enable effective power-cycling architectures to minimize power consumption for battery-powered devices. A class-AB output driver provides a strong 500 µA maximum output to drive capacitive loads up to 1000 pF and is designed to directly interface to analog-to-digital converter sample and hold inputs. With excellent accuracy and a strong linear output driver, the TMP23x analog output temperature sensors are cost-effective alternatives to passive thermistors.

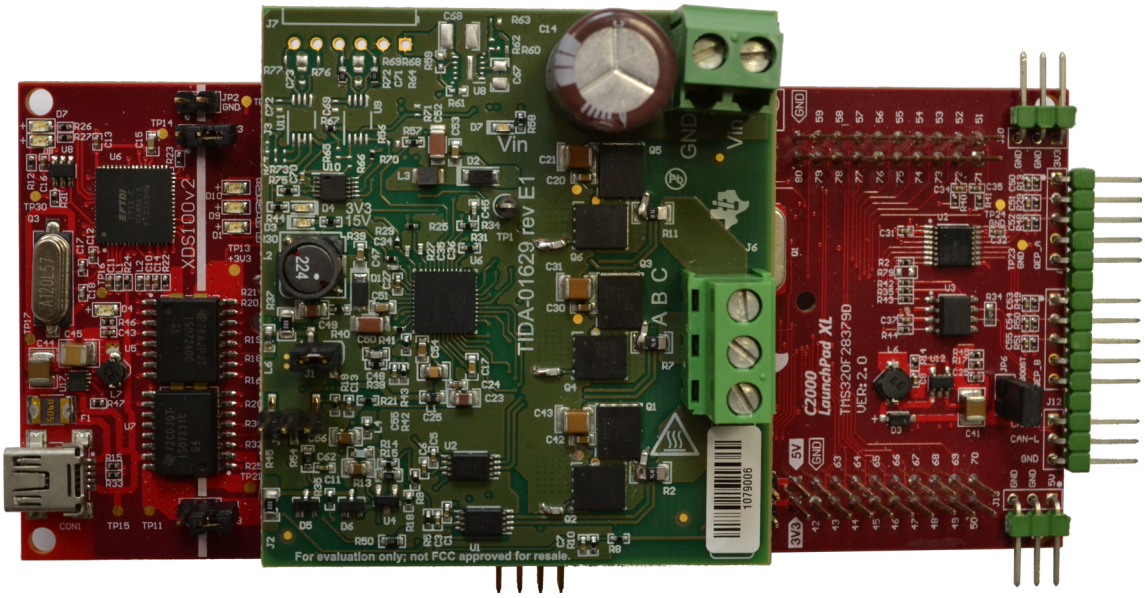
The relationship between the output voltage and the sensed temperature (in Celsius) is found in the *Feature Description* section of *TMP23x Low-Power, High-Accuracy Analog Output Temperature Sensors*.

3 Hardware and Test Results

3.1 PCB Overview

図 5 shows a photo of the top side of the TIDA-01629 PCB with the Launchxl-f28379d. The headers and default jumper settings of the TIDA-01629 are explained in 3.1.1.2.

図 5. Board Picture (Top View)



3.1.1 Hardware Configuration

3.1.1.1 Prerequisites

The following hardware equipment and software is required for the evaluation of the TIDA-01629 TI Design.

表 5. Prerequisites

EQUIPMENT	COMMENT
TIDA-01629	
C2000 F28379D LaunchPad	Available through TI eStore
Code Composer Studio™ 6	Download from http://www.ti.com/tools-software/ccs.html
controlSUITE™	Download from www.ti.com/ControlSuite
Motor	Needs to support voltage and current level of the design
Power supply	Needs to support voltage and current level of the design

3.1.1.2 Default Resistor and Jumper Configuration

Prior to working with the TIDA-01629 board, make sure that the correct resistor settings are applied. 表 6 shows the default jumper configuration on the board picture.

表 6. Default Resistor and Jumper Settings

HEADER OR RESISTOR	JUMPER SETTING
Header	Jumper for the 12-V gate drivers
Header	Jumper for voltage measurement of temperature or gate drive voltage

3.1.1.3 Host Processor Interface

表 7 shows the signals the TIDA-01629 TI design uses to communicate with the C2000 LaunchPad.

表 7. TIDA-01629 Pinout of J3 and J4 - Host Processor Interface

LAUNCHXL-F28379D				TIDA-01629 REVISION E1			
J1	**J3**	**J4**	**J2**	**J3**		**J4**	
3V3	5V	PWM1A	GND	3V3		PWMAH	GND
GPIO32	GND	PWM1B	SPIACS/GPIO61		GND	PWMAL	SPISTE
SCIB_RX	ADCIN14	PWM2A	GPIO123		IA	PWMBH	*ENC_CS*
SCIB TX	ADCINC3	PWM2B	GPIO122		IB	PWMBL	MUX_Channel
GPIO67	ADCINB3	PWM3A	RESETn	nFault	IC	PWMCH	
GPIO111	ADCINA3	PWM3B	SPIASIMO		Vbus	PWMCL	SPISIMO
SPIACLK	ADCINC2	GPIO24	SPIASOMI	SPICLK/GPIO65	VA	*ENC_CLK-BAR3*	SPISOMI
GPIO22	ADCINB2	GPIO16	GPIO124	*ENC-PWREN*	VB	*SPICLK-BAR4*	EN_DRV
GPIO105	ADCINA2	DAC1	GPIO125		VC		SPICS/GPIO27
GPIO104	ADCINA0	DAC2	GPIO29		*15V/Temp*		*ENC_DRCTL*

The signals in italics were not tested in this design, these signals were added to enable an encoder connection using the *Position Manager* of the C2000 MCU.

3.2 Testing and Results

Tests were done to characterize each individual functional block, as well as the entire board. In particular, the following tests were conducted:

- Three-phase power stage tests
- Power management
- Voltage and current sensing tests
- System performance

Tests were done at room temperature around 28 degrees Celsius.

3.2.1 Test Setup

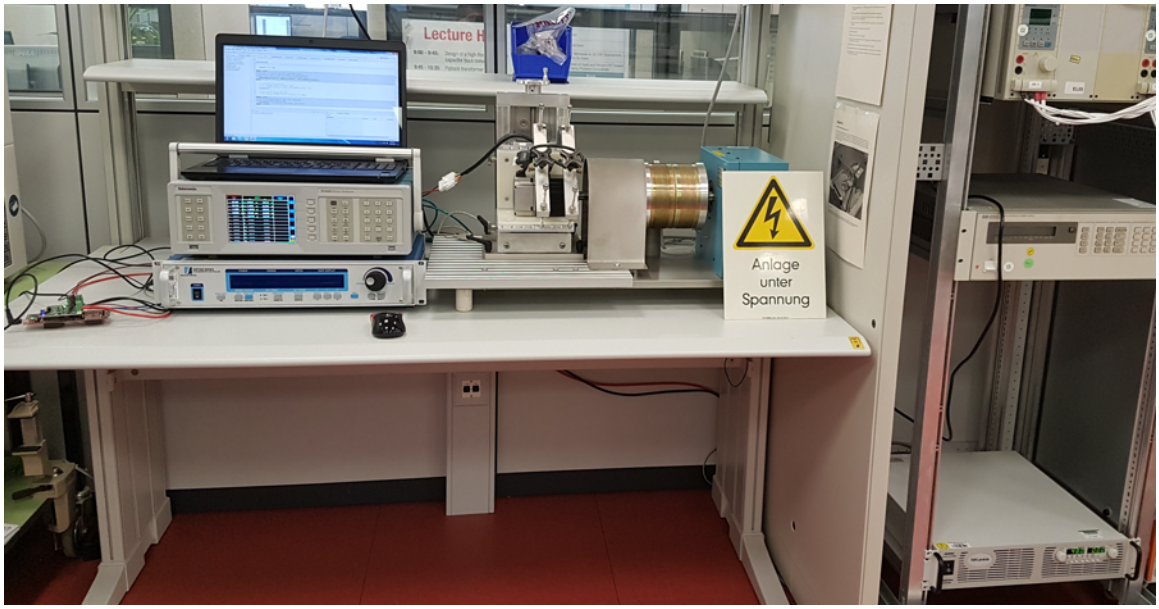
The following equipment was used for the TIDA-01629 testing session:

表 8. Test Equipment for TIDA-01629 Performance Tests

TEST EQUIPMENT	PART NUMBER
Oscilloscope Isolated	RTH1004 Rhode and Schwarz
Probes	RT-ZI10 Rhode and Schwarz
High-speed oscilloscope	Tektronix TDS784C
Differential probes	Tektronix P6630
Single-ended probes	Tektronix P6139A
Current probe	Tektronix TCPA300
Power analyzer	Tektronix PA4000-4
Dynamometer	Magtrol DSP7001
	Magtrol HD705-8
PMSM Motor	Moons SM0803DE2-KCF-NNV
Thermal camera	Fluke TI40
Power supply	TDK Lampda – GEN100-33

For the different tests, some of the equipment is used as described in 表 8. 図 6 shows a test setup used for the system.

図 6. TIDA-01629 Picture of Test Setup for System Tests



During testing, the DRV8350R is set up with the following conditions, if not otherwise specified.

表 9. DRV8350R Settings During Test

PARAMETER	VALUE	PARAMETER	VALUE
IDRIVEP_LS	300 mA (0100b)	IDRIVEP_HS	300 mA (0100b)
IDRIVEN_LS	600 mA (0100b)	IDRIVEN_HS	600 mA (0100b)
PWM_MODE	6 PWM mode (00b)	DEAD_TIME	50-ns dead time (00b)

表 10. C2000™ Settings During Test

PARAMETER	VALUE	PARAMETER	VALUE
PWM	16 kHz	Dead time	10 ns

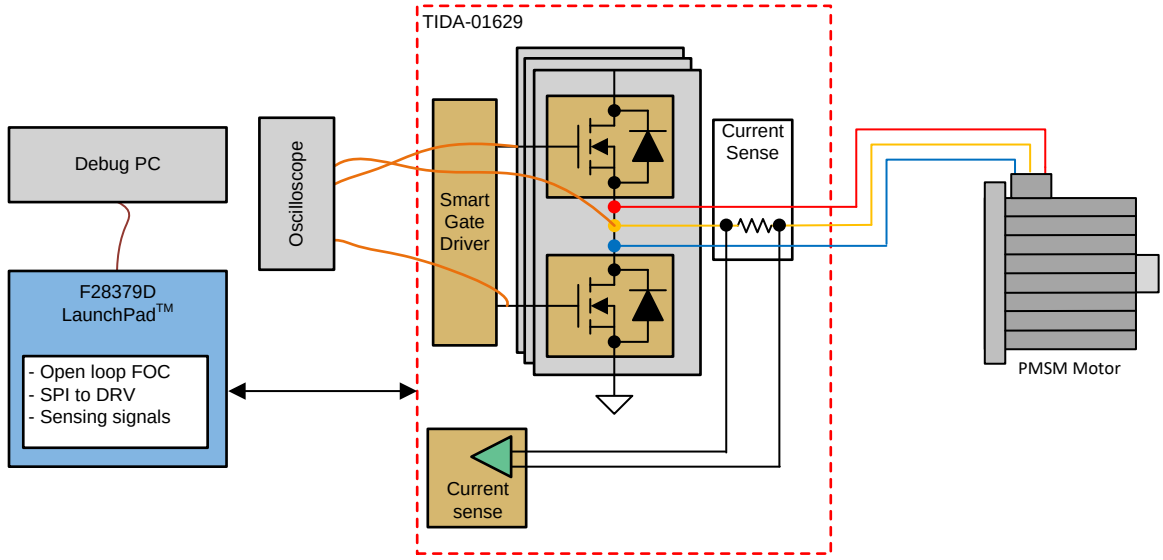
The different test setups used are described in 3.2.2 with a diagram showing each setup.

3.2.2 Design Test Results

3.2.2.1 Gate Drive Voltage and Phase Voltage

図 7 shows the test setup for the gate voltage and switch-node measurements. This section details the measurements of the gate voltage vs switch node.

図 7. TIDA-01629 Diagram of Test Setup for the Gate Voltage and Switch-Node Measurements



For this test, the system is using a 48-V and 60-V input voltage and the motor is set to a fixed angle using open loop FOC control. The signals are measured using phase A, and a low-side gate drive and phase voltage signals are referenced to GND. The high-side gate drive signal is referenced to the phase voltage.

The measurements in 図 8 through 図 11 show that the half bridge switch point from low to high and from high to low in the condition that the TIDA-01629 system is setting have either different positive and negative currents on phase A. This shows all configurations of soft and hard switching of the phase used which are 4 measurements per current level.

図 8. Soft Switching Phase A Voltage Falling Edge, Phase Current at 48 V, –10 A

図 9. Hard Switching Phase A Voltage Rising Edge, Phase Current at 48 V, –10 A

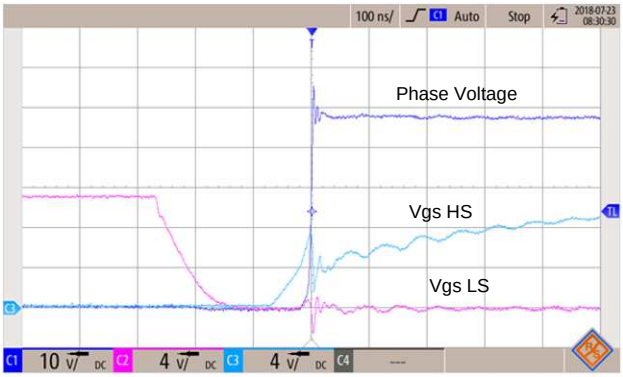


図 10. Hard Switching Phase A Voltage Falling Edge, Phase Current at 48 V, 10 A

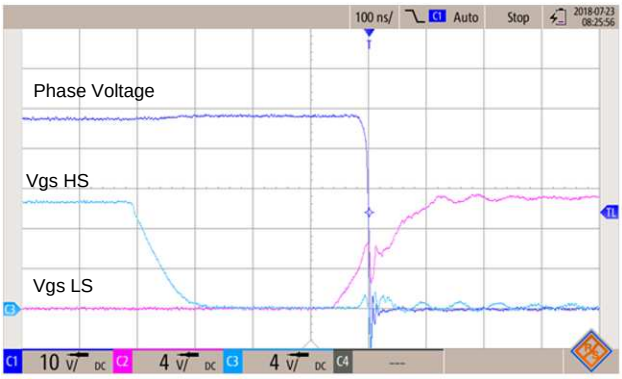
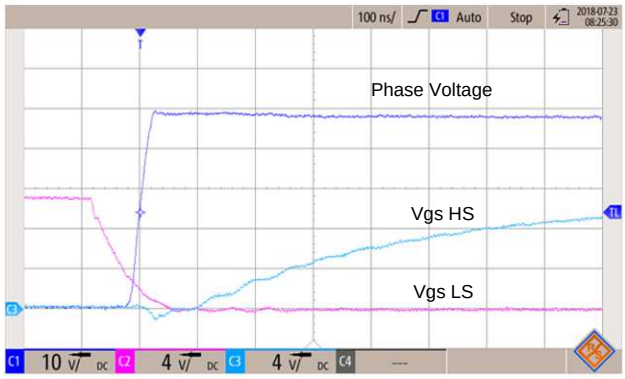


図 11. Soft Switching Phase A Voltage Rising Edge, Phase Current at 48 V, 10 A



These images show in the two hard switching cases that the overshoot is in the switch turn on around 6 V and the turn off is around –9.5 V. The DRV8350R can handle both these cases on the phase voltage. shows that the DRV8350R pin GHx (phase voltage) can handle up to –10 V at a 200-ns pulse and –5 V continuous.

When investigating this half bridge phenomenon, it is important to ensure what negative pulse the gate driver can survive. The waveforms illustrate that the snubber network has been optimized for 48-V system.

図 12 through 図 15 show the performance using 60 V using the same settings for 48 V.

図 12. Soft Switching Phase A Voltage Falling Edge, Phase Current at 60 V, –10 A

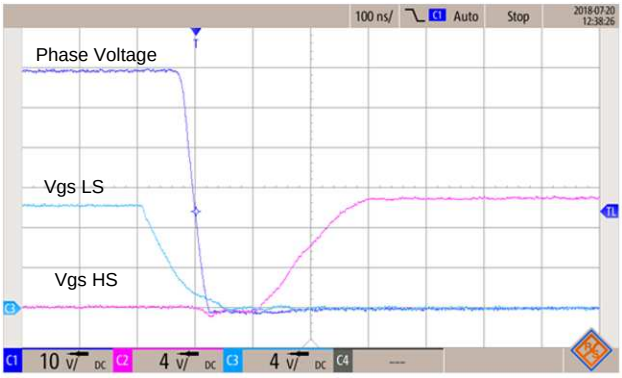


図 13. Hard Switching Phase A Voltage Rising Edge, Phase Current at 60 V, –10 A

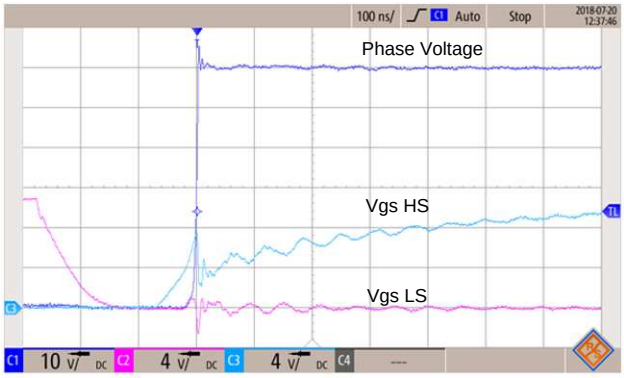


図 14. Hard Switching Phase A Voltage Falling Edge, Phase Current at 60 V, 10 A

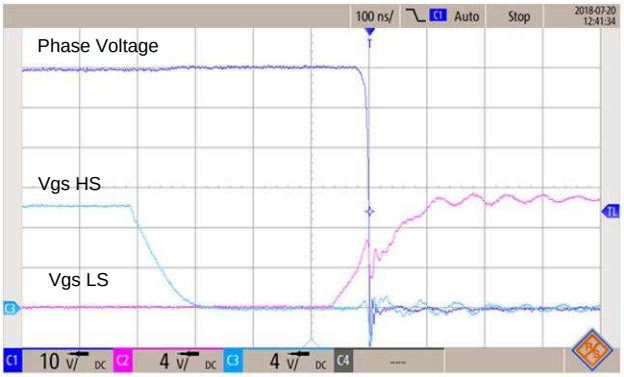
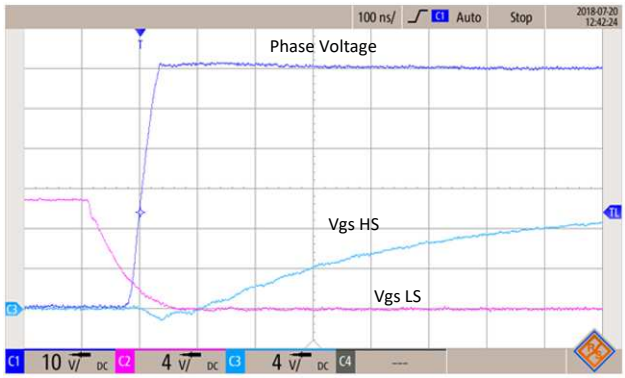


図 15. Soft Switching Phase A Voltage Rising Edge, Phase Current at 60 V, 10 A

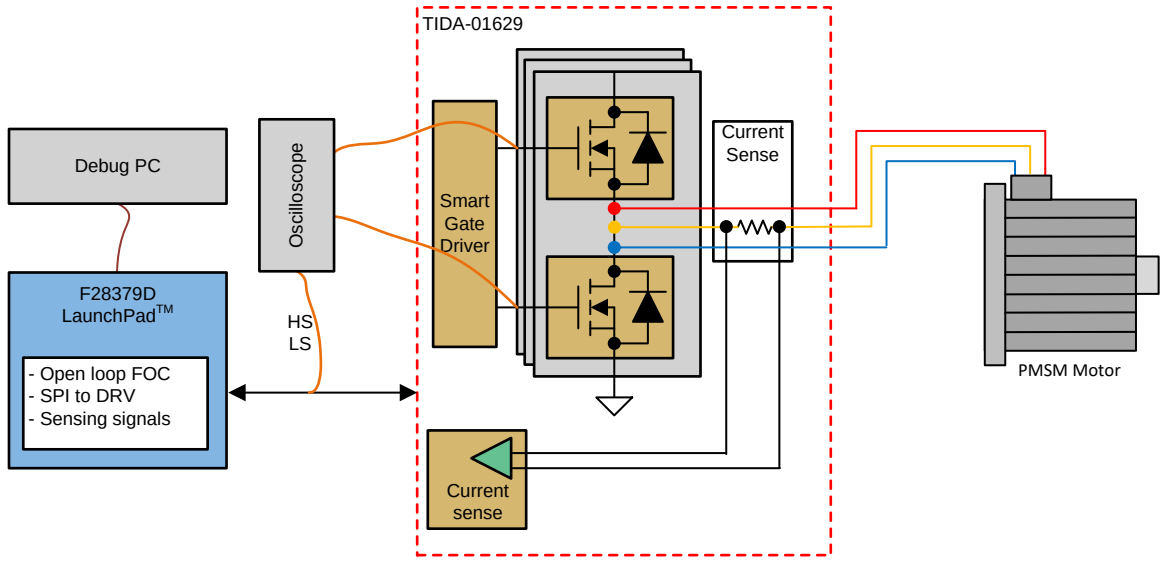


The waveforms in the two hard switching cases shows that the overshoot is in the switch turn on around 6 V and the turn off is around –9.5 V, which is the same performance as of the 48-V system.

3.2.2.2 *Digital PWM and Gate Voltage*

図 16 shows the test setup. The image shows the measurement of the propagation delay between the digital PWM and the gate voltage.

図 16. TIDA-01629 Diagram of Test Setup for the Digital PWM and Gate Voltage Measurements



For this test, the system is using a 48-V input voltage and is setting the motor to a fixed angle using open loop FOC control. The signals are measured using phase A and all signals are referenced to GND of the TIDA-01629 board.

The measurements in 図 17 to 図 20 show that the half bridge switch point from low to high and from high to low in the condition that the TIDA-01629 system is setting either 5 A or –5 A on phase A. This shows all configurations of soft and hard switching of the phase used. This measurement also shows the option of using the DRV8350R in either 6PWM mode which adds a dead time and a handshake delay of the high side and low side gate drive or independent mode where the digital PWM generation has to generate the dead time. Here the high-side gate driver is driven with 1000 mA.

6 PWM Mode

図 17. 6-Mode PWM vs V_{GS} LS and HS. Phase A Current at 48 V, 5 A Hard Switching

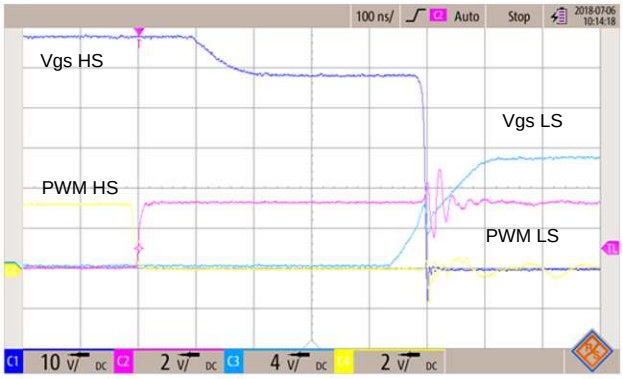


図 18. 6-Mode PWM vs V_{GS} LS and HS, Phase A Current at 48 V, 5 A Soft Switching

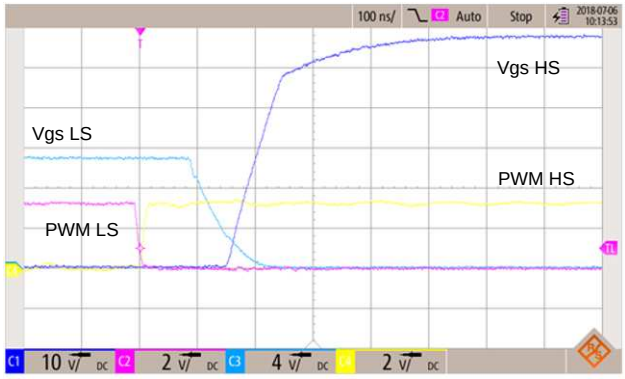


図 19. Six Mode PWM vs V_{GS} LS and HS. Phase A Current at 48 V, –5 A Hard Switching

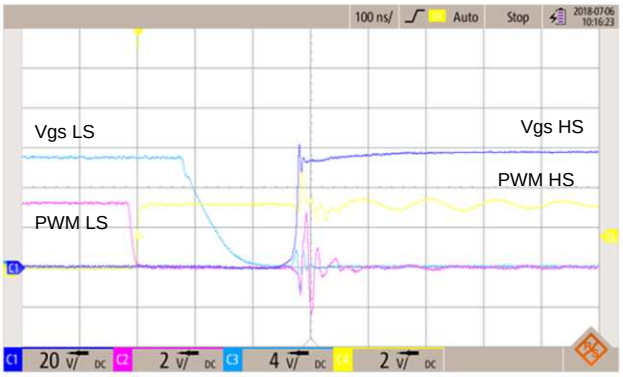


図 20. Six Mode PWM vs V_{GS} LS and HS, Phase A Current at 48 V, –5 A Soft Switching

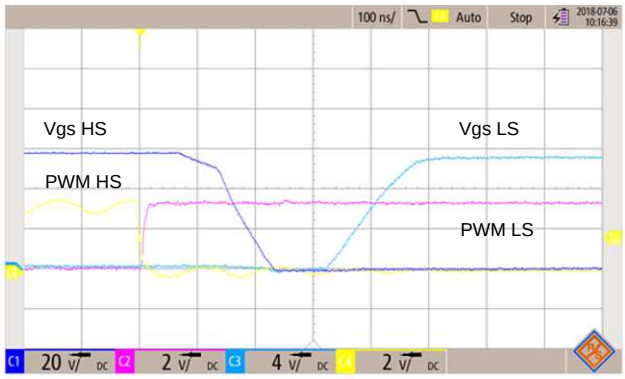


図 17 through 図 20 It can be seen on the figures above that the “6 PWM mode” adds a dead time and has a hand shake which ensures that the half bridge does not have shoot through.

This automatically inserted dead time is between 180 ns to 340 ns depending of which current and switching condition the gate driver is switching at. Here the dead time is seen from the start of turn off of the FET until the start of turn on of the FET.

Independent mode

図 21. Independent Mode PWM vs V_{GS} LS and HS. Phase A Current at 48 V, 5 A Hard Switching

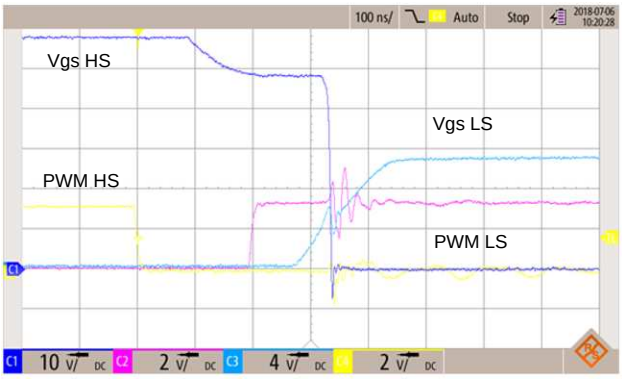


図 22. Independent Mode PWM vs V_{GS} LS and HS, Phase A Current at 48 V, 5 A Soft Switching

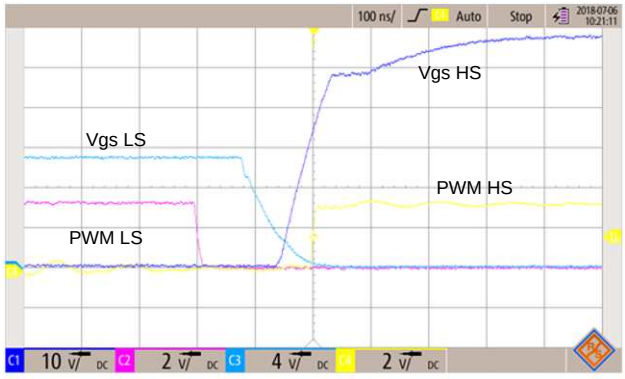


図 23. Independent Mode PWM vs V_{GS} LS and HS. Phase A Current at 48 V, –5 A Hard Switching

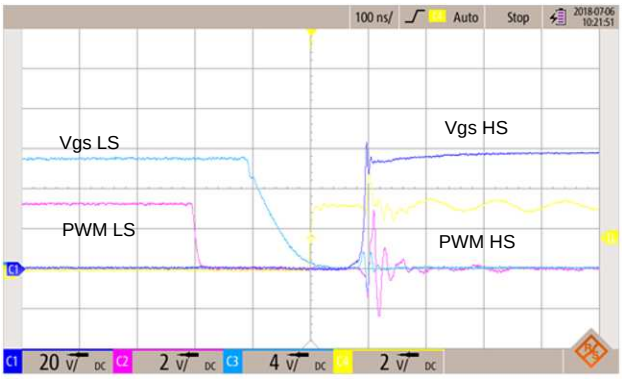
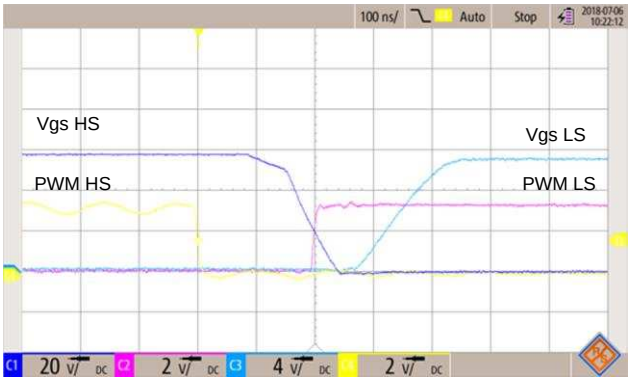


図 24. Independent Mode PWM vs V_{GS} LS and HS, Phase A Current at 48 V, –5 A Soft Switching

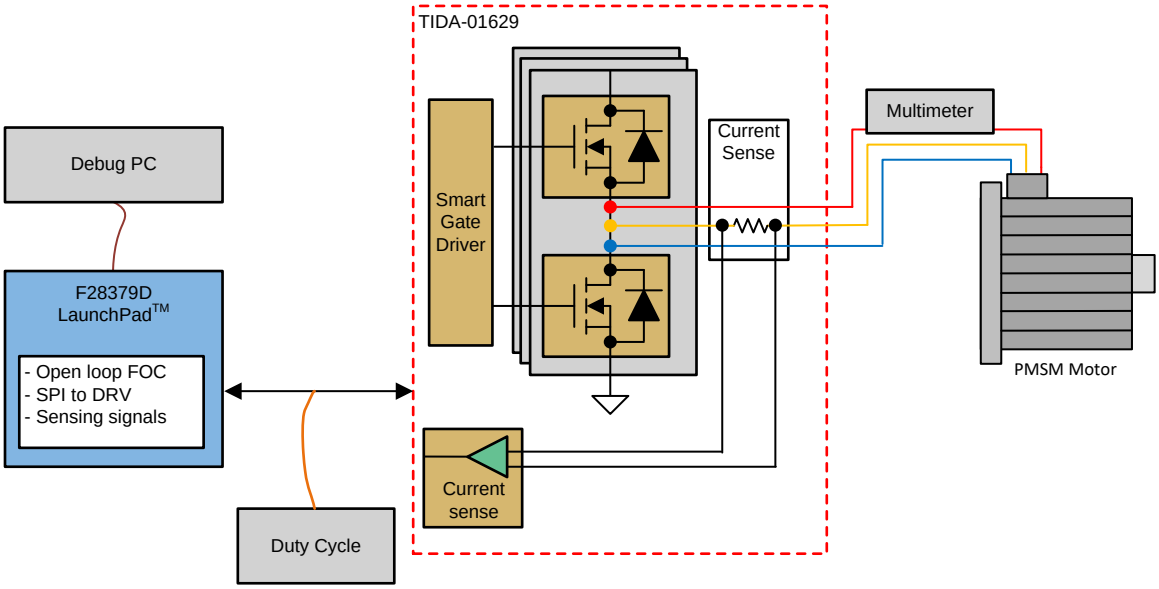


The DRV8350R also has a mode called “independent mode” here there is no handshake or dead time delay added by the DRV8350R. Now the PWM controller has to add the dead time. Using this approach and adding 200-ns dead time on the digital PWM signals it shows that the dead time difference is around 180 ns to 220 ns, this difference is due to the internal clock synchronization of the DRV8350R. Here the dead time is seen from start of turn off of the FET until the start of turn on of the FET.

3.2.2.3 Linearity Measurement

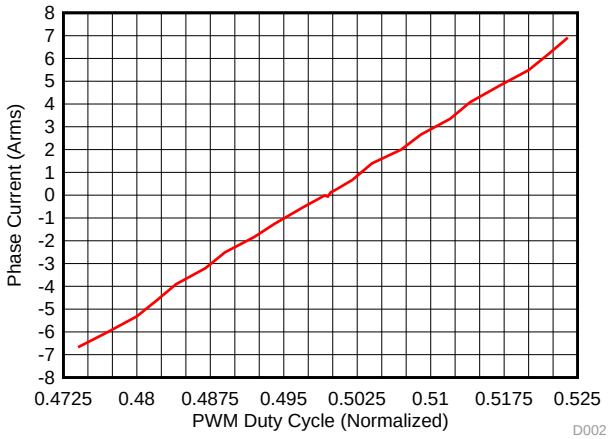
This section shows how the system performs generating a linear current for the motor control. This can be used to show how well the system handles low currents on the motor. 図 25 shows the test setup for the linearity measurement.

図 25. TIDA-01629 Diagram of Test Setup for the Linearity Measurements



For this measurement the independent PWM mode is used with 200 ns dead time. This measurement shows how well the gate drivers supports giving currents, for motors running with low current and low torque it is important that the duty cycle produced gives a predefined current which can be used for the motor control, depending on the precision wanted of the drive this curve can also be used and compensated to achieve a linear current on the drive. The curve in Below a curve can be seen showing 図 26 the linearly performance of the gate driver with the FETs.

図 26. Linearity Measurement of the TIDA-01629 Design Using Independent PWM Mode

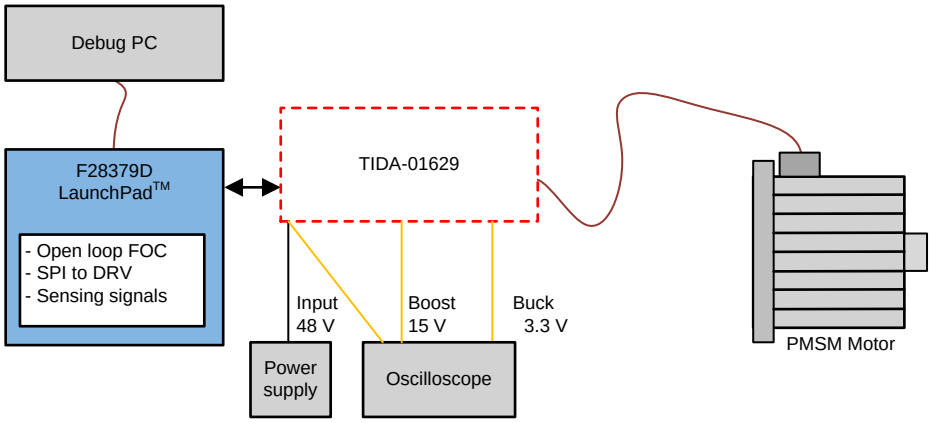


Due to the low dead time needed using the DRV8350R with the CSD19532 FETs 図 26 shows that the linearity of the driver stage has an excellent performance, even at low currents.

3.2.2.4 Power Management

The section shows the power up and power down sequence of the TIDA-01629. The measurements are done with the following methods:

図 27. TIDA-01629 Diagram of Test Setup for the Power Measurements



Power up

図 28. Power-up Sequence of the TIDA-01629 Design

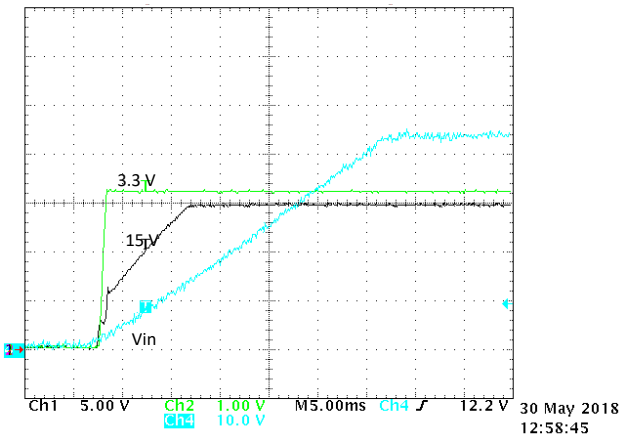
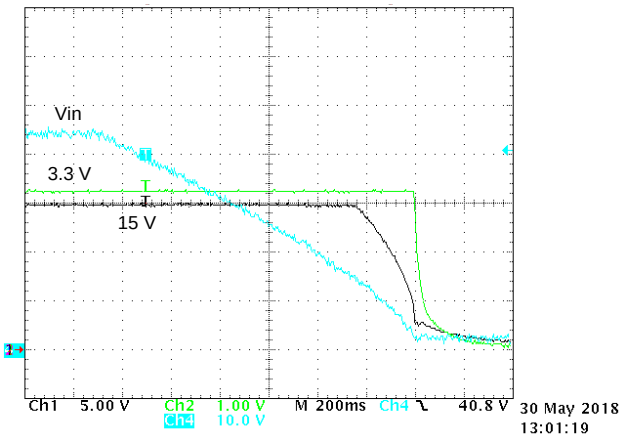


図 28 shows that the power up sequence of the system is V_{IN} goes above approximately 4 V, the DRV8350R starts providing the 15-V rail, when this rail is approximately 4 V it enables the 3.3-V rail.

V_{IN} has a slow ramp as it is charging the V_{IN} capacitors which are
180 µF + 2 × 1µF + 6 × 2.2 µF + 8 × 0.1µF + 3.3 µF × 2 which is a total of 202.6 µF.

Power Down

図 29. Power-Down Sequence of the TIDA-01629 Design



V_{IN} is ramp down is again slow as it has to discharge the 202.6-µF capacitors.

As the V_{IN} voltage goes below approximately 7 V, the 15-V rail starts to power down when this rail gets to approximately 4 V it shuts down the 3.3-V rail which then slowly dissipates the remaining charge of the capacitors.

表 11. Power Consumption 15-V Rail

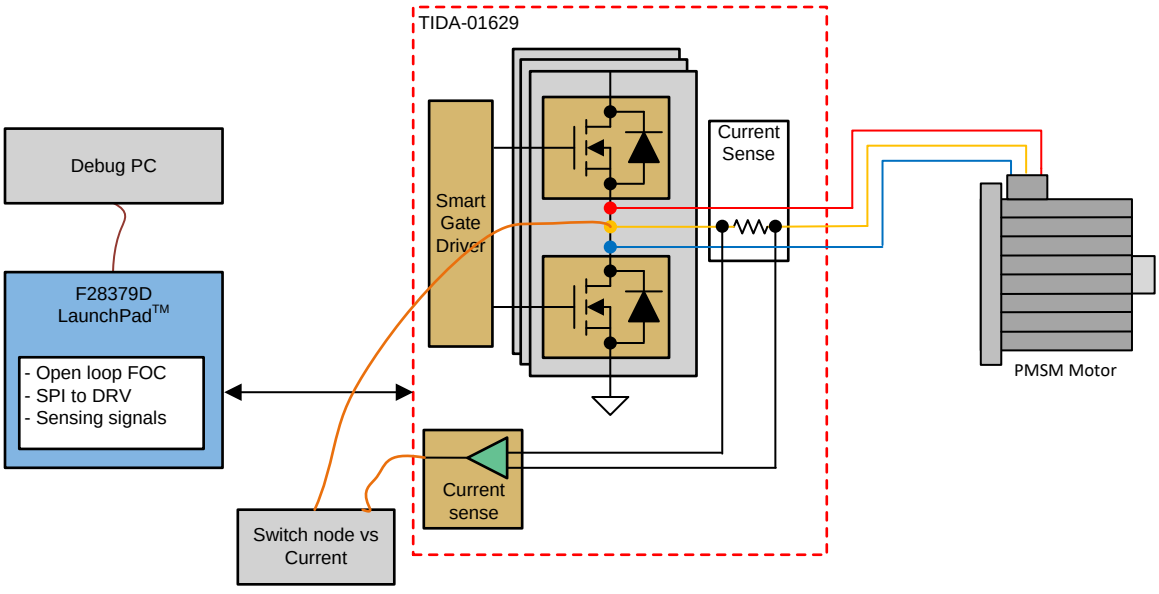
MEASUREMENT	TASK	15-V DRV8350R GATE DRIVER
Current [mA]	Idle (Gate driver disabled)	0.13 mA
Current [mA]	16-kHz PWM	14.68 mA

The 15-V rail measurement only includes the gate driver of the DRV8350R.

3.2.2.5 Phase Current Measurements

This section shows how the phase current measurement performance generating Open loop rotating field for the motor control.

図 30. TIDA-01629 Diagram of Test Setup for the Current Measurements



Below two measurements are shown one with the motor rotating and one zooming in on a phase voltage switch point.

図 31. Rotating Current Measured on the Output of the INA240

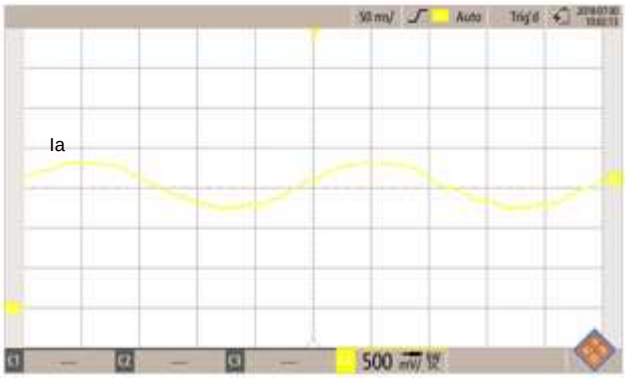
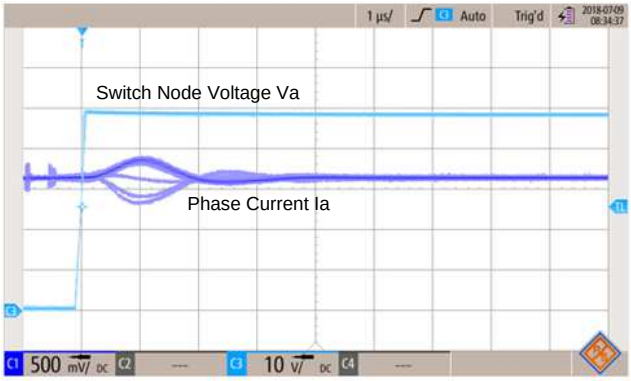


図 31 shows that the INA240 shows a sinusoidal waveform, here the system is running open loop, which is why there are the distortions of the sine wave. 図 32 shows the common mode performance of the INA240.

図 32. INA240 Output Measured During Switch Point



This measurement shows that measuring several switch points at the same time make it possible to see the worst-case scenario of the settling time of the amplifier. A maximum settling time of around 2.0 µs can be expected.

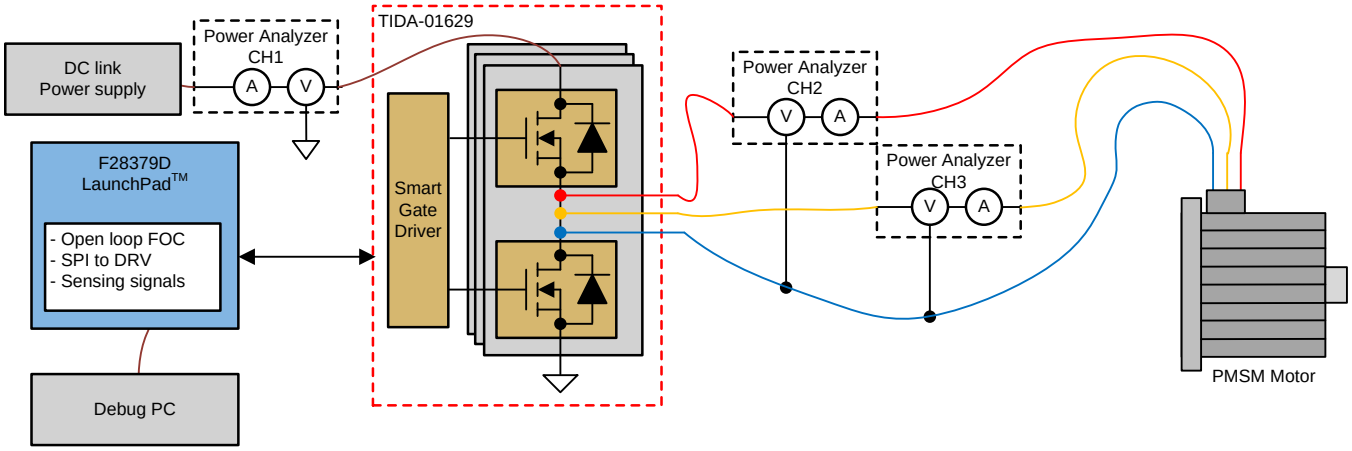
For further details on the INA240, see the design TIDA-00913, for a thorough analysis of the current sensing device in a motor control system with fast transients using the LMG5200 80-V GaN half bridge power stage.

3.2.3 System Test Results

3.2.3.1 Efficiency Measurement

The efficiency testing was performed at a 28°C lab temperature using a *Tektronix PA4000 Power Analyzer*. The TIDA-01629 device was powered with a 48-V DC and a Moons low-voltage servo motor was used as the load. The test software implemented on the C2000 LaunchPad was configured for open-loop control and generated the corresponding PWM to drive an impressed three-phase AC current at a 10-Hz frequency with configurable amplitude. The PWM carrier frequency was set to either 16 Hz. During the efficiency testing, no cooling or heat sink was used on the TIDA-01629 to show system performance. 図 33 shows a diagram of the test setup.

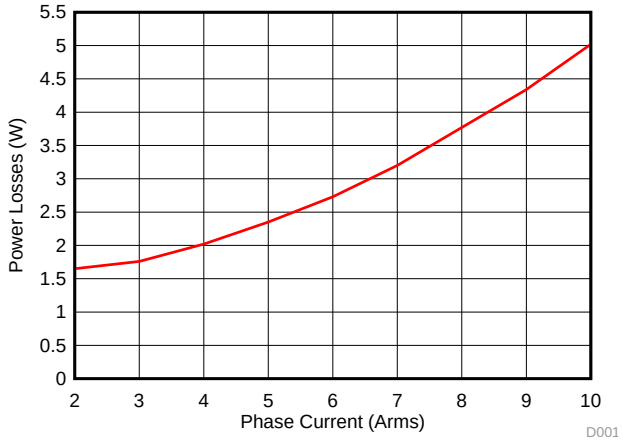
図 33. TIDA-01629 Diagram of Test Setup for Efficiency Measurement



The motor is run at 10 Hz electrically with an open loop FOC space vector control testing the system up to 10 A_{RMS} on the phases. With these settings the power losses at 48 V was as seen in 図 34, this figure includes all losses of the TIDA-01629 board.

図 34 shows the TIDA-01629 power losses versus the three-phase motor load current in A_{RMS}.

図 34. TIDA-01629 Board Losses at 16-kHz PWM at 48-V Input vs Motor Phases Current With Moons Motor at Zero Torque



式 6 to 式 8 are used to calculate the estimated maximum apparent load for a three-phase motor. To calculate the motor phase-to-phase voltage, 式 6 was used, here it is assumed that *Space-Vector Modulation* is used.

$$V_{p2p} = \frac{V_{bus} \times \sqrt{3}}{2 \times \sqrt{2}} \times SVM = \frac{48\ V \times \sqrt{3}}{2 \times \sqrt{2}} \times \frac{2}{\sqrt{3}} \approx 34\ V \quad (6)$$

With the phase-to-phase voltage found, the apparent load for the motor can be calculated assuming a power factor of the PMSM motor of 0.9.

$$P_{estload} = I_{RMS} \times V_{p2p} \times \sqrt{3} \times pF = 10\ A_{RMS} \times 34\ V \times \sqrt{3} \times 0.90 \approx 529\ W \quad (7)$$

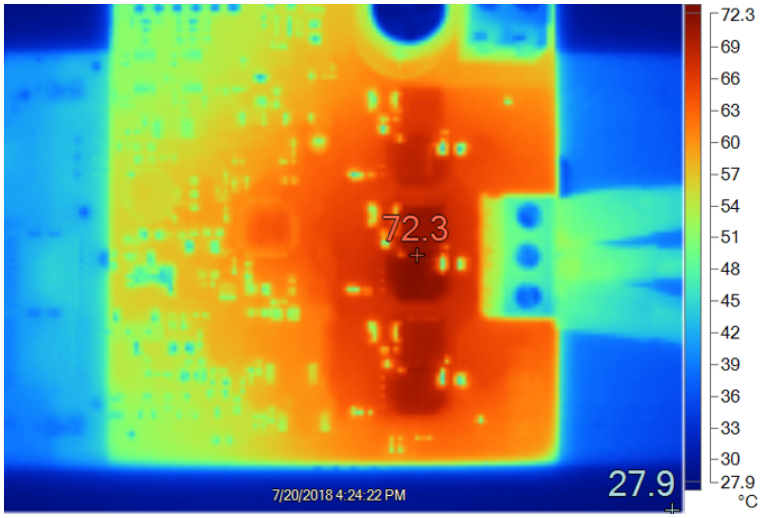
To calculate the efficiency at maximum load the following equation was used.

$$\eta = \frac{P_{estload} - P_{loss}}{P_{estload}} = \frac{529\ W - 5.02\ W}{529\ W} = 99.05\% \quad (8)$$

3.2.3.2 Thermal Analysis

The thermal analysis of the design was performed at a 28ºC lab temperature with a 48-V DC input with a 16-kHz PWM with the low-voltage servo motor driven with sinusoidal phase currents at a 100% load current (10 A_{RMS}, 14.14-A peak). This test did not use a heatsink or fan. 図 35 shows the thermal picture of the test setup.

図 35. TIDA-01629 Thermal Picture at 10 A_{RMS}



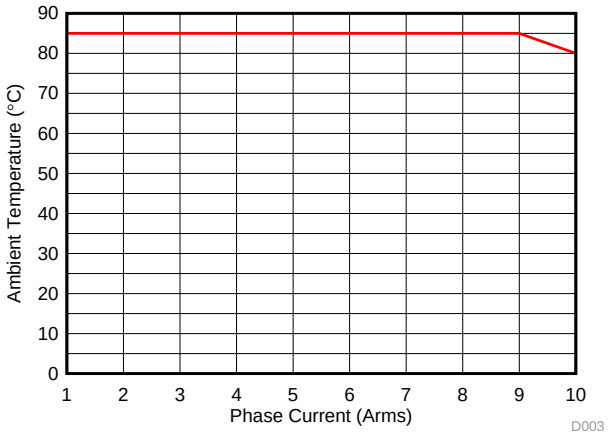
This measurement shows that at 10 A_{RMS} the FETs have a temperature increase of 44.4ºC with the consideration that the IC can be 125ºC junction, this means that the current design without heat sink can work up to 79.99ºC without heat sink, if 85ºC is needed a heat sink or cooling is needed at 10 A_{RMS}.

The CSD19532Q5B maximum junction temperature of at the maximum load is estimated based on the power losses of the CSD19532Q5B at 5.02 W at 16-kHz PWM for the six FETs, this means that I assume the full board loaded of the TIDA-01629 is dissipated through the FETs. This means that the maximum junction temperature of the CSD19532Q5B is 72.97ºC see 式 9, assuming that all of the six CSD19532Q5B power losses are dissipated through the top-side package.

$$T_J = 72.3^{\circ}C + \frac{5.02\ W}{6 \times 0.8\ \frac{C}{W}} = 72.97^{\circ}C \tag{9}$$

With this consideration, the following safe operating area of the TIDA-01629 with no cooling or heat sink is evident in 図 36.

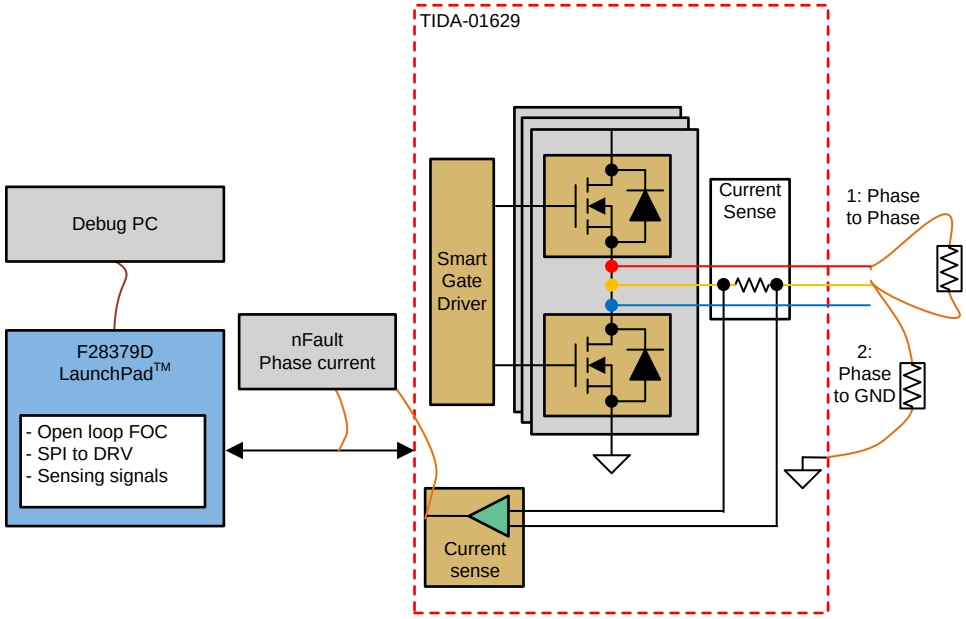
図 36. TIDA-01629 Safe Operating Area With Natural Convection



3.2.3.3 Short-Circuit Protection

This section shows how the system performs when introducing faults to the system. Here the overcurrent protection of the DRV8350R is tested.

図 37. TIDA-01629 Diagram of Test Setup for Fault Generation



With this test setup, two conditions are tested first the phase to phase short and the phase to GND short is tested. A load was added with a 0.5-Ω resistor which can simulate the current when having a short circuit. On the plots in 図 38 and 図 39, the phase current is measured using the INA240. This test shows how the DRV8350R overcurrent protection works.

For this test setup the DRV8350R fault setup was generated as option 1 (phase to phase).

図 38. nFault Measurement at Overcurrent Condition Phase A to Phase C

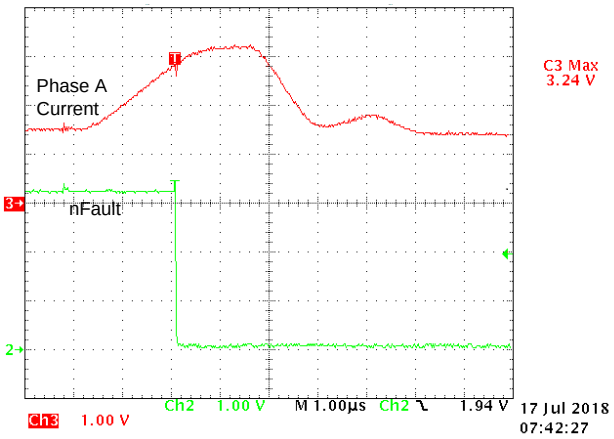


図 38 shows that the Vds fault is tripping at 26 A and it takes 2 µs until the FETs are set in high Z. This is illustrated using 表 2 and fits the considerations used when choosing the FETs.

For this test setup the DRV8350R fault setup was generated as option 2 (phase to GND).

図 39. nFault Measurement at Overcurrent Condition Phase A to GND

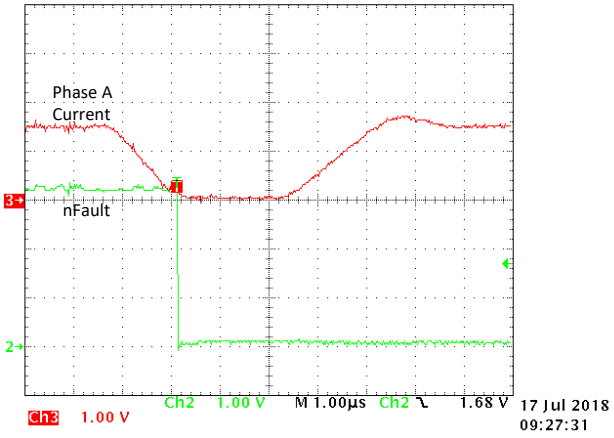


図 39 shows that the Vds fault is tripping at –26 A and it takes 2 µs until the FETs are set in high Z. This is illustrated using 表 2 in 2.2.1.2.

This shows that the fault condition gets tripped in both positive and negative current flow through the FET.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01629.

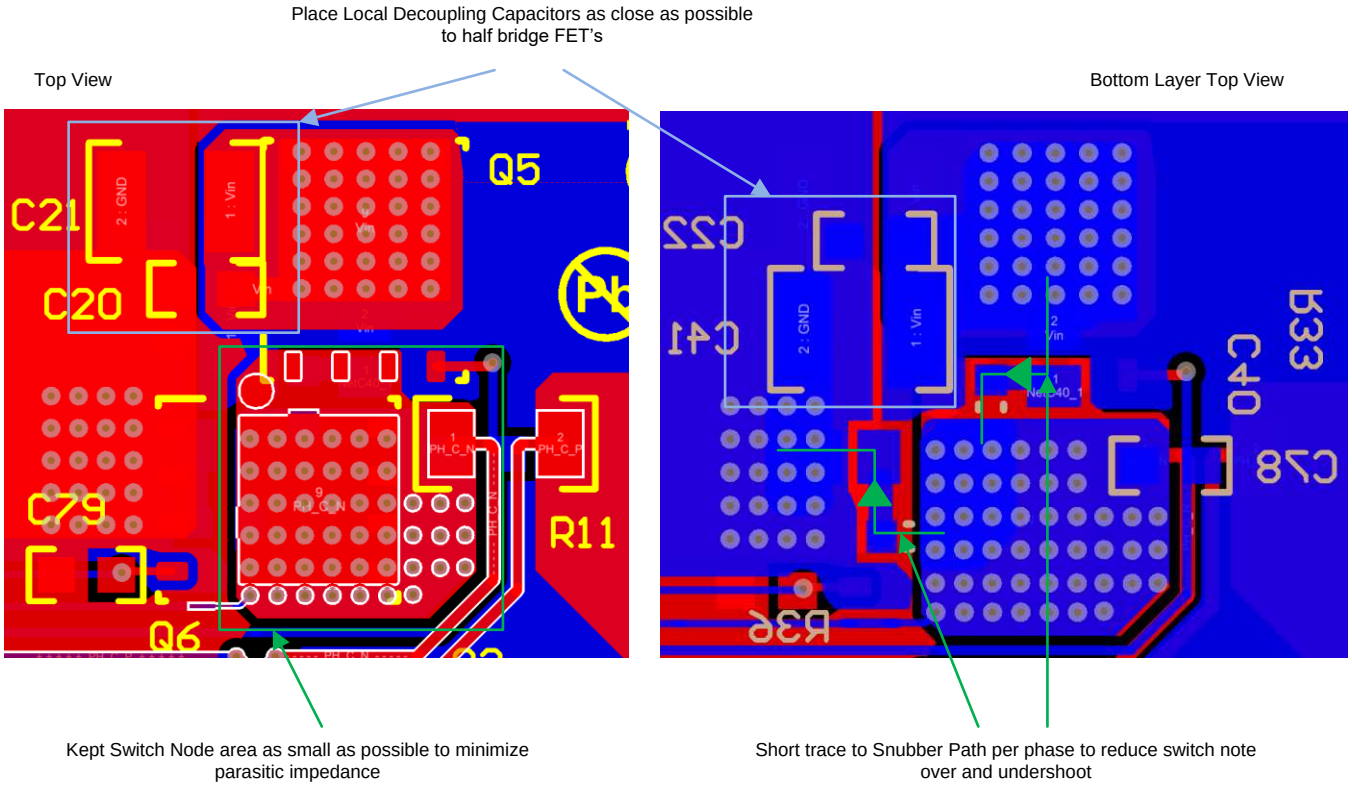
4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01629.

4.3 PCB Layout Recommendations

図 40 explains some layout guidelines for placing the FET's.

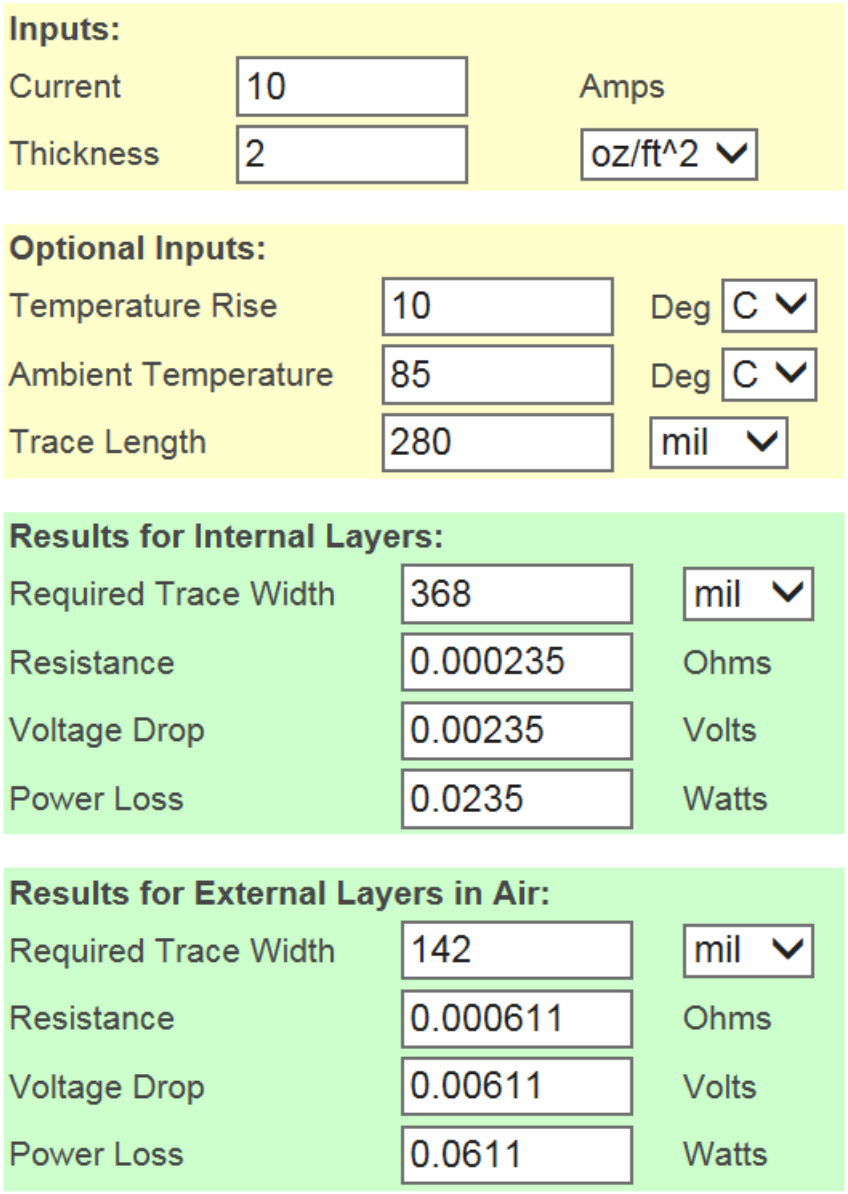
図 40. Considerations When Placing the Half Bridge FETs With Snubber and Decoupling Capacitors



Another consideration is what thickness copper is used for the design, this will also influence the thermal performance and also which type of pitch of the components can be used. Special care needs to be taken when doing the packet footprint that the distances can be built with the chosen copper thickness.

When the copper thickness is chosen it can also be defined how much temperature increase is wanted with the A_{RMS} used in the system, tools to show this can be found on the web. 図 41 shows an example used for this system. thickness. When

図 41. PCB Considerations When Routing High-Current Traces



4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01629.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-01629.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01629.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01629.

5 Software Files

To download the software files, see the design files at TIDA-01629.

6 Related Documentation

1. Texas Instruments, *DRV835x 100-V Three-Phase Smart Gate Driver*
2. Texas Instruments, *LM5008A 100-V 350-mA Constant On-Time Buck Switching Regulator*
3. Texas Instruments, *DesignDRIVE Development Kit IDDK v2.2 User's Guide*

6.1 商標

7 About the Author

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