参考資料

TI Designs: TIDA-00835
24ビットのデルタ-シグマADCを使用する、高精度±0.5%の電流および絶縁電圧測定のリファレンス・デザイン

TEXAS INSTRUMENTS

概要

このリファレンス・デザインは、ダイナミック・レンジが広い4チャネル、24ビット同時サンプリングの差動入力デルタ-シグマADCを使用して、正確な電圧および電流測定を行います。ADCは±2.5Vのバイポーラ入力を測定するよう構成されており、±4Vを測定できます。入力は、固定ゲイン・アンプを使用して、ADCの入力範囲である±2.5Vにスケーリングされます。このAFEは、共通の外部クロックとバッファを使用して2つのADCをチェーン接続することで、入力チャネルの数を8つに増やしており、すべての入力チャネルを同時にサンプリングできます。モジュールごとの測定チャネル数を増やすことで、システムの総コストを削減できます。さらに、TIDA-00810に示すように、診断機能もデザインに組み入れることができます。

リソース

TIDA-00835	デザイン・フォルダ
ADS131A04	プロダクト・フォルダ
ADS131A02	プロダクト・フォルダ
CDCLVC1102PW	プロダクト・フォルダ
OPA4180ID	プロダクト・フォルダ
AMC1301	プロダクト・フォルダ
ISO224	プロダクト・フォルダ
SN6501	プロダクト・フォルダ
TPS60403DBVR	プロダクト・フォルダ
TPS72325DBVT	プロダクト・フォルダ
TPS71733DCKR	プロダクト・フォルダ
TLV70450DBVR	プロダクト・フォルダ
LM27762	プロダクト・フォルダ
MSP432P401R	プロダクト・フォルダ
REF3425	プロダクト・フォルダ
REF3440	プロダクト・フォルダ
TLV9061	プロダクト・フォルダ
OPA4171	プロダクト・フォルダ
TVS0500	プロダクト・フォルダ

TI E2E™ Community　E2Eエキスパートに質問

特長

- データ収集
  - 4チャネルの同時サンプリング、24ビットのデルタ-シグマ(ADS131A04) ADCベースのAFEにより、広い範囲の入力を±0.5%以内の精度で測定
  - 2つのADC間の同期により、入力チャネルを拡張（合計8チャネル）
- アナログ入力
  - オンボードの負荷抵抗と外付けの変流器による入力電流測定
  - アクティブ・ハードウェア・インテグレータによりTIDA-00777 Rogowskiの出力に接続
  - 分圧器とAMC1301強化絶縁アンプ（従来の変圧器に代わる製品）を使用して、または絶縁なしで電圧測定
  - AMC1301の出力は、バイポーラ(±2.5V)用に構成されたADCと互換
- ホスト・インターフェイス用の±2.5V AVDD電源および3.3V DVDD電源に対応
- バイポーラ・モードで2.5Vまたは4Vの外部基準電圧に対応し、ダイナミック・レンジが拡大
- ARM® Cortex®-M4Fベースの低消費電力MCU (MSP432P401R)との接続

アプリケーション

- 保護リレー
- リモート端末ユニット、データ端末ユニット
- 電力品質解析
- ACB、MCCB

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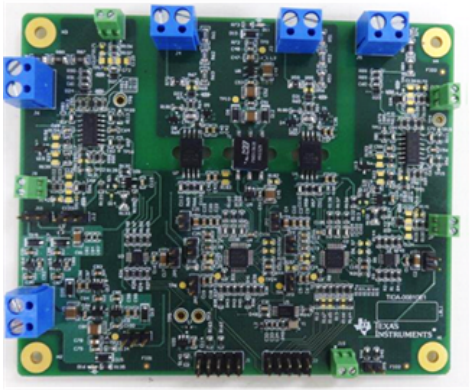

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1 System Overview

1.1 Protection Relay

Protection relays installed along power systems protect the primary equipment and customer loads (motors and busbar). Protection relays are used during generation, transmission, distribution, and at consumer locations. The features and complexities vary depending on the installation. Protection relays detect defective lines, apparatus, and other power system conditions of an abnormal or dangerous nature. Protection relays also initiate appropriate control over circuit action. Relays detect and locate faults by measuring electrical quantities in the power system, which are different during normal and intolerable conditions. The most important role of protection relays is to protect individuals first and then equipment.

Protection relays also minimize the damage and expense caused by insulation breakdowns (above overloads) called faults. These faults can occur as a result of deteriorated insulation or unforeseen events such as lightning strikes or power trips, caused by contact with trees and foliage. Protection relays are not required to operate during normal operation, but must immediately activate to handle intolerable system conditions. This immediate availability criterion is necessary to avoid serious outages and damages to portions of or the entire power network. In theory, a relay system must be able to respond to an infinite number of abnormalities that may occur within the network.

Protection relays are intelligent electronic devices (IEDs) that receive measured signals from the secondary side of current transformers (CTs) and voltage transformers (VTs). The relays detect whether or not the protected unit is in a stressed condition (based on the type and configuration of the unit). The protective relays send a trip signal to the circuit breakers to disconnect the faulty components from the power system if necessary.

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1.2 Introduction to Protection Relay and Subsystems for Grid Applications

図 1 shows a generic block diagram for a multifunction protection relay.

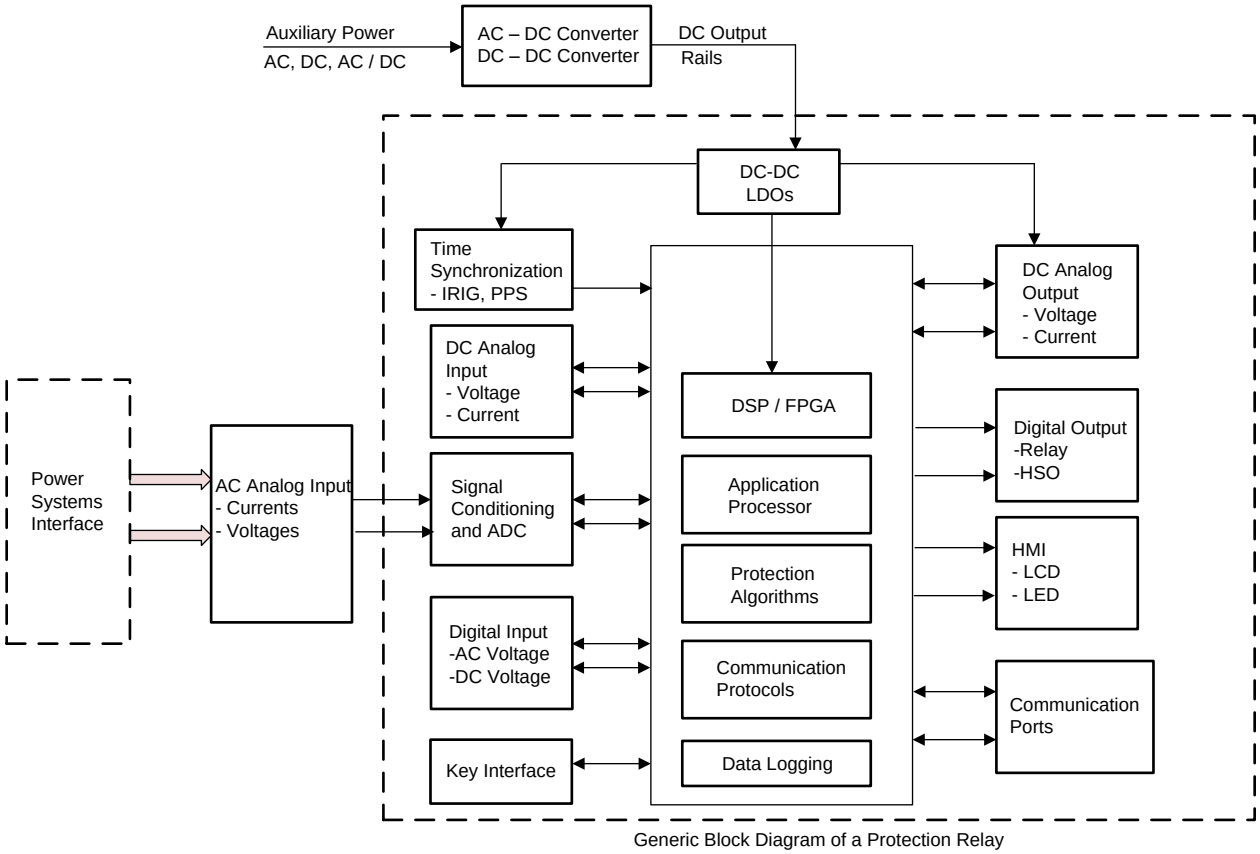

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図 1. General Block Diagram of Protection Relay

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Protective relays are categorized based on the equipment type protected such as generators, transmission lines, transformers, and loads. The protection relay, or IED, used in grid applications has the following generic subsystems, which are based on functionality:

- CPU or DSP module: This module handles all protection functions and logic, as well as the HMI and communication functions.
- Power supply
  - Nominal auxiliary voltage: 24-V DC, 48- to 60-V DC, 110- to 125-V DC, 220-V DC, and 230-V AC, 50 or 60 Hz, ±20%, and 40-W maximum admissible consumption
  - Stored energy for up to 50-ms power supply interruption
- AC measurement inputs
  - Nominal frequency (FNOM): 50 Hz or 60 Hz
  - Operating range: 45 Hz to 66 Hz
  - Accuracy: 0.2% F_S at FNOM
- CT measurements inputs
  - Nominal current: 1 or 5 A (IN)
  - Nominal consumption per phase: < 0.15 A at IN
  - Load rating: 20 A in continuous, 30 A for 3 sec, and 100 A for 1 sec
- VT measurements inputs
  - Nominal voltage: 57.7 to 500 V
  - Nominal consumption per phase: < 0.1 VA at 130 V
  - Maximum measurable voltage: 577 V_{RMS}
- DC analog input range (independently configurable)
  - ±1.25, ±2.5, ±5, and ±10 V
  - ±1, ±5, ±10, and ±20 mA
  - 0 to 1, 0 to 5, 0 to 10, 0 to 20, and 4 to 20 mA
- DC analog output range (independently configurable): ±5, ±10, ±20 mA, and 4 to 20 mA
- Digital inputs
  - Nominal voltage: 24-V DC, 48- to 60-V DC, 110- to 125-V DC or AC, 220-V DC or AC, ±20% or multi-voltage (24- to 250-V DC or AC)
  - Groups of 4, 8, 12, 16, or 32
- Digital output relays – Continuous current: 5 A
- Control output relays – Continuous current: 5 A
- Time synchronization by:
  - IRIG–B GPS clock (through the IRIG-B input)
  - Ethernet SNTP server
  - Time telegram message issued by remote SCADA (DNP3.0, IEC 60870-5-101, or IEC 60870-5-104)
- Communication capabilities – Ethernet communication
- 10BASE-TX and 100BASE-TX, auto-crossing, or 100BASE-FX

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- Protocols include UCA2 or IEC 61850, IEC 60870-5-104 (multi-client), or DNP3.0 IP
- Embedded Ethernet switch module with up to six ports (permitting a compact connection of various devices or I/O extensions) – Serial communication
- Up to two SCADA or four IED links per device
- SCADA protocol can be switched between DNP3.0, IEC 60870-5-101, and MODBUS
- IED protocol can be switched between DNP3.0, IEC 60870-5-103, MODBUS, and IEC 60870-5-101

This TI Design focuses on voltage and current input measurement using a high-resolution delta-sigma ADC.

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1.3 Voltage, Current, and Power Measurement of AFE

The AFE for measurement of AC voltage and current inputs consists of the following:

- Voltage input circuit with potential divider, signal conditioning, and interface to the ADC
- Current input circuit consists of burden resistors, signal conditioning, and interface to the ADC
- Signal condition circuit provides fixed or variable gain to the AC inputs and a common-mode DC level shift based on application to interface to the ADC.
- ADC for sampling the analog inputs includes multichannel inputs and high-resolution capable of sampling at > 80 samples (80 samples for protection and 256 samples for measurement as per IEC61850-9-2) per cycle.
- Interface to the MCU to process the sampled values includes an 32-bit ARM Cortex-M4F MCU and interconnection to the AFE.
- Power supply subsystem includes generation of required positive and negative power supplies.

Additional features of the AFE include:

- Measurement of a wide range of input currents and voltages
- Accurate measurement of AC parameters over the entire input range
- Isolated measurement of voltages using isolation amplifiers
- Measurement of increased number of channels

1.4 Accurate Measurement of AC Voltage, Current, and Power

Most of the current generation of multifunction protection relays provides power-measurement features. Protection relays are specified to measure wide input voltage and currents within a specified range of accuracy. To achieve wide dynamic input measurement within specified accuracy, ADC with PGA or a high-resolution ADC are used. In this design a 24-bit delta-sigma ADC is used.

1.5 Increasing Analog Input Channels

Depending on the protection relay configuration and application, the number of current and voltage channels varies from 4 to 16 channels. These 4 to 16 channels are realized by using multiple ADCs. If each ADC has separate interfaces, the complexity increases. Also, it may be necessary to synchronize multiple ADCs to ensure accuracy. The simplest way to interface multiple ADCs are daisy-chaining and using a common clock. In this design two ADCs are used. Each ADC has four channels. The ADCs are chained as a single interface and share a common clock.

1.6 Measurement of Voltages and Currents

Protection relay is used in HV, MV, and LV applications. Depending on the application the voltage levels are high, and during fault conditions high voltage levels damage the protection relay. The solution to this problem is isolating the voltage and current inputs. Voltages are isolated to provide user safety. The inputs can be isolated using analog isolation amplifiers or digitally using modulators. In this design, isolation amplifiers are used and the output of the isolation amplifiers is interfaced to the delta-sigma ADC.

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1.6.1 Current Transformer or Rogowski Inputs

Primary current is reduced to measurable secondary current by an external CT and applied to the protection relay. The protection relay has an internal CT to transform the secondary current to a measurable input current level. The advantage to using CTs is that they provide isolation, and no additional isolation is required on the protection relay when an internal CT is used.

1.6.2 Voltage Inputs

High-voltage inputs are connected to a PT and the secondary is connected to the input of the protection relay. Internally the protection relays have a potential transformer that can transform the input AC voltage into a measurable value. Potential transformers are large and have inherent nonlinearity, which is overcome by using a resistor divider. Resistor dividers do not provide isolation, as provided by the PT. Isolation amplifiers provide the required isolation when resistor dividers are used. Isolation amplifiers with either basic or reinforced isolation can be used based on the application. The solution using the resistor divider and isolation amplifier can be considered an alternative to the conventional potential transformer.

1.6.3 Alternative Methods for Interfacing Analog Inputs to ADC

ADS131A04 is a differential input. In applications where differential measurement is preferred consider the following solutions:

- THS4551: Low-noise, precision, 150-MHz, fully differential amplifier
- THS4541High-Speed Differential I/O Amplifier
- THS4531A: Ultra-low-power, RRO, fully differential amplifier

For cost-sensitive applications, sensor output can be directly interfaced to the differential input of the ADC. The performance must be evaluated with specific sensors for accuracy.

1.7 Key System Specifications

表 1 lists the key system specifications.

表 1. Specifications for Data Acquisition AFE

SERIAL NUMBER	PARAMETERS	DESCRIPTION	COMMENTS
1	ADC for measurement of analog inputs: • Type • resolution	Delta-sigma, 24-bit	Measurement accuracy ±0.5%
2	Number of analog inputs	Eight, two-chained, 4-channel ADCs	Both ADCs are synchronized with a common clock.
3	Non-isolated voltage input range	5 to 300 V with resistor divider and fixed-gain amplifier	Measurement accuracy ±0.5%
4	Isolated voltage input range	10- to 270-V AC AMC1301 isolation (reinforced) amplifier based	Measurement accuracy ±0.5%
		10- to 270-V AC AMC1200 isolation (basic) amplifier based	Measurement accuracy ±0.5%
5	Current input measurement range	0.25- to 100-A AC with fixed-gain amplifier	Measurement accuracy ±0.5%
6	ADC clock	16.384-MHz oscillator with two output clock buffer	—

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表 1. Specifications for Data Acquisition AFE (continued)

SERIAL NUMBER	PARAMETERS	DESCRIPTION	COMMENTS
7	Reference	Internal: • 2.442-V DC • 4-V DC	On power up, ADC defaults to external reference.
		External (optional): • 2.5- or 4.096-V DC	
8	Power supply for AFE	Positive • Digital : 3.3 V • Analog : 5 V, 2.5 V	Analog input voltage: VAVDD to VAVSS +5 V is used for unipolar input. VAVDD to VGND +2.5 V is used for bipolar input.
		Negative • Analog : –5 V, –2.5 V	VAVSS to VGND -2.5 V is used for bipolar input.
9	Isolated power	Positive • Analog : 5 V	—
10	Interface to MCU for delta-sigma	SPI™	See 3 for connection details.

1.8 Block Diagram

The high-performance AC analog input data acquisition AFE (see 図 2) has two 24-bit, delta-sigma ADCs chained to measure up to eight analog inputs. Potential dividers are provided to directly connect the AC voltage up to 300 V. Using isolation amplifiers provides the option to measure isolated voltage. The current and isolated voltage inputs have a fixed-gain front-end amplifier for adjusting the current measurement range, and the output of the amplifier is connected to the ADCs. The voltage and current inputs are measured as pseudo-differential inputs, and the voltage inputs from the isolation amplifier are measured as differential input. The positive and negative power supply required for the ADCs operation is generated from a single DC input, and provision to configure the power supply based on the input configuration is provided. Isolated power required for the operation of the isolation amplifier is also generated onboard.

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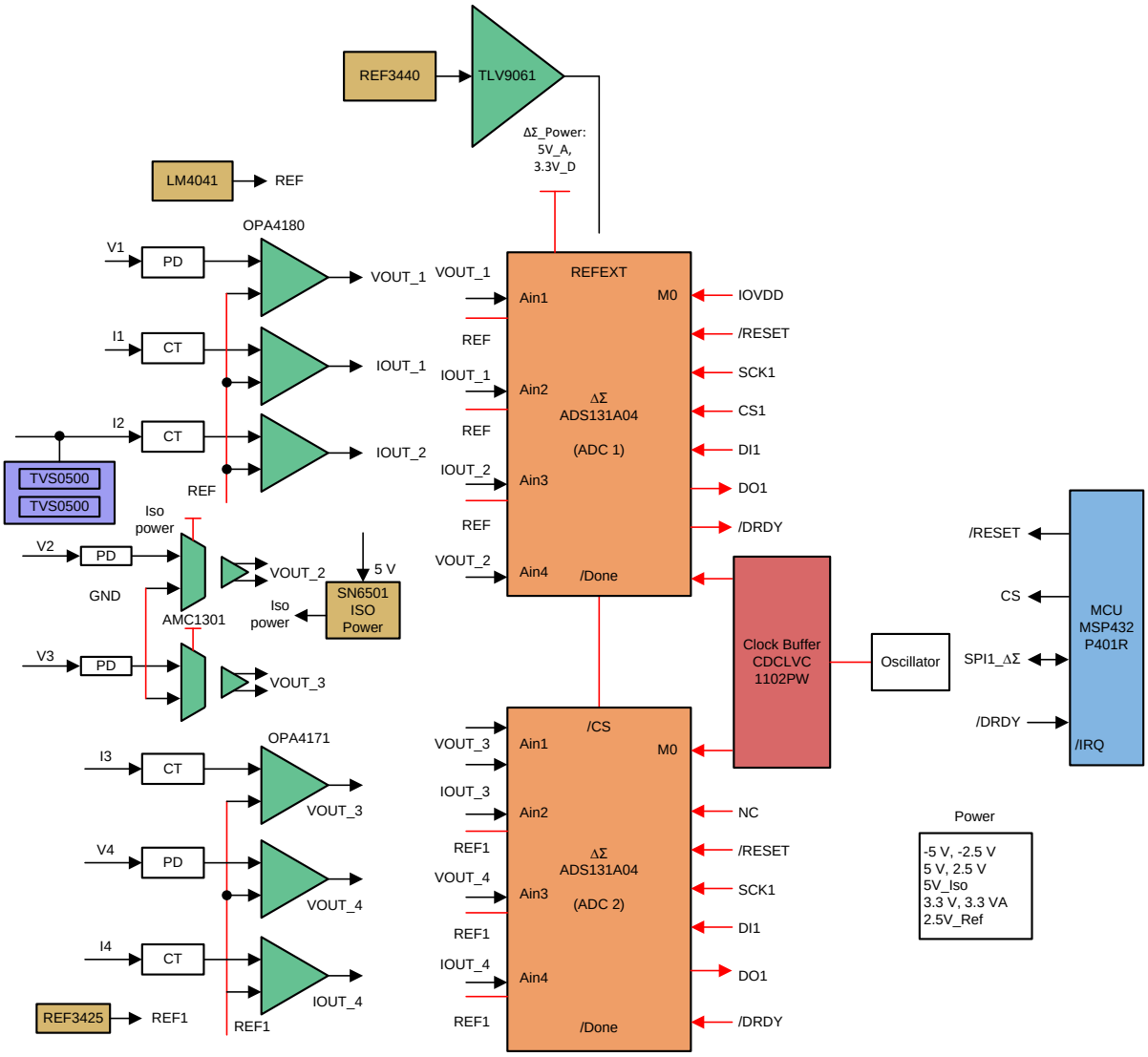

図 2. TIDA-00835 Block Diagram

1.8.1 Delta-Sigma ADC for Measurement

ADS131A04 is a 24-bit, four-channel, simultaneous-sampling differential ADC, used for measuring the analog input accurately over a wide range. Two ADCs are chained to be able to measure up to eight channels. A common clock oscillator of 16.384-MHz frequency and clock buffer CDCLVC1102PW are used for synchronizing the chained ADCs. The ADC analog power input is configurable from 0 to 5 V or ±2.5 V, based on the application and the input configuration. The isolated voltage output is connected differentially to the ADC. The current and non-isolated voltage gain amplifier outputs are connected in a pseudo-differential input configuration to the ADCs.

1.8.1.1 ADC Interface to MCU—MSP432P401R

Provision to interface the ADS131A04 to the MSP432P401R LaunchPad™ is provided onboard. The SPI signals the ADC reset, and the ADC data ready signals are interfaced to the MSP432™ LaunchPad. The ADC IOVDD is configured as asynchronous interrupt mode for communicating with the MSP432 MCU.

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In applications requiring higher memory for processing, MSP432P411Y SimpleLink Ultra-Low-Power 32-Bit Arm Cortex-M4F MCU with Precision ADC, 1MB Flash and 256KB RAM or MSP432P4011 SimpleLink Ultra-Low-Power 32-Bit Arm Cortex-M4F MCU with Precision ADC, 2MB Flash and 256KB RAM can be considered.

1.8.2 Signal Conditioning

1.8.2.1 Current and Non-Isolated Voltage Inputs (With Potential Divider)

The current inputs are connected to an external current transformer of accuracy class 0.1, and the secondary output is connected to the AFE. The transformer has a turns ration of 2000. The secondary of the current transformer is differentially connected to the signal conditioning circuit. The gain is provided using an accurate op amp OP4180 or OPA4171. The output of the gain amplifier is a single-ended output connected to the delta-sigma ADC.

AC voltage input up to 300 V can be directly connected to the AFE. The AFE has an onboard potential divider which divides the 300-V AC input into less than 1.5 V. An amplifier is used to provide a fixed gain and the output of the amplifier is connected to the ADC.

1.8.2.2 Isolated Voltage Input Using AMC1301

In applications which need reinforced isolation, TI recommends the AMC1301. The voltage input is applied across a potential divider and the potential divider output is connected to the AMC1301. The AMC1301 has an input range of ±250 mV. The output has a common-mode shift of 1.42 V with a 5-V supply and ×8.2 gain. The output of the AMC1301 is differentially connected to the ADC. The AMC1301 can be used in any of the ADS131A04 ADC configurations as follows:

- 0- to 5-V analog input
- ±2.5-V analog input

The AMC1301 output can also be interfaced to the MSP432 differential ADC input for cost optimized applications.

Alternatively in application with requirement for measuring higher input voltages, ISO224 ±12V Reinforced Isolated Amplifier for Voltage Sensing can be considered.

Find more information at the device's product page: http://www.ti.com/product/ISO224

1.8.2.3 Reference

The ADC internal reference is 2.442 V or 4 V. The ADC provides a reference output, which can be used for the AFE signal conditioning. The ADC reference is by default configured for external reference. The device must be configured to internal reference for the reference output to be active. Alternatively, for improved performance, an external 2.5-V or 4-V reference can be used to maximize dynamic range.

1.8.2.4 Analog Inputs Protection

The current inputs are protected against sensor opening by using two parallel resistors and TVS. Two of the TVS0500 connected back-to-back are used for overvoltage protection. The voltage inputs are protected for overvoltage, and multiple resistors are used as potential dividers for improved reliability. The potential divide input to the isolation amplifier is also protected for overvoltage. Additionally, the isolation amplifiers are protected for overvoltage.

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1.8.3 Power Supply

1.8.3.1 Non-Isolated Power

The ADS131A04 has flexible analog power-supply input options for operation as follows:

- Unipolar supply: 3.3 to 5.5 V
- Bipolar supply: ±2.5 V
- Digital supply: 1.65 to 3.6 V

The required power supplies are generated from a single 5.5-V input. The positive voltages generated are 5 V, 3.3 V, and 2.5 V, and the negative voltages generated are –5 V and –2.5 V. These voltages provide flexibility to operate the ADC in any required input configurations.

1.8.3.2 Isolated Power

The isolation amplifier operates with 5 V on the analog input side. The isolated power supply required is generated from 5 V on the digital side. The required isolated power is generated using the SN6501 transformer driver and LDO. The transformer for the isolated power has also been chosen with a dielectric voltage of > 5 kV_{RMS}.

Alternatively DCH010505S or DCH010505D Miniature, 1W, 3kVDC Isolated DC/DC Converters can be considered which simplifies the isolated power supply design.

Find more information at the device's product page: http://www.ti.com/product/DCH010505S

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2 System Design Theory

2.1 Delta-Sigma ADC for Analog Input Measurement

図 3 and 図 4 show two ADS131A04 devices in a chain configuration interfaced to the MCU.

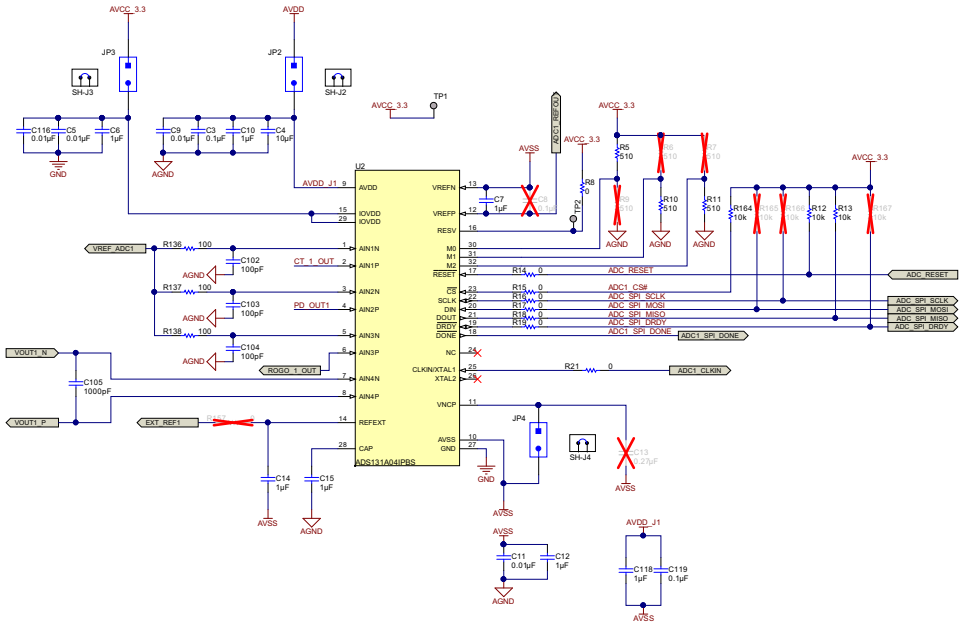

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図 3. Delta-Sigma ADC1 Configuration

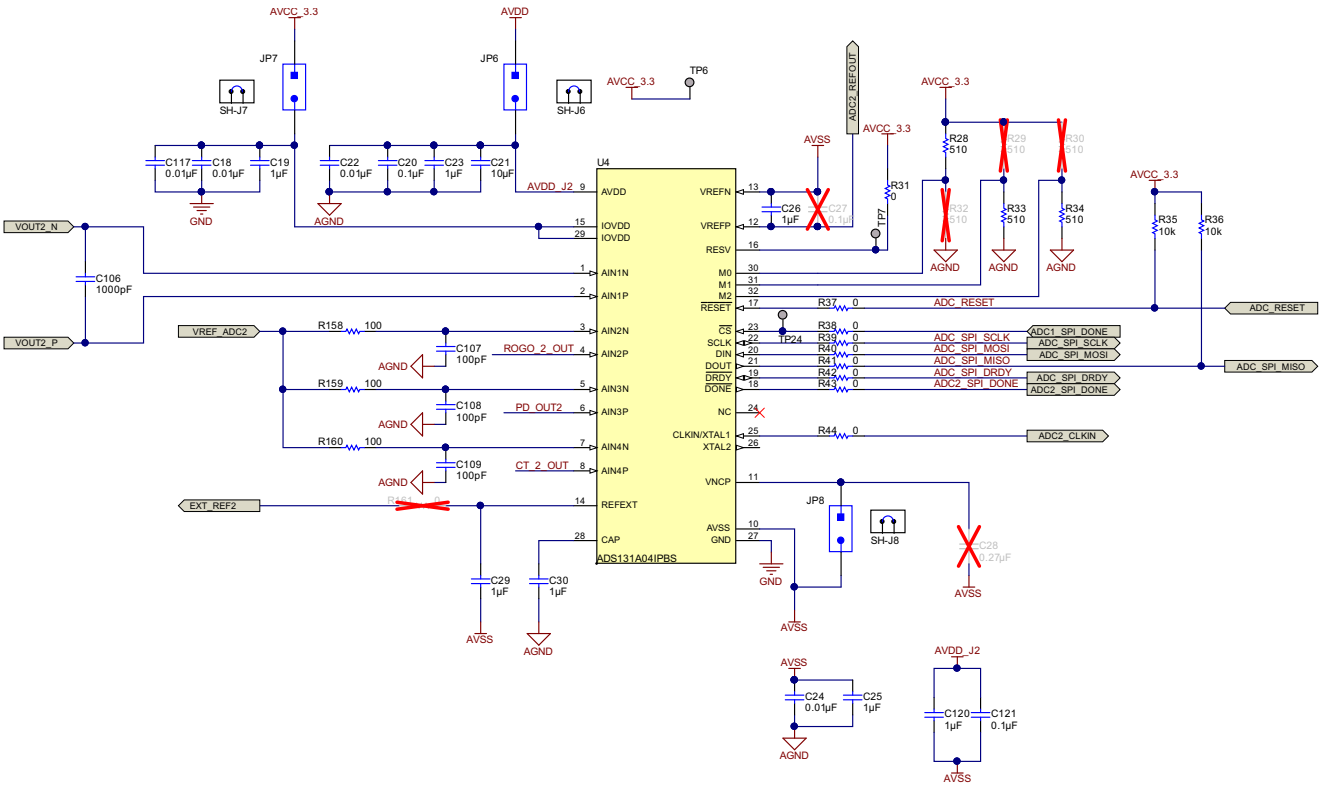

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図 4. Delta-Sigma ADC2 Configuration

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Two ADS131A04 ADCs are chained in this TI Design. The following inputs are connected:

- Current input
- Non-isolated voltage inputs
- Isolated amplifier output (isolated voltage)

The current inputs and the non-isolated voltage inputs are applied in a pseudo-differential configuration. The isolated voltage inputs are applied as differential inputs to the ADC. The ADC has an internal reference. The ADC is configured to use the internal ADC, and an external clock input is applied for operation.

Jumpers are provided for the following:

- AVDD: JP2 and JP6
- AVCC: JP7 and JP3
- Charge pump disable: JP4 and JP8

In the current design configuration the charge pump is disabled by mounting the jumpers. The power supply jumpers must also be mounted for proper operation.

For unipolar mode operation, an input of 0 to 5 V can be applied, and for bipolar input an ±2.5-V input can be applied. The M0, M1, and M2 pins are used to configure the ADC. The ADC is configured in asynchronous Interrupt mode in this design. Two devices have been chained to achieve eight inputs.

2.1.1 Delta-Sigma ADC—ADS131A04

The ADS131A04 is a four-channel, simultaneously sampling, 24-bit, delta-sigma ADC. The wide dynamic range, scalable data rates and internal fault monitors make the ADS131A04 ideally-suited for energy monitoring, protection, and control applications. Flexible power-supply options are available to maximize the effective number of bits (ENOB) for high dynamic range applications. Asynchronous and synchronous master and slave interface options are available, providing ADC configuration flexibility when chaining multiple devices in a single system.

Features:

- Four simultaneously sampling differential inputs
- Data rates up to 128 kSPS
- Noise performance
  - Single-channel accuracy better than 0.1% at 10000:1 dynamic range
  - ENOB: 19.1 bits at 8 kSPS
  - THD: –100 dB at 50 Hz and 60 Hz
- Integrated negative charge pump
- Flexible analog power-supply operation
  - Using negative charge pump: 3.0 to 3.45 V
  - Unipolar supply: 3.3 to 5.5 V
  - Bipolar supply: ±2.5 V
- Digital supply: 1.65 to 3.6 V
- Low-drift internal voltage reference: 4 ppm/°C
- ADC self checks

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- Cyclic redundancy check (CRC) and hamming code error correction on communications
- Multiple SPI data interface modes
  - Asynchronous interrupt
  - Synchronous master and slave
- Package: 32-pin TQFP
- Operating temperature range: –40°C to 125°C

Find more information at the device's product page: http://www.ti.com/product/ADS131A04

注: The ADS131A02 2-Channel AFE can be considered in single-phase applications.

2.1.2 Clock Buffer CDCLVC1102PW

Two ADCs are used in this TI Design. To synchronize the sampling of the two ADCs the same clock is applied to both. A 16.348-MHz oscillator is to generate the clock. The clock output is buffered using a clock buffer (see 図 5).

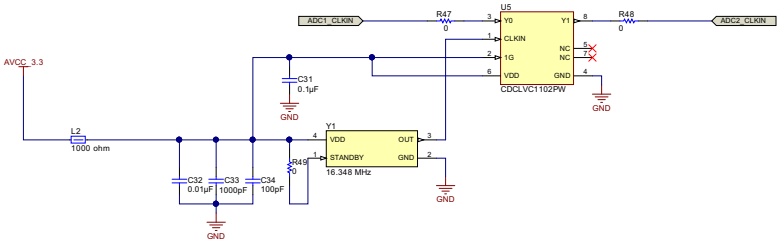

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図 5. Clock Buffer for Delta-Sigma ADCs

The CDCLVC11xx is a modular, high-performance, low-skew, general-purpose clock buffer family from TI. Seven different fan-out variations, 1:2 to 1:12, are available. All of the devices are pin compatible to each other for easy handling. All family members share the same high-performing characteristics such as low-additive jitter, low skew, and wide operating temperature range.

Features:

- High-performance LVCMOS clock buffer family
- Very low pin-to-pin skew < 50 ps
- Very low additive jitter < 100 fs
- Supply voltage: 3.3 V or 2.5 V
- f_{max} = 250 MHz for 3.3 V
- f_{max} = 180 MHz for 2.5 V
- Operating temperature range: –40°C to 85°C

表 2 lists the CDCLVC1102PWR features.

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表 2. CDCLVC1102PWR Features

PARAMETER	DETAILS
Part number	CDCLVC1102PWR
Description	IC CLK BUFFER 1:2 250-MHZ 8TSSOP
Type	Fan-out buffer (distribution)
Number of circuits	1
Ratio—input:output	1:2
Differential—input:output	No / no
Input	LVCMOS
Output	LVCMOS
Voltage supply	2.3 to 3.6 V
Mounting type	Surface mount
Supplier device package	8-TSSOP

Find more information at the device's product page: http://www.ti.com/product/CDCLVC1102

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2.1.3 Delta-Sigma to ADC Interface to MCU—MSP432P401R

Delta-sigma ADCs are interfaced to the MCU MSP432F401R through the SPI. The interface signals required from the ADC are terminated to connector J2. Resetting the ADC is critical. Follow the instructions in Section 9.4.5 Reset (RESET) of the data sheet (SBAS590B) to reset the ADC during initialization. 図 6 shows the Delta-Sigma ADC to MSP432 interface connector.

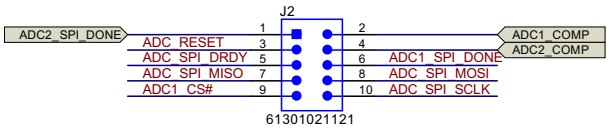

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図 6. Delta-Sigma ADC to MSP432 Interface Connector

The MSP432P401x device family is TI's latest addition to its portfolio of efficient ultra-low-power mixed-signal MCUs. The MSP432P401x family features the ARM Cortex-M4 processor in a wide configuration of device options, including a rich set of analog, timing, and communication peripherals, thereby catering to a large number of application scenarios where both efficient data processing and enhanced low-power operation are paramount.

Features:

- Core
  - ARM 32-bit Cortex-M4F CPU with floating-point unit and memory protection unit
  - Frequency up to 48 MHz
  - Performance benchmark:
    - 1.196 DMIPS/MHz (Dhrystone 2.1)
    - 3.41 CoreMark/MHz
  - Energy Benchmark: 167.4 ULPBench score
- Memory
  - Up to 256KB of flash main memory (simultaneous read and execute during program or erase)
  - 16KB of flash information memory
  - Up to 64KB of SRAM (including 8KB of backup memory)
  - 32KB of ROM with MSPWare driver libraries
- Operating Characteristics
  - Wide supply voltage range: 1.62 to 3.7 V
  - Temperature range (ambient): –40°C to 85°C
- Serial communication
  - Up to four eUSCI_A modules
    - UART with automatic baud-rate detection
    - IrDA encode and decode
    - SPI (up to 16 Mbps)
- Flexible I/O features
  - Ultra-low-leakage I/Os (±20-nA maximum)

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- Up to four high-drive I/Os (20-mA capability)
- All I/Os have capacitive touch capability
- Up to 48 I/Os with interrupt and wake-up capability
- Up to 24 I/Os with port mapping capability
- Eight I/Os with glitch filtering capability

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- Advanced low-power analog features
  - 14-bit, 1-MSPS SAR ADC
  - Internal voltage reference with 10-ppm/°C typical stability
  - Two analog comparators

Find more information at the device's product page: http://www.ti.com/product/MSP432P401R

2.1.3.1 MSP432P401R LaunchPad

The MSP432P401R LaunchPad lets users develop high-performance applications which benefit from low-power operation. The LaunchPad features the MSP432P401R, which includes the following:

- 48-MHz ARM Cortex-M4F
- 95 µA/MHz active power
- 850-nA RTC operation
- 14-bit 1-MSPS differential SAR ADC
- AES256 accelerator

This LaunchPad includes an onboard emulator with EnergyTrace™+ technology, which means users can program and debug their projects without the need for additional tools, while also measuring total system energy consumption. All pins of the MSP-EXP432P401R device are fanned out for easy access.

2.1.4 Chaining of Multiple Delta-Sigma ADCs

In this TI Design, two ADS131A04 devices have been chained to increase the number of analog channels. The ADS131A04 lets the designer add channels by adding an additional device to the bus. The first device in the chain can be configured using any of the interface modes. All subsequent devices must be configured in synchronous slave mode. In all cases, however, the chain of ADS131A04 devices appear as a single device with extra channels, with the exception that each device sends individual status and data integrity words. In this manner, no additional pins on the host are required for an additional device on the chain. The only special provisions required in the interface is to extend the frame to the appropriate length.

The first device is configured in asynchronous interrupt mode. 図 7 shows a multiple-device configuration where the first device is configured in asynchronous interrupt mode as noted by the state of the M0 pin. The second ADS131A0x device and any additional devices are configured in synchronous slave mode.

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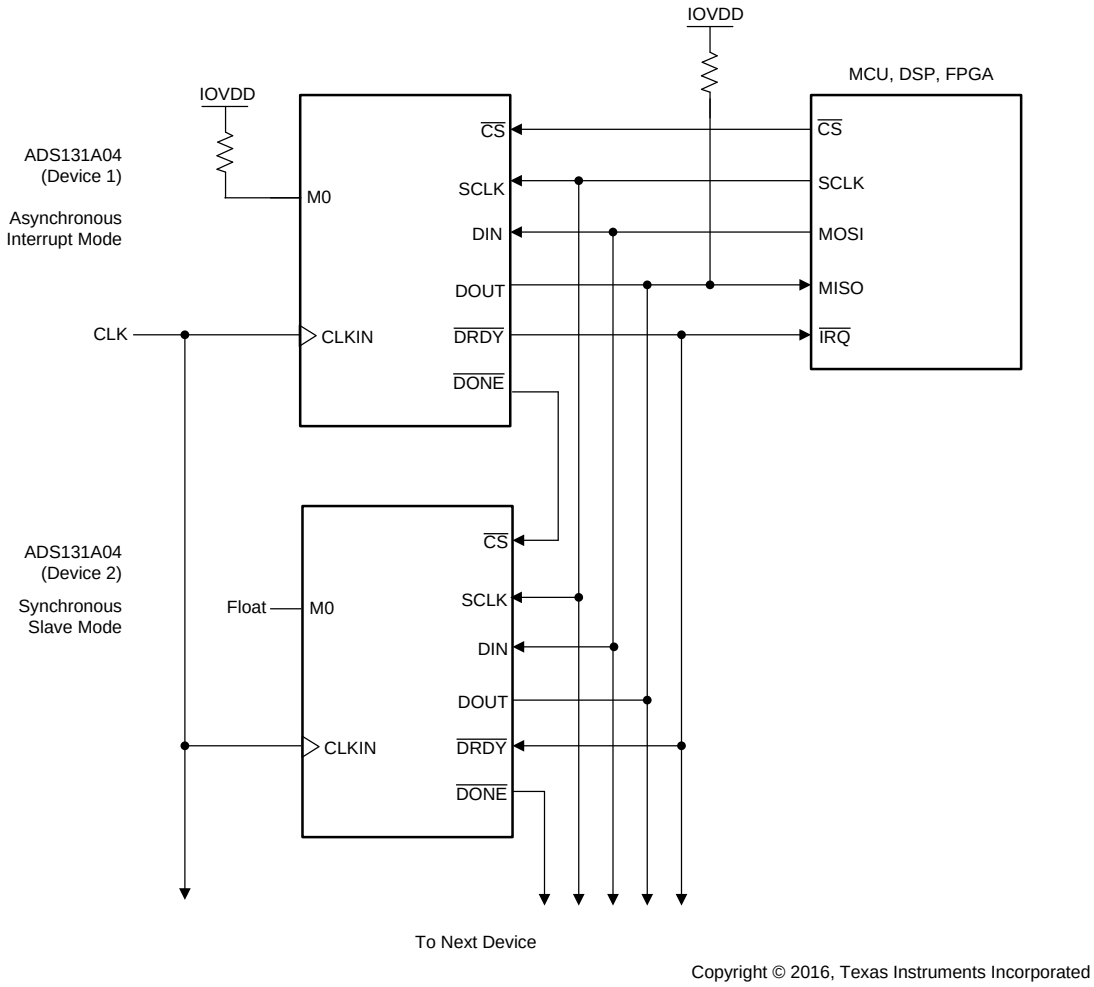

図 7. Multiple Device Configuration Using Asynchronous Interrupt Mode

See Section 10.1.3 of the data sheet *Chaining for Multiple Device Configuration* (SBAS590) for more information on chaining multiple devices.

2.1.5 Connecting External Reference to ADC1 and ADC2

External reference of 2.5 V or 4 V can be connected to the ADC based on the required input range. Provision to connect REF3425 or REF3440 has been provided in the design. The output of the reference is buffered using TLV9061 operational amplifiers and connected to ADC1 and ADC2.

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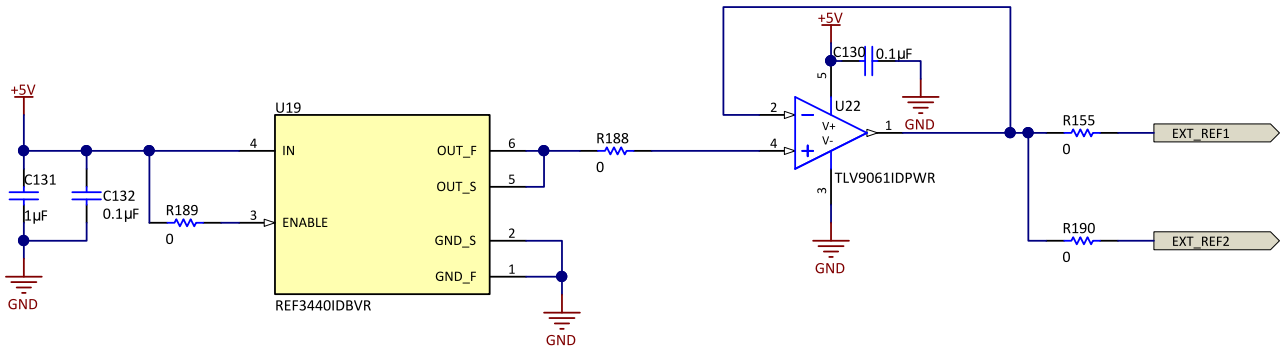

図 8. External Reference for ADC1 and ADC2

The REF34xx is a low temperature drift (6 ppm/°C), low-power, high-precision CMOS voltage reference, featuring ±0.05% initial accuracy, low operating current with power consumption less than 95 µA. This device also offers very low output noise of 3.8 µVp-p /V, which enables its ability to maintain high signal integrity with high-resolution data converters in noise critical systems. Stability and system reliability are further improved by the low output-voltage hysteresis of the device and low long-term output voltage drift.

Find more information at the device's product page: http://www.ti.com/product/REF3440 and http://www.ti.com/product/REF3425

TLV9061, is a single (1.8 V to 5.5 V) 10MHz operational amplifiers (op amps) with rail-to-rail input- and output-swing capabilities. These devices are highly cost-effective solutions for applications where low-voltage operation, a small footprint, and high capacitive load drive are required.

Find more information at the device's product page: http://www.ti.com/product/TLV9061

2.2 Signal Conditioning With Op-amp OPA4180 or OPA4171

The Signal condition for the voltage and current inputs can be implemented using OPA4180 or OPA4171.

The OPA4180 operational amplifiers use zero-drift techniques to simultaneously provide low-offset voltage (75 µV), and near zero-drift over time and temperature. These miniature, high-precision, low-quiescent current amplifiers provide high-input impedance and rail-to-rail output swing within 18 mV of the rails. The input common-mode range includes the negative rail. Either single or dual supplies can be used in the range of 4 to 36 V (±2 to ±18 V). The quad is offered in SOIC-14 and TSSOP-14 packages. All versions are specified for operation from –40°C to 105°C.

Features:

- Low offset voltage: 75 µV (maximum)
- Zero-drift: 0.1 µV / °C
- Low noise: 10 nV / √Hz
- Very low 1 / f noise
- Excellent DC precision:
  - PSRR: 126 dB
  - CMRR: 114 dB
  - Open-loop gain (AOL): 120 dB
- Quiescent current: 525 µA (maximum)

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- Wide supply range: ±2 to ±18 V
- Rail-to-rail output: input includes negative rail
- Low bias current: 250 pA (typical)
- RFI filtered inputs

Find more information at the device's product page: http://www.ti.com/product/OPA4180

Alternatively, for cost-sensitive applications, the OPA4171 can be used. The OPA4171 is a 36-V, single-supply, low-noise operational amplifier with the ability to operate on supplies ranging from 2.7 V (±1.35 V) to 36 V (±18 V). These devices offer low offset, drift, and bandwidth with low quiescent current. The OPA4171 family is specified from 2.7 to 36 V. Input signals beyond the supply rails do not cause phase reversal.

Find more information at the device's product page: http://www.ti.com/product/OPA4171

2.2.1 Current Inputs

図 9 shows the current input scaling amplifiers for four input currents.

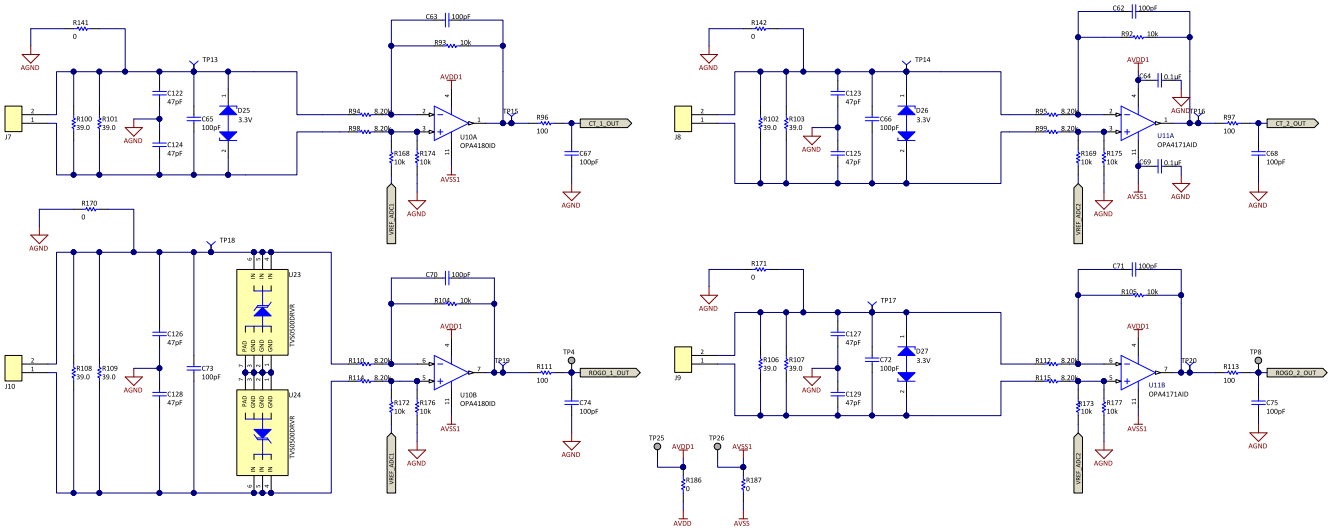

図 9. Current Input Connectors with Gain Amplifiers and Flat clamp TVS protection

This design provides provision to measure up to four current inputs. Two current channels are provided for each ADC. An external CT is used to step down the primary current. The CT ratio used in this design is 1:2000. The secondary current is connected as input to a fixed-gain amplifier. The amplifier is configured in differential mode and depending on the application and the input voltage range the gain can be configured. The output of the amplifier is connected to the delta-sigma ADC for measurement. The burden required for converting the current input to voltage is provided onboard.

表 3 lists the current input range calculation.

表 3. Calculation of Current Input Range

CURRENT MEASUREMENT	VALUE	UNIT
Burden	19.5000	Ω
Gain	1.2195	—
RF	10.0000	KΩ

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表 3. Calculation of Current Input Range (continued)

CURRENT MEASUREMENT	VALUE	UNIT
RI	8.2000	KΩ
Op amp rail	2300.0000	mV
Op amp output	1886.0000	mV (PK)
CT sec current	68.4002	mA
CT ratio	2000	—
Primary current	136.8005	A

The output of the TIDA-00777 can be connected to the current inputs designated Rogo_1_out and Rogo2_Out. The TIDA-00777 output is compatible to the ADS131A04 output when configured for a 2.442-V reference. To connect the Rogowski inputs, make the following changes:

1. Remove R111, R113, C74, and C75.
2. Connect current inputs to TP4 and TP6.

注: Ensure the ground of the two boards are connected together.

The current transformer inputs are protected against overvoltage using a TVS diode. An alternative approach for protection is to use the flat-clamp TVS diode TVS0500 connected in back-to-back configuration for bi-directional protection.

Find more information at the device's product page: http://www.ti.com/product/TVS0500

2.2.2 Non-Isolated Voltage Inputs (With Potential Divider)

図 10 shows voltage input scaling amplifiers for two non-isolated voltage inputs.

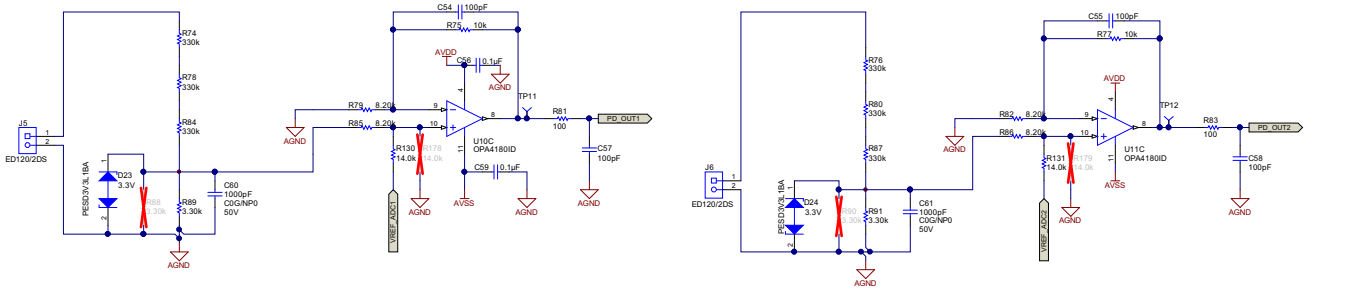

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図 10. Voltage Input Signal Conditioning

This design provides the option to measure two non-isolated voltage inputs. One input is provided on each ADC. The AC input can be directly applied across the potential divider provided onboard. The output of the potential divider is connected to a fixed-gain amplifier. The amplifier is configured in differential mode and depending on the application and the input voltage range, the gain can be configured. The output of the gain amplifier is connected to the ADC input.

表 4 lists the input range calculation for the non-isolated voltage input.

表 4. Input Range for Non-Isolated Voltage Input

VOLTAGE MEASUREMENT _PD	VALUE	UNIT
PD	993.3000	KΩ
Gain	1.2195	—

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表 4. Input Range for Non-Isolated Voltage Input (continued)

VOLTAGE MEASUREMENT _PD	VALUE	UNIT
RF	10.0000	KΩ
RI	8.2000	KΩ
Op amp rail	2300.0000	mV
Op amp input	1886.0000	mV (PK)
Op amp input	1333.8048	mV (RMS)
Voltage division ratio	301.0000	—
Primary voltage	401.4752	V

注: The OPA4188 can be consider for applications requiring improved accuracy performance.

2.2.3 Isolated Voltage Input Using AMC1301

図 11 shows the isolation amplifiers for voltage input.

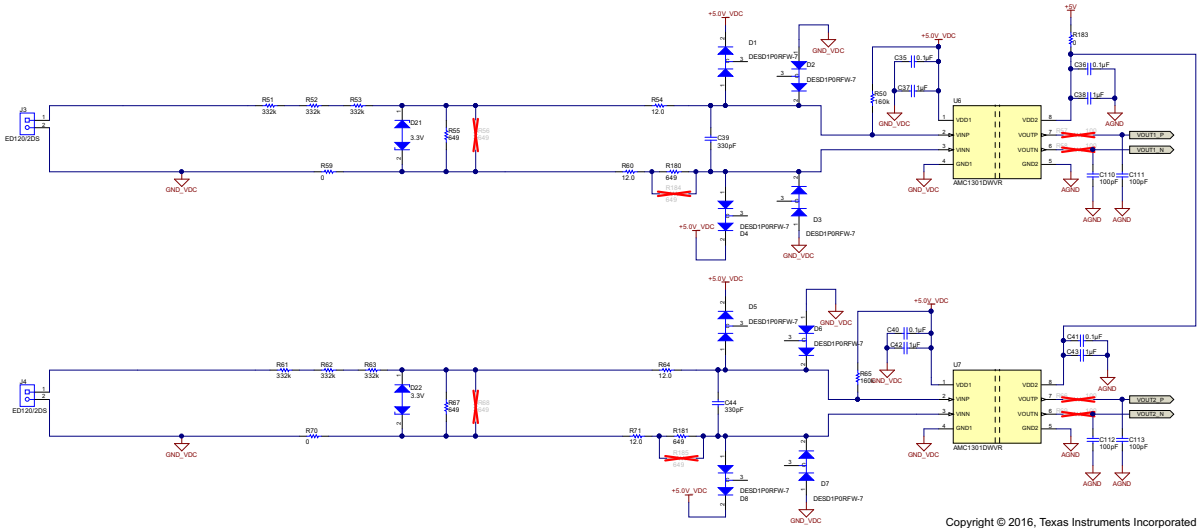

図 11. Isolation Amplifier With Input Protection and Potential Divider

The AMC1301 is a precision, isolated amplifier with an output separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced galvanic isolation of up to 7 kV_{PEAK} according to VDE-V 0884-10 and UL1577. Used with isolated power supplies, this device prevents noise currents on a high common-mode voltage line from entering the local ground and interfering with or damaging sensitive circuitry. The integrated common-mode overvoltage and missing high-side supply voltage detection features of the AMC1301 simplify system-level design and diagnostics. The AMC1301 is fully specified over the extended industrial temperature range of –40°C to 125°C and is available in a wide-body, 8-pin, SOIC (DWV) package.

Features:

- ±250-mV input voltage range optimized for current measurement using shunt resistors
- Low offset error and drift:
  - ±200 µV (maximum) at 25°C
  - ±3 µV/°C (maximum)

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- Fixed gain: 8.2
- Very low gain error and drift:
  - ±0.3% (maximum) at 25°C
  - ±50 ppm/°C (maximum)
- Very low nonlinearity and drift:
  - 0.03% (maximum)
  - 1 ppm/°C (typical)
- 3.3-V operation on high-side and low-side
- System-level diagnostic features
- Safety and regulatory approvals:
  - 7000-V_{PK} reinforced isolation per DIN V VDE-V 0884-10 (VDE-V 0884-10): 2006-12
  - 5000-V_{RMS} isolation for 1 minute per UL1577
  - CAN/CSA No. 5A-component acceptance service notice, IEC 60950-1, and IEC 60065 end equipment standards
- Fully specified over the extended industrial temperature range

Find more information at the device's product page: http://www.ti.com/product/AMC1301

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This design provides the option to measure two isolated voltage inputs. The isolation amplifier is used to provide the required analog isolation. The isolator provides reinforced isolation with a fixed gain of ×8.2. The common-mode output of the isolation amplifier is 1.44 V. The advantage of the AMC1301 is that it can be used with the ADC configured for unipolar inputs (0 to 5 V) and bipolar inputs ±2.5 V. The AMC1301 can also be used with a 2.442-V and 4-V reference. The AC input is specified to be linear up to a ±250-mV input. The output of isolation amplifier is differentially connected to the ADC. The required protection for input overvoltage is provided.

表 5 lists the input range calculation for the AMC1301.

表 5. Input Voltage Range Calculation for AMC1301

VOLTAGE MEASUREMENT_ISO Amp_AMC1301	VALUE	UNIT
PD	996.6500	KΩ
Gain	8.2000	—
Output Peak	2.0500	—
Output RMS	1.4498	V
Input	0.1768	V
Voltage division ratio	1533.0000	—
Primary voltage	271.0396	V

2.2.4 Reference—LM4040 and Buffer (For Common-Mode DC Level Shift)

The reference and buffers are used to provide the required DC common-mode level shifting for using the ADC range (see 図 12).

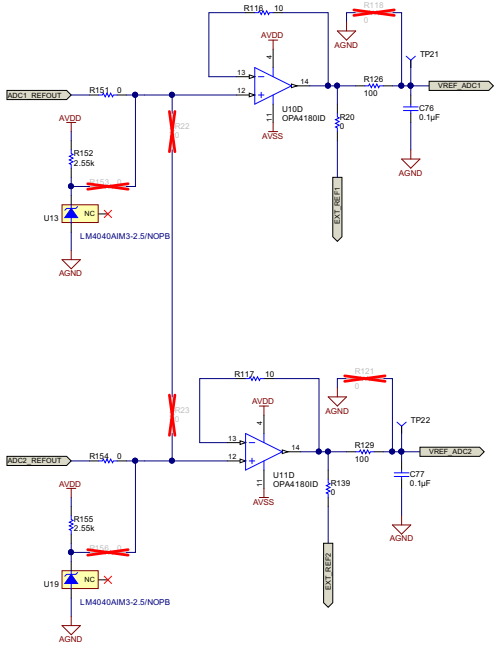

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図 12. Reference With Buffer for Gain Amplifiers

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The LM4040-N precision voltage reference is available in an SOT-23 surface-mount package. The advanced design of the LM4040-N eliminates the need for an external stabilizing capacitor while ensuring stability with any capacitive load, making the LM4040-N easy to use. The minimum operating current increases from 60 µA for the 2.5-V LM4040-N to 100 µA for the 10-V LM4040-N. All versions have a maximum operating current of 15 mA. The LM4040-N uses a fuse and Zener-zap reverse breakdown voltage trim during wafer sort to ensure that the prime parts have an accuracy of better than ±0.1% (A grade) at 25°C. Curvature correction for bandgap reference temperature drift and low dynamic impedance ensure stable reverse breakdown voltage accuracy over a wide range of operating temperatures and currents.

Features:

- No output capacitor required
- Tolerates capacitive loads
- Key specifications (2.5-V LM4040-N)
  - Output voltage tolerance (A grade, 25°C): ±0.1% (maximum)
  - Low output noise (10 Hz to 10 kHz): 35 μV_{RMS} (typical)
  - Wide operating current range: 60 µA to 15 mA
  - Low temperature coefficient: 100 ppm/°C (maximum)

表 6 lists the LM4040 external reference specifications.

表 6. LM4040 Features

PARAMETER	DETAILS
Part number	LM4040AIM3-2.5 / NOPB
Reference type	Shunt
Output type	Fixed
Voltage output (minimum / fixed)	2.5 V
Current output	15 mA
Tolerance	±0.1%
Temperature coefficient	100 ppm/°C
Noise: 10 Hz to 10 kHz	35 µVrms
Current cathode	65 µA
Supplier device package	SOT-23-3

The delta-sigma ADC operates with unipolar input or bipolar inputs. For bipolar inputs the reference is zero, and for unipolar input the reference must be shifted—typically, the input range is 2. The amplifier outputs are level shifted depending on the input configuration. The references can be configured as follows:

- ADC REFP out for DC level shifting the analog input
  - R151 and R154 mounted
  - R153 and R156 not mounted
- External reference for DC level shifting the analog input
  - R153 and R156 mounted
  - R151 and R154 not mounted

Based on the power supply configuration, the reference output to the op amp gain amplifier can be selected as follows:

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- 0-V reference
  - R118 and R121 mounted
  - R126 and R129 not mounted
- 2.5-V reference
  - R126 and R129 mounted
  - R118 and R121 not mounted

2.3 Power Supply

The delta-sigma ADC has flexible analog power-supply options for operation as follows:

- Unipolar supply: 3.3 to 5.5 V
- Bipolar supply: ±2.5 V
- Digital supply: 1.65 to 3.6 V

The power supply required to operate the ADC is provided onboard (see 図 13). The power supply operates from a single positive input voltage. The required negative power supply is generated using high-efficiency input inverters and negative LDOs. The required overvoltage protection has been provided using Zener diodes. Jumpers J11, J12, and J14 are used to configure the ADC analog supply input range.

Alternatively LM27762 Low-Noise Positive- and Negative-Output Charge Pump With Integrated LDO can be considered simplifying power supply design.

Find more information at the device's product page: http://www.ti.com/product/LM27762

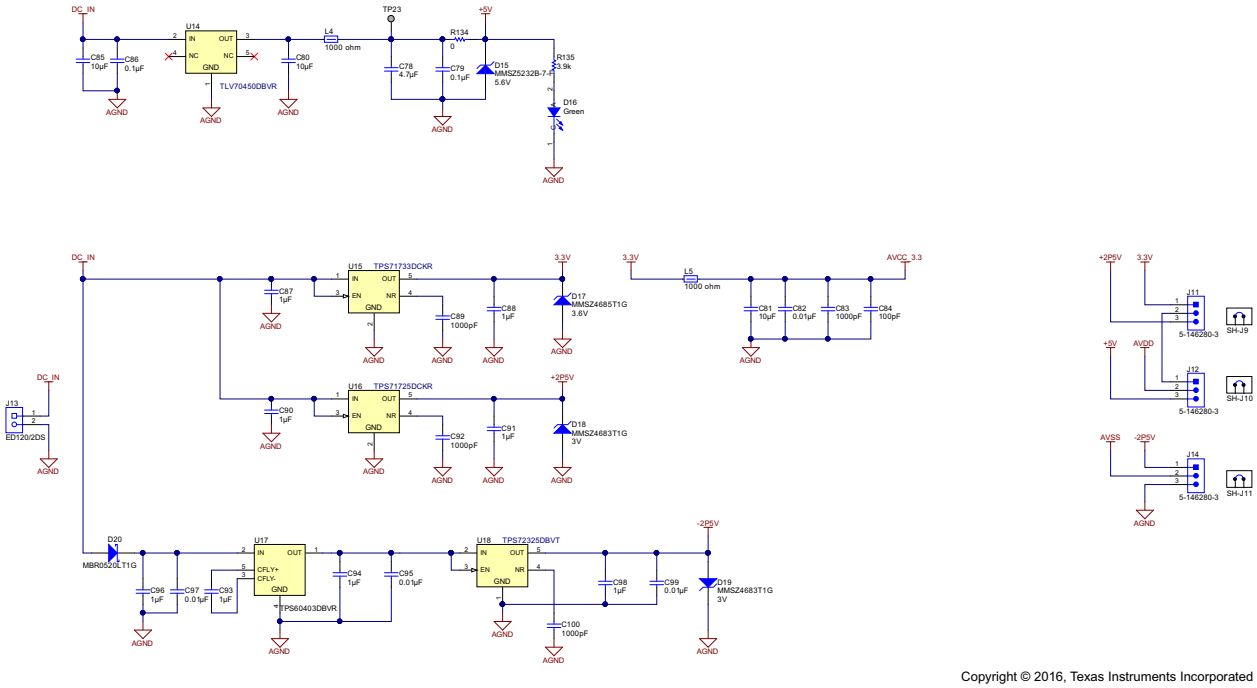

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図 13. Onboard Positive and Negative Power Supply With Protection

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2.3.1 Non-Isolated Power

2.3.1.1 +5 V (U14)

The TLV704 series of LDO regulators are ultra-low quiescent current devices designed for extremely power-sensitive applications. Quiescent current is virtually constant over the complete load current and ambient temperature range. These devices are an ideal power-management attachment for low-power MCUs, such as the MSP430. The TLV704 operates over a wide operating input voltage of 2.5 to 24 V. Therefore, the device is an excellent choice for battery-powered systems and industrial applications that undergo large line transients.

Features:

- Wide input voltage range: 2.5 to 24 V
- Low 3.2-µA quiescent current
- Ground pin current: 3.4 µA at 100-mA I_{OUT}
- Stable with a low-ESR, 1-µF, typical output capacitor

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表 7 lists the TLV70450 features.

表 7. TLV70450 LDO Features

PARAMETER	DETAILS
Part number	TLV70450DBVR
Regulator topology	Positive fixed
Voltage output	5 V
Current output	150 mA
Voltage dropout (typical)	0.85 V at 100 mA
Number of regulators	1
Voltage input	Up to 24 V
Current limit (minimum)	160 mA
Operating temperature	–40°C to 125°C
Supplier device package	SOT-23-5

2.3.1.2 +3.3 V (U15)

The TPS717xx family of LDOs, low-power linear regulators, offers very high-power supply rejection (PSRR) while maintaining very low 45-µA ground current in an ultra-small, 5-pin, SOT package. The family uses an advanced BiCMOS process and a PMOS pass device to achieve fast start-up, very low noise, excellent transient response, and excellent PSRR performance. The TPS717xx is stable with a 1-µF ceramic output capacitor and uses a precision voltage reference and feedback loop to achieve a worst-case accuracy of 3% overall load, line, process, and temperature variations.

Features:

- Input voltage: 2.5 to 6.5 V
- Available in multiple output versions:
  - Fixed output with voltages from 0.9 to 5 V
  - Adjustable output voltage from 0.9 to 6.2 V
- Ultra-high PSRR:
  - 70 dB at 1 kHz
  - 67 dB at 100 kHz
  - 45 dB at 1 MHz
- Excellent load and line transient response
- Very LDO: 170 mV typical at 150 mA
- Low noise: 30 μV_{RMS} typical (100 Hz to 100 kHz)

表 8 lists the TPS71733 LDO features.

表 8. TPS71733 LDO Features

PARAMETER	DETAILS
Part number	TPS71733DCKR
Regulator topology	Positive fixed
Voltage output	3.3 V
Current output	150 mA
Voltage dropout (typical)	0.17 V at 150 mA

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表 8. TPS71733 LDO Features (continued)

PARAMETER	DETAILS
Number of regulators	1
Voltage input	Up to 6.5 V
Current limit (minimum)	200 mA
Operating temperature	–40°C to 125°C
Supplier device package	SC-70-5

2.3.1.3 +2.5 V (U16)

The TPS717xx family of LDO, low-power linear regulators offers very high-power supply rejection (PSRR) while maintaining very low 45-µA ground current in an ultra-small, 5-pin SOT package. The family uses an advanced BiCMOS process and a PMOS pass device to achieve fast start-up, very low noise, excellent transient response, and excellent PSRR performance. The TPS717xx is stable with a 1-µF ceramic output capacitor and uses a precision voltage reference and feedback loop to achieve a worst-case accuracy of 3% over all load, line, process, and temperature variations.

Features

- Input voltage: 2.5 to 6.5 V
- Available in multiple output versions:
  - Fixed output with voltages from 0.9 to 5 V
  - Adjustable output voltage from 0.9 to 6.2 V
- Ultra-high PSRR:
  - 70 dB at 1 kHz
  - 67 dB at 100 kHz
  - 45 dB at 1 MHz
- Excellent load and line transient response
- Very LDO: 170 mV typical at 150 mA
- Low noise: 30 μV_{RMS} typical (100 Hz to 100 kHz)

表 9 lists the TPS71725 LDO features.

表 9. TPS71725 LDO Features

PARAMETERS	DETAILS
Part number	TPS71725DCKR
Regulator topology	Positive fixed
Voltage output	2.5 V
Current output	150 mA
Number of regulators	1
Voltage input	2.5 to 6.5 V
Current limit (minimum)	200 mA
Operating temperature	–40°C to 125°C
Mounting type	Surface mount

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2.3.1.4 –5 V (U17)

The TPS6040x family of devices generates an unregulated negative output voltage from an input voltage ranging from 1.6 to 5.5 V. The devices are typically supplied by a pre-regulated supply rail of 5 V or 3.3 V. Only three external 1-µF capacitors are required to build a complete DC-DC charge pump inverter. The TPS6040x can deliver a maximum output current of 60 mA with a typical conversion efficiency of greater than 90% over a wide output current range.

Features:

- Inverts input supply voltage
- Up to 60-mA output current
- Only three small 1-µF ceramic capacitors needed
- Input voltage range from 1.6 to 5.5 V
- Device quiescent current typical 65 µA
- Integrated active Schottky diode for start-up into load

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表 10 lists the TPS60403 features.

表 10. TPS60403 Inverter (Charge Pump) Features

PARAMETERS	DETAILS
Part number	TPS60403DBVR
Function	Ratiometric
Output configuration	Positive or negative
Topology	Charge pump
Output type	Fixed
Number of outputs	1
Voltage input (minimum)	1.8 V
Voltage input (maximum)	5.25 V
Voltage output (minimum / fixed)	–Vin, 2Vin, Vin / 2
Current output	60 mA
Frequency switching	250 kHz
Synchronous rectifier	No
Operating temperature	–40°C to 125°C (T_J)

2.3.1.5 –2.5 V (U18)

The TPS723xx family of LDO negative voltage regulators offers an ideal combination of features to support low noise applications. These devices are capable of operating with input voltages from –10 to –2.7 V, and support outputs from –10 to –1.2 V. These regulators are stable with small, low-cost ceramic capacitors, and include enable (EN) and noise reduction (NR) functions. Thermal short circuit and over-current protections are provided by internal detection and shutdown logic. High PSRR (65 dB at 1 kHz) and low noise (60 μV_{RMS}) make the TPS723xx ideal for low-noise applications.

Features:

- Ultra-low noise: 60 μV_{RMS} typical
- High PSRR: 65 dB typical at 1 kHz
- LDO voltage: 280 mV typical at 200 mA, 2.5 V
- Available in –2.5 V
- Stable with a 2.2-µF ceramic output capacitor
- Less than 2-µA typical quiescent current in shutdown mode
- 2% overall accuracy (line, load, and temperature)
- Thermal and overcurrent protection
- SOT23-5 (DBV) package

表 11 lists the TPS72325 features.

表 11. TPS72325 Features

PARAMETERS	DETAILS
Part number	TPS72325DBVT
Regulator topology	Negative fixed
Voltage output	–2.5 V
Current output	200 mA
Voltage dropout (typical)	0.28 V at 200 mA

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表 11. TPS72325 Features (continued)

PARAMETERS	DETAILS
Number of regulators	1
Voltage Input	–10 to –1.2 V
Current limit (minimum)	300 mA
Operating temperature	–40°C to 125°C

2.3.1.6 Power Supply Jumper Options

表 12 lists the power supply jumper options.

表 12. Power Supply Jumper Options

CONNECTOR	1-2	3-2
J11	3.3 V	+2 P 5 V
J12	AVDD = 2.5 V	AVDD = 5 V
J14	AVSS = –2.5 V	AVSS = 0 V

2.3.1.7 Isolated Power

図 14 shows the transformer driver and LDO, which generate an isolated power supply for the isolation amplifier.

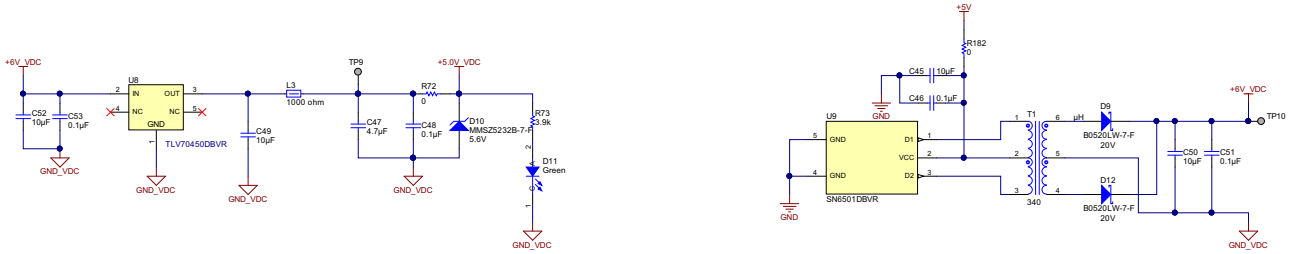

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図 14. Isolated Power Supply for Isolation Amplifiers

The SN6501 is a monolithic oscillator and power-driver, specifically designed for small form factor, isolated power supplies in isolated interface applications. The device drives a low-profile, center-tapped transformer primary from a 3.3- or 5-V DC power supply. The secondary can be wound to provide any isolated voltage based on transformer turns ratio. The SN6501 consists of an oscillator followed by a gate drive circuit that provides the complementary output signals to drive the ground referenced N-channel power switches. The internal logic ensures break-before-make action between the two switches.

Features:

- Push-pull driver for small transformers
- Single 3.3- or 5-V supply
- High primary-side current drive:
  - 5-V supply: 350 mA (maximum)
  - 3.3-V supply: 150 mA (maximum)
- Low ripple on rectified output permits
- Small output capacitors

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- Small 5-pin SOT-23 package

Find more information at the device's product page: http://www.ti.com/product/SN6501

2.4 Design Enhancements

2.4.1 Sampling Rate

This TI design has been tested with the ADC configured to sample the analog input at 80 samples per cycle. ADC is capable of providing data rates up to 128 kSPS. There are 16 selectable oversampling ratio (OSR) options to optimize the converter for a specific data rate. Higher data rates are typically used in grid infrastructure applications that implement software re-sampling techniques to help with channel-to-channel phase adjustment for voltage and current. See Section 9.3.1, *Clock*, of the data sheet for more details.

2.4.2 Using External Reference With ADS131A04

The delta-sigma ADC has an internal reference of 2.442 V. The dynamic range can be increased by using an external reference of 2.5 V. Provision to provide an external reference input to the delta-sigma ADC is provided. In the ADS131A04 by default, the external reference is selected (INT_REFEN = 0). If reference output is required for testing before interfacing to the MCU, a low cost reference can be used.

2.4.3 Using 4-V Reference for Analog Input Measurement

The differential input voltage range for the ADS131A04 is –VREF / Gain to VREF / Gain. The internal reference can be programmed to either 2.442 V or 4 V. The dynamic range of the ADC can be improved by configuring VREF = 4 V, the VREF_4 V bit can be set to 1 when VAVDD – VAVSS > 4.5 V. In this design the reference has been programmed to 2.442 V and tested. To use the 4 V reference the ADC must be configured to measure bipolar input.

By configuring VREF = 4 V the input range can be increased from ±2.442 to ±4 V which increases the AC input range by ×1.65 compared to VREF = 2.442 V. This configuration can be used when wider current ranges are required to be measured. The op amps used in the design can work for ±5 V. In this design, ±5-V rails are available onboard. By making these simple changes in the design the input measurement range can be extended.

表 13 provides information to configure the power supply for different reference voltage configuration.

表 13. Changes for Reference Configuration

REFERENCE	POPULATE	DEPOPULATE
2.442 V	R186 and R187	—
4 V	Use TP25 and TP26 to connect external voltage up to ±5 V	R186 and R187

2.5 Board Design Guideline

2.5.1 Delta-Sigma ADC

Recommendations

- Partition the analog, digital, and power-supply circuitry into separate sections on the PCB.
- Use a single ground plane for analog and digital grounds.
- Place the analog components close to the ADC pins using short, direct connections.
- Keep the SCLK pin free of glitches and noise.

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- Verify that the analog input voltages are within the specified voltage range under all input conditions.
- Tie unused analog input pins to GND.
- Provide current limiting to the analog inputs in case overvoltage faults occur.
- Use a LDO regulator to reduce ripple voltage generated by switch-mode power supplies. This reduction is especially true for AVDD where the supply noise can affect performance.
- Keep the input series resistance low to maximize THD performance.
- Do not cross analog and digital signals.
- Do not allow the analog power supply voltages (AVDD – AVSS) to exceed 3.6 V under any conditions, including during power up and power down when the negative charge pump is enabled.
- Do not allow the analog power supply voltages (AVDD – AVSS) to exceed 6 V under any conditions, including during power up and power down when the negative charge pump is disabled.
- Do not allow the digital supply voltage to exceed 3.9 V under any conditions, including during power up

2.5.2 AMC1301

See the following sections in the data sheet for design and layout guidelines:

- Section 10 *Power Supply Recommendations*
- Section 11 *Layout*

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2.5.3 CDCLVC1102PW

See the following sections in the data sheet for

- Section 11 *Power Supply Recommendations*
- Section 12 *Layout*

2.6 Software Implementation

This section discusses the software implementation. The first subsection discusses the software used to setup the MSP432 peripherals, ADS131A04 ADC, and ADC104S021 ADC. Subsequently, the metrology software is described as two major processes: the foreground process and background process.

2.6.1 Setup Software

2.6.1.1 MSP432 Setup

The MSP432 is used to set up the ADS131A04 and ADC104S021, calculate metrology parameters, and communicate these parameters through the RS-232 to a terminal program.

2.6.1.1.1 GPIO, SPI, and UART Setup

For communication of the metrology parameters, a UART port is used on the MSP432. The UART communication is set to a baud rate of 57600 with 8 data bits, no parity, and 1 stop bit. By connecting the UART port pins to an isolated UART, then to the RS-232 board (such as TIDA-00163), the metrology parameters calculated by the MSP432 can be displayed by a PC using a terminal program.

To communicate with the ADS131A04 and ADC104S021, two different SPI ports are used. The SPI clock for both of these ports is set to 3 MHz with the most significant bit shifted out first. These different SPI ports are independent of each other but are used to communicate to the two devices of a particular ADC. For example, the ADS131A04 uses the same UCB0 port for the two ADS131A04 devices on this board. Similarly, the ADC104S021 uses the same UCB2 port for the two ADC104S021 devices.

In addition to the normal SPI lines used to communicate to the A04, the A04 devices also use additional GPIO lines for communication. One of these additional GPIO pins is used to provide a reset signal to the ADS131A04 to get it to a known state before sending commands to it. The second extra GPIO pin is connected to the DRDY pin of the ADS131A04. This pin is used to alert the MSP432 of a new set of ADS131A04 ADC samples now ready so that the MSP432 can query the ADS131A04 devices for these new ADC samples. To immediately alert the MSP432 of the new ADC samples, the MSP432 GPIO pin connected to DRDY is configured as an interruptible input.

As a method to determine when there is an issue with the ADC reference of the A04 devices, the board also has comparators which compare the ADS131A04 references to a set voltage threshold. By connecting the output of these comparators to the corresponding interruptible GPIO pins on the MSP432, the state of the two ADC references can be logged.

表 14 lists the GPIO associations in the application.

表 14. GPIO Associations

PORT PIN	FUNCTION
RS-232 GPIO CONFIGURATION	
P3.2(UCA2 UART port)	UART receive for RS-232 communication
P3.3 (UCA2 UART port)	UART transmit for sending metrology parameters through the RS-232

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表 14. GPIO Associations (continued)

PORT PIN	FUNCTION
ADS131A04 GPIO CONFIGURATION	
P5.2	ADS131A04 chip select
P1.5 (UCB0 SPI port)	ADS131A04 SPI clock
P1.6 (UCB0 SPI port)	ADS131A04 SPI input (SIMO)
P1.7 (UCB0 SPI port)	ADS131A04 SPI output (MISO)
P3.0	ADS131A04 DRDY
P4.5	ADS131A04 RESET
ADS131A04 REFERENCE CHECK GPIO CONFIGURATION	
P2.7	ADCREF1 OK (for status of U2 reference)
P2.6	ADCREF2 OK (for status of U4 reference)
ADC104S021 GPIO CONFIGURATION	
P5.0	Chip select 1 for the U1 device on the board
P5.1	Chip select 2 for the U3 device on the board
P3.5 (UCB2 SPI port)	ADC104S021SPI clock
P3.6 (UCB2 SPI port)	ADC104S021SPI input (SIMO)
P3.7(UCB2 SPI port)	ADC104S021SPI output (MISO)

2.6.1.1.2 Clocks

The MSP432 uses multiple clocks in this application. 表 15 lists the different clock settings used in this application.

表 15. Application Clock Settings

PORT PIN	FUNCTION
MASTER CLOCK (MCLK, CPU CLOCK)	
Clock frequency	48 MHz (clock divider = 1)
Number of flash wait states	2
Clock source	Internal DCO of the MSP432
SUBSYSTEM MASTER CLOCK (SMCLK)	
Clock frequency	24 MHz (clock divider = 2)
Clock source	Internal DCO of the MSP432
AUXILIARY CLOCK (ACLK)	
Clock frequency	32768 Hz
Clock source	32768-kHz crystal
RS-232	
Speed	57600 baud
Clock source	SMCLK
TIMER FOR UPDATE OF METROLOGY PARAMETERS	
Timer used	Timer A0
Clock source	ACLK
Generated interval	1 second (32768 counts)
Timer mode	Up mode
ADC104S021 SPI CLOCK	
Clock frequency	3 MHz (clock divider = 8)
Clock source	SMCLK
Clock polarity	Inactive state is high (UCCKPL = 1)
Clock phase	Data is valid on clock leading edge (UCCKPH = 0)

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表 15. Application Clock Settings (continued)

PORT PIN	FUNCTION
ADS131A04 SPI CLOCK	
Clock frequency	3 MHz (clock divider = 8)
Clock source	SMCLK
Clock polarity	Inactive state is low (UCCKPL = 0)
Clock phase	Data is valid on clock leading edge (UCCKPH = 0)

2.6.1.1.3 Direct Memory Access (DMA)

The direct memory access (DMA) module is used to transfer all of the ADS131A04 and ADC104S021 ADC samples from these devices to the memory of the MSP432 with minimal bandwidth requirements from the CPU. To get the ADC sample data from the ADC devices, the MSP432 requires writing data to the SPI transmit buffers to activate the SPI clocks. The DMA module is used to not only transfer the received SPI data to memory, but also is used to write the dummy data to the SPI transmit buffers of the MSP432 so that the receive operations can be triggered. As a result, there are two DMA channels used for each of the SPI ports used for communication to an ADC. One channel is for sending the dummy data from the MSP432 memory to the SPI transmit buffers. The other channel is used for moving the received SPI data to the memory of the MSP432. Once the transfer is complete, an interrupt is generated to complete any necessary post-transfer processing.

表 16 lists the DMA channel associations.

表 16. DMA Channel Associations

DMA CHANNEL NUMBER	FUNCTION
0	ADS131A04 SPI transmit (for triggering receive)
1	ADS131A04 SPI receive
2	Not used
3	Not used
4	ADC104S021 SPI transmit (for triggering receive)
5	ADC104S021 SPI receive
6	Not used
7	Not used

2.6.1.1.4 Interrupt Priorities

The software has five interrupts that are prioritized. 表 17 lists these interrupt priorities.

表 17. Interrupt Priorities

INTERRUPT	SIGNIFICANCE	PRIORITY CODE
DMA1	Transfer of ADS131A04 ADC samples to the MSP432 memory has completed.	0x20
PORT3	New ADS131A04 ADC samples have been generated so the MSP432 can now query the ADS131A04 device for the new ADC samples.	0x40
DMA2	Transfer of ADC104S021 ADC samples to the MSP432 memory has completed.	0x60
TA0_0	Time to send a new metrology parameter for RS-232 communication.	0x80
EUSCIA2	Transmit buffer for RS-232 communication is empty so a new byte of the RS-232 communication packet can be sent.	0x80

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In 表 17, the interrupts with the lower priority code value have higher interrupt priority. In the software, communication to the terminal is a relatively low priority so the TA0_0 and EUSCIA2 priorities have the highest priority code. The DMA2 interrupt has the next lowest priority since no time critical processing is required to be done in this interrupt. For the Port3 interrupt, a high priority interrupt is selected because this interrupt is where the majority of the sample processing is done. The DMA1 interrupt has the highest priority since a CRC check is performed on the sample data received from the ADS131A04 in this interrupt and if there are any CRC errors are present it should be detected as soon as possible so that the MSP432 can request and receive the sample data again before the next ADC sample is ready.

2.6.1.2 ADS131A04 Setup

For communication to the ADS131A04 devices, the device chaining feature of these devices is enabled so that communication to the two ADS131A04 devices can be done transparently, by concatenating the packets to be sent to the two A04 devices into one merged packet and sending it out through the shared SPI lines. This method of chaining does not use two different chip select lines from the MSP432 like what is done for the ADC104S021 devices.

After reset, the MSP432 device first sends a reset signal to the ADS131A04 device to get it to a known state. After resetting the ADS131A04 devices, commands are sent to these devices to initialize them. These setup commands are sent out manually to the software so a DMA is not used for transferring this command data to the ADS131A04. The order of commands sent is as follows:

1. Send an UNLOCK command to the ADS131A04 until an UNLOCK ACK is received from both ADS131A04 devices.
2. Send a WAKEUP command to the ADS131A04 until a WAKEUP ACK is received from both ADS131A04 devices.
3. Send a command to set the ICLK divider of the A04 devices to 2. Keep sending this command until the appropriate ACK is received.
4. Send a command to set the OSR to 256 and the Modclk divider either to 8 (for a 50-Hz nominal line frequency) or 6 (for a 60-Hz nominal line frequency). This step results in a sample rate of 4000 samples per seconds whenever the software is configured for a line frequency of 50 Hz and a sample rate of 5333.3 whenever the software is configured for a line frequency of 60 Hz. Keep sending this command until the appropriate ACK is received.
5. Send a command to the A04 devices to use the following configuration:
   - High resolution mode
   - Negative charge pump disabled
   - Internal reference enabled

   Keep sending the command until the appropriate ACK is received.
6. Send a command to the A04 devices to use a fixed frame size of six words. In the hardware configuration of the board, each word is set to be 24-bits long resulting in a communication frame size of 18 bytes per ADS131A04 device. Keep sending this command until the appropriate ACK is received.
7. Send a command to enable all of the ADS131A04 ADCs. Keep sending this command until the appropriate ACK is received.
8. Send a command to the A04 devices to use the following configuration:
   - CRC is enabled on all bits received and transmitted.
   - The time before the device asserts the done signal after the LSB is shifted out is set to 12 ns.
   - The time before the device asserts Hi-Z on Dout after the LSB of the data frame is shifted out is 12 ns.

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After the ADS131A04 devices are set up, it alerts the MSP432 of new sample data being available. This alert is done through providing GPIO interrupts from the DRDY pin of the ADS131A04. After receiving one of these interrupts, the MSP432 only needs to write dummy data into the SPI transmit buffers so that it can receive the ADC sample data from the ADS131A04 devices. The ADS131A04 automatically sends this data out through the SPI port so no command data must be sent to the ADS131A04 once it is set up. Due to the chaining of the two ADS131A04 devices, the received data frame consists of the data frames of each of the A04 devices which means that a total of twelve 24-bit words (36 bytes) are sent from the ADS131A04 devices. The first six words sent correspond to the first ADS131A04 device (designated as U2 on the PCB) and the last six words correspond to the second ADS131A04 device (designated as U4 on the PCB). 図 15 shows the order of words in a data frame that is received from each individual ADS131A04 device by the MSP432.

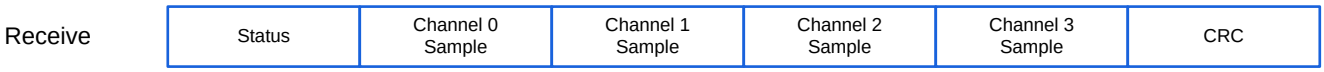

図 15. Words Received From Each ADS131A04 Device

In the data received from an A04 device, the first word provides a status update of the ADC internal system monitor, the next four words represent the ADC samples, and the last word is the CRC word calculated by the ADS131A04. Once this packet is received by the MSP432, it extracts the CRC word, calculates its own CRC based on the values of the other words in the packet, and compares the two CRCs to ensure that no data transmissions have occurred. To accelerate the CRC calculation, the CRC module of the MSP432 is used for performing the CRC calculations of the first 14 bytes of the 15 byte data used in the calculation. If the two CRCs match, the received sample words are parsed into the corresponding ADC sample data for use for metrology calculations. If the two CRCs do not match, the MSP432 initializes the resending of the sample data.

The ADC samples of the two ADS131A04 devices are concatenated to form a single array of eight ADC samples. The channel associations used for these eight channels are shown in 表 18. These channel mappings differ when compared to the channel mappings of the ADC104S021.

表 18. ADS131A04 ADC Channel Associations

SOFTWARE CHANNEL NUMBER	ADC NAME (PCB DESIGNATION)	ADC CHANNEL NUMBER	CORRESPONDING HEADER (PCB DESIGNATION)
0	U2	0	J7 (current transformer 1)
1	U2	1	J5 (potential divider 1)
2	U2	2	J10 (Rogowski 1)
3	U2	3	J3 (AMC 1)
4	U4	0	J4 (AMC 2)
5	U4	1	J9 (Rogowski 2)
6	U4	3	J6 (potential divider 2)
7	U4	2	J8 (current transformer 2)

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2.6.1.3 ADC104S021 Setup

To communicate to the ADC104S021, the only command that must be sent to the ADC is the next ADC channel to sample. In the software, a total of five 16-bit words (10 bytes) are sent as a packet to the ADC. Simultaneously, a total of five 16-bit words are read, which are parsed to extract the values of the ADC sample data. The SPI transmission and reception from the ADC104S021 is done by the DMA module of the MSP432. The extracted ADC sample data received from the ADC104S021 is translated into a signed 16 bit number for further processing. This translation allows the ADC results from the ADC104S021 to be treated as a 16-bit signed number when performing mathematical operations.

Words 1 through 4 sent to the ADC are used to select the next ADC to sample. In the software, sample all four of ADC104S021 device's channels every time the SAR ADC is triggered. The corresponding ADC sample data is contained in words 2-5 of the response sent by the ADC. Word 1 of the ADC response is not used by the software. Also, to ensure that the fifth response word is read by the MSP432, a dummy value is written to the SPI transmit buffer for the fifth transmission word. Writing this dummy value enables the SPI clock so that the fifth response word can be obtained. 図 16 shows the order of the words written and received by the MSP432 in a data frame.

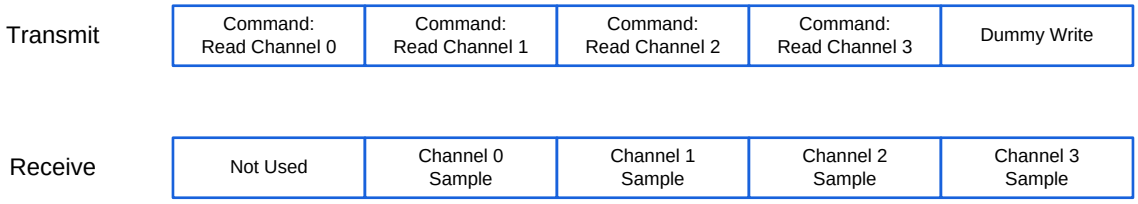

図 16. Words Sent and Received in ADC104S021 Data Frame

In this TI Design, all four channels of an ADC104S021 device are sampled every time a new set of ADS131A04 sample readings are generated. To enable sensing both ADC104S01 devices in this design, the actual ADC104S021 device that is enabled is alternated every sample by toggling the individual ADC104S021 chip select lines. As a result, the sampling rate of the ADC104S021 samples is half of the sample rate of the ADS131A04 samples.

The ADC samples of the two ADC104S021 devices are concatenated to form a single array of eight ADC samples. The channel associations used for these eight channels are listed in 表 19. Note that these channel mappings differ when compared to the channel mappings of the ADS131A04.

表 19. ADC104S021 ADC Channel Associations

SOFTWARE CHANNEL NUMBER	ADC NAME (PCB DESIGNATION)	ADC CHANNEL NUMBER	CORRESPONDING HEADER (PCB DESIGNATION)
0	U1	0	J7 (current transformer 1)
1	U1	1	J5 (potential divider 1)
2	U1	2	J3 (AMC 1)
3	U1	3	J10 (Rogowski 1)
4	U3	0	J9 (Rogowski 2)
5	U3	1	J4 (AMC 2)
6	U3	2	J8 (current transformer 2)
7	U3	3	J6 (potential divider 2)

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2.6.2 Foreground Process

The foreground process includes the initial setup of the hardware and MSP432 software immediately after a device RESET. 図 17 shows the flowchart for this process.

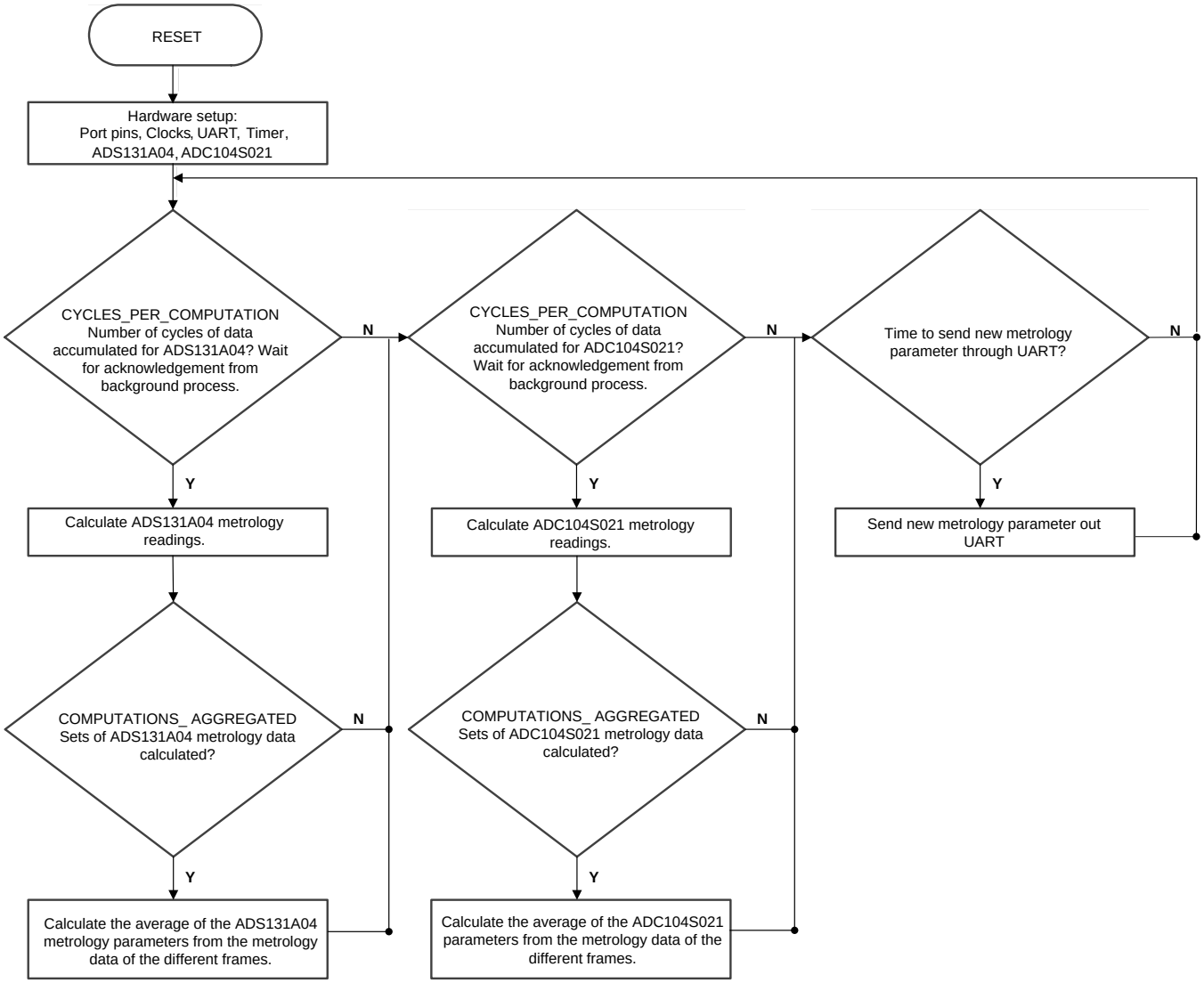

図 17. Foreground Process

The initialization routines involve the setup of the general purpose input/output (GPIO) port pins, clock system, UART for metrology parameter communication and its associated timer for triggering sending new parameters through UART as well as the software for enabling communication to the ADS131A04 and ADC104S021. A description of this setup software is provided in 2.6.1.

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After the hardware is setup, the foreground process checks whether the background process has notified the foreground process to calculate new metering parameters based on the samples from the ADS131A04 devices. This notification is sent through the assertion of the "PHASE_STATUS_NEW_LOG" status flag whenever a frame of data is available for processing. The data frame consists of the processed dot products that were accumulated for the number of cycles that are set by the CYCLES_PER_COMPUTATION setting. By default, this macro is set to one tenth of the nominal frequency (that is, five cycles for a 50-Hz nominal frequency and six cycles for a 60-Hz nominal frequency).

The processed dot products for the ADS131A04-based metrology parameters include RMS voltage, RMS current, active power and reactive power. These dot products are used by the foreground process to calculate the corresponding metrology readings in real-world units. Using the foreground's calculated values of active and reactive power, the apparent power is calculated. The frequency (in Hertz) and power factor are also calculated using parameters calculated by the background process using the formulas in 2.6.2.1. After the ADS131A04-based metrology parameters for one frame are calculated, they are stored until a certain number of frames of ADS131A04-based frames of data have been computed. Once this number of frames of parameters (set by the "COMPUTATIONS_AGGREGATED" macro) has been calculated, they are averaged together to generate the aggregated metrology parameters. A similar process like what is used for the ADS131A04 is also used to calculate the ADC104S021-based metrology parameters except only RMS voltage, RMS current, and frequency are calculated.

After it is checked whether it is time to calculate new ADS131A04-based or ADC104S021-based metrology parameters, it is checked whether it is time to send out a new parameter through the UART port. A timer is used to generate the intervals between the sending of consecutive metrology parameters. In this software, this interval is set by default to be one second.

2.6.2.1 Formulae

This section briefly describes the formulas used for the voltage, current, and power. As previous sections described, voltage and current samples are obtained at a sampling rate of either 4000 Hz (for a nominal frequency of 50 Hz) or 5333.3 Hz (for a nominal frequency of 60 Hz). All of the samples are taken over the number of cycles set by the CYCLES_PER_COMPURATION macro. The RMS values are obtained by the following formulas:

$$V_{RMS,\,ADS131A04} = K_{v,ADS13104} \times \sqrt{\frac{\sum_{n=1}^{\text{Sample count } v_{ADS131A04}} v_{ADS131A04}(n) \times v_{ADS131A04}(n)}{\text{Sample count}_{ADS131A04}}} - V_{offset,\,ADS131A04} \quad (1)$$

$$I_{RMS,\,ADS131A04} = K_{i,ADS13104} \times \sqrt{\frac{\sum_{n=1}^{\text{Sample count } v_{ADS131A04}(n)} i_{ADS131A04}(n) \times i_{ADS131A04}(n)}{\text{Sample count}_{ADS131A04}}} - i_{offset,\,ADS131A04} \quad (2)$$

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$$V_{RMS,\,ADC104S021} = K_{v,ADC104S021} \times \sqrt{\frac{\sum_{n=1}^{Sample\ count\ v_{ADC104S021}(n)} v_{ADC104S021}(n) \times v_{ADC104S021}(n)}{Sample\ count_{ADC104S021}}} - v_{offset,\,ADC104S021} \quad (3)$$

$$I_{RMS,\,ADC104S021} = K_{i,ADC104S021} \times \sqrt{\frac{\sum_{n=1}^{Sample\ count_{ADC104S021}} i_{ADC104S021}(n) \times i_{ADC104S021}(n)}{Sample\ count_{ADS104S021}}} - i_{offset,\,ADC104S021} \quad (4)$$

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Where:

- $V_{ADS131A04}(n)$ = ADC sample from the voltage channel of the ADS131A04, taken at sample instant N
- $V_{offset,\ ADS131A04}$= Offset used to subtract effects of the additive white Gaussian noise from the ADS131A04 ADC used to measure voltage
- $i_{ADS131A04}(n)$ = ADC sample from the current channel of ADS131A04, taken at sample instant n
- $i_{offset,\ ADS131A04}$ = Offset used to subtract effects of the additive white Gaussian noise from the ADS131A04 current converter
- Sample $count_{ADS131A04}$ = Number of samples accumulated in the ADS131A04 window defined by the CYCLES_PER_COMPUTATION number of mains cycles
- $K_{v,ADS131A04}$ = Scaling factor for the voltage measured by the ADS131A04
- $K_{i,ADS131A04}$ = Scaling factor for current measured by the ADS131A04
- $V_{ADC104S021}(n)$ = ADC sample from the voltage channel of the ADC104S021, taken at sample instant n
- $i_{ADC104S021}$ = Offset used to subtract effects of the additive white Gaussian noise from the ADS104S021 ADC used to measure voltage
- $i_{ADC104S021}(n)$ = ADC sample from the current channel of the ADC104S021, taken at sample instant n
- $i_{ADC104S021}$ = Offset used to subtract effects of the additive white Gaussian noise from the ADC104S021 current converter
- Sample $count_{ADC104S021}$ = Number of samples accumulated in the ADC104S021 window defined by the CYCLES_PER_COMPUTATION number of mains cycles
- $K_{v,\ ADC104S021}$ = Scaling factor for the voltage measured by the ADC104S021
- $K_{i,\ ADC104S021}$ = Scaling factor for current measured by the ADC104S021

Using the ADS131A04 current and voltage samples, power is calculated for a frames worth of active and reactive energy samples. These samples are phase corrected and passed on to the foreground process, which uses the number of samples (sample $count_{ADS131A04}$) to calculate phase active and reactive powers through the following formulas:

$$P_{ACT} = K_{ACT} \frac{\sum_{n=1}^{\text{Sample count}_{ADS131a04}} v_{ADS131A04}(n) \times i_{ADS131A04}(n)}{\text{Sample count}_{ADS131A04}} \quad (5)$$

$$P_{REACT} = K_{REACT} \frac{\sum_{n=1}^{\text{Sample count}_{ADS131A04}} v_{90,ADS131A04}(n) \times i_{ADS131A04}(n)}{\text{Sample count}_{ADS131A04}} \quad (6)$$

$$P_{App} = \sqrt{P_{ACT}^2 + P_{REACT}^2} \quad (7)$$

$v_{90,ADS131A04}$ (n) = Voltage sample of the waveform that results from shifting $v_{ADS131A04}$ (n) by 90° , taken at a sample instant n

- K_{ACT}= Scaling factor for active power
- K_{REACT}= Scaling factor for reactive power

Note that for reactive energy, the 90° phase shift approach is used for two reasons:

- This approach allows accurate measurement of the reactive power for very small currents.

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- This approach conforms to the measurement method specified by IEC and ANSI standards.

The calculated mains frequency from the ADS131A04 voltage channel is used to calculate the 90 degrees-shifted voltage sample. Because the frequency of the mains varies, it is important to first measure the mains frequency accurately to phase shift the voltage samples accordingly.

To get an exact 90° phase shift, interpolation is used between two samples. For these two samples, a voltage sample slightly more than 90° before the current sample is used and a voltage sample slightly less than 90° before the current sample is used. The application's phase shift implementation consists of an integer part and a fractional part. The integer part is realized by providing an N samples delay.

The fractional part is realized by a one-tap FIR filter. In the software, a lookup table provides the filter coefficients that are used to create the fractional delays.

The background process also calculates the frequency in terms of samples per mains cycle. The foreground process then converts this samples per mains cycle to Hertz by the following formulas:

$$\text{Frequency}_{\text{ADS131A04}}\,(\text{Hz}) = \frac{\text{Sampling Rate}_{\text{ADS131A04}}\,(\text{samples / second})}{\text{Frequency}_{\text{ADS131A04}}\,(\text{samples / cycle})} \tag{8}$$

$$\text{Frequency}_{\text{ADC104S021}}\,(\text{Hz}) = \frac{\text{Sampling Rate}_{\text{ADC104S021}}\,(\text{samples / second})}{\text{Frequency}_{\text{ADC104S021}}\,(\text{samples / cycle})} \tag{9}$$

2.6.3 Background Process

図 18 shows the background process, which mainly deals with timing critical events in software. The background process uses the assertion of the DRDY signal to provide a GPIO interrupt to the MSP432 whenever new ADS131A04 samples are ready. The port interrupt is used to both retrieve the sample data from the ADS131A04 as well as trigger the ADC104S021 to start conversions and retrieve the new ADC104S021 values. While retrieving the ADC samples from the ADS131A04 and ADC104S021 through DMA, per-sample processing is done on the previous set of ADS131A04 and ADC104S021 samples and these ADC samples are stored in arrays for any desired ADC sample analysis. The sample processing is not done on every ADC channel but is done on the channels that are designated as the voltage ADC channel and the current ADC channel. The sampling processing done on the ADS131A04 sample data is done by the DS_processing function while the sample processing done on the ADC104S021 is done by the SAR_processing function.

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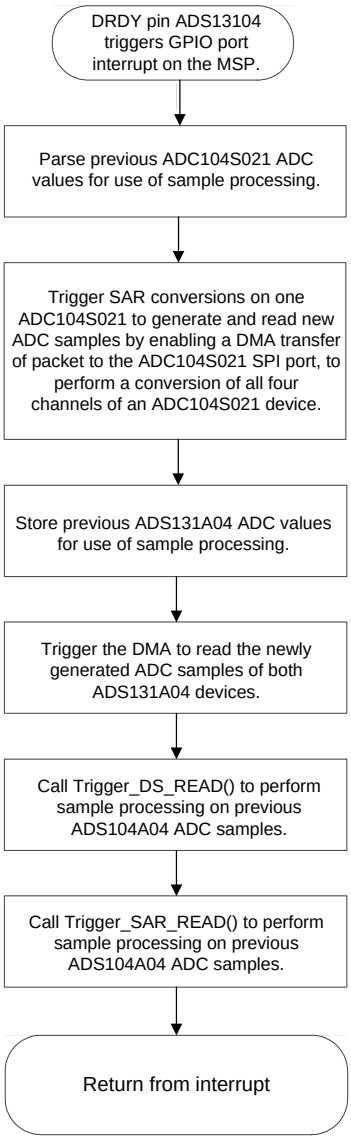

図 18. Background Process

Once the ADS131A04 response packet has been completely transmitted from the ADS131A04 to the MSP432, a DMA1 interrupt is generated. 図 19 shows what occurs in the DMA1 ISR. In the DMA1 ISR, the received packet from the ADS131A04 has its sent CRC compared to the CRC calculated by the MSP432 to ensure that the data has been accurately transmitted to the MSP432. This CRC check is done on each ADS131A04 device. If the CRC check passes for a ADS131A04 device, the corresponding packet for that ADS131A04 device is parsed to extract the sample values of the four ADC channels for that device. These new ADC values will have sample processing performed on them during the next port interrupt that is generated by the DRDY pin of the ADS131A04. If any of the ADS131A04 devices do not pass the CRC check, then the DMA triggers rereading the received data from all of the ADS131A04 devices. However, for the case where only one of the ADS131A04 devices had previously failed the CRC check, once the retransmitted data is received for both ADS131A04 devices only the packet of the ADS131A04 device that failed the CRC check would be parsed if it passes the CRC check this time. There is no need to parse the data for the ADS131A04 that previously passed the CRC check since the correct data was already parsed when it previously passed the CRC check.

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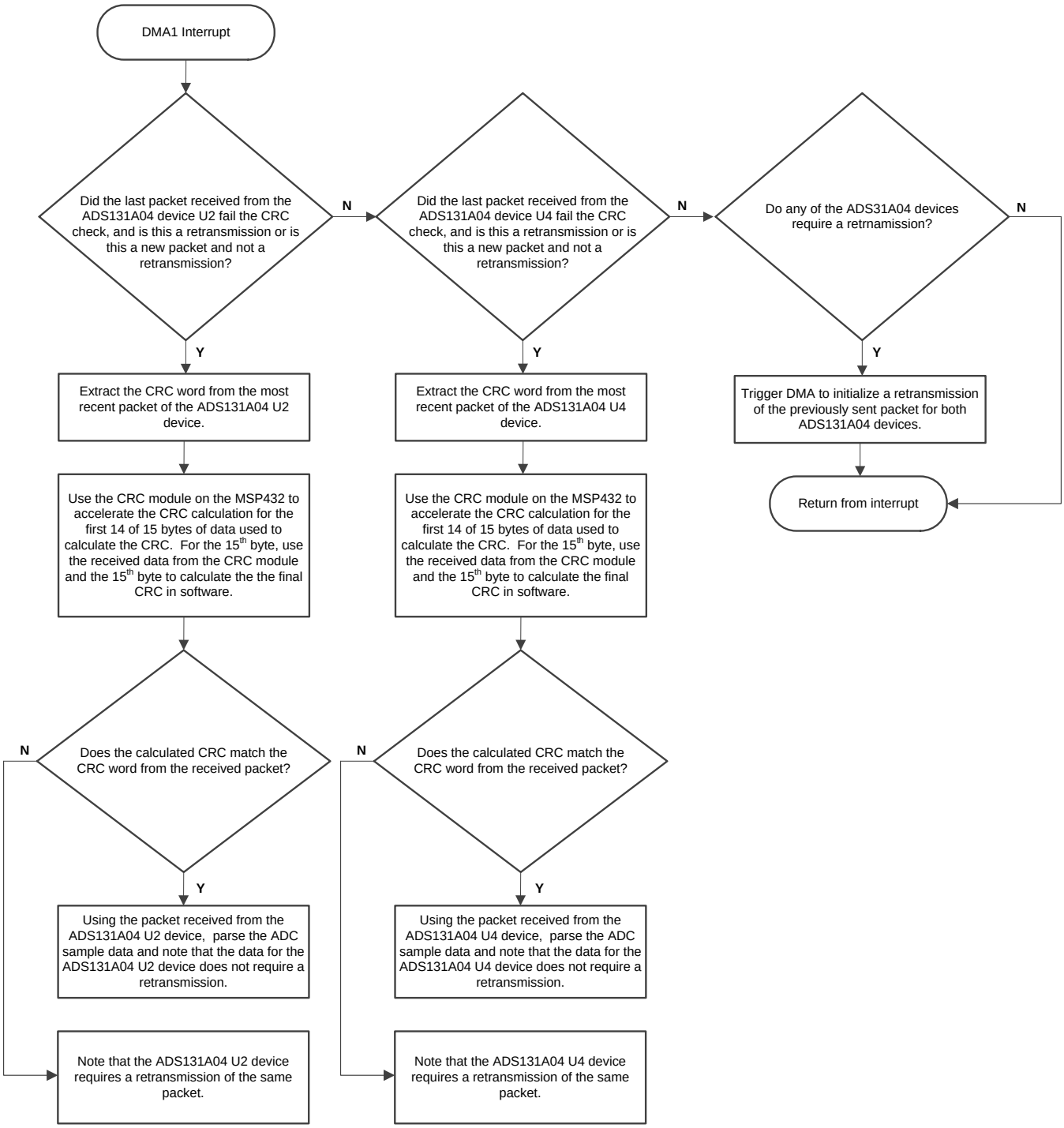

図 19. DMA1 ISR

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After the MSP432 has received the response packet from the ADC104S021, a DMA2 interrupt is generated. In the DMA2 ISR, the state of the chip select lines for both ADC104S021 devices are toggled so that the currently enabled ADC104S021 device is disabled and the currently disabled ADC104S021 device is enabled. The next time the SAR ADC is triggered the most recently enabled ADC104S021 device would perform conversions on all of its channels while the other ADC104S021 device would be disabled. This would cause the different ADC104S021 devices to have a sample rate that is half of the ADS131A04.

2.6.3.1 Sample Processing

図 20 shows the flowchart for the DS_processing function. The DS_processing function uses the ADS131A04 24-bit ADC samples to calculate intermediate dot product results that are fed into the foreground process for the calculation of the ADS131A04-based metrology readings. The current and voltage samples are processed and accumulated in dedicated 64-bit variables. In addition, active power and reactive power are also accumulated in dedicated 64-bit variables.

図 21 shows the flowchart for the SAR_processing function. The SAR_processing function uses the ADC104S021 ADC samples to calculate intermediate dot product results that are fed into the foreground process for the calculation of the ADC104S021-based metrology readings. The ADC104S021 ADC samples are translated from an unsigned 10-bit representation to a 16-bit signed integer representation for mathematical operations. The current and voltage samples are processed and accumulated in dedicated 64-bit variables. Since power is only calculated from the ADS131A04 ADCs, active power and reactive power are not accumulated in the SAR_processing function.

For both DS_processing and SAR_processing functions, arrays of the five largest ADC voltage and current samples within a mains cycle as well as arrays of the five smallest ADC readings within the same mains cycle are stored. Each of the five largest ADC samples for the ADS131A04 and the five largest ADC samples for the ADC104S021 are compared for diagnostic purposes. Similarly, each of the five smallest ADC samples for the ADS131A04 and the five smallest ADC samples for the ADC104S021 are also compared, as is described in 2.6.3.1.2.

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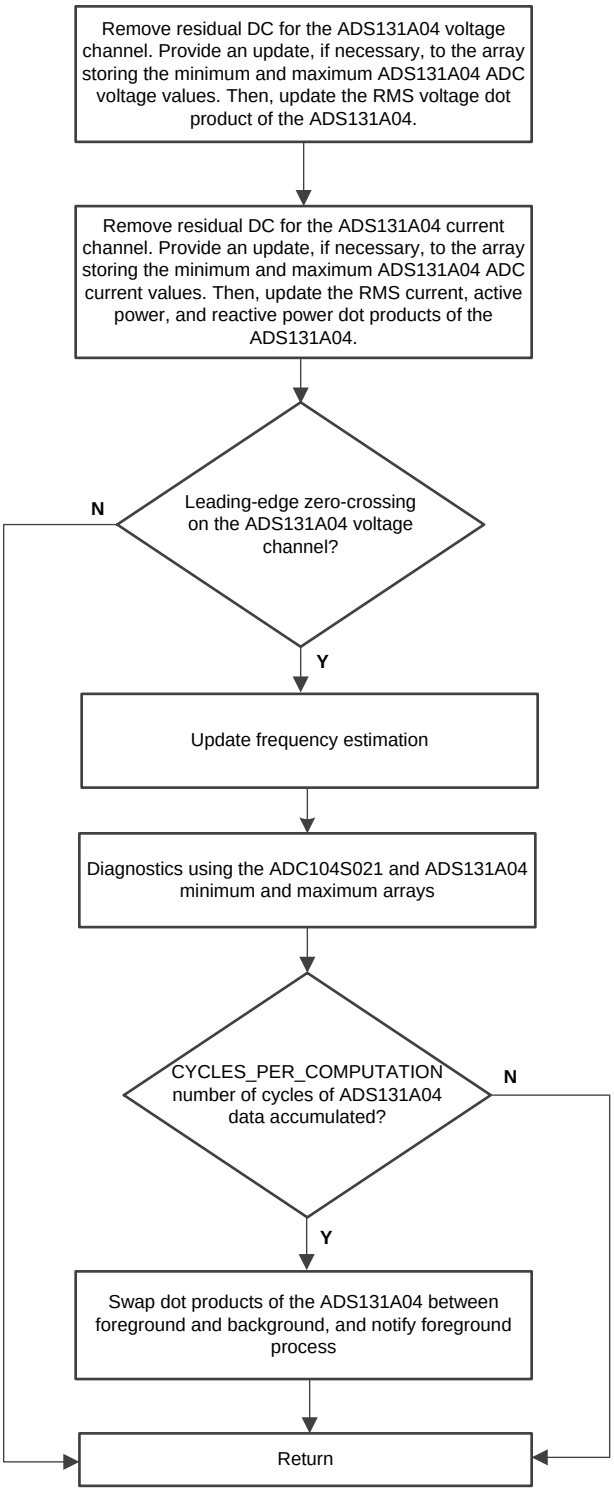

図 20. DS_processing Function

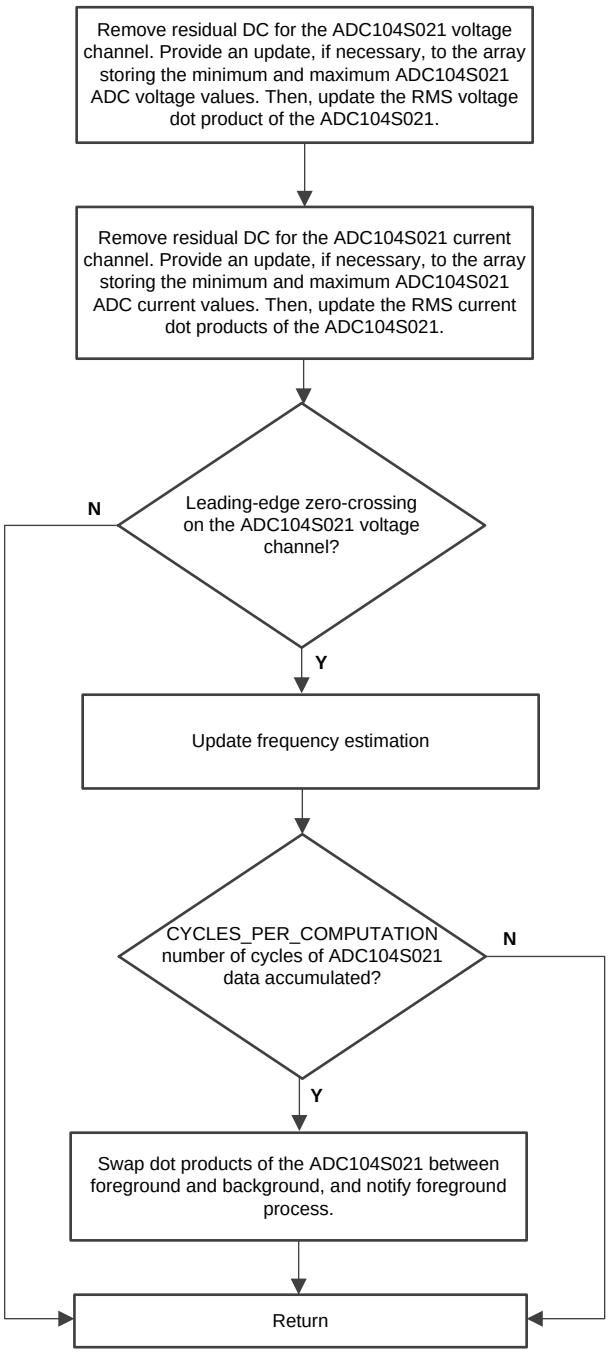

図 21. SAR_processing Function

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Whenever there is a leading-edge zero-crossing (− to + voltage transition) on an ADC's voltage channel, the corresponding ADC's frequency estimation (in units of samples per cycle) is updated. Also, after data corresponding to CYCLES_PER_COMPUTATION, the number of mains cycles have been accumulated for an ADC, the background process triggers the foreground function to calculate the metrology parameters for that ADC. For the ADS131A04, the calculated values include RMS voltage, RMS current, active power, reactive power, apparent power, and frequency. For the ADC104S021, the calculated values include RMS voltage, RMS current, and frequency.

In the software, there are two sets of dot products for each ADC (the ADS131A04 has two sets of dot products and the ADC104S021 has a separate two sets of dot products). At any given time, one set is used by the foreground for calculation and the other used as the working set by the background. After the background process has sufficient samples, it swaps the two dot products so that the foreground uses the newly acquired dot products that the background process just calculated and the background process uses a new empty set to calculate the next set of dot products.

2.6.3.1.1 Voltage and Current Signals

The ADC samples are represented as signed integer and any stray DC or offset value on these converters are removed using a DC tracking filter. Separate DC estimates for all voltages and currents are obtained using the filter and voltage and current samples, respectively. These estimates are then subtracted from each voltage and current sample. The resulting instantaneous voltage and current samples are used to generate the following intermediate dot product results:

- Accumulated squared values of ADS131A04 voltage and currents samples, which is used for the ADS131A04's calculation of V_{RMS} and I_{RMS}, respectively.
- Accumulated squared values of ADC104S021 voltage and currents samples, which is used for the ADC104S021's calculation of V_{RMS} and I_{RMS}, respectively.
- Accumulated ADS131A04 power samples to calculate active energy
- Accumulated ADS131A04 power samples using the ADS131A04 current samples and 90° phase shifted ADS131A04 voltage samples to calculate reactive energies

These accumulated values are processed by the foreground process.

2.6.3.1.2 Diagnostics Using ADC104S021 and ADS131A04

Within each mains cycle, the five largest and smallest ADC samples are stored for both the ADS131A04 and ADC104S021. This is represented in the software as eight different arrays:

- ADS131A04 voltage min array
- ADC104S021 voltage min array
- ADS13A04 voltage max array
- ADC104S021 voltage max array
- ADS131A04 current min array
- ADC104S021 current min array
- ADS13A04 current max array
- ADC104S021 current max array

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When a new mains cycle is detected (specifically at the negative to positive zero crossing) on the ADS131A04 voltage channel the eight arrays are compared, where the following pairs of arrays are compared to each other: the voltage min array of the ADS131A04 and ADC104S021, the voltage max array of the ADS131A04 and ADC104S021, the current min array of the ADS131A04 and ADC104S021, and the current max array of the ADS131A04 and ADC104S021. In each of these array comparisons, each element of the corresponding array of the ADC104S021 is translated into high and low threshold values that can be directly compared to the corresponding element of the ADS131A04 array. As a result, during each mains cycle five sets of comparisons are done for each pair of arrays (element x of an ADC104S021 array is compared to element x of the corresponding ADS131A04 array).

For each array element comparison, a minimum and maximum threshold value is generated using the ADC104S021 array element, the THRESHOLD macro, and the SAR_OFFSET macro. These threshold values are then translated so that they could be directly compared to the ADS131A04 ADC value stored in the corresponding element of the ADS131A04 array. This translation ensures that the ADC sample comparisons done correspond to actually comparing the voltage and current readings of the ADS131A04 and ADC104S021 in real-world units.

If any of the five ADC samples in the ADS131A04 array is beyond the corresponding minimum and maximum thresholds that were calculated using the ADC104S021 samples, then a mismatch and its associated type is noted for this mains cycle. There are four mismatch types based on the different arrays that are compared: a voltage min mismatch, a voltage max mismatch, a current min mismatch, and a current max mismatch. The state of whether a mismatch has occurred for the voltage min, voltage max, current min, and current_max is stored for each mains cycle. When the foreground process is called, the total number of cycle mismatches over the 5 (for 50 Hz) or 6 (for 60 Hz) cycle frame is summed for each type of mismatch (this means that the sum's maximum value for a type of mismatch is either 5 or 6 because this is equal to the number of cycles in the frame of data). This summed value is displayed as one digit in the mismatch diagnostic parameters that are sent out through the UART (see 3.2.3.1 for details).

2.6.3.1.3 Frequency Measurement and Cycle Tracking

A cycle tracking counter and sample counter keep track of the number of samples accumulated for an ADC. When approximately "CYCLES_PER_COMPUTATION" number of mains cycles have been accumulated, the background process switches the foreground and background dot products and then notifies the foreground process to calculate the final values of metrology parameters for that frame of data.

For frequency measurements, a straight-line interpolation is used between the zero-crossing voltage samples. 図 22 shows the samples near a zero cross and the process of linear interpolation.

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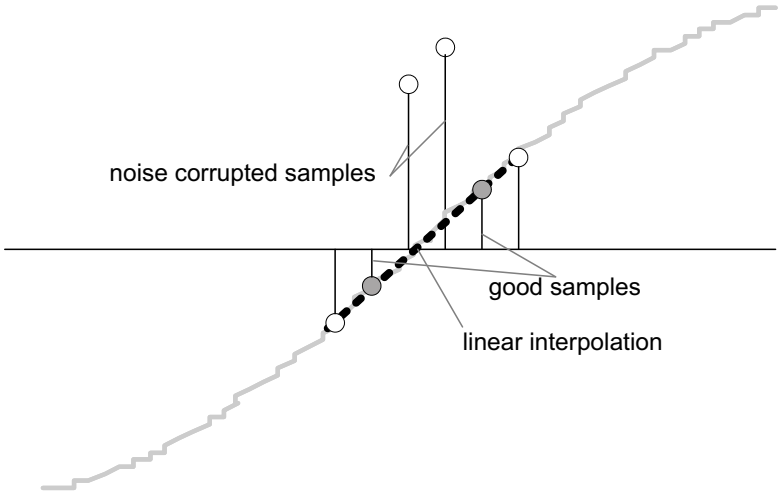

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図 22. Frequency Measurement

Because noise spikes can also cause errors, the application uses a rate of change check to filter out the possible erroneous signals and make sure that the two points that are interpolated are from genuine zero crossing points. For example, with two negative samples, a noise spike can make one of the samples positive, thereby making the negative and positive pair look as if there is a zero crossing. The resultant cycle-to-cycle timing goes through a weak low-pass filter to further smooth out cycle-to-cycle variations. This filtering results in a stable and accurate frequency measurement that is tolerant of noise.

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2.6.3.2 Phase Compensation

To ensure accurate power measurements from the ADS131A04 samples, the relative phase shift between voltage and current samples must be compensated. This phase shift may be caused by the passive components of the voltage and current input circuit or even the utilized current sensor. The implementation of the phase shift compensation consists of an integer part and a fractional part. The integer part is realized by providing an N samples delay. The fractional part is realized using a one-tap finite impulse response (FIR) filter that interpolates between two samples, similar to the FIR filter used for providing 90°-shifted voltage samples for reactive energy measurements. In the software, a lookup table provides the filter coefficients that are used to create the fractional delays. The lookup table provides fractional phase shifts as small as 1/256th of a sample. The 4000 sample rate at 50 Hz used in this application corresponds to a 0.0176° degree resolution while the 5333.3 sample rate at 60 Hz corresponds to a 0.0158° degree resolution. In addition to the filter coefficients, the lookup table also has an associated gain variable for each set of filter coefficients. This gain variable is used to cancel out the resulting gain from using a certain set of filter coefficients.

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3 Getting Started Hardware and Software

3.1 Hardware

The following connections must be made for testing the AFE:

- DC power supply
- Interface to MSP432 for delta-sigma ADC
- Isolated voltage input
- Non-isolated voltage input
- Current input

Connectors have been provided to interface the input. Ensure to use the proper connectors, defined in 図 23 and 図 24.

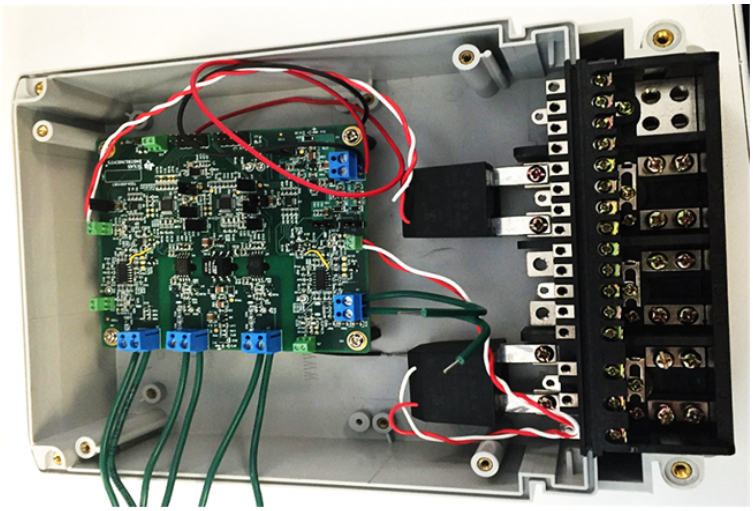

図 23. Data Acquisition AFE With External CTs

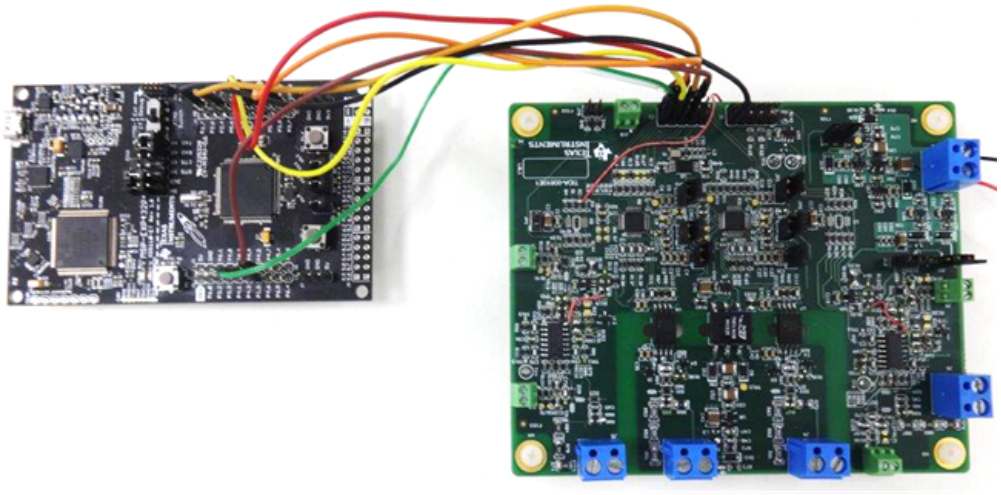

図 24. Data Acquisition AFE With MCU Interface

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3.1.1 Power Supply Jumper

3.1.1.1 External DC Input

The DC input of 5.5 V is consented using the jumpers in 表 20, 表 21, and 表 22.

表 20. External DC Input

JUMPER	PINS	DESCRIPTION
J13	1	DC_IN
	2	AGND

3.1.1.2 Jumpers for 0- to 5-V ADC Operation

表 21. Jumpers for Delta-Sigma ADC 0- to 5-V Operation

POWER	JUMPER	PINS	STATUS
AVDD	J11	1-2 (3.3)	NA
		3-2 (2.5)	NA
	J12	1-2 (3.3 / 2.5)	Open
		3-2 (5 V)	Mounted
AVSS	J14	1-2 (–2.5)	Open
		3-2 (0 V)	Mounted

3.1.1.3 Jumpers for ±2.5-V Operation

表 22. Jumpers for Delta-Sigma ADC ±2.5-V Operation

POWER	JUMPER	PINS	STATUS
AVDD	J11	1-2 (3.3)	NA
		3-2 (2.5)	Mounted
	J12	1-2 (3.3 / 2.5)	Mounted
		3-2 (5 V)	Open
AVSS	J14	1-2 (–2.5)	Mounted
		3-2 (0 V)	Open

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3.1.2 TIDA-00835 AFE to MSP432 MCU Interface

3.1.2.1 ADS131A04 to MSP432 Interface

表 23 provides details on the interface connections between the ADC and MSP432P401R.

表 23. MSP432 to Delta-Sigma ADC ADS131A04 Interface

SIGNAL	LAUNCHPAD PIN	TIDA-00835 INTERFACE
ADC_RESET	P4.5 (GPIO) Reset for ADS131A04	J2 – Pin 3
ADC_SPI_DRDY	Delta-sigma DRDY → P3.0 (interruptible GPIO pin)	J2 – Pin 5
ADC1_SPI_DONE	Done of device 1→ P5.1 (not used)	J2 – Pin 6
ADC_SPI_MISO	Delta-sigma data out → P1.7 (UCB0SOMI)	J2 – Pin 7
ADC_SPI_MOSI	Delta-sigma data in → P1.6 (UCB0SIMO)	J2 – Pin 8
ADC1_CS#	Delta-sigma chip select → P5.2 (GPIO pin)	J2 – Pin 9
ADC_SPI_SCLK	Delta-sigma SPI clock → P1.5 (UCBOCLK)	J2 – Pin 10
GND	J2 – GND	J1 – Pin 10
ADC1_Comp	P2.7 (GPIO)	J2 – Pin 2
ADC2_Comp	P2.6 (GPIO)	J2 – Pin 4

3.1.2.2 RS-232 Interface

表 24 provides information on connecting the MSP432P401R LaunchPad to the PC through the RS-232.

表 24. MSP432 LaunchPad Serial Interface

PORT PIN	FUNCTION
RS-232 GPIO configuration: • P3.2(UCA2 UART Port) • P3.3 (UCA2 UART Port)	RS-232 GPIO configuration: • UART Receive for RS-232 Communication • UART Transmit for sending metrology parameters via RS-232
J3 – Pin 22	Ground

3.1.3 AFE Interface

3.1.3.1 Current Inputs

3.1.3.1.1 CT Input

表 25 provides information on the connector, which connects the current inputs to the ADCs.

表 25. CT_Rogowski Input to Delta-Sigma ADC Configuration

ADC	CONNECTOR	ADC CHANNEL
U2	J7	CT_1_Out
	J10	ROGO_1_Out
U4	J8	CT_2_Out
	J9	ROGO_2_Out

注: External current inputs are applied across the previous jumpers. To configure the previous inputs to measure Rogowski input from an external active integrator board, the following changes must be made.

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3.1.3.1.2 Rogowski Coil Integrator Output

表 26 provides information on the connector which connects the TIDA-00777 integrator output to the ADCs.

表 26. Rogowski Coil Integrator Output Connection

ADC	CONNECTOR	ADC CHANNEL	ACTION
U2	J10	ROGO_1_Out	Depopulate R111 and C74
			Connector Integrator output to TP4
U4	J9	ROGO_2_Out	Depopulate R113 and C75
			Connector Integrator output to TP6

3.1.3.2 Non-Isolated Voltage Input

表 27 lists the connectors used to connect the non-isolated AV voltage input for measurement.

表 27. Non-Isolated Voltage Input to Potential Divider

ADC	CONNECTOR	ADC CHANNEL
U2	J5	PD_Out1
U4	J6	PD_Out2

3.1.3.3 Isolated Voltage Input

表 28 lists the connectors used to connect the isolated AV voltage input for measurement.

表 28. Non-Isolated Voltage Input to Potential Divider

ADC	CONNECTOR	ADC CHANNEL
U2	J3	VOUT1_P
		VOUT1_N
U4	J4	VOUT2_P
		VOUT2_N

3.1.4 ADC Jumpers

3.1.4.1 Delta-Sigma

表 29 lists the connectors used to connect the isolated AV voltage input for measurement.

表 29. Delta-Sigma ADC Jumper Configuration

ADC	JUMPER	ENABLE	DISABLE
U2	Charge pump	Depopulate JP4	Populate JP4
	AVCC_3.3	Populate JP3	Depopulate JP3
	AVDD	Populate JP2	Depopulate JP2
U4	Charge pump	Depopulate JP8	Populate JP8
	AVCC_3.3	Populate JP7	Depopulate JP7
	AVDD	Populate JP6	Depopulate JP6

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3.1.5 Reference

3.1.5.1 External or Internal

3.1.5.1.1 AFE Signal Conditioning

表 30 provides jumper information for configuring the AFE reference.

表 30. AFE Reference Configuration

ADC	INTERNAL	EXTERNAL
U2	Populate R151	Populate R153
	Depopulate R153	Depopulate R151
U4	Populate R154	Populate R156
	Depopulate R156	Depopulate R154

3.1.5.1.2 Delta-Sigma ADC

表 31 describes the configuration of reference to the delta-sigma ADC.

表 31. Delta-Sigma Reference Configuration

ADC	INTERNAL	EXTERNAL
U2	Depopulate R157	Populate R157
U4	Depopulate R161	Populate R161

3.1.5.2 Analog Input Range

表 32 provides jumper information for configuring the delta-sigma reference.

表 32. Delta-Sigma Analog Input Configuration

ADC	0 to 5 V	±2.5 V
U2	Populate 126	Populate 118
	Depopulate118	Depopulate126
U4	Populate 129	Populate 121
	Depopulate 121	Depopulate 129

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3.2 Firmware

3.2.1 Loading Code to MSP432

This firmware was developed with Code Composer Studio™ (CCS) Version: 6.1.1.00022. To load this firmware onto the MSP432, follow these instructions:

1. From the downloaded software zip file, run the TIDA00810lib-1.0-windows-installer.exe file to download and extract this design firmware. This produces the TIDA-00810 lib folder, which contains the software's CCS project and software.
2. Open CCS. On the Workspace Launcher window that pops up after starting CCS (shown in 図 25), select the desired workspace path and click OK. The CCS Edit window will pop up as shown in 図 26.

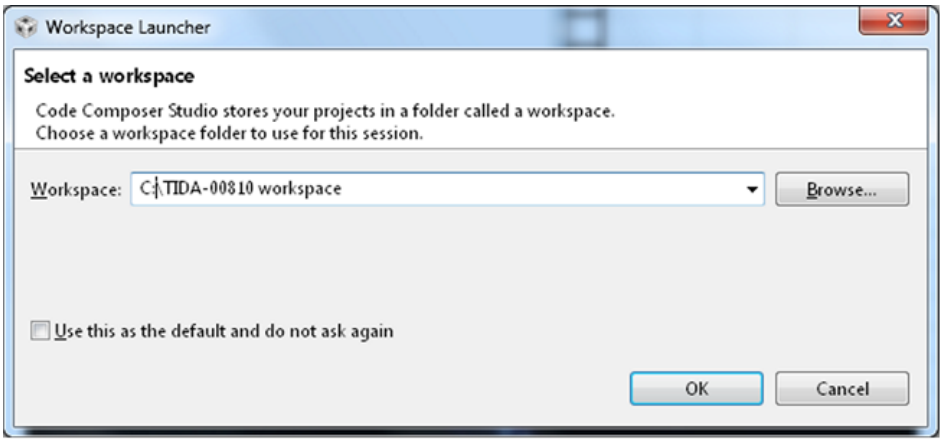

図 25. Workspace Launcher Window

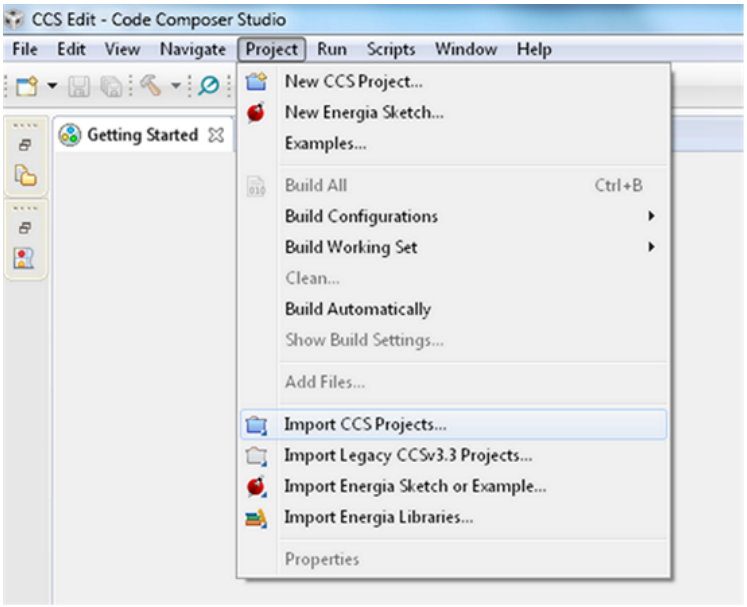

図 26. CCS Edit Window

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3. From the CCS Edit window click Project, and select Import CCS Projects as shown in 図 26. The Import CCS Eclipse Projects window shown in 図 27 appears.

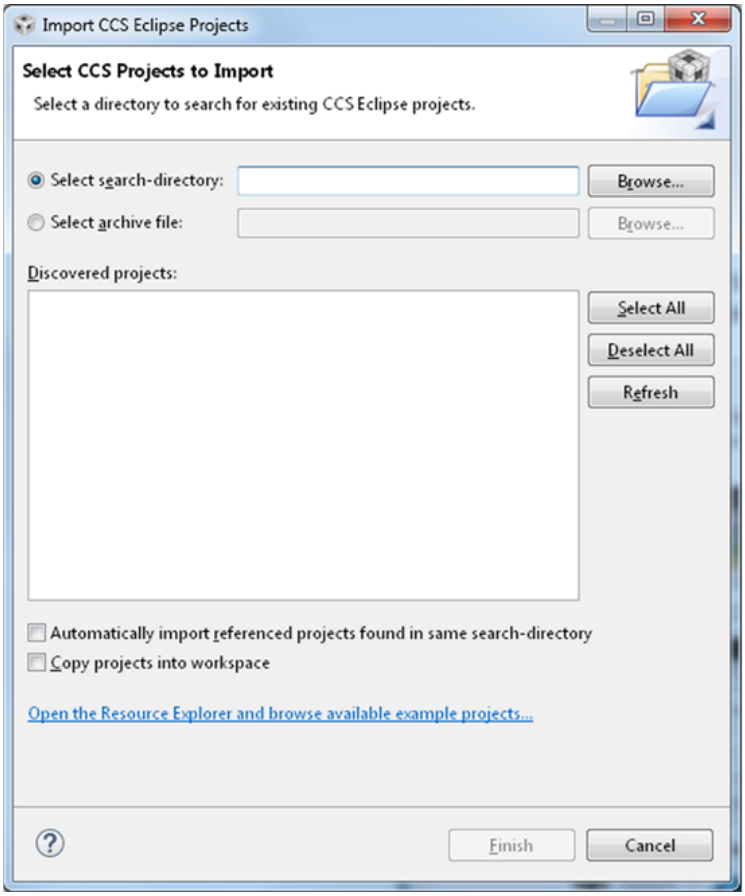

図 27. Import CCS Eclipse Projects Window

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4. From the Import CCS Eclipse Projects window that pops up, select the Select search-directory button and click the Browse button then select the TIDA-00810 lib folder where the design software is located. After selecting the proper directory, the design's CCS project should be discovered as shown in 図 28. Once this project has been discovered, click Finish.

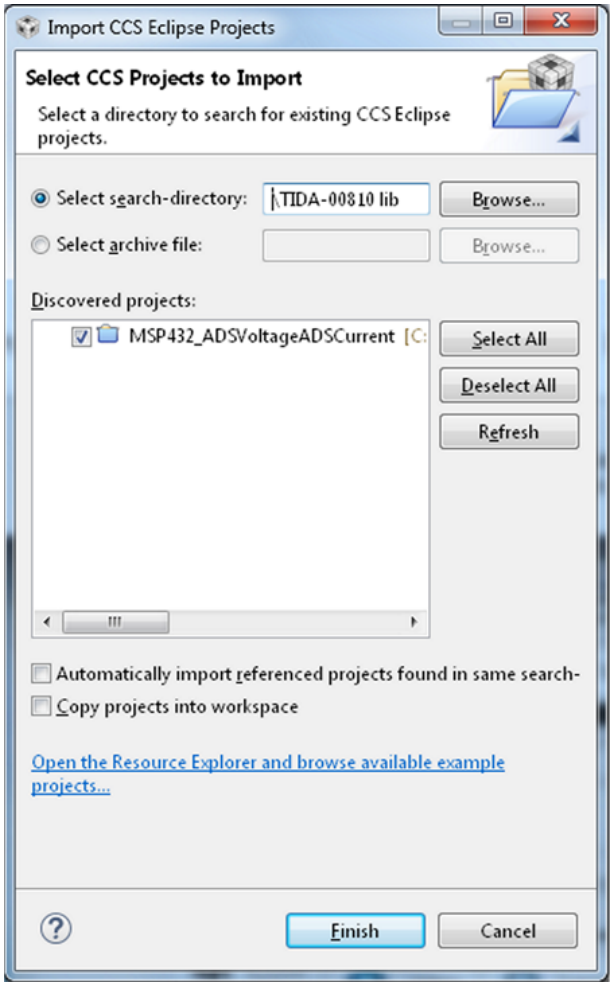

図 28. Import CCS Eclipse Projects Window With TIDA-00810 Software Discovered

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5. In the Project Explorer, right click the project name and select Clean Project. This is shown in 図 29.

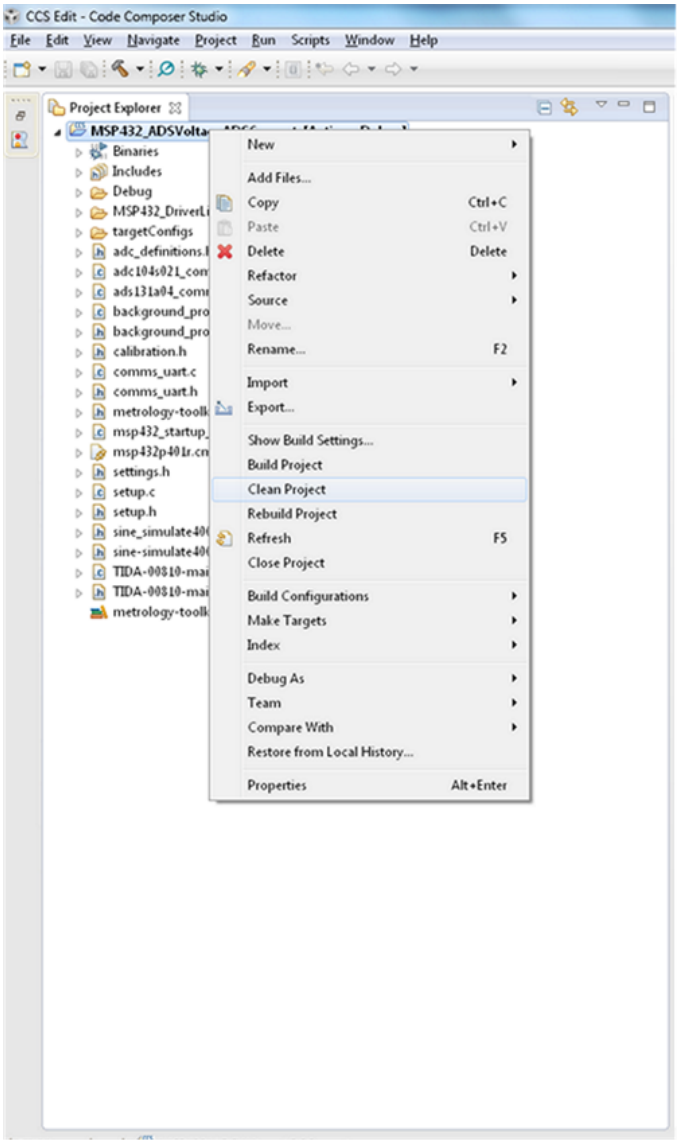

図 29. Steps for Cleaning A Project

6. After the project has been cleaned, load the code onto the MSP432 by clicking on the Run menu and selecting Debug as shown in 図 30.

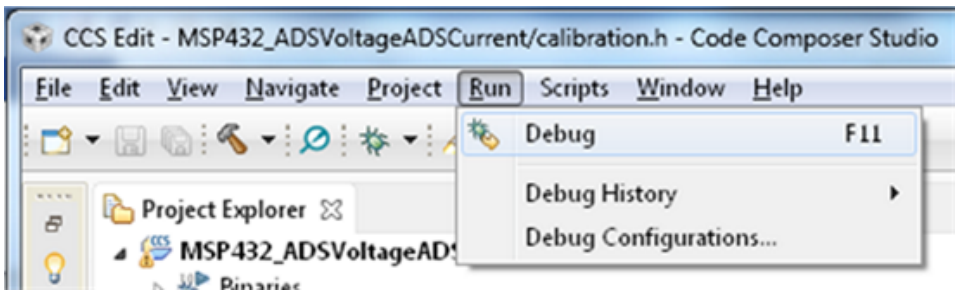

図 30. Loading Code on MSP432

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3.2.2 Configuration Options

In the firmware package, the settings.h file contains macros that can be adjusted to configure the system as necessary. In this file, the following macros are available:

- VOLTAGE_CHANNEL_NUMBER: The value of this macro defines which ADS131A04 channel will correspond to the voltage channel so that the voltage samples used for ADS131A04-based metrology calculations will be taken from this ADS131A04 channel. To select a particular ADS131A04 channel for the voltage channel of the ADS131A04, define this macro to be equal to the corresponding software channel number mentioned in 表 18.
- CURRENT_CHANNEL_NUMBER: The value of this macro defines which ADS131A04 channel will correspond to the current channel so that the current samples used for ADS131A04-based metrology calculations will be taken from this ADS131A04 channel. To select a particular ADS131A04 channel for the current channel of the ADS131A04, define this macro to be equal to the corresponding software channel number mentioned in 表 18.
- SAR_VOLTAGE_CHANNEL_NUMBER: The value of this macro defines which ADC104S021 channel will correspond to the voltage channel so that the voltage samples used for ADC104S021-based metrology calculations will be taken from this ADC104S021 channel. To select a particular ADC104S021 channel for the voltage channel of the ADC104S021, define this macro to be equal to the corresponding software channel number mentioned in 表 18.
- SAR_CURRENT_CHANNEL_NUMBER: The value of this macro defines which ADC104S021 channel will correspond to the current channel so that the current samples used for metrology calculations will be taken from this ADC104S021 channel. To select a particular ADC104S021 channel for the current channel of the ADC104S021, define this macro to be equal to the corresponding software channel number mentioned in 表 18.
- COMPUTATIONS_AGGREGATED: This value defines how many 100-ms frames of data should be averaged together for the metrology parameters that are actually sent through the UART. By default, this value is set to 10, which leads to the metrology parameters sent out through the UART being averaged over an approximately one second time interval.
- MAINS_NOMINAL_FREQUENCY: This macro defines the nominal mains frequency and can only take the values of 50 or 60. When this macro is configured for 50, the sample rate of the ADS131A04 is set to 4000 samples per second with metrology parameters being calculated once every five mains cycles (approximately 100 ms). If this macro is configured for 60, the sample rate is set to 5333.3 samples per second with metrology parameters being calculated once every six mains cycles (approximately 100 ms).
- SAR_OFFSET: When performing comparisons of the 24-bit ADS131A04 ADC results and the translated 16-bit ADC104S021 ADC results, this provides an acceptable offset threshold (in ADC units) so that the diagnostic logic does not indicate a possible mismatch in the min or max for low voltages or low currents. This macro is defined in terms of the 16-bit translated value of the ADC104S021. As a result, a value of 64 would correspond to 1 LSB of the ADC104S021.
- THRESHOLD: This macro along with the SAR_OFFSET macro define at what error percentage would the software indicate the occurrence of a mismatch between the min/max values between the ADS131A04 ADC values and the translated, corresponding ADC104S021 ADC values. If the SAR_OFFSET is set to 0, the corresponding error threshold for determining mismatch could be found by using the following formula : (±100%)/2^THRESHOLD . For example, a value of 2 for this threshold would correspond to an error threshold of ±25%, which means that an error would be triggered whenever the ADS131A04 value is either less than 75% of the translated ADC104S021 value or if it is

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greater than 125% of the translated ADC104S021 value.

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3.2.3 Viewing Metrology and ADC Sample Results

3.2.3.1 *Viewing Metrology Results Using RS-232*

By following the RS-232 and UART settings mentioned in 2.6.1.1.1, the metrology parameters can be viewed from a terminal program, as shown in 図 31.

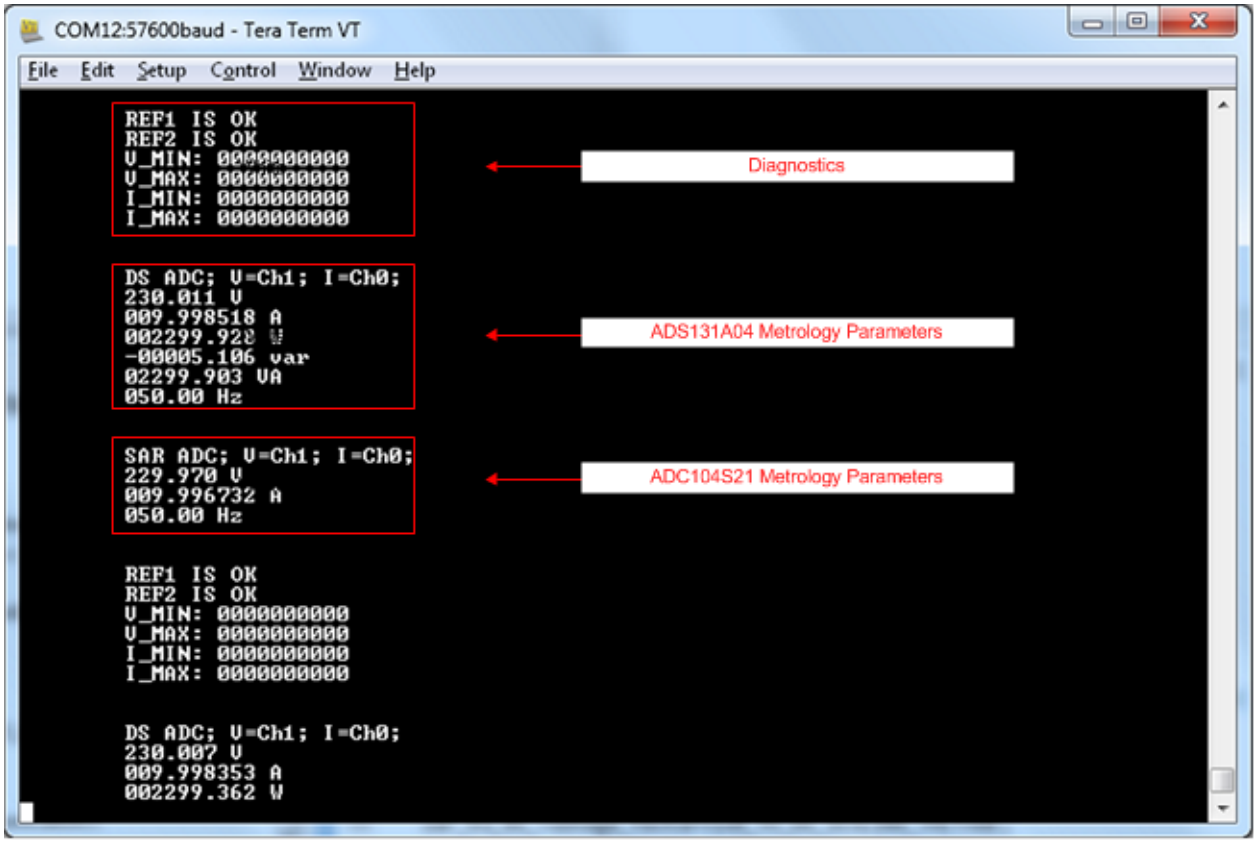

図 31. Viewing Metrology Results Using Terminal Program

By default, a new metrology parameter is sent from the MSP432's UART at a rate of approximately once per second. There are three sets of parameters that are sent out of the UART of the MSP432. The first item that is sent is the diagnostics information. 表 33 shows the different parameters that are sent in this set, the relative order in which these parameters are sent out through the UART, and a description of these parameters. The second set of parameters sent are the metrology parameters that are calculated using the ADS131A04 ADC. 表 34 provides a description of these ADS131A04-based parameters. The final set of parameters that are sent are the metrology parameters that are calculated using the ADC104S021. Similarly, 表 35 provides a description of these ADC104S021-based parameters.

表 33 provides a description of these ADC104S021-based parameters.

表 33. Diagnostic Parameters Sent Out UART

SENDING ORDER	PARAMETER	DESCRIPTION
Sent first	Reference voltage 1 status; start of diagnostic parameters	This parameter reflects the state of the comparator used to determine the health of reference voltage 1 (for ADS131A04 U2 device). If the comparator indicates that the sensed reference is below the set threshold, this parameter would be displayed as CHECK REF1. Otherwise, this parameter is displayed as REF1 IS OK.

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表 **33. Diagnostic Parameters Sent Out UART (continued)**

SENDING ORDER	PARAMETER	DESCRIPTION
Sent second	Reference voltage 2 status	This parameter reflects the state of the comparator used to determine the health of reference voltage 2 (for ADS131A04 U4 device). If the comparator indicates that the sensed reference is below the set threshold, this parameter would be displayed as CHECK REF2. Otherwise, this parameter is displayed as REF2 IS OK.
Sent third	Mismatches between ADS131A04 and ADC104S021 voltage minimum ADC values (V_MIN)	The value of this parameter contains 10 digits where each digit represents a different 5 cycle (for a 50-Hz nominal frequency) or 6 cycle (for a 60-Hz nominal frequency) frames of data. Within each mains cycle, five of the most minimum voltages are logged for both the ADS131A04 and the ADC104S021. If any of the logged minimum voltages for the ADS131A04 are beyond the corresponding minimum voltages logged by the ADC104S021 by a certain threshold, this cycle is noted as having a mismatch between the minimum voltages registered by the two ADCs. Each digit of the V_MIN parameter represents the number of cycles that have a voltage minimum mismatch out of the 5 or 6 cycle frames of data.
Sent fourth	Mismatches between ADS131A04 and ADC104S021 voltage maximum ADC values (V_MAX)	The value of this parameter contains 10 digits where each digit represents a different 5 cycle (for a 50-Hz nominal frequency) or 6 cycle (for a 60-Hz nominal frequency) frames of data. Within each mains cycle, five of the most maximum voltages are logged for both the ADS131A04 and the ADC104S021. If any of the logged maximum voltages for the ADS131A04 are beyond the corresponding maximum voltages logged by the ADC104S021 by a certain threshold, this cycle is noted as having a mismatch between the maximum voltages registered by the two ADCs. Each digit of the V_MAX parameter represents the number of cycles that have a voltage maximum mismatch out of the 5 or 6 cycle frames of data.
Sent fifth	Mismatches between ADS131A04 and ADC104S021 current minimum ADC values (I_MIN)	The value of this parameter contains 10 digits where each digit represents a different 5 cycle (for a 50-Hz nominal frequency) or 6 cycle (for a 60-Hz nominal frequency) frames of data. Within each mains cycle, five of the most minimum current are logged for both the ADS131A04 and the ADC104S021. If any of the logged minimum current for the ADS131A04 are beyond the corresponding minimum current logged by the ADC104S021 by a certain threshold, this cycle is noted as having a mismatch between the minimum current registered by the two ADCs. Each digit of the I_MIN parameter represents the number of cycles that have a current minimum mismatch out of the 5 or 6 cycle frames of data.
Sent sixth	Mismatches between ADS131A04 and ADC104S021 voltage maximum ADC values (I_MAX)	The value of this parameter contains 10 digits where each digit represents a different 5 cycle (for a 50-Hz nominal frequency) or 6 cycle (for a 60-Hz nominal frequency) frames of data. Within each mains cycle, five of the most maximum current are logged for both the ADS131A04 and the ADC104S021. If any of the logged maximum current for the ADS131A04 are beyond the corresponding maximum current logged by the ADC104S021 by a certain threshold, this cycle is noted as having a mismatch between the maximum current registered by the two ADCs. Each digit of the I_MAX parameter represents the number of cycles that have a current maximum mismatch out of the 5 or 6 cycle frames of data.

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表 34. ADS131A04-Based Metrology Parameters Sent Out Through UART

SENDING ORDER	PARAMETER	DESCRIPTION
Sent first	ADS131A04 metrology parameter designator	This parameter is used to denote the start of the ADS131A04-based metrology parameters and also provides information on which ADS131A04 channels are used for the voltage and current samples. The value of this parameter is equal to DS ADC; V = Chx; I = Chy; where x is set to the VOLTAGE_CHANNEL_NUMBER macro and y is set to the CURRENT_CHANNEL_NUMBER.
Sent second	Voltage	The ADS131A04-based metrology calculation of the RMS voltage in V.
Sent third	Current	The ADS131A04-based metrology calculation of the RMS current in A.
Sent fourth	Active power	The ADS131A04-based metrology calculation of the active power in W.
Sent fifth	Reactive power	The ADS131A04-based metrology calculation of the reactive power in var.
Sent sixth	Apparent power	The ADS131A04-based metrology calculation of the apparent power in VA.
Sent seventh	Frequency	The ADS131A04-based metrology calculation of voltage frequency in Hz.

表 35. AD04S021-Based Metrology Parameters Sent Out Through UART

SENDING ORDER	PARAMETER	DESCRIPTION
Sent first	ADC104S021 metrology parameter designator	This parameter is used to denote the start of the ADC104S021-based metrology parameters and also provides information on which ADC104S021 channels are used for the voltage and current samples. The value of this parameter is equal to SAR ADC; V = Chx; I = Chy; where x is set to the SAR_VOLTAGE_CHANNEL_NUMBER macro and y is set to the SAR_CURRENT_CHANNEL_NUMBER.
Sent second	Voltage	The ADC104S021-based metrology calculation of the RMS voltage in units of V.
Sent third	Current	The ADC104S021-based metrology calculation of the RMS current in units of A.
Sent fourth	Frequency	The ADC104S021-based metrology calculation of voltage frequency in units of Hz.

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3.2.3.2 Viewing Metrology Results and ADC Values Using Software Variables

In addition to viewing the metrology values using RS-232, the values of the metrology values as well as the ADC values can be obtained directly from the proper variables in the code. Specifically, there are four sets of variables of interest: metrology parameters (parameters calculated every 5 or 6 cycles), aggregated metrology parameters(parameters calculated once per second that are sent out through the UART), sample data for all ADC channels (1 sample per channel), and sample data for the voltage and current channels (4000 samples for both the voltage and current channels of each ADC). 表 36, 表 37, 表 38, and 表 39 provide information on the specific variables to probe in the software for information on the values of the metrology parameters or the ADC results.

表 36. Variable Names for 5- or 6-Cycle Metrology Parameters

VARIABLE NAME	VARIABLE TYPE	VARIABLE DESCRIPTION
active_power	int32_t [COMPUTATIONS_AGGREGATED]	The ADS131A04-based calculation of active power for a 5 (at 50 Hz) or 6 (at 60 Hz) cycle frames of data. This array stores the last COMPUTATIONS_AGGREGATED number of these frames.
reactive_power	int32_t [COMPUTATIONS_AGGREGATED]	The ADS131A04-based calculation of reactive power for a 5 (at 50 Hz) or 6 (at 60 Hz) cycle frames of data. This array stores the last COMPUTATIONS_AGGREGATED number of these frames.
apparent_power	int32_t [COMPUTATIONS_AGGREGATED]	The ADS131A04-based calculation of apparent power for a 5 (at 50 Hz) or 6 (at 60 Hz) cycle frames of data. This array stores the last COMPUTATIONS_AGGREGATED number of these frames.
rms_voltage	int32_t [COMPUTATIONS_AGGREGATED]	The ADS131A04-based calculation of RMS voltage for a 5 (at 50 Hz) or 6 (at 60 Hz) cycle frames of data. This array stores the last COMPUTATIONS_AGGREGATED number of these frames.
rms_current	int32_t [COMPUTATIONS_AGGREGATED]	The ADS131A04-based calculation of RMS current for a 5 (at 50 Hz) or 6 (at 60 Hz) cycle frames of data. This array stores the last COMPUTATIONS_AGGREGATED number of these frames.
sar_rms_voltage	int32_t [COMPUTATIONS_AGGREGATED]	The ADC104S021-based calculation of RMS voltage for a 5 (at 50 Hz) or 6 (at 60 Hz) cycle frames of data. This array stores the last COMPUTATIONS_AGGREGATED number of these frames.
sar_rms_current	int32_t [COMPUTATIONS_AGGREGATED]	The ADC104S021-based calculation of RMS current for a 5 (at 50 Hz) or 6 (at 60 Hz) cycle frames of data. This array stores the last COMPUTATIONS_AGGREGATED number of these frames.
V_min_out_of_range	Int16_t [COMPUTATIONS_AGGREGATED]	This variable stores the number of V_min mismatches. Each element stores the number of V_min mismatch for one 5 (at 50 Hz) or 6 (at 60 Hz) cycle frames of data.
V_max_out_of_range	Int16_t [COMPUTATIONS_AGGREGATED]	This variable stores the number of V_max mismatches. Each element stores the number of V_max mismatch for one 5 (at 50 Hz) or 6 (at 60 Hz) cycle frames of data.
I_min_out_of_range	Int16_t [COMPUTATIONS_AGGREGATED]	This variable stores the number of I_min mismatches. Each element stores the number of I_min mismatch for one 5 (at 50 Hz) or 6 (at 60 Hz) cycle frames of data.
I_max_out_of_range	Int16_t [COMPUTATIONS_AGGREGATED]	This variable stores the number of I_max mismatches. Each element stores the number of I_max mismatch for one 5 (at 50 Hz) or 6 (at 60 Hz) cycle frames of data.
frequency	int16_t	The mains voltage frequency calculated from the ADS131A04 voltage channel.
sar_frequency	int16_t	The mains voltage frequency calculated from the ADC104S021 voltage channel.

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表 37. Variable Names for Aggregated Metrology Parameters

VARIABLE NAME	VARIABLE TYPE	VARIABLE DESCRIPTION
active_power_aggregated	int32_t	The aggregated active power calculation that is taken by averaging a COMPUTATIONS_AGGREGATED number of frames of the 5 or 6 cycle active power readings calculated from the ADS131A04 ADC channels.
reactive_power_aggregated	int32_t	The aggregated active power calculation that is taken by averaging a COMPUTATIONS_AGGREGATED number of frames of the 5 or 6 cycle reactive power readings calculated from the ADS131A04 ADC channels.
apparent_power_aggregated	int32_t	The aggregated active power calculation that is taken by averaging a COMPUTATIONS_AGGREGATED number of frames of the 5 or 6 cycle apparent power readings calculated from the ADS131A04 ADC channels.
rms_voltage_aggregated	int32_t	The aggregated active power calculation that is taken by averaging a COMPUTATIONS_AGGREGATED number of frames of the 5 or 6 cycle RMS voltage readings calculated from the ADS131A04 ADC channels.
rms_current_aggregated	int32_t	The aggregated active power calculation that is taken by averaging a COMPUTATIONS_AGGREGATED number of frames of the 5 or 6 cycle RMS current readings calculated from the ADS131A04 ADC channels.
sar_rms_voltage_aggregated	int32_t	The aggregated active power calculation that is taken by averaging a COMPUTATIONS_AGGREGATED number of frames of the 5 or 6 cycle RMS voltage readings calculated from the ADC104S021 ADC channels.
sar_rms_current_aggregated	int32_t	The aggregated active power calculation that is taken by averaging a COMPUTATIONS_AGGREGATED number of frames of the 5 or 6 cycle RMS current readings calculated from the ADC104S021 ADC channels.

表 38. Variable Names of Arrays Used to Store all ADC Samples

VARIABLE NAME	VARIABLE TYPE	VARIABLE DESCRIPTION
channel_data	int32_t[8]	This array stores the raw ADC samples of the two ADS131A04 devices. The mapping of each element of the array is according to 表 7.
sar_channel_data	int16_t[8]	This sarray stores the raw ADC samples of the two ADC104S021 devices. The mapping of each element of the array is according to 表 7. This array is updated at half of the rate of the channel_data array.

表 39. Variable Names of Voltage and Current Samples of ADC104S021 and ADS131A04

VARIABLE NAME	VARIABLE TYPE	VARIABLE DESCRIPTION
results_current	int32_t[4000]	This array contains the last 4000 DC-filtered ADC samples of the ADS131A04 current channel.
results_voltage	int32_t[4000]	This array contains the last 4000 DC-filtered ADC samples of the ADS131A04 voltage channel.
SAR_results_current	int16_t[4000]	This array contains the last 4000 DC-filtered ADC samples of the ADC104S021 current channel.
SAR_results_voltage	int16_t[4000]	This array contains the last 4000 DC-filtered ADC samples of the ADC104S021 voltage channel.

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3.2.4 Calibration

Calibration is key to system performance. Different boards of this design (and even different channels within the same board) would exhibit different accuracies due to silicon-to-silicon differences, sensor accuracies, and other passive tolerances. To nullify these effects, the system must be calibrated. To perform calibration accurately, there must be an accurate AC test source and a reference meter available. The source must be able to generate any desired voltage, current, and phase shifts (between V and I). To calculate errors in measurement, the reference meter acts as an interface between the source and the meter being calibrated. This section discusses a simple and effective method of calibration of this design.

The received metrology values on the serial terminal can be used to calculate new calibration factors from the old calibration factors to give the least error in measurement. In this design, there are six main calibration factors for the ADS131A04:

- VOLTAGE_CALIBRATION_DS (voltage scaling factor)
- VOLTAGE_AC_OFFSET_DS (voltage AC offset factor)
- CURRENT_CALIBRATION_DS (current scaling factor)
- CURRENT_AC_OFFSET_DS (current AC offset factor)
- ACTIVE_POWER_CALIBRATION (active power scaling factor)
- PHASE_SHIFT_CALIBRATION (phase shift compensation factor)

For the ADC104S021, there are four main calibration factors:

- VOLTAGE_CALIBRATION_SAR (voltage scaling factor)
- VOLTAGE_AC_OFFSET_SAR (voltage AC offset factor)
- CURRENT_CALIBRATION_SAR (current scaling factor)
- CURRENT_AC_OFFSET_SAR (current AC offset factor)

The voltage, current, and power scaling factors translate measured quantities in metrology software to real-world values represented in volts, amps, and watts, respectively. The voltage AC offset and current AC offset are used to eliminate the effect of additive white Gaussian noise (AWGN) associated with each channel. This noise is orthogonal to everything except itself; as a result, this noise is only present when calculating RMS voltages and currents. The last calibration factor is the phase compensation factor, which is used to compensate any phase shifts introduced by the current sensors and other passives. Please note that the voltage, current, and power calibration factors are independent of each other. Therefore, calibrating voltage does not affect the readings for RMS current or power.

When the firmware is first loaded onto the MSP432, the default calibration factors are used. These default calibration values need to be modified in the source code during calibration. After modifying these calibration factors, the code must be recompiled and reloaded onto the MSP432 for the new calibration factors to be used.

3.2.4.1 Gain Calibration

To calibrate the voltage and current readings, follow these steps:

1. Connect an isolated UART-to-RS-232 board to the UART port that is used for sending metrology parameters and the RS-232 port of a computer. An example of a UART-to-RS-232 board is the TIDA-00163.
2. Open a terminal program for viewing the readings for voltage, current, and active power.
3. Configure the test source to supply desired voltage and current. Ensure that these are the voltage and current calibration points with a zero-degree phase shift between the voltage and current. For example,

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230 V, 10 A, 0º (PF = 1).

4. Based on the RMS voltage reading from the ADS131A04 devices, the actual RMS voltage supplied to the system, and the VOLTAGE_CALIBRATION_DS macro (from calibration.h), calculate a new value of the VOLTAGE_CALIBRATION_DS macro by using 式 10:

$$\left(\text{VOLTAGE\_CALIBRATION\_DS}_{\text{new}} \right) = \left(\text{VOLTAGE\_CALIBRATION\_DS}_{\text{old}} \right) \left(\frac{V_{\text{RMS, Supplied}}}{V_{\text{RMS, ADS131A04\_Reading}}} \right) \quad (10)$$

5. Replace the old value of VOLTAGE_CALIBRATION_DS in calibration.h with the VOLTAGE_CALIBRATION_DSNEW value calculated. For this macro, round to the nearest whole number.
6. Based on the RMS voltage reading from the ADC104S021 devices, the actual RMS voltage supplied to the system, and the VOLTAGE_CALIBRATION_SAR macro (from calibration.h), calculate a new value of the VOLTAGE_CALIBRATION_SAR macro by using 式 11:

$$\left(\text{VOLTAGE\_CALIBRATION\_SAR}_{\text{new}} \right) = \left(\text{VOLTAGE\_CALIBRATION\_SAR}_{\text{old}} \right) \left(\frac{V_{\text{RMS,Supplied}}}{V_{\text{RMS,ADC104S021\_Reading}}} \right) \quad (11)$$

7. Replace the old value of VOLTAGE_CALIBRATION_SAR in calibration.h with the VOLTAGE_CALIBRATION_SARNEW value calculated. For this macro, round to the nearest whole number.
8. Based on the RMS current reading from the ADS131A04 devices, the actual RMS current supplied to the system, and the CURRENT_CALIBRATION_DS macro (from calibration.h), calculate a new value of the CURRENT_CALIBRATION_DS macro by using 式 12:

$$\left(\text{CURRENT\_CALIBRATION\_DS}_{\text{new}} \right) = \left(\text{CURRENT\_CALIBRATION\_DS}_{\text{old}} \right) \left(\frac{I_{\text{RMS,Supplied}}}{I_{\text{RMS,ADS131A04\_Reading}}} \right) \quad (12)$$

9. Replace the old value of CURRENT_CALIBRATION_DS in calibration.h with the CURRENT_CALIBRATION_DSNEW value calculated. For this macro, round to the nearest whole number.
10. Based on the RMS current reading from the ADC104S021 devices, the actual RMS current supplied to the system, and the CURRENT_CALIBRATION_SAR macro (from calibration.h), calculate a new value of the CURRENT_CALIBRATION_SAR macro by using 式 13:

$$\left(\text{CURRENT\_CALIBRATION\_SAR}_{\text{new}} \right) = \left(\text{CURRENT\_CALIBRATION\_SAR}_{\text{old}} \right) \left(\frac{I_{\text{RMS,Supplied}}}{I_{\text{RMS,ADC104S021\_Reading}}} \right) \quad (13)$$

11. Replace the old value of CURRENT_CALIBRATION_SAR in calibration.h with the CURRENT_CALIBRATION_SARNEW value calculated. For this macro, round to the nearest whole number.
12. Based on the active power readings from the ADS131A04, the actual active power readings, and the ACTIVE_POWER_CALIBRATION macro (from calibration.h), calculate a new value of the ACTIVE_POWER_CALIBRATION macro by using 式 14:

$$\left(\text{ACTIVE\_POWER\_CALIBRATION}_{\text{new}} \right) = \left(\text{ACTIVE\_POWER\_CALIBRATION}_{\text{old}} \right) \left(\frac{P_{\text{ACT,actual}}}{P_{\text{ACT,ADS131A04\_Reading}}} \right) \quad (14)$$

13. Replace the old value of ACTIVE_POWER_CALIBRATION in calibration.h with the ACTIVE_POWER_CALIBRATIONNEW value calculated. For this macro, round to the nearest whole number.
14. Save calibration.h and load the code onto the MSP432 by clicking on the Run menu and selecting Debug as shown in 図 32:

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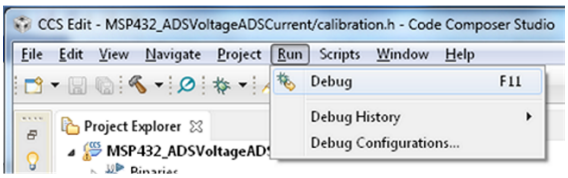

図 32. Loading Code on MSP432

3.2.4.2 Phase Correction

After performing power gain calibration, phase calibration must be performed. To perform phase correction calibration, follow these steps:

1. If the AC test source has been turned OFF or reconfigured, perform Steps 1 through 3 from 3.2.4.1 using the identical voltage and current used in that section.
2. Modify only the phase-shift to a non-zero value; typically, 60º is chosen.
3. Observe the active power readings and compare it to the actual active power value. Use these values to calculate the % error using 式 15:

$$\%_{error} = \left(\frac{P_{ACT,ADS131A04\_Reading}}{P_{ACT,actual}} - 1 \right) \times 100 \quad (15)$$

4. If the active power % error is not close to zero, or is unacceptable, perform phase correction by following these steps:
   a. Modify the PHASE_SHIFT_CALIBRATION macro to minimize the active power % error. Usually, a small ± integer should be entered to bring the error closer to zero. If increasing the PHASE_SHIFT_CALIBRATION scaling factor causes the absolute value of the active percent error to increase, then calibration should be performed by reducing the value of the PHASE_SHIFT_CALIBRATION scaling factor until the absolute value of active power % error is minimized. Alternatively, if increasing the PHASE_SHIFT_CALIBRATION scaling factor causes the absolute value of the active power percent error to decrease, then the PHASE_SHIFT_CALIBRATION scaling factor should be increased until the absolute value of the active power % error is minimized.
   b. Save calibration.h and load the code onto the MSP432 by clicking on the Run menu and selecting Debug as shown in 図 32.
   c. If this measurement error (%) is not accurate enough, fine tune by incrementing or decrementing by a value of 1 based on Step 4a and 4b. Note that, after a point, the fine-tuning will only result in the error oscillating on either side of zero. The value that has the smallest absolute error must be selected.
   d. Change the phase now to –60° and check if this error is still acceptable. Ideally, errors should be symmetric for same phase shift on lag and lead conditions.

After performing phase correction, calibration is complete.

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4 Testing and Results

4.1 Test Setup

図 33 shows the test setup.

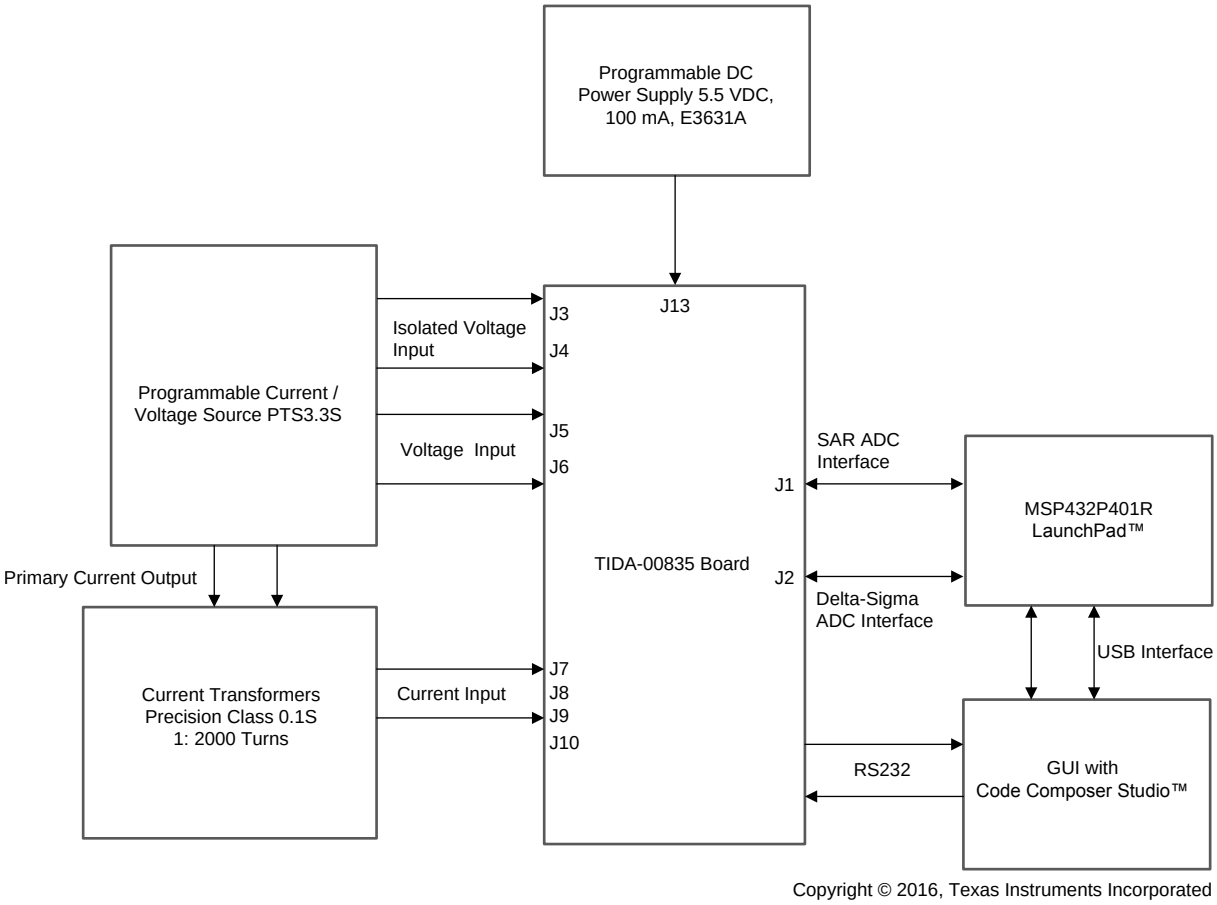

図 33. Test Setup for Testing AFE

The test setup for test the data acquisition AFE consists of the following:

- Current controlled DC power supply
- Accurate programmable voltage and current source with power factor
- External current transformer
- Voltage input from the AC source
- MSP432 LaunchPad interfaced to the AFE
- Computer to load the firmware and capture data from the AFE

4.2 Test Data

For these tests:

- All measurements in this section are RMS values
- The source uncertainty is ±0.05%
- Take care avoid opening the current outputs during testing

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- The inputs must be connected with the AC voltage and current source output programmed to 0 and the output switched off

4.2.1 Functional Testing

The functional testing was done by applying DC input and measuring the power supply output. The required AC RMS voltage and AC RMS currents were applied for testing the functionality of delta-sigma and SAR ADC. The AFE was interfaced to MSP432 LaunchPad for testing.

表 40 lists the test results.

表 40. AFE Functional Test Results

PARAMETERS	SPECIFICATIONS	OBSERVATIONS
Non-isolated power	5 V	4.978
	3.3 V	3.2987
	2.5 V	2.505
	–5.362 V	–5.358
	–2.5 V	–2.510
Isolated power	5 V	5.051
AFE	Current input 1—output DC offset	OK
	Current input 2—output DC offset	OK
	Current input 3—output DC offset	OK
	Current input 4—output DC offset	OK
	Non-isolated voltage 1—output DC offset	OK
	Non-isolated voltage 2—output DC offset	OK
	Current input 1—amplifier gain	OK
	Current input 2—amplifier gain	OK
	Current input 3—amplifier gain	OK
	Current input 4—amplifier gain	OK
	Non-isolated voltage 1—amplifier gain	OK
	Non-isolated voltage 2—amplifier gain	OK
AFE – isolated voltage measurement	Isolated amplifier 1 common-mode DC output	OK
	Isolated amplifier 2 common-mode DC output	OK
	Isolated amplifier 1 gain	?
	Isolated amplifier 2 gain	OK
Reference	ADC1 REFP out	2.441
	External ref 1 out	2.498
	Buffer 1 out	2.498
	Reference comparator 1 output	OK
	ADC2 REFP out	2.441
	External ref 2 out	2.5
	Buffer 2 out	2.5
	Reference comparator 2 output	OK

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表 40. AFE Functional Test Results (continued)

PARAMETERS	SPECIFICATIONS	OBSERVATIONS
Delta-sigma ADC input channels functionality	ADC1—CH0	OK
	ADC1—CH1	OK
	ADC1—CH2	OK
	ADC1—CH3	OK
	ADC2—CH0	OK
	ADC2—CH1	OK
	ADC2—CH2	OK
	ADC2—CH3	OK
SAR ADC input channels functionality	ADC1—CH0	OK
	ADC1—CH1	OK
	ADC1—CH2	OK
	ADC1—CH3	OK
	ADC2—CH0	OK
	ADC2—CH1	OK
	ADC2—CH2	OK
	ADC2—CH3	OK
Delta-sigma clock	16.385 oscillator	OK
	Clock buffer output 1	16.385 MHz
	Clock buffer output 2	16.385 MHz

4.2.2 Summary of Tests Performed

The focus of this TI Design is to test the performance of the following devices:

- ADS131EA04: The ADC performance was tested by applying voltage and current over a wide range and capturing waveforms for 100 ms and 1000 ms. The ADC sampling rate was fixed at 4000 samples. The accuracy testing was performed with a 2.442-V reference. Two delta-sigma ADCs were chained and the synchronization between ADCs was tested by measuring active power at UPF and 0.5 Lag.
- ADC104S021: The SAR ADC is for diagnostics and is to check if the input is measured within a range of the Delta-Sigma to confirm the Delta-Sigma performance is within a range.

表 41 lists the different test that have been performed.

表 41. Summary of Performance Tests Conducted

SERIAL NUMBER	TESTS	DETAILS
1	Unipolar_Input_with _ADC_REFPout_SignalConditioning	Power measurement: multiple devices synchronization
		Isolated and non-isolated voltage measurement: 1 sec
		Current measurement: 1 second
		Isolated and non-isolated voltage measurement: 100 ms
		Current measurement: 100 ms
2	Performance testing – Unipolar_Input_Ext reference for signal conditioning	Voltage, current, and power measurement
		Measurement with isolated voltage input
		Measurement with Rogowski integrator output
3	Performance testing – Bipolar_Input_Ext reference for signal conditioning	Voltage, current, and power measurement

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4.2.3 Performance Testing—Unipolar_Input_With_ADC_Refout_SignalConditioning

Delta-sigma ADCs positive reference voltage output was used for providing the DC common mode level shift to the AC inputs. This level shifting is required to make the op-amp gain output compatible to ADC input range when the ADC is configured for a 0- to 5-V input. Power measurements were averaged for 3 seconds (average multiple 1-second values) voltage and current measurements were taken for 1 second and 100 ms.

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4.2.3.1 Power Measurement—Multiple Devices Synchronization

The synchronization of multiple devices was verified by measuring the accuracy in the following combination in 表 42.

表 42. ADC Synchronization Combinations

COMBINATION	VOLTAGE	CURRENT
Combination1	ADC2	ADC2
Combination2	ADC2	ADC1

The voltage, current, power, and phase coefficients were kept the same for all combinations, and power accuracy for different current inputs was tested. The measurement accuracy was verified to be within ±0.5% in all conditions with no change in the phase error compensation factor in both conditions.

4.2.3.1.1 Non-Isolated Voltage × CT Input

表 43 and 表 44 provide power measurement accuracy readings for non-isolated voltage and CT input.

表 43. V (DS_ADC2) × I (DS_ADC2)

V-CH6	I-CH7	P-U	P-L	P-U-M	P-L-M	CH6_7 P-U-E	CH6_7 P-L-E	CH6_7 U-L-E
240	0.10	24	12	24.028	12.023	0.117	0.195	–0.079
240	0.25	60	30	60.029	30.038	0.048	0.125	–0.077
240	0.50	120	60	119.923	59.989	–0.064	–0.019	–0.045
240	1.00	240	120	239.804	120.035	–0.082	0.029	–0.111
240	2.50	600	300	599.326	299.813	–0.112	–0.062	–0.050
240	5.00	1200	600	1199.155	600.253	–0.070	0.042	–0.113
240	10.00	2400	1200	2401.153	1201.364	0.048	0.114	–0.066
240	15.00	3600	1800	3600.286	1800.730	0.008	0.041	–0.033
240	20.00	4800	2400	4798.003	2398.922	–0.042	–0.045	0.003
240	30.00	7200	3600	7194.587	3598.082	–0.075	–0.053	–0.022
240	50.00	12000	6000	11988.610	6000.167	–0.095	0.003	–0.098
240	75.00	18000	9000	17997.149	8996.299	–0.016	–0.041	0.025
240	100.00	24000	12000	23981.929	12003.501	–0.075	0.029	–0.104

表 44. V (DS_ADC2) × I (DS_ADC1)

V-CH6	I-CH0	P-U	P-L	P-U-M	P-L-M	CH6_0 P-U-E	CH6_0 P-L-E	CH6_0 U-L-E
240	0.10	24	12	24.026	12.011	0.107	0.094	0.013
240	0.25	60	30	60.017	30.015	0.029	0.052	–0.023
240	0.50	120	60	119.914	59.965	–0.072	–0.058	–0.014
240	1.00	240	120	240.213	120.112	0.089	0.093	–0.004
240	2.50	600	300	600.171	299.880	0.029	–0.040	0.069
240	5.00	1200	600	1198.956	600.389	–0.087	0.065	–0.152
240	10.00	2400	1200	2399.035	1200.578	–0.040	0.048	–0.088
240	15.00	3600	1800	3598.754	1802.319	–0.035	0.129	–0.163
240	20.00	4800	2400	4802.330	2399.025	0.049	–0.041	0.089
240	30.00	7200	3600	7202.061	3602.318	0.029	0.064	–0.036
240	50.00	12000	6000	12007.262	5999.039	0.061	–0.016	0.077
240	75.00	18000	9000	18021.525	8999.077	0.120	–0.010	0.130

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表 44. V (DS_ADC2) × I (DS_ADC1) (continued)

V-CH6	I-CH0	P-U	P-L	P-U-M	P-L-M	CH6_0 P-U-E	CH6_0 P-L-E	CH6_0 U-L-E
240	100.00	24000	12000	24028.951	12006.789	0.121	0.057	0.064

図 34 shows the graph for the previous two accuracy tables.

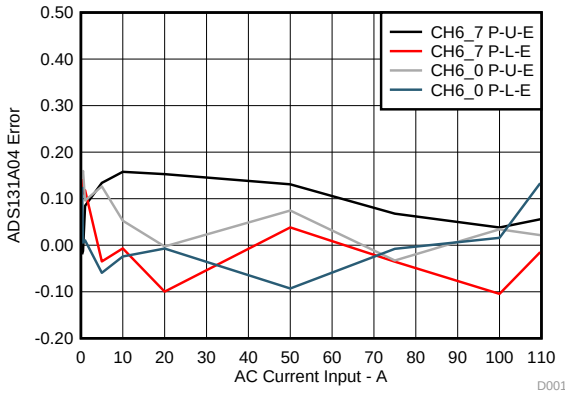

図 34. Power Measurement—ADC1 and ADC2

4.2.3.1.2 Isolated Voltage × CT Input

表 45 and 表 46 provide power measurement accuracy readings for isolated voltage and CT input.

表 45. V (DS_ADC2) × I (DS_ADC2)

V-CH4_Iso	I-CH5	P-U (W)	P-L (W)	P-U-M	P-L-M	CH4_5 P-U-E	CH4_5 P-L-E	CH4_5 U-L-E
240	0.25	60	30	60.035	30.050	0.058	0.167	–0.108
240	0.50	120	60	120.110	60.099	0.092	0.165	–0.073
240	1.00	240	120	240.434	120.276	0.181	0.230	–0.049
240	2.50	600	300	601.200	300.391	0.200	0.130	0.070
240	5.00	1200	600	1201.351	600.935	0.113	0.156	–0.043
240	10.00	2400	1200	2405.050	1201.960	0.210	0.163	0.047
240	15.00	3600	1800	3603.840	1800.921	0.107	0.051	0.055
240	20.00	4800	2400	4811.142	2401.129	0.232	0.047	0.185
240	30.00	7200	3600	7209.648	3605.880	0.134	0.163	–0.029
240	50.00	12000	6000	12022.727	6002.303	0.189	0.038	0.151
240	75.00	18000	9000	18015.882	9004.693	0.088	0.052	0.036
240	100.00	24000	12000	24022.446	12010.484	0.094	0.087	0.006

表 46. V (DS_ADC2) × I (DS_ADC1)

V-CH4_Iso	I-CH2	P-U	P-L	P-U-M	P-L-M	CH4_2 P-U-E	CH4_2 P-L-E	CH4_2 U-L-E
240	0.25	60	30	60.081	30.033	0.135	0.110	0.024
240	0.50	120	60	120.140	60.051	0.116	0.085	0.031
240	1.00	240	120	240.162	120.047	0.067	0.039	0.028
240	2.50	600	300	600.559	299.774	0.093	–0.075	0.169
240	5.00	1200	600	1200.798	601.080	0.067	0.180	–0.113
240	10.00	2400	1200	2403.026	1201.646	0.126	0.137	–0.011

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表 46. V (DS_ADC2) × I (DS_ADC1) (continued)

V-CH4_Iso	I-CH2	P-U	P-L	P-U-M	P-L-M	CH4_2 P-U-E	CH4_2 P-L-E	CH4_2 U-L-E
240	15.00	3600	1800	3601.895	1801.945	0.053	0.108	–0.055
240	20.00	4800	2400	4805.713	2399.741	0.119	–0.011	0.130
240	30.00	7200	3600	7207.286	3605.980	0.101	0.166	–0.065
240	50.00	12000	6000	12019.580	6013.253	0.163	0.221	–0.058
240	75.00	18000	9000	18030.600	9020.381	0.170	0.226	–0.056
240	100.00	24000	12000	24042.923	12025.172	0.179	0.210	–0.031

図 35 shows the graph for the previous two accuracy tables.

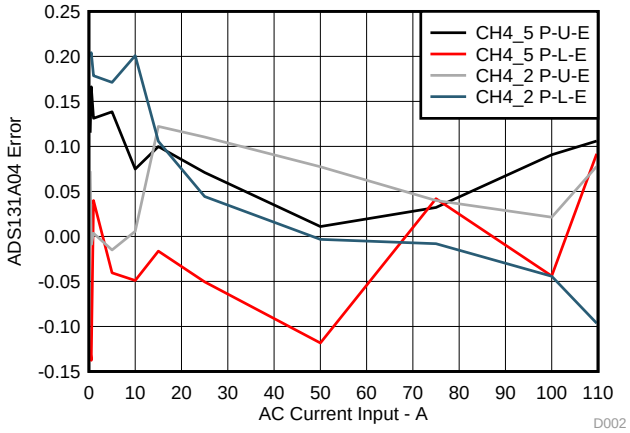

図 35. ISO_V_CT Power Measurement—ADC1 and ADC2

4.2.3.2 *Isolated and Non-Isolated Voltage and Current Measurement*

表 47 and 表 48 provide voltage and current measurement accuracies.

表 47. Voltage and Current Measurement Results 1 Second for ADC1—Isolated and Non-Isolated

APPLIED				MEASURED				% ERROR			
V-CH1	I-CH0	V-CH3-Iso	I-CH2	V-CH1	I-CH0	V-CH3-Iso	I-CH2	V-CH1	I-CH0	V-CH3-Iso	I-CH2
—	0.25	—	0.25	—	0.251	—	0.251	—	0.200	—	0.240
—	0.50	—	0.50	—	0.500	—	0.501	—	0.070	—	0.140
—	1.00	—	1.00	—	1.002	—	1.001	—	0.160	—	0.070
5	2.50	5	2.50	4.997	2.502	5.000	2.501	–0.060	0.076	–0.002	0.044
10	5.00	10	5.00	9.985	5.004	9.990	5.003	–0.150	0.088	–0.100	0.066
25	10.00	25	10.00	24.968	10.007	24.998	10.011	–0.128	0.067	–0.008	0.110
50	15.00	50	15.00	49.898	15.019	50.001	15.019	–0.204	0.127	0.002	0.127
100	20.00	100	20.00	99.832	20.039	100.056	20.030	–0.168	0.196	0.056	0.152
150	30.00	125	30.00	149.856	30.038	125.215	30.019	–0.096	0.127	0.172	0.063
200	50.00	150	50.00	199.965	50.076	150.119	50.074	–0.017	0.151	0.079	0.148
250	75.00	200	75.00	249.980	75.056	200.169	75.043	–0.008	0.075	0.085	0.057
300	100.00	250	100.00	299.818	100.142	250.215	100.043	–0.061	0.142	0.086	0.043

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表 48. Voltage and Current Measurement Results 1 Second for ADC2—Isolated and Non-Isolated

APPLIED				MEASURED				% ERROR			
V-CH4-Iso	I-CH5	V-CH6	I-CH7	V-CH4-Iso	I-CH5	V-CH6	I-CH7	V-CH4-Iso	I-CH5	V-CH6	I-CH7
—	0.25	—	0.25	—	0.251	—	0.251	—	0.340	—	0.300
—	0.50	—	0.50	—	0.501	—	0.501	—	0.220	—	0.280
—	1.00	—	1.00	—	1.001	—	1.002	—	0.140	—	0.230
5	2.50	5	2.50	4.999	2.502	4.999	2.502	–0.020	0.079	–0.022	0.096
10	5.00	10	5.00	9.988	5.002	9.989	5.004	–0.120	0.035	–0.111	0.088
25	10.00	25	10.00	24.972	10.010	24.983	10.004	–0.112	0.099	–0.069	0.040
50	15.00	50	15.0	50.025	15.032	49.909	15.003	0.050	0.213	–0.181	0.023
100	20.00	100	20.00	100.027	20.013	99.956	20.016	0.027	0.067	–0.044	0.082
125	30.00	150	30.00	125.114	30.031	149.872	30.003	0.091	0.103	–0.085	0.009
150	50.00	200	50.00	149.945	50.054	199.910	50.074	–0.037	0.108	–0.045	0.147
200	75.00	250	75.00	200.175	75.102	249.951	75.012	0.088	0.136	–0.020	0.016
250	100.00	300	100.00	250.390	100.154	300.108	100.058	0.156	0.154	0.036	0.058

図 36 shows the graph for current measurement of ADC1 and ADC2.

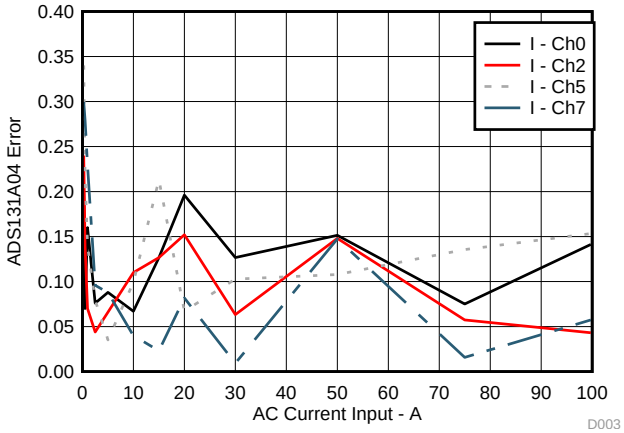

図 36. Voltage Current Measurement—ADC1 and ADC2

4.2.3.3 Isolated and Non-Isolated Voltage and Current Measurement (100 ms)

表 49, 表 50, 表 51, and 表 52 show measurement accuracies for voltages and currents.

表 49. 100-ms Current Measurement for ADC2—CH5

I-CH5-A	MEASURED		% ERROR	
	100 ms	1 sec	100 ms	1 sec
0.5	0.5000	0.5008	0.0010	0.1665
1.0	1.0006	1.0021	0.0583	0.2081
5.0	5.0192	5.0098	0.3839	0.1957
10.0	10.0256	10.0191	0.2564	0.1914
20.0	20.0229	20.0318	0.1144	0.1591
50.0	49.9967	50.0768	–0.0066	0.1535
100.0	100.2778	100.1970	0.2778	0.1970
110.0	110.1756	110.2830	0.1597	0.2572

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表 50. 100-ms Current for ADC1—CH0

I-CH0-A	MEASURED		% ERROR	
	100 ms	1 sec	100 ms	1 sec
0.5	0.5007	0.4990	0.1470	–0.1920
1.0	1.0011	0.9997	0.1149	–0.0300
2.5	2.5026	2.4958	0.1055	–0.1684
10.0	10.0077	10.0006	0.0768	0.0060
20.0	20.0284	20.0244	0.1420	0.1222
50.0	50.0643	50.0340	0.1286	0.0680
75.0	75.0832	75.0914	0.1109	0.1219
100.0	100.2538	100.2134	0.2538	0.2134
110.0	110.2736	110.0939	0.2487	0.0854

表 51. Isolated Voltage Measurement for AMC1200

V-CH4-V	MEASURED		% ERROR	
	100 ms	1 sec	100 ms	1 sec
10	9.981	9.972	–0.190	–0.280
25	24.977	24.955	–0.092	–0.180
110	109.883	109.864	–0.106	–0.124
240	240.087	240.003	0.036	0.001
260	260.186	259.982	0.072	–0.007

表 52. Voltage With PD for ADC1

V-CH1-V	MEASURED		% ERROR	
	100 ms	1 sec	100 ms	1 sec
10	9.986	9.987	–0.140	–0.130
25	24.967	24.913	–0.132	–0.348
110	109.907	109.768	–0.085	–0.211
240	240.024	239.836	0.010	–0.068
300	300.101	299.463	0.034	–0.179

4.2.4 Performance Testing—Unipolar_Input_Ext_reference for Signal Conditioning

4.2.4.1 Voltage, Current, and Power Measurement

表 53 and 表 54 lists the measurement accuracy for voltages, currents, and power measurement.

表 53. V (DS_ADC2) × I (DS_ADC2) With External Reference for Signal Conditioning

ACTUAL				MEASURED				% ERROR			
V-CH6	I-CH7	P-UPF	P-Lag	I-CH7 (100 ms)	I-CH7 (1 sec)	P-ADC2 (UPF)	P-ADC2 (0.5 Lag)	I-CH7 (100 ms E)	I-CH7 (1 sec E)	CH6_7 P_U_E	CH6_7 P_L_E
240	0.05	12	6	0.05	0.05	12.07	—	0.88	0.97	0.58	—
240	0.10	24	12	0.10	0.10	24.04	12.06	0.65	0.42	0.19	0.47
240	0.25	60	30	0.25	0.25	59.99	30.04	0.37	0.22	–0.02	0.15
240	0.50	120	60	0.50	0.50	119.98	60.07	0.27	0.20	–0.01	0.11
240	1.00	240	120	1.00	1.00	240.20	120.14	0.33	0.25	0.08	0.12
240	5.00	1200	600	5.01	5.01	1201.61	599.79	0.27	0.24	0.13	–0.03

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表 53. V (DS_ADC2) × I (DS_ADC2) With External Reference for Signal Conditioning (continued)

ACTUAL				MEASURED				% ERROR			
V-CH6	I-CH7	P-UPF	P-Lag	I-CH7 (100 ms)	I-CH7 (1 sec)	P-ADC2 (UPF)	P-ADC2 (0.5 Lag)	I-CH7 (100 ms E)	I-CH7 (1 sec E)	CH6_7 P_U_E	CH6_7 P_L_E
240	10.00	2400	1200	10.02	10.03	2403.78	1199.92	0.22	0.26	0.16	–0.01
240	20.00	4800	2400	20.05	20.05	4807.33	2397.61	0.24	0.26	0.15	–0.10
240	50.00	12000	6000	50.11	50.12	12015.71	6002.29	0.23	0.23	0.13	0.04
240	75.00	18000	9000	75.17	75.16	18012.21	8996.82	0.22	0.21	0.07	–0.04
240	100.00	24000	12000	100.34	100.29	24009.14	11987.44	0.34	0.29	0.04	–0.10
240	110.00	26400	13200	110.29	110.24	26414.87	13198.40	0.26	0.22	0.06	–0.01

表 54. V (DS_ADC2) × I (DS_ADC1) With External Reference for Signal Conditioning

ACTUAL				MEASURED				% ERROR			
V-CH6	I-CH0	P-UPF	P-Lag	I-CH0 (100 ms)	I-CH0 (1 sec)	P-ADC2 (UPF)	P-ADC2 (0.5 Lag)	I-CH0 (100 ms E)	I-CH0 (1 sec E)	CH6_0 P_U_E	CH6_0 P_L_E
240	0.05	12	6	0.05	0.05	12.01	—	0.22	0.14	0.07	—
240	0.10	24	12	0.10	0.10	24.01	12.02	0.14	0.10	0.05	0.16
240	0.25	60	30	0.25	0.25	60.09	30.04	0.03	0.05	0.14	0.14
240	0.50	120	60	0.50	0.50	120.19	60.00	0.05	0.03	0.16	0.01
240	1.00	240	120	1.00	1.00	240.23	120.01	0.05	0.02	0.10	0.01
240	5.00	1200	600	5.00	5.00	1201.52	599.64	0	0.01	0.13	–0.06
240	10.00	2400	1200	10.00	10.00	2401.26	1199.71	0.04	–0.01	0.05	–0.02
240	20.00	4800	2400	20.00	19.99	4799.86	2399.83	–0.01	–0.04	0	–0.01
240	50.00	12000	6000	50.04	49.99	12008.94	5994.42	0.09	–0.02	0.07	–0.09
240	75.00	18000	9000	75.02	74.94	17994.07	8999.29	0.02	–0.07	–0.03	–0.01
240	100.00	24000	12000	99.96	99.97	24008.17	12001.91	–0.04	–0.03	0.03	0.02
240	110.00	26400	13200	109.97	109.97	26405.59	13218.07	–0.03	–0.03	0.02	0.14

図 37 shows the graph plot for power measurement accuracies.

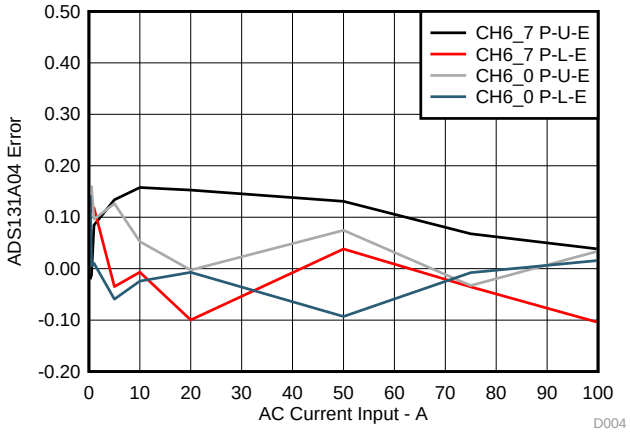

図 37. 0- to 5-V External Reference Power Measurement—ADC1 and ADC2

表 55 lists voltage measurement values and % error for different inputs.

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表 55. Voltage Measurement With External Reference for Signal Conditioning

V-CH6	V-CH6 (100 ms)	V-CH6 (1 sec)	V-CH6 (100 ms E)	V-CH6 (1 sec E)
320	320.580	320.340	0.180	0.100
300	300.520	300.260	0.170	0.090
270	270.430	270.100	0.160	0.040
240	240.280	240.130	0.120	0.050
200	200.160	200.010	0.080	0.010
110	110.040	110.000	0.040	0
50	50.010	50.010	0.020	0.020
25	25.000	25.000	0.010	0
10	10.000	9.990	0	–0.060
5	5.000	5.000	0.020	–0.040
2	1.987	1.985	–0.653	–0.754

4.2.4.2 Measurement With Isolated Voltage

表 56 and 表 57 lists measurement values for voltages, current, and power for the AMC1301 isolation amplifier.

表 56. AMC1301_CT_V (DS_ADC2) × I (DS_ADC2) External Reference for Signal Conditioning

ACTUAL			MEASURED				% ERROR		
V-CH4	I-CH7	P-UPF	P-Lag	I-CH7 (1 sec)	P-ADC2 (UPF)	P-ADC2 (0.5 Lag)	I-CH7 (1 sec E)	CH4_7 P_U_E	CH4_ P_L_E
240	0.05	12	6	0.0503	12.0020	—	0.5106	0.0163	—
240	0.10	24	12	0.1000	23.9769	12.0324	–0.0184	–0.0964	0.2697
240	0.25	60	30	0.2501	60.0268	30.0545	0.0204	0.0447	0.1818
240	0.50	120	60	0.5000	120.0977	60.1559	–0.0012	0.0814	0.2598
240	1.00	240	120	0.9999	239.9880	120.2570	–0.0145	–0.0050	0.2142
240	5.00	1200	600	4.9992	1200.5924	601.5347	–0.0161	0.0494	0.2558
240	10.00	2400	1200	10.0008	2401.7509	1203.1460	0.0076	0.0730	0.2622
240	20.00	4800	2400	20.0071	4797.7964	2408.0910	0.0354	–0.0459	0.3371
240	50.00	12000	6000	50.0194	11998.3258	6014.3322	0.0388	–0.0140	0.2389
240	75.00	18000	9000	75.0208	17992.2326	9020.0764	0.0277	–0.0432	0.2231
240	100.00	24000	12000	100.0097	24008.2497	12031.0991	0.0097	0.0344	0.2592
240	110.00	26400	13200	110.0359	26387.648	13239.6747	0.0327	–0.0468	0.3006

表 57. Isolated Voltage Measurement With AMC1301

V-CH4	V-CH4 (100 ms)	V-CH4 (1 sec)	V-CH4 (100 ms E)	V-CH4 (1 sec E)
300	298.685	298.816	–0.4403	–0.3962
270	270.010	269.703	0.0037	–0.1101
240	239.938	239.729	–0.0258	–0.1130
200	199.864	199.765	–0.0680	–0.1176
110	109.842	109.782	–0.1438	–0.1986
50	49.900	49.860	–0.2004	–0.2808
25	24.947	24.940	–0.2125	–0.2406
10	9.977	9.973	–0.2305	–0.2707

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表 57. Isolated Voltage Measurement With AMC1301 (continued)

V-CH4	V-CH4 (100 ms)	V-CH4 (1 sec)	V-CH4 (100 ms E)	V-CH4 (1 sec E)
5	4.989	4.984	–0.2205	–0.3210

4.2.4.3 Measurement With Rogowski Interface

表 58 lists the current and power measurement values with the current input provided from the TIDA-00777 Rogowski coil with an op-amp based active integrator.

表 58. Measurement With AMC1301 Rogowski Hardware Integrator Interface

ACTUAL				MEASURED				% ERROR			
V-CH4	I-CH5	P-ADC2 (UPF)	P-ADC2 (0.5 Lag)	I-CH5 (100 ms)	I-CH5 (1 sec)	P-ADC2 (UPF)	P-ADC2 (0.5 Lag)	I-CH5 (100 ms E)	I-CH5 (1 sec E)	P-ADC2 (UPF)	P-ADC2 (0.5 Lag)
240	0.5	120	60	0.503	0.500	119.779	—	0.644	–0.048	–0.184	—
240	1.0	240	120	0.999	1.002	239.909	120.259	–0.090	0.217	–0.038	0.216
240	5.0	1200	600	4.998	5.002	1201.324	601.253	–0.047	0.042	0.110	0.209
240	10.0	2400	1200	10.022	10.001	2401.833	1201.903	0.218	0.010	0.076	0.159
240	15.0	3600	1800	15.026	15.012	3606.843	1802.673	0.176	0.081	0.190	0.148
240	25.0	6000	3000	25.036	25.009	6009.882	3000.188	0.144	0.036	0.165	0.006
240	50.0	12000	6000	50.068	49.982	12014.866	6010.210	0.136	–0.035	0.124	0.170
240	75.0	18000	9000	75.118	75.066	18032.983	9011.041	0.157	0.088	0.183	0.123
240	100.0	24000	12000	100.131	99.980	24014.035	12009.353	0.131	–0.020	0.058	0.078
240	110.0	26400	13200	109.914	110.105	26432.057	13205.314	–0.078	0.096	0.121	0.040
240	120.0	28800	14400	119.913	120.144	28832.774	14404.842	–0.073	0.120	0.114	0.034

4.2.5 Performance Testing—Bipolar_Input_Ext Reference for Signal Conditioning

4.2.5.1 Voltage, Current, and Power Measurement

表 59 and 表 60 lists the measurement errors for current and power with the ADC configured in bipolar input mode.

表 59. V (DS_ADC2) × I (DS_ADC2) With Bipolar Input

ACTUAL				MEASURED				% ERROR			
V-CH6	I-CH7	P-UPF	P-Lag	I-CH7 (100 ms)	I-CH7 (1 sec)	P-ADC2 (UPF)	P-ADC2 (0.5 Lag)	I-CH7 (100 ms E)	I-CH7 (1 sec E)	CH6_7 P_U_E	CH6_7 P_L_E
240	0.25	60	30	0.25	0.25	60.06	29.96	0.11	0.02	0.11	–0.12
240	0.50	120	60	0.50	0.50	120.20	59.92	0.12	0.02	0.17	–0.14
240	1.00	240	120	1.00	1.00	240.31	120.05	0.15	0.03	0.13	0.04
240	5.00	1200	600	5.01	5.00	1201.66	599.76	0.10	0.02	0.14	–0.04
240	10.00	2400	1200	10.02	10.00	2401.79	1199.41	0.17	–0.03	0.07	–0.05
240	150.0	3600	1800	15.03	15.01	3603.59	1799.71	0.23	0.04	0.10	–0.02
240	25.00	6000	3000	25.03	25.03	6004.26	2998.49	0.14	0.14	0.07	–0.05
240	50.00	12000	6000	50.04	50.03	12001.32	5992.90	0.08	0.06	0.01	–0.12
240	75.00	18000	9000	75.09	75.03	18005.78	9003.77	0.12	0.04	0.03	0.04

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表 59. V (DS_ADC2) × I (DS_ADC2) With Bipolar Input (continued)

ACTUAL				MEASURED				% ERROR			
V-CH6	I-CH7	P-UPF	P-Lag	I-CH7 (100 ms)	I-CH7 (1 sec)	P-ADC2 (UPF)	P-ADC2 (0.5 Lag)	I-CH7 (100 ms E)	I-CH7 (1 sec E)	CH6_7 P_U_E	CH6_7 P_L_E
240	100.00	24000	12000	100.11	100.06	24021.77	11994.73	0.11	0.06	0.09	–0.04
240	110.00	26400	13200	110.12	110.11	26428.11	13212.66	0.11	0.10	0.11	0.10

表 60. V (DS_ADC2) × I (DS_ADC1) With Bipolar Input

ACTUAL				MEASURED				% ERROR			
V-CH6	I-CH2	P-UPF	P-Lag	I-CH2 (100 ms)	I-CH2 (1 sec)	P-ADC2 (UPF)	P-ADC2 (0.5 Lag)	I-CH2 (100 ms E)	I-CH2 (1 sec E)	CH6_2 P_U_E	CH6_2 P_L_E
240	0.25	60	30	0.25	0.25	60.05	30.06	0.05	0	0.08	0.20
240	0.50	120	60	0.50	0.50	119.99	60.12	0.04	–0.08	–0.01	0.20
240	1.00	240	120	1.00	1.00	240.01	120.21	0.08	–0.05	0	0.18
240	5.00	1200	600	5.00	5.00	1199.82	601.03	0.09	–0.08	–0.02	0.17
240	10.00	2400	1200	10.01	9.99	2400.14	1202.41	0.13	–0.06	0.01	0.20
240	15.00	3600	1800	15.01	15.00	3604.40	1801.90	0.09	0	0.12	0.11
240	25.00	6000	3000	25.03	25.00	6006.63	3001.33	0.12	0	0.11	0.04
240	50.00	12000	6000	50.05	50.02	12009.29	5999.80	0.10	0.04	0.08	0
240	75.00	18000	9000	75.03	74.96	18007.18	8999.28	0.04	–0.06	0.04	–0.01
240	100.00	24000	12000	100.06	99.94	24005.12	11994.68	0.06	–0.06	0.02	–0.04
240	110.00	26400	13200	110.08	110.01	26421.00	13187.06	0.07	0.01	0.08	–0.10

表 61 lists voltage measurement accuracy with the ADC configured in bipolar input mode.

表 61. Voltage Measurement With Bipolar Input

V-CH6	V-CH6 (100 ms)	V-CH6 (1 sec)	V-CH6 (100 ms E)	V-CH6 (1 sec E)
300	300.82	300.45	0.27	0.15
270	270.61	270.43	0.23	0.16
240	240.49	240.41	0.20	0.17
200	200.38	200.35	0.19	0.18
110	110.14	110.15	0.13	0.14
50	50.05	50.03	0.10	0.07
25	25.02	25.02	0.09	0.10
10	10.01	10.00	0.08	0.02
5	5.00	5.00	0.06	0.06

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4.2.6 Summary

表 62 summarizes the different tests and the observation completed for this TI Design.

表 62. Test Results Summary for ADS131A04 AFE With Reinforced Isolation

SERIAL NUMBER	PARAMETERS	OBSERVATIONS
1	Non-isolated power supply	OK
2	Isolated power supply	OK
3	Gain amplifier output—current and voltage	OK
4	Reference output—internal and external	OK
5	ADC interface to MCU	OK
6	Clock buffer output	OK
7	Measurement of voltage and current with different analog input voltage ranges	OK
8	Multiple ADC synchronization test for accuracy	Accuracy within ±0.5% in all combinations
9	Voltage measurement accuracy • Isolated or non isolated • Bipolar or unipolar	Within ±0.5%
10	Current measurement accuracy—bipolar or unipolar	Within ±0.5%
11	Active power measurement accuracy—bipolar or unipolar	Within ±0.5%

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5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-00835.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00835.

5.3 PCB Layout Recommendations

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00835.

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-00835.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00835.

6 Software Files

To download the software files, see the design files at TIDA-00835.

7 Related Documentation

1. Texas Instruments, *ADC124S101EVM BoosterPack User's Guide* (SNAU166)
2. Texas Instruments, *ADS131A04 24-bit, Delta-Sigma Analog-to-Digital Converter Evaluation Module* (SBAU259)
3. Texas Instruments, *Tripping Point: Isolation amplifier-based alternating current voltage measurement in protection relays*, TI E2E Community
4. Texas Instruments, *High-Resolution, Fast Start-Up, Delta-Sigma ADC-Based AFE for Air Circuit Breaker (ACB) Reference Design*, TIDA-00661 Design Guide (TIDUB80)
5. Texas Instruments, *Active Integrator for Rogowski Coil Reference Design With Improved Accuracy for Relays and Breakers*, TIDA-00777 Design Guide (TIDUBY4)
6. Texas Instruments, *Reference Design to Measure AC Voltage and Current in Protection Relay With Delta-Sigma Chip Diagnostics*, TIDA-00810 Design Guide (TIDUBY7)
7. Texas Instruments, *Flat-Clamp TVS Based Reference Design for Protection Against Transients for Grid Applications*, TIDA-010008 Design Guide (TIDUEC1)

7.1 商標

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8 Terminology

CT— Current transformer

RTU— Remote terminal unit

DTU— Distribution terminal unit

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FTU— Feeder terminal unit

PD— Potential divider

9 About the Authors

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資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (November 2016) から **Revision B** に変更 **Page**

- REF3425、REF3440、TLV9061、OPA4171、TVS0500製品フォルダへのリソース・リンクを 追加 1
- 特長の情報を 変更 1
- 最初のページからブロック図を 削除 2
- descriptions in 表 1 変更 7
- OPA4171 to 1.8.2.1 追加 10
- information in 1.8.2.3 変更 10
- information in 1.8.2.4 変更 10
- 2.1.5 追加 19
- OPA4171 to 2.2 title 追加 20
- information regarding OPA4171 to 2.2 追加 21
- information regarding TVS0500 to 2.2.1 追加 22
- units in 表 4 変更 22
- units in 表 5 変更 25
- link to the TIDA-010008 Design Guide in 7 追加 88

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- プレビューのドラフト版から 変更 1

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