参考資料

TI Designs: TIPD216
クワッド・チャネルの産業用電圧および電流出力ドライバのリファレンス・デザイン（EMC/EMIテスト済み）

概要

このクワッド・チャネル、アナログ出力モジュールは、高度に統合されたDAC8775アナログ・フロントエンド(AFE)を使用して、電圧および電流を出力します。適合型電力管理が内蔵されており、チップの消費電力を最小化します。さらに、IEC61000-4の一連のテストへの耐性を実現するために外部保護回路が実装されています。

リソース

TIPD216	デザイン・フォルダ
DAC8775	プロダクト・フォルダ

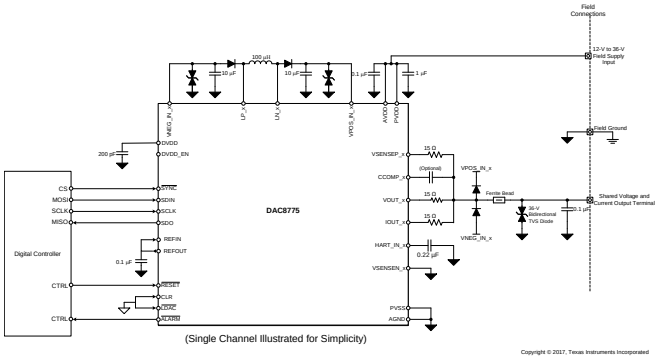
TI E2E™ Community　E2E エキスパートに質問

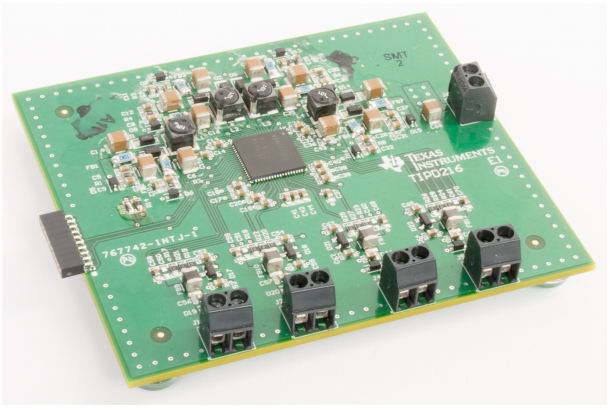
特長

- ファクトリ・オートメーションや制御用のクワッド・チャネルのアナログ出力
- 4mA～20mAの電流出力
- ±10Vの電圧出力
- 12V～36Vの入力電源範囲
- 電流出力用の適合型電力管理
- IEC61000-4のESD、EFT、放射エミッションについてクラスAの結果、IEC61000-4の放射耐性および伝導耐性についてクラスBの結果、詳細は 2.1.1.2を参照

アプリケーション

- ファクトリ・オートメーション/制御
- ビルディング・オートメーション
- モーター駆動





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1 System Overview

1.1 System Description

This system accepts supply voltages in the range of 12 V to 36 V which accommodates common industrial supply voltages and produces four independent voltage or current sources with programmable ranges commonly used in factory automation and control applications. The 16-bit voltage and current outputs each realize less than 0.1% full-scale range (FSR) of total unadjusted error (TUE) at room temperature. The system uses adaptive power management to minimize the power dissipation of the chip.

1.1.1 Analog Front End

The following subsections show simplified versions of each of the subcircuits inside the DAC8775 used to deliver the voltage and current outputs common for analog output modules. A similar scheme can be used to implement a discrete solution. A 5-V digital-to-analog converter (DAC) drives the inputs for both the voltage (V_{OUT}) and current (I_{OUT}) output stages. The DAC uses an accurate, low-drift reference voltage (V_{REF}) for strong DC performance.

1.1.2 I_{OUT} Circuitry

図 1 shows a simplified version of the I_{OUT} circuit, which consists of a bidirectional, precision current source. The circuit is composed of a high-side current source and a low-side current sink using amplifiers A1 and A2, two MOSFETs, and two sense resistors (R_{SENSE}). This stage provides a current output according to the 16-bit DAC code and is supplied by dual buck-boost converters with adaptive power management to minimize the power dissipation of the chip. Only one of the current stages are active at any given time, for example when sourcing current the sinking NMOS node is driven to high-impedance while the sourcing PMOS is driven to source current.

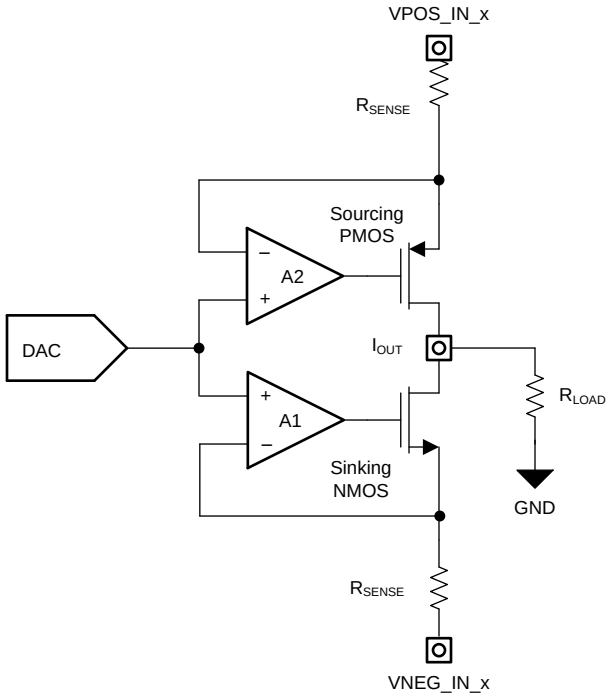

図 1. DAC8775 Current Output

1.1.3 V_{OUT} Circuitry

The V_{OUT} circuit is composed of amplifiers A3 and A4. The resistor network consisting of RFB, RG1, RG2, R0, R1, R2, R3, and R4 determine the gain. The DAC controls the non-inverting input and the inverting input has one path to GND and a second path to reference voltage REFIN. This configuration allows the single-ended DAC to create both the unipolar 0- to 5-V and 0- to 10-V outputs and the bipolar ±5-V and ±10-V outputs. The resistor switching network is used to change the values of RG1 and RG2 depending on the selected voltage output range.

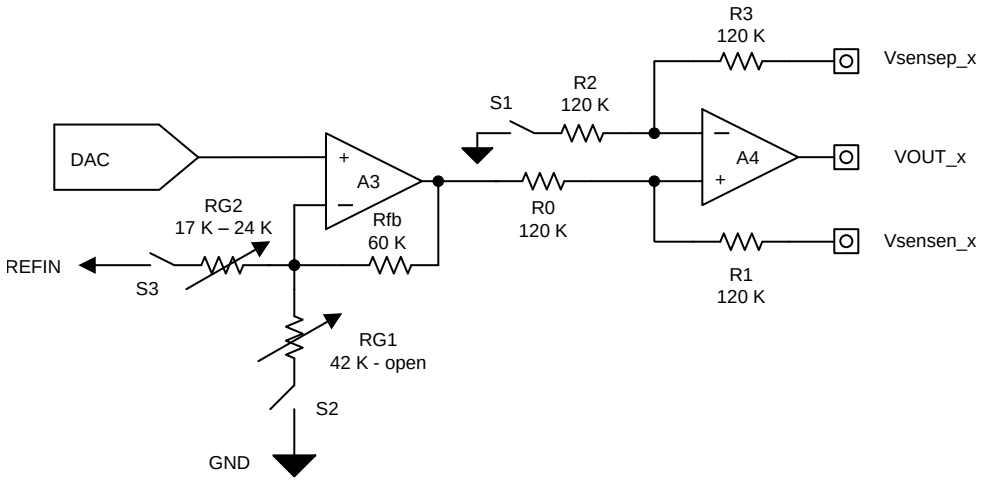

図 2. DAC8775 Voltage Output

1.1.4 Buck-Boost Converter

The DAC8775 includes a buck-boost converter to minimize the power dissipation of the chip and provide significant system integration. The buck-boost converter is based on single-inductor multiple output (SIMO) architecture. The converter requires a single inductor per channel to generate all the required analog power supplies.

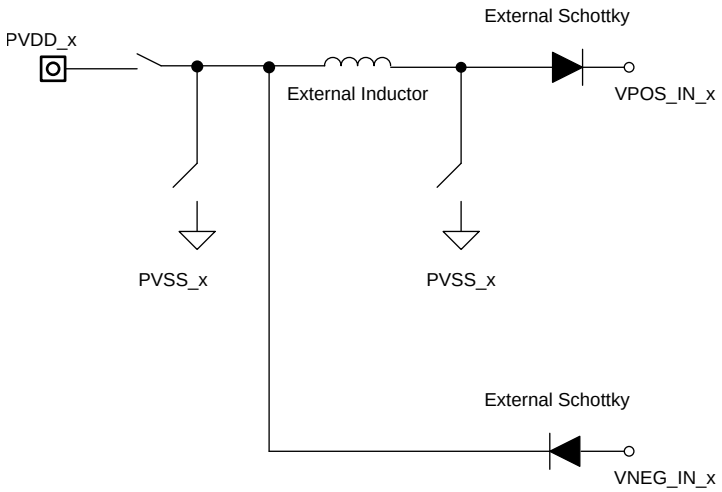

図 3. DAC8775 Buck-Boost Converter

1.1.5 FCC Radiated Emissions

Radiated emission testing consists of measuring the electromagnetic field strength of the emissions that are intentionally or unintentionally generated by the board. The receiving antenna, in horizontal and vertical positions, picks up the electromagnetic field from the device under test within a frequency band of 30 MHz to 1 GHz.

1.1.6 IEC61000-4 Immunity

Many transient signals or radiated emissions that are common in industrial applications can cause electrical overstress (EOS) damage or other disruptions to unprotected systems. IEC61000-4 is a test suite that simulates these transient and emission signals and awards a certification to systems that prove to be immune.

During each of the IEC61000-4 tests, the output of the equipment under test (EUT) is monitored for deviations or total failure. Results are assigned one of four class ratings for each test. The classes are listed and described in 表 1.

表 1. IEC61000-4 Classes

GRADE	DESCRIPTION
Class A	Normal performance within an error band specified by the manufacturer
Class B	Temporary loss of function or degradation of performance which ceases after the disturbance is removed; the equipment under test recovers its normal performance without operator interference
Class C	Temporary loss of function or degradation of performance; correction of performance requires operator intervention
Class D	Loss of function or degradation of performance which is not recoverable; permanent damage to hardware or software, or loss of data

Full details of each of the IEC61000-4 tests are licensed by the IEC and must be purchased.

1.1.6.1 IEC61000-4-2

IEC61000-4-2 is the electrostatic discharge (ESD) immunity test. This test simulates the electrostatic discharge (ESD) of an operator directly onto an electrical component. To simulate this event, an ESD generator applies ESD pulses to the EUT either through air discharge or through vertical and horizontal coupling planes. Air discharge tests are conducted near any exposed I/O terminal.

The ESD test pulse is a high-frequency transient with a pulse period of less than 100 ns. The pulse is a high-voltage signal, ranging from 4 kV to 15 kV depending on the threat level appropriate for the EUT. The complete ESD test requires ten sequential discharges of each positive and negative polarity for each test configuration.

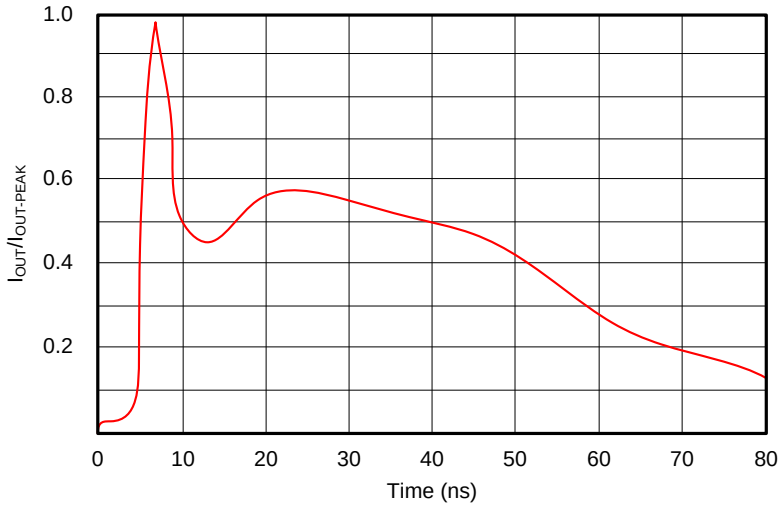

図 4. IEC61000-4 ESD Test Pulse

1.1.6.2 IEC61000-4-3

IEC61000-4-3 is the radiated immunity (RI) test. This test simulates exposure to high-frequency radiated emissions, such as radio devices or other emissions common in industrial processes. The frequency range and field strength of the radiated signals vary in this test based on the type of EUT. For this design, the tested frequency range was 80 MHz to 1 GHz and the field strength was 20 V/m.

1.1.6.3 EC61000-4-4

IEC61000-4-4 is the burst immunity, or electrically fast transient (EFT) test. This test simulates day-to-day switching transients from various sources in a typical industrial application space. The test is performed on power, signal, and earth wires—or a subset depending on what is appropriate for the EUT.

In this test a burst generator produces a series of EFT bursts, each lasting 15 ms with 300 ms in between bursts (see 図 5). The pulse rate of each burst is approximately 5 kHz. A typical test exposes the EUT to 1 to 3 minutes of EFT bursts. Similar to the ESD test pulse, the EFT pulses are a high-frequency signal but the magnitude of the EFT test pulse only ranges from 0.25 kV to 4 kV. Bursts of both positive and negative polarity are applied.

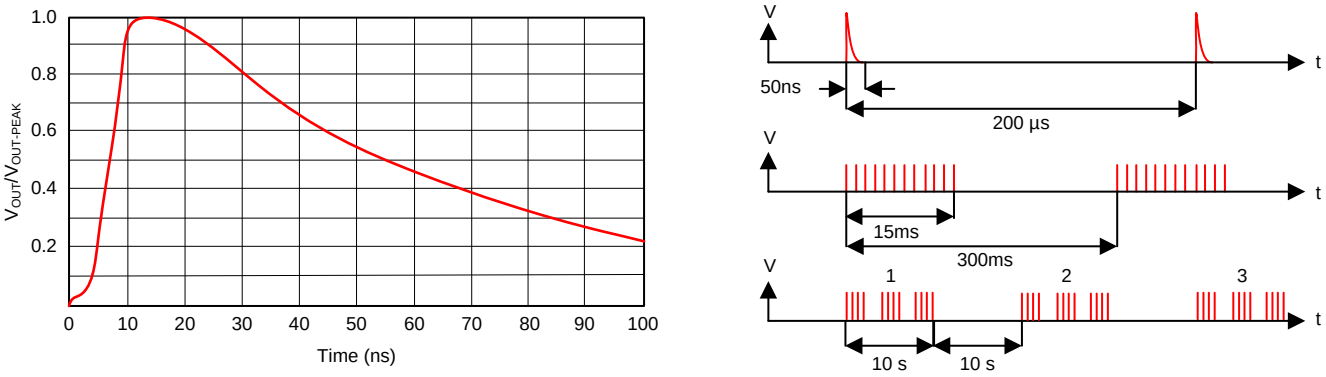

図 5. IEC61000-4-4 EFT Test Pulses

1.1.6.4 IEC61000-4-6

IEC61000-4-6 is the conducted immunity (CI) test. This test simulates exposure to radio frequency transmitters in the range of 15 kHz to 80 MHz. Like the RI test, the field strength of the CI transmitter can vary, ranging from 3 V/m to 10 V/m.

1.1.7 Protection Circuitry

The IEC61000-4 transients have two main components: a high-frequency component and a high-energy component. These two properties can be leveraged with a strategy of attenuation and diversion by the protection circuitry to deliver robust immunity.

Attenuation uses passive components, primarily resistors and capacitors, to attenuate high-frequency transients and to limit series current. Ferrite beads can also be used and are useful to maintain DC accuracy while still delivering the ability to limit current from high-frequency transients. This circuit utilizes capacitors placed at each of the voltage and current output terminals. A resistor is placed on the current output to limit current flowing into the IOUT terminal of the DAC8775 during exposure to high-voltage transients. The voltage output stage uses a similar strategy with two resistors in the voltage-output feedback loop in addition to a ferrite bead outside of the loop.

Diversion capitalizes on the high-voltage properties of the transient signals by using diodes to clamp the transient within supply voltages or to divert the energy to ground. Transient voltage suppressor (TVS) diodes are helpful to protect against the IEC transients because they break down very quickly and often feature high power ratings, which are critical to survive multiple transient strikes. Schottky diodes feature very-low forward voltage drop and are used to clamp the voltage on the input and output (I/O) lines to within the absolute maximum ratings of the DAC8775.

1.2 Key System Specifications

表 2. Key System Specifications

PARAMETER	GOAL	MEASURED	MEASURED DURING TRANSIENT TESTING
Voltage output: total unadjusted error	0.1 %FSR (max)	0.015 %FSR (max)	0.02 %FSR (max)
Current output: total unadjusted error	0.01 %FSR (max)	0.07 %FSR (max)	0.3 %FSR (max)
Peak-to-peak voltage output ripple	0.2 mV (typical)	0.184 mV (typical)	—
Peak-to-peak current output ripple	8 µA (typical)	6.72 µA (typical)	—
IEC61000-4 immunity	Pass	—	Pass, Class A and B (1)

(1) Detailed test results for voltage and current mode are given in each IEC61000-4 test result section.

1.3 Block Diagram

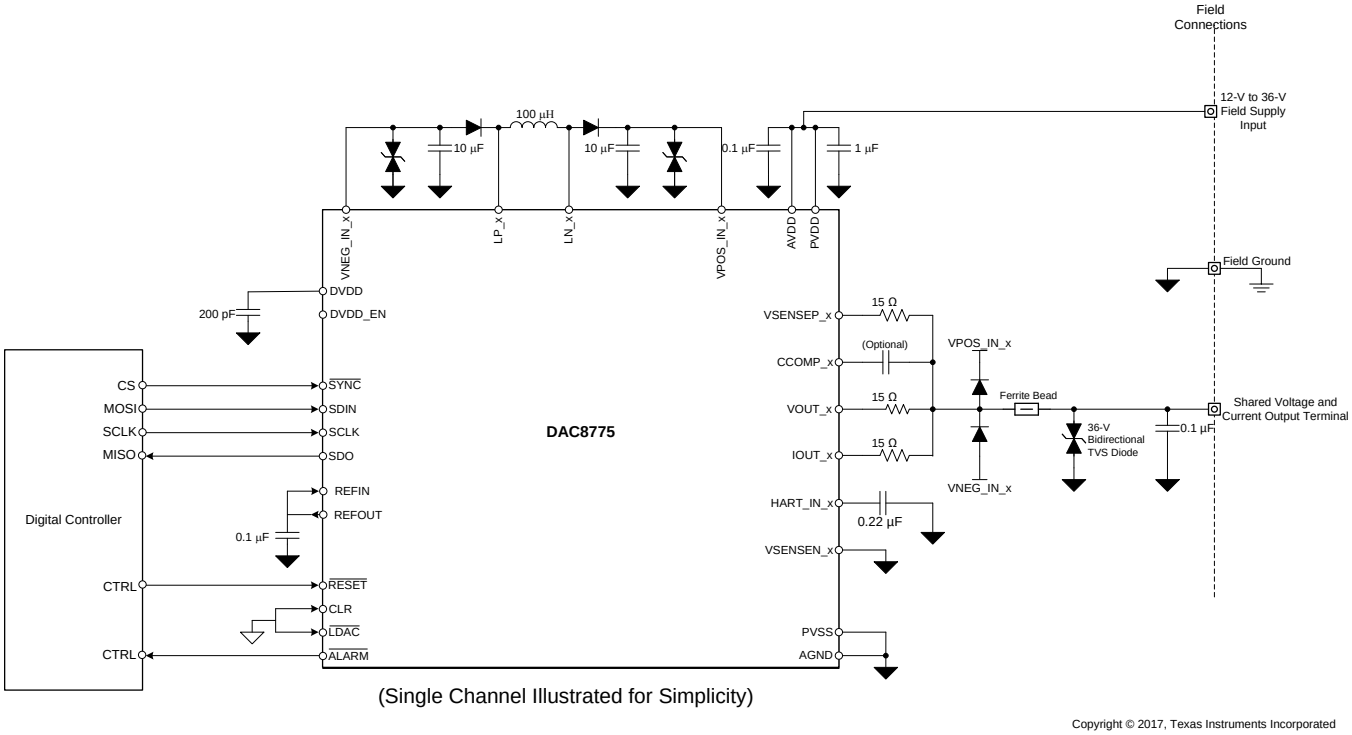

図 6. Reference Design Block Diagram

1.4 Design Considerations

The design requirements are as follows:

- Supply voltage: 12 V to 36 V
- Input: Four-wire serial peripheral interface (SPI)
- Voltage output: ±10 V
- Current output: 4 mA to 20 mA

The primary objective for this design is to provide immunity to the IEC-61000-4 suite of tests with minimum impact on the performance of the DAC8775 in an analog output module application. The specific design goals and performance are summarized in 表 2.

1.5 Highlighted Products

1.5.1 DAC

The DAC8775 device has been chosen for this design for its high level of integration, which is helpful to simplify the design of an electromagnetic compatibility (EMC) and electromagnetic interference (EMI) protection solution.

The DAC8775 includes the DAC, current and voltage amplifiers, regulated voltages, and all of the switches, transistors, and resistors required to create a configurable integrated solution for industrial voltage and current output drivers. The DAC8775 features a max 0.1% full-scale range (FSR) total-unadjusted-error (TUE) specification, which includes offset error, gain error, and integral non-linearity (INL) errors at 25°C. The 0.1% FSR TUE is valid for all of the voltage and current output stages and provides a baseline for the final system accuracy. The max differential non-linearity (DNL) specification of ±1 least significant bit (LSB) provides fully-monotonic operation for both V_{OUT} and I_{OUT}.

1.5.2 TVS Diode

A bidirectional TVS diode can be used to divert high-voltage transients to ground for systems that utilize symmetrical supply voltages, such as ±15 V. Two unidirectional TVS diodes must be used for non-symmetrical supply voltages. In both cases, diode selection is based on working voltage, breakdown voltage, and power rating.

The working voltage specification of a diode defines the largest reverse voltage at which the diode is meant to be continuously operated without it conducting. This working voltage is the voltage at the “knee” of the reverse breakdown curve where the diode begins to break down and exhibits some small leakage current. As the voltage increases above the working voltage, more current begins to flow through the diode. The breakdown voltage defines the reverse voltage at which the diode fully allows current to flow. One important thing to note is that if excessive current flows through a diode, the breakdown voltage rises.

The diode breakdown voltage should be low enough to protect all components connected to the output terminals and to provide headroom for the breakdown voltage to rise with reasonably large currents. The DAC8775 absolute maximum supply ratings are specified as 40 V to ground. To match the power-supply voltages, a bidirectional TVS diode with a working voltage of 36 V, a breakdown voltage of 40 V, and power rating of 400 W has been chosen.

An additional parameter to consider for TVS diode selection is leakage current. At the working voltage, when the diode is not operating in its breakdown region, some current flows through the diode and can affect system accuracy. The diode selected for this design features 1-µA maximum leakage current at the working voltage.

1.5.3 Schottky Diode

All Schottky diodes feature low forward voltage drop for reasonable currents, but the forward voltage drop may increase beyond being useful in the circuit when exposed to excessive current. The Schottky diode used in this design must maintain low enough forward voltage drop to keep the voltage at the input terminals within the absolute maximum ratings for all components connected to the output terminals. The diode used in this design features a forward voltage drop of 1.5 V when 1 A flows through the diode, which means the diodes clamp at 16.5 V for transients with 1 A of current.

Like the TVS diodes, Schottky diodes can contribute some leakage current on the voltage and current outputs based on the reverse leakage current specification. Reverse leakage current is usually specified at a specific reverse voltage. The diode used in this design has a reverse leakage current specification of 1 µA at a 70-V reverse voltage.

1.5.4 Passive Components

The capacitors placed on the output terminals of the voltage and current outputs are used in combination with the source impedance of the transient generator to attenuate and slow signals before they are clamped by the TVS diodes or Schottky diodes. The size of the capacitor plays an important role for delivering class A performance in the IEC61000-4 tests at the cost of system bandwidth.

For the current output, a resistor is placed between the TVS diodes and Schottky diodes to provide a pass element between the TVS clamp voltage and the Schottky, as well as to limit current flowing into the DAC8775 output terminals. This resistor should be sized appropriately to provide some series current limit without causing compliance voltage at the current output.

The voltage output uses a ferrite bead between the TVS diodes and Schottky diodes for the same purpose as the resistor on the current output. Because the component location is not included in the voltage output feedback loop, a ferrite bead was used instead of a resistor to maintain DC accuracy. The selected ferrite has a DC impedance of 40 mΩ and an impedance of 600 Ω at 100 MHz. Two additional resistors are included in the voltage output feedback loop to provide additional current limiting to the DAC8775 output terminals.

1.5.5 Inductor

A single inductor per channel of the DAC8775 is required for the internal buck-boost converter to generate the positive and negative rails. The recommended inductor value is 100 µH with a peak current of 500 mA or greater with 20% inductance tolerance at the peak current. Inductor values as small as 80 µH may be used; however, this limits the buck-boost converter efficiency, increases output ripple, and reduces the effective output voltage range.

2 Hardware, Software, Testing Requirements, and Test Results

2.1 Required Hardware and Software

The reference design was designed and fabricated and only requires an external supply and load resistors to perform the tests as outlined in 1.2. The exception is performing the voltage and current ripple test, which requires a first-order filter with fc = 50 kHz and an external operational amplifier (op amp) to gain the voltage ripple by 10x so it can be measured on an oscilloscope.

2.1.1 Testing and Results

The preceding 1.2 specifies the tests performed for the design.

2.1.1.1 Test Setup

2.1.1.1.1 Current Mode TUE

An external load of 250 Ω was applied to each current output individually and the supply was set to 24 V. The DAC8775 was set to 4-mA to 20-mA current output mode and then swept from zero code to 0xFFFF and the current was measured at each code. The result was normalized to the internal V_{REF} on the DAC8775 device.

2.1.1.1.2 Voltage Mode TUE

An external load of 10 kΩ was applied to each voltage output individually and the supply was set to 24 V. The DAC8775 was set to ±10-V voltage output mode and then swept from zero code to 0xFFFF and the voltage was measured at each code. The result was normalized to the internal V_{REF} on the DAC8775 device.

2.1.1.1.3 Peak-to-Peak Output Ripple

An external load of 250 Ω was applied to each current output individually and the supply was set to 24 V. The DAC8775 was set to 4-mA to 20-mA current output mode using the full-scale code (0xFFFF). A first-order RC filter with fc = 50 kHz was applied to the output before capturing the output ripple on an oscilloscope.

2.1.1.1.4 Peak-to-Peak Voltage Output Ripple

An external load of 10 kΩ was applied to each current output individually and the supply was set to 24 V. The DAC8775 was set to ±10-V voltage output mode using the full-scale code (0xFFFF). A first-order RC filter with fc = 50 kHz was applied to the output before going to a 10x op amp circuit and then on to an oscilloscope.

2.1.1.1.5 IEC61000-4 Testing

The IEC61000-4 certifications clearly define conditions for class B, C, and D performance but do not provide an explicit definition for class A. Class A conditions are defined by the manufacturer. For this EUT, class A performance is assigned for outputs that stay within 0.1% FSR of their intended value, corrected for DC errors intrinsic to the DAC, during exposure to each disturbance. The DAC8775 device is set to the 4- to 20-mA range for current outputs and the ±10-V range for voltage outputs.

The IEC61000-4 certifications do not specify what supporting equipment is used to monitor the output of the EUT. For this design, an Agilent 34401A 6½ digit digital multimeter has been selected to monitor the output with its resolution set to fast 5½ digit mode.

2.1.1.2 Test Results

2.1.1.2.1 Current Mode TUE

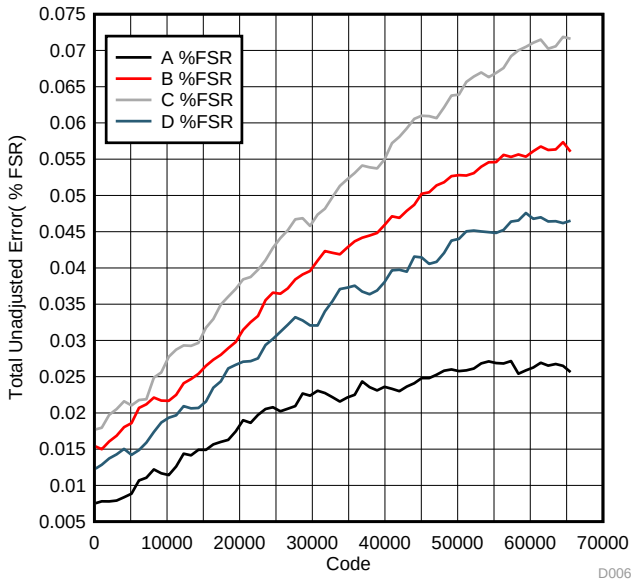

図 7. Measured Current Output Total Unadjusted Error (%FSR)

2.1.1.2.2 Voltage Mode TUE

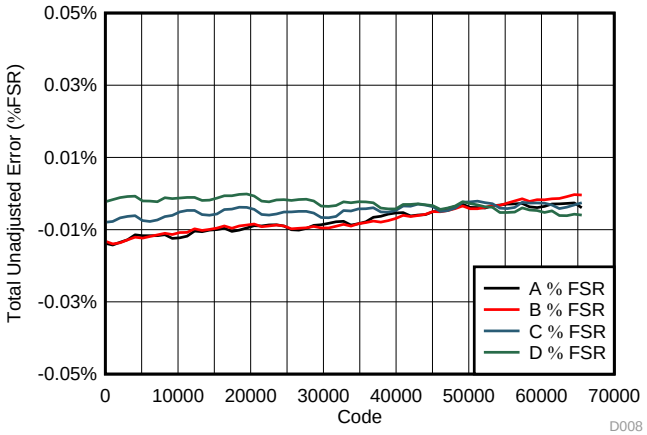

図 8. Measured Voltage Output Total Unadjusted Error (%FSR)

2.1.1.2.3 Peak-to-Peak Current Output Ripple into 250-Ω Load

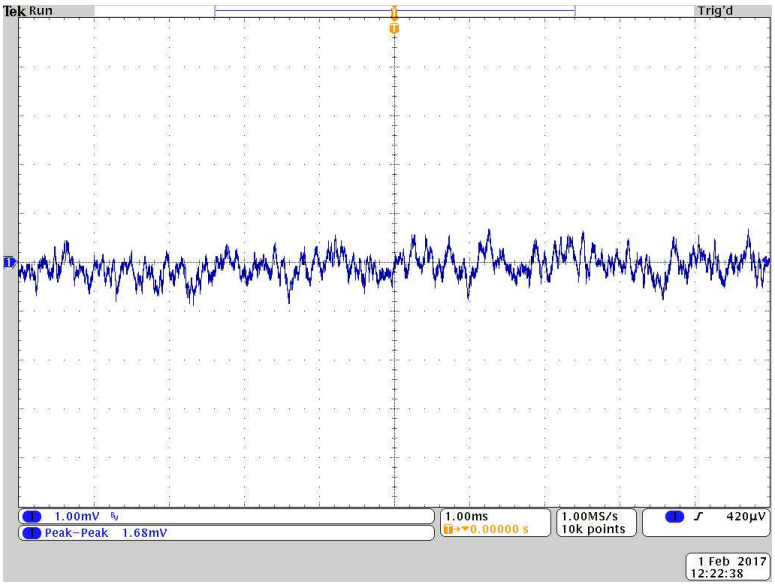

図 9. Measured Output Current Ripple

2.1.1.2.4 Peak-to-Peak Voltage Output Ripple (10x Multiplied)

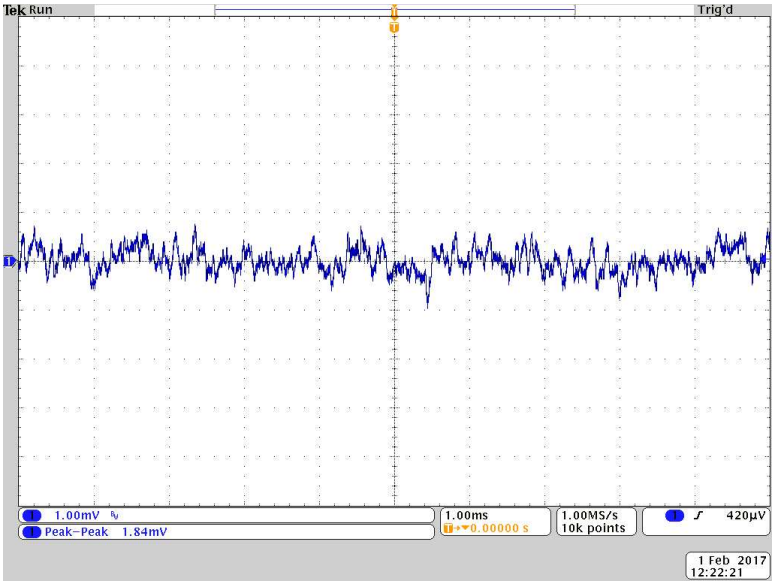

図 10. Measured Output Voltage Ripple

2.1.1.2.5 IEC61000-4-2: ESD (Electrostatic Discharge)

ESD tests were conducted at ±15-kV air discharge and ±8-kV coupling plane discharge. ESD showed almost no effect on the voltage and current outputs of the system. During and after the tests, the output remained within 0.1% FSR of the output value corrected for DC errors. 表 3 summarizes the results of the ESD tests. 図 11 through 図 14 show the output during each test.

表 3. IEC61000-4-2 Results

OUTPUT	ORIENTATION	RESULT	CLASS
Voltage (±10 V)	Coupling plane discharge	Pass	A
	Air discharge	Pass	A
Current (4 mA to 20 mA)	Coupling plane discharge	Pass	A
	Air discharge	Pass	A

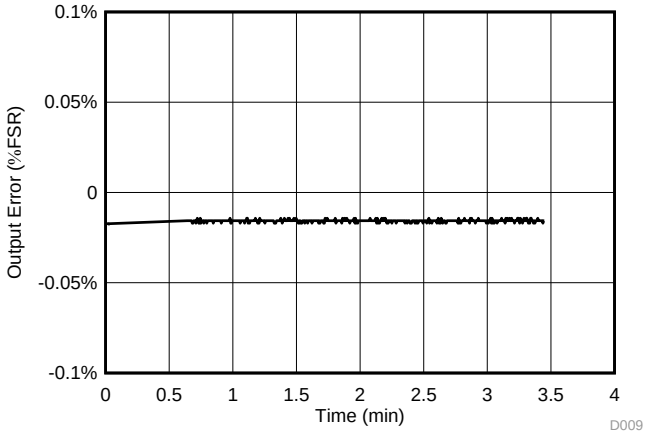

図 11. Voltage Output: ±15-kV ESD Air Discharge

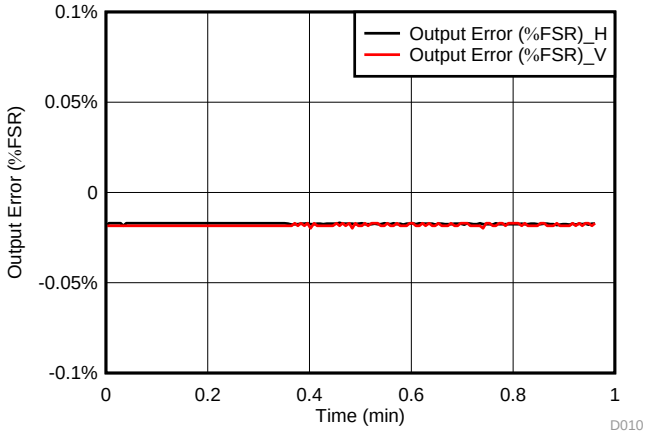

図 12. Voltage Output: ±8-kV ESD Vertical and Horizontal Coupling Plane Discharge

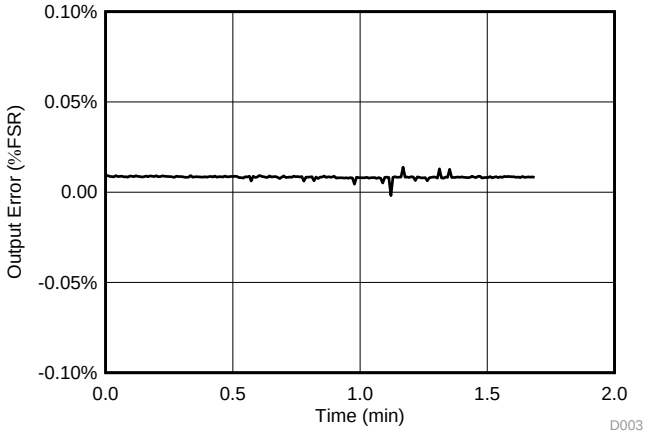

図 13. Current Output: ±15-kV ESD Air Discharge

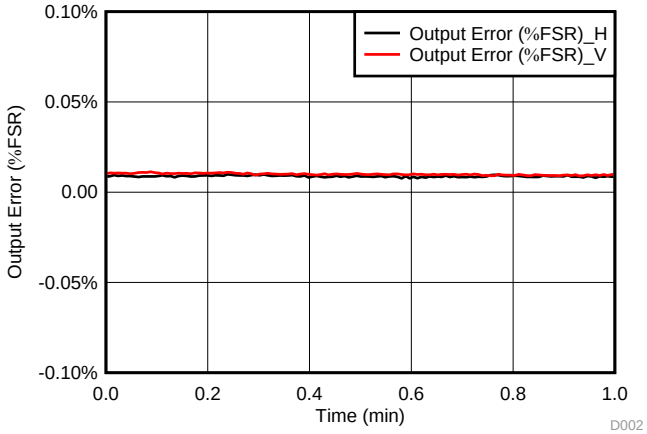

図 14. Current Output: ±8-kV ESD Vertical and Horizontal Coupling Plane Discharge

2.1.1.2.6 IEC61000-4-3: RI (Radiated Immunity)

Exposure to radiated emissions with a field strength of 20 V/m caused the current output to deviate and resulted in almost zero deviations on the voltage output. The current output remained within 0.3% FSR of the output value corrected for DC errors. After the test was completed, both the voltage and current outputs returned to normal operation without deviation. 表 4 summarizes the results of each test. 図 15 and 図 16 show the outputs during each test.

表 4. IEC61000-4-3 Results

OUTPUT	ORIENTATION	RESULT	CLASS
Voltage (±10 V)	Vertical	Pass	A
	Horizontal	Pass	A
Current (4 mA to 20 mA)	Vertical	Pass	B
	Horizontal	Pass	B

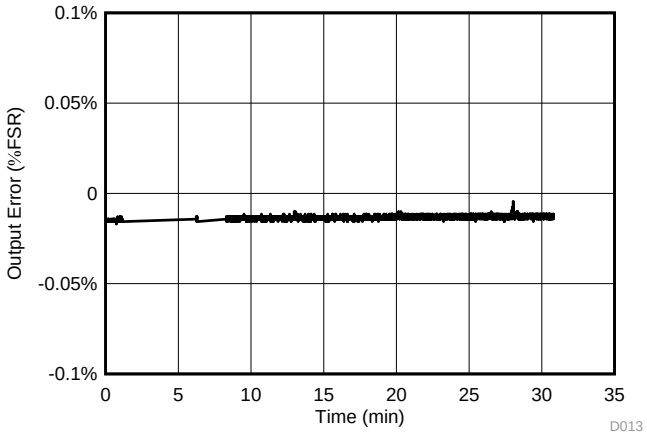

図 15. Voltage Output: 20-V/m Radiated Immunity

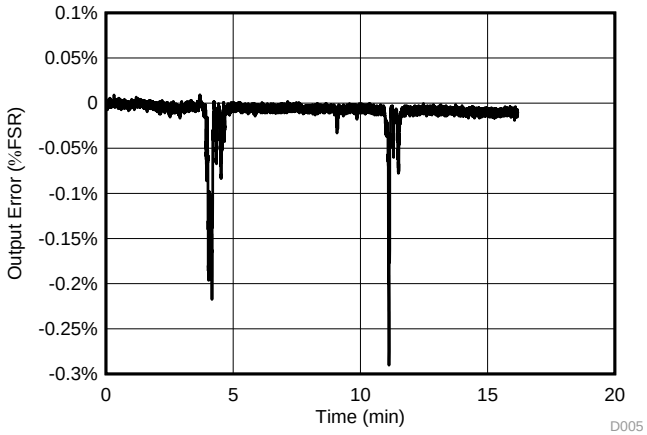

図 16. Current Output: 20-V/m Radiated Immunity

2.1.1.2.7 IEC61000-4-4: EFT (Electrically Fast Transient)

The EFT bursts had almost no effect on the voltage output. The current output was not disturbed by the negative polarity EFT bursts, but slight deviations were seen with positive polarity EFT bursts. After testing was complete, normal functionality was restored. 表 5 summarizes the results of each test. 図 17 and 図 18 show the voltage and current outputs during each test.

表 5. IEC61000-4-4 Results

OUTPUT	ORIENTATION	RESULT	CLASS
Voltage (±10 V)	Vertical	Pass	A
	Horizontal	Pass	A
Current (4 mA to 20 mA)	Vertical	Pass	A
	Horizontal	Pass	A

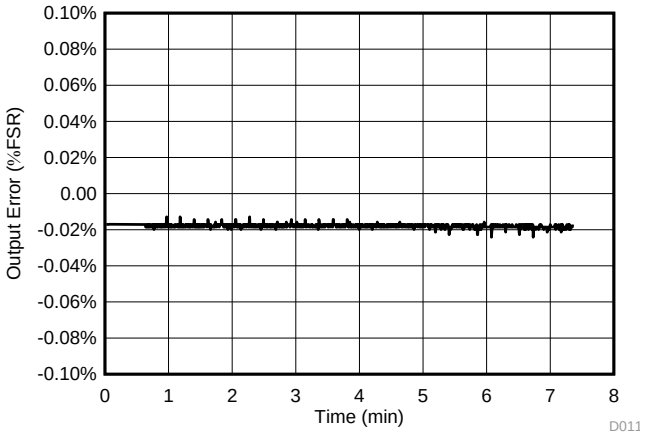

図 17. Voltage Output: ±4-kV Electrically Fast Transient

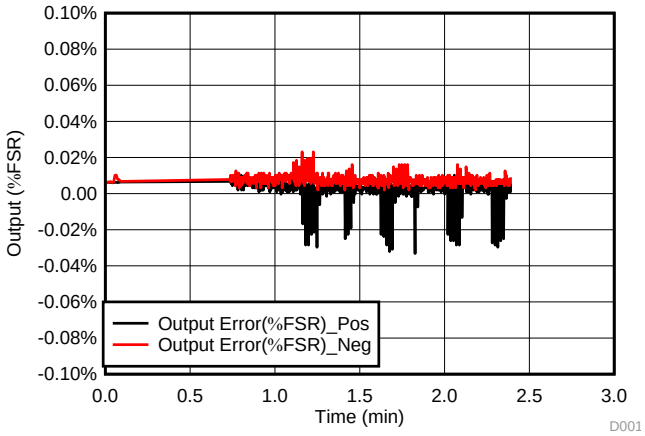

図 18. Current Output: ±4-kV Electrically Fast Transient

2.1.1.2.8 IEC61000-4-6: CI (Conducted Immunity)

The conducted immunity tests caused deviation to the current outputs. These deviations were outside of the 0.1% FSR range, resulting in a class B rating for IEC61000-4-6. The results are summarized in 表 6. 図 19 and 図 20 show the behavior of the outputs during exposure to the CI test.

表 6. IEC61000-4-6 Results

OUTPUT	RESULT	CLASS
Voltage (±10 V)	Pass	A
Current (4 mA to 20 mA)	Pass	B

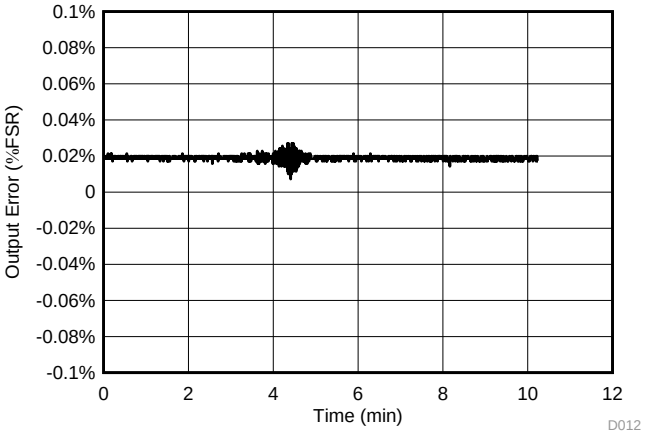

図 19. Voltage Output: 10-V/m Conducted Immunity

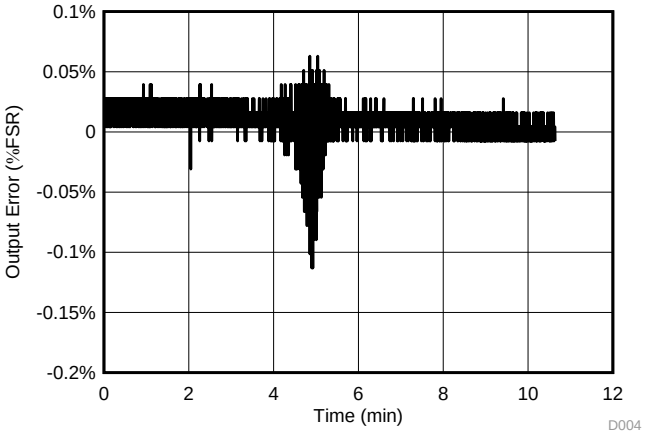

図 20. Current Output: 10-V/m Conducted Immunity

2.1.1.2.9 FCC Radiated Emission (Radiated Emission Sourced by TIPD216)

Additional radiated emission tests were performed to make sure the circuit does not generate noise in the 30-MHz to 1-GHz frequency range. An antenna was set in two positions: horizontal and vertical. The generated noise level was very low: 15 dBuV/m below the upper limit. 図 21 and 図 22 show the test result.

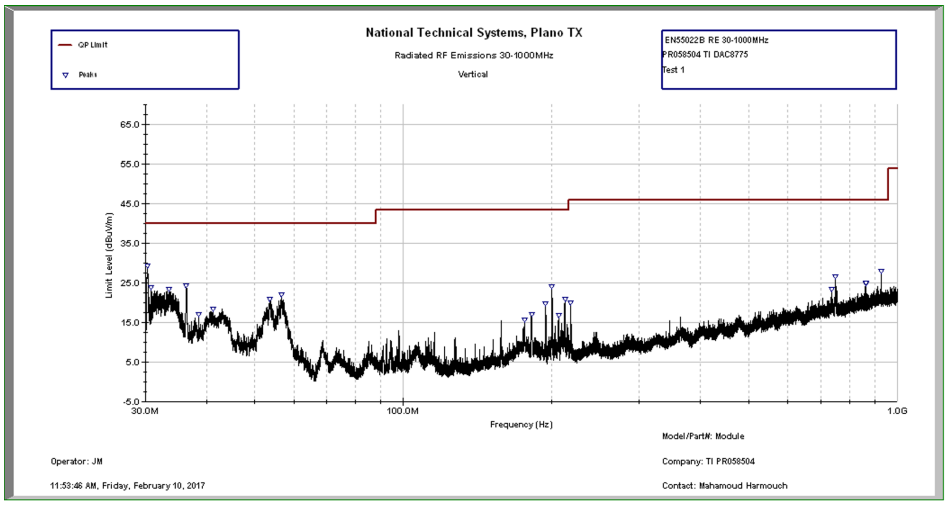

図 21. Vertical Antenna

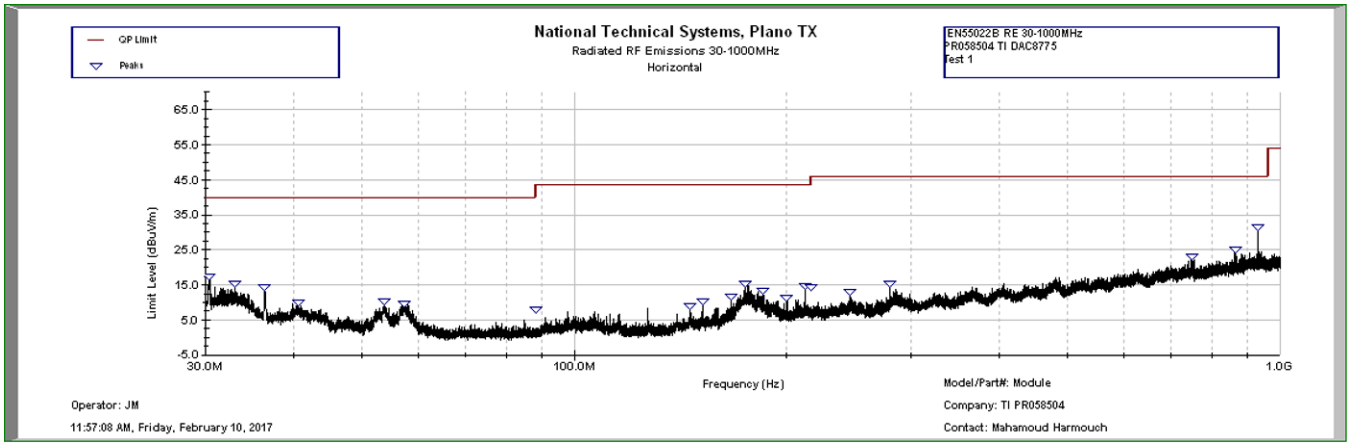

図 22. Horizontal Antenna

3 Design Files

3.1 Schematics

The following figures show the schematics. To download the schematics, see the design files at TIPD216.

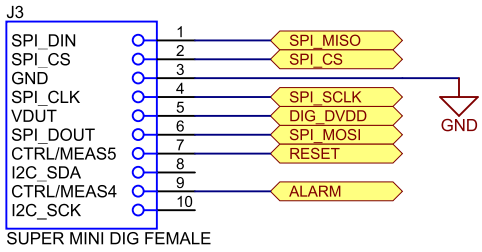

図 23. DAC8775 Digital Input Schematic

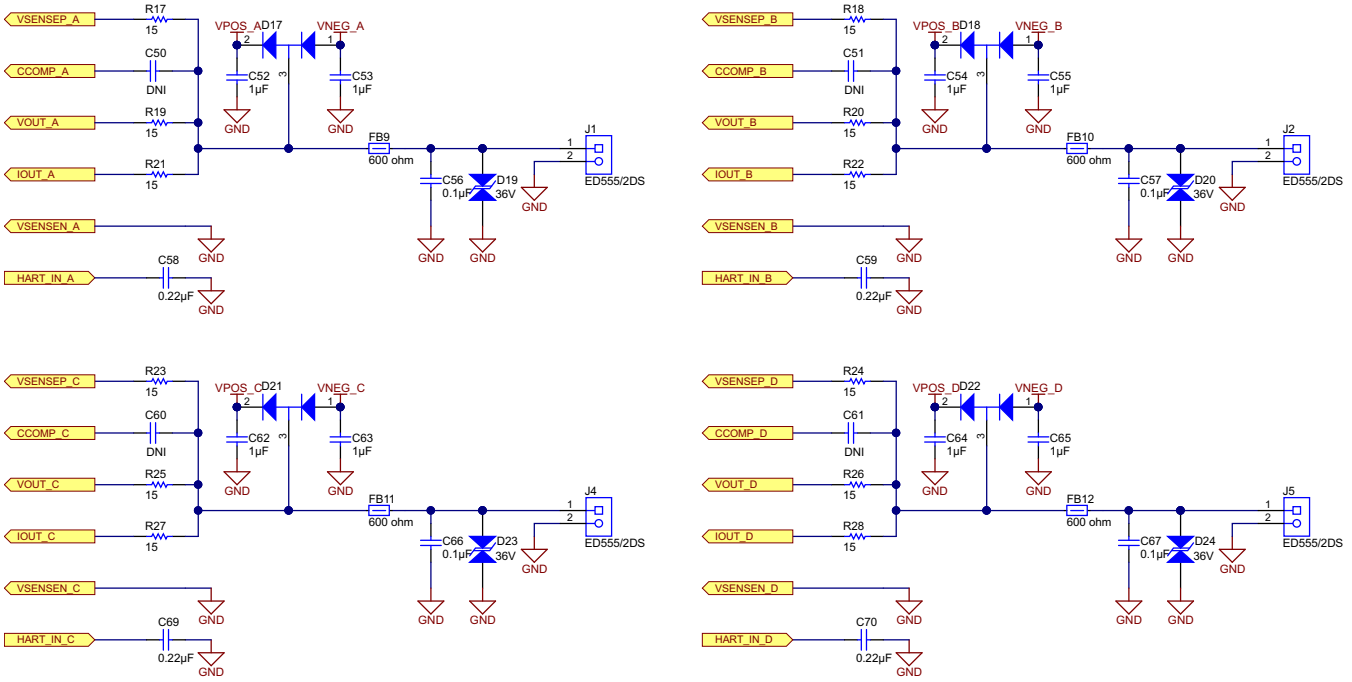

図 24. DAC8775 Outputs Schematic

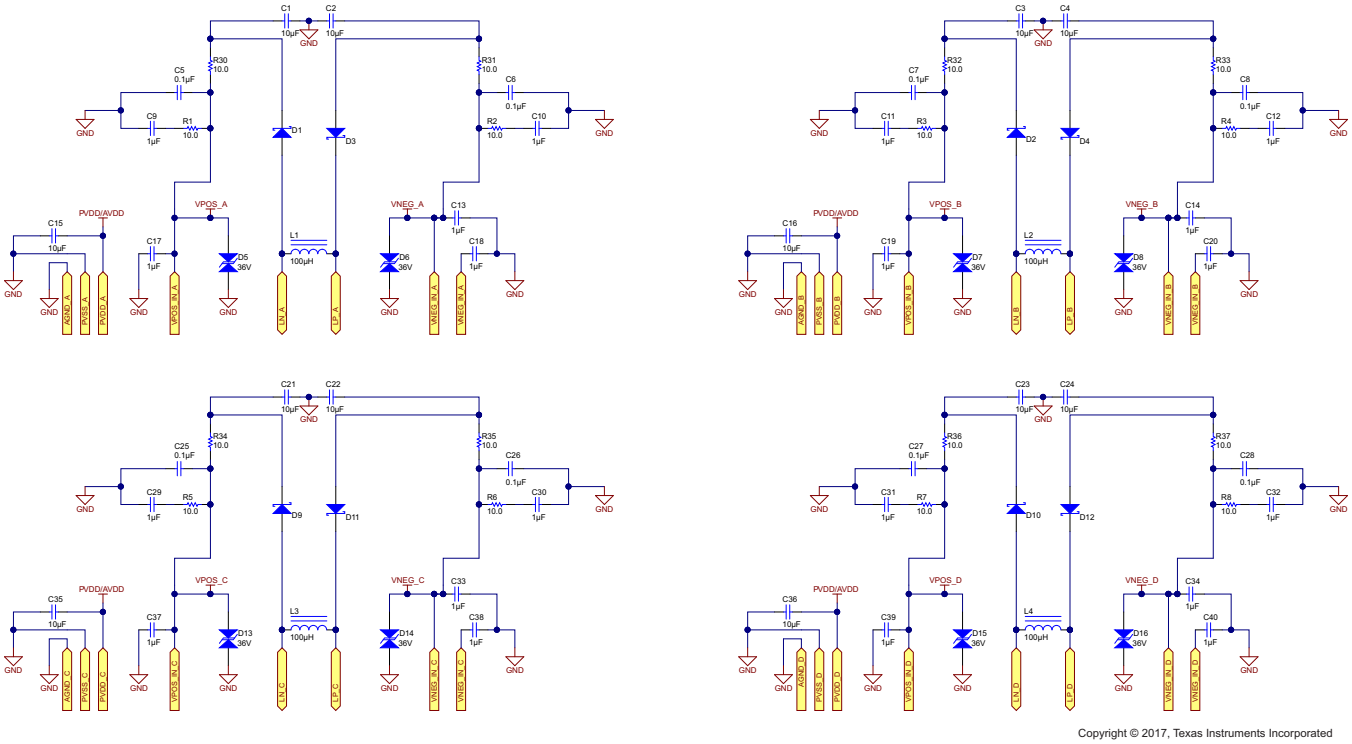

図 25. DAC8775 DC-DC Schematic

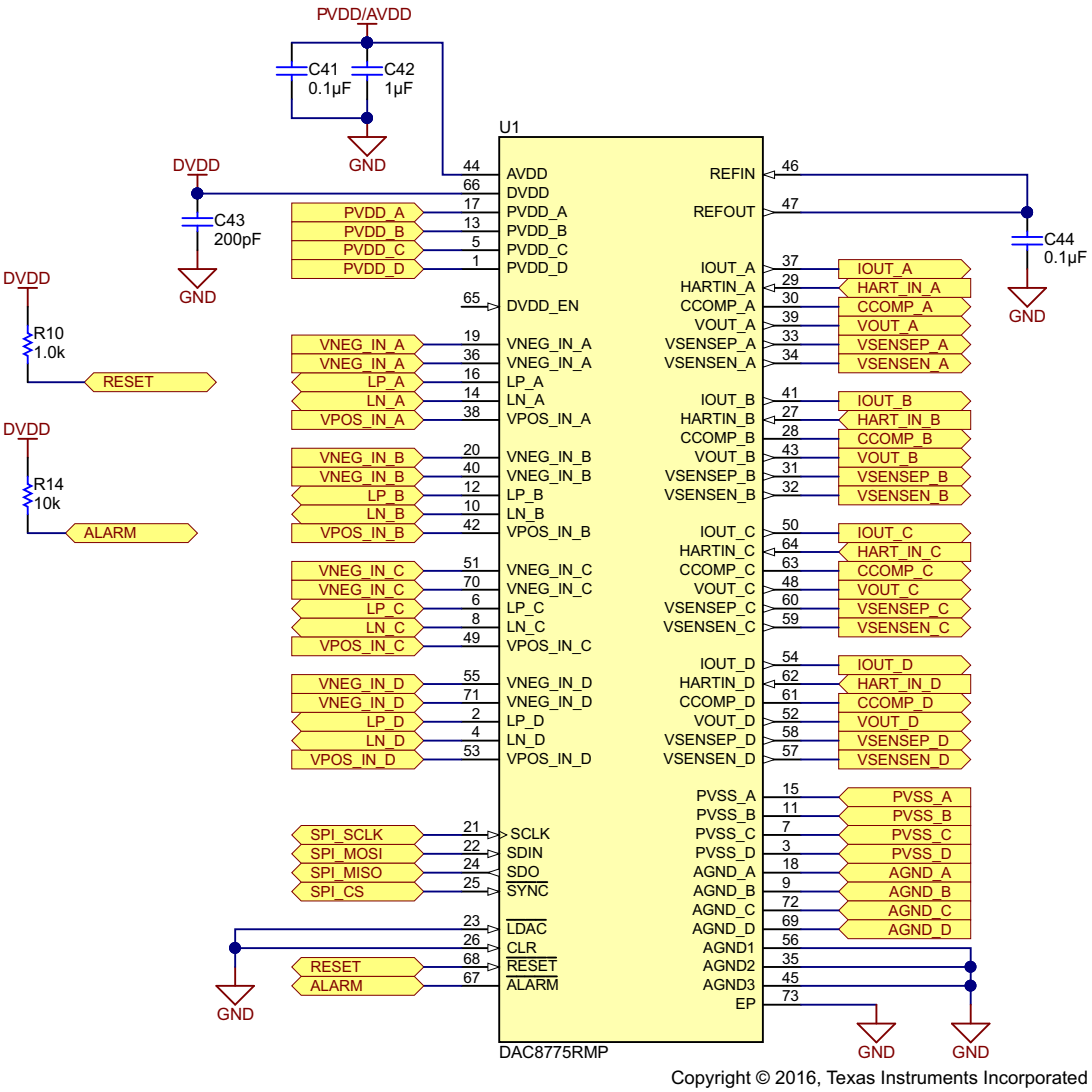

図 26. DAC8775 IC Schematic

3.2 Bill of Materials

表 7 shows the bill of materials (BOM). To download the BOM, see the design files at TIPD216.

表 7. BOM

ITEM #	DESIGNATOR	QUANTITY	VALUE	PART NUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
1	!PCB1	1		TIPD215	Any	Printed Circuit Board	
2	C1, C2, C3, C4, C15, C16, C21, C22, C23, C24, C35, C36, C68	13	10uF	UMK325AB7106KM-T	Taiyo Yuden	CAP, CERM, 10 µF, 50 V, +/- 10%, X7R, 1210	1210
3	C5, C6, C7, C8, C25, C26, C27, C28, C41, C44, C56, C57, C66, C67	14	0.1uF	GRM188R71H104KA93D	MuRata	CAP, CERM, 0.1uF, 50V, +/- 10%, X7R, 0603	0603
4	C9, C10, C11, C12, C13, C14, C17, C18, C19, C20, C29, C30, C31, C32, C33, C34, C37, C38, C39, C40, C42, C52, C53, C54, C55, C62, C63, C64, C65	29	1uF	UMK107AB7105KA-T	Taiyo Yuden	CAP, CERM, 1uF, 50V, +/- 10%, X7R, 0603	0603
5	C43	1	200pF	GRM1885C1H201JA01D	MuRata	CAP, CERM, 200pF, 50V, +/- 5%, C0G/NP0, 0603	0603
6	C50, C51, C60, C61	4					0603
7	C58, C59, C69, C70	4	0.22uF	C1608X7R1H224K080AB	TDK	CAP, CERM, 0.22 µF, 50 V, +/- 10%, X7R, 0603	0603
8	D1, D2, D3, D4, D9, D10, D11, D12	8	60V	MBRX160-TP	Micro Commercial Components	Diode, Schottky, 60V, 1A, SOD-123	SOD-123
9	D5, D6, D7, D8, D13, D14, D15, D16, D19, D20, D23, D24	12	36V	CDSOD323-T36SC	Bourns	Diode, TVS, Bi, 36V, 400W, SOD323, 2-Leads, Body 1.9x1.45mm, No Polarity Mark	SOD323, 2-Leads, Body 1.9x1.45mm, No Polarity Mark
10	D17, D18, D21, D22	4	75V	BAV99-7-F	Diodes Inc.	Diode, Switching, 75V, 0.3A, SOT-23	SOT-23
11	FB9, FB10, FB11, FB12	4	600 ohm	FBMH3225HM601NT	Taiyo Yuden	Ferrite Bead, 600 ohm @ 100 MHz, 3 A, 1210	1210
12	FID1, FID2, FID3	3		N/A	N/A	Fiducial mark. There is nothing to buy or mount.	Fiducial
13	J1, J2, J4, J5, J6	5		ED555/2DS	On-Shore Technology	Terminal Block, 3.5mm Pitch, 2x1, TH	7.0x8.2x6.5mm
14	J3	1		851-43-010-20-001000	Mill-Max	Receptacle, 50mil 10x1, R/A, TH	receptacle 10x1, 50mil
15	L1, L2, L3, L4	4	100uH	74408943101	Wurth Elektronik	Inductor, Shielded Drum Core, Ferrite, 100 µH, 0.52 A, 0.77 ohm, SMD	4.8x3.8x4.8mm

表 **7. BOM (continued)**

ITEM #	DESIGNATOR	QUANTITY	VALUE	PART NUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
16	R1, R2, R3, R4, R5, R6, R7, R8, R30, R31, R32, R33, R34, R35, R36, R37	16	10.0	CRCW060310R0FKEA	Vishay-Dale	RES, 10.0 ohm, 1%, 0.1W, 0603	0603
17	R10	1	1.0k	CRCW06031K00JNEA	Vishay-Dale	RES, 1.0 k, 5%, 0.1 W, 0603	0603
18	R14	1	10k	CRCW060310K0JNEA	Vishay-Dale	RES, 10k ohm, 5%, 0.1W, 0603	0603
19	R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28	12	15	CRCW060315R0JNEA	Vishay-Dale	RES, 15 ohm, 5%, 0.1W, 0603	0603
20	U1	1		DAC8775RMP	Texas Instruments	Quad-Channel, 16-Bit Programmable Current Output and Voltage Output Digital-to-Analog Converter with Adaptive Power Management, RMP0072A	RMP0072A

3.3 PCB Layout Recommendations

For optimal performance of this design, follow standard printed-circuit board (PCB) layout guidelines, including proper decoupling close to all integrated circuits and adequate power and ground connections with large copper pours. Additional considerations must be made for providing robust EMC and EMI immunity. All protection elements should be placed as close to the output connectors as possible to provide a controlled return path for transient currents that does not cross sensitive components. Wide, low-impedance, low-inductance traces should be used along the output signal path and protection elements to allow optimum current flow . When possible, use copper pours in place of traces. Stitching the pours provides an effective return path around the PCB and helps reduce the impact of radiated emissions.

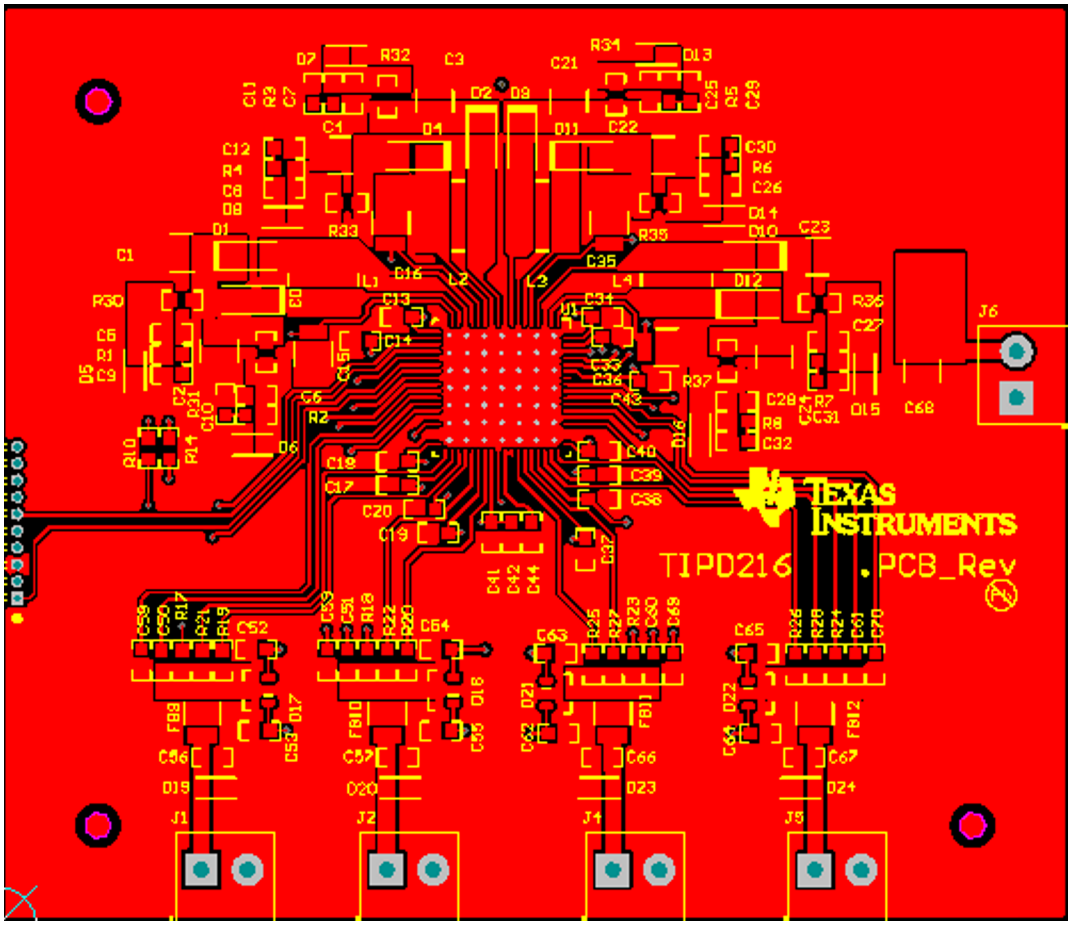

図 27. PCB Layout

3.3.1 Layout Prints

To download the layer plots, see the design files at TIPD216.

3.4 Altium Project

To download the Altium project files, see the design files at TIPD216.

3.5 Gerber Files

To download the Gerber files, see the design files at TIPD216.

3.6 Assembly Drawings

To download the assembly drawings, see the design files at TIPD216.

4 Software Files

To download the software files, see the design files at TIPD216.

5 Related Documentation

1. Texas Instruments, *DAC8775 Quad-Channel, 16-Bit Programmable Current Output and Voltage Output Digital-to-Analog Converter with Adaptive Power Management* , DAC8775 Datasheet (SLVSBY7)

5.1 商標

6 About the Author

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改訂履歴

2017年3月発行のものから更新 **Page**

- Figure 7 to correct the y-axis to show percentage of full-scale range 変更 11

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