

## TI Designs: TIDA-01589

# ノイズ・リダクションおよびエコー・キャンセル機能を持つ、高忠実度、ニアフィールド2ウェイ・オーディオのリファレンス・デザイン



### 概要

人間と機械との連携には、全二重のハンズフリー通信を行うための音響インターフェイスが必要です。ハンズフリー・モードでは、スピーカーからの遠端または近端のオーディオ信号の一部が、マイクロフォンにカップリングされます。さらに、ノイズの多い環境では、マイクロフォンが有用な近端オーディオ信号とともに、環境のノイズを拾う可能性があります。キャプチャされたマルチ・マイクロフォンのオーディオ信号が背景の音響ノイズやエコー信号の影響を受けることで、目的の信号の明瞭度が大きく損なわれ、以後のオーディオ処理システムの性能が制限されます。このリファレンス・デザインでは、デュアル・マイクロフォンによるオーディオ入力に対して、ステレオADCと低消費電力DSPによってノイズ・リダクション、音響エコー・キャンセル、その他のオーディオ品質向上アルゴリズムを適用する方法を紹介します。また、このデザインはTIのSmart Ampテクノロジーを使用して、マイクロ・スピーカーから高品質で高音圧レベル(SPL)のオーディオを出力します。

### リソース

<a href="#">TIDA-01589</a>	デザイン・フォルダ
<a href="#">TPS65023</a>	プロダクト・フォルダ
<a href="#">TLV320ADC3101</a>	プロダクト・フォルダ
<a href="#">TPS386000</a>	プロダクト・フォルダ
<a href="#">TPS3850</a>	プロダクト・フォルダ
<a href="#">TMS320C5517</a>	プロダクト・フォルダ
<a href="#">TAS2557</a>	プロダクト・フォルダ

### 特長

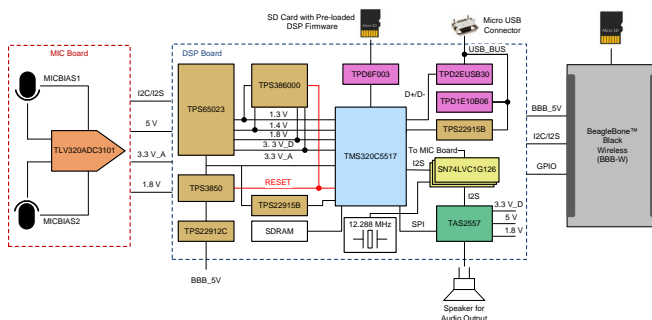
- 2ウェイ・オーディオのモジュール式プラットフォームで、アナログまたはデジタル・マイクロフォンによるオーディオのキャプチャと、TI Smart Ampテクノロジーによるマイクロ・スピーカーでの再生をサポート
- 92dBA SNR、0.003% THDの内蔵PGA、AGC、mini-DSPを搭載したTLV320ADC3101ステレオADCによる、デシメーション・フィルタ処理を実装
- 強力なTMS320C5517 DSPにより、適応型スペクトル・ノイズ・リダクション(ASNR)や、128msまでのエコー・テールを処理する音響エコー・キャンセル(AEC)など、各種のオーディオ処理アルゴリズムを実装
- 超低ノイズのオーディオDAC、Class-Dパワー・アンプ、内蔵のスピーカー検出および保護機能を搭載したSmart Amp TAS2557により、マイクロ・スピーカーで高いSPLを実現
- AM335xベースの BeagleBone™ Black Wirelessへの接続により、オプションとしてクラウド接続をサポート

### アプリケーション

- ビデオ・ドアベル
- サーモスタット
- IPネットワーク・カメラ
- Wi-Fi@カメラ
- スマート・ホーム・アラーム・システム



E2E™ エキスパートに質問





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## 1 System Description

Audio as *Human Machine Interface* (HMI) is an emerging trend in many building automation end-equipment such as IP network camera, Wi-Fi security camera, video doorbell, thermostat, smoke detector, intercom panel, smart speaker, audio and video conferencing systems, and others. The whole idea of having audio in *smart* home devices is to provide full duplex hands-free communication making the user experience more simple, comfortable, and reliable. The ability of the system to extract clear speech or audio from a noisy environment is important to applications that use voice activation and speech recognition. Particularly, hands-free systems implementing voice-activation and speech recognition also incorporate an audio playback path. This represents another challenge to voice recognition systems, as it adds other noise components. The realization of a hands-free communication system requires solutions to several fundamental challenges:

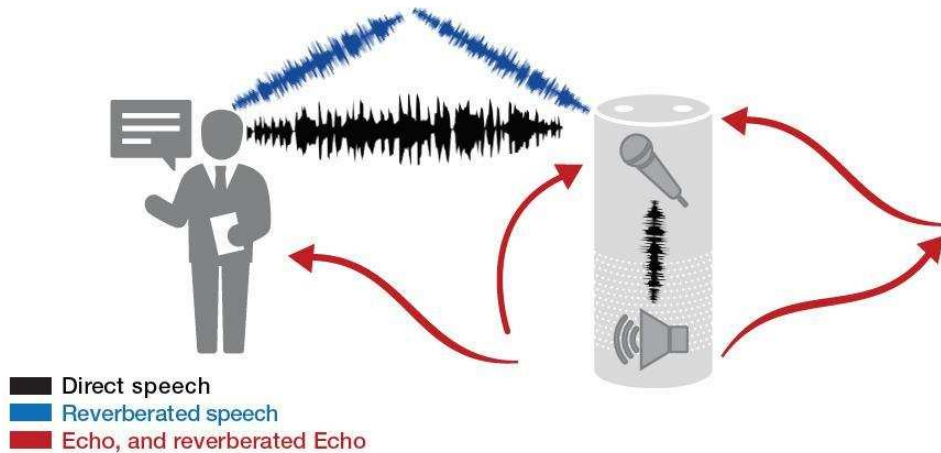
- Noise reduction: Handling background noise to extract clear audio
- Echo cancellation: Ensuring that there is no echo under any usage condition
- De-reverberation: Ensuring consistent performance even during changes to echo path
- Ensuring a full-duplex performance during double talk
- Limited on-chip resources to process audio data and running several algorithms to improve system performance
- Real-time processing of captured audio data along with additional features like voice activation and speech recognition
- Higher sound pressure level (SPL) using micro-speaker and speaker protection

There are various ways that audio artifacts can be introduced to the system degrading the quality of captured audio. Ambient noise in the environment picked up by the microphones can create problems that corrupt the audio signal being transmitted and heard on the other end. Signal processing techniques such as adaptive spectral noise reduction (ASNR) and automatic gain control (AGC) are used to improve overall system performance ensuring high fidelity communication. ASNR helps to reduce background and broadband noise with a minimal reduction in signal quality and automatic gain control (AGC) helps to boost lower level speech signals in hands-free environments. Spectral noise reduction uses the frequency domain to effectively remove ambient and unwanted noise components from an audio signal, making it easier to hear the desired signal. Using adaptive filtering techniques creates an estimate of the signal's noise component. This noise component, when subtracted from the composite signal, reveals the best possible representation of the actual speech signal.

Acoustic echo occurs when the audio being played back is picked up directly or indirectly by the microphones and fed back in to the system. It can be exacerbated when the audio playback volume is high or the speaker and microphones are in close proximity. While some of the echo can be mitigated by keeping distance between the microphone and speaker however, this might not be possible in small space constrained systems. A more robust answer is to use acoustic echo cancellation (AEC) algorithms. In brief, an AEC samples audio from the far side as it comes in and compares it to audio from captured by microphones. If any of the audio matches, the AEC removes it by creating adaptive filters to prevent effect

of echo in real time. A critical attribute of the acoustic echo cancellation is its ability to quickly detect the time variances and the reflected audio signals and adapt to a changing environment while minimizing any audio distortion. In real-life, this could be introduced by a participant who is moving while speaking or is in a dynamic environment that might have changing attributes like a door opening and closing.  1 shows the effect of how echo and reverberation complicate the capture of a clean voice signal at the microphone.

 1. Effect of Echo and Reverberation When Speaker and Microphone Elements are in Close Proximity



Protecting the speaker requires controlling the voice-coil temperature and keeping the cone/diaphragm excursion within safe limits. Conventional hardware-based speaker protection matches the continuous power output of the audio amplifier with the speaker output rating and sometimes incorporates high pass filtering to prevent over-excursion. Unfortunately, imposing a hard limit on speaker output suppresses audio peaks and also reduces clarity. A more sophisticated approach uses an in-depth understanding of speaker behavior to protect it from failure while simultaneously increasing loudness and preserving audio quality. PurePath™ Smart Amp technology replaces hardware-based speaker protection methods with predictive algorithms, speaker characterization tools and real-time signal monitoring to increase the peak output of the speaker without damage. IV Sense amplifiers or Smart Amps from Texas Instruments™ build upon the classic Class-D audio amplifier by adding the ability to monitor the temperature and excursion of the speaker in real time. This is controlled by an algorithm running in the DSP inside the device. This feedback allows the device to monitor the health of the speaker and optimize the sound quality to enable great audio.

TIDA-01589 features multi-microphone capable advanced audio processing algorithms from Adaptive Digital Technologies running on C5517 DSP such as beamforming, adaptive spectral noise reduction, acoustic echo cancellation, anti-howling, adaptive filtering, nonlinear processing, and double talk detection to produce a high-quality, full-duplex communication. This design also provides a scalable platform for implementing new features like voice activation, speech recognition and directional of arrival (DOA) of sound. TI has a suite of silicon and third party based software algorithms, from the analog front end to processed speech output that you can integrate into a complete yet efficient solution for a given application.

## 1.1 Key System Specifications

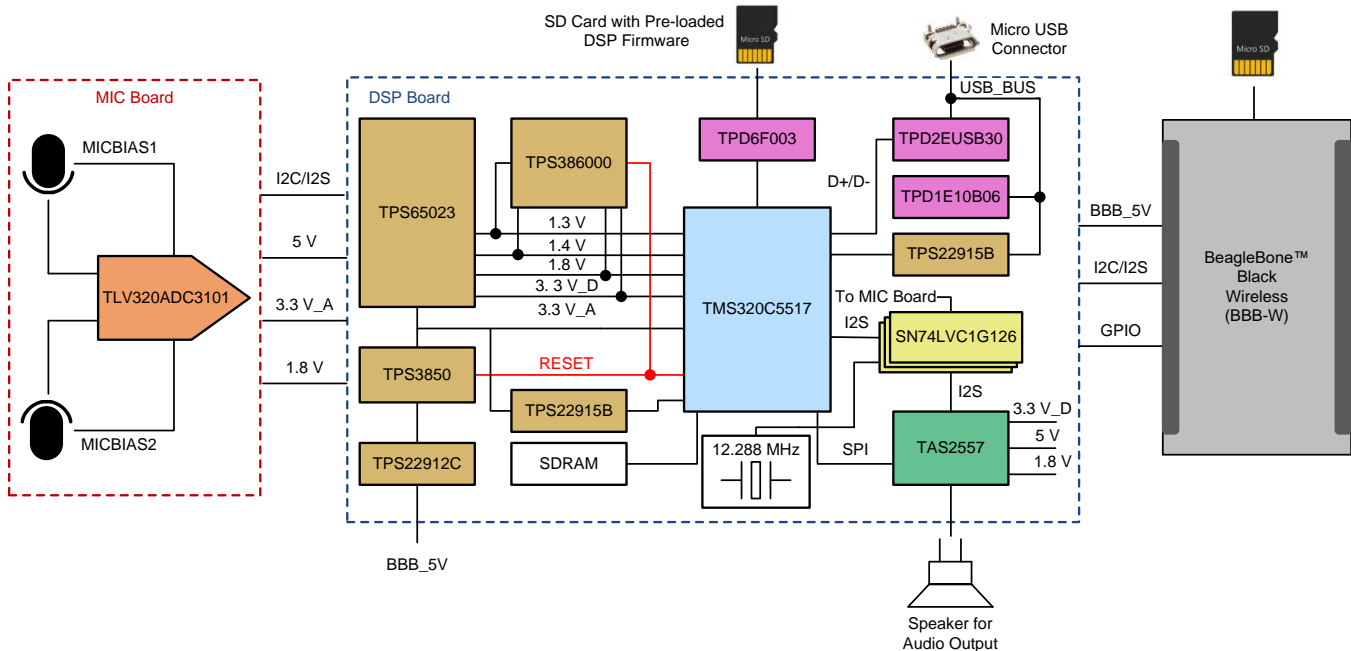
表 1. Key System Specifications

PARAMETERS	SPECIFICATIONS	Details
Microphone	Number of microphones : Two	<a href="#">2.3.2.1</a>
	Type of microphone : Analog	
	<a href="#">ICS-40618</a> : High dynamic range microphone with differential output and low power	
Boot image	DSP board boot image - Contact <a href="#">Adaptive Digital</a> for Boot image	C5517 Boot Image Explained in <a href="#">2.3.3</a>
	BeagleBone Black wireless boot image - Contact <a href="#">Adaptive Digital</a> for Boot image	<a href="#">2.3.5</a>
Speaker	SPS0916B-J-01 mounted on DSP board	<a href="#">2.3.4.1</a>
Code Composer Studio version	<a href="#">Code Composer Studio 8</a>	
<b>External Interfaces</b>		
Input voltage (VDD_5V)	Input DC voltage (4.5V to 5.5V, Typical 5V)	<a href="#">2.3.1</a>
JTAG	7 × 2 male header J7 on DSP board	JTAG Interface in <a href="#">2.3.3</a>
MIC board connector	Male header J1 on DSP board	
BeagleBone cape connectors	Male headers J4 and J5 to connect BeagleBone Black wireless	
Speaker connector	Terminal connector (J15) to connect speaker terminals	

## 2 System Overview

### 2.1 Block Diagram

図 2. TIDA-01589 Block Diagram



### 2.2 Highlighted Products

#### 2.2.1 TPS65023 - Power Management IC (PMIC) With 3 DC/DCs, 3 LDOs, I2C Interface and DVS

TPS65023x has 5 regulator channels, 3 DC/DCs and 2 LDOs. DCDC3 has dynamic voltage scaling feature (DVS) that allows for power reduction to CORE supplies during idle operation or overvoltage during heavy-duty operation. With DVS and 2 more DC/DCs plus 2 LDOs, the TPS65023x is ideal for CORE, Memory, IO, and peripheral power for the entire system.

For noise-sensitive circuits, the DC/DCs can be synchronized out of phase from one another, reducing the peak noise at the switching frequency. Each converter can be forced to operate in PWM mode to ensure constant switching frequency across the entire load range. However, for low load efficiency performance the DC/DCs automatically enter PSM mode which reduces the switching frequency when the load current is low, saving power at idle operation.

#### 2.2.2 TLV320ADC3101 - Low-Power Stereo ADC With Embedded miniDSP for Wireless Handsets and Portable Audio

TLV320ADC3101 is a flexible, low-power, stereo audio ADC device with extensive feature integration supporting sampling rates from 8 kHz to 96 kHz and has provision for both analog and PDM microphones input. Audio data is transferred between the host processor and the TLV320ADC3101 via the digital-audio serial-data interface, or audio bus.

### 2.2.3 **TPS386000 - Quad Supply Voltage Supervisors With Adjustable Delay and Watchdog Timer**

The TPS3860x0 multi-channel supervisory family of devices combines four complete SVS function sets into one IC, along with a watchdog timer, a window comparator, and negative voltage sensing.

TPS386000 is used to monitor voltage rails powering C5517 DSP.

### 2.2.4 **TPS3850 - Precision Voltage Supervisor With Window Watchdog Timer and Programmable Delay**

The TPS3850 is a high-accuracy voltage supervisor with an integrated watchdog timer. It is used to monitor voltage rail powering C5517 DSP.

### 2.2.5 **TMS320C5517- Fixed-Point Digital Signal Processor**

TMS320C5517 is a member of TI's C5000™ fixed-point Digital Signal Processor (DSP) product family and is designed for low active and standby power consumption. It is used to process audio data coming from stereo ADC and perform audio quality enhancement algorithms like Adaptive Spectral Noise Reduction (ASNR), Acoustic Echo Cancellation (AEC) and Beamforming (BF).

### 2.2.6 **TAS2557 - 5.7-W Class-D Mono Audio Amplifier with Class-H Boost and Speaker Sense**

The TAS2557 device is a state-of-the-art Class-D audio amplifier which is a full system on a chip (SoC). The device features a ultra low-noise audio DAC and Class-D power amplifier which incorporates speaker voltage and current sensing feedback. An on-chip, low-latency DSP supports Texas Instruments' Smart Amp speaker protection algorithms to maximize loudness while maintaining safe speaker conditions.

### 2.2.7 **TPS22915- 5.5-V, 2-A, 38-mΩ Load Switch With Quick Output Discharge**

TPS22915 is a 5.5-V, 2-A load switch in a 4-pin YFP package. To reduce voltage drop for low voltage and high current rails, the device implements an ultra-low resistance N-channel MOSFET which reduces the drop out voltage through the device. It is used for power sequencing in this design.

### 2.2.8 **TPS22912C- Ultra-small, Low On Resistance Load Switch With Controlled Turn-on**

TPS22912C is single channel, 2-A load switches in ultra-small, space saving 4-pin WCSP package. These devices implement a low resistance P-channel MOSFET with a controlled rise time for applications that need to limit the inrush current and has Full time reverse current protection. It is used to power BeagleBone from DSP board.

### 2.2.9 **SN74LVC1G126- Single Bus Buffer Gate With 3-State Outputs**

The SN74LVC1G126 device contains a dual buffer gate with output enable control and performs the Boolean function  $Y = A$

### 2.2.10 **TPD6F003- 6-Channel EMI Filter for Display Interface**

The TPDxF003 family is a series of highly integrated devices designed to provide EMI filtering in all systems subjected to electromagnetic interference. These filters also provide a Transient Voltage Suppressor (TVS) diode circuit for ESD protection which prevents damage to the application when subjected to ESD stress far exceeding IEC 61000-4-2 (Level 4).

### 2.2.11 TPD2EUSB30- 2-Channel ESD Solution for SuperSpeed USB 3.0 Interface

The TPD2EUSB30, TPD2EUSB30A, and TPD4EUSB30 are 2 and 4 channel Transient Voltage Suppressor (TVS) based Electrostatic Discharge (ESD) protection diode arrays. The TPDxEUSB30/A devices are rated to dissipate ESD strikes at the maximum contact level specified in the IEC 61000-4-2 international standard (Contact). These devices also offer 5 A (8/20  $\mu$ s) peak pulse current ratings per IEC 61000-4-5 (surge) specification.

### 2.2.12 TPD1E10B06- Single-Channel ESD in 0402 Package With 10-pF Capacitance and 6-V Breakdown

The TPD1E10B06 is a single-channel ESD TVS diode in a small 0402 package. This TVS protection product offers  $\pm$ 30-kV IEC air-gap,  $\pm$ 30-kV contact ESD protection, and has an ESD clamp circuit with a back-to-back TVS diode for bipolar or bidirectional signal support. The 12-pF line capacitance of this ESD protection diode is suitable for a wide range of applications supporting data rates up to 400 Mbps.

## 2.3 System Design Theory

This section explains the design theory for the key devices used in the design. The TIDA-01589 demonstration setup highlights modular architecture with three boards:

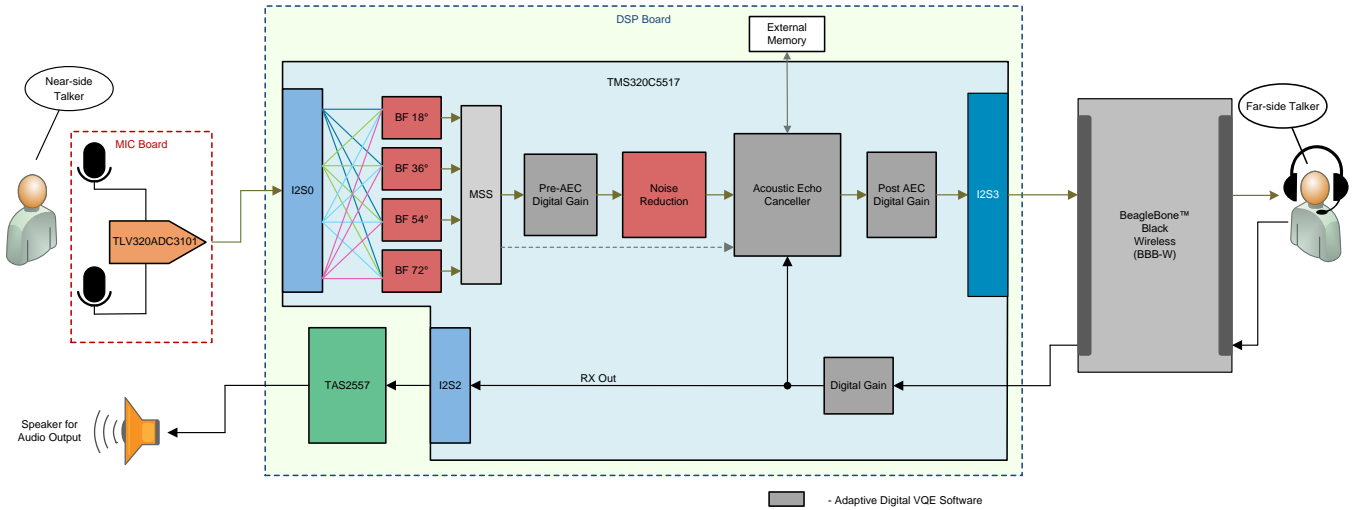
- DSP board with Power management, TMS320C5517 DSP, TAS2557 Smart Amp, and micro-speaker
- MIC board with two microphones and TLV320ADC3101 stereo ADC
- BeagleBone black wireless (BBB-W)

TIDA-01589 features the *High-Definition Acoustic Echo Canceller* (HD AEC™) from [Adaptive Digital Technologies](#) which is multi-microphone capable and includes beamforming, noise reduction, anti-howling, adaptive filtering, nonlinear processing, and double talk detection to produce a high-quality, full-duplex real-time communication between two participants.

Figure 3 shows a diagram with the signal flow for this application. The “near side” participant’s voice is input through the 2-mic array on MIC board and sampled at 16-kHz (wideband) rate by the TLV320ADC3101 low-power stereo ADC. Digital PCM audio samples are passed from the audio ADC to the TMS320C5517 DSP over I2S where beamforming (BF) is performed and the HD AEC™ is running. Processed (clean) audio samples from DSP are passed as PCM data over I2S to the BeagleBone Black Wireless (BBB-W). BBB-W is used to tie in the “far side” participant and provides audio playback over USB to a headset attached to it. A microphone in the headset of the far-side participant will take voice input and pass it via BBB-W to the DSP over I2S interface.

The DSP application provides a clean audio signal to TAS2557 over I2S which drives micro-speaker attached to the DSP board. TAS2557 features an ultra-low noise digital-to-analog converter (DAC) and Class-D power amplifier with speaker voltage and current sensing feedback. An on-chip DSP provides speaker protection algorithms, tuned to the micro-speaker for maximizing audio output while maintaining safe speaker operation.

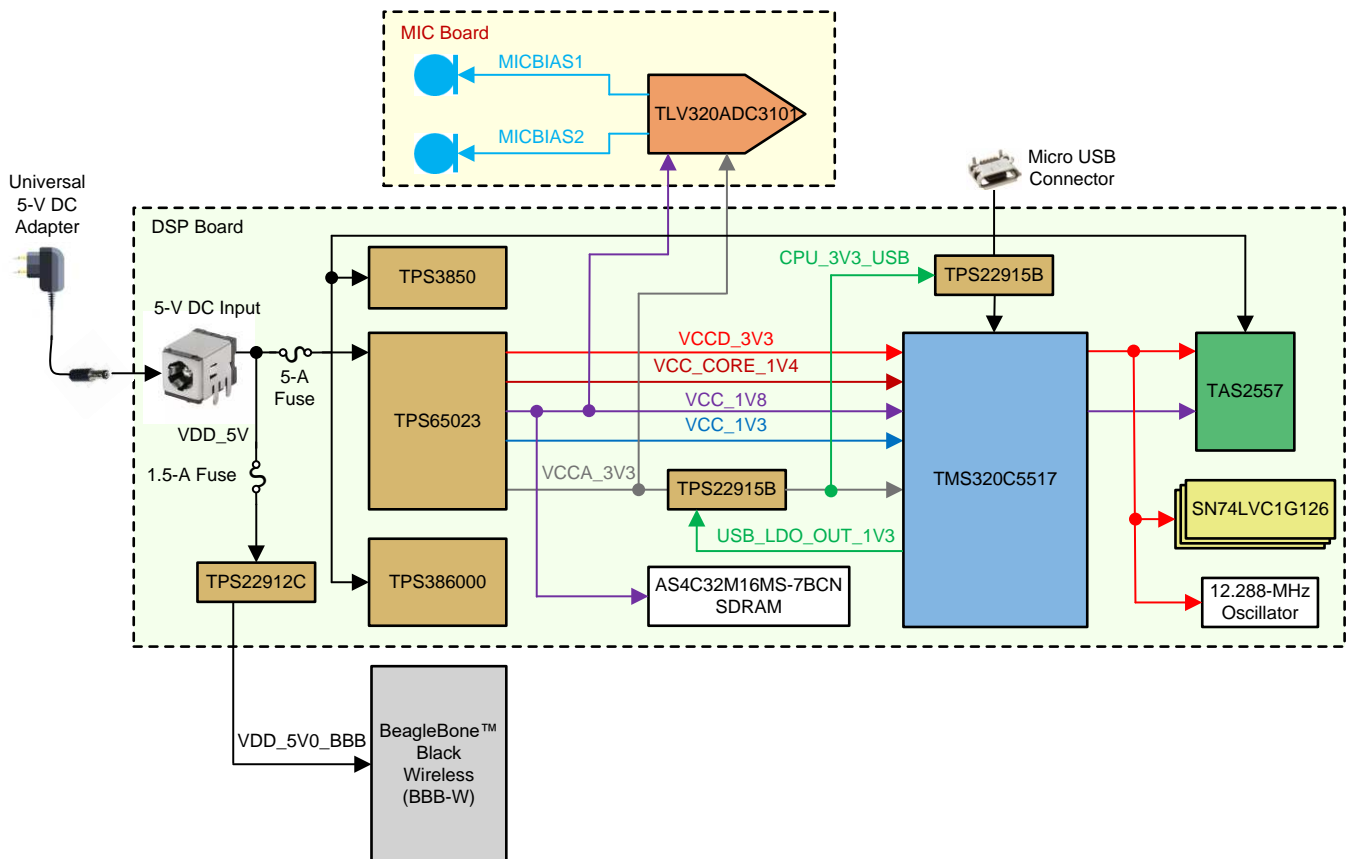
図 3. HD AEC™ Signal Flow on TIDA-01589 Hardware



### 2.3.1 Power Management

The input power to TIDA-01589 is provided by connecting a DC adapter of 5 V, with 6.5-A current rating through the DC Jack (J10) available on the DSP board. All the required power rails are generated from the TPS65023 PMIC which has 3 DC/DCs and 2 LDOs integrated. 図 4 shows power tree for TIDA-01589:

図 4. TIDA-01589 Power Tree





注: The BeagleBone Black Wireless (BBB-W) gets power from the TIDA-01589 DSP board so there is no need to connect a DC adapter to BBB-W. The [TPS22912C](#) load switch with full time reverse current blocking powers the BBB-W with 5-V DC input from the DSP board.

## 2.3.2 Audio Input

### 2.3.2.1 Microphone Selection

The choice of analog or digital microphone depends entirely on system space constraints, complexity of design, cost and sources of Noise and Interference in the system. The key parameters for selecting an analog microphone are as follows:

- Sensitivity
- Directionality
- Signal-to-Noise Ratio (SNR)
- Equivalent Input Noise (EIN)
- Dynamic range
- Frequency Response
- Total Harmonic Distortion (THD)
- Power Supply Rejection (PSR) AND Power Supply Rejection Ratio (PSRR)
- Acoustic Overload Point (AOP)

For more details on the previously-listed parameters, see the [MICROPHONE SPECIFICATIONS EXPLAINED](#) application note. In this design two [ICS-40618](#) analog microphones are selected based on the previously-listed parameters. The [ICS-40618](#) device includes a MEMS microphone element, an impedance converter, and a differential output amplifier. They are bottom-ported microphones with small audio ports in the PCB to allow the acoustic signal to pass.

The ICS-40618 needs supply voltage ranging from 1.52 V to 3.63 V supplied by [TLV320ADC3101](#) which includes two programmable microphone bias outputs (MICBIAS1, MICBIAS2), each capable of providing output voltages of 2 V or 2.5 V with 4-mA output-current drive capability. In addition, the MICBIAS outputs may be programmed to be switched to AVDD(3.3 V) directly through an on-chip switch which is enabled or disabled over I2C interface.


表 2 provides key Specifications for selected Microphone in High Performance mode:

**表 2. Microphone Parameters in High Performance Mode**

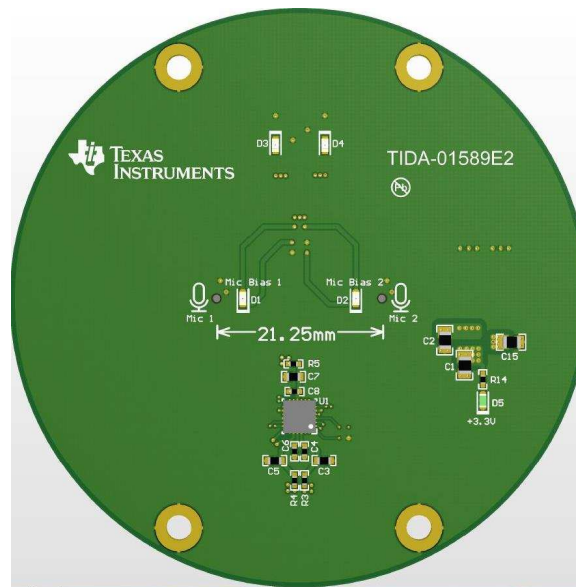
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>PERFORMANCE</b>					
Directionality		Omni			
Output polarity		Non-Inverted			
Sensitivity	1 kHz, 94 dB SPL, differential	-39	-38	-37	dBV
<b>HIGH-PERFORMANCE MODE</b>					
Signal-to-Noise Ratio (SNR)	20-kHz bandwidth, A-weighted		67		dB
Equivalent Input Noise (EIN)	20-kHz bandwidth, A-weighted		27		dB
Dynamic range	Derived from EIN and acoustic overload point		105		dB

**表 2. Microphone Parameters in High Performance Mode (continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Total Harmonic Distortion (THD)	105 dB SPL		0.2		%
Power Supply Rejection Ratio (PSRR)	1-kHz, 100-mV p-p sine wave superimposed on VDD = 2.75 V		-85		dB
Power Supply Rejection (PSR)	217-Hz, 100-mVp-p square wave superimposed on VDD = 2.75 V		-112		dBV
Acoustic overload point	10% THD		132		dB SPL
<b>OUTPUT CHARACTERISTICS</b>					
Differential output impedance	High-performance mode		355		ohm
Output common-mode voltage	OUTPUT+ and OUTPUT-, high-performance mode		1		V
Output differential offset	Between OUTPUT+ and OUTPUT-, high-performance mode		10		mV
Startup time	Output to within $\pm 0.5$ dB of stable sensitivity		15	20	ms
Maximum output voltage	132 dB SPL input		1.0		$V_{RMS}$
Noise Floor	20 Hz to 20 kHz, A-weighted, RMS, high-performance mode		-105		dBV

Two analog microphones are mounted at a distance of 21.25 mm in a linear geometry on the MIC board as  5 shows.

**図 5. MIC Board**



**2.3.2.2 Stereo ADC - TLV320ADC3101**

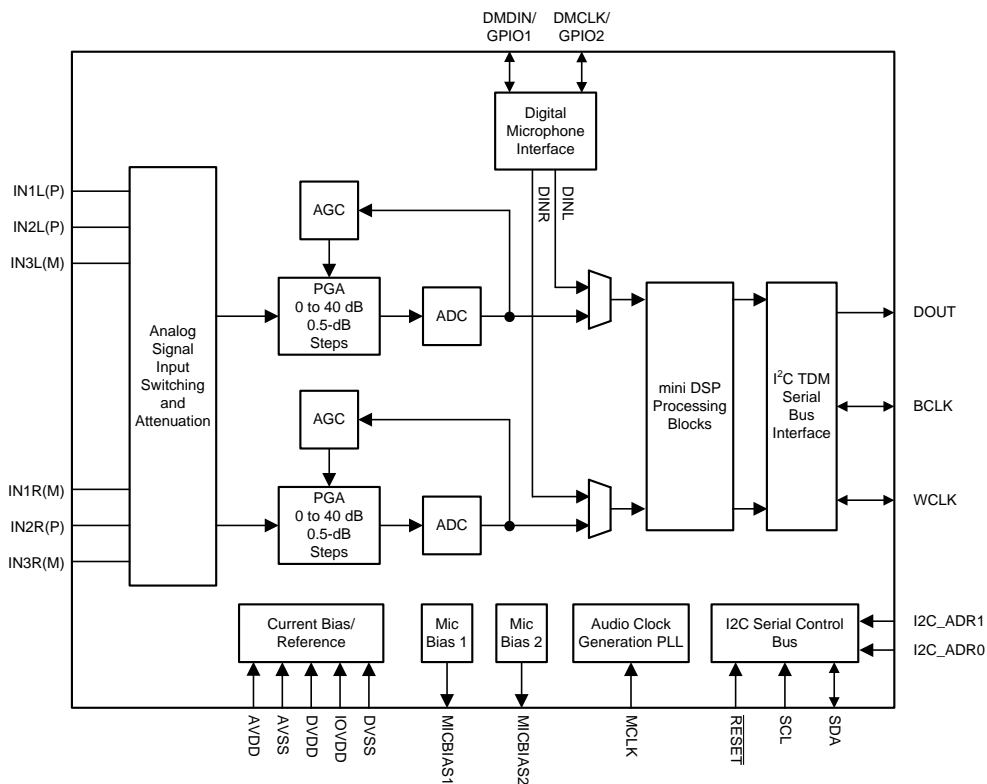
The TLV320ADC3101 device samples the captured audio signal from microphones and streams the digital values to TMS320C5517 DSP over I2S interface. The MIC board gets power and ground from the DSP board. The TLV320ADC3101 device consists of the following blocks:

- Stereo audio multi-bit delta-sigma ADC (8 kHz–96 kHz)
- Programmable digital audio effects processing (3-D, bass, treble, mid-range, EQ, de-emphasis)
- Register-configurable combinations of up to six single-ended or three differential audio inputs

- Fully programmable PLL with extensive ADC clock-source and divider options for maximum end-system design flexibility

☒ 6 shows the TLV320ADC3101 functional block diagram:

☒ 6. TLV320ADC3101 Block Diagram




In this design, TLV320ADC3101 initializes with following configuration settings after reset state:

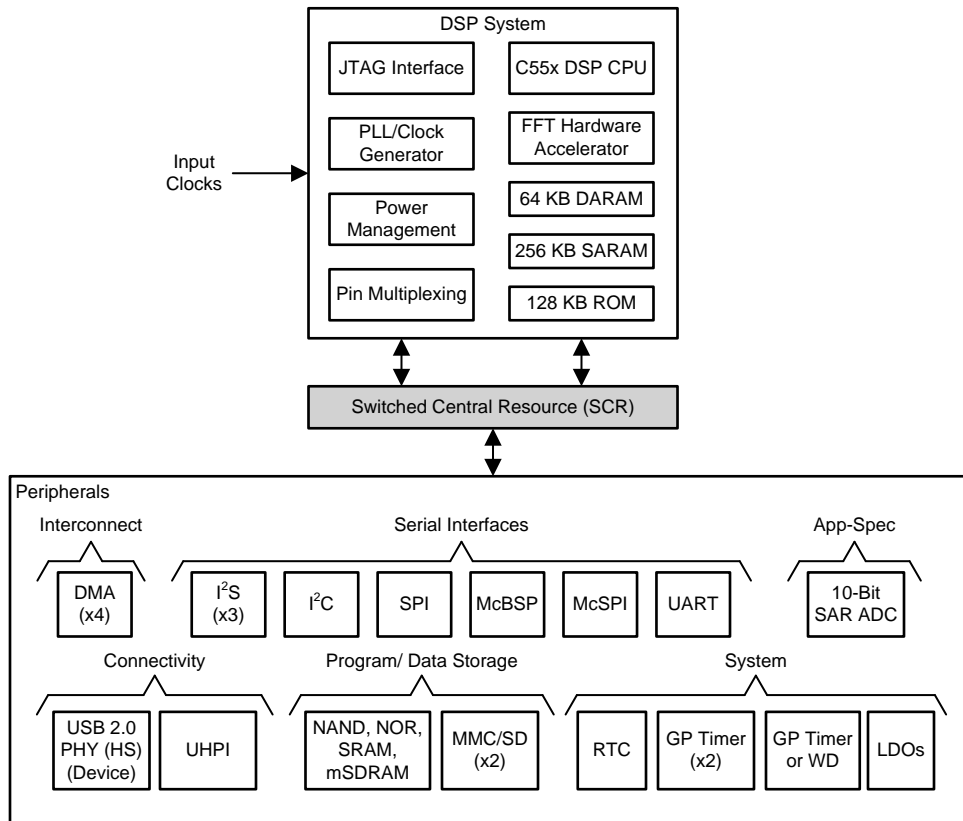
- Control Interface: I2C Interface with C5517 DSP
  - Configured as I2C slave and TMS320C5517 DSP as Master
  - I2C address for TLV320ADC3101: 0x18h
  - I2C interface supports both standard and fast communication modes
- Source reference clock: 12.288 MHz
  - Internally generated using integrated PLL
  - This reference clock is used to generate Internal ADC Clocks.
- Internal PLL Powered up
- ADC sampling frequency: 16 kHz
- Audio Interface: I2S interface with TMS320C5517 DSP
  - Configured as I2S slave and TAS2557 Smart Amp as Master as default setting
  - BCLK: 1.024 MHz
  - WCLK: 16 kHz
  - I2S word length: 24 bits
- MICBIAS1 and MICBIAS2 Outputs: 2.5 V

- High Performance mode for ICS-40618
- Selected Processing Block: PRB\_R1

### 2.3.3 Audio Processing - TMS320C5517

The C5517 DSP-based processor supports the real-time processing necessary along with the scalability desirable for voice triggering and related products.  7 shows the functional block diagram of the device.

 7. TMS320C5517 Block diagram




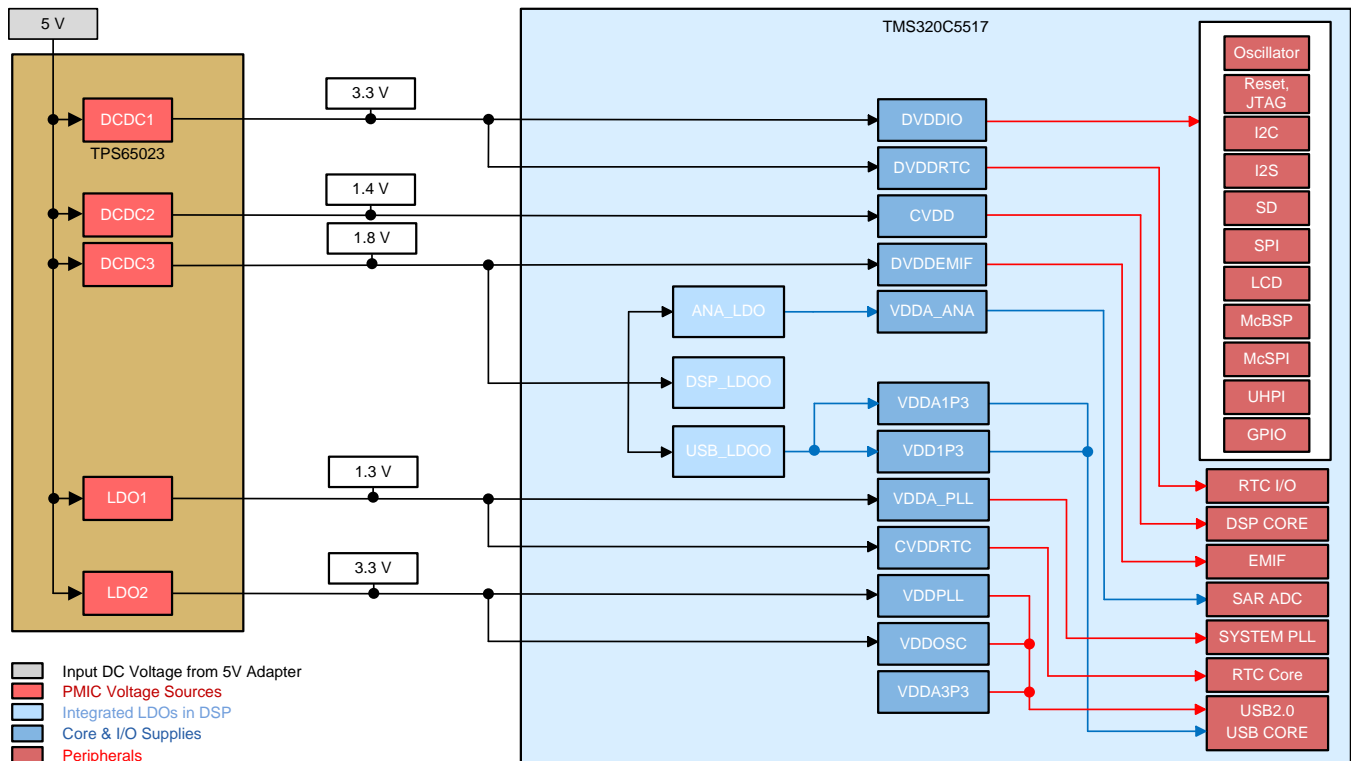
The device includes four core voltage-level supplies (CVDD, CVDDRTC, USB\_VDD1P3, USB\_VDDA1P3), and several I/O supplies including—DVDDIO, DVDDMIF, DVDDRTC, USB\_VDDOSC, and USB\_VDDA3P3.  8 highlights the set of peripherals available on the C5517 DSP used in this design and their I/O Power supplies:

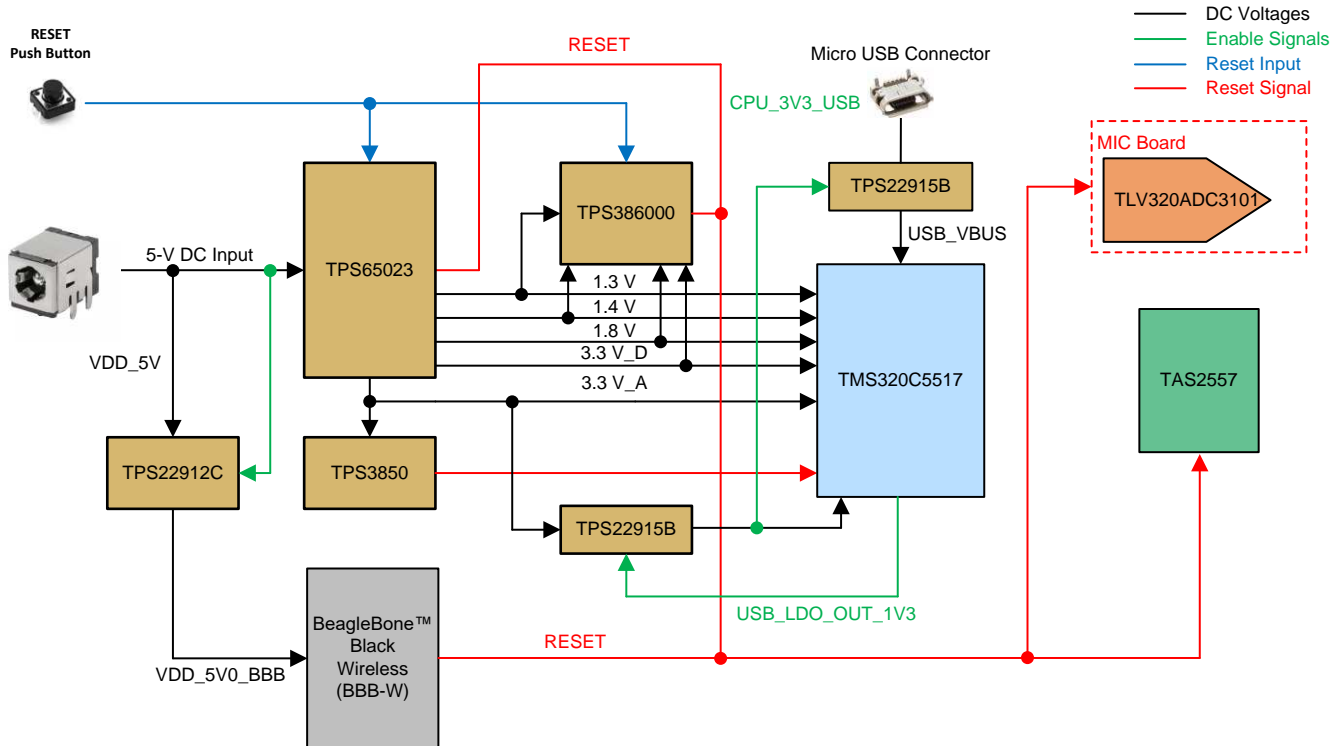
図 8. Peripherals in C5517 DSP and I/O Power Supplies



The C5517 DSP includes three low-dropout regulators (LDOs) which are used to regulate the power supplies of the SAR ADC and power management (ANA\_LDO), digital core (DSP\_LDO), and USB core (USB\_LDO). The device does not require a specific power-up sequence. In this design, the DSP\_LDO is disabled (DSP\_LDO\_EN = high) and an external regulator (DCDC2 of the TPS65023 PMIC) supplies power to the CPU core (CVDD).

TPS386000 and TPS3850 are used to monitor rails powering up C5517 DSP and the external reset signal (RESET) remains asserted until all of the supply voltages reach their valid operating ranges. 図 9 shows RESET architecture for whole design and power sequencing needed for USB section in C5517 DSP.

図 9. Reset and Power Sequencing



The I/O design allows either the core supplies (CVDD, CVDDRTC, USB\_VDD1P3, USB\_VDDA1P3) or the I/O supplies (DVDDIO, DVDDMIF, DVDDRTC, USB\_VDDOSC, and USB\_VDDA3P3) to be powered up for an indefinite period of time while the other supply is not powered if the following constraints are met:

1. All maximum ratings and recommended operating conditions are satisfied.
2. All warnings about exposure to maximum rated and recommended conditions, particularly junction temperature are satisfied. These apply to power transitions as well as normal operation
3. Bus contention while core supplies are powered must be limited to 100 hours over the projected lifetime of the device
4. Bus contention while core supplies are powered down does not violate the absolute maximum ratings

The USB subsystem in C5517 DSP must be powered up in the following sequence:

1. USB\_VDDA1P3 and USB\_VDD1P3
2. USB\_VDDA3P3
3. USB\_VBUS

A supply bus is powered up when the voltage is within the recommended operating range. The supply bus is powered down when the voltage is below that range, either stable or while in transition.

### HD AEC™ Running on C5517 DSP

The algorithms and processing written by *Adaptive Digital Technologies* for this demonstration correct for the problems that are found in microphone array and loud-speaker applications. Beamforming (BF), noise reduction (NR) and adaptive filtering algorithms focus the processing system on speech as the critical audio signal, and filter out other high-frequency and low-frequency signals in the environment. Non-linear processing helps account for the artifacts introduced by the acoustic characteristics of the system. The HD AEC is responsible for removing the echo coming from the 2-way real-time nature of the communication. Anti-howling and double talk detection work to balance audio signals, remove jitter in the transmitted signal and improve the overall quality of the final signal.

The HD AEC features very fast convergence, and demonstrates virtually no audio artifacts being transmitted based on a changing environment on the near-side. The HD AEC handles echo tails of up to 128 ms. A long echo tail allows the echo canceller to listen longer for audio reflections to remove. Short tail lengths mean a greater likelihood that acoustic echoes will be transmitted. Being a programmable DSP-based solution, the HD AEC is customizable for shorter or longer tail lengths (based on available processing resources) to more accurately suit the system environment.

### ***C5517 Boot Image Explained***

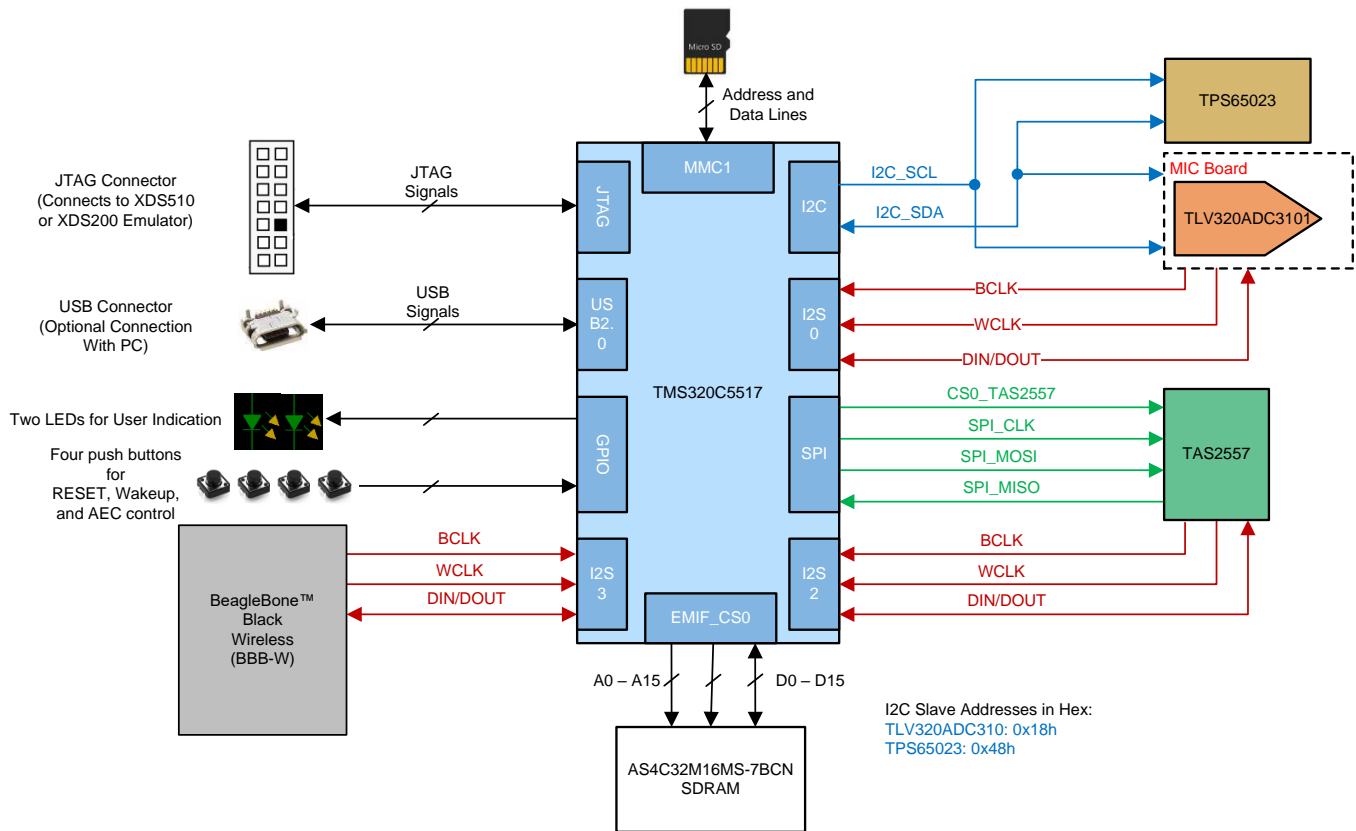
The C5517 DSP boots from the uSD card as SD Card is the default boot option for TIDA-01589. The SD card boot image on the C5517 DSP board contains the required software to run the audio processing application. The binary contents are as follows:

- Acoustic Echo Cancellation (AEC)
- Beamforming
- Acoustic Spectral Noise Reduction (ASNR)
- Dynamic Range Control (DRC)
- Drivers to control the TLV320ADC3101 ADC, TAS2557 Smart Amp and audio to and from the BeagleBone Black Wireless

### ***External Interfaces With C5517 DSP***

☒ 10 highlights external interfaces of C5517 DSP used in TIDA-01589.

図 10. Externals Interfaces With C5517 DSP



**JTAG Interface**

[XDS510 USB PLUS](#) and [XDS200 USB](#) JTAG emulator supports C5517 DSP with JTAG interface. The USB JTAG Emulator is a table top module that attaches to a personal computer or laptop to allow hardware engineers and software programmers to develop applications with TMS320C5517 DSP. TIDA-01589 DSP Board has 2 x 7 JTAG Male header (J7) mounted on board. The [BH-ADP-20e\\_cTI-14t\\_TI](#) adapter is required to interface between the JTAG header of the DSP board and header of the emulator. The adapter plugs onto the 2 x 7 female connector of the emulator on one side and the 2 x 7 male connector of the DSP board on the other. This adapter resolves the voltage differences required for correct operation. 図 27 shows the hardware connections for the JTAG connector on the DSP board with the emulator. JTAG connection with DSP board is not required to run the demonstration. It is only required for debugging and development purposes.

For more information on the JTAG interface implemented in this design, see the [XDS510 USB JTAG Emulator Installation Guide](#).

• **I2S Interface**

The C5517 DSP has a total of three I2S ports of which one is used to receive digital audio data from two microphones via the TLV320ADC3101 device, the second port is used to exchange audio data with the TAS2557 device to be played on the speaker and the third I2S port is used to pipe the audio in and out of the system to the BeagleBone black wireless.



## 2.3.4 Audio Out

### 2.3.4.1 Selection of Speaker

One of the first steps in an audio design is to decide which speaker to use. There are many different parameters to look at when making this decision: output power, SPL, size, cost, and more. TI's Smart Amp products work with a wide variety of speakers on the market, and it is important to confirm the following items to ensure highest audio quality:

- Nominal speaker impedance: 4 to 32  $\Omega$
- Resonant frequency: 200 to 1400 Hz

If the speaker follows these guidelines, it will allow for the highest quality of TI audio at the maximum sound pressure level.

Speaker key specifications are as follows:

1. Power rating
2. Speaker impedance
3. Sensitivity
4. Rated frequency range
5. Frequency response
6. THD variation over frequency range
7. Resonance frequency
8. Speaker dispersion or directivity

For this design, SPS0916B-J-01 speaker is selected and the speaker wires connect to Terminal Connector (J15) mounted on TIDA-01589 DSP board. If any other speaker is selected for integrating in End system then speaker parameter should be obtained for selected speaker. TIDA-01589 Software Package already includes characterization files for SPS0916B-J-01 speaker.

 13 highlights the step-by-step process from speaker characterization to end-system integration.

### 2.3.4.2 TAS2557 Smart Amp - 5.7-W Class-D Mono Audio Amplifier With Class-H Boost and Speaker Sense

The TAS2557 smart amplifier is a hybrid analog or digital device that includes several digital-signal-processing (DSP) blocks. A smart integrated multilevel Class-H boost converter maximizes system efficiency at all times by tracking the required output voltage. The TAS2557 can drive up to 3.8 W from a 4.2-V supply into an 8- $\Omega$  speaker with 1% THD, or up to up 5.7 W into a 4- $\Omega$  speaker with 1% THD. The Class-D output switching frequency is synchronous with the digital input audio sample rate to avoid left and right PWM frequency differences from beating in stereo applications. The *PWM Edge* rate control and *Spread Spectrum* features are available if further EMI reduction is desired. The TAS2557 internal processing algorithm automatically enables the boost when needed. A look-ahead algorithm monitors the input voltage and the digital audio stream. When the speaker output approaches the input voltage the boost is enabled in-time to supply the required speaker output voltage. When the boost is no longer required it is disabled and bypassed to maximize efficiency. The boost can be configured in one of two modes. The first is low in-rush (Class-G) supporting only boost on-off and has the lowest in-rush current. The second is high-efficiency (Class-H) where the boost voltage level is adjusted to a value just above what is needed. This mode is more efficient but has a higher in-rush current to quickly transition the levels.

図 11. Smart Amp Features Two Selectable Boost Functions

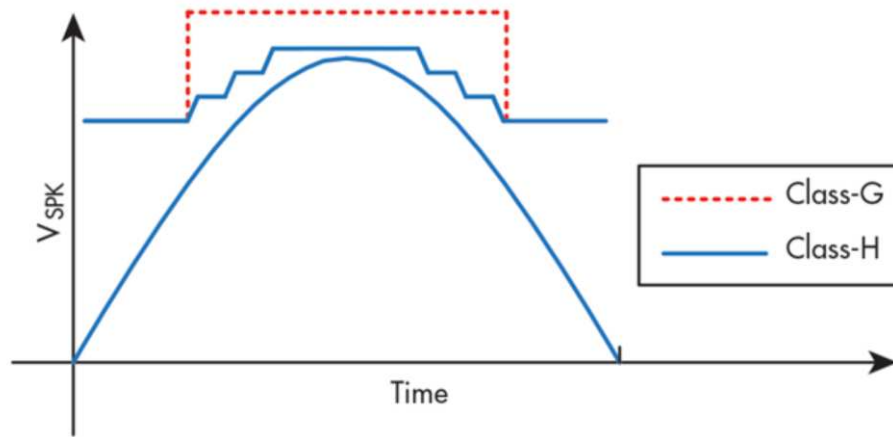


図 12 shows the TAS2557 functional block diagram:

図 12. TAS2557 Block Diagram

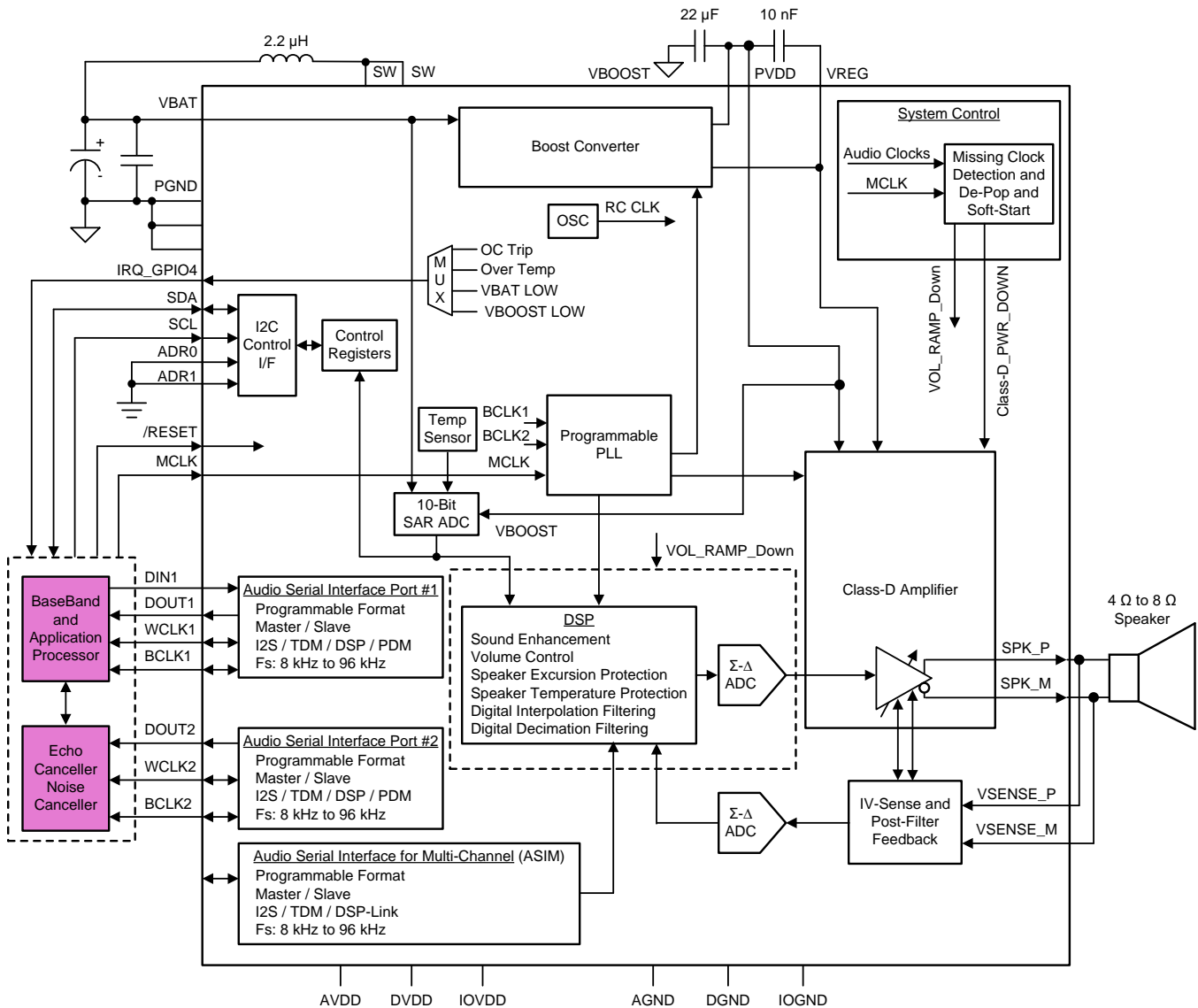


表 3 highlights recommended external components used for the TAS2557 design:

表 3. Recommended External Components

COMPONENT	DESCRIPTION	SPECIFICATION	MIN	TYP	MAX	UNITS	
L16	Boost converter inductor	Inductance, 20% tolerance	1	2.2		μH	
		Saturation current		3.1		A	
C108	Boost converter input capacitor	Capacitance, 20% tolerance		10		μF	
L61 and L62	EMI filter inductors (optional). These are not recommended because they degrade THD+N performance. The TAS2557 device is a filter-less Class-D and does not require these bead inductors.	Impedance at 100 MHz		120		Ω	
		DC resistance			0.095		
		DC current				2	A
		Size			0402		

表 3. Recommended External Components (continued)

COMPONENT	DESCRIPTION	SPECIFICATION	MIN	TYP	MAX	UNITS
C112	Boost converter output capacitor	Type		X5R		
		Capacitance, 20% tolerance		22		μF
		Rated voltage		16		V
		Capacitance at 8.5-V derating		7		V
C118 and C119	EMI filter capacitors (optional: must use L2 and L3 if C3 and C4 are used)	Capacitance		1		nF

TAS2557 provides speaker voltage and current sense for real-time monitoring of loudspeaker behavior. The V-Sense terminals are used to eliminate IR drop error due to packaging, PCB interconnect, and ferrite bead filter resistance. The V-sense terminals are also used to close the Class-D feedback loop post filter. There is a placeholder for Post-Filter Feedback (PFFB) which minimizes the THD introduced from the filter beads used in the system. Any interconnect resistance or non-linearities after the V-Sense terminals connection point will not be corrected for.

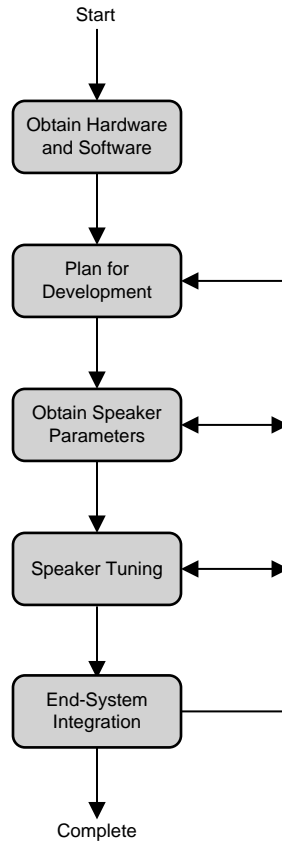
In this design, the TAS2557 device initializes with following configuration settings during after reset state:

- Mono or stereo mode: Mono
  - Mono or stereo configuration does not impact the device performance
- Control interface: SPI interface with C5517 DSP
  - TAS2557 as SPI slave and C5517 DSP as master
- Audio input interface: I2S interface with C5517 DSP
  - Configured as I2S master and C5517 DSP as slave
  - BCLK: 1.024 MHz
  - WCLK: 16 kHz
  - I2S word length: 24 bits
- Current and voltage data stream: digital audio, I2S interface
- I-Sense current range: 1.5 A
  - 6-Ω speaker load impedance
- Class-D edge rate control: 14 ns
  - This allows adjusting the switching edge rate of the Class-D amplifier, trading off efficiency for lower EMI.
- Boost mode: class-G
  - Low in-rush
- Boost current limit ( $I_{LIM}$ ): 3 A
- Source reference clock: 12.288 MHz (form external oscillator Y3)
  - The external reference clock is provided on MCLK pin (24th pin)
- Sampling frequency: 16 kHz

### 2.3.4.2.1 TAS2557 Development Overview

Figure 13 summarizes step-by-step Smart Amp evaluation, planning, characterization, tuning and end system integration:

Figure 13. Smart Amp Development Flow



#### Obtaining TI Hardware and Software:

Speaker characterization and tuning are performed using the PurePath™ Console 3 software. The TI Learning Board 2 and the TAS2557EVM are needed to fully evaluate and develop with TAS2557 Smart Amp.

- Order Learning Board 2 and TAS2557EVM from ti store.
- TI approval is required to download Smart Amp-related hardware software. Click the button in the TAS2557 device web site to begin the approval process. Once approved, the user receives an email confirming access to the mySecureSoftware web site. Download the PurePath™ Console 3 (PPC3) software from the PUREPATHCONSOLE software product page and TAS2557 App for PurePath™ Console 3 on mySecureSoftware.

All the resources are available on TAS2557 Device and EVM folders.

注: There is no need to download separate plugins – Smart Amp Applications are automatically available within the PurePath™ Console 3 once access is provided to the proper software product.

Contact [audio\\_software@ti.com](mailto:audio_software@ti.com) for any issues related to software access.

#### Plan for development:

Developing Smart Amp-based systems for the first time is different than working with conventional amplifiers. Information obtained during the speaker characterization process often leads to changes to the speaker or enclosure to maximize output and quality.

**Obtaining Speaker Parameters:**

It is important to know where to get the speaker parameters and to ensure their accuracy when starting an audio design. For Smart Amp devices, these parameters affect how the algorithm protects the speaker. 表 4 lists where to find the most important speaker parameters. Some of the parameters are found by using the *Learning Board 2*, but it is best to request these details in a data sheet from your speaker vendor. The *Speaker Characterization* section of the design guide focuses on the procedure to obtain speaker parameters using *Learning Board 2*.

**表 4. Smart Amp Speaker Parameters**

KEY PARAMETERS	OBTAINED FROM SPEAKER VENDOR DATA SHEET	OBTAINED FROM LEARNING BOARD CHARACTERIZATION
Xmax (mm)	Yes	No
Tmax (°C)	Yes	No
Temperature coefficient (K <sup>-1</sup> )	Yes	No
Sd (cm <sup>2</sup> )	Yes	No
Bl	Yes	No
Re (Ω)	Yes	Yes
f0 (Hz)	Yes	Yes
Tolerances of Re	Yes	No
Impedance transfer function	Yes	Yes
Excursion transfer function	Yes	Yes

**Speaker Characterization:**

Advanced speaker modeling is essential to maximize the performance of the selected speaker while still protecting it from damage. The speaker model is obtained using the characterization process in PPC3 (request access on the [Smart Amp product folder](#) on ti.com). The linear parameters of the speaker are obtained through the Characterization tab in the PPC3 software. Characterization of the speaker is done using the *Learning Board 2* along with the [TAS2557EVM](#) and [PurePath Console 3 \(PPC3\) Software](#).

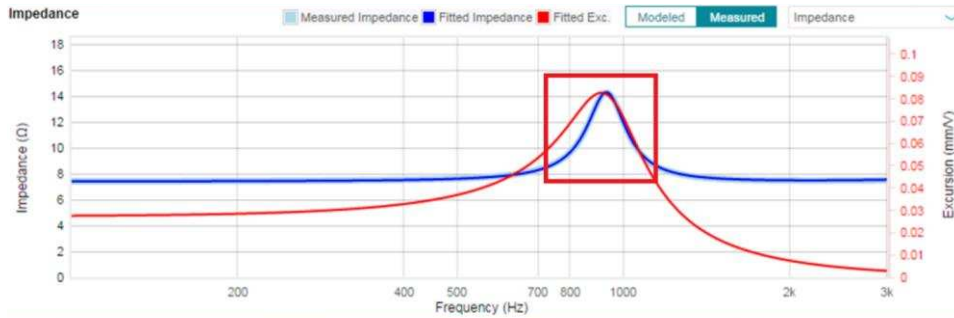
For step-by-step speaker-characterization procedures, see the *Speaker Characterization* section of the [Smart Amp Quick Start Guide](#). The video link for speaker characterization is: <https://training.ti.com/smart-amp-quick-start-how-characterize-your-speaker>.

The results from the characterization process provide the following 3 plots:

1. Impedance and excursion
  2. Temperature
  3. SPL
- Impedance and excursion plot

The impedance and excursion plot is similar to 図 14. In this plot, ensure there is a defined peak at the resonance frequency of the speaker as the red block in 図 14 highlights. Also ensure the impedance plot matches the plot in the speaker data sheet. If the resonance frequency is below the specified value on the speaker data sheet, this could indicate that there is a leak on the speaker box. If there is more than one resonance frequency, it could mean that the speaker box has a port or a passive radiator.

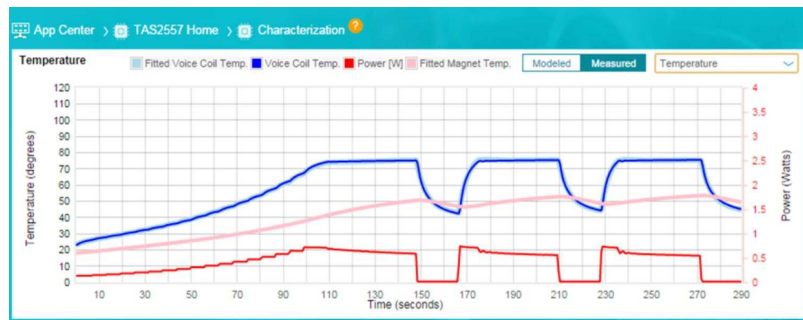
図 14. Impedance and Excursion Plot



- Temperature Plot

The temperature plot from the characterization will look similar to 図 15. Ensure there the speaker heats up to the maximum temperature of the speaker which is 75°C in 図 15

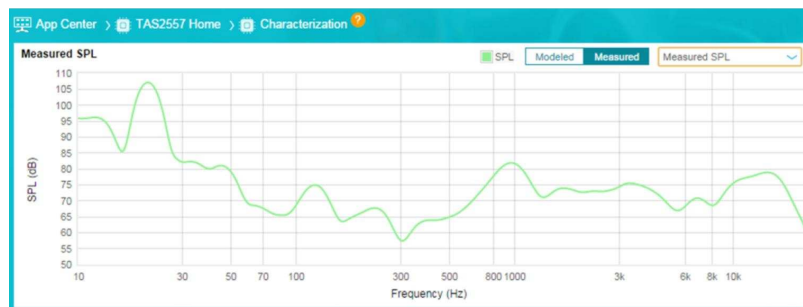
図 15. Temperature Plot



- SPL Plot

The SPL plot will look similar to the plot in 図 16. Lower frequencies (< 100 Hz) in the SPL plot show room noise, but they will not be used by the Smart Amp. To ensure the speaker is in a sealed enclosure (closed box), check to see if there is a peak at the resonance frequency of the speakers.

図 16. SPL Measurement Plot



**Speaker Tuning:**

Micro-speakers are especially limited in maximum SPL and bass response due to the small diaphragm size; however, the smart amp allows the user to tune the speaker to achieve the maximum audio quality from a limited speaker. Application specific speaker tuning is important to optimize the sound quality and SPL of a speaker. An example of this may be to have the highest quality sound for voice in a video doorbell, thermostat, and so forth. The TAS2557 Smart Amp allows custom speaker tuning all within the PPC3 Software GUI. PPC3 enables speaker tuning using 10 biquads and features like Psychoacoustic Bass Enhancer, and Dynamic Range Compression to mention a few.

It is assumed that the speaker parameters, such as the  $R_e$ ,  $B_l$ ,  $X_{max}$ ,  $T_{max}$ ,  $S_d$ , Thiele-Small model, and temperature model are measured and loaded correctly into the .ppc3 file before proceeding with the tuning. Import parameters from one .ppc3 file to another or enter them manually, if acquired by other means. For step-by-step speaker-tuning procedures, see the *Speaker Tuning* section of the [Smart Amp Tuning Guide](#).

### **End System Integration:**

The End System Integration step creates the final binary file for the end system driver to load. The final step of the Smart Amp Process is the End System Integration Step. Once this step is complete, users will be on your way in using TAS2557 to drive the audio requirements of the system. For step-by-step procedures on end-system integration, see the *System Integration Guidance* section of the [Smart Amp Tuning Guide](#).

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注: For more information on the end-system integration process, refer to the [TAS2555 End-System Integration Guide](#).

---

Speaker parameters may vary from the vendor data sheet. This can lead to inaccurate speaker protection in situations where one speaker model is used to fit all speakers. For this reason, the TAS2557 Smart Amp algorithm can be calibrated to the specific speaker parameters to ensure protection of the speaker on a speaker by speaker basis. The Factory Test and Calibration (FTC) is performed to calibrate the Smart Amp algorithm and protect the speaker from speaker parameter variations. The FTC obtains the speaker  $R_{e0}$ ,  $f_0$ ,  $Q$ , and voice coil temperature. TI recommends the FTC is performed on all units to ensure protection of the speaker. For step-by-step procedures on Factory Test and Calibration (FTC), see the *Factory Test and Calibration (FTC) Implementation* section of the [Smart Amp Tuning Guide](#).

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注: For more information on the tuning factory test and calibration, see the [TAS2555, TAS2557, and TAS2559 Factory Test and Calibration Guide](#).

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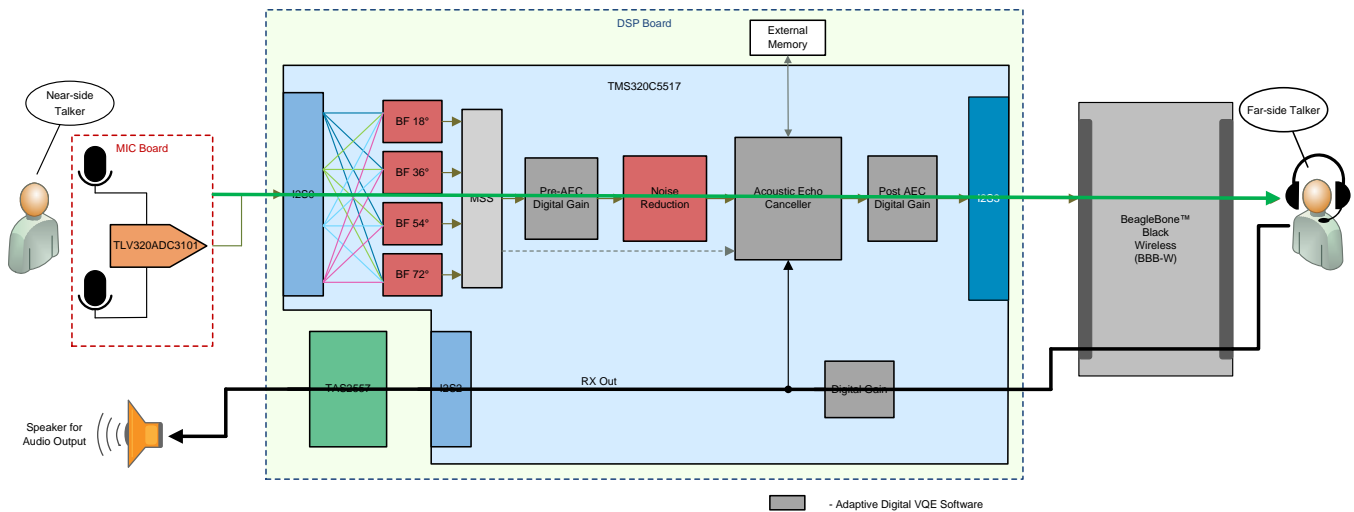
## **2.3.5 Connectivity With BeagleBone™ Black Wireless**

TIDA-01589 DSP board is designed as a “cape” for BeagleBone Black Wireless (BBB-W), which is used with this design to complete the two-way audio demonstration. [AM335x Linux Processor Software Development Kit 5.0 \(PSDK-Linux\)](#) supports the BeagleBone Black-Wireless and is used as the baseline kit for development of this demo. To run this demo, a dummy codec driver in Linux called “generic 2-way” is created to provide support for audio input and audio output. The device is referred to as a dummy codec because there is no specific hardware codec device being used. The main purpose of this driver is to facilitate moving audio from the audio serial port (McASP) driver level to the ALSA layer. In addition to adding a codec driver, Linux device tree changes are also required in order to configure the audio I/O connections between the AM335x and the codec. The McASP on the AM335x processor must be configured as a slave since the TAS2557 is responsible for generating the clocks in this design.



A multimedia framework called **Gstreamer** is used to capture and playback real time audio on the BBB-W. Upon boot, the USB dongle is detected by the BBB-W and two Linux audio services are started concurrently. Each service calls a python script that is responsible for calling a Gstreamer command. One Gstreamer command transfers audio from the DSP board to be played back over the headphone. The second command moves captured audio from the headset microphone to the DSP board. The flow from these commands are depicted in **Figure 17**, as the green line and black line, respectively.

**Figure 17. Gstreamer Script Flow**



The TAS2557 on the DSP board is required to be initialized before the “USR3” LED illuminates on the BeagleBone black wireless. This allows the proper clocks to be provided to the BeagleBone black wireless from the system master, and subsequently start the audio application by calling the Gstreamer commands.

## 3 Hardware, Software, Testing Requirements, and Test Results

### 3.1 Required Hardware and Software

#### 3.1.1 Getting Started Hardware

##### 3.1.1.1 Prerequisites

To properly setup the hardware connections with TIDA-01589, the following tools are required:

- DC adapter with 5-V, 6.5-A output rating
- [BeagleBone Black Wireless \(BBB-W\)](#)
- [XDS200 USB](#) or [XDS510 USB PLUS](#) JTAG Emulator (Optional: Not required to run demo)
- 20-pin compact TI (cTI) header to the standard 14-pin target JTAG header (Optional: Not required to run demo)
  - Manufacturer part number: [BH-ADP-20e\\_cTI-14t\\_TI](#)
- Two Micro SD Cards for Booting TIDA-01589 DSP Board and Beaglebone black wireless
- USB Audio Adapter
  - Manufacturer part number: [SD-CM-UAUD](#)
- External Headset with microphone with separate microphone and headphone cable or Normal Headset/earphone with Microphone along with [MIC and Headphone splitter cable](#)
  - Manufacturer part number for Headset with separate microphone and headphone cable: [87070](#)
- Two 3.5-mm male auxiliary to 3.5-mm female stereo audio extension cables
  - Manufacture part number: [25 Feet cable](#) or [15 Feet cable](#)
- TIDA-01589 Smartkit
  - TIDA-01589 MIC Board
  - TIDA-01589 DSP Board with Micro-speaker attached
  - Ribbon Cable to connect MIC and DSP Board

#### 3.1.2 Getting Started Firmware

##### 3.1.2.1 Prerequisites

To run the audio demonstration on the DSP board and BeagleBone Black Wireless, there are two software images that are required:

1. bootimg.bin – This is the binary that needs to be flash on the SD card for the TMS320C5517 DSP on DSP board.
2. BBB-W.zip – This directory needs to decompressed and the files are written on SD card for the BeagleBone Black Wireless.

---

注: Software images for BeagleBone black wireless and TIDA-01589 DSP board are provided by [Adaptive Digital](#). Contact Adaptive Digital for getting Boot images.

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## 3.2 Testing and Results

### 3.2.1 TIDA-01589 DSP board Software Setup

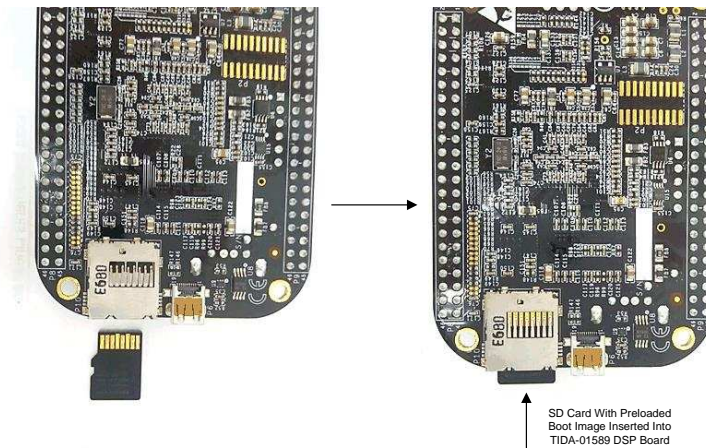
- Download Boot image for DSP board in PC and format the SD card in either FAT32 or FAT16 format
- Copy the downloaded ".bin" (ex: bootimg.bin) file to the formatted SD Card under root partition (filename MUST BE "bootimg.bin")

### 3.2.2 BeagleBone™ Black Wireless Software Setup

#### **SD Card setup:**

- Download Boot image for BeagleBone black wireless in PC and use this image file to create a SD Card containing the embedded Linux system provided with the Linux SDK  
To create the SD card, see [Windows SD Card Creation Guide](#). In short, SD card creation process involves writing download image to uSD card.
- After SD card creation, eject the SD card from PC and Insert SD card with preloaded boot image into BeagleBone™ Black Wireless as shown in [Figure 18](#)

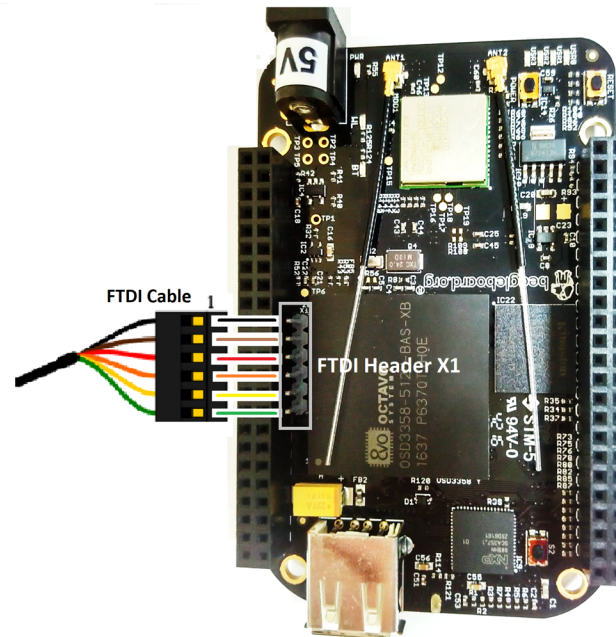
**Figure 18. SD Card With Pre-Loaded Boot Image Inserted Into BeagleBone™ Black Wireless**



#### **BeagleBone Black Wireless Terminal Setup:**

- Connect a FTDI cable to BeagleBone Black Wireless as shown in [Figure 19](#)

図 19. FTDI Cable Connected to BeagleBone™ Black Wireless



注: The black wire will be next to the TP6/X1 marker and connects the USB to the PC.

- Users can connect to the BeagleBone Black Wireless via a serial console of their choice and boot the device. The settings are shown in 図 20

図 20. Serial Port Settings

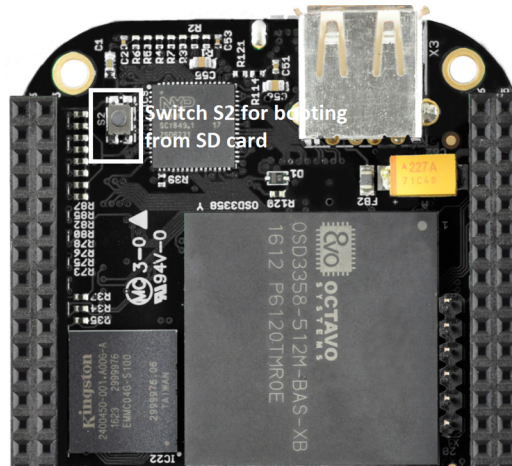
Tera Term: Serial port setup

Port:	<input type="text"/>
Baud rate:	<input type="text" value="115200"/>
Data:	<input type="text" value="8 bit"/>
Parity:	<input type="text" value="none"/>
Stop:	<input type="text" value="1 bit"/>
Flow control:	<input type="text" value="none"/>

**BeagleBone Black Wireless (BBB-W) SD card boot:**

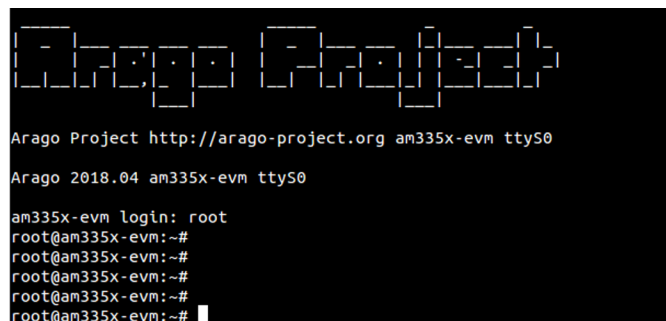
- By default, BeagleBone Black Wireless boots from the External MMC. To boot from the SD card, press and hold the S2 switch on BeagleBone Black Wireless and apply 5-V power to the BBB-W using DC Adapter.

図 21. Position of Switch S2 on BeagleBone™ Black Wireless



- Hold the S2 switch for a couple of seconds and once the boot is complete, the following prompt should be observed shown in 図 22

図 22. Prompt After Boot Completion



- Once the terminal is displayed, type the following command to clear the EMMC: “dd if=/dev/zero of=/dev/mmcblk1 bs=512 count=1024”. Now, reboot the board and the board should be booting from the SD card.

---

注: Making uSD card as the default Boot option on the BeagleBone black wireless is required only once.

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- Remove the FTDI cable and power from the BeagleBone Black Wireless.

### 3.2.3 Hardware Connections

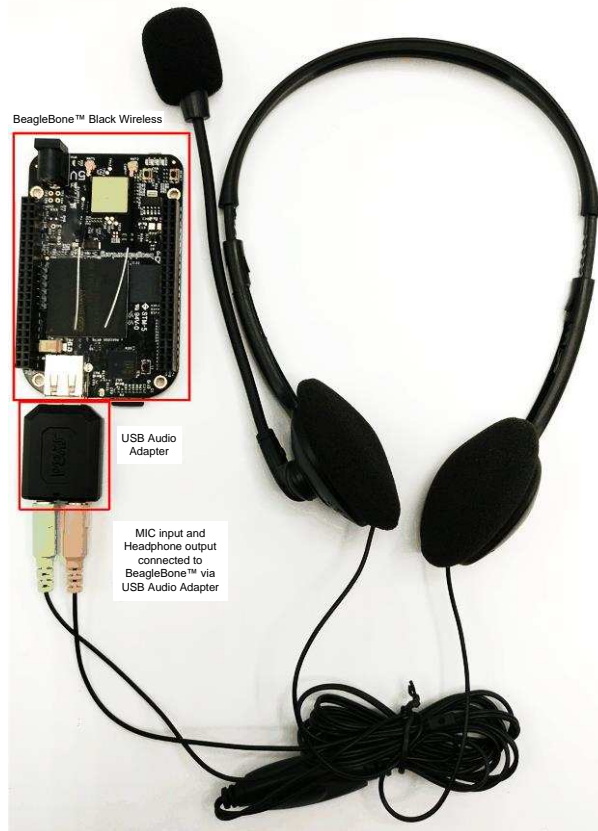
Prior to running the demonstration, some hardware considerations need to be made:

- Ensure that the SD cards are ready with boot images for DSP board and BeagleBone Black Wireless as per 3.2.1 and 3.2.2.

#### **BeagleBone™ Black Wireless Connections:**

- Connect the USB audio dongle onto the USB port of the BeagleBone Black Wireless and connect the headphones to the audio dongle with the microphone and headphones matched to the relevant port using stereo extension cables as shown in 図 23

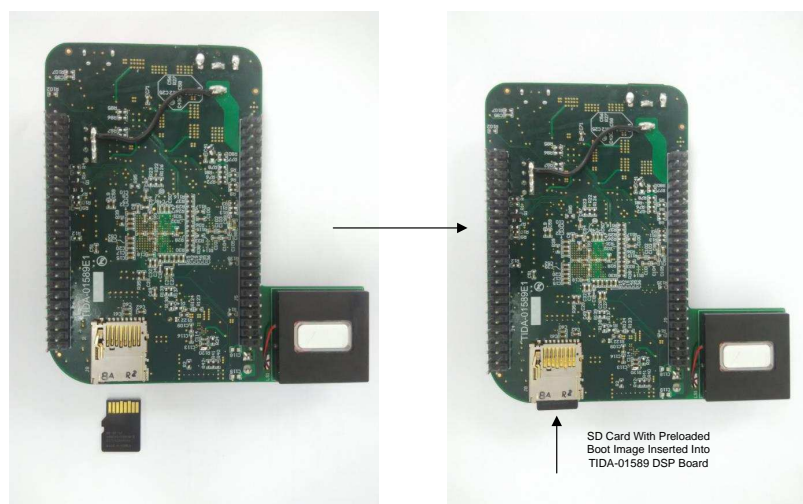
図 23. Headset Connected to BeagleBone™ Black Wireless via USB Audio Adapter



**DSP Board connections:**

- Insert other SD card with preloaded boot image into DSP board as 図 24 shows.

図 24. SD Card With Pre-Loaded Boot Image Inserted Into DSP Board



- Couple the BeagleBone Black Wireless (BBB-W) and the DSP board by placing the DSP board on top of the BBB-W. Ensure the orientation of the boards prior to combining are correct as shown in 図 25. The DC Jack of BBB-W and DSP board should be aligned vertically after proper mating as shown in 図 26

図 25. DSP Board Sitting on top of BeagleBone™ Black Wireless

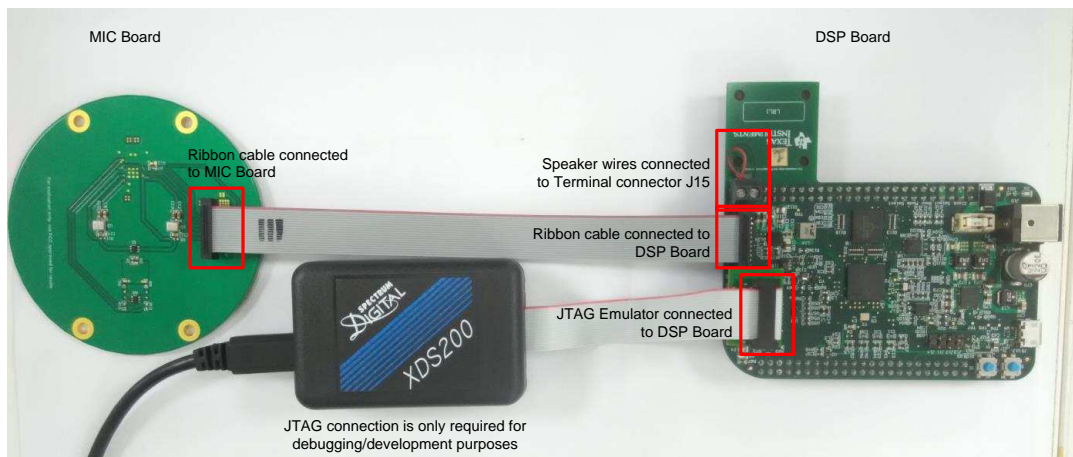


図 26. DSP Board Sitting on top of BeagleBone™ Black Wireless With DC Jacks Aligned



- Attach the speaker on the DSP audio board by screwing in the wires from the speaker onto the terminal connector J15 as shown in 図 27. The polarity is not important for the speaker wires.
- Connect one end of the ribbon cable on the J1 connector of the DSP board as 図 27 shows.

図 27. MIC Board and Speaker Wires Connected to DSP Board

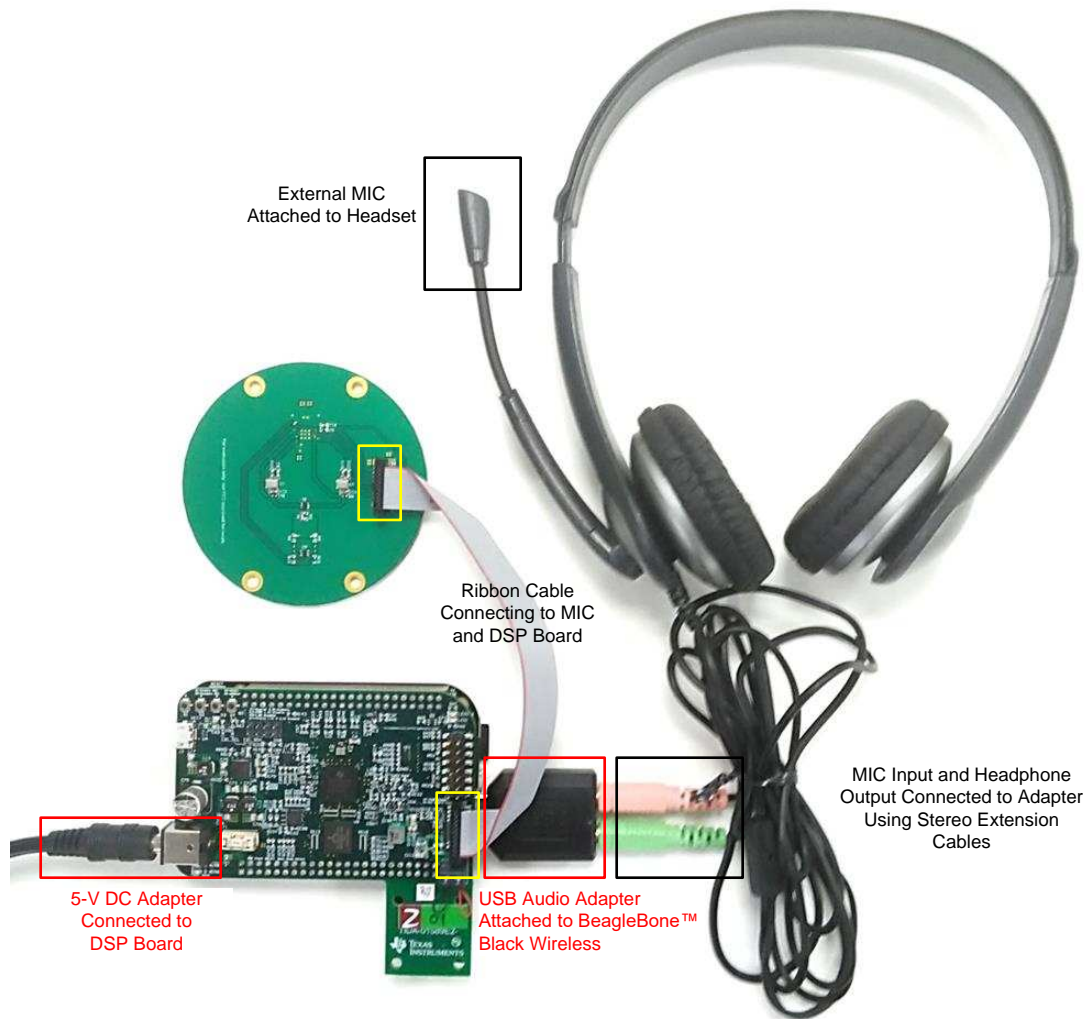


注: The JTAG connection with the DSP board is not required to run the demonstration. It is only required for debugging and development purposes.

**MIC board Connections:**

- Connect other end of the ribbon cable on the microphone board as shown in [Figure 27](#). The cable can only be inserted in a fixed direction and not be reversed.
- At last, connect a 5-V DC Adapter to Power Jack J10 on the DSP board. This will ensure both the BeagleBone Black Wireless and DSP board are powered.

**Figure 28. TIDA-01589 Demonstration Setup**





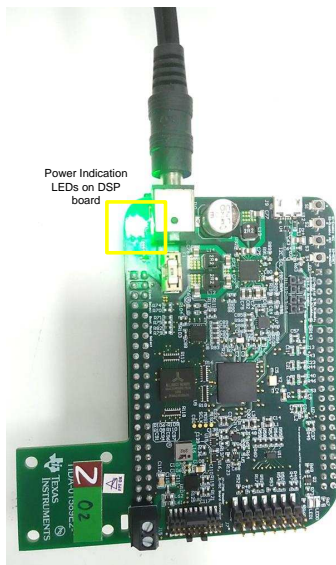
### 3.2.4 Test Board Preparation

After connecting a 5-V DC adapter to the DSP board, the following LEDs are present onboard for indicating user on proper power-up and booting operation:

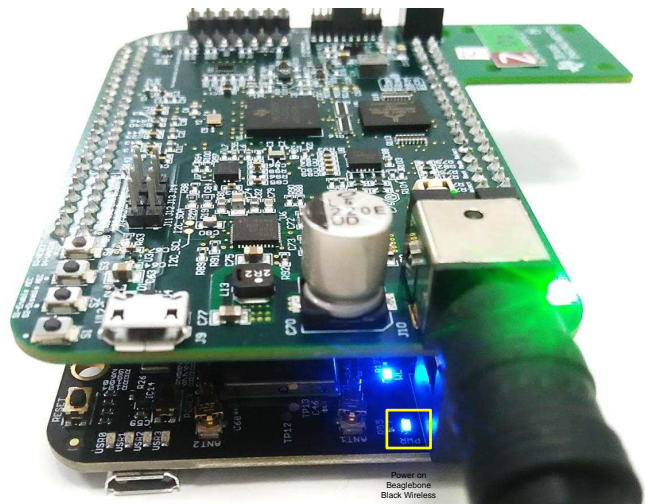
**LED indications of power:**

- Two green power LEDs Vin\_5V and VDD\_BBB will indicate power being supplied to the DSP board and BBB-W respectively as shown in [Figure 29](#)
- The blue power LED on the BeagleBone Black Wireless indicates power on the BBB-W as [Figure 30](#) shows.

**Figure 29. Power Indication LEDs on DSP Board**



**Figure 30. Power Indication LED BeagleBone™ Black Wireless**



- The Blue power LED on the MIC board indicates the power on the board as [Figure 31](#) shows.

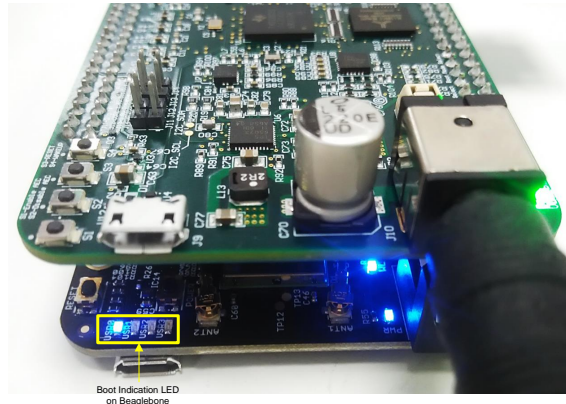
図 31. Power Indication LED on MIC Board



**LED indications of Booting and Initialization:**

- The Linux image will be boot of the SD card on the BeagleBone Black Wireless and USRx LEDs on the BeagleBone Black Wireless will indicate successful boot of the Linux Kernel as shown in [図 32](#)

**図 32. Boot Indication LEDs on BeagleBone™ Black Wireless**



注: After a successful boot, the USRx LED on the BeagleBone black wireless glows continuously. DSP board boots much faster than Beaglebone Black Wireless.

- Two red LEDs D1 and D2 on the MIC board glow continuously indicating the presence of MIC BIAS as [図 33](#) shows.

**図 33. MIC BIAS and ADC3101 Initialization Indication LEDs on MIC Board**

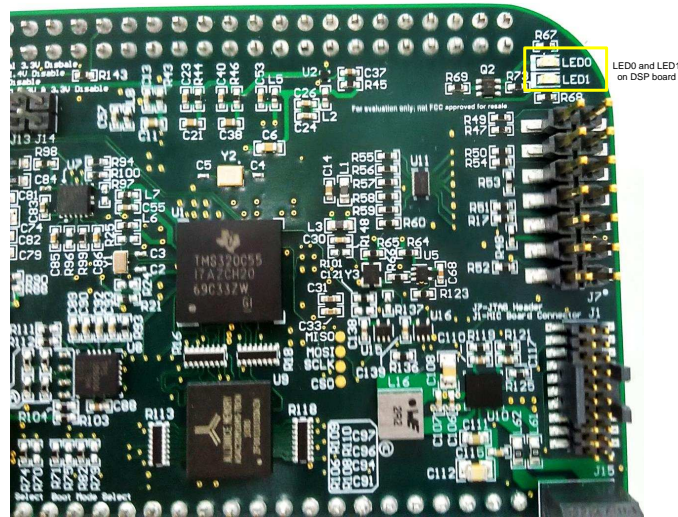


- Blue LEDs D3 and D4 on MIC board will illuminate indicating a successful initialization of the TLV320ADC3101 as shown in [図 33](#)

**AEC and NR Enable/Disable Indication LEDs:**

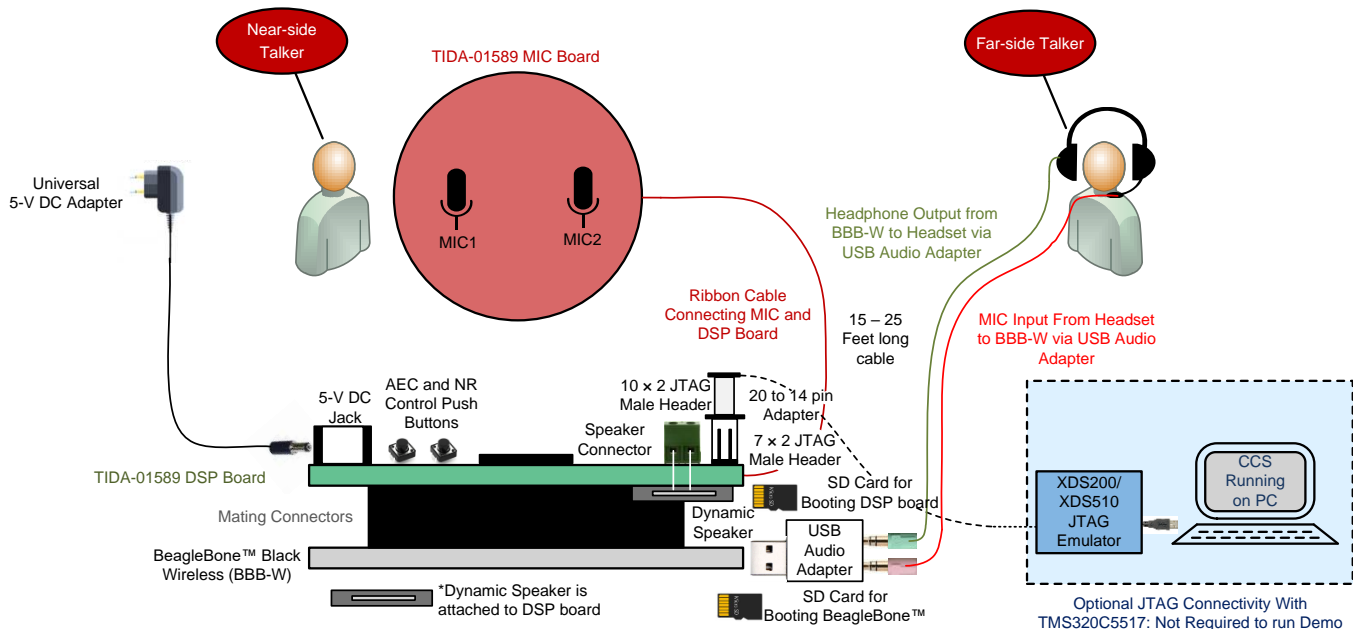
- Green LED LED0 on DSP board indicates enable or disable status of Acoustic Echo Cancellation (AEC) running on C5517 DSP. LED0 glows continuously when AEC is enabled.
- Green LED LED1 on DSP board indicates enable or disable status of Noise Reduction (NR) running on C5517 DSP. LED1 glows continuously when NR is enabled.

図 34. LED0 and LED1 for Enable or Disable Status of AEC and NR



### 3.2.5 Test Setup

図 35. TIDA-01589 Test Setup



### 3.2.6 Test Procedure

Once the DSP board and beaglebone black wireless are able to boot successfully, verify proper operation by following procedure:

1. Speak in normal tones from a normal distance into the MIC board. The audio captured by the MIC board should be transmitted and audible through the headset attached to the beaglebone black wireless via audio adapter.
2. Speak in normal tones into the microphone that is part of the headset. The audio should be heard through the external speaker attached to the DSP board.

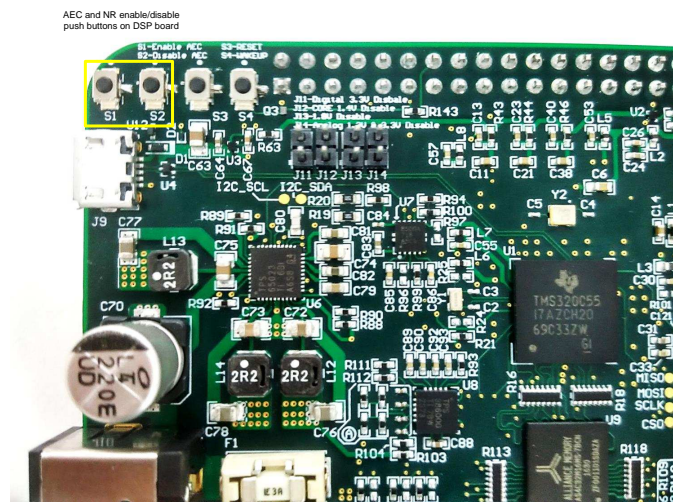
If each of these tests are successful, the boards and demonstration is operating properly. Proceed to [3.2.6.1](#) and [3.2.6.2](#) for further testing.

If the tests are not successful, remove power from DSP board and review the steps in [3.2.1](#), [3.2.2](#) and [3.2.3](#) to make sure each connection is correct and robust. Proceed to reviewing the software setup steps and try again.

### 3.2.6.1 Audio Echo Cancellation testing

1. With both boards booted successfully, test the functionality of audio echo canceller running on C5517 DSP.
2. By default, the AEC is enabled. Speak into the far-end microphone(attached to Headset) and the near-end speaker(attached to DSP board) outputs the audio without any echo being heard on the far-end speaker. Test the same in the reverse direction by speaking into the mic board on the near-end, and the spoken audio is heard out of the far-end headphones without hearing any echo back on the near-end.
3. LED0 on DSP board glows continuously when AEC is enabled.
4. Press switch S1 on the DSP board to disable the AEC functionality. Speak into either microphone and echoed speech should now be observed. Press switch S1 to enable AEC again.

☒ 36. Enable and Disable AEC Push Buttons on DSP Board



### 3.2.6.2 Noise Reduction Testing

1. By default, NR is enabled, With a source of white noise playing close to the MIC board (near-end), speak into the MIC board and observe the output of the audio on micro-speaker attached to speaker. The audio will have noise eliminated from the speech as a result of the Adaptive Spectral Noise Reduction (ASNR) algorithm executing on the C5517 DSP. To better observe the noise suppression levels, it is recommended to record the audio on a PC and use software such as [Audacity](#) to evaluate the audio spectrum.
2. LED1 on DSP board glows continuously when NR is enabled.
3. Press switch S2 on the DSP board to disable the NR functionality and notice the difference. Press switch S2 to enable NR again.

### 3.2.7 Test Results

表 5 provides MIPS and memory usage data of different algorithms running on C5517 DSP

**表 5. MIPS and Memory Usage Data**

DSP ALGORITHM	MIPS AVERAGE, PEAK	MEMORY (BYTES)			INSTANCE DATA (BYTES)		
		PROGRAM	DATA	TOTAL	INSTANCE SIZE	NUMBER INSTANCES	TOTAL
Fixed Beamformer	9.2 avg	6844	344	7188	1360	2	2720
	9.3 peak						
Noise reduction	13.2 avg	7429	1926	9355	4886	2	9772
	13.5 peak						
HD AEC	113.1 avg	54617	11608	66225	67120	1	67120
	131.1 peak						
Full DSP Application	136.6 avg			308142			
	157.3 peak						

---

注: All program and data fits on the internal memory of the C5517 DSP. The external SDRAM is used to only store uninitialized data capture buffers.

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## 4 Design Files

### 4.1 Schematics

To download the schematics, see the design files at [TIDA-01589](#).

### 4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-01589](#).

### 4.3 PCB Layout Recommendations

#### 4.3.1 Layout Prints

To download the layer plots, see the design files at [TIDA-01589](#).

### 4.4 Altium Project

To download the Altium Designer® project files, see the design files at [TIDA-01589](#).

### 4.5 Gerber Files

To download the Gerber files, see the design files at [TIDA-01589](#).

### 4.6 Assembly Drawings

To download the assembly drawings, see the design files at [TIDA-01589](#).

## 5 Software Files

To download the software files, see the design files at [TIDA-01589](#).

## 6 Related Documentation

1. [MICROPHONE SPECIFICATIONS EXPLAINED Application Note](#)
2. [XDS510 USB JTAG Emulator Installation Guide](#)
3. Texas Instruments, [TMS320C5517 Digital Signal Processor Technical Reference Manual](#)
4. Texas Instruments, [C55x v3.x CPU Reference Guide](#)
5. Texas Instruments, [Power Estimation and Power Consumption Summary for TMS320C5517 Device Application Report](#)
6. Texas Instruments, [Sitara™ Linux ALSA DSP Microphone Array Voice Recognition Application Report](#)
7. Texas Instruments, [Usage Guidelines for C55x On-Chip Low Dropout Regulators \(LDOs\) Application Report](#)
8. Texas Instruments, [Smart Amp Quick Start Guide Application Report](#)
9. Texas Instruments, [Getting Started with Smart Amp Development](#)
10. Texas Instruments, [Smart Amp Tuning Guide Application Report](#)
11. Texas Instruments, [TAS2557 and TAS2559 End-System Integration Guide Application Report](#)
12. Texas Instruments, [TAS2555, TAS2557, and TAS2559 Factory Test and Calibration Guide Application Report](#)
13. [Make Your Audio System Sound Better with Smart Amp Technology](#)
14. Texas Instruments, [SmartPA Speaker Protection Algorithm Application Report](#)

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## 7 About the Author

**SURYA MISHRA** is a systems engineer at Texas Instruments where he is responsible for developing reference design solutions for the Building Automation, Industrial Segment. Surya earned his bachelor of electronics and communication engineering from the Motilal Nehru National Institute of Technology (MNNIT), Allahabad.



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