参考資料

TI Designs: TIDA-010010
産業用ギガビット・イーサネットPHYのリファレンス・デザイン

概要

PLCアプリケーションには、高速のギガビット・イーサネット・インターフェイスが必要です。このインターフェイスは、Sitara™ AM5728プロセッサ内のギガビット・イーサネットMACペリフェラル・ブロックにDP83867IR産業用ギガビット・イーサネット物理レイヤ・トランシーバを実装したTIのリファレンス・デザインを使うことで実現できます。

このTI Designでは、DP83867IR産業用ギガビット・イーサネット物理レイヤ・トランシーバ(PHY)を、Sitara™AM5728高性能アプリケーション・プロセッサ内のギガビットMAC(GMAC)ペリフェラル・ブロックに接続する方法を紹介します。このハードウェア設計は、AM5728評価モジュール(EVM)の回路図とレイアウトに基づいていますが、2つのKSZ9031イーサネットPHYをTIのDP83867IRギガビット・イーサネットPHYに置き換えています。DP83867IRによるソリューションには、従来のソリューションと比較して基板面積が小さく、部品数(BOM)が少なく、消費電力が小さく、総製造コストを削減できるなど多くの利点があります。このTI Designでは、電源供給、イーサネットPHYのクロック生成、RGMIIおよびMDIインターフェイスなどの設計課題に対処しています。パワー・オン・リセットの生成、ブートストラップ機能、レジスタ構成に関するDP83867IR PHYの参照実装も提供します。

リソース

TIDA-010010	デザイン・フォルダ
DP83867IR	プロダクト・フォルダ
AM5728	プロダクト・フォルダ
TPS659037	プロダクト・フォルダ
TPS54531	プロダクト・フォルダ

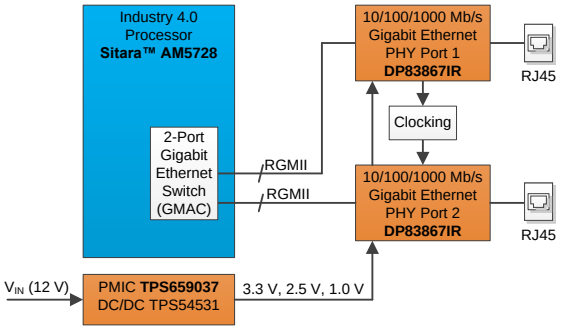
TI E2E™ Community　E2E™エキスパートに質問

特長

- 過酷環境向けDP83867IR産業用ギガビット・イーサネットPHYと Sitara™AM5728高性能アプリケーション・プロセッサの統合
- 電源のコストを低減し、RGMII終端抵抗とPHYクロック生成ツリーを内蔵することで、ギガビット・イーサネット・デバイス統合の部品表(BOM)を簡素化
- 最大457mWの低消費電力で動作するDP83867IR産業用イーサネットPHY
- MDI終端抵抗を内蔵することで、BOMの削減、基板面積の削減、レイアウトの単純化を実現
- DP83867IR PHY内のMII、GMII、RGMII終端インピーダンスをプログラム可能
- DP83867IR PHYレジスタ構成例(ブートストラップ、MDIOソフトウェア付き)
- パワー・オン・リセットとPHYブートストラップのための、RGMIIとMDIOのシグナル・インテグリティの確保

アプリケーション

- ファクトリ・オートメーション/制御
- 産業用ドライブ
- グリッド・インフラ
- ビルディング・オートメーション



1 System Description

This TI design interfaces the DP83867IR gigabit Ethernet PHY to the Sitara AM5728 high performance application processor from Texas Instruments (TI). The hardware schematics are based on the AM5728 evaluation module (EVM) and replaces the KSZ9031 Ethernet PHY with DP83867IR Ethernet PHY. System designers can leverage from the benefits of using DP83867IR for reduces board space and BOM, reduced PHY power consumption. The TI design is a hardware reference implementation and reference register configuration for the DP83867IR with AM5728.

The TI design addresses system designer challenges like RGMII and MDI signal integrity, DP83867IR bootstrap configuration, register configuration over MDIO, DP83867IR clocking tree and DP83867IR voltage supply generation.

1.1 Key System Specifications

表 1. Key System Specifications

FUNCTION	SPECIFICATION	COMMENT
Number of Ethernet ports	2 Ports	2 × DP83867IR
MDI	1000BASE-T (copper), 100BASE-TX, 10BASE-Te	-
MAC interface	RGMII	-
EMAC and switch	2-Port gigabit Ethernet (GMAC)	GMAC integrated inside Sitara AM5728
Status LEDs	2 per single Ethernet Port	Integrated into RJ45 jack
IEEE 1588v2	Y	Hardware enabled, not tested
RJ45 jack with integrated transformer	Y	-
Serial Management Interface (SMI)	Y	-
Low power	457 mW in 1000Base-T (copper) mode	-
Integrated termination resistors	Y	Integrated into DP83867IR
RGMII delay mode on RX and TX	Programmable delay	Integrated into DP83867IR
Clock	25 MHz (<50 ppm)	-
Shared clocking tree	Y	PHY 1 generated clock for PHY 2
Ethernet PHY power supply	Onboard power management integrated circuit (PMIC) generates 3.3 V, 2.5 V and 1.0 V	No additional DC/DC or LDO needed

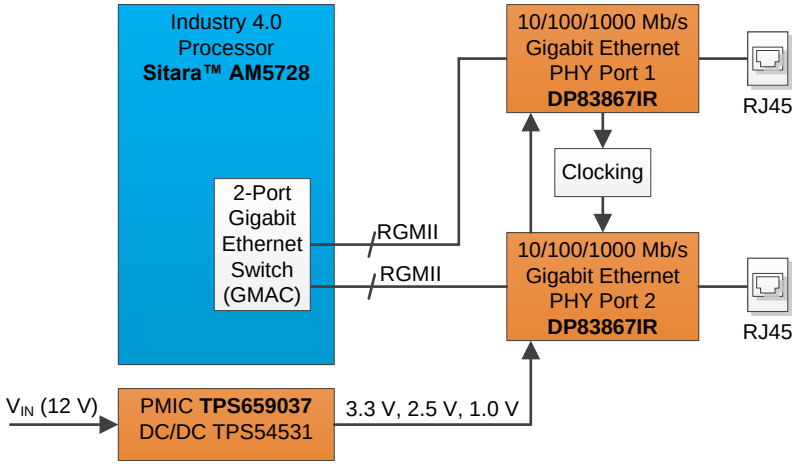
表 1. Key System Specifications (continued)

FUNCTION	SPECIFICATION	COMMENT
Reference register configuration software	Y	Based on TI real-time operating system (RTOS) with source code portable to other operating systems

2 System Overview

2.1 Block Diagram

図 1. TIDA-010010 Block Diagram



2.2 Design Considerations

This TI design interfaces the DP83867IR gigabit Ethernet PHY to the Sitara AM5728 high-performance application processor. The AM5728 EVM (TMDSEVM572X) uses the KSZ9031 Ethernet PHY which has several disadvantages when compared to the DP83867IR gigabit Ethernet PHY solution. This TI design shows engineers on how to migrate to the DP83867IR gigabit Ethernet PHY solution on the area of RGMII interface signal integrity, PHY bootstrap configurations, PHY register configuration over MDIO, PHY clocking, PHY power supply. It also lists alternative power supply and clocking options.

2.3 Highlighted Products

2.3.1 DP83867IR 10/100/1000-Mbps Gigabit Ethernet PHY

- Fully compatible to IEEE 802.3 10BASE-Te, 100BASE-TX, and 1000BASE-T specification
- Industrial operating temperature range –40°C to 85°C
- Clock output to clock additional PHYs using one crystal (or clock) source
- 8-kV IEC 61000-4-2 ESD protection (direct contact)
- RGMII interface with support for programmable clock skew
- RGMII Integrated termination resistors
- Low power: 457 mW
- Low deterministic TX and RX latency

For the full feature description, see the *DP83867IR Robust, Low Power 10/100/1000 Ethernet Physical Layer Transceiver* data sheet.

2.3.2 AM5728 Sitara Processor: Dual ARM® Cortex®-A15 and Dual DSP

- ARM dual Cortex-A15 microprocessor subsystem
- Up to 2 C66x™ floating-point VLIW DSP

- 2-Port *Gigabit Ethernet* (GMAC)
- 2 × dual-core *Programmable Real-Time Unit and Industrial Communication Subsystem* (PRU-ICSS) for industrial Ethernet
- Up to 2.5MB of on-chip L3 RAM
- Two DDR3, DDR3L Memory Interface (EMIF) Modules
- Quad SPI (QSPI)
- PCI-Express® 2.0 Subsystems with two 5-Gbps lanes
- *Dual Controller Area Network* (DCAN) modules

For the full feature description, see the *AM572x Sitara™ Processors Silicon Revision 2.0* data sheet.

2.3.3 TPS659037 Power Management Unit (PMU) for Processors

- Seven step-down *Switched-Mode Power Supply* (SMPS) regulators
- Seven general-purpose Low Dropout Regulators (LDOs) with 50-mV steps
- Short-circuit protection
- Powergood indication (voltage and overcurrent indication)
- Clock management 16-MHz crystal oscillator and 32-kHz RC oscillator
- *Real-Time Clock* (RTC) with alarm wake-up mechanism
- 12-bit Sigma-Delta General-Purpose Analog-to-Digital Converter (ADC) with three external input channels and six internal channels for self monitoring
- Thermal Monitoring: High temperature warning and thermal shutdown
- Undervoltage Lockout

For the full feature description, see the *TPS65903x-Q1 Automotive Power Management Unit (PMU) for Processor* data sheet.

2.3.4 TPS54531 570-kHz Step-Down Converter

- 3.5 to 28 V input voltage range
- Adjustable output voltage down to 0.8 V
- High efficiency at light loads with a pulse skipping Eco-mode
- 570-kHz switching frequency
- Overvoltage transient protection
- Cycle-by-cycle current-limit, frequency fold back and thermal shutdown protection
- Available in easy-to-use thermally enhanced 8-pin SO PowerPAD package

For the full feature description, see the *TPS54531 5-A, 28-V Input, Step-Down SWIFT™ DC-DC Converter With Eco-mode™* data sheet.

2.4 System Design Theory

2.4.1 DP83867IR Gigabit Ethernet PHY and AM5728 EVM Introduction

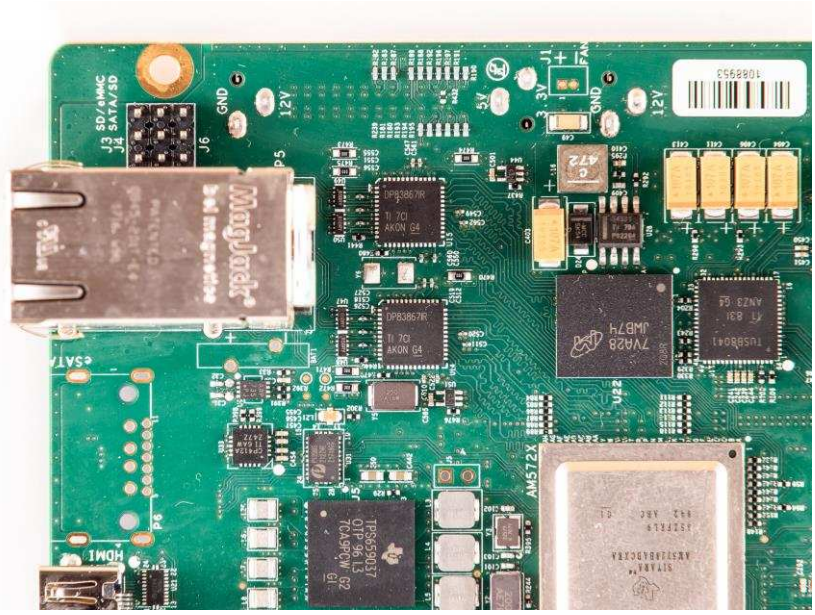
The AM5728 EVM is a high-performance application processor evaluation and development platform with dual ARM Cortex A-15 and two C66x DSP. TI offers processor software development kits (Processor SDK) for TI RTOS (real-time operating system), Linux (high level operating system, HLOS) and Linux RT (real-time Linux). Engineers can reuse the existing hardware and software infrastructure when interfacing the DP83867IR gigabit Ethernet PHY with the AM5728 EVM.

Using the DP83867IR in designs has several advantages over the KSZ9031:

- DP83867IR supports harsh industrial environments
- Industrial temperature range from –40°C to +85°C
- Small form factor in QFN(48) package
- Reduced system power consumption
- Simplifying BOM by removing large size FETs for PHY power generation
- Using existing PMIC to generate DP83867IR voltage supply
- First PHY generates clock for second PHY
- Integrated termination resistors in RGMII and MDI interface, no need to add external resistors

図 2 shows the board.

図 2. DP83867IR Gigabit Ethernet PHY on AM5728 EVM



The next sections explain the integration of the DP83867IR onto the AM5728 EVM.

2.4.2 DP83867IR Power Supply Generation

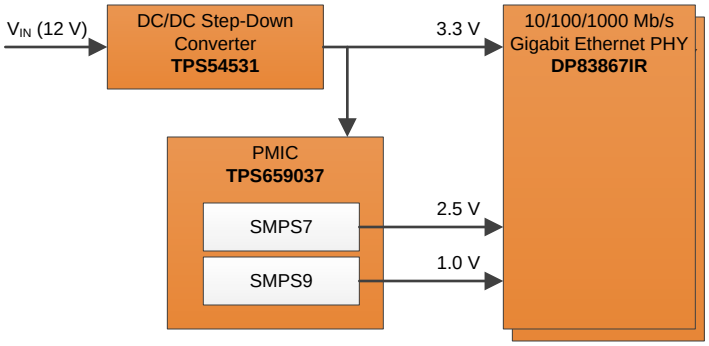
The DP83867IR device support either a 2-supply or a 3-supply configuration. The difference between these two configurations is an additional 1.8-V supply in the 3-supply configuration, leads to archive additional power savings. The 1.8-V supply is removed in the 2-supply configuration. This TI design uses the 2-supply configuration. More information on power supply is found in the *DP83867IR Robust, Low Power 10/100/1000 Ethernet Physical Layer Transceiver* data sheet.

The DP83867IR Ethernet PHY requires the following voltage supplies for the 2-supply configuration: 3.3 V, 2.5 V and 1.0 V for the QFN48 package.

The current (typical values) for each voltage rail are:

- 3.3 V: 14 mA
- 2.5 V: 137 mA
- 1.0 V (QFN48 package): 108 mA

図 3. DP83867IR Power Supply Generation



The 3.3-V voltage for the DP83867IR is generated by the TPS54531 step-down converter which generates the 3.3-V supply for the complete board. The 2.5 V and 1.0 V are generated by two SMPT rails within the TPS6590378, which were unused in the TMDSEVM572X EVM design. The two SMPT rails are configured and enabled by the application software because they are not present after PMIC power up. Note that using the AM5728 internal boot ROM does not enable those voltages hence prevent using the internal boot ROM to boot from Ethernet option. However, any external bootloader (for example, MLO, u-boot, and so forth) can enable the SMPT supply rails of the PMIC to enable boot over Ethernet by the secondary bootloader.

注: In case the system design does not allow using two SMPT rails of the PMIC, use the following alternative options to generate 2.5-V and 1.0-V voltage supply.

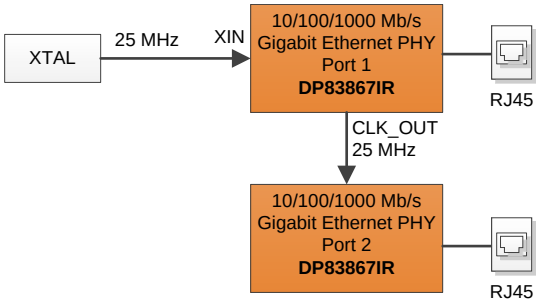
1. WCSP package option with 0.35-mm pitch enables smaller PCB board space area
   - From 5-V or 3.3-V source voltage to 2.5-V supply voltage: TPS62802 - this is a 5.7 mm^2 total solution size when using 0603 inductor and 0402 capacitors.
   - From 5-V or 3.3-V or 2.5-V source voltage to 1.0-V supply voltage: TPS62801 - this is 5.7 mm^2 total solution size when using 0603 inductor and 0402 capacitors
2. QFN package option
   - From 5-V or 3.3-V voltage to 2.5-V supply voltage: TPS62230
   - 5-V or 3.3-V or 2.5-V voltage to 1.0 V: TPS62239

2.4.3 DP83867IR Clock Generation

The TMDS5728EVM uses a two crystal clock solution approach, that is, one crystal generating 25-MHz clock for each PHY. This TI design leverages the CLK_OUT signal available from the DP83867IR, which is a 25-MHz clock signal generated by the PHY form the XIN signal. Use the CLK_OUT signal from the first PHY to provide the 25-MHz clock to a second PHY. Therefore the second crystal is not required and can be removed from the BOM.

The 25-MHz crystal is connected to the XIN/XOUT of the first PHY. After power up the first PHY outputs the 25 MHz at the CLK_OUT pad, which is feed into the XIN of the second PHY. Note that a dedicated reset sequence is required for this daisy chaining of clocks, which is controlled by the application processor using GPIOs.

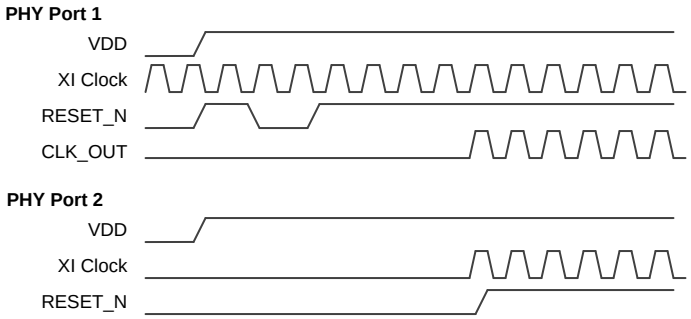
図 4. DP83867IR Clock Generation



2.4.4 DP83867 Reset Generation

The use of the daisy chained clock approach - - requires a specific PHY reset sequence after power up. The reason for the reset sequence is that a valid clock signal needs to be present at the PHY before the RESET signal is released. Once power is applied to the first PHY the crystal starts to generate the 25-MHz clock at the XIN pad. After 25 MHz are present at the first PHY the RESET signal of the first PHY is released. It takes then some specific time inside the first PHY before the CLK_OUT signal puts out 25-MHz clock. This TI design uses the worst case delay time of 201 ms. After 201 ms the second PHY will have 25 MHz at the XIN pad and the RESET signal of the second PHY can be released.

図 5. DP83867 Reset Generation



The reset generation of the PHY cannot be controlled by the a single GPIO from the application processor because of the reset sequence. Hence this TI design used two dedicated GPIO port from the application processor to control the RESET signal of the two PHYs. Each GPIO is combined with a SN74LVC1G08 AND gate of the PORZ signal from the PMIC to enable a common system reset. In case only a single GPIO signals is available from the processor, then the designer can choose to use the PORZ signal for the first PHY only and only reset the second PHY with a combination of GPIO and PORZ signal.

When selecting another GPIO for controlling the RESET signal, please choose them with low after the processor power on reset to keep the PHYs in reset state until the power supply has been enabled.

2.4.5 DP83867 and AM5728 Bootstrap Consideration for Mid-Voltage Levels

The DP83867IR is configured through bootstrap mode during power-on-reset. At power-on-reset the DP83867IR latches a user defined voltage level at a set of dedicated bootstrap input pins. The DP83867IR supports 4 voltage levels for bootstrap configuration. With each of the voltage level a dedicated configuration mode is set, for example, full-duplex or half-duplex operation mode, configuration of the MDIO address and others. The voltage levels detected by the DP83867IR are 0 V (Mode 1), 1.4 V (Mode 2), 2.4 V (Mode 3) and 3.3 V (Mode 4). Especially 1.4 V (Mode 2) and 2.4 V (Mode 3) are referred as mid-voltage level in the following description.

The AM5728 processor has a constrain with exposed to mid-voltage levels, which has an effect o the power-on-hour (POH) lifetime. The AM5728 exposure to mid-voltage levels time should be avoided and the voltage level have to be kept either above Vhmin or below Vlmax as specified in the *AM572x Sitara™ Processors Silicon Revision 2.0* data sheet.

Typically the mid-voltage levels are present in the system during power up of the devices. Because the AM5728 has configured many of its pads as input after system reset, the AM5728 is exposed to the mid-voltage levels before the bootloader and application reconfigure those pins in the correct operation mode.

This TI design uses only Mode 1 or Mode 4 as bootstrap configuration modes for the DP83867IR PHY to avoid mid-voltage levels. One of the bootstrap configurations is configure individual MDIO addresses for each PHY. All remaining PHY configuration is performed over MDIO access once the PHY is released out of reset. Using this approach eliminates the need for additional buffers to isolate the AM5728 pads from the DP83867 pads to avoid mid-voltage levels.

In case the system design requires mid-voltage level, the use of buffers is required which isolates the mid-voltage level for the DP83867IR bootstrapping to be seen AM5728 pad. Please refer to TIDA-00299 on how the buffers can be added to the system design.

The DP83867IR PHY register configuration over MDIO interface is part of this TI Design.

2.4.6 Reduced Gigabit Media Independent Interface (RGMII)

The DP83867IR has integrated termination resistors in the RXD data lines, which are RX_D0, RX_D1, RX_D2, RX_D3, RX_CLK and RX_CTRL. Therefore there are no external line driver resistors needed to be added on the PCB between the DP83867IR and the AM5728. The DP83867IR has control registers to adjust the drive strength of the RXD data lines to control the voltage slope for voltage under- and overshoot.

The TXD data lines, which are TX_D0, TX_D1, TX_D2, TX_D3, TX_CLK and TX_CTRL have line driver resistors of 22 Ω added between the DP83867IR and the AM5728.

During the trace length have of the RXD as well as the TXD have to be matched. For more details, see the *DP83867IR Robust, Low Power 10/100/1000 Ethernet Physical Layer Transceiver* data sheet and TI Design TIDA-00204.

The line driver resistors in the TXD path have to get placed as close as possible to the AM5728 pins to be effective.

2.4.7 Media Dependent Interface (MDI)

The MDI interface is connects the DP83867IR to the transformer and the RJ45 connector. There is no need to place external termination resistors for the MDI interface as the he MDI interface of the DP83867IR has integrated termination resistors. The magnetic can be placed separately or they can be integrated into the RJ45 connector.

There are a variety of RJ45 connector with integrated magnetic. Typically the integrated magnetic can have a variety of configurations of resistor and capacitor connects. It is important to select the magnetic according , hence make sure to select a magnetic that follows the DP83867IR data sheet recommendations.

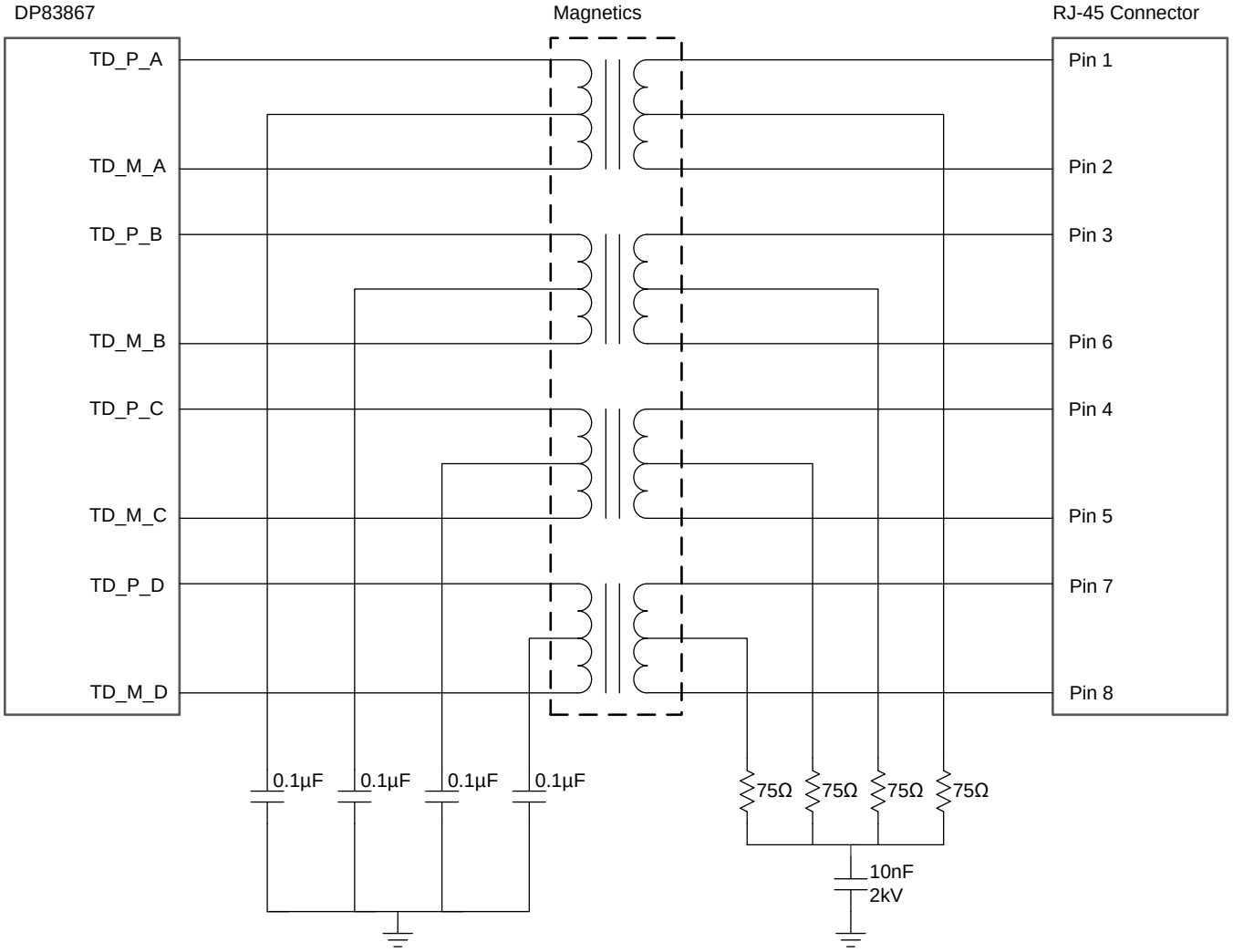


図 6. Magnetics Connections

There are solutions with the transformer integrated into the RJ45 connector as well as separate transformer and RJ45 connectors. This TI design uses an integrated transformer into the RJ45 connector. The TIDA-00204 shows an example of separate transformers. Use a length matching of each MDI pair as well as to the pairs itself.

Specific care has to be taken when routing the traces of the MDI lines and signal pairs. They PCB traces must be length matched.

Lastly, ESD protection devices TPD1E05U06 are added between the DP83867IR and transformer to prevent ESD strikes to reach the DP83867IR device.

2.4.8 RJ45 Port With Integrated Magnetic and Status LEDs

The magnetic on the MDI interface between the DP83867IR and the RJ45 port can either be external (they need to be placed on the PCB between the DP83867IR and the RJ45 connector) or they can be integrated into the RJ45 connector. Similar options are available for the status LEDs, and it is up to the system requirements to choose the appropriate solution. The benefits of external magnetic and status LEDs are a higher immunity against EMI.

This TI design used integrated magnetic and status LEDs. For a TI design reference with external magnetic please refer toTIDA-00204.

2.5 Gigabit Ethernet Solution Comparison

This section compares the TI DP83867IR solution against the KSZ9031 solution.

表 2. Comparison of the DP83867IR and KSZ9031 Solutions

FUNCTION	DP83867IR	KSZ9031	COMMENT
Voltages	3.3 V, 2.5 V, 1.0 V	3.3 V, 1.2 V	2 × DP83867IR
Voltage generation	PMIC, DC/DC	DC/DC, LDO (FDT434P), inductor	LDO is not power efficient and uses bigger board space
RGMII TX termination resistors	Integrated	External termination resistors	External resistors require more board space
Power consumption	467 mW	621 mW	LDO losses of KSZ9031 are not part of the calculation
Clock generation	Single XTAL	Two 25-MHz crystals	Two crystals require more board space
MDI Interface	Integrated ESD protection	NA	-
PHY boot strapping	Minimum bootstrapping required	Y	-

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

The following hardware components are required to validate the Ethernet functionality

- TIDA-010010 - AM5728 EVM with two DP83867IR Ethernet PHYs
- Multi-meter
- Oscilloscope
- Windows PC with two Gbit Ethernet ports
- Ethernet cables CAT5e or better quality to support 1000 Mbps Ethernet

3.1.2 Software

The following software components are required to validate the Ethernet functionality

- Code Composer Studio 7.4 or higher
- Processor SDK RTOS for AM572x
- Ethernet packet sniffer (for example, Wireshark)
- Ethernet packet generator (for example, Colasoft Packet Builder 2.0)
- Test application project *EMAC_DP83867_evmAM572x*

3.1.2.1 Power Supply for DP83867IR

The DP83867IR requires 3 voltages: 3.3 V, 2.5 V and 1.0 V. The 3.3-V voltage is generated by the DC/DC converter TPS54531D after board power is enabled by TPS6590378 PMIC. The 2.5 V and 1.0 V voltages are generated by the TPS6590378 PMIC through the integrated DC/DC converters SMPS7 (2.5 V) and SMPS9 (1.0 V). The SMPS7 and SMPS9 rails need to get configured and enabled by the application software.

The TPS6590378 PMIC is programmed over the I2C interface. The Processor SDK RTOS provides a chip support library (CSL) to read and write from the PMIC device over the I2C interface.

The function *dp83867_pmic_init()* in file phy_init.c configure and enable the 2.5-V and 1.0-V voltages output in the PMIC.

```
void dp83867_pmic_init(void)
{
    const pmhalPmicOperations_t *pmicOps;
    uint32_t    retVal;

    /* Register the I2C functions with the PMIC Communication to ensure the
     * PMIC can be communicated with I2C driver
     */
    PMHALI2CCommRegister(&gPmicI2cfunc);
    pmicOps = PMHALTps659037GetPMICOps();
    retVal = PMHALPmicRegister(pmicOps);
    if(retVal != 0)
        return;

    /* enable the PHY voltage supplies */

PMHALPmicSetRegulatorVoltage(PMHAL_PRCM_PMIC_REGULATOR_EPHY2V5,2500,PM_TIMEOUT_INFINITE,FALSE);
```

```
PMHALPmicSetRegulatorVoltage(PMHAL_PRCM_PMIC_REGULATOR_EPHY1V0,1000,PM_TIMEOUT_INFINITE,FALSE);
    PMHALPmicEnableRegulator(PMHAL_PRCM_PMIC_REGULATOR_EPHY2V5);
    PMHALPmicEnableRegulator(PMHAL_PRCM_PMIC_REGULATOR_EPHY1V0);
}
```

3.1.2.2 DP83867IR Reset Sequence

The two DP83867IR requires a reset sequence as described here

The application software controls the signals GPIO5_17 and GPIO3_29 to perform the RESET sequence for the two DP83867IR. The application software first sets both GPIOs to '0' to set both DP83867IR into RESET state. After 1µs the application software releases the RESET for the first DP83867IR. It takes approximately 200 ms (worst case) for the first PHY to output the 25-MHz clock on its CLK_OUT pin. After this wait time the application software releases the RESET signal of the second DP83867IR.

The function *dp83867_reset_sequence()* in file phy_init.c performs the reset sequence as previously described.

```
void dp83867_reset_sequence(void)
{
    uint32_t regVal = 0;
    /* configure GPIOs as outputs*/

    /* pinmux */
    /* AM572x EVM GPIO5_17 RESET PHY1 */
    CSL_FINS(regVal, CONTROL_CORE_PAD_IO_PAD_RMII_MHZ_50_CLK_RMII_MHZ_50_CLK_MUXMODE, 0xEU);
    ((CSL_padRegsOvly) CSL_MPU_CORE_PAD_IO_REGISTERS_REGS)->PAD_RMII_MHZ_50_CLK = regVal;

    /* AM572x EVM GPIO3_29 RESET PHY2 */
    CSL_FINS(regVal, CONTROL_CORE_PAD_IO_PAD_VIN2A_DE0_VIN2A_DE0_MUXMODE, 0xEU);
    ((CSL_padRegsOvly) CSL_MPU_CORE_PAD_IO_REGISTERS_REGS)->PAD_VIN2A_DE0 = regVal;

    /* configure GPIO */
    GPIO_init();

    /* Reset sequence: 1us reset asserted; then first PHY needs to wait for 201 ms before second
PHY comes out of reset */
    GPIO_write(0, 0);   /* set GPIO5_17 to low */
    GPIO_write(1, 0);   /* set GPIO3_29 to low */
    delay(1);        /* wait 8 us*/
    GPIO_write(0, 1);   /* set GPIO5_17 to high */
    delay(201*125);       /* wait 201 ms */
    GPIO_write(1, 1);   /* set GPIO3_29 to high */
}
```

3.1.2.3 DP83867IR Configuration Over MDIO

The TI design applies only a minimum bootstrap resistors to configure the DP83867IR. All additional register configuration is performed over the MDIO interface by the application software.

The initial DP83867IR register configuration is performed by function ENETPHY_Init() in file enet_phy.c.

```
int32_t ENETPHY_Init(ENETPHY_Handle hPhyDev, uint32_t miibase, uint32_t inst, uint32_t PhyMask,
uint32_t MLinkMask, uint32_t MdixMask, uint32_t PhyAddr, uint32_t ResetBit, uint32_t MdioBusFreq,
uint32_t MdioClockFreq,int32_t verbose)
{
  uint32_t *PhyState = &((ENETPHY_DEVICE *) hPhyDev)->PhyState;

  int32_t  ret =0 ;
  uint32_t phy;

  ((ENETPHY_DEVICE *) hPhyDev)->miibase   = miibase;
  ((ENETPHY_DEVICE *) hPhyDev)->inst      = inst;
```

```
  ((ENETPHY_DEVICE *) hPhyDev)->PhyMask   = PhyMask;
  ((ENETPHY_DEVICE *) hPhyDev)->MLinkMask = MLinkMask;
  ((ENETPHY_DEVICE *) hPhyDev)->MdixMask  = MdixMask;

   *PhyState &= ~ENETPHY_MDIX_MASK;   /* Set initial State to MDI */

  CSL_MDIO_setClkDivVal((CSL_mdioHandle) ((ENETPHY_DEVICE *) hPhyDev)-
>miibase, (MdioBusFreq/MdioClockFreq - 1));
  CSL_MDIO_enableFaultDetect((CSL_mdioHandle) ((ENETPHY_DEVICE *) hPhyDev)->miibase);
  CSL_MDIO_disablePreamble((CSL_mdioHandle) ((ENETPHY_DEVICE *) hPhyDev)->miibase);
  CSL_MDIO_enableStateMachine((CSL_mdioHandle) ((ENETPHY_DEVICE *) hPhyDev)->miibase);

  ENETPHY_UserAccessRead(hPhyDev, ENETPHY_BMCR, PhyAddr, &phy);
  phy |= DP_AUTO_NEGOTIATION_ENABLE | DP_DUPLEX_MODE;
  ENETPHY_UserAccessWrite(hPhyDev, ENETPHY_BMCR,PhyAddr,phy);
  ENETPHY_UserAccessRead(hPhyDev, ENETPHY_ANAR, PhyAddr, &phy);
  phy |= DP_TX_FD | DP_TX | DP_10_FD | DP_10BASETE_EN;
  ENETPHY_UserAccessWrite(hPhyDev, ENETPHY_ANAR,PhyAddr,phy);
  ENETPHY_UserAccessRead(hPhyDev, ENETPHY_CFG1, PhyAddr, &phy);
  phy |= DP_1000BASE_T_FULL_DUPLEX | DP_1000BASE_T_HALF_DUPLEX;
  ENETPHY_UserAccessWrite(hPhyDev, ENETPHY_CFG1,PhyAddr,phy);

  /* disable clock out of second PHY */
  if(PhyAddr != 0)
  {
      ENETPHY_UserAccessRead(hPhyDev, ENETPHY_IO_MUX_CFG, PhyAddr, &phy);
      phy &= ~(DP_CLK_O_DISABLE);
      ENETPHY_UserAccessWrite(hPhyDev, ENETPHY_IO_MUX_CFG,PhyAddr,phy);
  }

  /* set RGMII Delay Control Register TX Delay) */
  ENETPHY_UserAccessRead(hPhyDev, ENETPHY_RGMIIDCTL, PhyAddr, &phy);
  phy &= ~(0xF<<4);
  phy |= 0x3<<4;        /* set RGMII_TX_DELAY_CTRL to 1.00 ns */
  ENETPHY_UserAccessWrite(hPhyDev, ENETPHY_RGMIIDCTL, PhyAddr, phy);
     (void)ResetBit; /* suppress warning */

     *PhyState=INIT;

  return ret;
}/* end of function ENETPHY_Init*/
```

3.1.3 2 Gigabit Ethernet (GMAC) Peripheral

The GMAC is a peripheral inside the AM5728 application processor. It is a 2-port switch with two physical ports connector to the two DP83867IR Ethernet PHYs and one internal host port. The host port is named P0 and the two physical ports are named P1 and P2. When the application software sends a broadcast Ethernet frame into the GMAC via port P0, the GMAC will send out this broadcast Ethernet frame both ports, P1 and P2. Similar to when a broadcast frame is either received from port P1 or P2, the GMAC will send it out on P0 and P2 or P1. Please refer to the AM5728 technical reference manual (TRM) for additional information about the GMAC peripheral.

The application software configures the GMAC through the CSL library. The GMAC example with DP83867OIR is based on the example project *EMAC_BasicExample_evmAM572x_armBiosExampleProject* from the Processor SDK RTOS. The example demonstrates how to receive and transmit Ethernet frames without any TCP/IP stack and is best suited for DP83867IR and AM5728 solution validation.

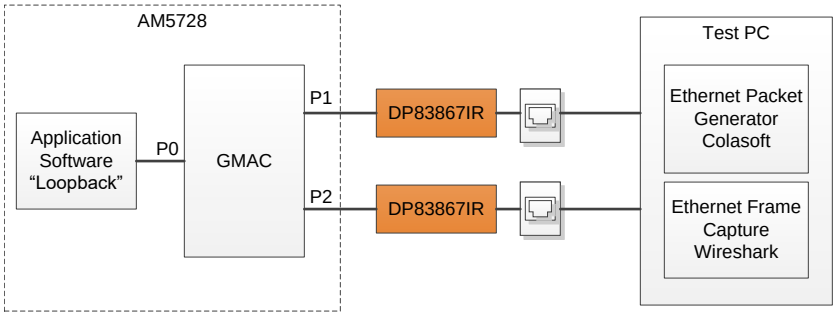
3.2 Testing and Results

The testing of this design focuses on receiving and transmitting of Ethernet frames. The test PC transmits broadcast Ethernet frame to Ethernet Port P1 (or P2). Each broadcast frame is transmitted by the GMAC to P0 and P2 (or P1). The application software send any received Ethernet frame back to P0 (Ethernet application loopback). Each frame transmitted from the test PC is received twice on both Ethernet Ports P1 and P2 and once at the host port P0. For validation the test PC sends out a known number of broadcast frames. The reception is confirmed by the Ethernet Tools Wireshark on the PC and with the RX/TX statistics in the GMAC peripheral.

3.2.1 Test Setup

図 7 shows the test setup.

図 7. Test Setup

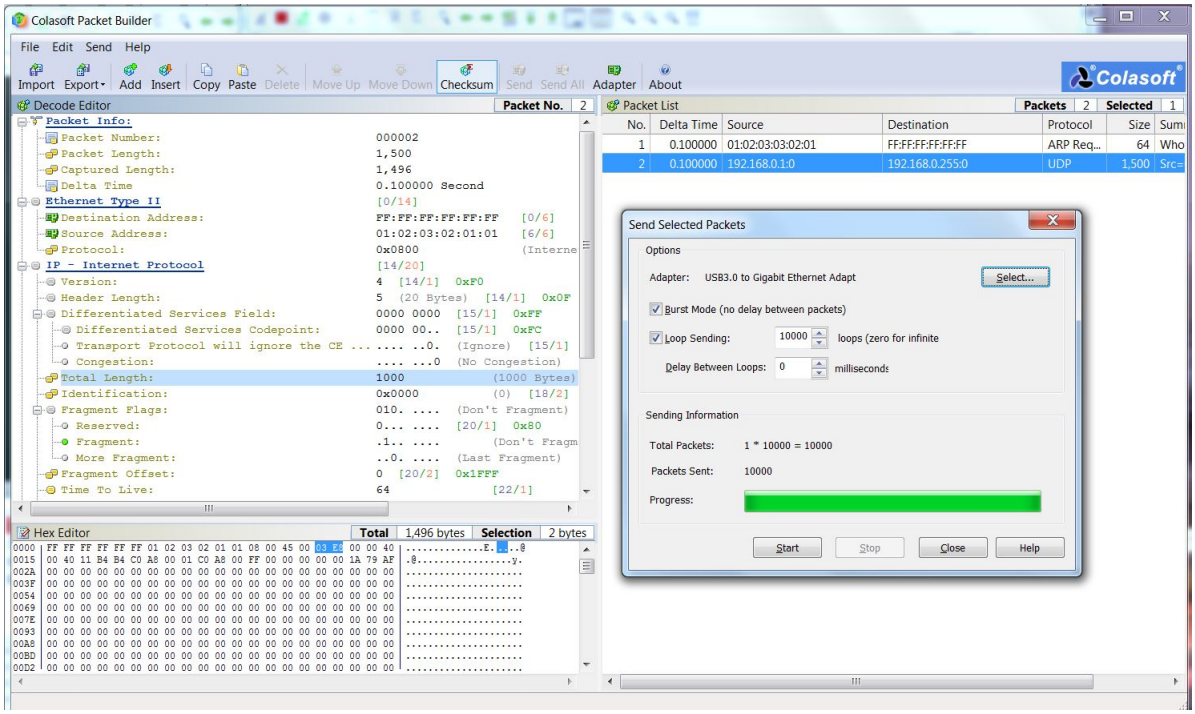


3.2.2 Test Results

3.2.2.1 Ethernet Frame Generation

The Ethernet frame generator on the test PC 1 generates 10,000 Ethernet frames (size 1500 bytes). 図 8 shows the configuration.

図 8. Colasoft® Packet Builder GUI - Configuration



3.2.2.1.1 GMAC Statistics Registers

図 9 shows the RX statistics. The GMAC statistics shows that it received 10,000 (0x2710 hex) good frames.

図 9. GMAC RX Statistics

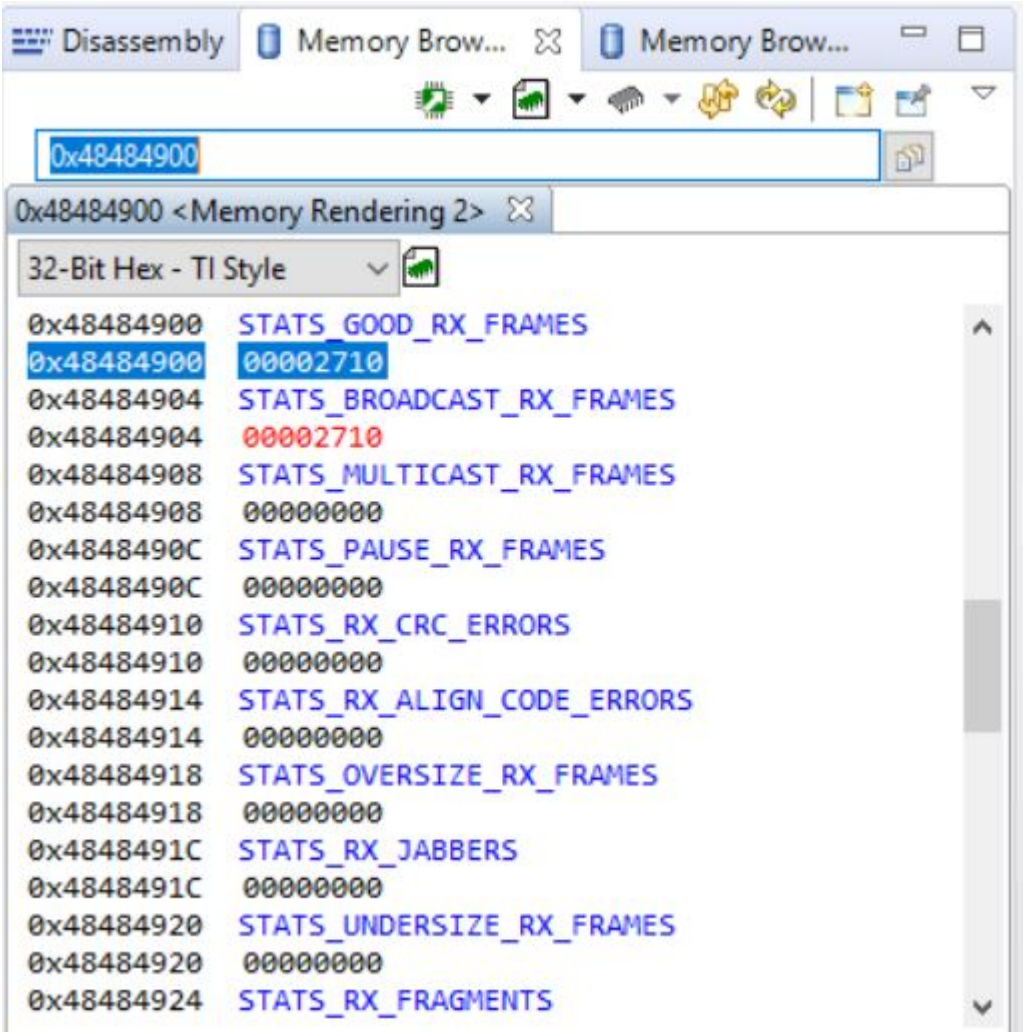
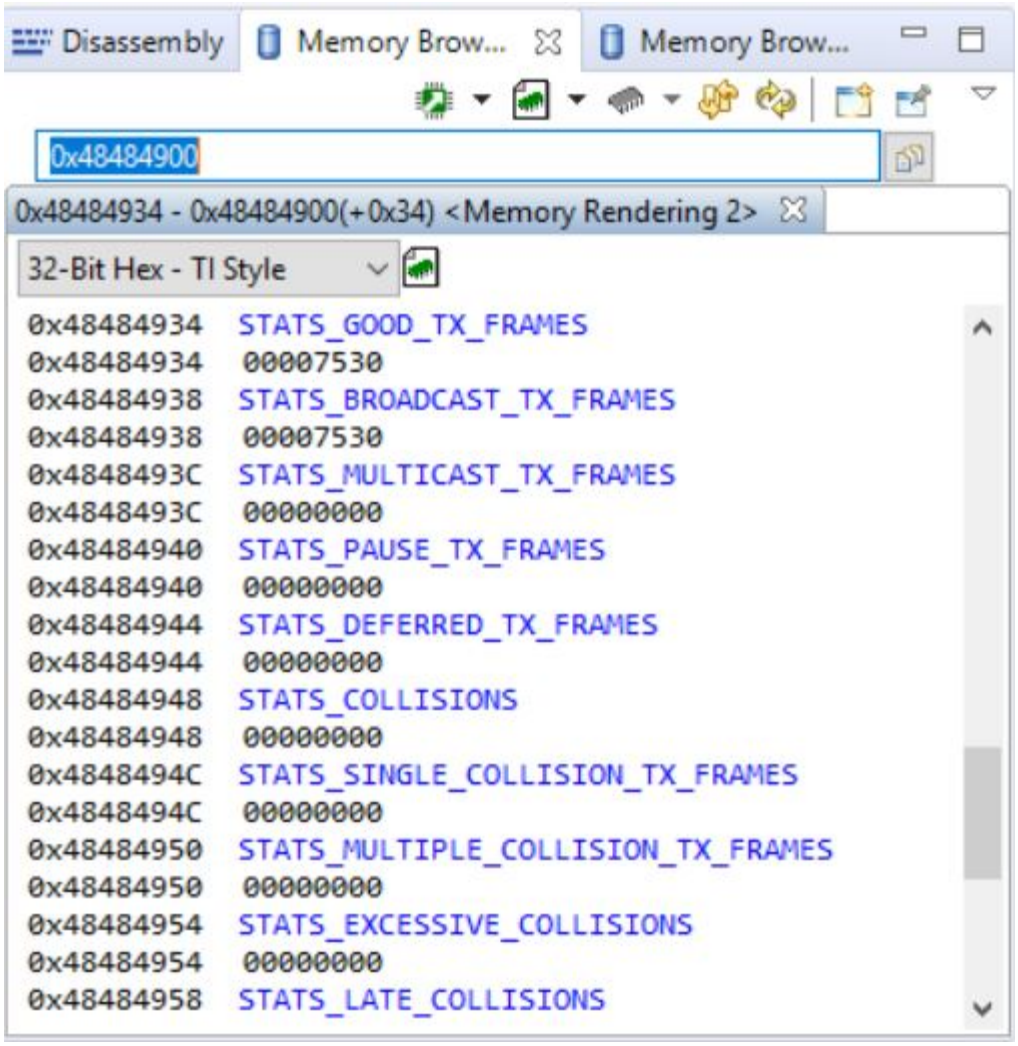


図 10 shows the TX statistics. The GMAC statistics shows that it transmitted 30,000 (0x7530 hex) good frames. This amount splits up in port P2 transmitting the frames received from the test PC at port P1, and port P1 and P2 transmitting the loopback frames from the application software on P0.

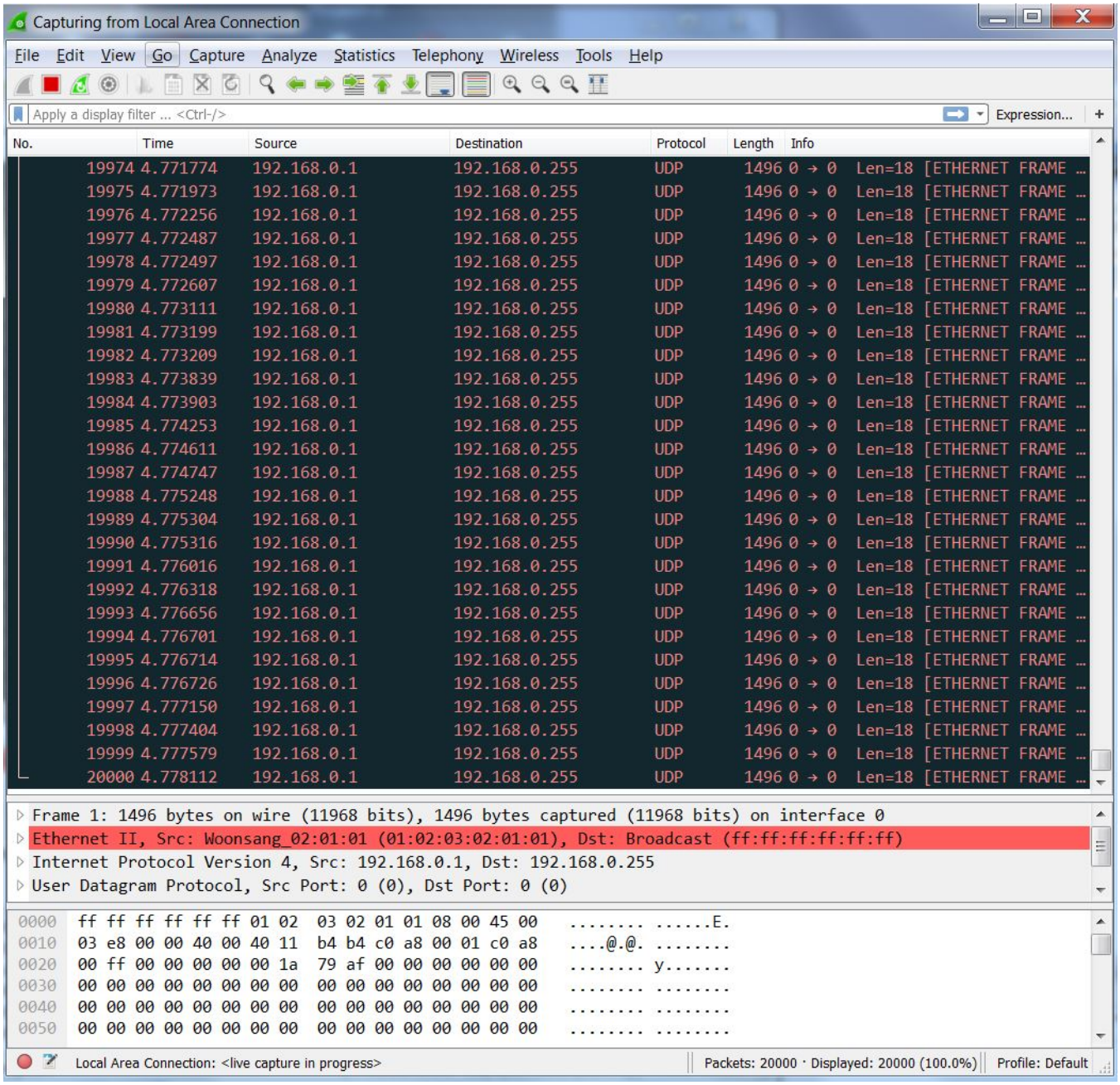
図 10. GMAC RX Statistics



3.2.2.2 Test PC Received Frames

図 11 shows the Ethernet frame captured on one Ethernet port of a total of 20,000 Ethernet frames.

図 11. Ethernet Frame Capture Example



4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-010010.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-010010.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-010010.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-010010.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-010010.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-010010.

5 Software Files

To download the software files, see the design files at TIDA-010010.

6 Related Documentation

1. Texas Instruments, *DP83867 Troubleshooting Guide Application Reports*
2. Texas Instruments, *AM572x Sitara Processors Silicon Revision 2.0, 1.1 Technical Reference Manual*

6.1 商標

7 Terminology

GMAC— 2-port gigabit Ethernet

PHY— Ethernet Physical Transceiver

MAC— Media Access Controller

RGMII— Reduced gigabit Media Independent Interface

MDI— Media Dependent Interface

EVM— Evaluation Module

BOM— Bill of Material

RTOS— Real-time Operating System

HLOS— High-level Operating System

OS— Operating System

CSL— Chip Support Library

8 About the Author

Thomas Mauer is a System Engineer in the Factory Automation and Control Team at Texas Instruments Freising. He is responsible for developing reference design solutions for the industrial segment. Thomas brings his extensive experience in industrial communications like Industrial Ethernet and fieldbuses and industrial applications to this role. Thomas earned his degree in Electrical Engineering (Dipl. Ing. (FH)) at the University of Applied Sciences in Wiesbaden, Germany.

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