参考資料

デザイン・ガイド：TIDA-01027
12.8GSPS データ・アクイジション・システムの性能を最大化する低ノイズ電源のリファレンス・デザイン

TEXAS INSTRUMENTS

概要

数 GSPS クラスの高速データ・アクイジション (DAQ) を必要とするアプリケーションには、ネイティブのアナログ・フロント・エンド (AFE) 信号チェーンの性能を維持できる、効率的で低ノイズのポイント・オブ・ロード (PoL) 電源設計を含める必要があります。AFE 電源には多くの場合、メイン・バスから電力を供給される複数の電源レールが含まれます。複数のフリーランニング DC/DC コンバータが生成する周波数成分は、伝導と放射の両方のノイズを発生し、信号チェーンの性能に悪影響を及ぼす可能性があるため、電源設計ではすべての信号チェーンの影響を最小限に抑えることが最も重要です。このリファレンス・デザインでは、12.8GSPS を超える超高速 DAQ システム用の、効率的で低ノイズな 5 レールの電源の設計を示します。入力電流リップルを最小化し、周波数成分を制御するために、電源の DC/DC コンバータは周波数同期および位相シフトされます。さらに、TI の高性能 *HotRod™* パッケージング・テクノロジを使用することで、放射電磁妨害 (EMI) も最小限に抑えています。

リソース

TIDA-01027、TIDA-01022	デザイン・フォルダ
TPSM84424、LMZM23601	プロダクト・フォルダ
CD74HC4017	プロダクト・フォルダ
TPS7A84、TPS7A8300、TPS7A33、TPS7A49	プロダクト・フォルダ
TSW14J57EVM、TSW14J56EVM	ツール・フォルダ

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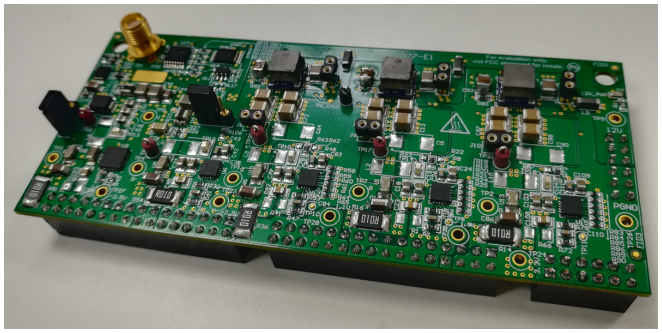
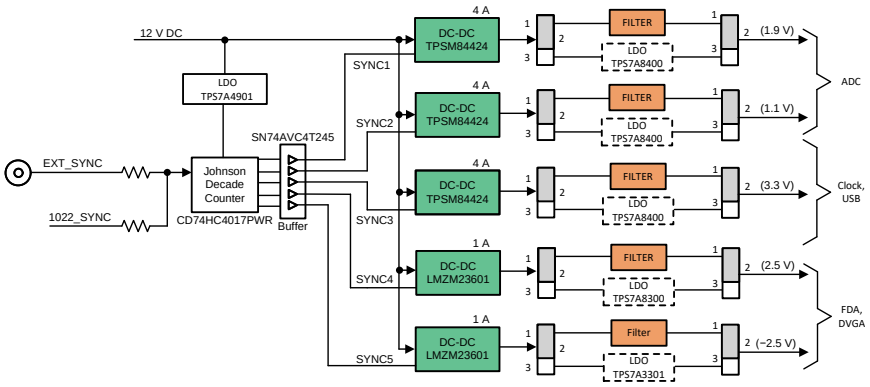
特長

- 超高速 AFE 用の、効率的で低ノイズなポイント・オブ・ロード DAQ 電源
- 位相シフトした DC/DC コンバータ・クロックにより、突入電流と電源ノイズを低減
- 外部周波数同期により DC/DC コンバータのスプリアスを管理
- 出力の構成により、各 LDO をバイパスし、DC/DC コンバータとフィルタのみを使用可能
- TIDA-01022 および TIDA-01028 とともに使用し、9GHz のアナログ帯域幅を持つ 12.8GSPS AFE への影響を実証

アプリケーション

- 高速 DAQ (DAQ)
- 高性能オシロスコープ (DSO)
- ワイヤレス通信のテスト機器(WCTE)
- レーダー、非軍事用地上モバイル無線





1 System Description

Multichannel, high-speed, GSPS data acquisition (DAQ) applications such as a digital storage oscilloscope (DSO), phased-array radio detection and ranging (RADAR), multiple-input multiple-output (MIMO) wireless communication, and wireless communication tester equipment (WCTE) all require accurate phase-coherency between channels to effectively direct multi-antenna systems and for accurate data reconstruction. These complex, high-tech systems, illustrated in 図 1, 図 2, and 図 3, consist of high-speed AFE, clocking, point-of-load (PoL) power, and calibration subsystems. This reference design focuses on the PoL power design of the AFE, highlighted in blue, and how to maximize efficiency and minimize any impact on the raw signal chain performance.

図 1. High-Performance DSO AFE Subsystem

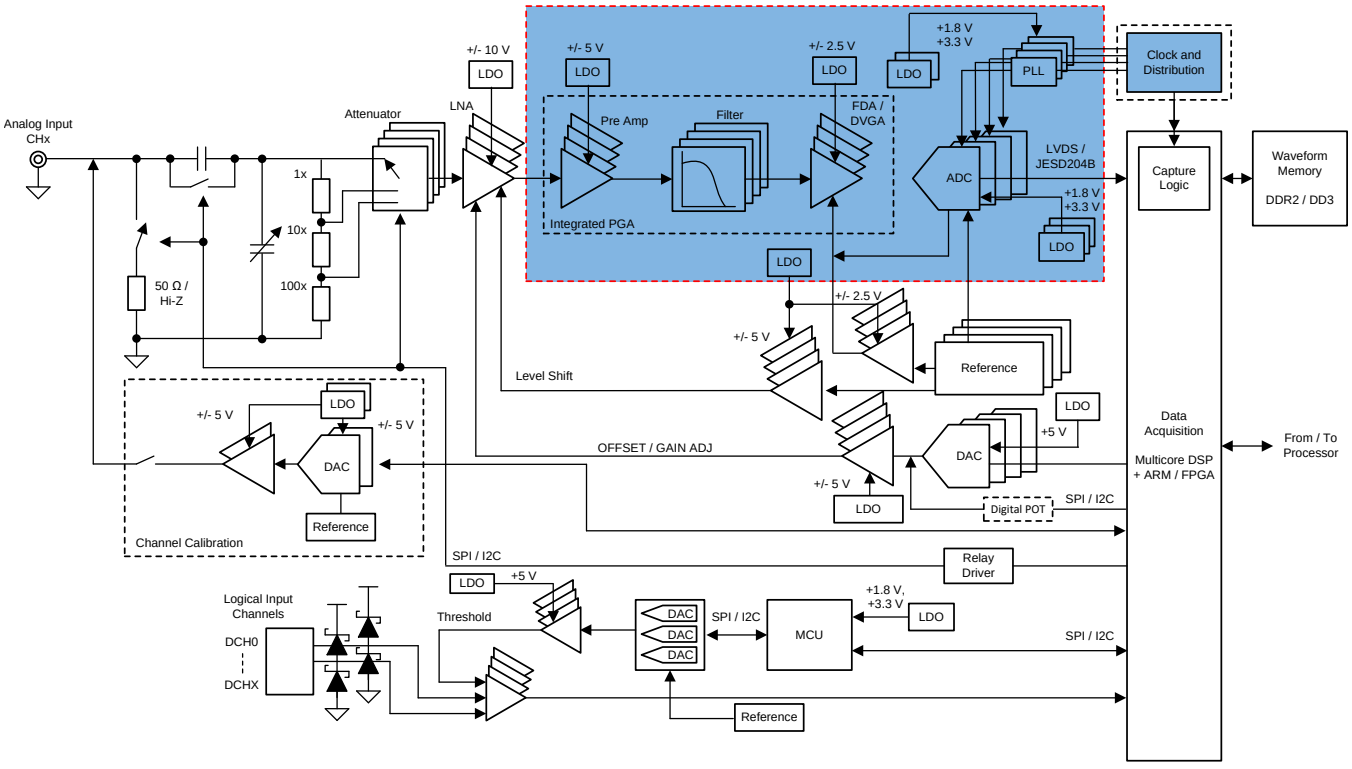


図 2. RADAR, RF Subsystem

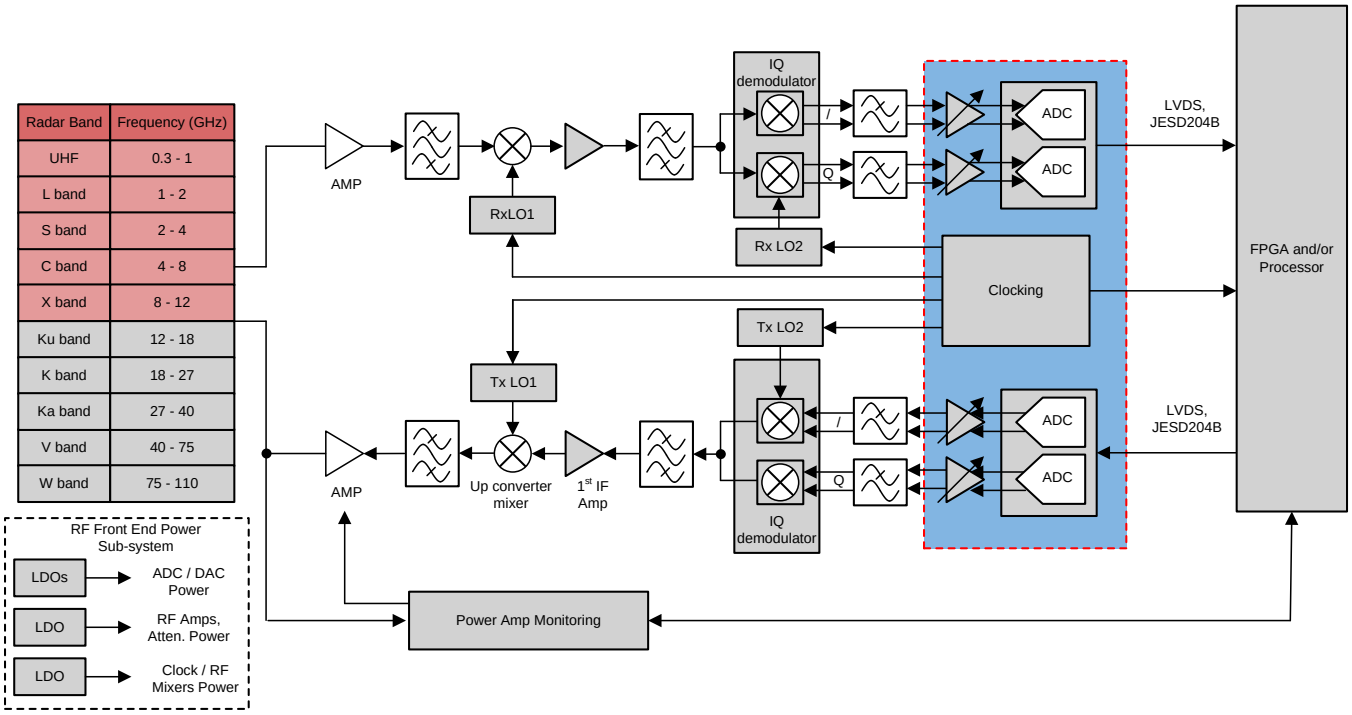
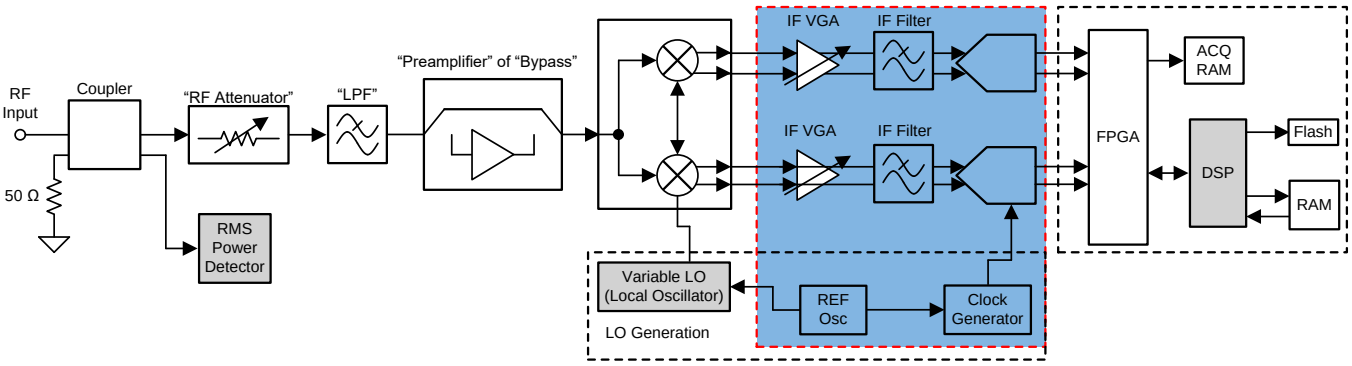


図 3. Wireless Communication Test Equipment AFE Subsystem



1.1 Key System Specifications

表 1. Key System Specifications(1)

PARAMETER	SPECIFICATIONS	DETAILS
Input voltage range	5 V to 17 V	2.2.3.1
Total number of outputs	5	2.1
Output voltage, maximum output current	+1.9 V - 4 A, +1.1 - 4 A, +3.3 V - 4 A, +2.5 V - 1000 mA, –2.5 V - 800 mA (at 12-V input)	2.2.3.1
Efficiency	> 85% (DC/DC + Filter at 12-V input)	3.2.2.3
External frequency synchronization DC/DC	750 kHz at 12-V input, 700 kHz to 1300 kHz at 5-V input	
Connectors	2.54-mm header and compatible with TIDA-01022 hardware	3.1.1
Form factor	107 mm × 25 mm (only DC/DC converters), 117.5 mm × 51 mm (PCB form factor)	3.1.1

(1) See *Testing and Results* (3.2) for more details.

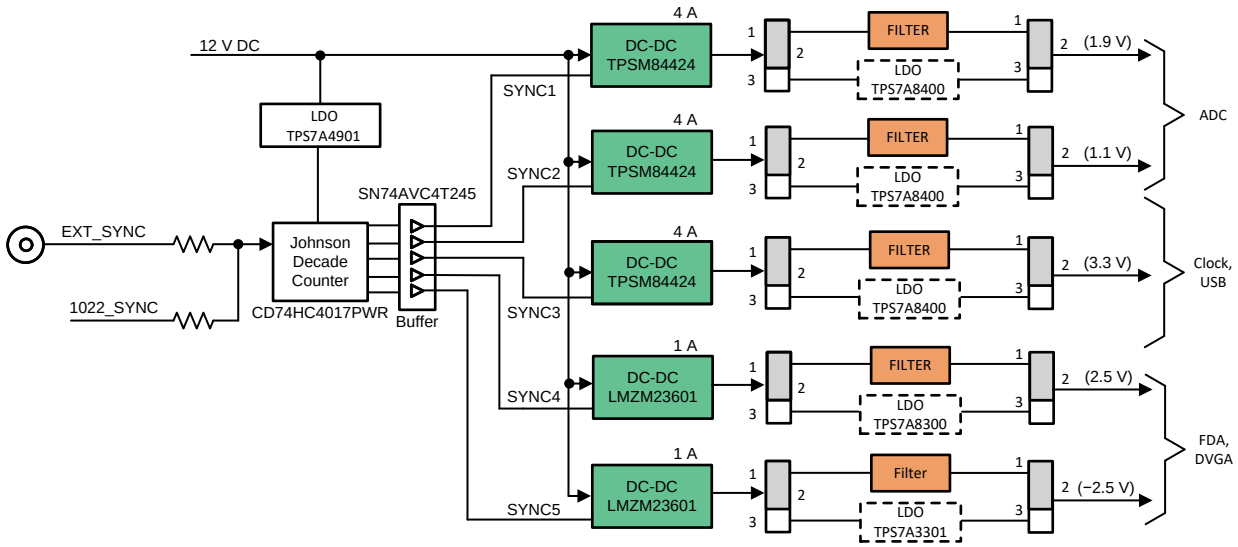
2 System Design Overview

By their very nature, these multichannel, high-precision applications require multiple (2 to > 1000) signal chains which demand both power and PCB-efficient design. The power demands and increased board density add the additional design challenge that the power supply components can interfere directly by either conductive or radiated energy, degrading the system's total effective number of bits (ENOB). Therefore, it is important the PoL power supply design be optimized for efficiency and noise. In this reference design we first consider power tree optimization for both supply and PCB efficiency. Next, we closely choose the DC/DC converters that will optimize efficiency for the given load, in this example, the TIDA-01022, TIDA-01028, 1–4 channel, 12 bit up to 12.8 GSPS AFE. As part of our converter selection, products that are known to limit EMI radiation are used. Finally, we consider the LDO efficiency and what impact, if any, it will have on the system ENOB if removed.

2.1 Block Diagram

図 4 shows the simplified block diagram of this design. A 12-V input supply is bucked down to supply 5 separate AFE supplies using TI's efficient DC/DC converter modules. These supplies are used to power the FDA, DVGA, ADC, and clock, USB components of the AFE. Each converter output can be buffered by a low-noise LDO to help filter any supply ripple and noise within the bandwidth of the LDO. The LDO can be bypassed to measure the signal chain impact and efficiency improvement. To reduce inrush current, a Johnson counter is used to generate multi-phase, frequency synced clocks for the DC/DC converters. This not only reduces the amplitude, but also increases the effective beat frequency by the number of phases generated by the counter.

図 4. TIDA-01027 Block Diagram



2.2 Design Considerations

This section describes different design challenges and their impact on the system performance. Noise-reduction methods and their implementation is also discussed in this section.

2.2.1 Design Challenges

Efficiency and Thermal Performance: A low-dropout regulator (LDO) between the switching regulator and the ADC is used to clean up the output noise and the switching-frequency spurs. However, this clean power-supply design comes at the expense of additional power consumption because the LDO requires headroom for the dropout voltage in order to function properly. Therefore, eliminating the low-noise LDO from this chain can bring significant power savings and also reduce the board space, heat, and cost of the design.

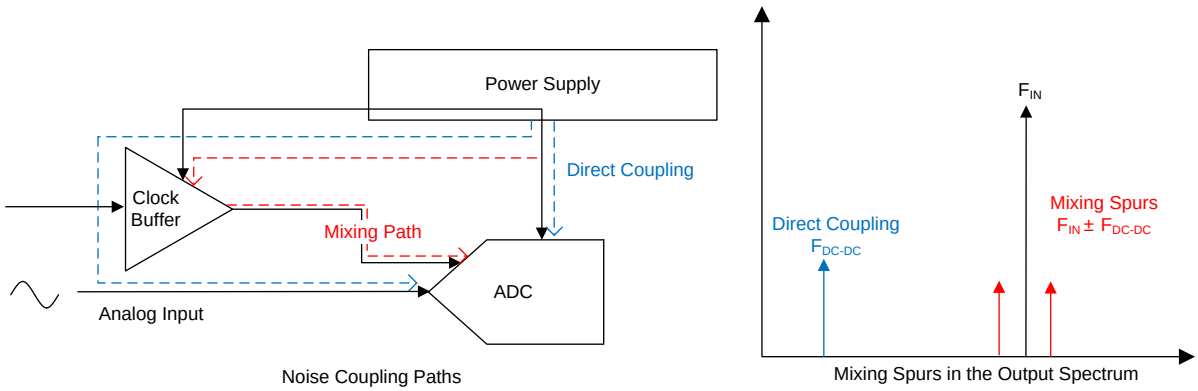
Power Supply Noise Sources:

1. Switching Noise: DC/DCs are the source for this noise
2. Electromagnetic Interference(EMI): EMI is mainly categorized into two types, Conducted EMI and Radiated EMI.
   a. Conducted EMI: Common impedance coupling and parasitic are major contributing sources
   b. Radiated EMI: The main source is external high-frequency signals, but the effect of dI/dt and ringing nodes of the power supply may be significant
3. Thermal, Flicker Noise: DC/DC and LDO are source of this noise

Impact of Noise:

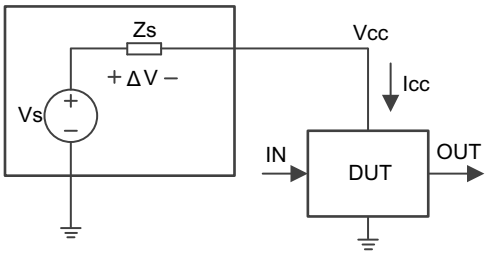
1. Impact noise in high-speed ADCs: Noise at the output power supply degrades performance of ADC (NSD, ENOB, and SFDR), as it directly couples to the ADC input path or to the clock path that generates spurs near to the input signal frequency. 図 5 shows coupling paths of switching noise and its effect on the ADC output spectrum. For more information, see the *Designing a modern power supply for RF sampling converters analog application journal*.

図 5. Power Supply Noise Coupling Paths and its Effect on the ADC Output Spectrum



2. Impact of noise in clock generators: Noise floor and phase noise at the output of the clock generator is mainly affected due to two reasons:
   a. The change in the current demand of the clock generators: 図 6 shows a simple setup with a clock generator and supply. As I_{CC} changes, and the drop across Z_S changes (that is, ΔV) this translates to changes in the supply V_{CC} and is added as noise to the clock generator.

図 6. Simple Setup With Clock Generator and Supply



b. LDO output noise: The LDO output is regulated with respect to the LDO band gap reference. Any noise on the band gap is translated at the LDO output that contributes to phase noise and increases noise floor of the system.

For more information, see the *Supply noise effect on oscillator phase noise application report*.

3. Impact of noise in high-speed systems:
   a. Digitizers, high-speed DAQ, oscilloscopes: ENOB is used to evaluate the performance of digitizers. It summarizes noise and frequency response of a system. As it decreases, it makes timing measurement less accurate and decreases measurement precision.
   b. RADAR, SDR: Instead of the traditional ADC specifications(SNR, SFDR and ENOB), intermodulation distortion (IMD) and noise floor are used to evaluate the performance of RADARs. Noise increases intermodulation distortion and noise floor of the system that reduces maximum range and receiver sensitivity.

2.2.2 How to Mitigate Noise in High-Speed Systems

表 2. Noise-Mitigating Options

NOISE REDUCTION OPTIONS	REDUCES SWITCHING NOISE	REDUCES EMI	DEVICE FEATURE	DESIGN OPTION	IMPLEMENTED ON THIS DESIGN	DESIGN THEORY
Spread Spectrum frequency modulation (SSFM)		✓	✓		x	
Clock synchronization pin	✓		✓		✓	2.2.3.4
TI HotRod™ or (FCOL QFN)		✓	✓		✓	
Integrated inductor power module		✓	✓		✓	
Slew rate control		✓	✓		x	
Pin optimization: Symmetric (butterfly) pinout		✓	✓		✓	
Slew rate control (RC snubber)		✓		x	x	
Phase control	✓	✓		✓	✓	2.2.3.4
Filtering: Discrete filter	✓			✓	✓	2.2.3.3.1
Filtering: LDO	✓			✓	✓	2.2.3.3.2

See 3.2.2.1 for the results after implementation of previously listed noise-reduction methods.

表 2 shows different device and system noise mitigation options. The following explains mitigation options mentioned in the table and how they are implemented.

1. Device features:
   a. Frequency and Phase control
      i. *Spread Spectrum frequency modulation* (SSFM): This method varies switching frequency of converters, typically ±10%. The improvement in EMI is achieved by not allowing radiated energy to stay in the interested bandwidth for a significant length of time. To implement SSFM, the device should have the capability to track frequency change with regard to time. SSFM may improve EMI, but it is not a substitute for standard layout, filter, and shielding practices. For more information, see the *EE Times* article: *Frequency spreading provides switching-supply EMI insurance*.

ii. Multiple Phase synchronization: This method applies to systems using two or more converters and is achieved by externally supplying phase-shifted synchronized clocks to converters. The result is less noise, as the converters are running at different time intervals in a switching cycle. It also reduces the beating effect of converters, inrush current, and input-output capacitors size. The device should have an external synchronization feature to implement this method. For more information, see the *EE Times* article: *Synchronizing Makes for Well-Behaved Power Supplies*.

b. Package

i. Flip-chip on lead (FCOL QFN) or TI HotRod™: This package reduces switch-node ringing (one of the contributors to EMI). In this type of package, there are no wires to connect the IC to the lead frame. Solder bumps are placed on the IC die; the die is then flipped and attached to the lead frame. This helps to reduce parasitic capacitance and inductance. For more information, see the *TI E2E*™ article: *Effects of IC package on EMI performance*.

ii. Integrated power modules: Integrated power modules include MOSFET and an inductor in a shielded package that helps to eliminate an EM coupling inductor from external sources. It simplifies the layout helping to reduce unwanted parasitic and current path compared to converter controllers. See the *Simplify low EMI design with power modules application report white paper* for more details.

To find the appropriate buck converter or to boost the power for your design, see to the following links:
Buck Modules Integrated Inductor
Boost Modules Integrated Inductor
Buck Boost Inverting Modules Integrated Inductor

c. Slew rate: Slew rate control devices have independent control on the turn-on and the turn-off time of the high- and low-side MOSFET of the converter. This allows better control on the rise and fall time of the switching node, helping to reduce the ringing. For more information, see the *TI E2E*™ article: *How to use slew rate for EMI control*.

d. Pin Optimization: The butterfly package of device helps designers reduce EMI using PCB layout. H-field due to high current paths can be cancelled, resulting in lower effective inductance and lower EMI. For more information, see the *TI E2E*™ article: *How a DC/DC converter package and pinout design can enhance automotive EMI performance*.

2. System Design:

a. Phase control: In this method, DC/DCs are operated with phase-shifted frequency synchronized clocks, to bring down EMI, switching noise, and di/dt. It is achieved by using an oscillator with programmable phase and frequencies.

b. Slew rate control (as in RC snubber): Ringing at the DC/DC output can be reduced by using an RC snubber at the switching node of the DC/DC converter. However, it increases losses and reduces efficiency.

c. Filtering: Noise due to power supply at the ADC input should be at least less than one-third of ADC noise floor. This is to ensure ADC performance is not limited by power supply. This is achieved with:

i. Discrete Filter: For more information, see 2.2.3.3.1 of this design guide.

ii. Linear Regulation: LDO is used to get the required power supply rejection ratio (PSRR) at ADC power supply to reduce switching noise of the DC/DC converters. To understand LDO PSRR in more detail, see the *Understanding power supply ripple rejection in linear regulators technical brief*.

2.2.3 Circuit Design

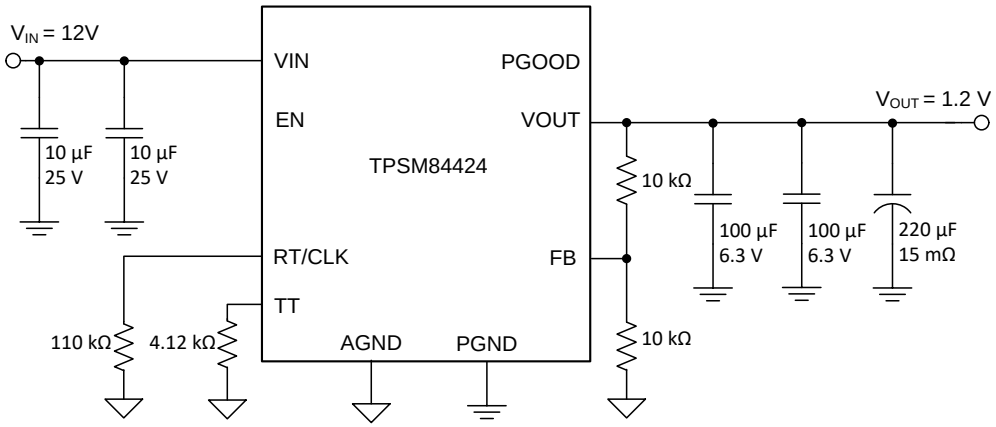
In this section, power supply design for high-speed ADC is described. Initially we start with DC/DC converter selection, and optimize power tree. This process is repeated for different DC/DC converters until it meets the efficiency and size requirements. Next, we select LDO or Filter to reject DC/DC output ripple and reduce power supply noise. In addition to this, multiphase frequency synchronization implementation is also discussed in this section. Finally, WEBENCH® Power Designer instructions are included.

2.2.3.1 DC/DC Converter Selection

The WEBENCH® Power Designer is used to select DC/DC converters for this design. 2.2.3.5 has the steps for using this tool. The TPSM84424 device is selected for this design to generate +1.9 V, +1.1 V, and +3.3 V, as it has both small form factor and high efficiency(> 87% at 1.9-V, 2-A output for 12-V input). This device output voltage ripple is less than 10 mV with a 12-V input and 1.9-V, 2-A output load. It has an enable pin, Power Good output, and *External Sync* option, that fulfill the design requirements. Furthermore, it supplies up to 4 A and is part of the TPSM84x24 family that can provide 6 A and 8 A in the same package size and support output voltages from 0.6 V to 10 V.

図 7 shows the circuit diagram to generate +1.2-V power rail using the TSPM84424 device. The output voltage of the TPSM84424 device is externally adjustable using a two-resistor divider (RFBT and RFBB). An external sync signal is provided to the RT/CLK pin of the converter to set the switching frequency, that enables the management of potentially degrading power-supply-generated spurs. The +3.3-V, +1.9-V, and +1.1-V rails use the same device in similar circuit configurations. See the *TPSM84424 4.5-V to 17-V input, 0.6-V to 10-V output, 4-A power module data sheet* or use WEBENCH to select the values of components.

図 7. TPSM84424 Circuit Diagram



The LMZM23601 DC/DC converter is used to generate ±2.5-V rails that are required for the input amplifiers of the AFE. It can deliver up to 1000 mA and is used in inverting buck-boost topology to generate a –2.5-V rail. The maximum output current of the –2.5-V rail is less than $Iout_{max}$ × (1 – D) (where D is duty cycle of the converter). The output voltage of the LMZM23601 device is externally adjustable using a two-resistor divider (RFBT and RFBB). In this design, the amplifier inputs were bypassed and the signal was directly input to the ADC with the balun. As a result, the sync pin was not utilized. See the *LMZM23601 36-V, 1-A step-down DC/DC power module in 3.8-mm × 3-mm package data sheet* and *Inverting application for the LMZM23601 and LMZM23600 application report* for more details.

2.2.3.2 Power Tree Selection

A DAQ system requires multiple rails to power the analog, digital, and mixed-signal circuits. The total system power requirement increases with the number-of-channels requirement. Therefore, select the power tree for high efficiency and small form factor. 図 8 and 図 9 show two different multi-channel power supply trees. To improve system efficiency, the input DC rail is down-converted using the DC/DC buck switching regulator and then regulated using a low-drop linear regulator as both 図 8 and 図 9 show.

図 8. Power Tree 1

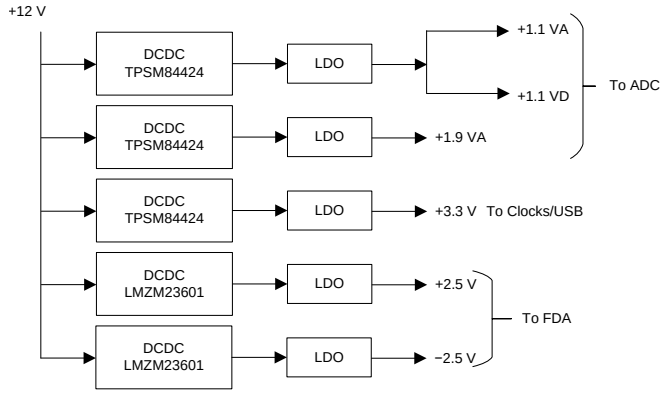


図 9. Power Tree 2

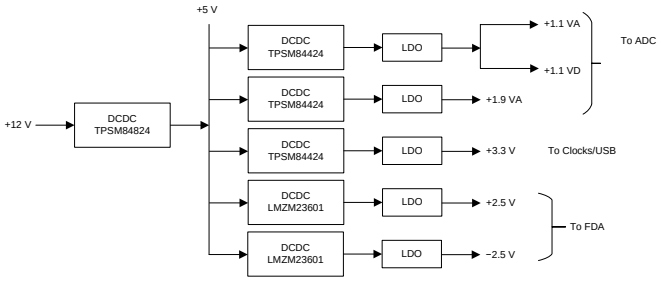


表 3. Efficiency of Converters at Different Output Voltages

CONVERTERS	I/P VOLTAGE	O/P VOLTAGE	LOAD	SWITCHING FREQUENCY	EFFICIENCY
TPSM84424	5V	1.1 V	2.5 A	400 kHz	92%
	5V	1.9 V	2.0 A	450 kHz	94%
	5V	3.3 V	2.0 A	1000 kHz	97%
	12 V	1.1 V	2.5 A	400 kHz	85%
	12 V	1.9 V	2.0 A	450 kHz	87%
	12 V	3.3 V	2.0 A	1000 kHz	92%
LMZM23601	5 V	2.5 V	0.5 A	1000 kHz	84%
	5 V	–2.5 V	0.5 A	1000 kHz	84%
	12 V	2.5 V	0.5 A	1000 kHz	76%
	12 V	–2.5 V	0.5 A	1000 kHz	76%
TPSM84824	12 V	5 V	4 A	1200 kHz	94%

Using data from 表 3, the final efficiency of DC/DCs is calculated using 式 1.

$$\text{Efficiency}(n) = \frac{\sum_{i=1}^{k} P_i}{\sum_{i=1}^{k} \frac{P_i}{n_i}} \quad (1)$$

where

- k is the number of output rails
- P_i is the output power of each rail
- n_i is the efficiency of each output rail

The net efficiency of converters using the power-supply tree shown in 図 8 = 86.6 %.

The net efficiency of converters using the power-supply tree shown in 図 9 = 87.5 %.

注: For calculation, the efficiency of the –2.5-V rail is assumed to be the same as the +2.5-V rail and the –2.5-V rail is generated using the LMZM23601 device in inverting buck-boost configuration.

The power-supply scheme in 図 9 shows only 1% better efficiency than the power supply shown in 図 8, but it uses an additional converter. Therefore, in this design the power-supply tree in 図 8 is used.

2.2.3.3 DC/DC Ripple Rejection Using Filter or LDO

DC/DC converter selection is discussed in 2.2.3.1. However, AFE needs a low-noise power supply for good performance. Therefore we use LDO, Filter, or its combination after DC/DC converters. This section describes filter design and LDO selection for high-speed GSPS ADC. They are designed for rejection such that power supply spurs are less than the next spur in the given bandwidth. In the next paragraph, rejection calculation is explained.

The TPSM84424 device has an output voltage ripple less 12 mV at the 12-V input and 1.1-V, 2.5-A output load. For a –100 dBFS spur target and 800-mV full scale of ADC, the required voltage ripple and PSRR is calculated using 式 2 and 式 3. The required PSRR equals to 63 dB, for previously listed data. In general, a high-speed ADC does not have good PSRR. With sufficient decoupling capacitors, more than 20-dB PSRR is achieved. Therefore, to meet the design target, more than 40-dB PSRR is required. It can be achieved using LDO, or a filter, or an LDO + filter combination. The following subsections detail the filter and LDO circuit design to achieve PSRR > 40 dB. If the required rejection is not met by LDO or Filter, then its combination is used.

$$V_{PPxdBFS} = V_{PP0dBFS} \times 10^{\text{Design Spur target(dBFS)} / 20} \quad (2)$$

$$\text{Required PSRR} = 20\log\left(\frac{V_{PP\_Source}}{V_{PPxdBFS}}\right) \quad (3)$$

2.2.3.3.1 Filter Design

A PI filter is used to filter DC/DC noise. The filter consists of a Ferrite bead (1000 Ω at 100 MHz, BLM41PG102SN1L) and two capacitors of 0.1 µF. A filter is placed near the ADC, for each of its power rails. 図 10 shows a ferrite bead equivalent circuit. It is modeled as R || L || C. The R, L, and C parameters are found from the impedance plot of the ferrite bead. 図 11 shows the insertion loss plot of the filter at a 1.1-V, 600-mA load from simulation. It provides rejection of 50 dB at 750 kHz which meets the design requirement. A feedthrough capacitor (such as the NFM31PC276B0J3) is also considered in this design, which works best as an electromagnetic interference (EMI) filter. ESR and ESL reduces for this type of geometry, compared to an equivalent, similar-sized MLCCs. Hence, it provides 10-dB to 15-dB rejection even at high frequency around 100 MHz. The feedthrough capacitor is placed near the DC/DC converter.

図 10. PI Filter Simulation Circuit

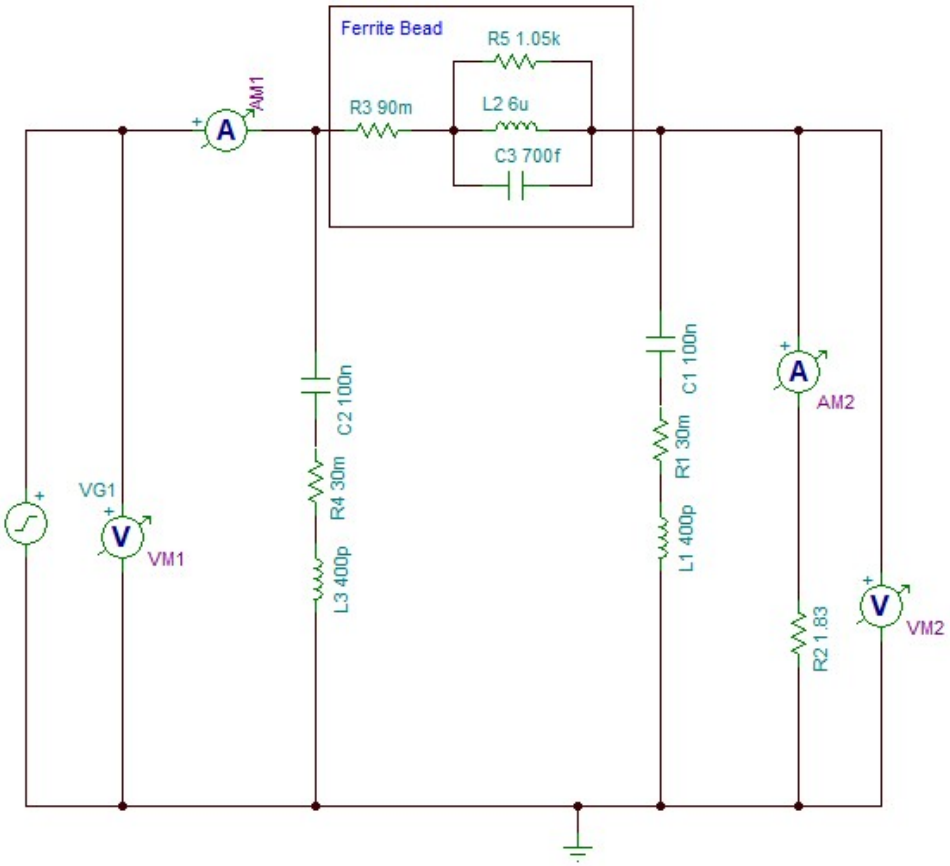
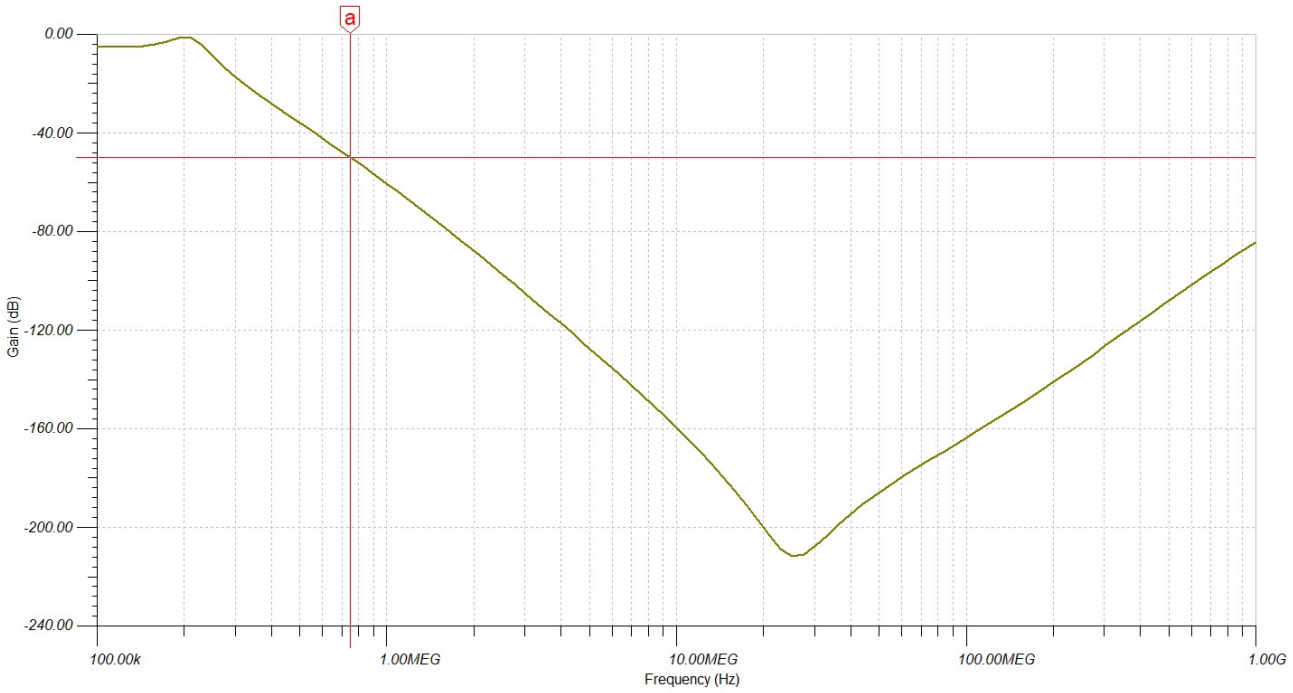


図 11. Insertion Loss of PI Filter



2.2.3.3.2 LDO Circuit

The TPS7A84 LDO is used in this design. This is a high PSRR, low-noise LDO, and has Power Good and enable pins. This device is provided for +3.3-V, +1.9-V, and +1.1-V power rails. It provides high PSRR up to 40 dB at 750 kHz, that meets the design requirement. If PSRR required is more, use a post PI filter to increase it.

This device has ANY-OUT™ programmable pins to program the desired output voltage. The sum of the internal reference voltage (VREF = 0.8 V) plus the accumulated sum of the respective voltage is assigned to each active pin. The ANY-OUT pins (pin 10, pin 7, and pin 6) are programmed to active low to achieve 1.9 V at output. 図 12 shows the LDO circuit.

図 13 shows PSRR vs frequency of this LDO for different input voltages. For V_{IN} = 3.8 V, LDO has PSRR of 40 dB at 500 kHz for 500-mV dropout voltage. And so we have set 500-mV LDO dropout for +3.3-V, +1.9-V, and +1.1-V power rails.

The TPS7A8300 and TPS7A33 devices are provided for ±2.5-V power rails. They both are ultra-low noise LDO capable of sourcing a maximum load of 1 A. The ±2.5-V rails are generated with output feedback resistors.

注: The TPS7A84 device requires a bias voltage ≥ 3.0 V to operate if 1.1 V ≤ V_{IN} < 1.4 V. This reference design does not have an option to supply the required bias voltage. Either the V_{IN} must be greater than 1.4 V, or bias voltage must be applied externally.

図 12. TPS7A84 LDO Circuit to Generate +3.3 V

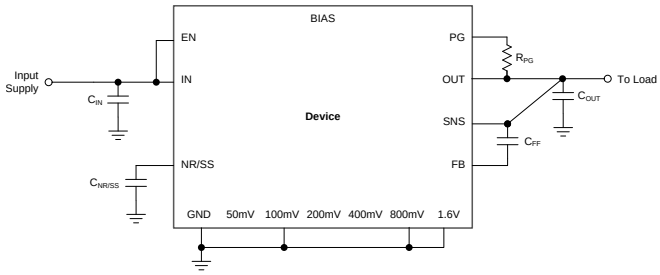
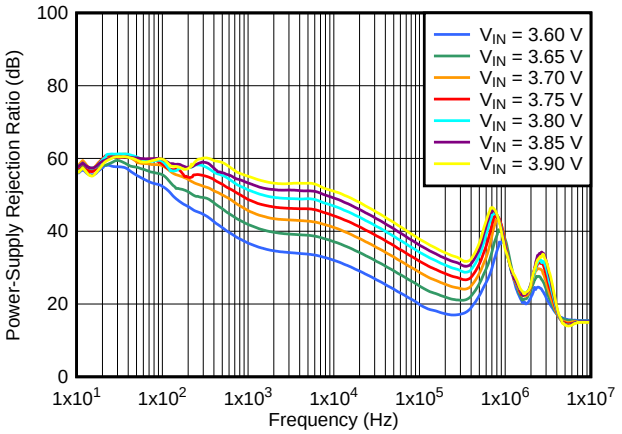


図 13. PSRR vs Frequency and V_{IN} for V_{OUT} = 3.3 V



IOUT = 3 A, COUT = 47 µF || 10 µF || 10 µF, CNR/SS = 10 nF, CFF = 10 nF

2.2.3.4 Multi-Phase Sync Generation

As discussed in 2.2.2, phase control helps to bring down EMI, switching noise, and di/dt. The basic idea is to operate DC/DC converters at different time intervals in a switching cycle, that reduces di/dt, and results in reduction in EMI. Furthermore, frequency sync is used to manage DC/DC-generated spurs in the ADC output spectrum. Consequently, a digital filter can be implemented to remove these known spurs. Frequency sync also helps in eliminating noise due to beating effect of DC/DC converters. In this design, all DC/DCs are selected such that they support external frequency synchronization. The Sync signal is provided to a high-speed ring counter with decoded outputs. This generates phase-shifted and phase-aligned clock signals that are fed to the converters.

図 14 and 図 15 show circuit diagrams to generate phase-aligned and phase-shifted sync pulses SYNC1, SYNC2, and SYNC3, respectively, for +1.9-V, +1.1-V and +3.3-V rails. In a phase-shifted sync scheme, sync signals are 120° phase apart. This reference design implements phase shifting of +1.9-V, +1.1-V, and +3.3-V rails, because ±2.5-V rails are powered down and the amplifier inputs were bypassed with the balun. Phase shifting also helps reduce input ripple current and input capacitance for DC/DC converters.

図 14. Phase-Aligned Sync

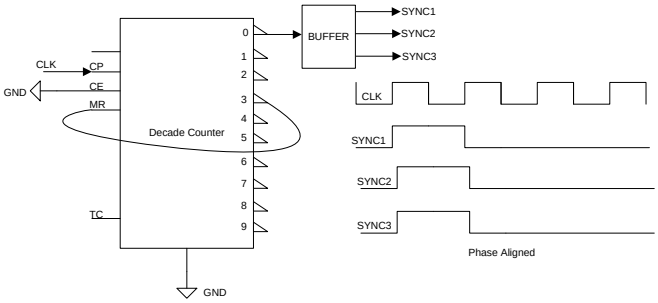
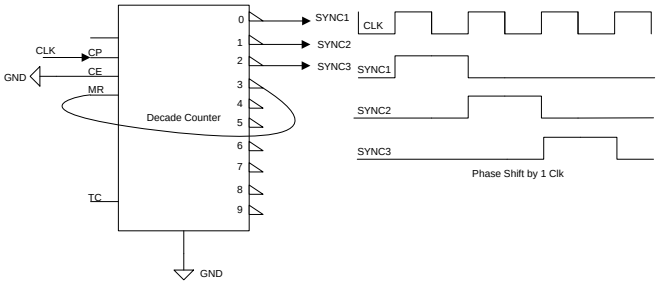


図 15. Phase-Shifted Sync

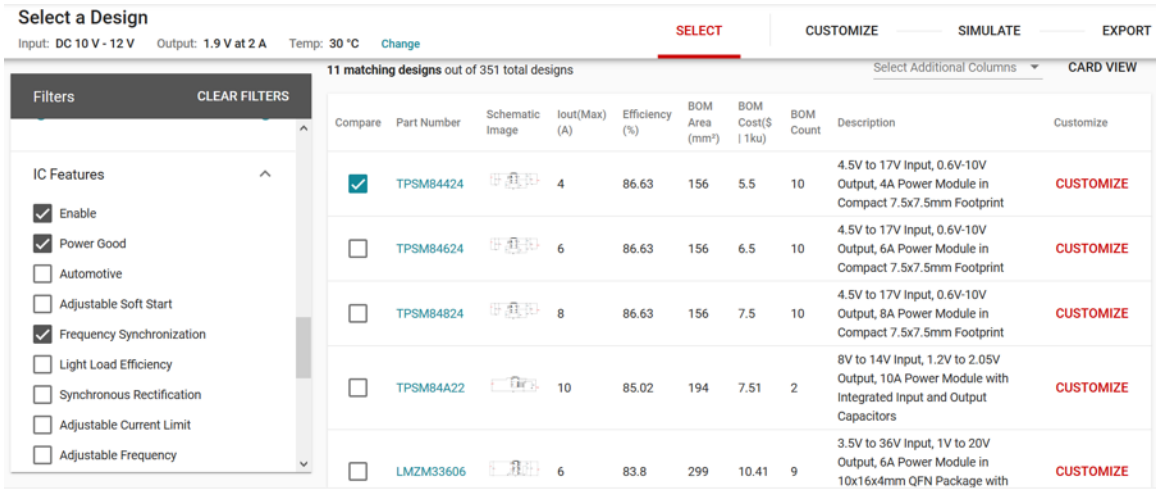


2.2.3.5 WEBENCH® Power Designer Steps

In this design, the WEBENCH® Power Designer is used to design power rail circuits. The WEBENCH® environment gives us end-to-end power supply design capabilities that save time during all phases of the design process. The following steps are used to design a 1.9-V power rail circuit:

1. Go to WEBENCH® Power Designer
2. Select *DC/DC Power Designs* and Click on *Start Design*
3. Provide *Input Voltage Range*, *Output Voltage*, and *Max Output Current*. Using the *Advanced Options*, set the *Max Vout Ripple* and Nominal Iout current parameters. Select one of the design considerations from *Balanced*, *Low cost*, *High Efficiency* and *Small Footprint*. In this design, the input voltage for DC/DC converters is 12 V, as most of the applications such as high-speed DAQ, oscilloscope, and so forth, use 12-V power rail to generate ADC power rails.
4. Agree to the Terms and Conditions of Use and Select View Designs
5. Apply filters to reduce the total number of designs. 図 16 shows a list of power supply designs for a 1.9-V rail in WEBENCH, after the following filters are applied.
   a. Regulator type - In this design, Module(Integrated Inductor) is selected
   b. Select IC features: This design requires converters to have Enable, Power Good, and SYNC pins.
   c. Select Design Attributes like efficiency, BOM Cost, Switching frequency, and so forth, if you have specific requirements.

図 16. Power Design Using WEBENCH®



6. Now, select a design from the available list and click *Customize*. In this design, the TPSM84424 device is used for +3.3-V, +1.9-V, and +1.1-V rails and the LMZM23601 device is used for ±2.5-V rail generation.
7. Simulate to verify the design. Select the simulation type from *Startup*, *Load Transient*, *Input Transient* and *Steady State*.

注: *WEBENCH provides options to export schematic, PCB Layout and BOM for Altium Designer, Cadence OrCAD, CadSoft Eagle, Mentor Graphics and P-CAD Software*.

WEBENCH Power Designer has much more capability than what is mentioned in this section. Refer to WEBENCH for more information or see the short training video WEBENCH Power Designer: Step by Step, to get started.

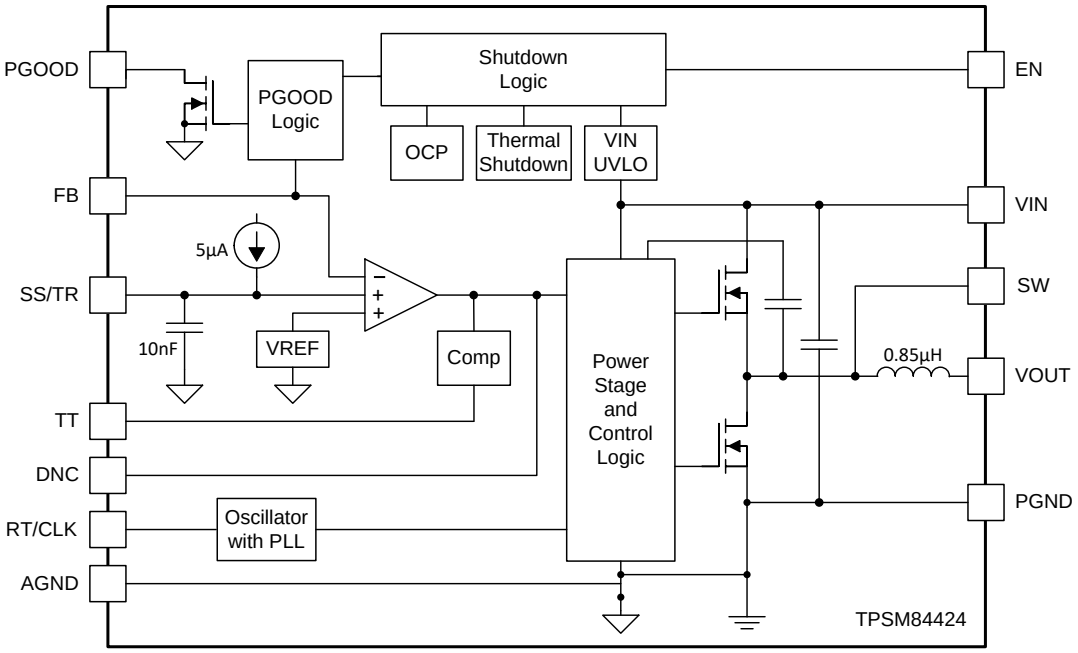
2.3 Highlighted Products

The devices used and the reasons for selecting them are explained in this section.

2.3.1 TPSM84424, TPSM84624, and TPSM84824

TPSM84424 4.5-V to 17-V input, 0.6-V to 10-V output, 4-A power module data sheet	TPSM84424 samples and availability
Evaluation Modules:	TPSM84424 EVM

図 17. TPSM84424 Functional Block Diagram



The TPSM84424 power module is an easy-to-use integrated power supply that combines a 4-A DC/DC converter with power MOSFETs, a shielded inductor and passives into a small form factor, QFM package. It is used in this design to bring down the 12-V input voltage to 1.9 V, 1.1 V and 3.3 V. This power solution allows as few as six external components while maintaining the ability to adjust key parameters to meet specific design requirements. It has the TurboTrans™ feature that allows the transient response to be optimized for reduced output voltage deviation with less required output capacitance.

Why choose this device? Key features:

- High efficiency, > 87% at 1.9-V, 2-A output for 12-V input
- HotRod package to reduce EMI
- Allows synchronization to an external clock
- 7.5-mm × 7.5-mm × 5.3-mm QFM package
- This device meets EN55011 Class B radiated EMI limits

Alternatives:

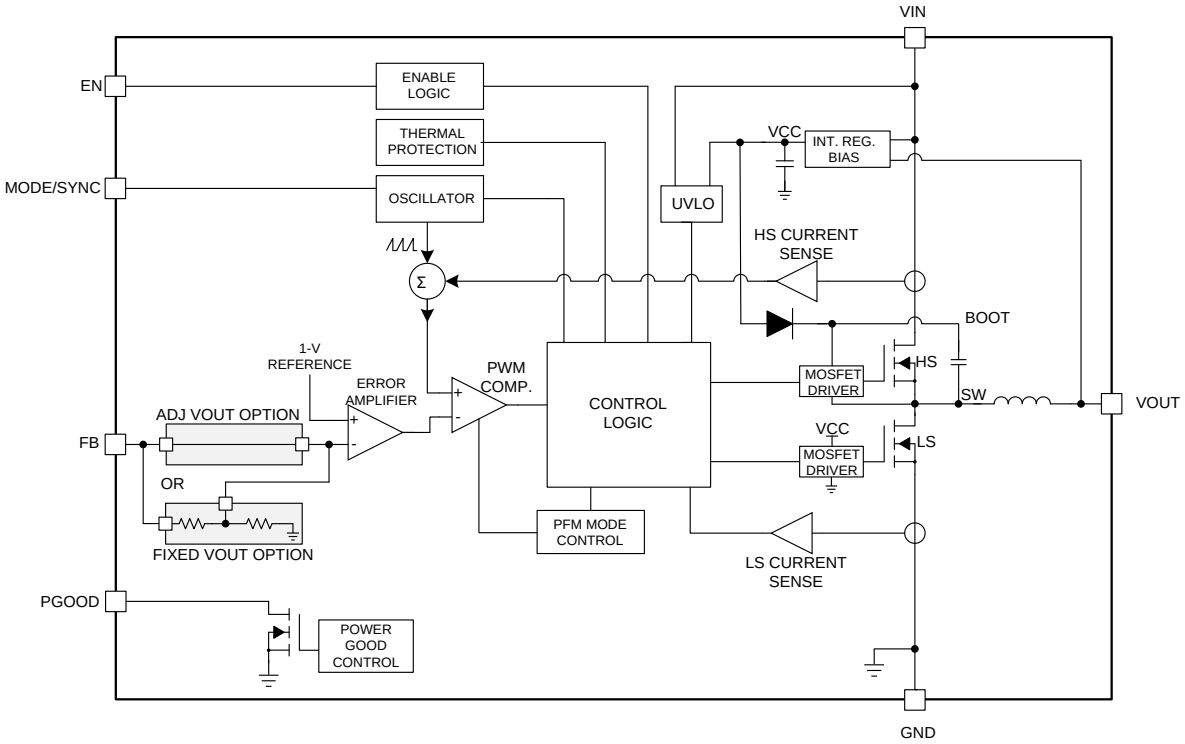
DEVICE	I_{OUT} (MAX) (A)	V_{IN} (MAX) (V)	V_{IN} (MIN) (V)	V_{OUT} (MAX) (V)	V_{OUT} (MIN) (V)	EMI TESTED, ENABLE, FREQUENCY SYNCHRONIZATION, POWER GOOD
TPSM84624	6	17	4.5	10	0.6	✓
TPSM84824	8	17	4.5	10	0.6	✓
LMZM33606	6	36	3.5	20	1	✓

Use the WEBENCH® Power Designer to create a custom design with the TPSM84424 device.

2.3.2 LMZM23601

LMZM23601 36-V, 1-A step-down DC/DC power module in 3.8-mm × 3-mm package data sheet	LMZM23601 Samples and Availability
Evaluation Modules	LMZM23601 3.3-V Output EVM, LMZM23601 5-V Output EVM

図 18. LMZM23601 Functional Block Diagram



The LMZM23601 device is an integrated-inductor power module, that is specifically designed for space-constrained industrial applications. It is used in this design to bring down the 12-V input voltage to ±2.5 V. It is available in two fixed output voltage options of 5-V and 3.3-V, and an adjustable (ADJ) output voltage option supporting a 2.5-V to 15-V range. The LMZM23601 has an input voltage range of 4-V to 36-V and can deliver up to 1000-mA of output current.

An inverting buck configuration is implemented using the LMZM23601 device for generation of a –2.5-V power rail. See the *LMZM23601 36-V, 1-A step-down DC/DC power module in 3.8-mm × 3-mm package data sheet* for more details.

Why choose this device? Key features:

- EMI tested
- Allows synchronization to an external clock
- Miniature 3.8-mm × 3-mm × 1.6-mm package

Alternatives:

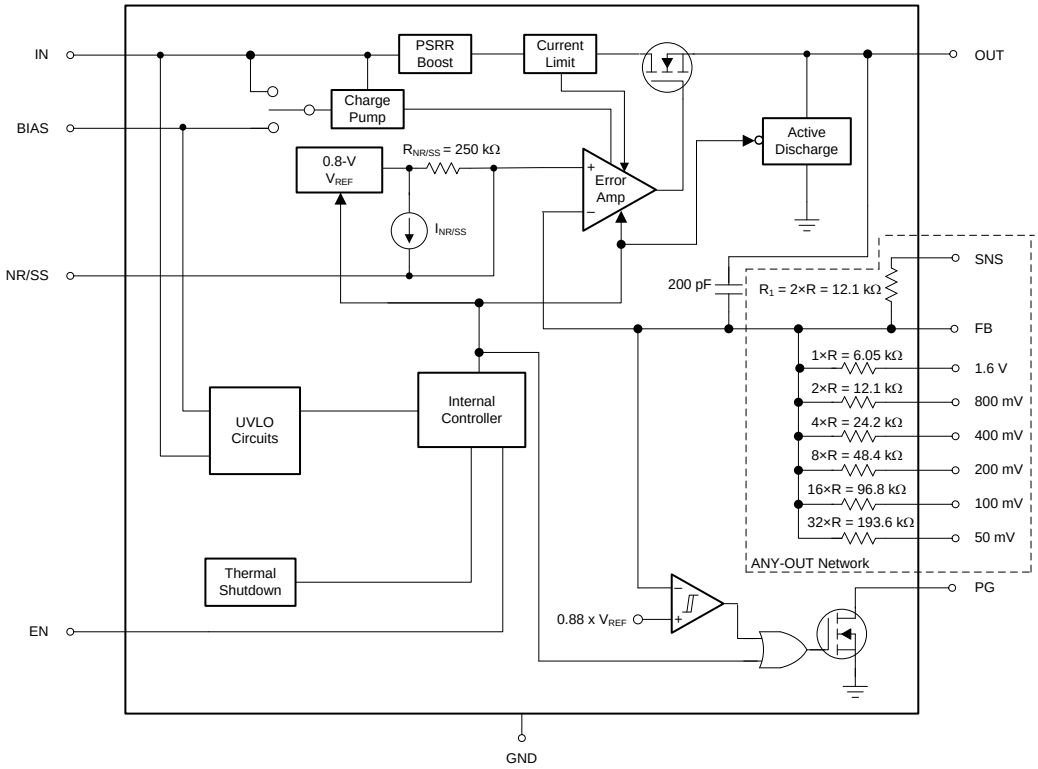
DEVICE	I_{OUT} (MAX) (A)	V_{IN} (MAX)(V)	V_{IN} (MIN) (V)	V_{OUT} (MAX)(V)	V_{OUT} (MIN) (V)	EMI TESTED, ENABLE, FREQUENCY SYNCHRONIZATION, POWER GOOD
LMZM23600	0.5	36	4	2.5	15	✓
LMZM33602	2	36	4	1	18	✓

Use the WEBENCH® Power Designer to create a custom design with the LMZM23601 device.

2.3.3 TPS7A84

TPS7A84 high-current (3 A), high-accuracy (1%), low-noise (4.4 μV_{RMS}), LDO voltage regulator data sheet	TPS7A84 samples and availability
Evaluation Modules	TPS7A84 EVM

図 19. TPS7A84 Functional Block Diagram



The TPS7A84 is a low-noise (4.4 μV_{RMS}), low-dropout linear regulator (LDO) capable of sourcing 3 A with only 180 mV of maximum dropout. The device output voltage is pin-programmable from 0.8 V to 3.95 V and adjustable from 0.8 V to 5.0 V using an external resistor divider.

Why choose this device? Key features:

- Good power-supply ripple rejection ratio: 40 dB at 500 kHz
- Low output voltage noise: 4.4 μV_{RMS} at 0.8-V output
- 1% (max) accuracy over line, load, and temperature
- Enable and Power Good pins to implement power sequencing

Alternatives

Device	I_{OUT} (MAX) (A)	V_{IN} (MAX) (V)	V_{IN} (MIN) (V)	V_{OUT} (MIN) (V)	V_{OUT} (MAX) (V)	PSRR at 500 kHz (dB)	FEATURES
TPS7A8300	2	6.5	1.1	0.8	5	30	Enable, output discharge, power good, soft start
TPS7A85	4	6.5	1.1	0.8	5	40	Enable, output discharge, power good, soft start

2.3.4 CD74HC4017

The CD74HC4017 device is a decade counter with decode outputs. It is used in this design to generate multi-phase synchronized clocks of switching regulators. It can take a maximum of 30-MHz clock input at VCC = 4.5 V and 25°C.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

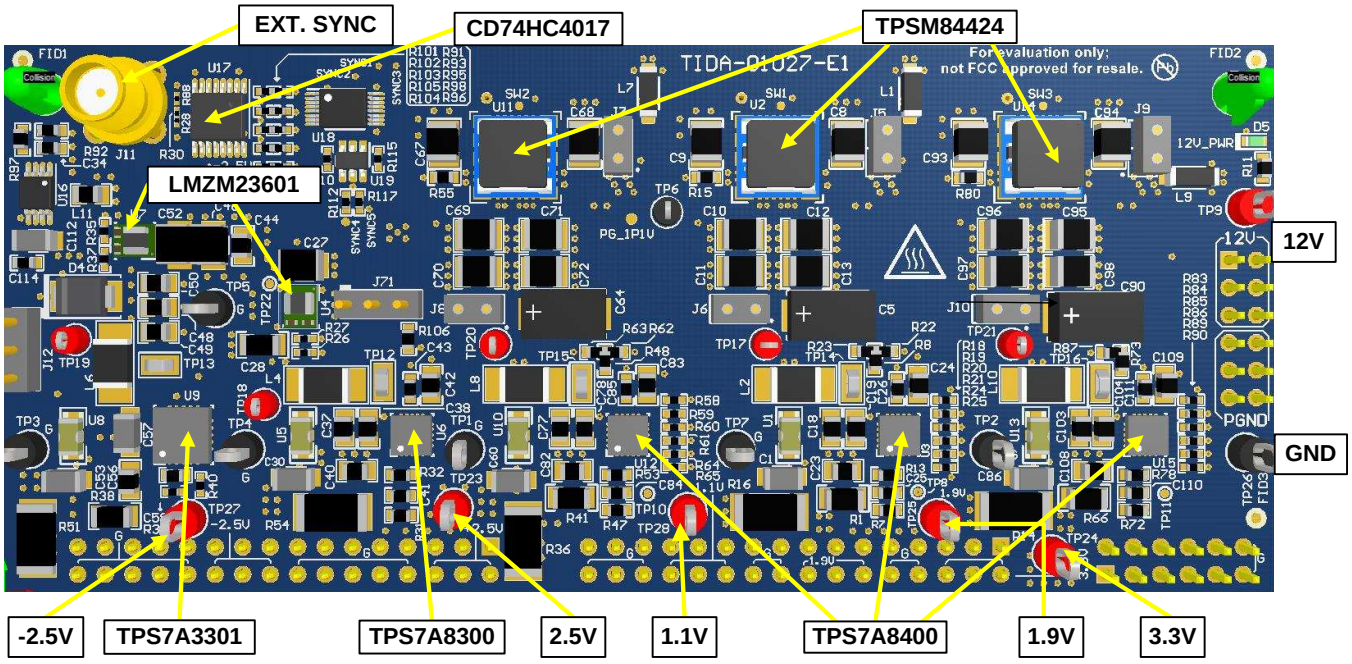
This design uses the following hardware and software to measure the impact of the power supply on DAQ performance.

- TIDA-01027 power supply board
- High-speed DAQ, (TIDA-01022 board is used)
- TSW14J57 capture card (FPGA)
- HSDC TID GUI (Used to program TIDA-01022 board)
- High-speed data converter pro software (Used to capture data from FPGA)

3.1.1 Hardware Description

図 20 shows the TIDA-01027 reference design hardware. The printed circuit board (PCB) has a 117.5-mm × 51-mm rectangular form factor. This board is compatible with the TIDA-01022 (high-speed DAQ) and can be plugged to the last for quick evaluation. The input voltage of the board ranges from 5 V to 17 V. The integrated circuits (TPSM84824, LMZM23601, CD74HC4017, TPS7A8400, TPS7A8300, and TPS7A3301), several test points, and jumpers are located on the top side of the PCB. SMA Connector J11 provides external synchronization of DC/DC converters. D5 LED ON state indicates the input voltage available. The default configuration is DC/DC + Filter, where LDOs are bypassed by the filters.

図 20. TIDA-01027 Hardware Image



3.1.2 Test Point Description

表 4 lists the test points and their functions.

表 4. Test Point Description

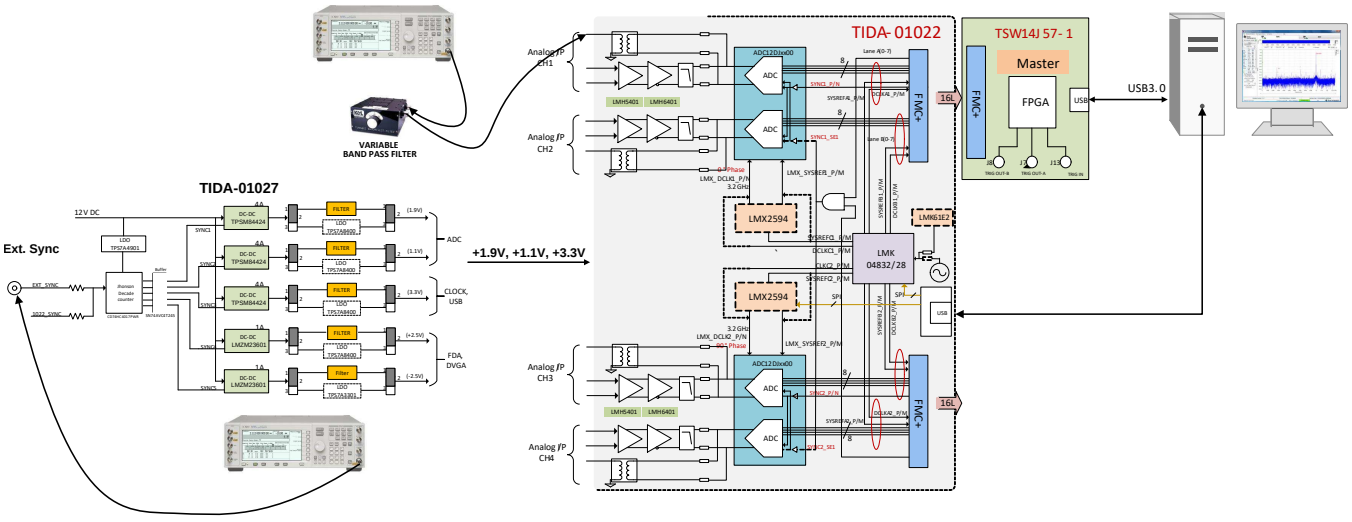
TEST POINT	FUNCTION
TP9	12-V DC Input
TP1, TP2, TP3, TP4, TP5, TP7, TP26	Ground
TP23	+2.5 V
TP27	-2.5 V
TP24	+3.3 V
TP25	+1.9 V
TP28	+1.1 V
SW1, SW2, SW3	Duty cycle of DC/DC 1.9 V, 1.1 V, and 3.3 V, respectively

3.2 Testing and Results

3.2.1 Test Setup

The TIDA-01022 board is used to measure the power supply impact on the AFE performance. This is a high-speed, multi-channel data capture board, capable of capturing data at a maximum of 12.8 GSPS. This board uses two 12-bit, 6.4 GSPS ADCs. See the TIDA-01022 and TIDA-01028 reference designs for more information. For all test results, the sampling frequency of the TIDA-1022 board is set to 3.2 GSPS. An input signal of frequency F_{IN} = 800 MHz and amplitude A_{IN} = –1 dBFS is used, and is synchronized to the ADC clock. This is done to avoid spectral leakage. The ±2.5-V power rail is powered down in the TIDA-01027 board, and an input signal is provided to the TIDA-01022 Channel 1 with balun. 図 21 shows the test setup to capture the ADC output spectrum.

図 21. Test Setup to Capture ADC Output Spectrum



3.2.2 Test Results

In the following subsections, the ADC output spectrum is compared between the power supply that uses Filter and LDO, and their impact on the ADC is observed. Furthermore, phase shifting is compared with phase aligned for input ripple current to show reduction in EMI due to phase shift. Finally, power-supply efficiency data is included for both DC/DC and DC/DC+LDO.

3.2.2.1 ADC Output Spectrum, Comparison Between LDO and Filter

In this test case, an input signal of 800-MHz frequency and an external low-noise 3.2-GHz clock are used. In the power-supply board, TIDA-01027, only three rails +1.9 V, +1.1 V, and +3.3 V are powered on. They are set at 750-kHz switching frequency and are 120° phase-shifted. Other rails ±2.5 V are powered down, because amplifiers are bypassed and input to ADC is provided with balun. The output spectrum of 12-bit ADC, **ADC12DJ3200**, is captured and compared for LDO and filter output options of the power supply. FFT uses 524288 samples and is averaged by 10 for this measurement.

When the Filter is removed, direct DC/DC output is provided to the ADC power-supply pins, $F_{DC/DC}$ and $F_{in}\pm F_{DC/DC}$ spurs appear in the spectrum, as 図 22 shows.In this case, spurs appear at 799.25 MHz and 800.75 MHz. Filter and LDO are used to reduce these spurs. 図 23, 図 24 and 図 25 show the output spectrum of the ADC with power supply that uses LDO and Filter. The output spectrum is compared between them. It is observed that there are not any $F_{DC/DC}$ and $F_{in}\pm F_{DC/DC}$ spurs in the spectrum either using LDO or Filter. The same noise floor is achieved by replacing LDO with Filter. Thus, Filter replaces LDO in this design.

図 22. ADC Output With Only DC/DC (F_{IN} ± 3 MHz)

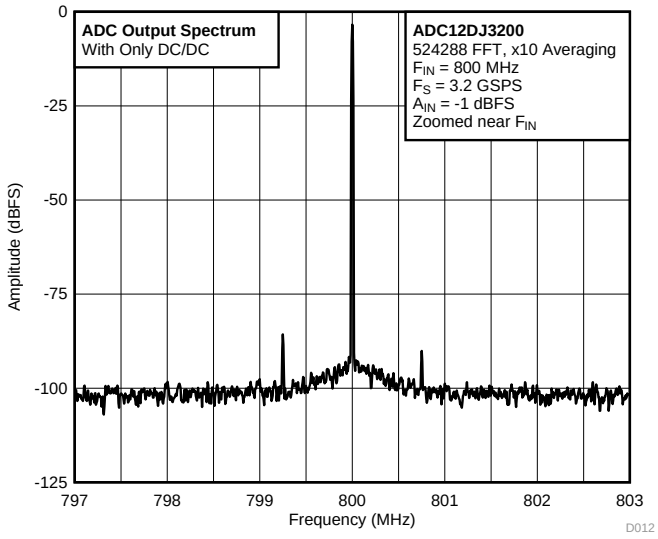


図 23. ADC Output, Filter vs LDO (Full Spectrum)

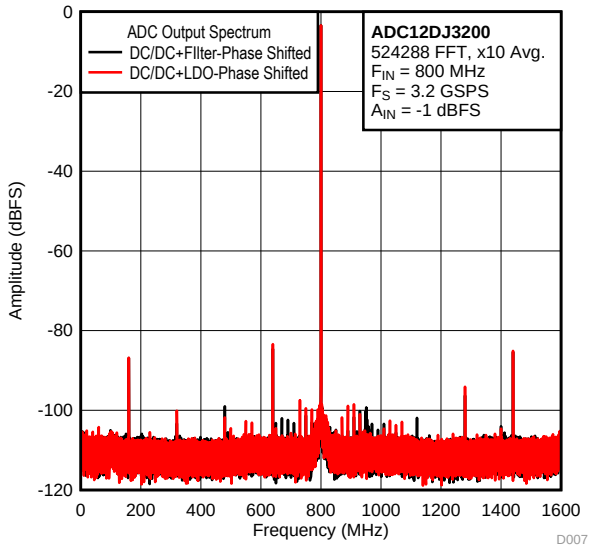


図 24. ADC Output, Filter vs LDO (F_{IN} ± 3 MHz)

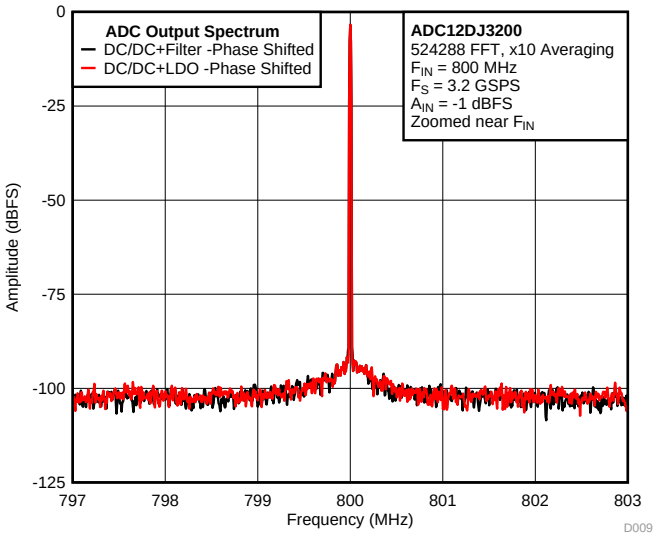
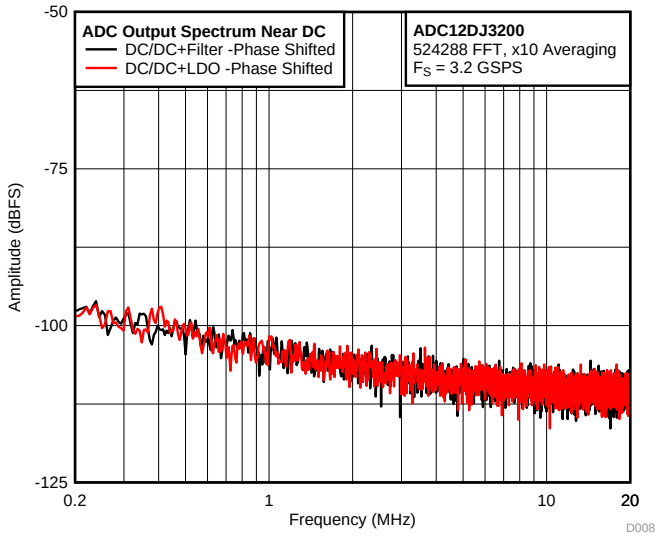


図 25. ADC Output, Filter vs LDO (Near DC)



3.2.2.2 Input Ripple Current

Input ripple is measured to compare between phase-shifted and phase-aligned frequency synchronization schemes. A current probe is used at the power supply input for this measurement. DC/DC converters are set to 750-kHz frequency with output loads of 2.5 A, 2.0 A, and 2.0 A for 1.1-V, 1.9-V, and 3.3-V rails, respectively. 図 26 and 図 27 show input ripple current measurement with a total 20-µF input capacitor. It is observed that phase shifting reduces input ripple current, that results in EMI reduction due to di/dt. Phase-shifting also reduces inrush current and total input capacitor.

図 26. Input Ripple Current Phase-Aligned

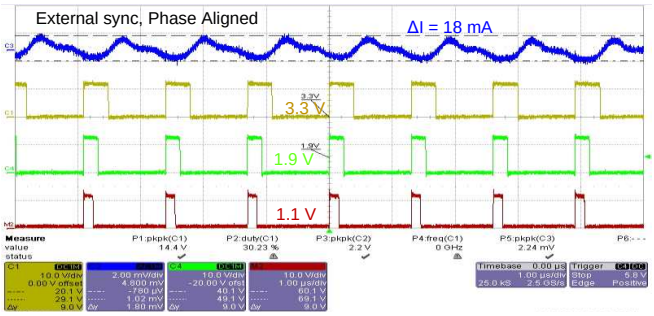
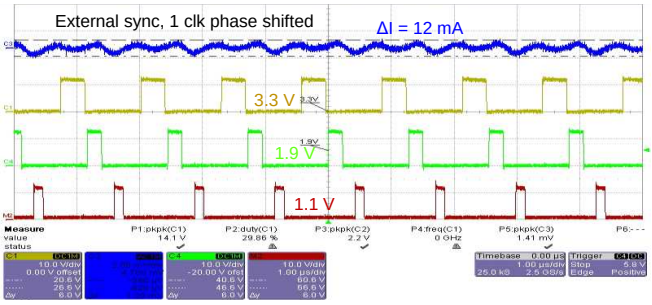


図 27. Input Ripple Current Phase-Shifted

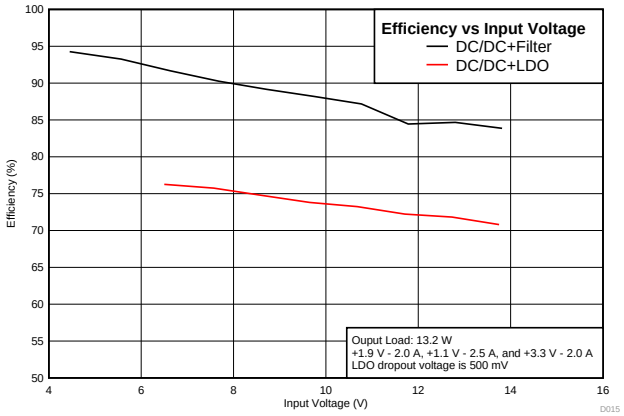


3.2.2.3 Power-Supply Efficiency

図 28 shows the power-supply efficiency comparison between DC/DC+Filter and DC/DC+LDO configurations. It is observed that removing LDO improves total efficiency by more than 13%, and maximum efficiency of 85% is achieved at the 12-V input.

To calculate the efficiency of the power supply, the input voltage is measured at the input of the converter. Output voltage is measured at Filter and LDO outputs, respectively, in the DC/DC+Filter and DC/DC+LDO case, and the output current is measured using 10-m resistors. In the TIDA-01027 board, only three rails +1.9 V, +1.1 V, and +3.3 V are powered. All converters are operating at 750 kHz. The LDO dropout voltage is set to 500 mV. The load current of converters are 2.5 A, 2.0 A, and 2.0 A for 1.1-V, 1.9-V, and 3.3-V power rails, respectively.

図 28. Efficiency vs Input Voltage Curve



3.2.3 Summary

The analog front end (AFE) performance remains unaffected after LDO is replaced with Filter for 12-bit high-speed GSPS systems. This improves power-supply efficiency, reduces power consumption and PCB size, and enhances thermal performance. TI HotRod™ package technology reduces DC/DC EMI. Phase-shifting reduces power-supply noise, inrush current, input ripple current, and input capacitance.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01027.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01027.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01027.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-01027.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01027.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01027.

5 Related Documentation

1. Texas Instruments, *Power-supply design for high-speed ADCs application report*
2. Texas Instruments, *Designing a modern power supply for RF sampling converters analog application journal*
3. Texas Instruments, *Using a buck converter in an inverting buck-boost topology*
4. Texas Instruments, *Inverting application for the LMZM23601 and LMZM23600 application report*
5. Texas Instruments, *Supply noise effect on oscillator phase noise application report*
6. Texas Instruments, *Low noise power solution reference design for clock generators design guide*
7. Texas Instruments, Simplify low EMI design with power modules white paper

5.1 商標

5.2 Third-Party Products Disclaimer

6 About the Author

SHAURY ANAND is a systems engineer at Texas Instruments India, where he is responsible for developing reference design solutions for the industrial segment

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