参考資料

デザイン・ガイド：TIDA-020014
3 種類の IGBT/SiC バイアス電源ソリューションを持つ HEV/EV トラクション・インバータ電力段のリファレンス・デザイン

概要

このリファレンス・デザインでは、ハイブリッド電気自動車および電気自動車 (HEV/EV) システム用の、3 つの 12V 車載バッテリ入力、4.2W バイアス電源ソリューションを持つ、トラクション・インバータの単相電力段を紹介します。すべてのバイアス電源ソリューションは、12V 車載バッテリから DC 4.5V～42V の広い範囲の電圧を入力でき、+15V、-8V、または +20V、-4V に構成可能な最大電流 180mA の出力を生成します。電力段には 5.7kV_{RMS} 強化絶縁の絶縁ゲート・ドライバが組み込まれ、SiC/IGBT ハーフブリッジ・モジュールに収まるように 100mm × 62mm の外形で設計されています。絶縁 DC バス・センシング機能、絶縁温度センシング機能、ロジック貫通電流保護機能、診断機能を搭載しています。入力が低電圧の場合のスタートアップ、効率、負荷レギュレーションの各テストを実施済みであるほか、高電圧の場合を想定し、すべてのバイアス電源を電力段と IGBT モジュールに接続する方法で、CMTI、ダブル・パルス、短絡の各テストも実施済みです。

リソース

TIDA-020014	デザイン・フォルダ
TIDA-020015	デザイン・フォルダ
LM5180-Q1	プロダクト・フォルダ
TPS40210-Q1	プロダクト・フォルダ
LM46002-Q1	プロダクト・フォルダ
SN6505B-Q1	プロダクト・フォルダ
ISO5852S-Q1	プロダクト・フォルダ
AMC1311-Q1、AMC1301-Q1	プロダクト・フォルダ

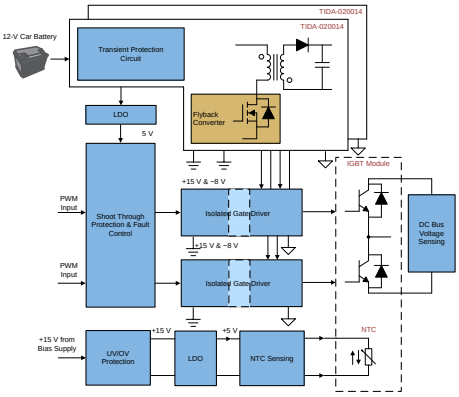
TI E2E™ Community　E2E™エキスパートに質問

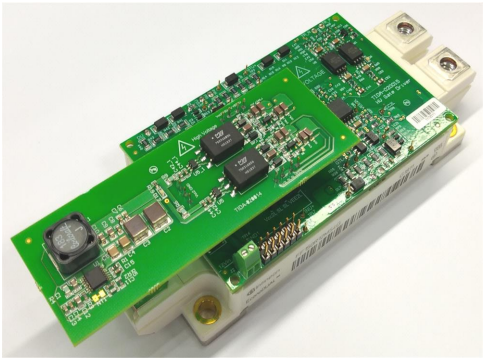
特長

- デュアル・チャネル絶縁ゲート・ドライバ、絶縁 DC バス電圧センシング、絶縁温度センシングを備えたトラクション・インバータ、単相、電力段設計
- IGBT/SiC 絶縁ゲート・ドライバ用の 3 種類の SiC/IGBT バイアス電源ソリューション
- DC 4.5V～42V の広い入力電圧 V_{IN} に対応するコンバータ
- +15V、-8V または +20V、-4V に構成可能な出力 (最大負荷 180mA) で、Si IGBT および SiC MOSFET モジュールを駆動
- 高電圧伝導過渡を、下流の回路にとって安全なレベルにクランプする保護機能
- フォトカプラ不要の 1 次側レギュレーションにより、小さな外形で長寿命を実現

アプリケーション

- インバータ / モータ制御
- オンボード・チャージャ (OBC) とワイヤレス・チャージャ
- ガソリン / ディーゼル・エンジン・プラットフォーム
- DC/DC コンバータ





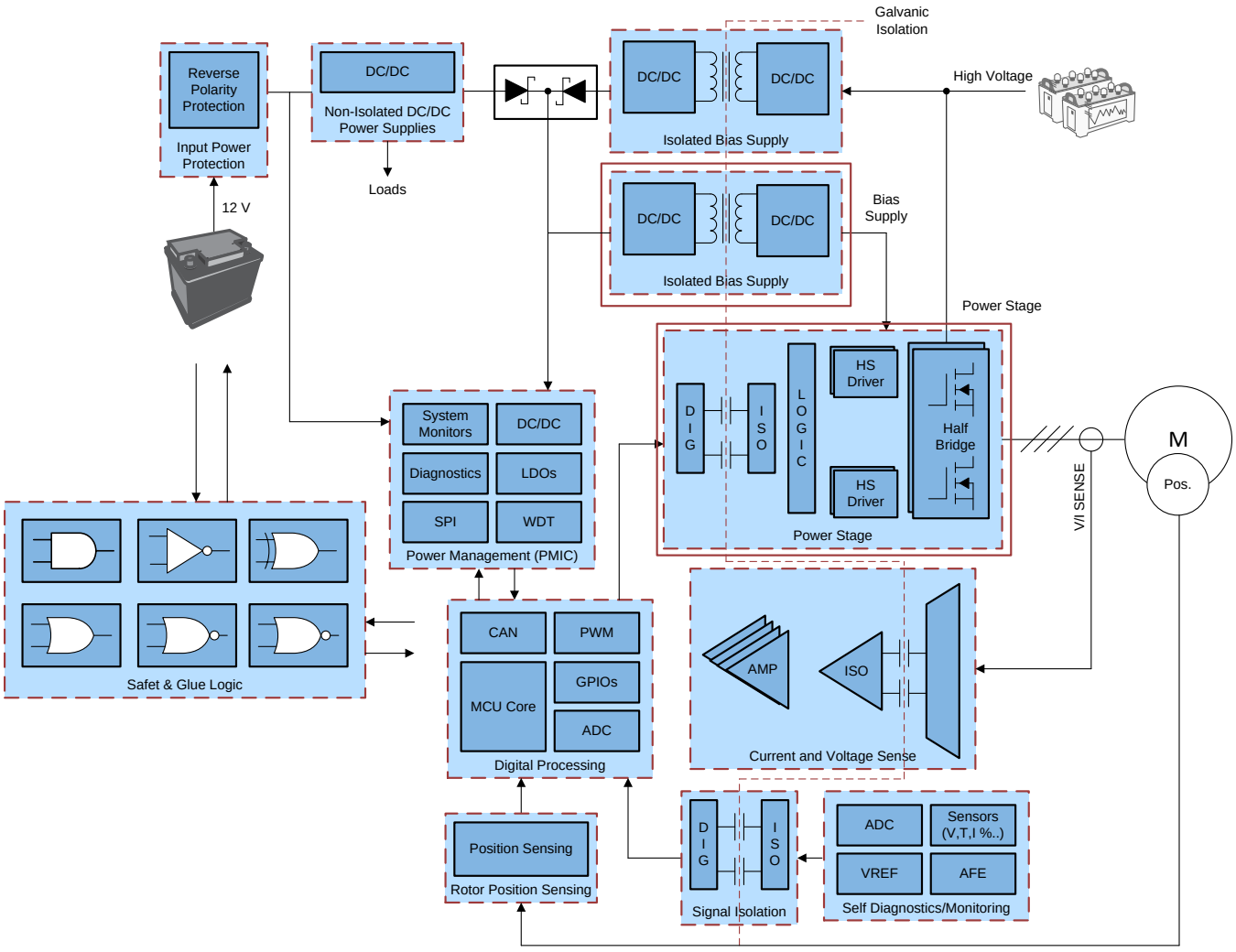
1 System Description

This reference design presents an HEV, EV traction inverter, single-phase power-stage with three bias-supply solutions. The supply solutions power a single channel of the IGBT/SiC isolated gate driver, and could be driven directly from the 12-V car battery with a wide input range of 4.5-V to 42-V DC. The bias supplies provide +15-V and –8-V isolated rails up to 180-mA output current. The architecture follows:

- Bias supply solution 1: Compact, primary-side regulated (PSR) flyback converter (based on the LM5180-Q1 device) with integrated switch and internal compensation.
- Bias supply solution 2: Low-cost, primary-side regulated (PSR) flyback converter (based on the TPS40210-Q1 device) with external switch and external compensation.
- Bias supply solution 3: Two stage approach of using two buck converters in redundancy as the front stage, and a push-pull transformer driver supply as the following stage (based on the LM46002-Q1 and SN6505-Q1 devices).

This design targets at powering IGBT/SiC isolated gate drivers implemented in hybrid electric vehicle and electric vehicle (HEV/EV) systems. 図 1 shows a traction inverter reference diagram where the positions of the TIDA-020014 design are highlighted. The isolated gate drivers galvanically isolate the high-voltage power switches from the low-voltage control signals. Each isolated gate driver requires a pair of positive-supply and negative-supply rails to fully turn on and off the IGBT/SIC power modules.

図 1. HEV/EV Traction Inverter Reference Block Diagram and the Position of TIDA-020014



Do not leave the device powered when unattended.

High voltage! There are accessible high voltages present on the board. Electric shock is possible. The board operates at voltages and currents that may cause shock, fire, or injury if not properly handled. Use the equipment with necessary caution and appropriate safeguards to avoid injury or damage to property. For safety, use of isolated equipment with overvoltage and overcurrent is highly recommended. TI considers it the user's responsibility to confirm that the voltages and isolation requirements are identified and understood before energizing the board or simulation. When energized, do not touch the design or components connected to the design.

Hot surface! Contact may cause burns. Do not touch! Some components may reach high temperatures > 55°C when the board is powered on. The user must not touch the board at any point during operation or immediately after operating, as high temperatures may be present.

1.1 Key System Specifications

表 1 details the key system specifications of the bias supplies.

表 1. Key System Specifications

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
System Input						
V_{IN}	Input voltage	Battery voltage range (DC)	4.5	13.5	42	V
F_{SW}	Switching frequency	Solution 1	10	350	350	kHz
F_{SW}	Switching frequency	Solution 2		100		kHz
F_{SW}	Switching frequency	Solution 3		450		kHz
Output Voltage						
V_{OUT1}		System output voltage, across load	+13	+15	+17	V
V_{OUT2}		System output voltage, across load	–6.5	–8	–8.2	V
Output Current						
I_{OUT}		Maximum output current. Drawing more than 180 mA is not recommended for thermal reasons. See the Thermal Images testing to see the temperature rise at full load		180		mA

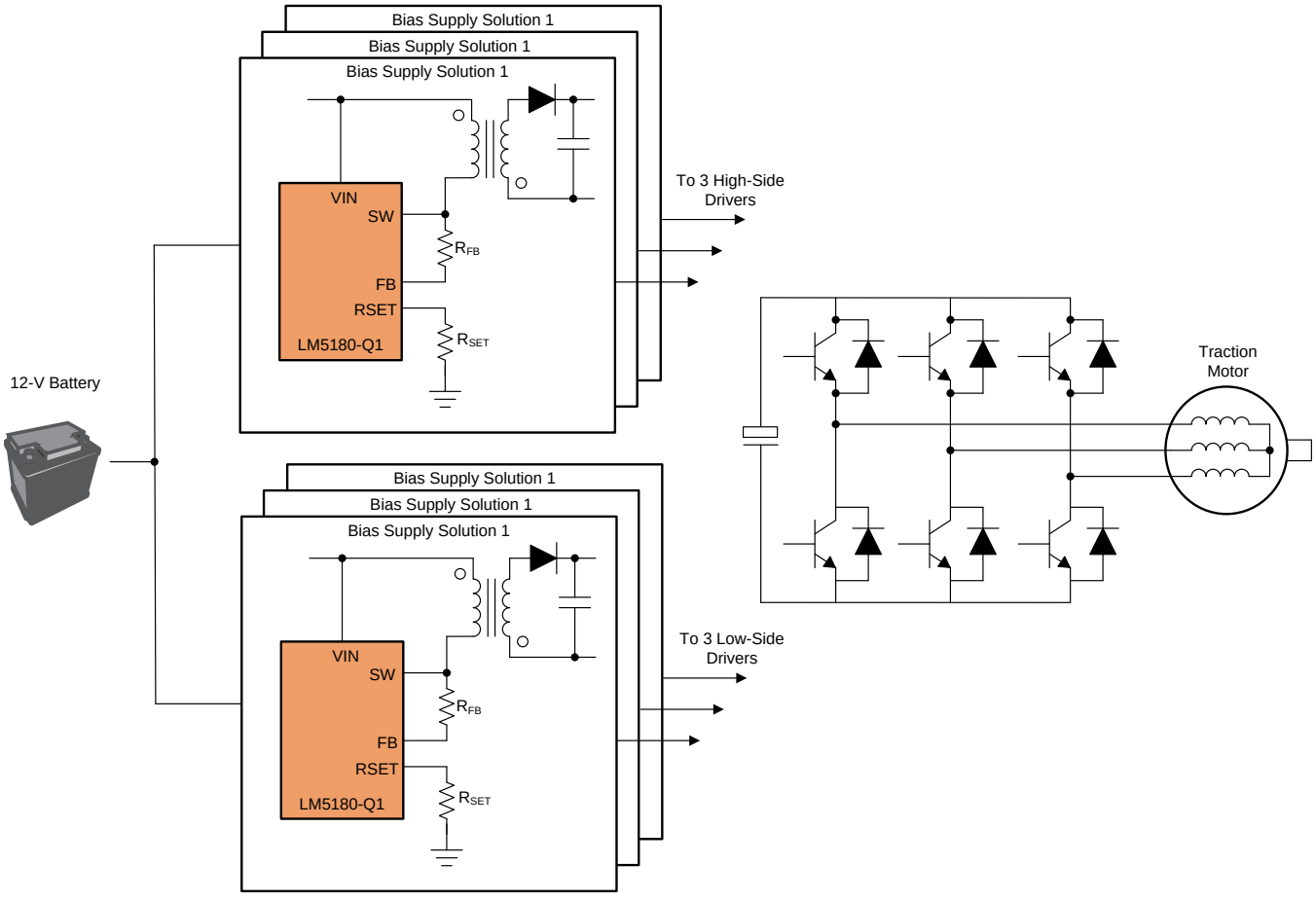
2 System Overview

2.1 Block Diagram

2.1.1 Bias Supply Solution 1

図 2 shows the system implementation block diagram of the bias supply solution 1. The three-phase traction inverter requires six IGBT/SiC switches through isolated gate drivers that galvanically isolate the high-voltage gate driver outputs from the low-voltage PWM signals. Hence six times of this design are required to power all six gate drivers: each power supply is connected to each and every gate driver, respectively. The input can be fed directly from a 12-V car battery. The output voltage levels can be configured to the required voltage levels for driving IGBT or SiC MOSFETs.

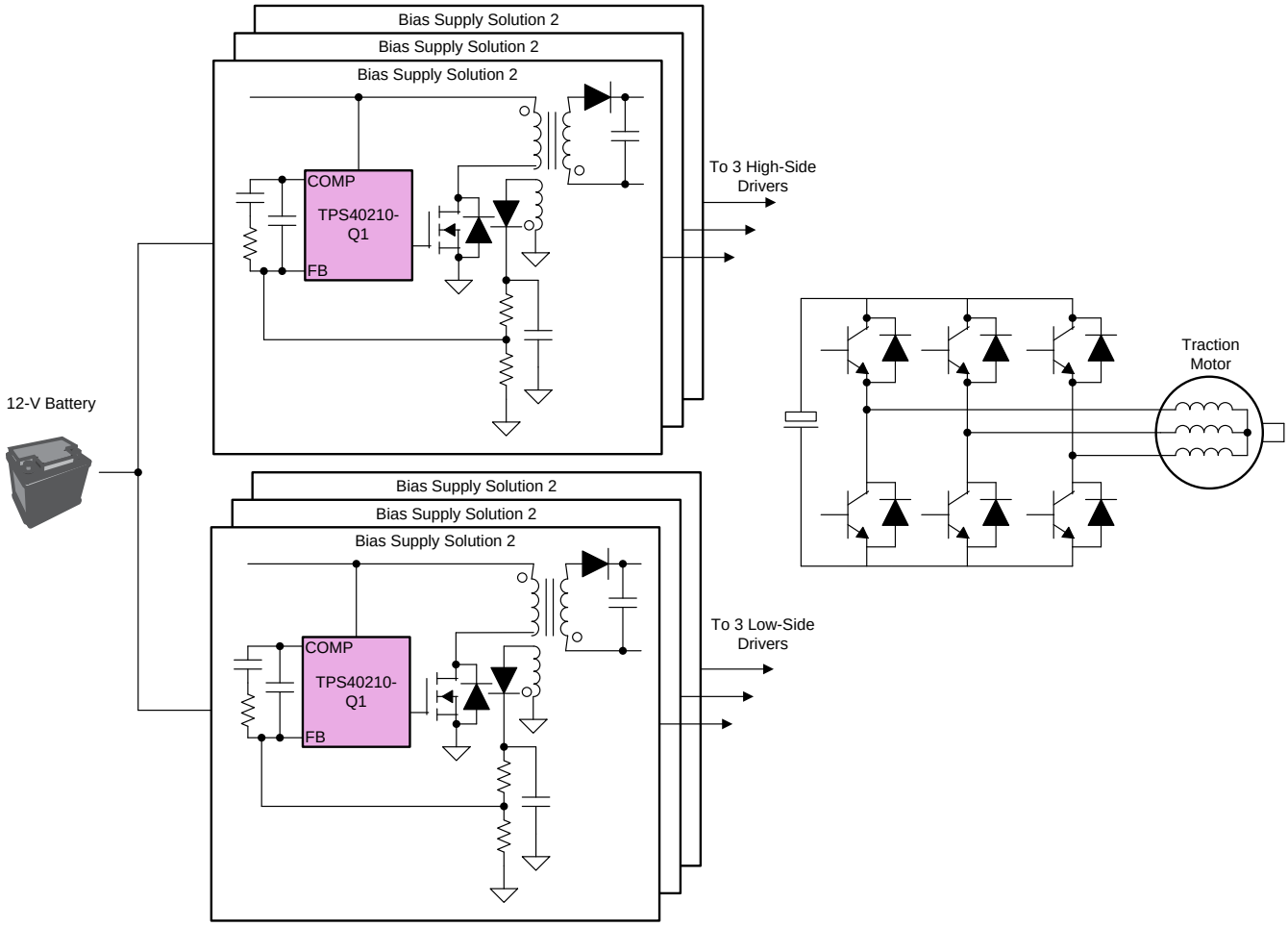
図 2. System Implementation Block Diagram of Bias Supply Solution 1



2.1.2 Bias Supply Solution 2

図 3 shows the system implementation block diagram of the bias supply solution 2. A flyback converter with an external MOSFET and compensation network has been used. The same traction inverter block diagram is shown.

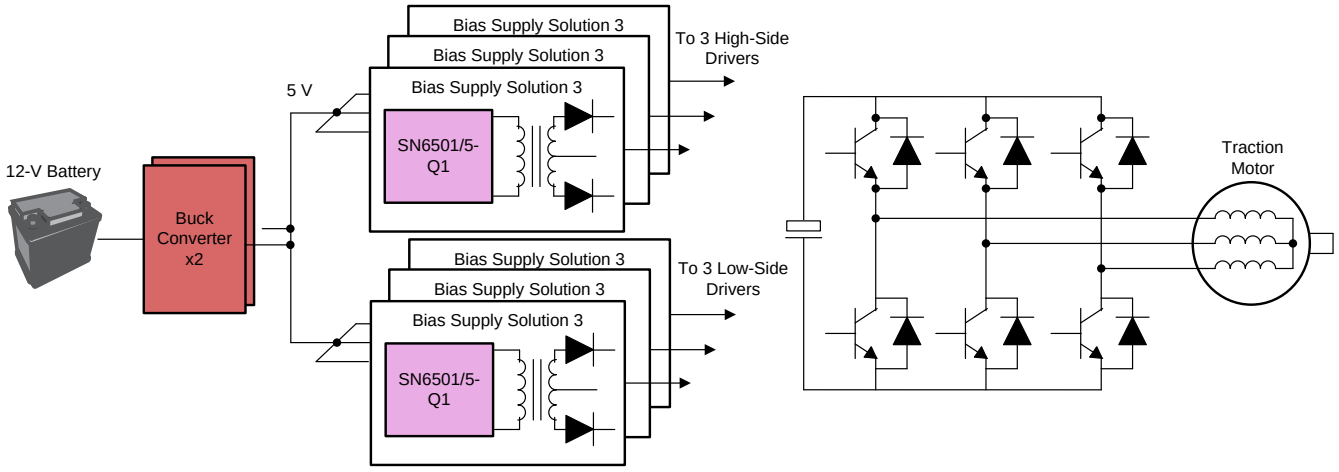
図 3. System Implementation Block Diagram of Bias Supply Solution 2



2.1.3 Bias Supply Solution 3

図 4 shows the system implementation block diagram of the bias supply solution 3 which is the two-stage architecture in redundancy for an increased level of safety. Two buck converters are connected in parallel and convert the 12-V battery input to 5-V output. Then the 5-V rail is fed into the push-pull transformer driver supply where the isolation is provided. The same traction inverter block diagram is shown.

図 4. System Implementation Block Diagram of Bias Supply Solution 3

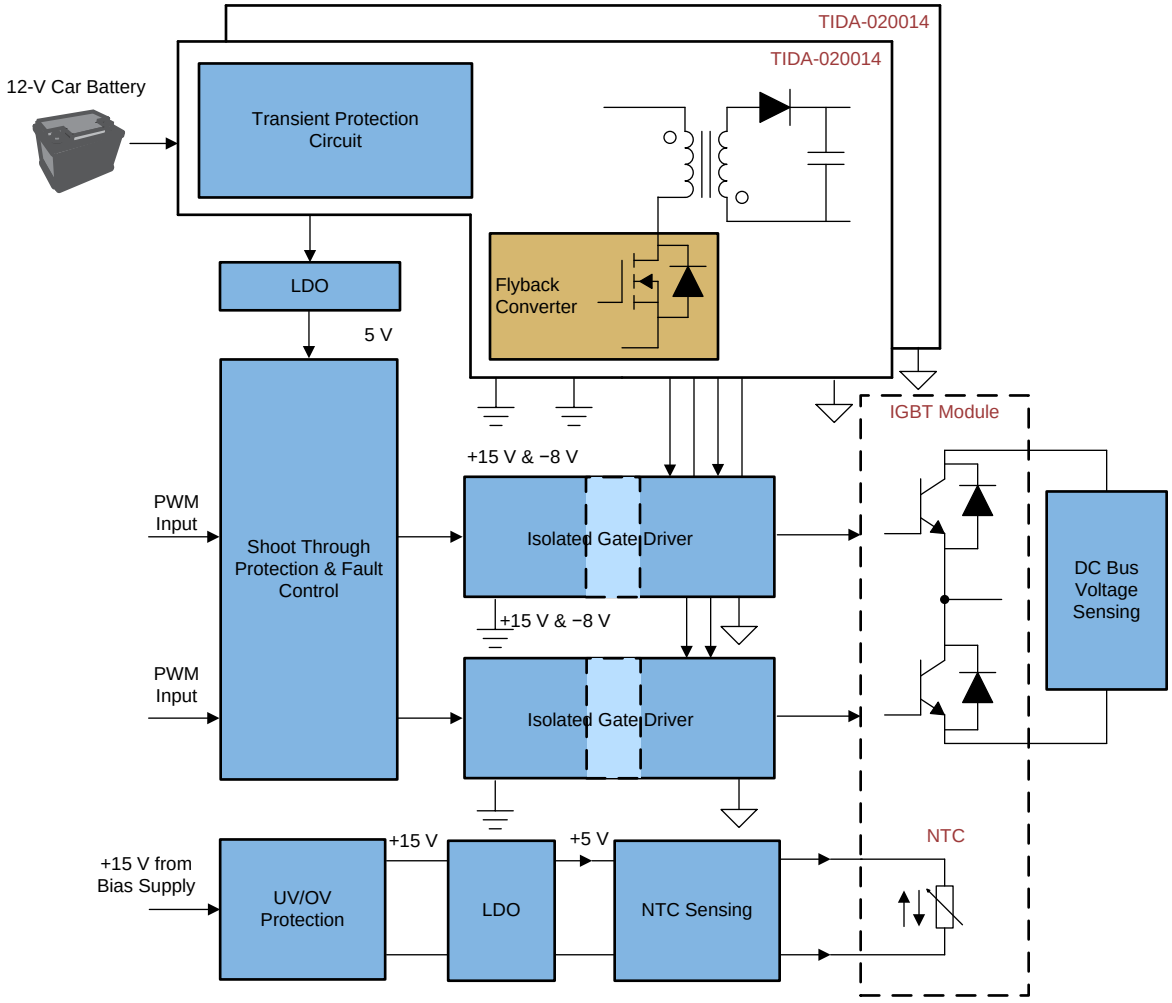


2.1.4 Inverter Power Stage Block Diagram

The power stage board is designed in a compact form factor. It includes gate drive, bias voltages, protection, and diagnostic needed for half-bridge SiC MOSFET and Si IGBT power modules housed in 150-mm × 62-mm × 17-mm packages. It consists of the high-side and low-side isolated gate drivers, the DC bus voltage sensing, the shoot-through protection and fault control, the high voltage input LDO, and the NTC sensing circuit. The connectors allow for plug-in connection to the gate drivers for easy evaluation. 図 5 shows the power stage board block diagram. The features are listed as follows:

- 20-A peak split sink and source drive current from external buffer to optimize turn on and turn off switching time
- Robust noise-immune solution with CMTI >100 V/ns
- Supports 5 kV_{RMS} reinforced isolation for input rail up to 1700 V
- Programmable short-circuit sensing and soft turn-off protection with the de-saturation circuit
- 2-A active Miller clamp
- Output short-circuit clamp
- Fault feedback with reset
- NTC temperature and DC bus voltage sensing

図 5. TIDA-020014 Power Stage Block Diagram



2.2 Highlighted Products

The TIDA-020014 reference design features the following Texas Instruments devices.

2.2.1 LM5180-Q1

The LM5180-Q1 device is a primary-side regulated (PSR) flyback converter with high efficiency over a wide input voltage range of 4.5 V to 65 V. The isolated output voltage is sampled from the primary-side flyback voltage, eliminating the need for an optocoupler, voltage reference, or third winding from the transformer for output voltage regulation. The high level of integration results is a simple, reliable and high-density design with only one component crossing the isolation barrier. Boundary conduction mode (BCM) switching enables a compact magnetic solution and better than ±1% load regulation and line regulation performance. An integrated 100-V power MOSFET provides output power up to 7 W with enhanced headroom for line transients.

2.2.2 TPS40210-Q1

The TPS40210-Q1 is a peak current-mode control low-side controller with a built in 400-mA gate driver designed to drive N-channel MOSFETs at a fixed frequency. The frequency is adjustable from 35 kHz to 1000 kHz. A small size combined with complete functionality makes the part both versatile and easy to use. The controller uses a low-value current-sensing resistor in series with the source connection of the power MOSFET to detect switching current. When the voltage drop across this resistor exceeds 150 mV, the part enters a hiccup fault mode with a time period set by the external soft-start capacitor.

2.2.3 LM74700-Q1

The LM74700-Q1 device is an ideal diode controller device that operates in conjunction with an external N-channel MOSFET as an ideal diode rectifier for low loss reverse polarity protection. The wide supply input range of 3 to 65 V allows control of many popular DC bus voltages. The device can withstand and protect the loads from negative supply voltages down to -65 V. With a low $R_{DS(on)}$ external N-channel MOSFET, a very low forward voltage drop can be achieved while minimizing the amount of power dissipated in the MOSFET.

2.2.4 TPS3700-Q1

The TPS3700-Q1 device is a wide-supply voltage window comparator which operates over a 1.8-V to 18-V range. The device has two high-accuracy comparators with an internal 400-mV reference and two open-drain outputs rated to 18 V for overvoltage and undervoltage detection. The TPS3700-Q1 device can be used as a window comparator or as two independent voltage monitors; the monitored voltage can be set with the use of external resistors.

2.2.5 LM46002-Q1

The LM46002 regulator is an easy to use synchronous step-down DC/DC converter that operates from 3.5-V to 60-V supply voltage. It is capable of delivering up to 2 A DC load current with exceptional efficiency and thermal performance in a very small solution size. An extended family is available in 0.5-A and 1.0-A load options in pin-to-pin compatible packages.

Optional features are included for more comprehensive system requirements, including power-good flag, precision enable, and synchronization to external clock, extendable soft-start time, and output voltage tracking. These features provide a flexible and easy to use platform for a wide range of applications. Protection features include over temperature shutdown, VCC undervoltage lockout (UVLO), cycle-by-cycle current limit, and short-circuit protection with hiccup mode.

2.2.6 SN6505-Q1

The SN6505-Q1 device is a monolithic push-pull transformer driver, specifically designed for small factor, isolated power supplies. It drives a low profile, center-tapped transformer from a 3.3-V or 5-V DC power supply. The SN6505x-Q1 consists of an oscillator followed by a gate drive circuit that provides the complementary output signals to drive ground referenced N-channel power switches. The device includes two 1-A Power-MOSFET switches to ensure start-up under heavy loads. The internal protection features include a 1.7-A current limiting, under-voltage lockout, thermal shutdown, and break-before-make circuitry.

2.2.7 TL431-Q1

The TL431-Q1 device is a three-pin adjustable shunt regulator with specified thermal stability over applicable automotive temperature ranges. The TL431-Q1 can be used as a single voltage reference, error amplifier, voltage clamp, or comparator with integrated reference. The TL431-Q1 consists of an internal reference and amplifier that outputs a sink current based on the difference between the reference pin and the virtual internal pin. The sink current is produced by the internal Darlington pair, which allows this device to sink a maximum current of 100 mA.

2.2.8 ISO5852S-Q1

The ISO5852S-Q1 device is a reinforced, isolated gate driver that is capable of driving a 1200-V IGBT module with current ratings from 50 A to 200 A. The device offers:

- High isolation ratings in the industry
  - 5.7-kV_{RMS} isolation voltage
  - 8000-Vpk Maximum transient isolation voltage
  - 2121-Vpk Maximum transient isolation voltage
- Split outputs
- 2.5-A Peak source and 5-A peak sink currents
- 100-kV/μs Minimum common-mode transient
- The device also includes the Miller clamp, soft turnoff, UVLO, DESAT detect, fault feedback, and Ready-status feedback features.

2.2.9 AMC1301-Q1

The AMC1301 is a fully-differential, precision, isolated amplifier. The input stage of the device consists of a fully-differential amplifier that drives a second-order, delta-sigma (ΔΣ) modulator. The modulator uses the internal voltage reference and clock generator to convert the analog input signal to a digital bit stream. The drivers transfer the output of the modulator across the isolation barrier that separates the high-side and low-side voltage domains.

2.2.10 AMC1311-Q1

The AMC1311-Q1 is a precision, isolated amplifier with an output separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced galvanic isolation of up to 7 kV peak according to VDE V 0884-11 and UL1577. Used in conjunction with isolated power supplies, this isolated amplifier separates parts of the system that operate on different common-mode voltage levels and protects lower-voltage parts from damage. The high-impedance input of the AMC1311-Q1 is optimized for connection to high-voltage resistive dividers or other voltage signal sources with high output resistance.

2.2.11 TPS7B8250-Q1

The TPS7B82-Q1 device is a 40-V_{IN}, 300-mA low-dropout linear regulator with ultra-low quiescent current. This voltage regulator consumes only 3 μA of quiescent current at light load, and is quite suitable for the automotive always on application. The device operates with a wide input-voltage range from 3 V to 40 V (45-V load dump protection).

2.3 System Design Theory

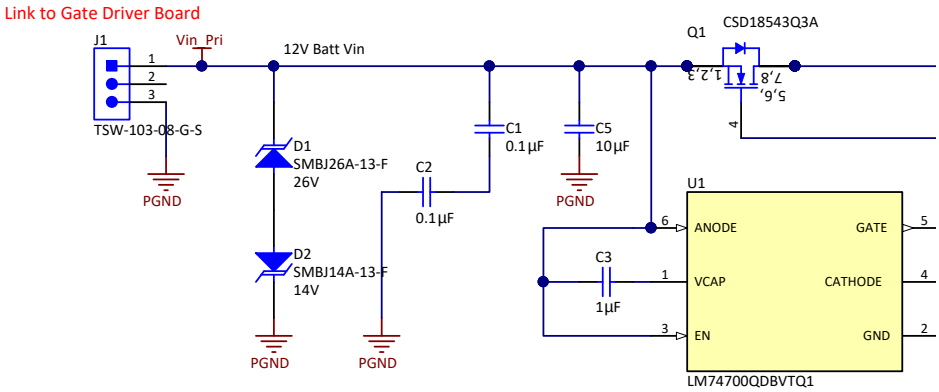
2.3.1 Reverse Polarity Protection

Reverse battery protection is required in every electronic subsystem of a vehicle, both by OEM standards, as well as ISO 16750-2, an international standard pertaining to supply quality. The goal is to prevent reverse-biasing components which are sensitive to polarity, like polarized capacitors and most integrated circuits.

図 6 shows the reverse polarity protection circuit schematic. It consists of a N-channel MOSFET (Q3) which is driven by the LM74700-Q1 smart diode controller. The traditional method which implements blocking diode results in large power dissipation due to the typical 400–700 mV forward-voltage drop. The smart diode solution decreases the losses as per the $R_{DS(on)}$ of the MOSFET. The LM74700-Q1 controller provides a gate drive for an external N-Channel MOSFET and a fast response internal comparator to discharge the MOSFET Gate in the event of reverse polarity. A unique advantage of this scheme is that it is not referenced to ground and thus has zero I_Q. The N channel MOSFET is selected according to the following criteria:

- Continuous current rating higher than 10 A which is the maximum input current at minimum input voltage in this design.
- The VGS threshold should be 2.5-V maximum
- Source-to-drain voltage V_{SD} should be at least 0.48 V at 2 A

図 6. Reverse Polarity Protection Circuit Schematic



2.3.2 LM5180-Q1 Flyback Converter

The bias supply solution 1 is the flyback converter based on the LM5180-Q1 device which has integrated MOSFET and internal compensation. The converter provides isolated output voltages with tight regulation crossing load. The design specifications are shown in 表 2. Highlights of the converter are summarized as:

- Boundary conduction mode (BCM) control architecture provides fast line and load transient response
  - Peak current-mode control
  - Quasi-resonant switching for reduced power loss
  - Internal loop compensation
- Integrated 100-V flyback power MOSFET
  - Provides large headroom for input voltage transients

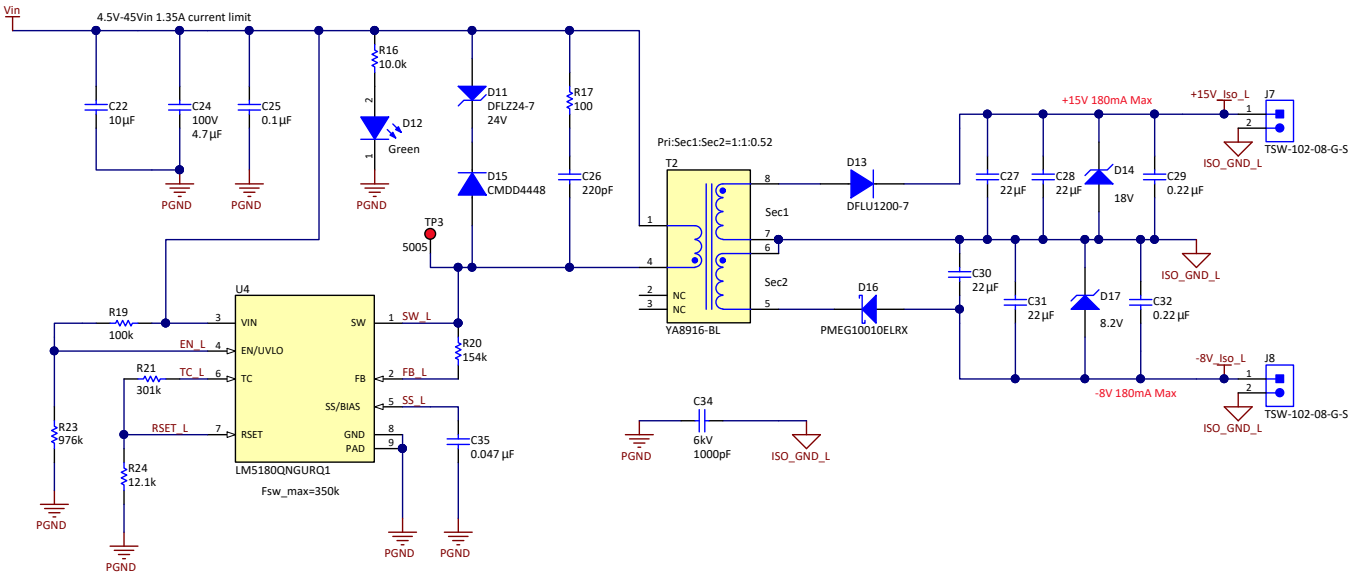
- Cycle-by-cycle overcurrent protection (OCP)
- Low transformer primary-to-secondary (inter-winding) capacitance to accommodate high dv/dt secondary-side common-mode swings.

図 7 shows the schematic of the converter.

表 2. LM5180-Q1 Based Flyback Converter Specifications

PARAMETER	SPECIFICATION
Input voltage (V_{in})	4.5 V–65 V DC (For flyback converter only, TVS limits the system input to 26 V DC)
Output voltage (V_{OUT})	+15 V, –9 V
Output ripple	±3%
Maximum output current (I_{out_max})	180 mA
Switching frequency	< 350 kHz
Output power (P_{out_max})	4.14 W
Efficiency	> 90% peak, 88% at full load

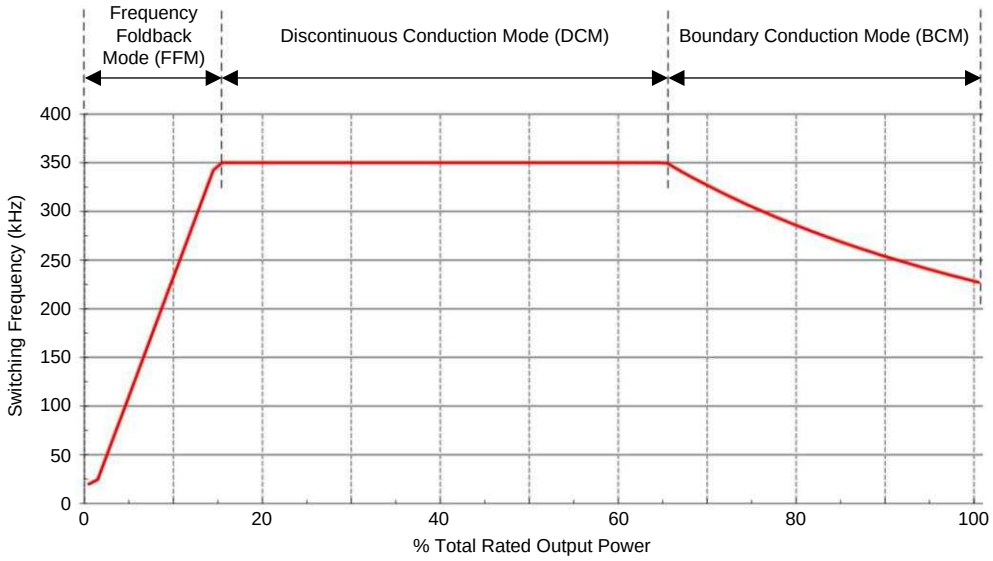
図 7. LM5180-Q1 Based Flyback Converter Schematic



2.3.2.1 Modes of Operation and Switching Frequency

The LM5180-Q1 device uses a variable-frequency, peak current-mode (VFPCM) control architecture with three possible modes of operation as 図 8 illustrates.

図 8. Operation Mode of the LM5180-Q1 Flyback Converter



At high loads, the LM5180-Q1 device operates in Quasi-Resonant Boundary Conduction Mode. The power MOSFET turns on when the current in the secondary winding reaches zero. The MOSFET turns off when the peak primary current reaches the level dictated by the output of the internal error amplifier. As the load is decreased, the peak current decreases and the frequency increases to maintain BCM operation.

2.3.2.2 Transformer Design

Key parameters to design the transformer include turns ratio, primary side inductance, switching frequency, saturation current, and so forth.

If ignoring the drop voltage across the switching MOSFET the winding turns ratio is calculated as:

$$V_{IN\_Min} \times T_{on} = (V_{OUT} + V_D) \times T_{off} \times N_{PS} \quad (1)$$

where

- V_{IN_Min} is the minimum input voltage
- T_{on} is the switch-on time of the switching MOSFET
- T_{off} is the off time of the switching MOSFET
- N_{PS} is the turns ratio of the transformer
- V_D is the output rectification diode

Considering

$$D = \frac{T_{on}}{T_{on} + T_{off}}$$

is the duty cycle, and choosing the maximum duty cycle 75% at minimum input voltage, the turns ratio of the transformer primary winding to the secondary winding is calculated as:

$$N_{PS} = \frac{V_{IN\_Min}}{V_{OUT} + V_D} \times \frac{D}{1-D} = 0.65 \quad (2)$$

Select a magnetizing inductance based on the minimum off-time constraint according to:

$$L_{MAG} \geq \frac{(V_{OUT} + V_D) \times N_{PS} \times t_{OFF\_MIN}}{I_{PRI\_PK}} = 26.5\ \mu H$$

where

- V_D is the forward drop voltage of the output rectification diode
- I_{PRI_PK} is the primary winding current when converter operates in frequency fold back mode (1.5 A according to the data sheet) (3)

The built-in MOSFET of the LM5180-Q1 device is rated at 100 V. In the off cycle, when the secondary (flyback) diode is on, the voltage on the drain (V_{DS}) is calculated as:

$$V_{DS} = V_{IN(MAX)} + V_{REF} + V_{RING} = 82\ V$$

where

- $V_{IN(MAX)}$ is the maximum input voltage
- V_{REF} is the voltage reflected from the secondary side
- V_{RING} is the excited spike due to resonance (4)

The voltage across the secondary side diode is calculated as:

$$V_{Diode} = V_{OUT} + \frac{V_{IN(MAX)}}{N_{PS}} + V_{SPIKE} = 112\ V$$

where

- V_{OUT} is the maximum output voltage
- V_{SPIKE} is the excited spike due to resonance (5)

The inductance of the transformer primarily determines the modes of operation in the LM5180-Q1 as the load is varied from the minimum load to full load. An increase in the magnetic inductance generally leads to an increase in the leakage inductance of the transformer. The LM5180-Q1 device has a minimum off-time ($T_{OFF(MIN)}$) of 500 ns: the magnetizing current should not decrease to zero in less than 500 ns. Therefore the minimum primary side inductance is calculated as:

$$L_{PRI} \geq \frac{\left(V_{out} + V_{FWD}\right) \times T_{OFF(MIN)} \times N_{PS}^2}{I_{PRI\_MIN} \times N_{PS}} = 30\ \ \mu H$$

where

- V_{OUT} is the nominal output voltage which is 24 V
- $T_{OFF(MIN)}$ is the minimum off time of LM5180-Q1
- I_{PRI_MIN} is the minimum peak current flowing at primary side for the LM5180-Q1 device which is 0.27 A
- N_{PS} is the primary to secondary turns ratio (6)

Thus, the designed transformer should have the minimum primary inductance of 30 µH. 表 3 lists the specifications of the designed flyback transformer.

表 3. Flyback Transformer Specifications

PARAMETER	SPECIFICATION
Power rating	4.2 W
Input voltage	4.5 V–65 V
Maximum output current (I_{out_max})	180 mA
Switching frequency	< 300 kHz
Maximum duty cycle	75%
Primary side inductance	30 µH ±10% at 300 kHz
Leakage inductance	< 1% of primary inductance
Parasitic capacitance primary to secondary	< 20 pF
Output voltage and current	+15 V and –9 V at 180-mA average current

表 3. Flyback Transformer Specifications (continued)

PARAMETER		SPECIFICATION
Turns ratio		1:1:0.52
Peak current	Primary	1.45 A
	Secondary	1 A
RMS current	Primary	1.1 A
	Secondary	380 mA

TI recommends the flyback transformer UA8916-BL from CoilCraft® for the LM5180-Q1-based flyback converter. The transformer features parasitic capacitance of 17 pF from the primary to secondary side.

2.3.2.3 Input Capacitors

The input capacitor must supply the input current during the input voltage dip from the 12-V battery. Input capacitors are essential in limiting the ripple voltage while supplying most of the switch current during the MOSFET switch on-time.

The input capacitance is calculated as:

$$C_{in} = \frac{I_{pri\_pk} \times D_{on}}{F_{SW} \times \Delta V_{ripple}} = \frac{1.45\ A \times 0.75}{300\ k \times 4.5\ V \times 3\%} = 26.8\ \mu F \quad (7)$$

2.3.2.4 Output Capacitors

The output capacitance ensures the converter has a small transient deviation to a step change of the load transient. The minimum needed capacitance is calculated as to maintain the output voltage drop less than 3% of the nominal voltage when the output current changes abruptly from the maximum to half (I_{step}):

$$I_{step} = \frac{I_{out}}{2} = \frac{180\ mA}{2} = 90\ mA \quad (8)$$

$$V_{drop} = V_{out} \times 3\% = 24\ V \times 1\% = 0.24\ V \quad (9)$$

As any forward converters, the Right-Half-Plan-Zero (RHPZ) limits the bandwidth of the flyback. The frequency of the RHPZ is calculated as:

$$f_{RHPZ} = \frac{R_{OUT} \times (V_{in} / V_{out})^2}{L_{PRI} \times 2\pi} = 24.8\ kHz$$

where

- R_{OUT} is the load impedance
- L_{PRI} is the primary inductance of the transformer (10)

The bandwidth of the system is estimated as 1/5 of the RHPZ:

$$f_{bandwidth} = \frac{1}{5} \times f_{RHPZ} = \frac{1}{5} \times 24.8\ kHz = 4.96\ kHz \quad (11)$$

As the result, the output capacitance at bandwidth frequency is calculated as:

$$C_{out\_min} = \frac{1}{2 \times \pi \times f_{bandwidth}} \times \frac{1}{\Delta V_{out} / \Delta I_{loadstep} - ESR_{out}} = 12\ \mu F \quad (12)$$

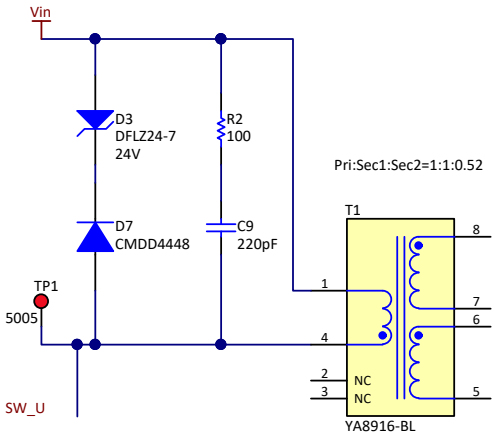
Therefore a minimum of 12-µF capacitance is required for this design.

2.3.2.5 RC Snubber Design

When the MOSFET turns off, a high-voltage spike occurs at the drain (switch node) because of the resonances between the leakage inductor of the main transformer and the parasitic capacitance in the circuit. This causes excessive voltage on the drain of the MOSFET which can lead to breakdown and eventually failure of the device. The parasitic capacitance is composed of 3 components: (1) output capacitance of the MOSFET, (2) junction capacitance of the output diode which reflects to the primary side, (3) parasitic capacitance of the transformer winding.

The transformer used in this design has relatively less leakage inductance. A Zener clamp is used in this reference design as 図 9 shows, due to ease-of-design and higher light load efficiency than the RCD snubber.

図 9. Snubber Circuit Schematic



The power dissipated in the snubber can be calculated as:

$$P_{sub} = \frac{1/2 \times L_{LK} \times I_{PK}^2 \times F_{SW}}{1 - V_{FBK}/V_{Ze}} \quad (13)$$

where

- L_{Lk} is the leakage inductance of the transformer
- I_{PK} is the primary peak current
- F_{SW} is the switching frequency
- The Zener diode is selected as 24 V

2.3.2.6 Verification on Input Voltage Range

The LM5180-Q1 device integrates a 100-V power MOSFET with maximum current of 1.5 A. The maximum drain-to-source voltage (V_{ds_max}) is calculated as:

$$V_{ds\_max} = n \times \frac{N_p}{N_s} \times (V_{out} + V_f) + V_{in\_max} = 102.5 \ \ V \quad (14)$$

where

- n is the safe margin which is normally 1.5 or 2 times of the nominal value.
- N_p/N_s is the turn ratio of the transformer primary winding to the secondary winding.
- V_{OUT} is the output voltage
- V_f is the forward voltage of the output diode
- V_{IN_max} is the maximum input voltage

Therefore, the selected MOSFET breaking voltage must be larger than 102.5 V.

2.3.2.7 LM5180-Q1 Settings

図 10 shows the schematic with components surrounding the LM5180-Q1 device. The UVLO is connected to V_{IN} directly for the lowest undervoltage lockout. With the designed turns ratio of the transformer and forward voltage of the secondary diode, the ratio between R20 (R_{FB}) and R24 (R_{RST}) determines the output voltage. R24 (R_{RST}) is selected as 12.1 kΩ according to the data sheet. The output voltage is 24 V, the forward voltage drop of the secondary diode is 0.7 V. R_{FB} is calculated as:

$$R_{FB} = \frac{(V_{OUT} + V_{FD}) \times N_{PS}}{0.1\ mA} = 154\ \ k\Omega \tag{15}$$

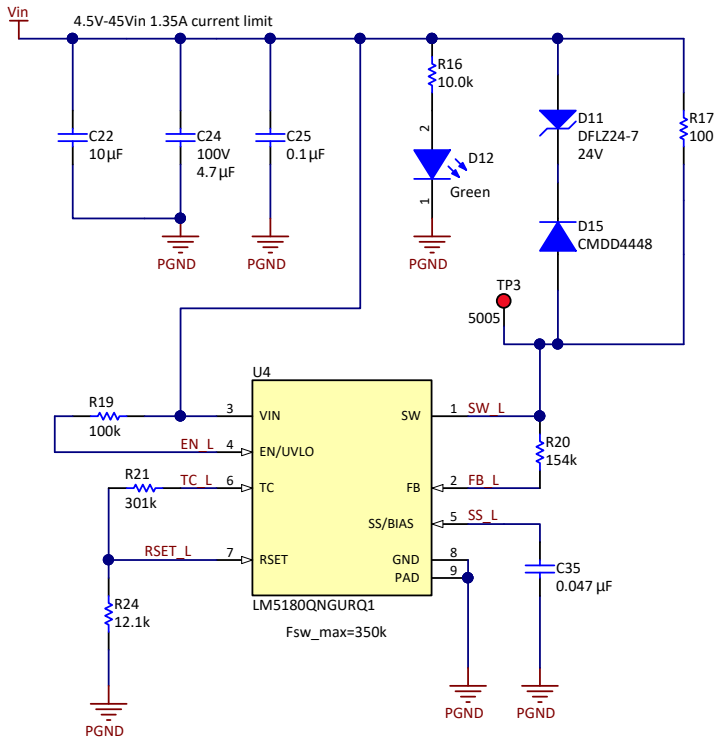
The LM5180-Q1 device employs a thermal-compensation circuit that adjusts the feedback reference based on the forward voltage thermal coefficient of the flyback diode. The thermal compensation resistor value is determined by R21 (R_{TC}) which is calculated as:

$$R_{TC} = \frac{R_{FB}}{N_{PS}} \times \frac{3\ mV/°C}{TC_{Diode}} = 301\ \ k\Omega \tag{16}$$

where

- TC_{Diode} is the absolute value of the temperature coefficient of the flyback diode

図 10. LM5180-Q1 Settings Schematic



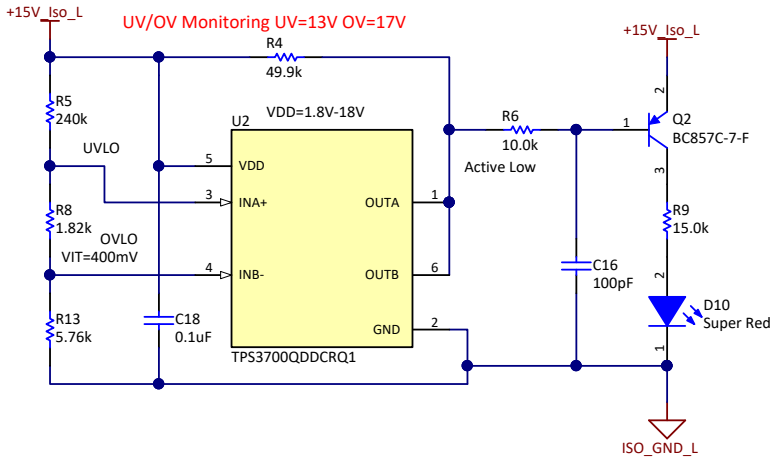
2.3.3 Overvoltage and Undervoltage Detection

The IGBT gate is driven from the 15-V rail to turn on the IGBT. The 15-V rail should not drop below the minimum gate voltage to properly turn on the IGBT. Driving the IGBT with lower gate voltage causes excessive power dissipation. Conversely, excessive higher gate voltage will destroy the IGBT.

The overvoltage and undervoltage detection is designed with the window comparator TPS3700-Q1. It has two high-accuracy comparators with an internal 400-mV reference and two open-drain outputs. 図 11 shows the schematic of the detection circuit. The INA+ / INB– implements open-drain output. OUTA is driven low when the voltage at INA+ is below ($V_{ITP} - V_{HYS}$) (according to the TPS3700-Q1 data sheet). The output goes high when the sense voltage returns above the respective threshold. OUTB is driven low

when the voltage at this comparator exceeds V_{ITP}. The output goes high when the sense voltage returns below the respective threshold. The undervoltage threshold is set as 13 V, and the overvoltage threshold is set as 17 V for this design. The OR logic is implemented by connecting the two open-drain outputs of the TPS3700-Q1 device. OUTA and OUTB can merge into one logic signal that goes low if either output is asserted. The 49.9-kΩ pullup resistor is used to hold these lines high when the output goes to high impedance.

図 11. Overvoltage and Undervoltage Detection Schematic



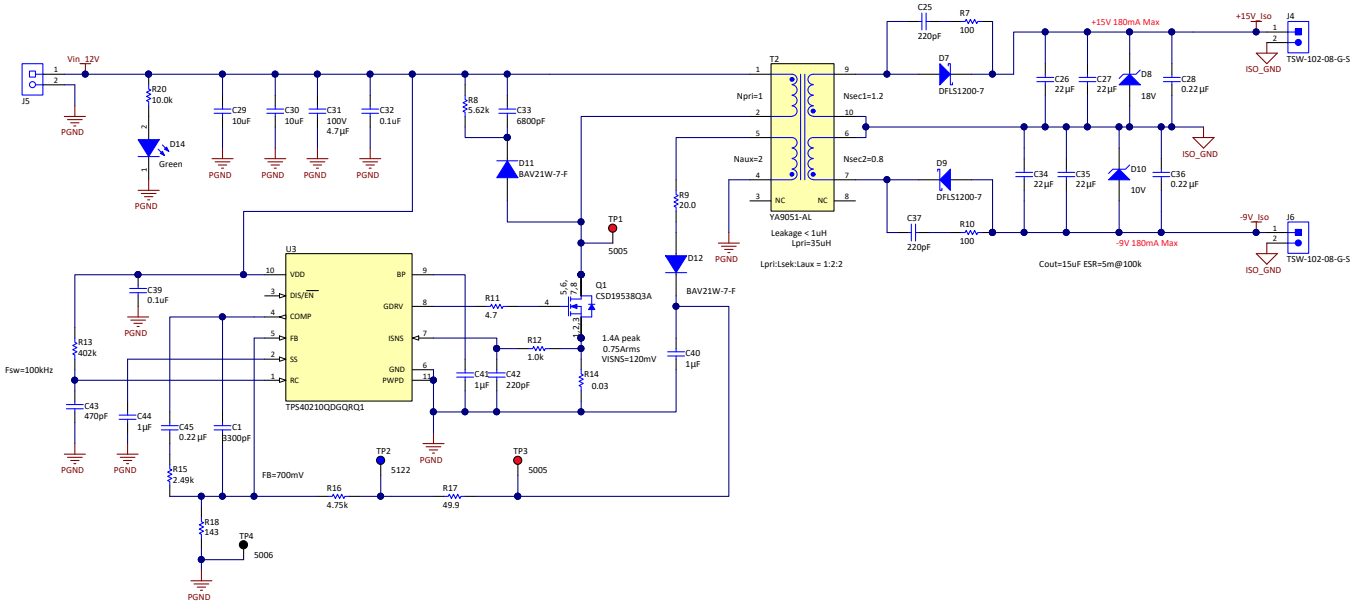
2.3.4 TPS40210-Q1 Flyback Converter

The bias supply solution 2 is the flyback converter based on the TPS40210-Q1 device which implements external MOSFET and primary side regulation. The procedure and calculations for designing the flyback converter are discussed in this section. 表 4 lists the design specification.

表 4. TPS40210-Q1 Based Flyback Converter Specifications

PARAMETER	SPECIFICATION
Input voltage (V_{IN})	5 V–42 V DC (52-V transient)
Output voltage (V_{OUT})	+15 V, –9 V
Output ripple	±3%
Maximum output current (I_{out_max})	180 mA
Switching frequency	100 kHz
Output power (P_{out_max})	4.14 W
Efficiency	> 81% peak, 80% at full load

図 12. TPS40210-Q1 Flyback Converter Schematic



2.3.4.1 Switching Frequency

The oscillator frequency is determined by a resistor and capacitor connected to the RC pin of TPS40210-Q1 device. A switching frequency of 100 kHz is selected as a compromise between component size, EMI, and efficiency. The required resistor for a given oscillator frequency is calculated from:

$$R_T = \frac{1}{5.8\times10^{-8}\times F_{SW}\times C_T + 8\times10^{-10}\times F_{SW}^2 + 1.4\times10^{-7}\times F_{SW} - 1.5\times10^{-4} + 1.7\times10^{-6}\times C_T - 4\times10^{-9}\times C_T^2} \quad (17)$$

where

- R_T is the timing resistance in kΩ
- F_{SW} is the switching frequency in kHz
- C_T is the timing capacitance in pF

C_T and R_T are selected as 470 pF and 402 kΩ, respectively for the 100-kHz switching frequency.

2.3.4.2 Transformer Design

A transformer is one of the most important elements to ensure the flyback converter operates reliably and efficiently. A flyback transformer is used as an energy storage device. The energy is stored in the air-gap of the core. The flyback converter is designed for continuous-conduction mode. In comparison with the discontinuous mode, the advantages are lower peak currents, lower output voltage spikes, and lower core losses.

If ignoring the drop voltage across the switching MOSFET, and output rectification diode, the winding turns ratio is calculated as:

$$V_{IN\_Min}\times T_{on} = V_{OUT}\times T_{off}\times N_{PS} \quad (18)$$

where

- V_{IN_Min} is the minimum input voltage
- T_{on} is the switch-on time of the switching MOSFET
- T_{off} is the off time of the switching MOSFET
- N_{PS} is the turn ratio between the primary turns and secondary turns of the transformer.

Considering:

$$D = \frac{T_{on}}{T_{on} + T_{off}}$$

is the duty cycle, and choosing the maximum duty cycle as 70%. Therefore, the turn ratio of the transformer primary winding to the secondary winding is calculated as:

$$N_{PS} = \frac{V_{IN\_Min}}{V_{OUT}} \times \frac{D}{1-D} = 0.49 \quad (19)$$

Hence, N_{PS} is selected as 1:2. The actual duty cycle (D_{ON_act}) is calculated as:

$$D_{ON\_act} = \frac{(V_{out} + V_f) \times N_{PS}}{V_{IN\_min} + (V_{out} + V_f) \times N_{PS}} = 0.71$$

where

- V_f is the forward drop voltage of the output rectification diode (20)

The turn-off time duty cycle of the MOSFET is calculated as:

$$D_{OFF\_act} = 1 - D_{ON\_act} = 0.29 \quad (21)$$

The average peak current (I_{sec_avgpk}) at the transformer secondary side is:

$$I_{sec\_avgpk} = I_{sec\_avg} / D_{OFF\_act} = 180\ mA / 0.29 = 620\ mA \quad (22)$$

The peak current at the transformer secondary side (I_{sec_pk}) is calculated as:

$$I_{sec\_pk} = \frac{2 \times I_{sec\_avgpk}}{2 - D_{OFF\_act}} = 0.73\ A \quad (23)$$

The average current flowing into the transformer secondary side is 180 mA. Therefore, the RMS current at the transformer secondary side (I_{sec_rms}) is calculated as:

$$I_{sec\_rms} = I_{sec\_avgpk} \times \sqrt{D_{OFF\_act}} = 0.39\ A \quad (24)$$

The average peak current (I_{pri_avgpk}) at the transformer primary side is calculated as:

$$I_{pri\_avgpk} = \frac{I_{sec\_avgpk}}{N_{PS}} = \frac{0.73\ A}{0.5} = 1.46\ A \quad (25)$$

The peak current at the transformer primary side (I_{pri_pk}) is calculated as:

$$I_{pri\_pk} = \frac{2 \times I_{pri\_avgpk}}{2 - D_{on\_act}} = \frac{2 \times 1.46\ A}{2 - 0.3} = 1.72\ A \quad (26)$$

The RMS current at the transformer primary side (I_{pri_rms}) is calculated as:

$$I_{pri\_rms} = I_{pri\_avgpk} \times \sqrt{D_{On\_act}} = 1.46 \times \sqrt{0.71} = 1.23\ A \quad (27)$$

The RMS current of the bias winding is selected as 50 mA according to the current limit of the internal regulator. The turn ratio of the transformer bias winding to the secondary winding is selected as 1:1 for better regulation. As the result, output voltage of the bias winding is Vbias = V_{OUT} = 24 V.

表 7 details the specifications of the designed flyback transformer.

表 5. Flyback Transformer Specifications

PARAMETER	SPECIFICATION
Qualification	AEC-Q200 Grade 1 qualified
Safety insulation	Reinforced
Power rating	4.2 W
Input voltage	4.5 V–42 V
Switching frequency	100 kHz
Maximum output current (I_{out_max})	180 mA
Maximum duty cycle	71%

表 5. Flyback Transformer Specifications (continued)

PARAMETER		SPECIFICATION
Primary-side inductance		35 µH ±10% at 100 kHz
Leakage inductance		< 2% of primary inductance
Parasitic capacitance primary to secondary		< 20 pF
Output voltage and current		24 V at 180 mA average current
Auxiliary winding output		24 V at 50 mA
Turns ratio (Pri:Sec:Aux)		1:2:2
Peak current	Primary	1.72 A
	Secondary	0.8 A
RMS current	Primary	1.2 A
	Secondary	350 mA

TI recommends the automotive grade AEC-Q200 qualified flyback transformer YA9051-AL from CoilCraft for the TPS40210-Q1-based design. The transformer features parasitic capacitance of 20 pF from primary to secondary side.

2.3.4.3 Input Capacitors

The input capacitor must supply the input current during the input voltage dip from the 12-V battery. Input capacitors are essential in limiting the ripple voltage while supplying most of the switch current during the MOSFET switch on-time.

The input capacitance is calculated from 6-V minimum input voltage with 10% ripple:

$$C_{in} = \frac{I_{pri\_pk} \times D_{on}}{F_{SW} \times \Delta V_{ripple}} = \frac{1.72\ A \times 0.75}{100\ k \times 6\ V \times 10\%} = 20\ \mu F \quad (28)$$

2.3.4.4 Output Capacitors

The output capacitance ensures the converter have a small transient deviation to a step change of the load transient. The minimum needed capacitance is calculated as to maintain the output voltage drop less than 3% of the nominal voltage when the output current changes abruptly from the maximum to half (I_{step}):

$$I_{step} = \frac{I_{out}}{2} = \frac{180\ mA}{2} = 90\ mA \quad (29)$$

$$V_{drop} = V_{out} \times 3\% = 24\ V \times 1\% = 0.24\ V \quad (30)$$

As any forward converters, the RHPZ limits the bandwidth of the flyback. The frequency of the RHPZ is calculated as:

$$f_{RHPZ} = \frac{R_{OUT} \times (V_{in} / V_{out})^2}{L_{PRI} \times 2\pi} = 24.8\ kHz$$

where

- R_{OUT} is the load impedance
- L_{PRI} is the primary inductance of the transformer (31)

The bandwidth of the system is estimated as 1/5 of the RHPZ:

$$f_{bandwidth} = \frac{1}{5} \times f_{RHPZ} = \frac{1}{5} \times 24.8\ kHz = 4.96\ kHz \quad (32)$$

As the result, the output capacitance at bandwidth frequency is calculated as:

$$C_{out\_min} = \frac{1}{2 \times \pi \times f_{bandwidth}} \times \frac{1}{\Delta V_{out} / \Delta I_{loadstep} - ESR_{out}} = 12\ \mu F \quad (33)$$

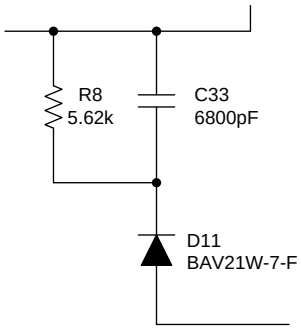
Therefore, a minimum of 12-µF capacitance is required for this design.

2.3.4.5 RC Snubber Design

When the MOSFET turns off, a high-voltage spike occurs at the drain (switch node) because of the leakage inductor of the main transformer and the parasitic capacitance in the circuit. The parasitic capacitance is composed of 3 components: (1) output capacitance of the MOSFET, (2) junction capacitance of the output diode which reflects to the primary side, (3) parasitic capacitance of the transformer winding.

As the result, implementation of an RC snubber circuit is very important to avoid MOSFET from avalanche breakdown and damage. 図 13 shows the schematic of the RC snubber circuit.

図 13. RC Snubber of the TPS40210-Q1 Flyback DC/DC Converter



Voltage rating of the damping capacitance is calculated as:

$$V_{SN} = 3 \times n \times V_{out} = 3 \times 0.5 \times 24\ V = 36\ V \quad (34)$$

The damping resistance (R_{SN}) is calculated as:

$$R_{SN} = \frac{V_{SN}^2}{\frac{1}{2} \times L_{lk1} \times i_{pri\_pk}^2 \times \frac{V_{SN}}{V_{SN} - n \times V_{out}} \times F_{SW}} = 8.3\ k\Omega \quad (35)$$

where

- L_{lk1} is the leakage inductance of the primary side
- I_{pri_pk} is the peak current flowing into the transformer primary side
- V_{SN} is the voltage across the snubber capacitor. It is determined at the minimum input load and full-load condition.
- F_{SW} is the switching frequency of the converter
- n is the turns ratio of the transformer primary to the secondary
- V_{OUT} is the output voltage

A 5.6-kΩ resistor is selected for higher power dissipation. The power rating of the damping resistor is calculated as:

$$P_{RSN} = \frac{V_{SN}^2}{R_{SN}} \times D = \frac{36\ V^2}{5.6\ k\Omega} \times 0.2 = 0.05\ W \quad (36)$$

where

- V_{SN} is the voltage across the snubber capacitor. It is determined at the minimum input load and full-load condition.
- D is the maximum duty cycle of the voltage spike.

The damping capacitance is calculated as:

$$C_{SN} = \frac{V_{SN}}{DV_{SN} \times R_{SN} \times F_{SW}} = \frac{36\ V}{36\ V \times 15\% \times 5.6\ k\Omega \times 100\ kHz} = 11\ nF \quad (37)$$

The higher the damping capacitance is, the lower the voltage spike is, and the longer the voltage spike duration will be.

Current flow through the freewheeling diode (D2) is calculated as:

$$i_D = C_{SN} \times \frac{dv}{dt} = 6.8\ nF \times \frac{42\ V + 0.5 \times 24\ V}{0.3 \times \frac{1}{100\ kHz}} = 0.12\ A \quad (38)$$

A Schottky diode with 200-V reverse blocking voltage, 0.2-A average current, and 2.5-A repetitive current flow is chosen in this design.

2.3.4.6 Selection of MOSFETs

Selection of the MOSFET is very important for a high efficient, size optimized, and thermally enhanced power supply design. The MOSFET drain-to-source breakdown voltage must be higher than the voltage imposed on the switch node. The maximum drain-to-source voltage (V_{ds_max}) is calculated as:

$$V_{ds\_max} = n \times \frac{N_p}{N_s} \times (V_{out} + V_f) + V_{in\_max} = 66.7\ V \quad (39)$$

where

- n is the safe margin which is normally 1.5 or 2 times of the nominal value
- N_p/N_s is the turn ratio of the transformer primary winding to the secondary winding
- V_{OUT} is the output voltage
- V_f is the forward voltage of the output diode
- V_{IN_max} is the maximum input voltage

Therefore, a MOSFET with maximum drain-to-source voltage rating larger than 66.7 V must be chosen. Calculations on losses are done at the 12-V nominal input because this is the condition under which the MOSFET mostly works. Four components must be taken into account when selecting the MOSFET:

- On-state conduction losses
- Gate driver losses
- Switching losses
- Output capacitance losses

The CSD19538Q3A, 100-V, 15-A MOSFET is selected for this reference design. The conduction losses of the MOSFET (P_{on}) are calculated as:

$$P_{on} = I_D^2 \times R_{DS(on)} \times D_{on} = (0.63\ A)^2 \times 59\ m\Omega \times 46.5\% = 0.01\ W \quad (40)$$

where

- I_D is the conducting current during the turn-on of the switch
- $R_{DS(on)}$ is the channel resistance when the switch is turned on
- D_{on} is the duty cycle at 12-V input

The gate driver losses (P_{drive}) are calculated as:

$$P_{drive} = Q_g \times V_{driver} \times F_{SW} = 4.3\ nC \times 8\ V \times 100\ kHz = 0.003\ W \quad (41)$$

where

- Q_g is the gate charge
- V_{driver} is the gate driver voltage
- F_{SW} is the switching frequency

Switching losses of the MOSFET (P_{SW}) are calculated as:

$$P_{SW} = \frac{1}{2} \times F_{SW} \times (V_{DSr} \times t_r \times I_{on} + V_{DSf} \times t_{off} \times I_{off}) = 0.02\ W$$

where

- V_{DSr} is the drain-to-source voltage when MOSFET is switching at rising edge
- V_{DSf} is the drain-to-source voltage when MOSFET is switching at falling edge
- F_{SW} is the switching frequency

- t_r is the switching rise time
- I_{on} is the current built up level during turn on
- t_{off} is the switching fall time
- I_{off} is the current level at the moment of turn off

(42)

The output capacitance losses (P_{coss}) are calculated as:

$$P_{coss} = \frac{1}{2} \times C_{oss} \times V_{DS}^2 \times F_{SW} = 0.003 \text{ W}$$

where

- C_{oss} is the output capacitance of the MOSFET
- V_{DS} is the Drain-to-Source voltage when MOSFET is switching
- F_{SW} is the switching frequency

(43)

Therefore, the total losses in the MOSFET are calculated as:

$$P_{total} = P_{on} + P_{SW} + P_{coss} = 0.01 \text{ W} + 0.02 \text{ W} + 0.003 \text{ W} = 0.023 \text{ W} \quad (44)$$

2.3.5 Buck Converter

The bias supply solution 3 implements a buck converter as the front stage and a push-pull transformer driver supply as the following stage. The synchronous step-down DC/DC converter LM46002-Q1 with integrated switch is selected as the front stage. It is capable of driving up to 2 A of load current from an input voltage ranging from 3.5 V to 60 V.

2.3.5.1 Switching Frequency

The switching frequency can be programmed by the impedance R_T from the RT pin to ground. The frequency is inversely proportional to the R_T resistance. The LM46002-Q1 device is operated at 480-kHz switching frequency in this design. R_T is calculated as:

$$R_T = \frac{40200}{F_{SW}} - 0.6 = 83.2 \text{ k}\Omega \quad (45)$$

2.3.5.2 Output Inductor

The buck converter inductance is calculated according to the switching frequency. The selected value compromises between the size of the inductor and the peak-to-peak output ripple current. A higher inductance gives lower ripple current, which then gives a lower output voltage ripple with the same output capacitors. An inductance that gives a ripple current of 20% to 40% at the maximum current is a good starting point. The minimum inductor value is calculated based on input voltage range, output voltage, maximum output current, and the switching frequency:

$$\frac{(V_{IN} - V_{OUT}) \times D}{0.4 \times F_{SW} \times I_{OUT}} \le L_{min} \le \frac{(V_{IN} - V_{OUT}) \times D}{0.2 \times F_{SW} \times I_{OUT}}$$

where

- V_{IN} is the maximum input voltage in 12-V battery nominal condition
- V_{OUT} is the output voltage
- F_{SW} is the switching frequency
- I_{OUT} is the output current
- D is the duty cycle at 16-V input

(46)

Hence, the calculated inductance is between 10µH and 20µH. For this design, 18-µH inductance is chosen. Besides the inductor size, the rated saturation current needs to be specified as:

$$I_{Ripple} = \frac{(V_{IN} - V_{OUT}) \times D}{L \times F_{SW}} \quad (47)$$

$$I_{L-peak} = I_{OUT} + \frac{I_{Ripple}}{2} \quad (48)$$

Hence, the inductor peak current is calculated as 3.6 A. The MSS1260-183MLB from Coilcraft with 5.22-A saturation current rating is selected for this design. A good practice is to use an inductor with the saturation current around 1.5 to 2 times higher than calculated.

In general, it is preferable to choose lower inductance in switching power supplies, because it usually corresponds to faster transient response, smaller DCR, and reduced size. However, inductance that is too low leads to high-output voltage ripple with the same output capacitance. It also generates more conduction loss because the RMS current is slightly higher relative that with a lower current ripple at the same DC current. As the LM46002-Q1 device implements peak current mode control, it is not recommended to have too small of an inductor current ripple. Enough of an inductor current ripple improves the signal-to-noise ratio on the current comparator and makes the control loop more immune to noise.

2.3.5.3 Output Capacitors

The value of output capacitors are calculated based on the maximum desired output voltage ripple, and the transient response:

$$C_{OUT} \geq \frac{1}{F_{SW} \times \frac{\Delta I_L}{I_{OUT}} \times \frac{\Delta V_{OUT}}{\Delta I_{OUT}}} \times \left[\frac{\Delta I_L}{I_{OUT} \times 12} \times (1 + (1 - D)) + (1 - D) \times \left(1 + \frac{\Delta I_L}{I_{OUT}}\right) \right]$$

where

- ΔI_{OUT} is the load step change
- ΔV_{OUT} is the target output voltage undershoot
- ΔIL is the inductor ripple current
- I_{OUT} is the output current

(49)

As a result, the output capacitance should be larger than 20 µF. Two 22-µF ceramic capacitors are connected in parallel to meet the requirement. The second requirement is the maximum ESR of the capacitor, which is calculated from:

$$ESR \leq \frac{1 - D}{F_{SW} \times C_{OUT}} \times \left(\frac{I_{OUT}}{\Delta I_L} + 0.5 \right)$$

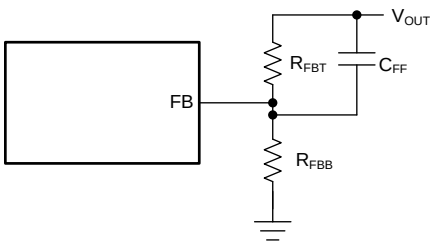
(50)

The maximum ESR is calculated to meet the required maximum output ripple. The equivalent ESR of the output capacitors should be lower than 0.288 Ω.

2.3.5.4 Loop Compensation

The LM46002-Q1 device is internally compensated with RC = 400 kΩ and CC = 50 pF. The internal compensation is designed such that the loop response is stable over the entire operating frequency and output voltage range. Depending on the output voltage, the compensation loop phase margin can be low with all ceramic capacitors. An external feed-forward cap C_{FF} is recommended to be placed in parallel with the top resistor divider RFBT for optimum transient performance.

図 14. Feed-Forward Capacitor for Loop Compensation



C_{FF} is chosen such that the phase margin is boosted at the crossover frequency. The crossover frequency without C_{FF} can be calculated as:

$$F_X = \frac{\Delta I_{OUT}}{2 \times \pi \times \Delta V_{OUT} \times C_{OUT}} \quad (51)$$

The C_{FF} should be selected such that the bandwidth of the control loop without the CFF is centered between the zero and pole frequencies caused by the feedforward capacitor. Therefore:

$$C_{FF} = \frac{1}{2 \times \pi \times F_X} \times \frac{1}{\sqrt{R_{FBT} \times (R_{FBT} \parallel R_{FBB})}} \quad (52)$$

A 100-pF feedforward capacitor is selected for this design.

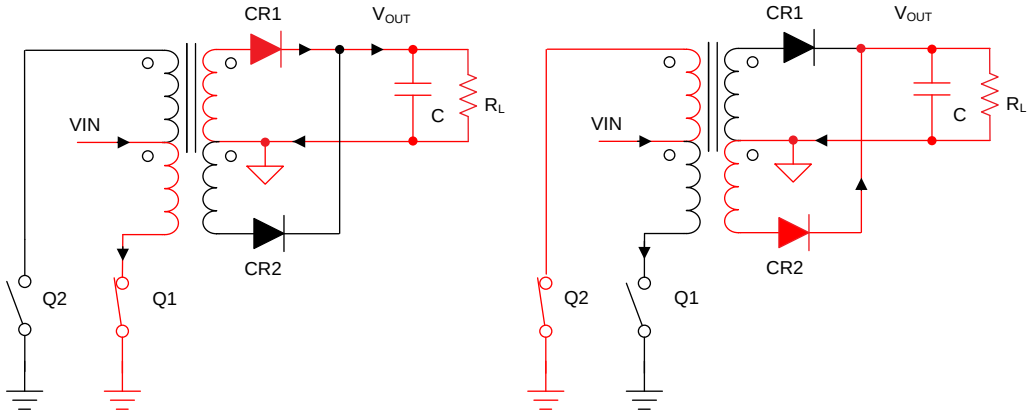
The LM46002 device needs a bootstrap capacitor between CBOOT and the SW pin. The recommended bootstrap capacitor is 0.47 µF and rated at 50 V. The bootstrap capacitor must be a high-quality ceramic type with X7R or X5R grade dielectric for temperature stability.

The VCC pin is the output of an internal LDO for the LM46002 device. The input for this LDO comes from either V_{IN} or bias. To ensure stability of the part, a minimum of a 2.2-µF, 10-V capacitor is connected from VCC to ground.

2.3.6 SN6505-Q1 Push-Pull Transformer Driver

The second stage implements a push-pull transformer driver to transfer power from the primary side to the secondary side. 図 15 shows the converter operation theory.

図 15. Push-Pull Converter Theory of Operation



When Q1 conducts, current is sourced from VIN into the ground through the lower half of the transformer primary, this creates a potential at the lower half of the primary winding with the primary center tap as the positive. This voltage transfers to the transformer secondary according to the transformer polarity and turns ratio. CR1 is now forward-biased and CR2 is reverse-biased, causing a current to flow through the upper half of the secondary winding. Similarly, when Q2 conducts, the transformer primary and secondary polarities reverse. CR1 is reverse-biased and CR2 is forward-biased, which causes a current to flow from the bottom half of the secondary through CR2 into the load. Q1 and Q2 switch alternatively, with approximately 50% duty cycle to transfer power from the primary to the secondary of the transformer.

Before either switch is turned ON, there must be a short period during which both transistors are high impedance. This short period, known as break-before-make time, is required to avoid shorting out both ends of the primary.

The SN6505-Q1 push-pull transformer driver has integrated MOSFET switches. The positive temperature co-efficient of these switches has a self-correcting effect on the V-t imbalance. During a slightly longer on-time, the prolonged current flow through a FET gradually heats the MOSFET, which leads to an increase in $R_{DS(on)}$. The higher resistance then causes the drain-source voltage, VDS, to increase. Because the voltage at the primary is the difference between the constant input voltage, VIN, and the voltage drop across the MOSFET is gradually reduced and V-t balance is restored.

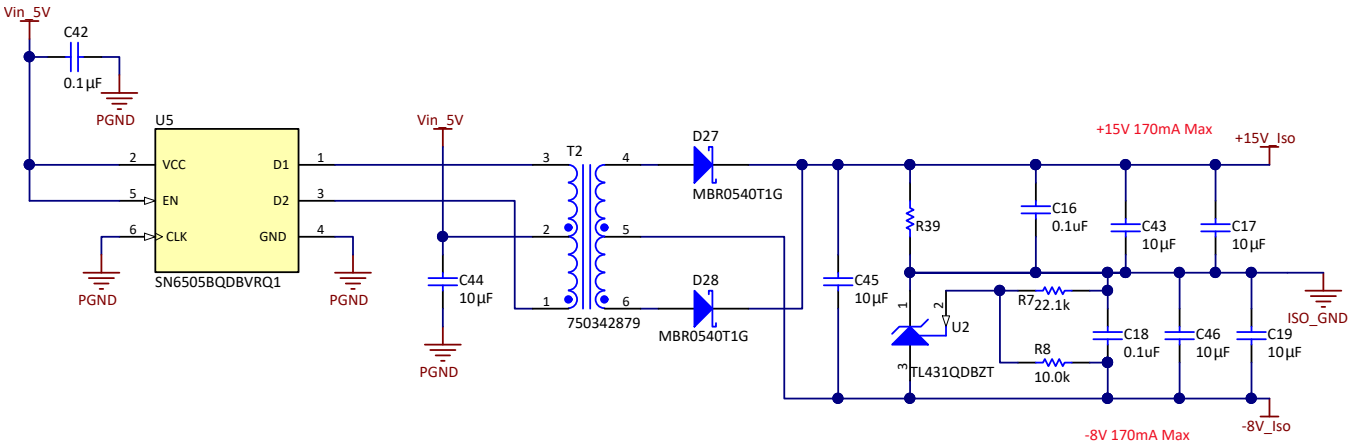
2.3.6.1 Power Supply Specification

Specifications of the designed push-pull power supply are summarized in 表 6. 図 16 shows the designed schematic. The required external discrete components are: center-tapped transformer, rectifier diodes, and input and output bulk capacitors.

表 6. Push-Pull Transformer Driver Power Supply Specifications

PARAMETER	SPECIFICATION
Input voltage	5 V ±5%
Output voltage	+15 V, –8 V
Output current	180 mA
Output voltage ripple	< 200 mV peak to peak at full load
Output power	4.14 W

図 16. Push-Pull Transformer Driver Power Supply Schematic



2.3.6.2 Transformer Design

The input peak current was calculated from 式 53. The factor 0.97 accounts for typical transformer power transfer efficiency.

$$I_{in\_peak} = \frac{P_{out\_max} / \eta}{V_{in\_min}} = \frac{4.32\ W / 0.97}{4.75\ V} = 882\ \ mA$$

where

- P_{out_max} is the maximum output power
- V_{IN_min} is the minimum input voltage (53)

The SN6505-Q1 device switches the internal dual MOSFETs with approximately 50% duty cycle each. Therefore, the AC current flowing through transformer primary (I_{pri}) can be calculated from:

$$I_{pri} = \frac{I_{in\_peak}}{2} = \frac{882\ mA}{2} = 441\ \ mA \quad (54)$$

The transformer turns ratio (N_{ps}) is calculated from:

$$N_{ps} = \frac{V_{pri}}{V_{sec} + V_f} = \frac{5\ V}{23\ V + 0.35\ V} = 1:4.67$$

where

- V_{sec} is the voltage across the secondary winding
- V_f is the forward voltage of the diode
- V_{pri} is the voltage across the primary winding (55)

The V-t product of the transformer must be greater than Vt_{min}. Failure to meet these criteria will lead to transformer core saturation:

$$Vt_{min} = V_{IN\_max} \times \frac{T_{max}}{2} = \frac{V_{IN\_max}}{2 \times F_{min}} = \frac{5\ V \times 1.05}{2 \times 300\ kHz} = 8.75\ V\ \mu s$$

where

- V_{IN_max} is the maximum input voltage
- F_{min} is the minimum switching frequency (56)

The 750342879 transformer from Wurth Electronics is selected for this design. 表 7 summarizes the specifications.

表 7. Push-Pull Transformer Specifications

PARAMETER	SPECIFICATION
Turns ratio (6 – 4):(1 – 3)	3.5 : 1, ±2%
DC resistance (1 – 3)	0.33 Ω maximum at 20°C
DC Resistance (6 – 4)	0.75 Ω maximum at 20°C
Inductance (1 – 2)	50-µH minimum at 100 kHz, 10 mVac
Dielectric (1 – 6)	5000 V_{RMS}, 1 minute
Operating temperature range	-40°C to 125°C
Clearance distance	8 mm

2.3.6.3 Rectifier Diode

To increase the efficiency of the push-pull forward converter, the forward voltage drop of the secondary side rectifier diodes must be minimized. This design implements the SN6505B version which has the high-switching frequency and the diodes are subject to excessive reverse recoveries. Schottky diodes are selected as they meet the requirements of low forward-voltage drop and fast recovery time. The diode should withstand a reverse voltage of twice the output voltage.

The forward current flowing through the diode is the rated output current which is 180 mA. The reverse blocking voltage of the diode is calculated as:

$$V_b = V_{out} + V_{in} \times \frac{N_{sec}}{N_{pri}} = 36\ V \quad (57)$$

Two 40-V, 500-mA Schottky diodes are chosen for this design.

2.3.6.4 Capacitor Selection

Considering two 22-µF ceramic capacitors being placed at output of the buck converter, one ceramic bypass capacitor of 100 nF is placed as close as possible to the V_{CC} pin for high frequency noise filtering.

The output capacitor is required to filter the output ripple. The output ripple specification is calculated as:

$$\Delta V = V_{out} \times 10\% = 23\ V \times 1\% = 0.23\ V \quad (58)$$

The required peak current which is delivered to the gate driver is 20 A, according to the isolated gate driver board. The required capacitance is calculated as:

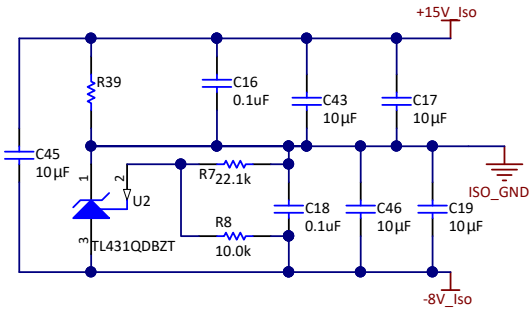
$$C \geq \frac{I_{peak} \times dt}{\Delta V} = 13 \ \ \mu F \tag{59}$$

Considering it could also be used to drive SiC MOSFETs with higher total gate charge, a total of two 10-µF ceramic capacitors are connected in parallel at the positive and negative supply outputs.

2.3.6.5 Generation of the Negative Supply

The power supply output is separated into the positive rail of +15 V and the negative rail of –8 V through the TL431-Q1 device which reacts as a shunt regulator. 図 17 shows the schematic.

図 17. Generation of Negative Voltage Rail Through TL431-Q1 Shunt Reference



To program the cathode voltage to a regulated voltage, a resistive bridge is shunted between the cathode and anode pins with the mid-point tied to the reference pin. The cathode voltage is calculated as:

$$V_{neg} = (1 + \frac{R_7}{R_8}) \times V_{ref} = (1 + \frac{22.1 \ k\Omega}{10 \ k\Omega}) \times 2.5 \ V = 8 \ \ V \tag{60}$$

For this equation to be valid, the TL431-Q1 device must be fully biased so that it has enough open loop gain to mitigate any gain error. The cathode current is set to:

$$I_{cat} = \frac{V_{out} - V_{neg}}{R_{39}} = \frac{23 \ V - 8 \ V}{15.4 \ k\Omega} = 0.97 \ mA \tag{61}$$

3 Hardware, Testing Requirements, and Test Results

3.1 Required Hardware

図 18 shows the inverter power stage board and connectors pin description. The placement of components and corresponding circuits are also described. 図 19 shows the PCB board image of LM5180-Q1 based flyback converter from top side and bottom side, respectively. The input and output connectors are indicated.

図 18. Power Stage and Connectors Pin Description

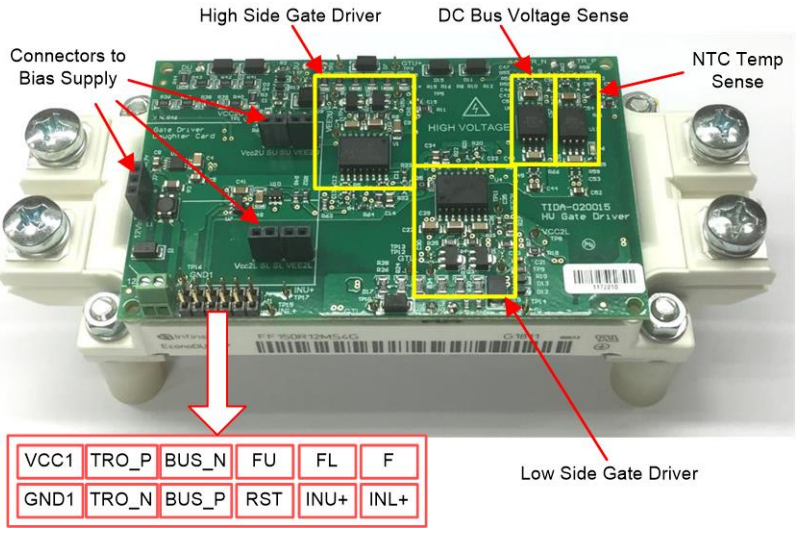


図 19. LM5180-Q1 Based Flyback PCB Board

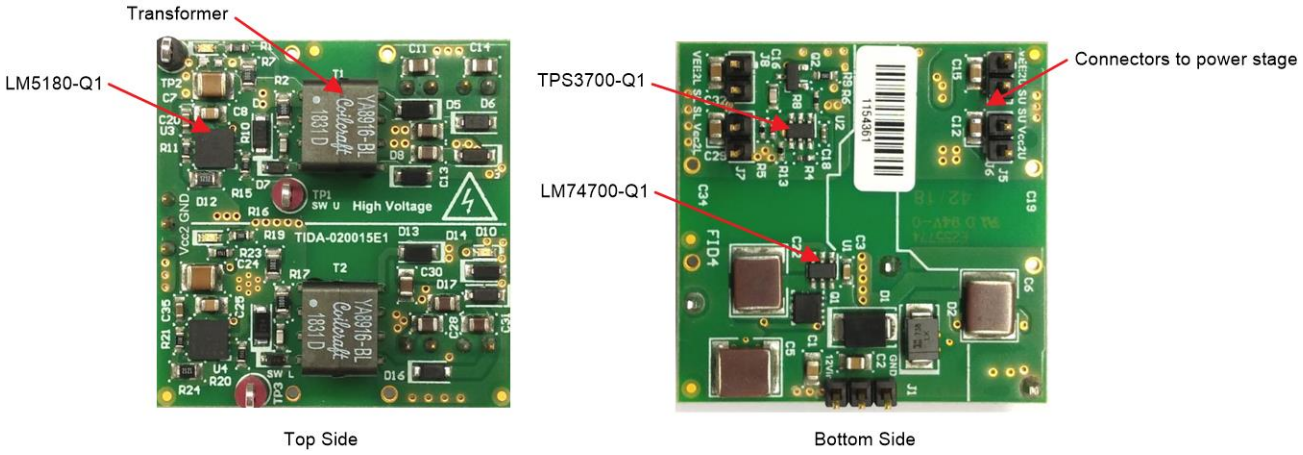


図 20 shows the LM5180-Q1 based flyback PCB board connected to the power stage.

図 20. LM5180-Q1 Based Bias Supply Connected to the Power Stage

図 21 shows the PCB board image of TPS40210-Q1 based flyback converter from top side and bottom side, respectively.

図 21. TPS40210-Q1 Based Flyback PCB Board Image

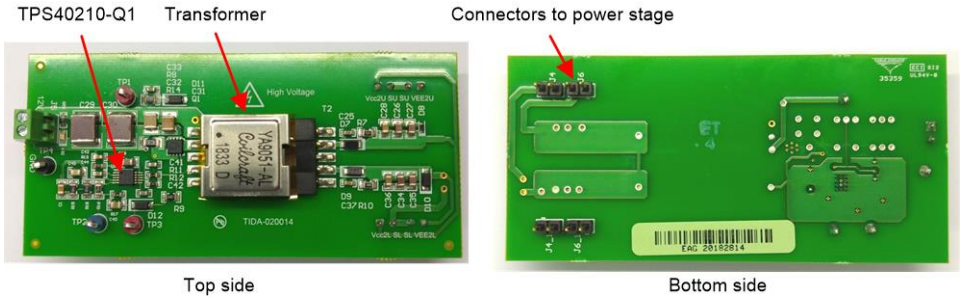


図 22 shows the PCB board image of buck with push-pull power supply from top side and bottom side, respectively.

図 22. Buck With Push-Pull Power Supply PCB Board

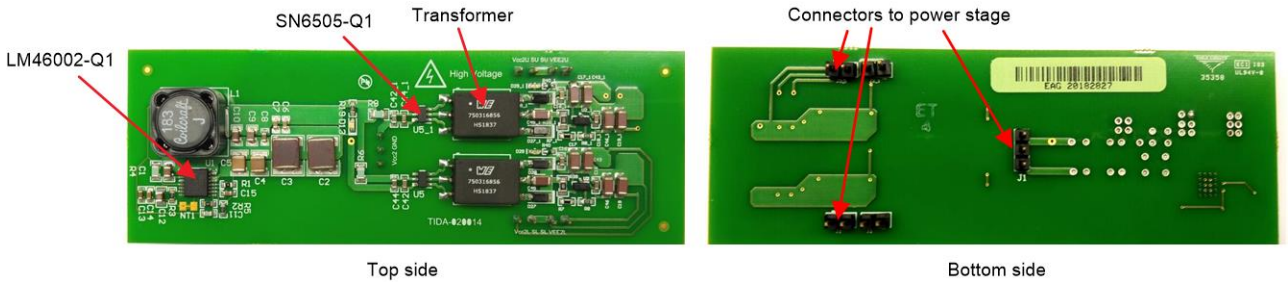


図 23 shows the buck with push-pull converter board implemented on top of the power stage and connected with the IGBT module.

図 23. Buck With Push-Pull Bias Supply Connected to the Power Stage

3.2 Testing and Results

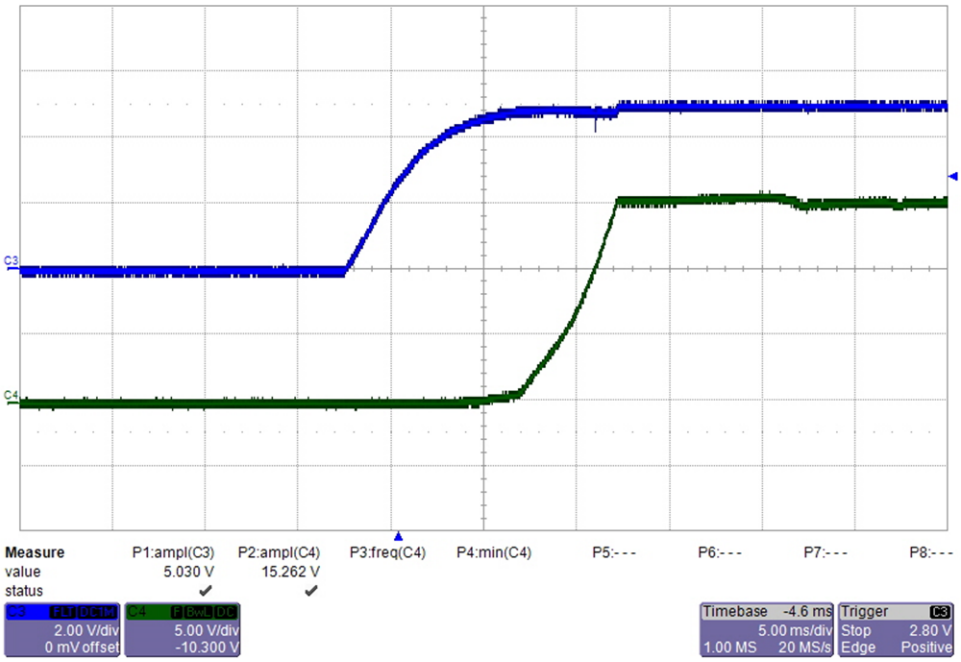
3.2.1 Low-Voltage Tests on the LM5180-Q1 Flyback Converter

This section presents the experimental results of the bias supply solution 1 which is the flyback converter based on the LM5180-Q1 device.

3.2.1.1 Startup

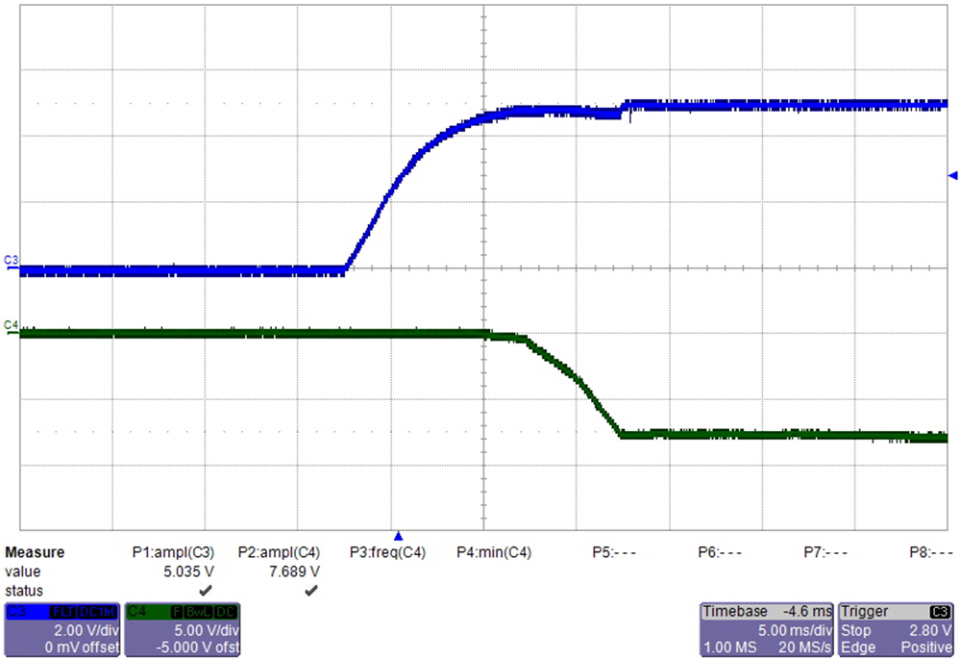
The start-up waveforms of the flyback converter designed with the LM5180-Q1 device are measured under 5- and 12-V inputs, respectively. The 15-V and –9-V rails are measured separately.

図 24. Start-up Waveform of the 15-V Rail With V_{IN} = 5 V and no Load (Bias Supply With LM5180-Q1)



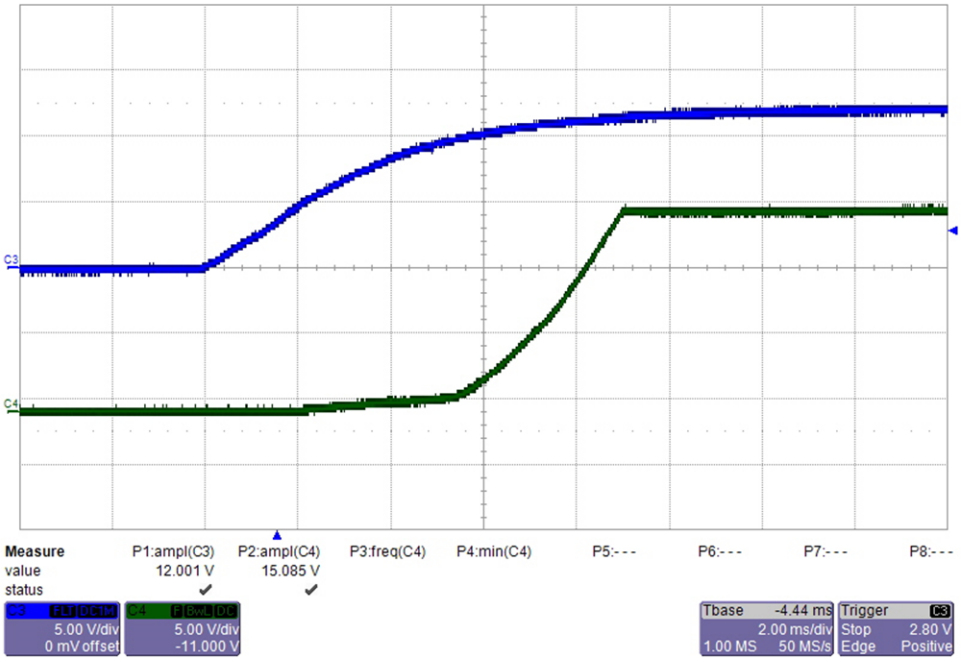
From top to bottom: CH3: input voltage 2 V/div, CH4: output voltage 5 V/div, 5 ms/div

図 25. Start-up Waveform of the –9-V Rail With V_{IN} = 5 V and no Load (Bias Supply With LM5180-Q1)



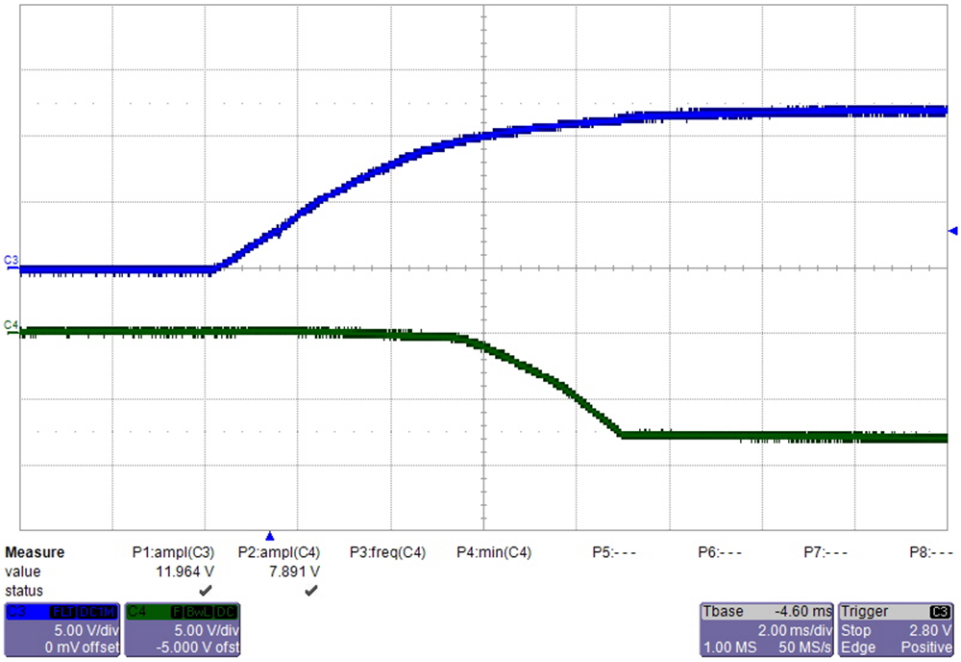
From top to bottom: CH3: input voltage 2 V/div, CH4: output voltage 5 V/div, 5 ms/div

図 26. Start-up Waveform of the 15-V Rail With V_{IN} = 12 V and 180-mA Load (Bias Supply With LM5180-Q1)



From top to bottom: CH3: input voltage 5 V/div, CH4: output voltage 5 V/div, 2 ms/div

図 27. Start-up Waveform of the –9-V Rail With V_{IN} = 12 V and 180-mA Load (Bias Supply With LM5180-Q1)

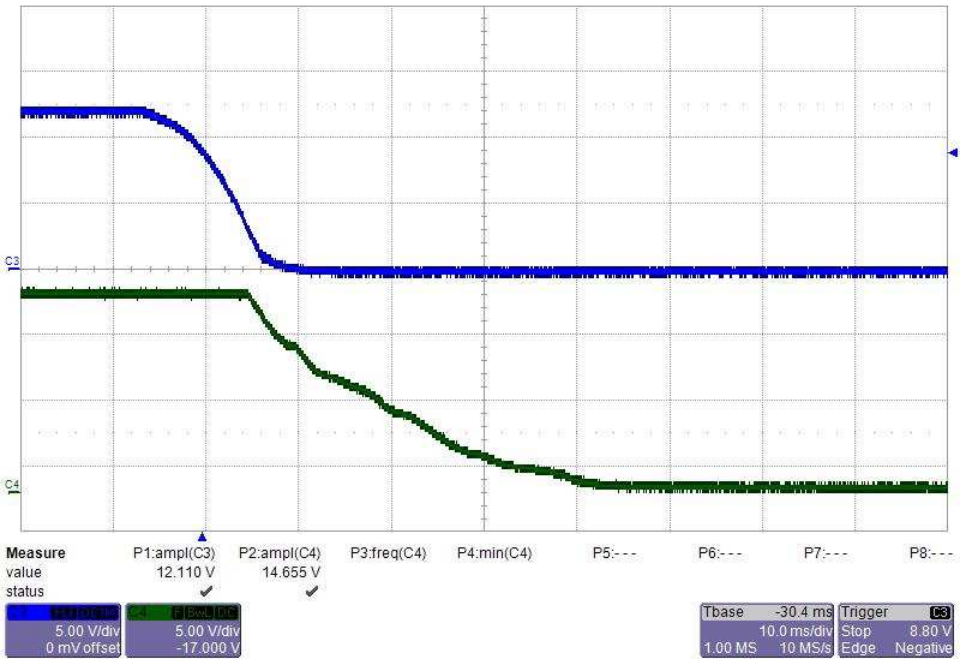


From top to bottom: CH3: input voltage 5 V/div, CH4: output voltage 5 V/div, 2 ms/div

3.2.1.2 Power Down

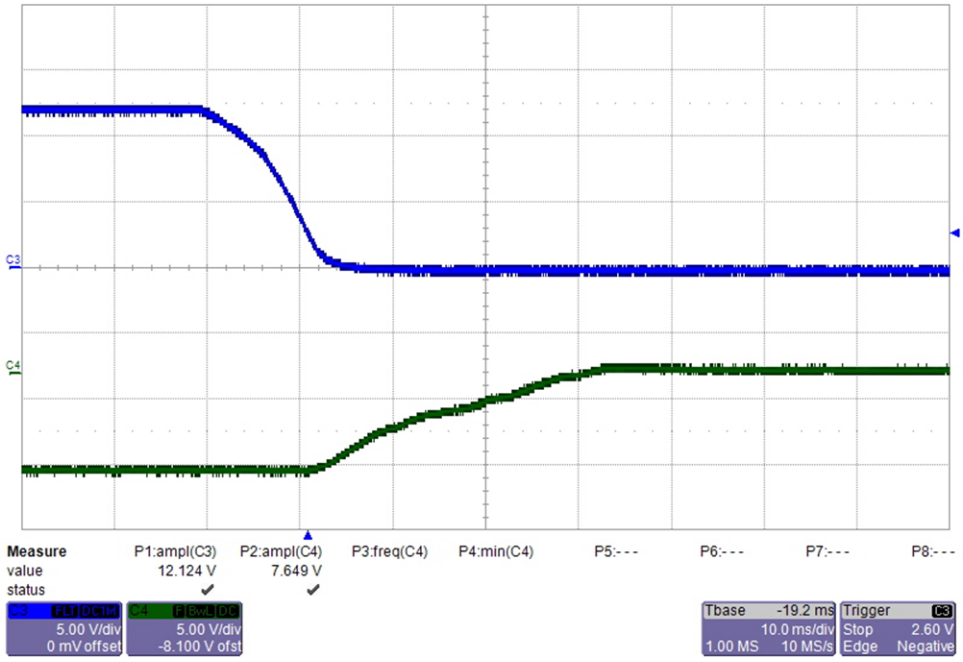
The power-down waveforms of the flyback converter designed with the LM5180-Q1 device are measured under 5- and 12-V inputs, respectively. The 15-V and –9-V rails are measured separately.

図 28. Power-Down Waveform of the 15-V Rail With V_{IN} = 12 V and no Load (Bias Supply With LM5180-Q1)



From top to bottom: CH3: input voltage 5 V/div, CH4: output voltage 5 V/div, 10 ms/div

図 29. Power-Down Waveform of the –9-V Rail With V_{IN} = 12 V and no Load (Bias Supply With LM5180-Q1)

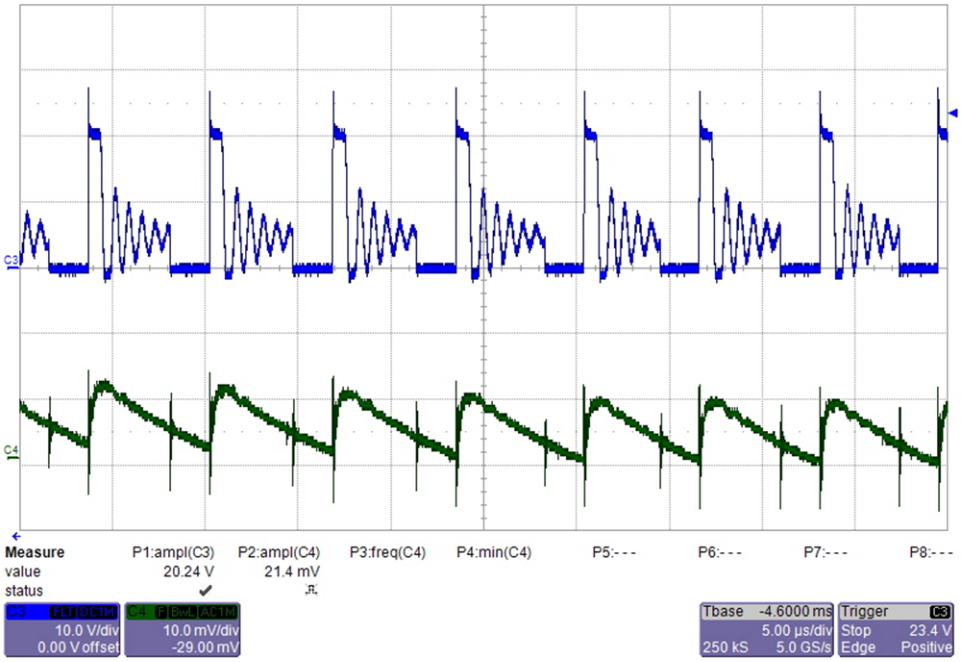


From top to bottom: CH3: input voltage 5 V/div, CH4: output voltage 5 V/div, 10 ms/div

3.2.1.3 Switch Node and Output Voltage Ripple

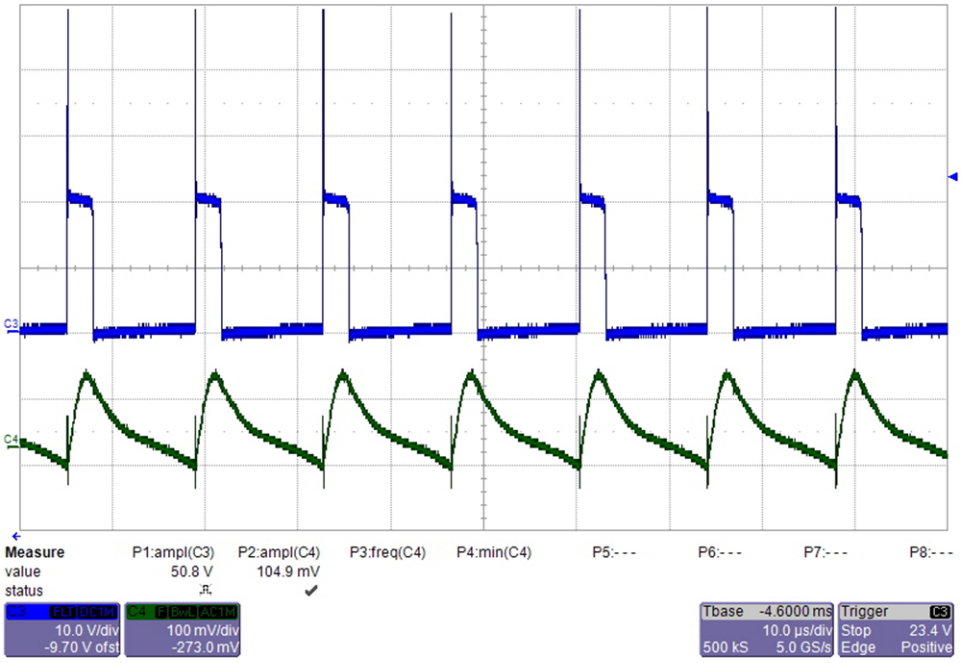
The switch node and output voltage ripple of the flyback converter designed with the LM5180-Q1 device are measured under 5-, 12-, and 18-V inputs, respectively. The +15-V and –9-V rails are measured separately.

図 30. Switch Node and Output Ripple of the 15-V Rail With V_{IN} = 5 V and no Load (Bias Supply With LM5180-Q1)



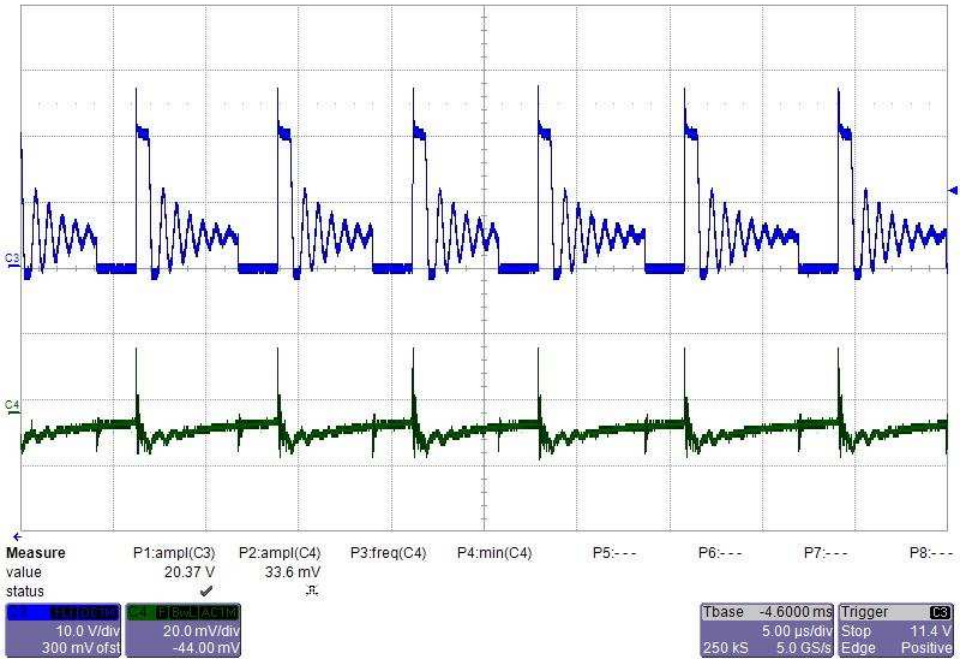
From top to bottom: CH3: switch node 10 V/div, CH4: output voltage ripple 10 mV/div, 5 µs/div

図 31. Switch Node and Output Ripple of the 15-V Rail With V_{IN} = 5 V and 85-mA Load (Bias Supply With LM5180-Q1)



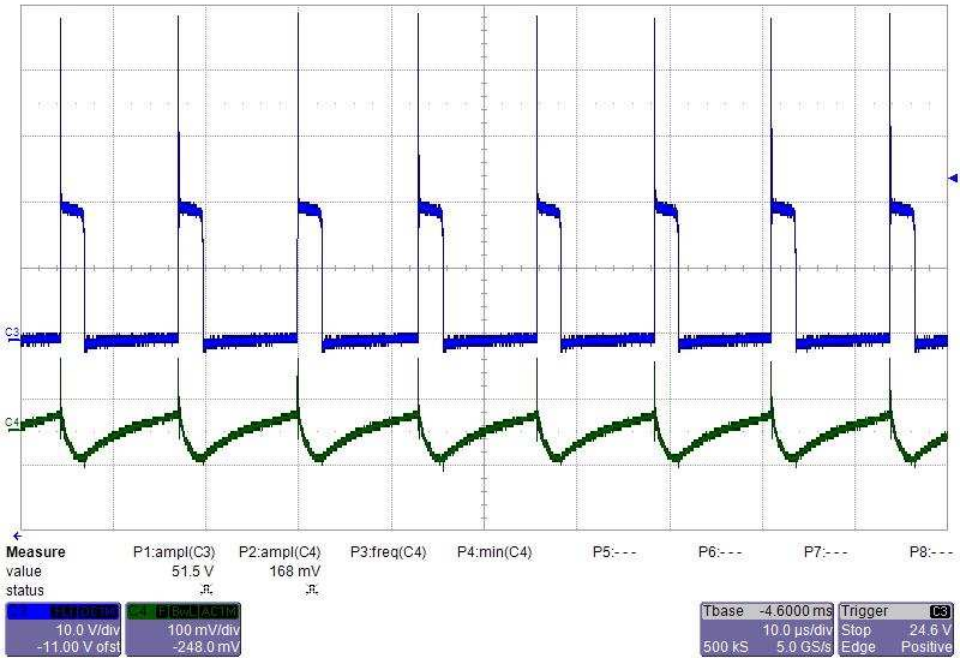
From top to bottom: CH3: switch node 10 V/div, CH4: output voltage ripple 100 mV/div, 10 µs/div

図 32. Switch Node and Output Ripple of the –9-V Rail With V_{IN} = 5 V and no Load (Bias Supply With LM5180-Q1)



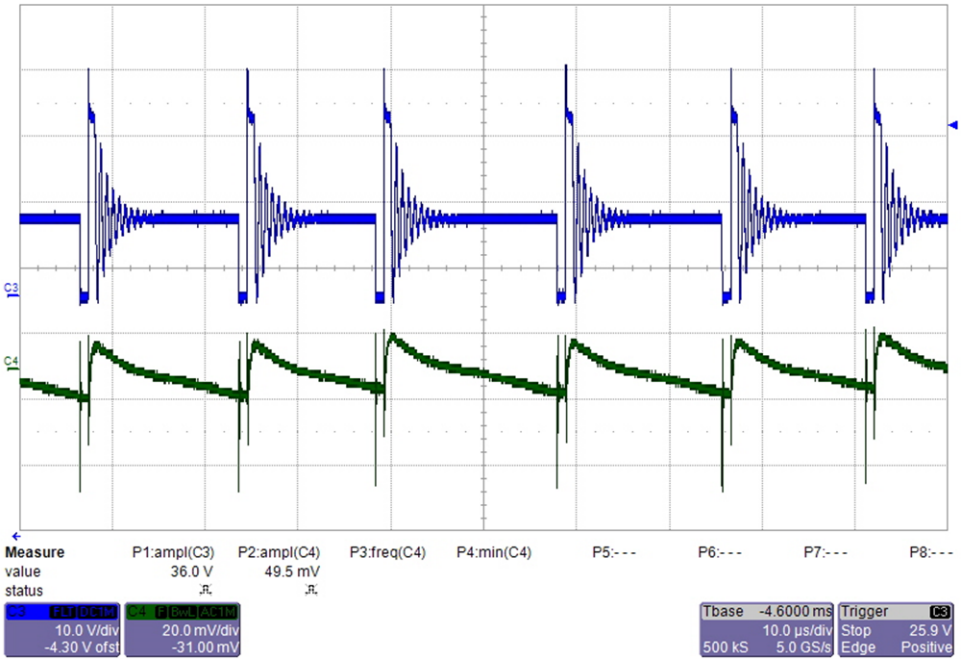
From top to bottom: CH3: switch node 10 V/div, CH4: output voltage ripple 20 mV/div, 5 µs/div

図 33. Switch Node and Output Ripple of the –9-V Rail With V_{IN} = 5 V and 85-mA Load (Bias Supply With LM5180-Q1)



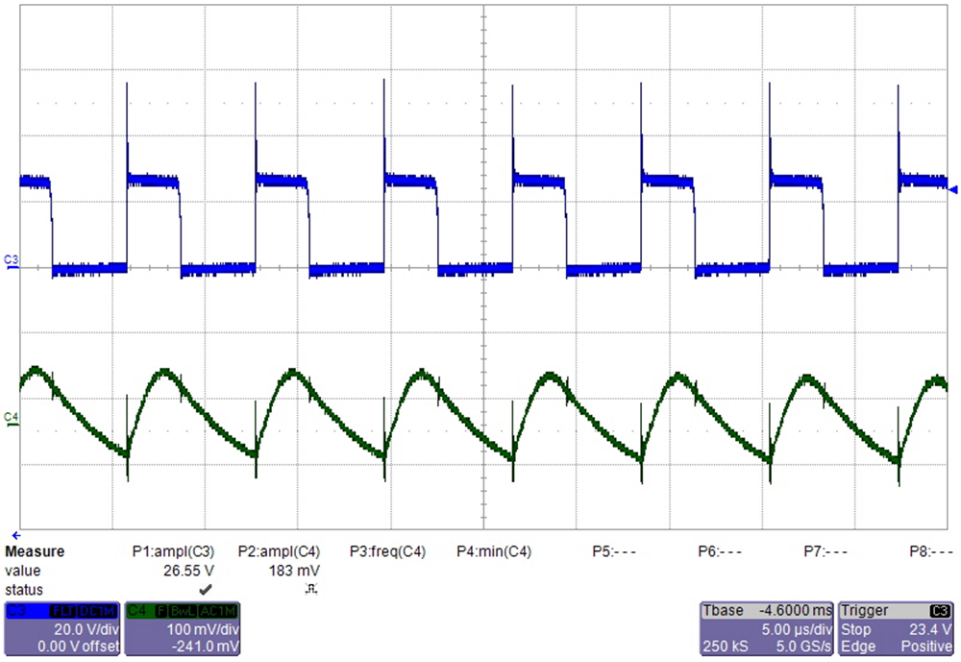
From top to bottom: CH3: switch node 10 V/div, CH4: output voltage ripple 100 mV/div, 10 µs/div

図 34. Switch Node and Output Ripple of the 15-V Rail With V_{IN} = 12 V and no Load (Bias Supply With LM5180-Q1)



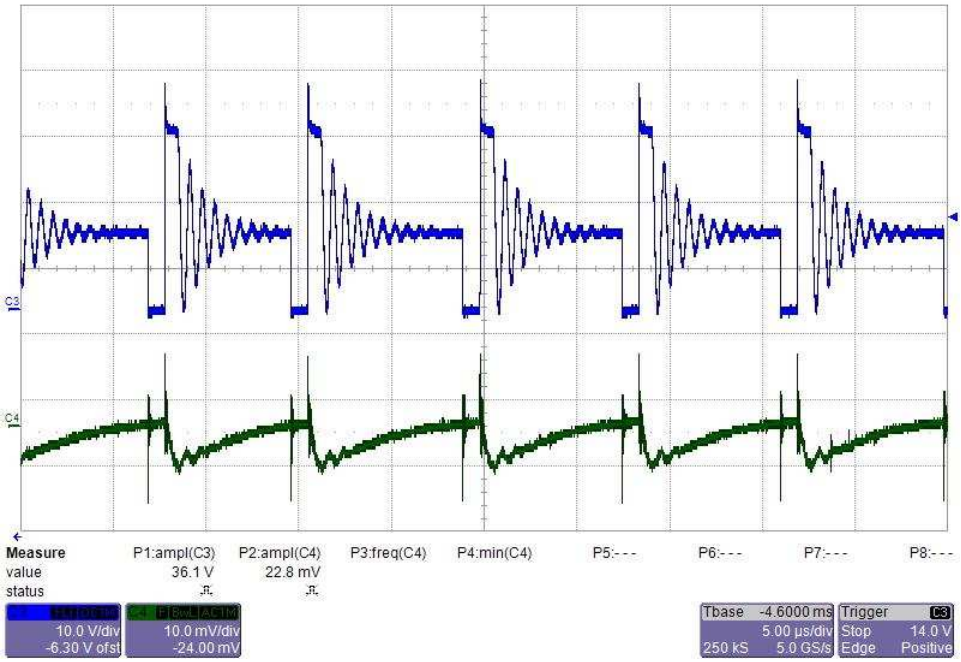
From top to bottom: CH3: switch node 10 V/div, CH4: output voltage ripple 20 mV/div, 10 µs/div

図 35. Switch Node and Output Ripple of the 15-V Rail With V_{IN} = 12 V and 180-mA Load (Bias Supply With LM5180-Q1)



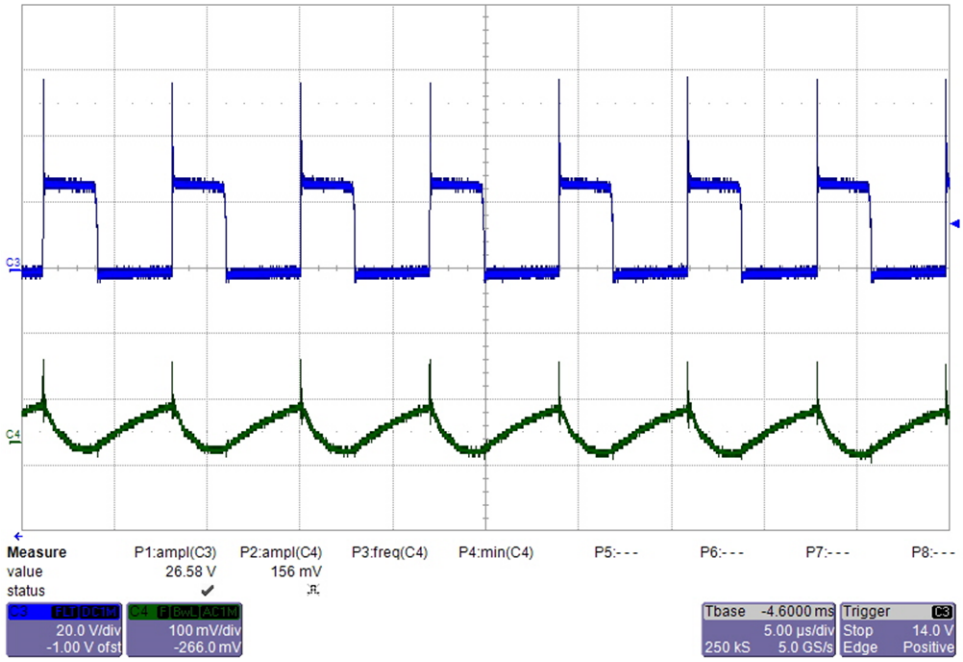
From top to bottom: CH3: switch node 20 V/div, CH4: output voltage ripple 100 mV/div, 5 µs/div

図 36. Switch Node and Output Ripple of the –9-V Rail With V_{IN} = 12 V and no Load (Bias Supply With LM5180-Q1)



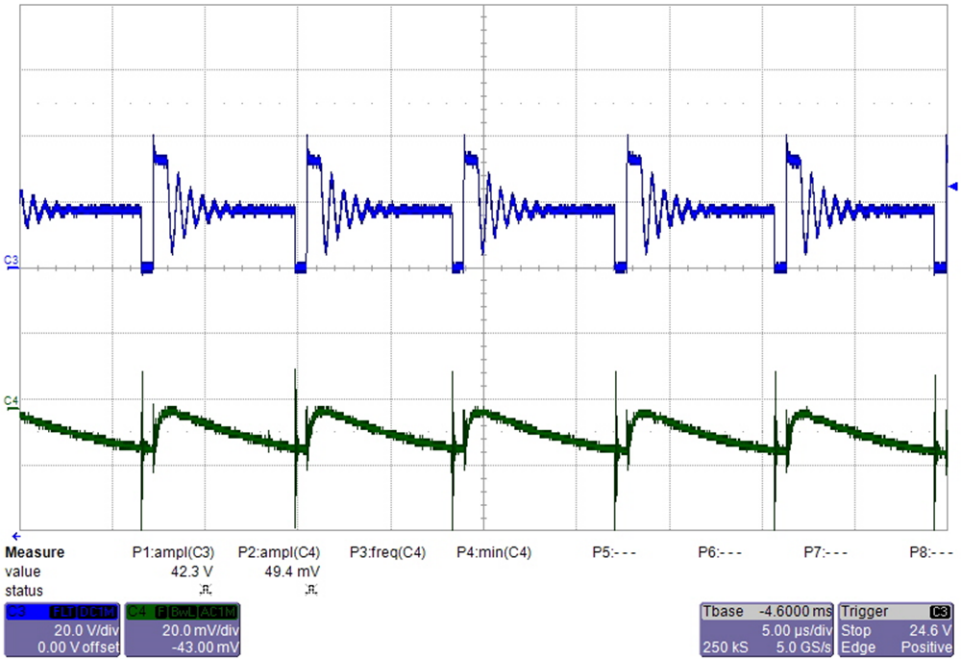
From top to bottom: CH3: switch node 10 V/div, CH4: output voltage ripple 10 mV/div, 5 µs/div

図 37. Switch Node and Output Ripple of the –9-V Rail With V_{IN} = 12 V and 180-mA Load (Bias Supply With LM5180-Q1)



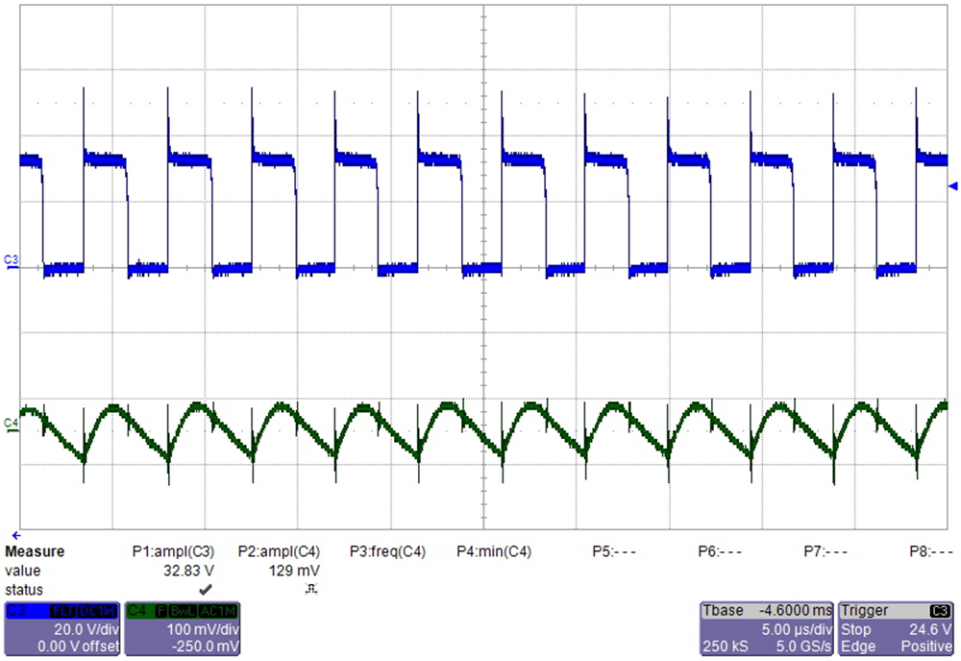
From top to bottom: CH3: switch node 20 V/div, CH4: output voltage ripple 100 mV/div, 5 µs/div

図 38. Switch Node and Output Ripple of the 15-V Rail With V_{IN} = 18 V and no Load (Bias Supply With LM5180-Q1)



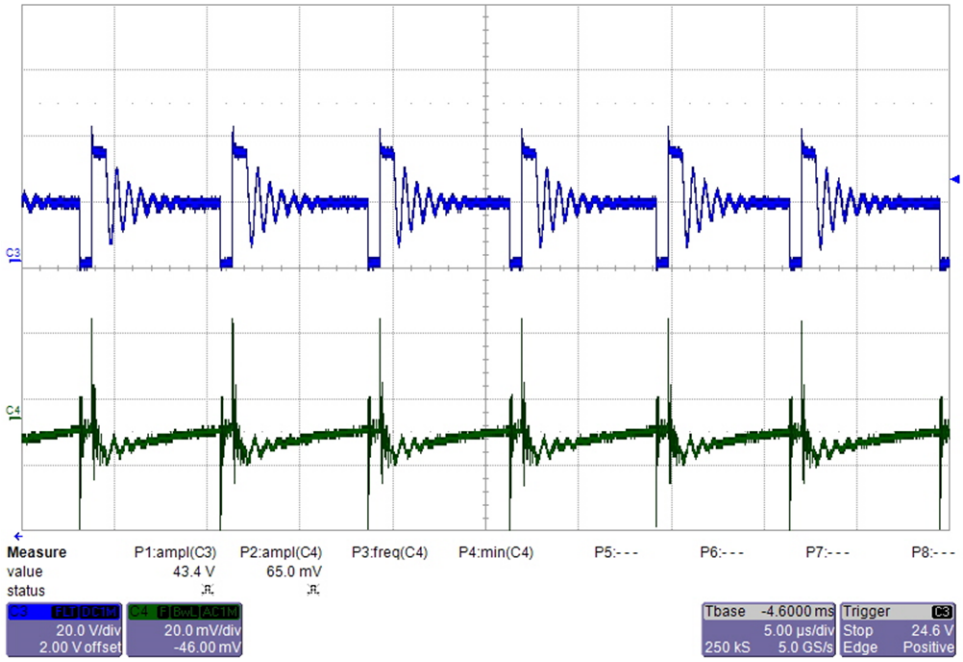
From top to bottom: CH3: switch node 20 V/div, CH4: output voltage ripple 20 mV/div, 5 µs/div

図 39. Switch Node and Output Ripple of the 15-V Rail With V_{IN} = 18 V and 180-mA Load (Bias Supply With LM5180-Q1)



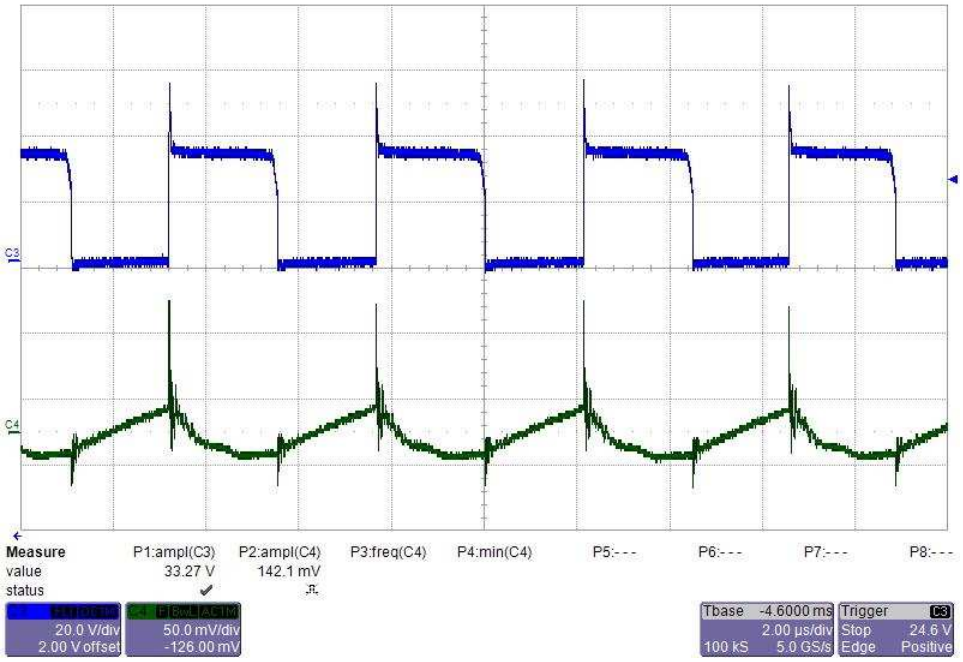
From top to bottom: CH3: switch node 20 V/div, CH4: output voltage ripple 100 mV/div, 5 µs/div

図 40. Switch Node and Output Ripple of the –9-V Rail With V_{IN} = 18 V and no Load (Bias Supply With LM5180-Q1)



From top to bottom: CH3: switch node 20 V/div, CH4: output voltage ripple 20 mV/div, 5 µs/div

図 41. Switch Node and Output Ripple of the –9-V Rail With V_{IN} = 18 V and 180-mA Load (Bias Supply With LM5180-Q1)

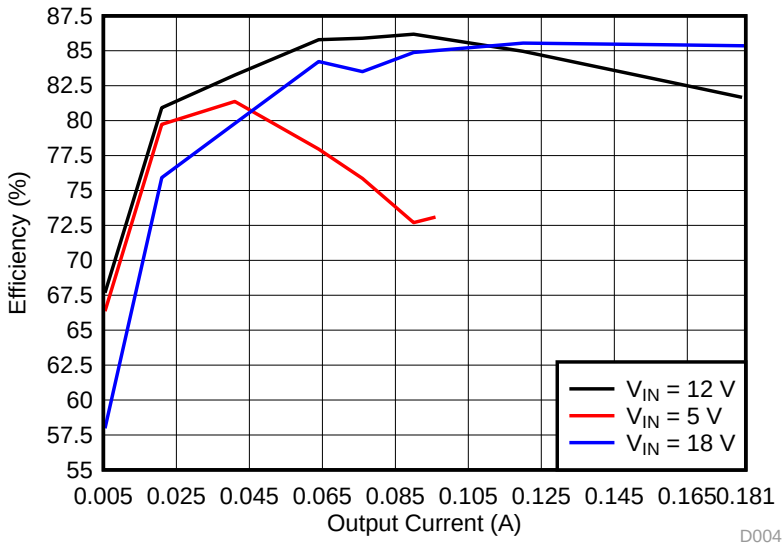


From top to bottom: CH3: switch node 20 V/div, CH4: output voltage ripple 50 mV/div, 2 µs/div

3.2.1.4 Efficiency

図 42 shows the measured efficiency of the flyback converter designed with the LM5180-Q1 device over the full-load range. As can be seen, around 86% peak efficiency is achieved with the input voltages of 5 V, 12 V, and 18 V, respectively.

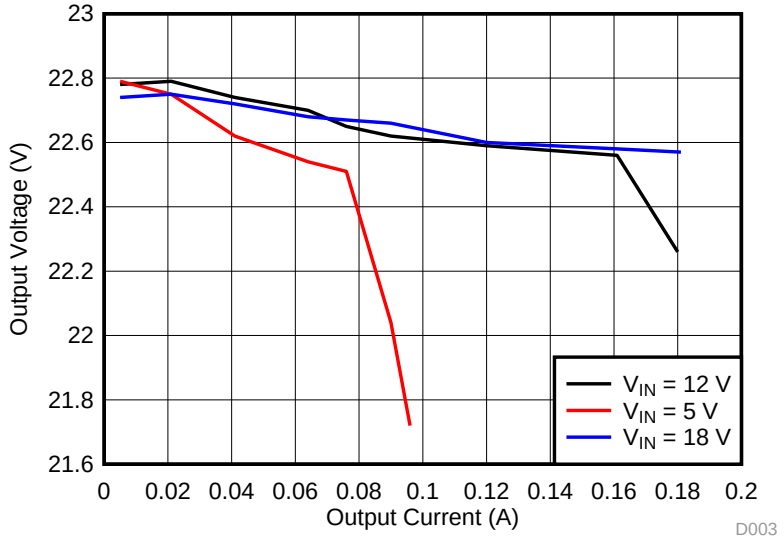
図 42. Measured Efficiency Under Input Voltages of 5 V, 12 V, and 18 V (Bias Supply With LM5180-Q1)



3.2.1.5 Load Regulation

Load regulation measurements show the % deviation from nominal output voltage as a function of output current. The measured result of the flyback converter designed with LM5180-Q1 is shown in 図 43. The load regulation is measured with the input voltages of 5 V, 12 V, and 18 V, respectively.

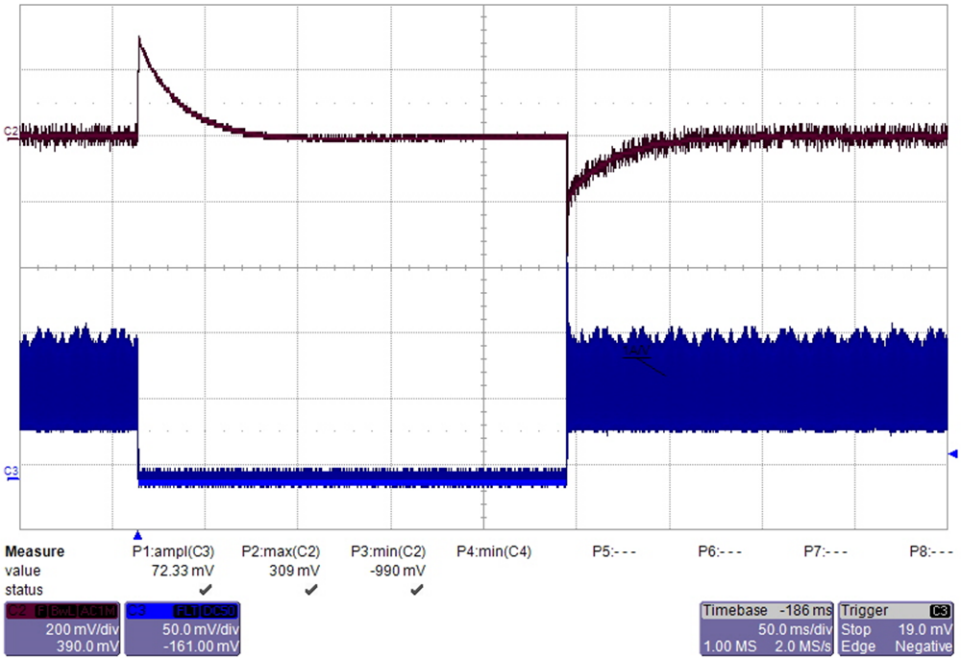
図 43. Load Regulation Under Input Voltages of 5 V, 12 V, and 18 V (Bias Supply With LM5180-Q1)



3.2.1.6 Load Transients

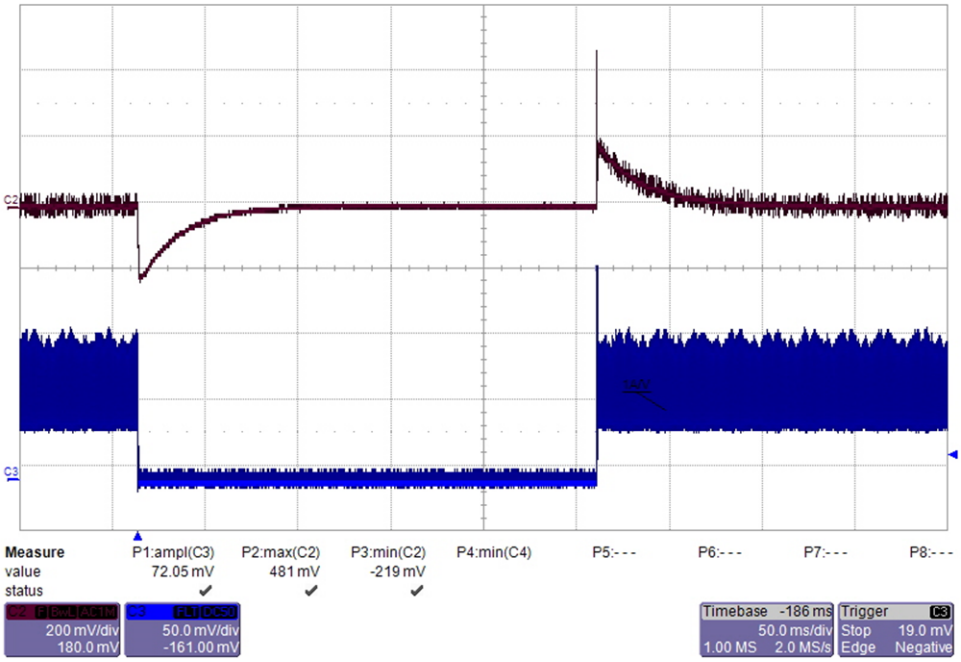
This section shows the load transient measurements of the flyback converter designed with the LM5180-Q1 device. The load transient response presents how well a power supply copes with the changes in the load-current demand. During the test, the load is switching from 0 to full under input voltages of 5 V, 12 V, and 18 V, respectively.

図 44. Load Transient Response of the 15-V Rail Under V_{IN} = 5 V and I_{OUT} Switching Between 0 and 80 mA (Bias Supply With LM5180-Q1)



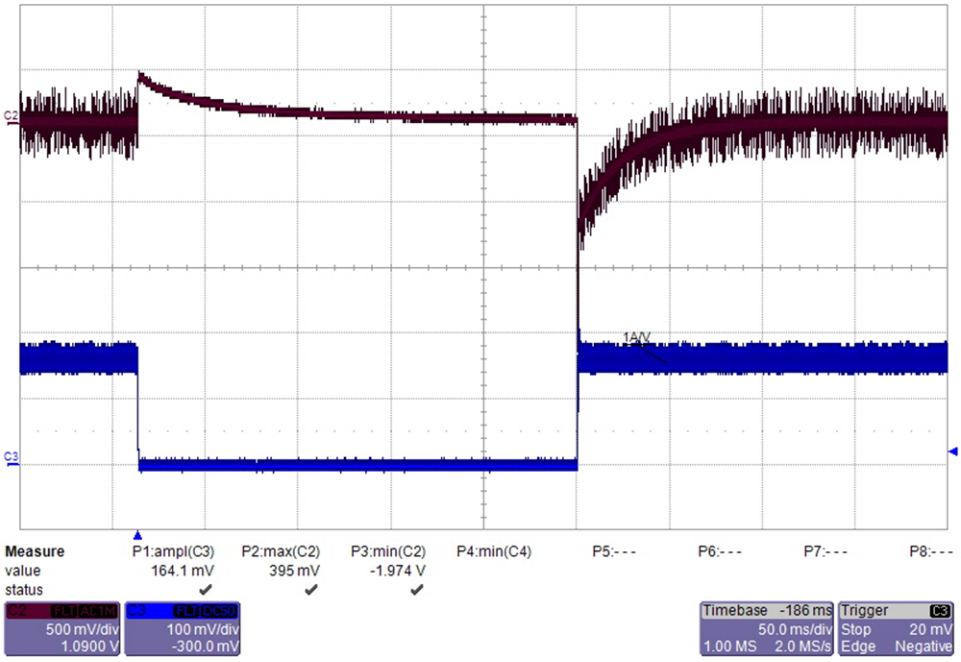
From top to bottom: CH2: output voltage 200 mV/div, CH3: load current 500 mA/div, 50 ms/div

図 45. Load Transient Response of the –9-V Rail Under V_{IN} = 5 V and I_{OUT} Switching Between 0 and 80 mA (Bias Supply With LM5180-Q1)



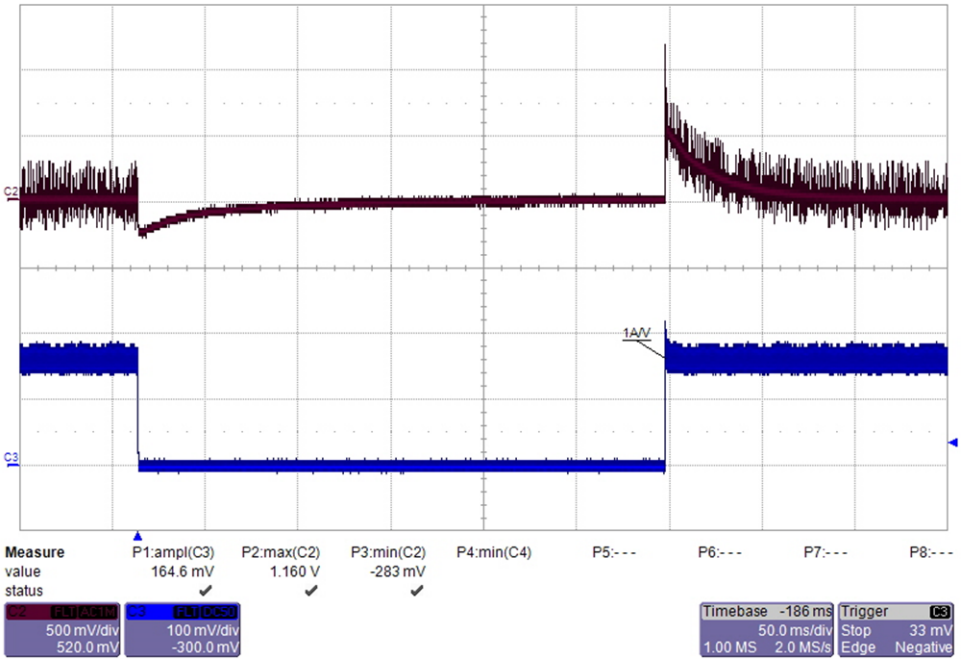
From top to bottom: CH2: output voltage 200 mV/div, CH3: load current 500 mA/div, 50 ms/div

図 46. Load Transient Response of the 15-V Rail Under V_{IN} = 12 V and I_{OUT} Switching Between 0 and 180 mA (Bias Supply With LM5180-Q1)



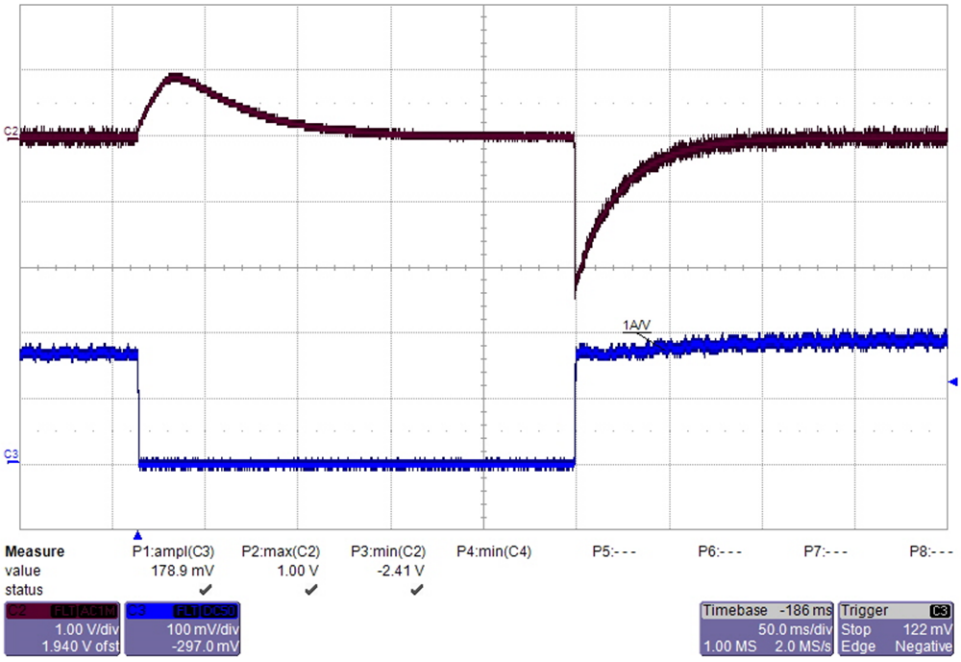
From top to bottom: CH2: output voltage 500 mV/div, CH3: load current 1 A/div, 50 ms/div

図 47. Load Transient Response of the –9-V Rail Under V_{IN} = 12 V and I_{OUT} Switching Between 0 and 180 mA (Bias Supply With LM5180-Q1)



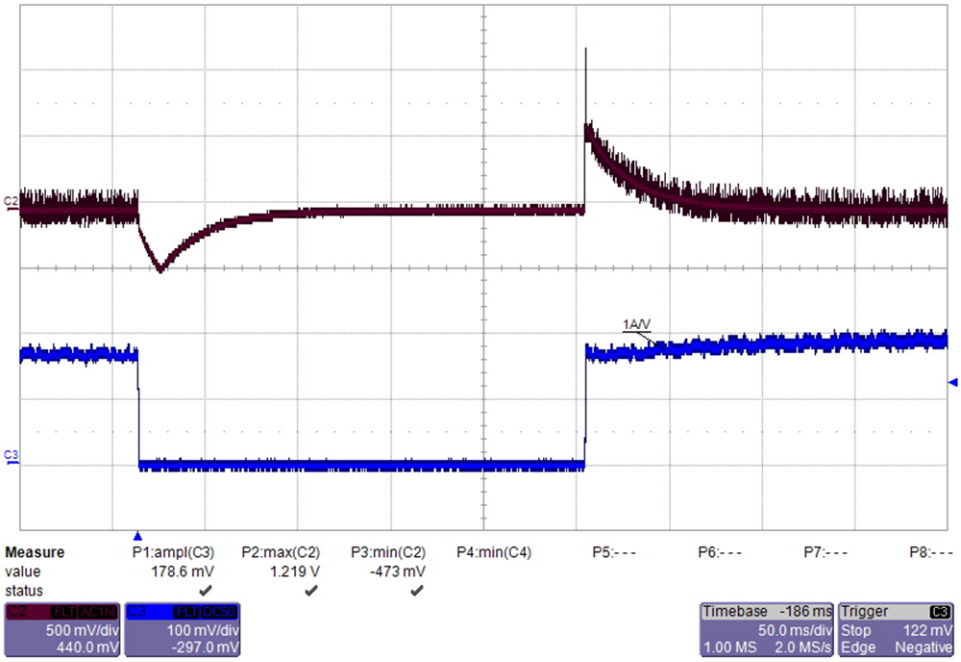
From top to bottom: CH2: output voltage 500 mV/div, CH3: load current 1 A/div, 50 ms/div

図 48. Load Transient Response of the 15-V Rail Under V_{IN} = 18 V and I_{OUT} Switching Between 0 and 180 mA (Bias Supply With LM5180-Q1)



From top to bottom: CH2: output voltage 1 V/div, CH3: load current 1 A/div, 50 ms/div

図 49. Load Transient Response of the –9-V Rail Under V_{IN} = 18 V and I_{OUT} Switching Between 0 and 180 mA (Bias Supply With LM5180-Q1)

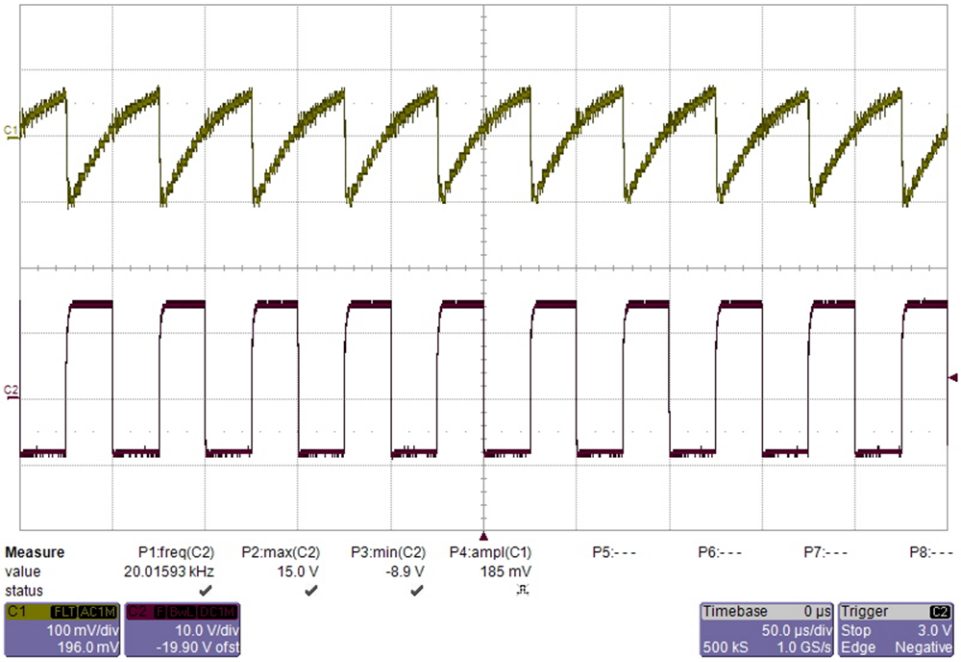


From top to bottom: CH2: output voltage 500 mV/div, CH3: load current 1 A/div, 50 ms/div

3.2.1.7 Voltage Ripple While Switching IGBT

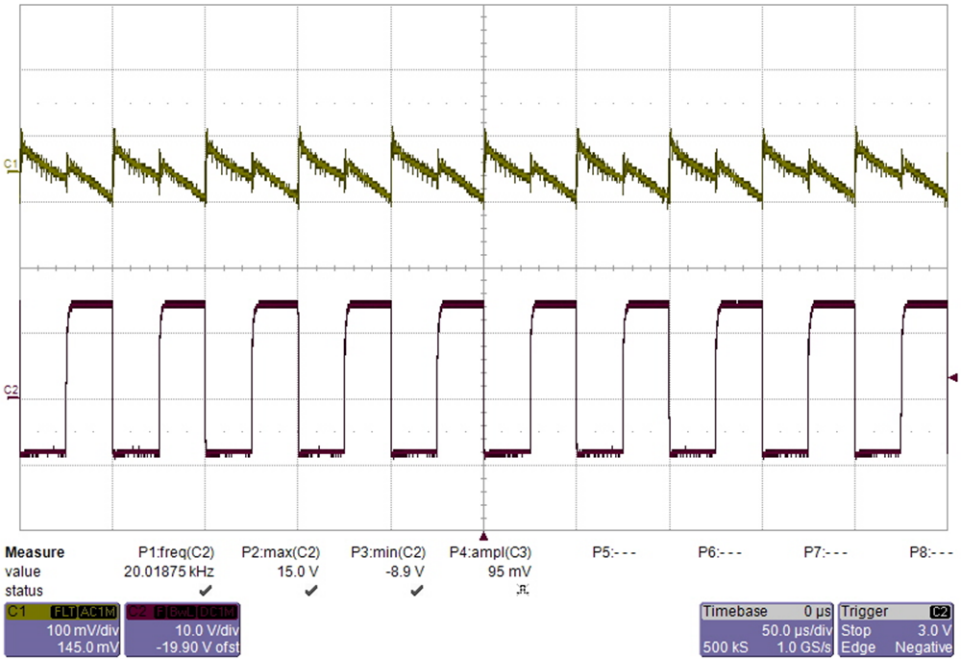
The flyback converter designed with the LM5180-Q1 device is connected to the isolated gate drivers (ISO5852S-Q1) and the 1200-V IGBT module (FF150R12MS4G) for checking the voltage ripple during the switching transients. The IGBTs are switched at 20- and 50-kHz frequencies, respectively.

図 50. Voltage Ripple of the 15-V Rail While Switching the IGBT Module at 20 kHz (Bias Supply With LM5180-Q1)



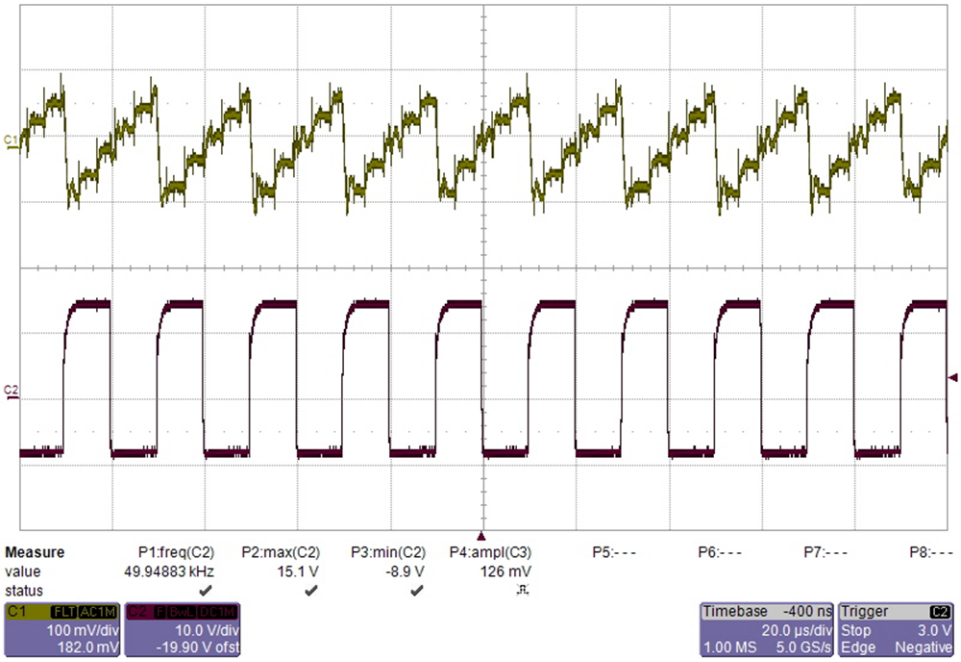
From top to bottom: CH1: output voltage 100 mV/div, CH2: gate PWM signal 10 V/div, 50 µs/div

図 51. Voltage Ripple of the –9-V Rail While Switching the IGBT Module at 20 kHz (Bias Supply With LM5180-Q1)



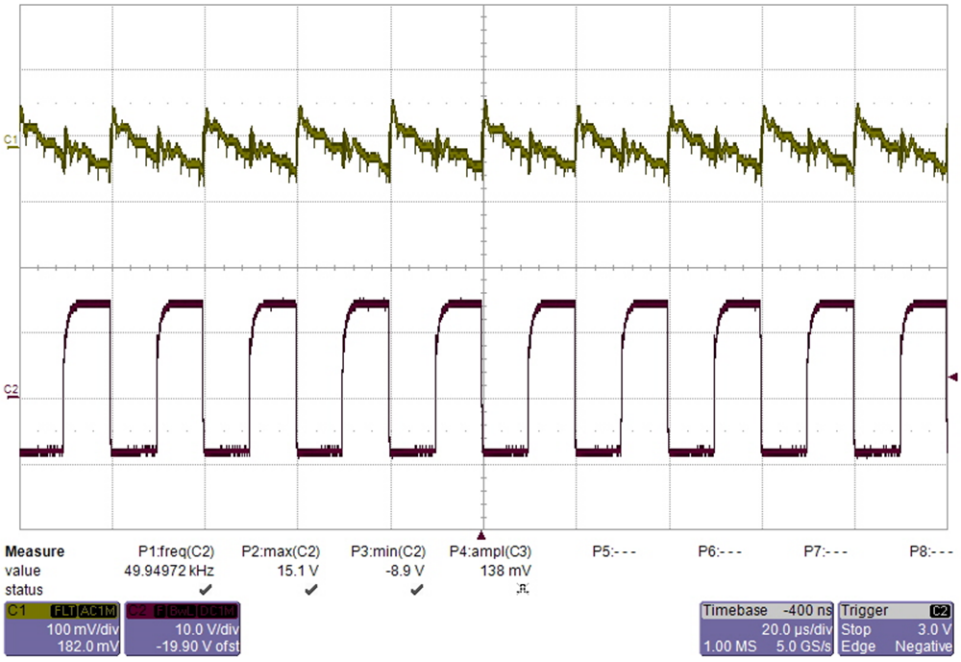
From top to bottom: CH1: output voltage 100 mV/div, CH2: gate PWM signal 10 V/div, 50 µs/div

図 52. Voltage Ripple of the 15-V Rail While Switching the IGBT Module at 50 kHz (Bias Supply With LM5180-Q1)



From top to bottom: CH1: output voltage 100 mV/div, CH2: gate PWM signal 10 V/div, 20 µs/div

図 53. Voltage Ripple of the –9-V Rail While Switching the IGBT Module at 50 kHz (Bias Supply With LM5180-Q1)

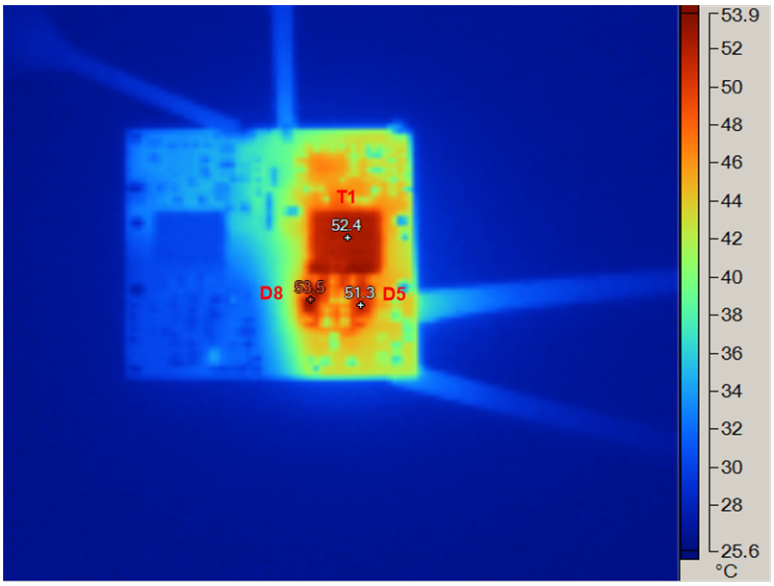


From top to bottom: CH1: output voltage 100 mV/div, CH2: gate PWM signal 10 V/div, 20 µs/div

3.2.1.8 Thermal Image

The thermal of the flyback converter designed with the LM5180-Q1 device is measured under the full-load conditions. The circuit runs at the room temperature for 30 minutes. A 12-V nominal voltage is applied. The converter is loaded with 180 mA. 図 54 shows the thermal image of the board.

図 54. Thermal Image With V_{IN} = 12 V and I_{OUT} = 180 mA (Bias Supply With LM5180-Q1)



T1: Flyback transformer, D8 and D5: secondary rectification diode

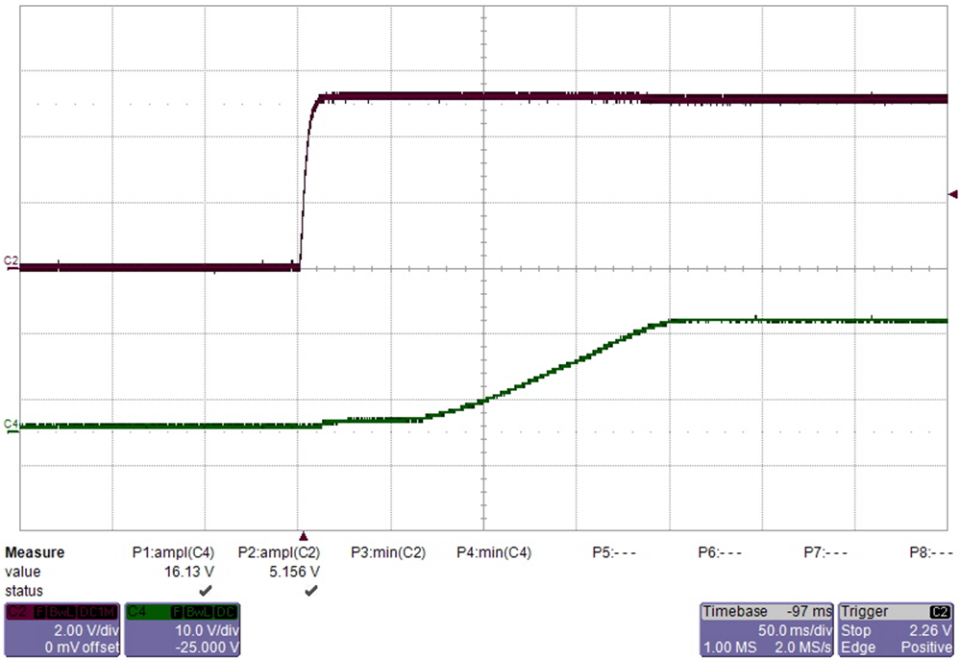
3.2.2 Low-Voltage Tests on the TPS40210-Q1 Flyback Converter

This section presents the experimental results of the bias supply solution 2 which is the flyback converter based on the TPS40210-Q1 device.

3.2.2.1 Startup

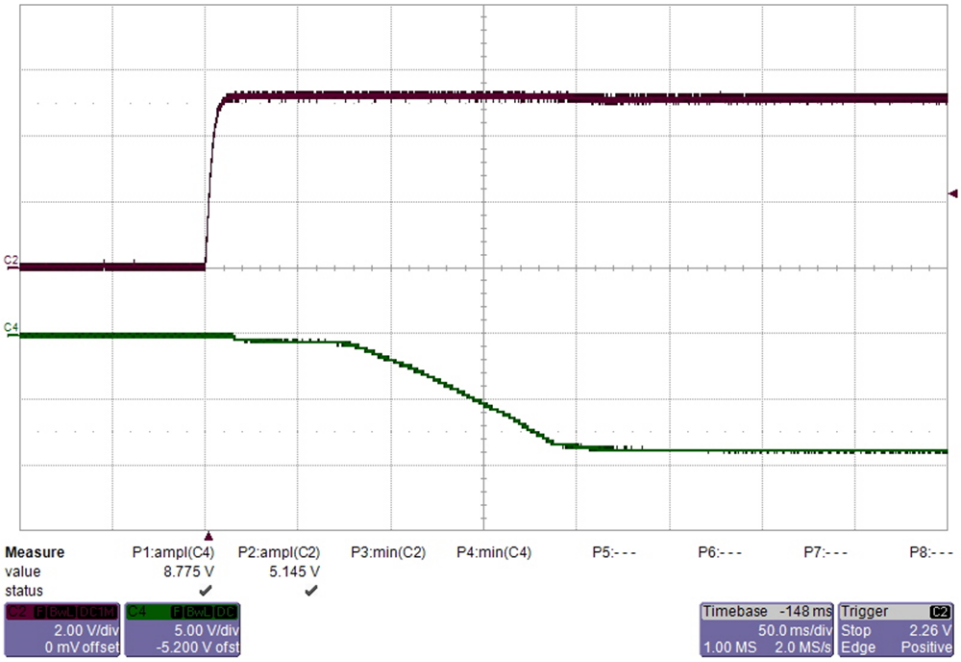
The startup waveforms of the flyback converter designed with the TPS40210-Q1 device are measured under 5- and 12-V inputs, respectively. The +15-V and –9-V rails are measured separately.

図 55. Start-up Waveform of the 15-V Rail With V_{IN} = 5 V and no Load (Bias Supply With TPS40210-Q1)



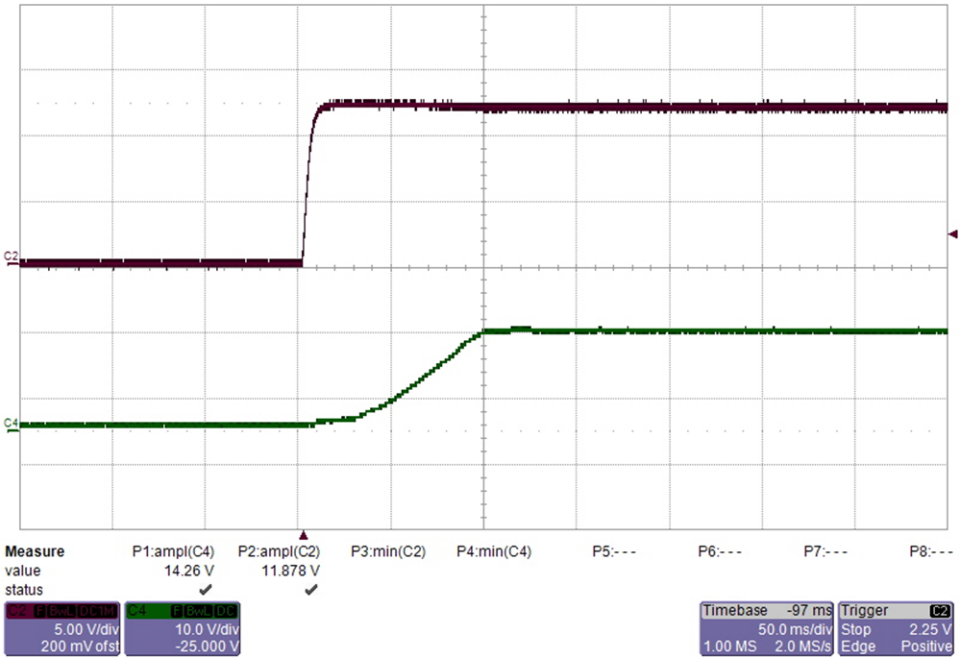
From top to bottom: CH2: input voltage 2 V/div, CH4: output voltage 10 V/div, 50 ms/div

図 56. Start-up Waveform of the –9-V Rail With V_{IN} = 5 V and no Load (Bias Supply With TPS40210-Q1)



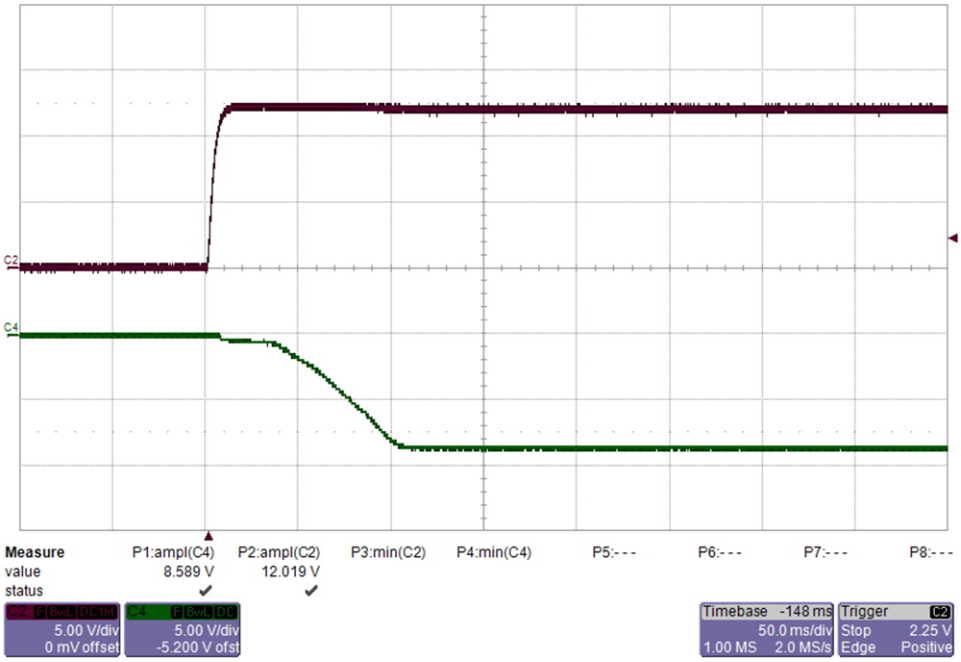
From top to bottom: CH2: input voltage 2 V/div, CH4: output voltage 5 V/div, 50 ms/div

図 57. Start-up Waveform of the 15-V Rail With V_{IN} = 12 V and 180-mA Load (Bias Supply With TPS40210-Q1)



From top to bottom: CH2: input voltage 5 V/div, CH4: output voltage 10 V/div, 50 ms/div

図 58. Start-up Waveform of the –9-V Rail With V_{IN} = 12 V and 180-mA Load (Bias Supply With TPS40210-Q1)

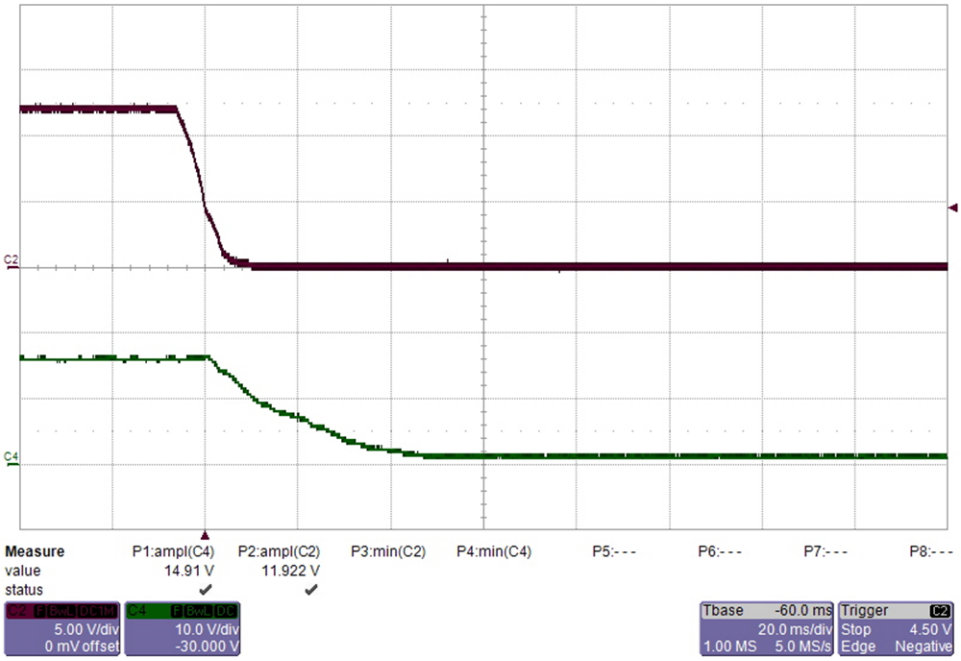


From top to bottom: CH2: input voltage 5 V/div, CH4: output voltage 5 V/div, 50 ms/div

3.2.2.2 Power Down

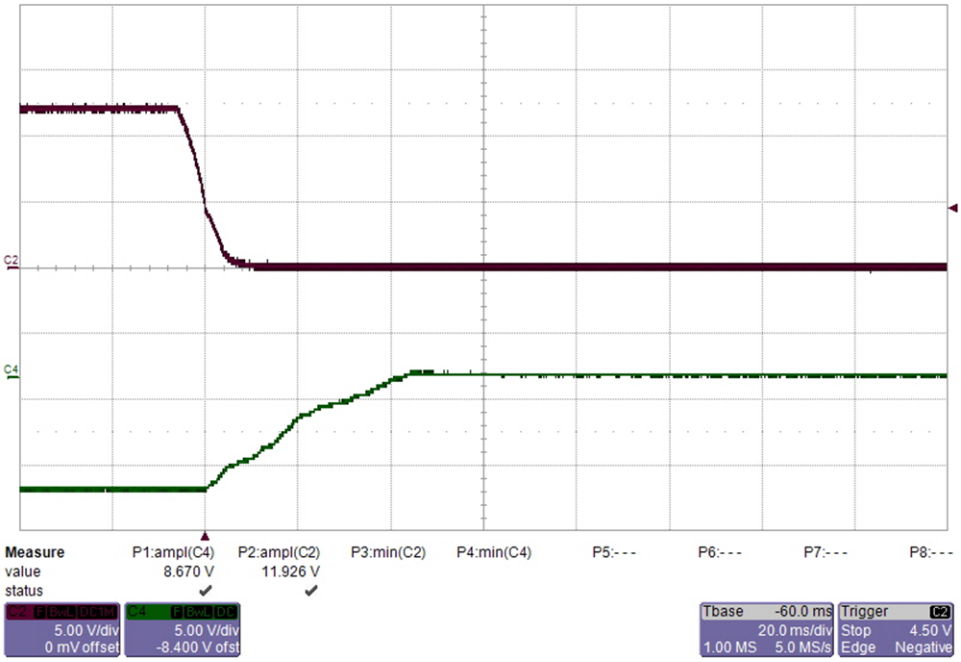
The power down waveforms of the flyback converter designed with the TPS40210-Q1 device are measured under 5- and 12-V inputs, respectively. The +15-V and –9-V rails are measured separately.

図 59. Power-Down Waveform of the 15-V Rail With V_{IN} = 12 V and no Loa (Bias Supply With TPS40210-Q1)



From top to bottom: CH3: input voltage 5 V/div, CH4: output voltage 10 V/div, 20 ms/div

図 60. Power-Down Waveform of the –9-V Rail With V_{IN} = 12 V and no Load (Bias Supply With TPS40210-Q1)

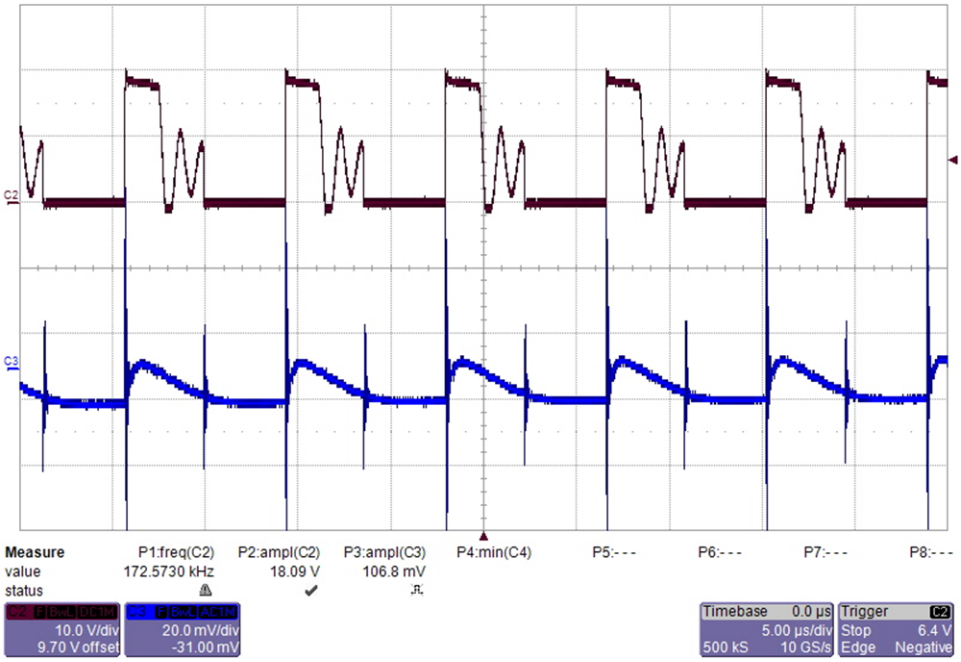


From top to bottom: CH3: input voltage 5 V/div, CH4: output voltage 5 V/div, 20 ms/div

3.2.2.3 Switch Node and Output Voltage Ripple

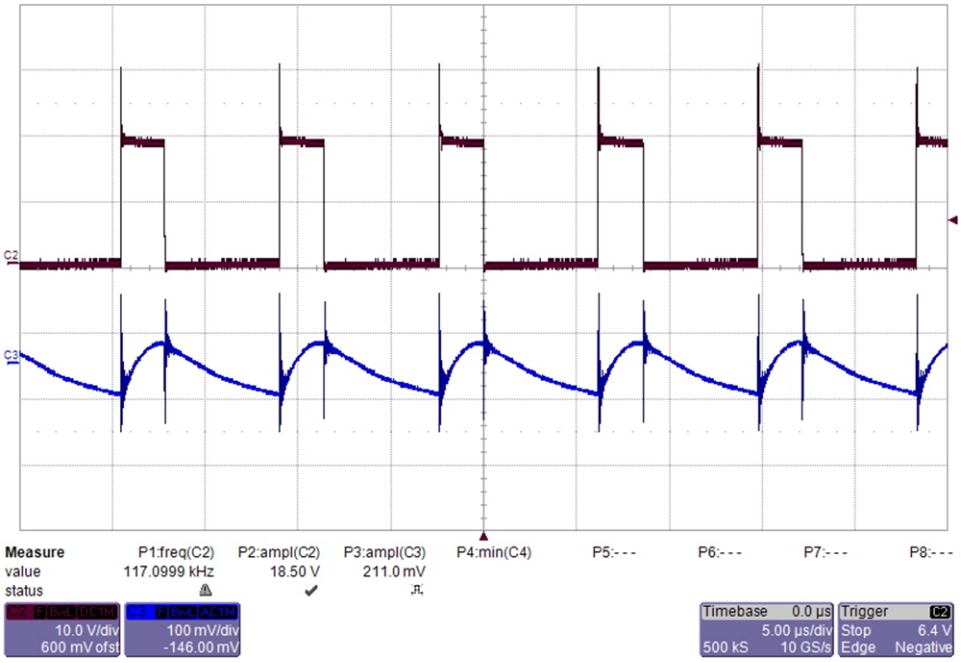
The switch node and output voltage ripple of the flyback converter designed with the TPS40210-Q1 device are measured under 5-, 12-, and 18-V inputs, respectively. The 15-V and –9-V rails are measured separately.

図 61. Switch Node and Output Ripple of the 15-V Rail With V_{IN} = 5 V and no Load (Bias Supply With TPS40210-Q1)



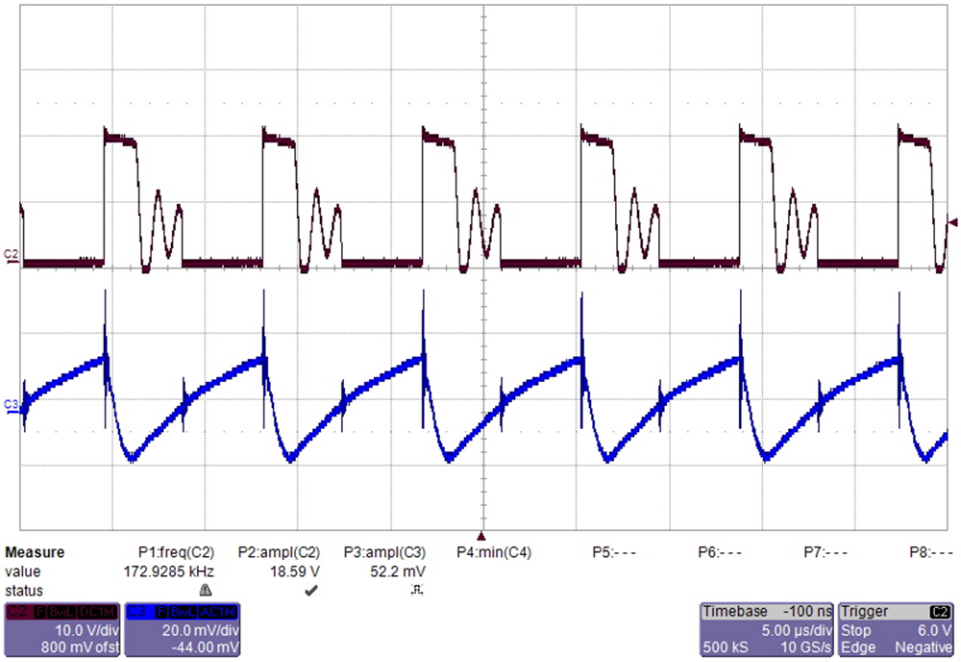
From top to bottom: CH2: switch node 10 V/div, CH3: output voltage ripple 20 mV/div, 5 µs/div

図 62. Switch Node and Output Ripple of the 15-V Rail With V_{IN} = 5 V and 80-mA Load (Bias Supply With TPS40210-Q1)



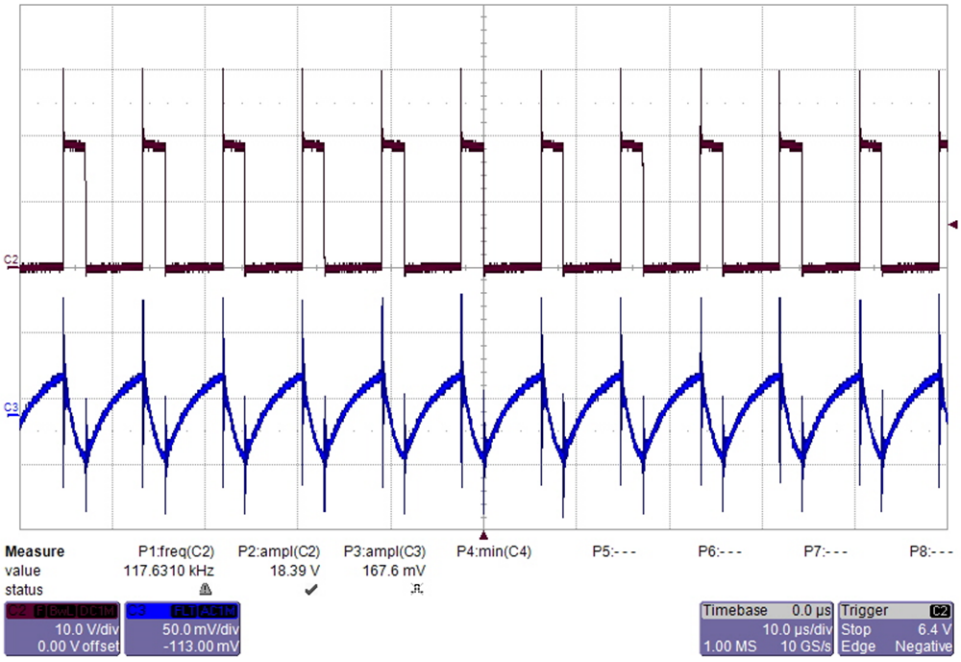
From top to bottom: CH2: switch node 10 V/div, CH3: output voltage ripple 100 mV/div, 5 µs/div

図 63. Switch Node and Output Ripple of the –9-V Rail With V_{IN} = 5 V and no Load (Bias Supply With TPS40210-Q1)



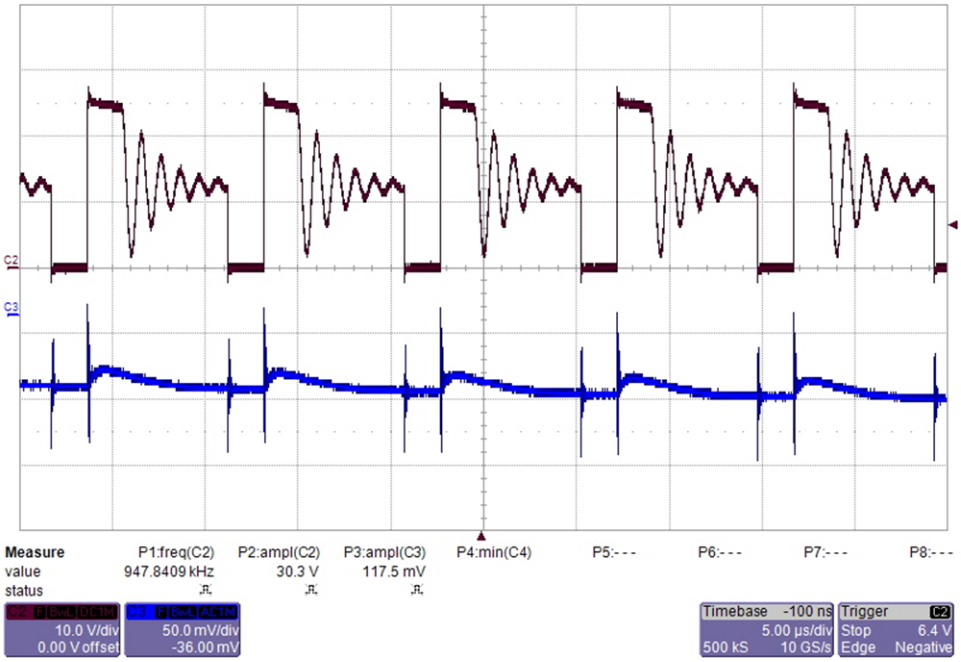
From top to bottom: CH2: switch node 10 V/div, CH3: output voltage ripple 20 mV/div, 5 µs/div

図 64. Switch Node and Output Ripple of the –9-V Rail With V_{IN} = 5 V and 80-mA Load (Bias Supply With TPS40210-Q1)



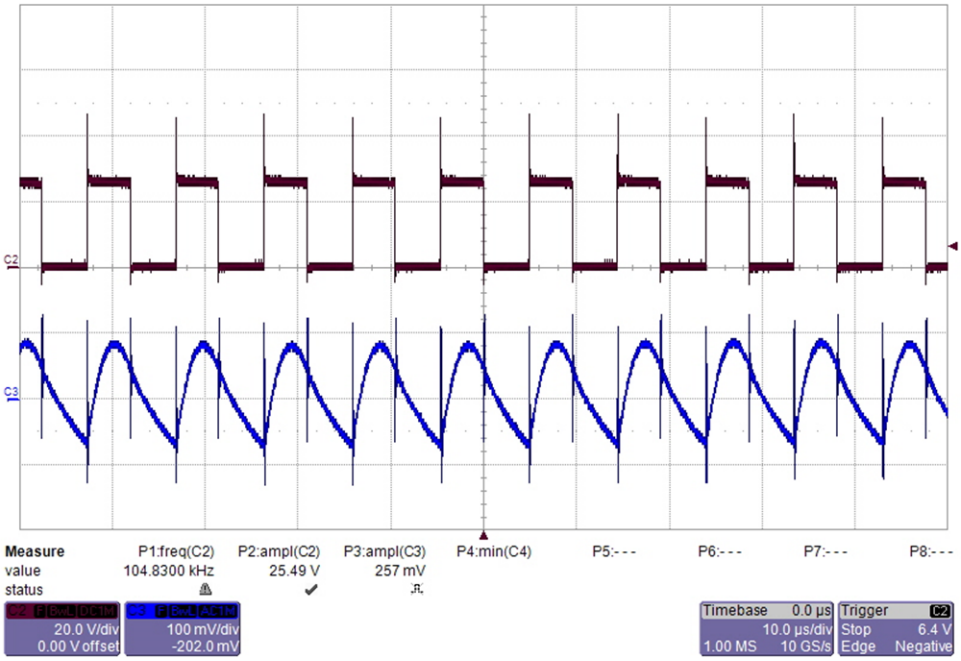
From top to bottom: CH2: switch node 10 V/div, CH3: output voltage ripple 50 mV/div, 10 µs/div

図 65. Switch Node and Output Ripple of the 15-V Rail With V_{IN} = 12 V and no Load (Bias Supply With TPS40210-Q1)



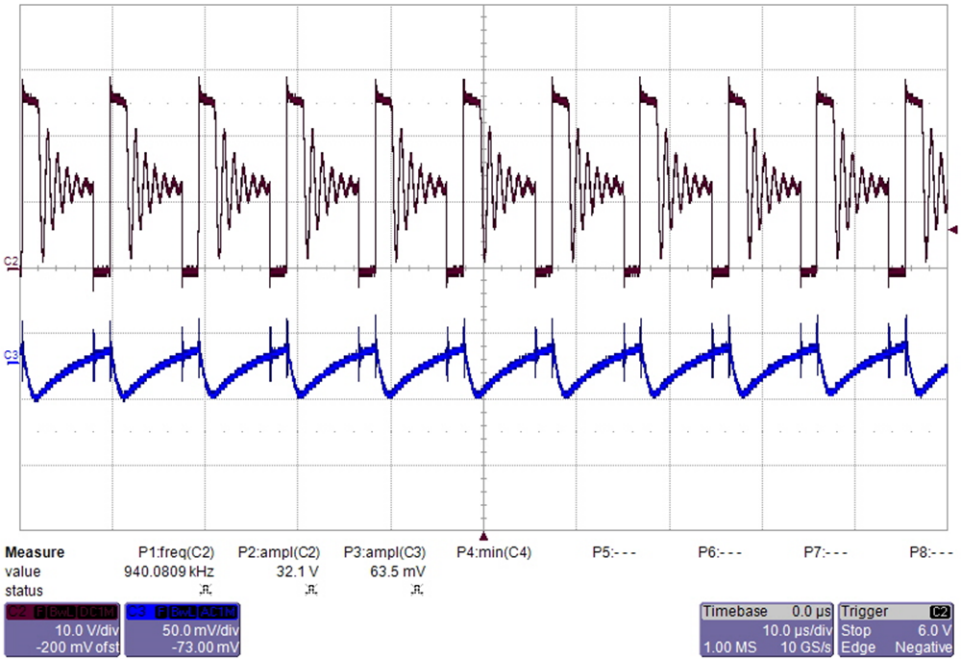
From top to bottom: CH2: switch node 10 V/div, CH3: output voltage ripple 50 mV/div, 5 µs/div

図 66. Switch Node and Output Ripple of the 15-V Rail With V_{IN} = 12 V and 180-mA Load (Bias Supply With TPS40210-Q1)



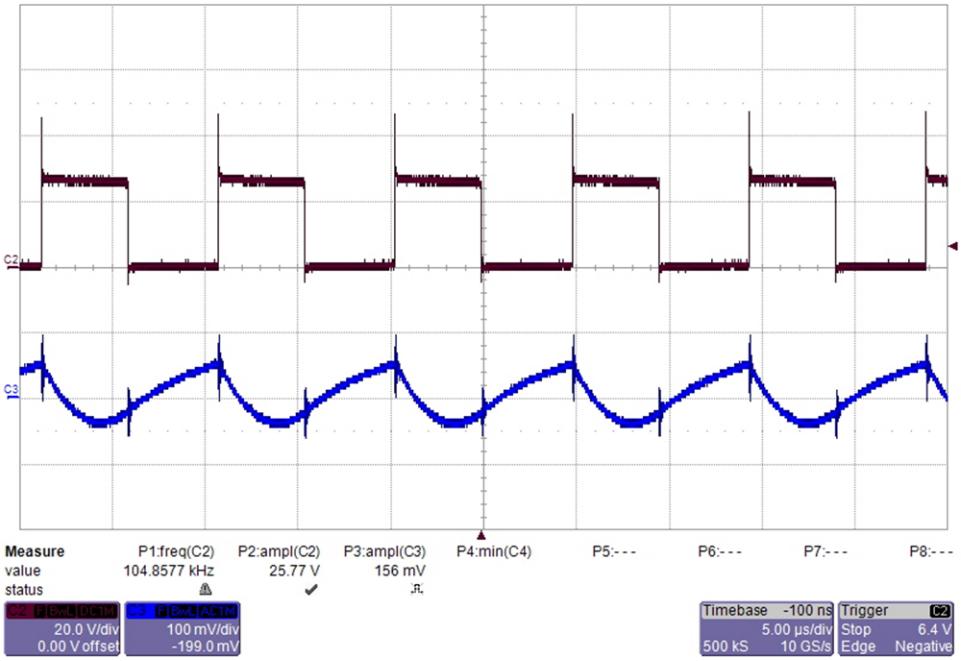
From top to bottom: CH2: switch node 20 V/div, CH3: output voltage ripple 100 mV/div, 10 µs/div

図 67. Switch Node and Output Ripple of the –9-V Rail With V_{IN} = 12 V and no Load (Bias Supply With TPS40210-Q1)



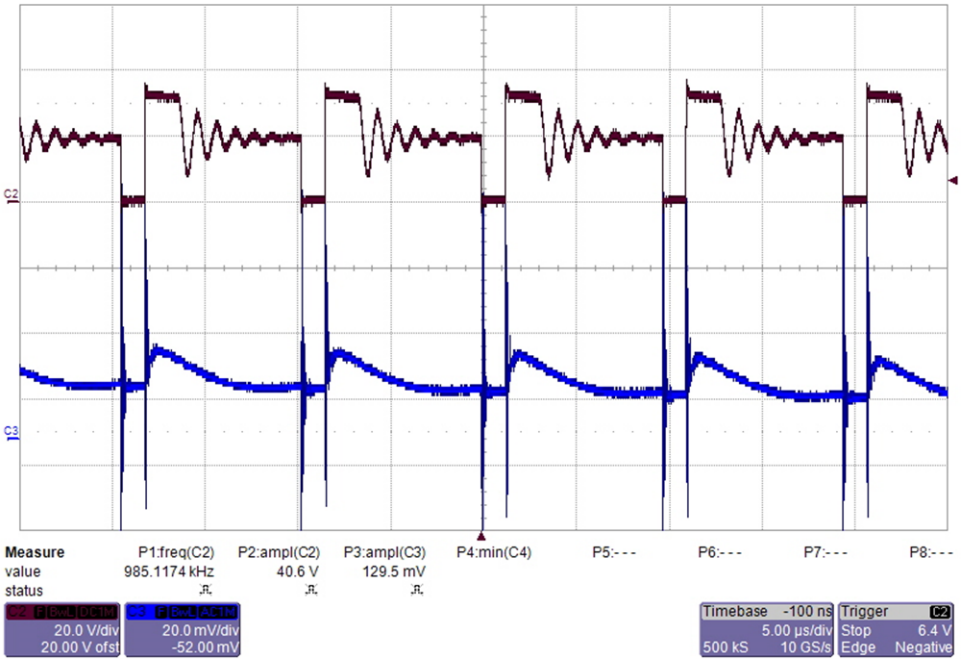
From top to bottom: CH2: switch node 10 V/div, CH3: output voltage ripple 50 mV/div, 10 µs/div

図 68. Switch Node and Output Ripple of the –9-V Rail With V_{IN} = 12 V and 180-mA Load (Bias Supply With TPS40210-Q1)



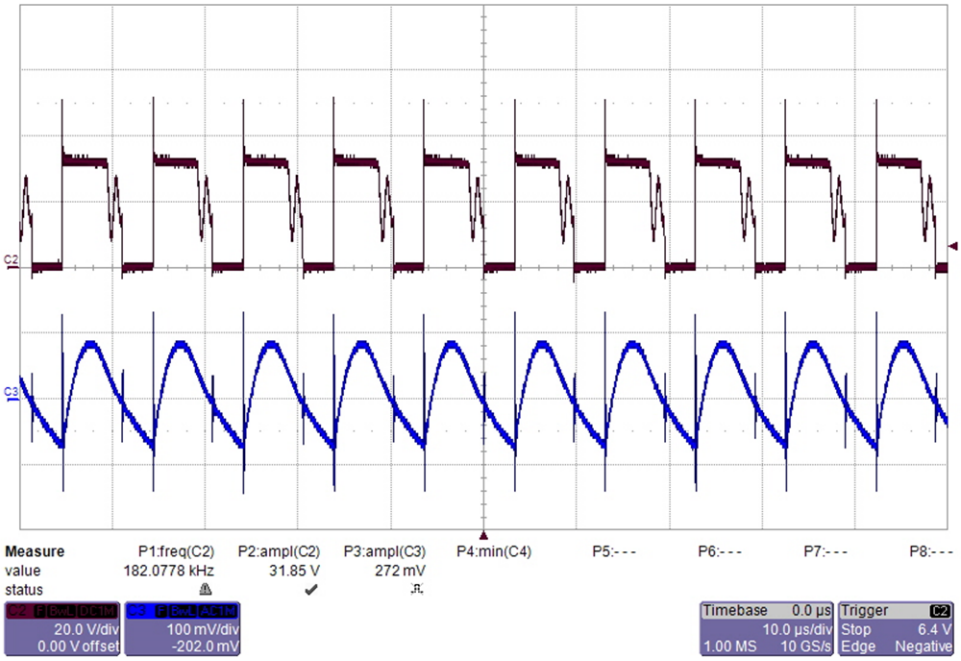
From top to bottom: CH2: switch node 20 V/div, CH3: output voltage ripple 100 mV/div, 5 µs/div

図 69. Switch Node and Output Ripple of the 15-V Rail With V_{IN} = 18 V and no Load (Bias Supply With TPS40210-Q1)



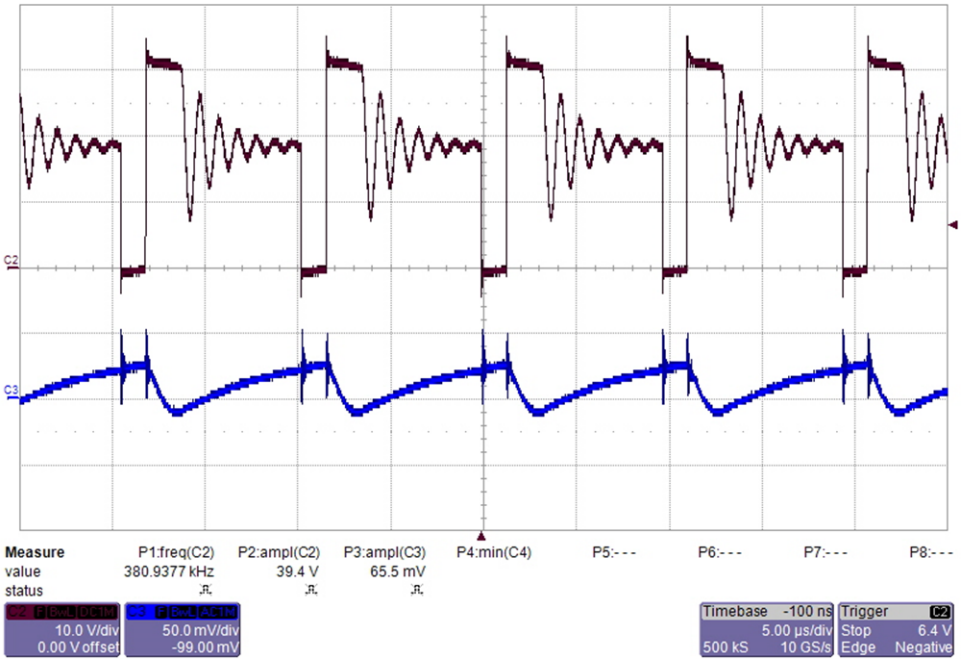
From top to bottom: CH2: switch node 20 V/div, CH3: output voltage ripple 20 mV/div, 5 µs/div

図 70. Switch Node and Output Ripple of the 15-V Rail With V_{IN} = 18 V and 180-mA Load (Bias Supply With TPS40210-Q1)



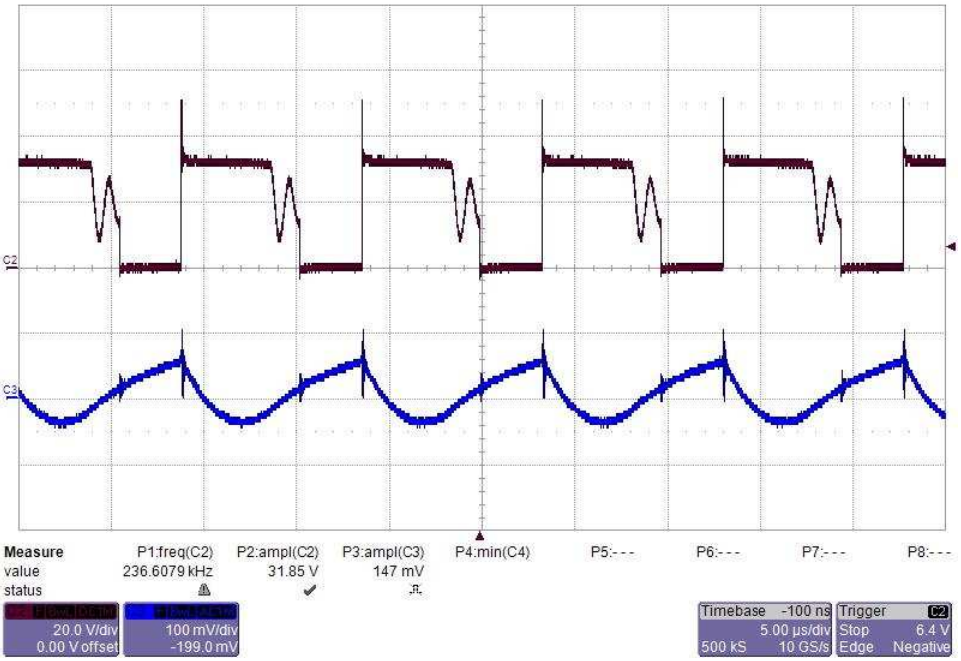
From top to bottom: CH2: switch node 20 V/div, CH3: output voltage ripple 100 mV/div, 10 µs/div

図 71. Switch Node and Output Ripple of the –9-V Rail With V_{IN} = 18 V and no Load (Bias Supply With TPS40210-Q1)



From top to bottom: CH2: switch node 10 V/div, CH3: output voltage ripple 50 mV/div, 5 µs/div

図 72. Switch Node and Output Ripple of the –9-V Rail With V_{IN} = 18 V and 180-mA Load (Bias Supply With TPS40210-Q1)

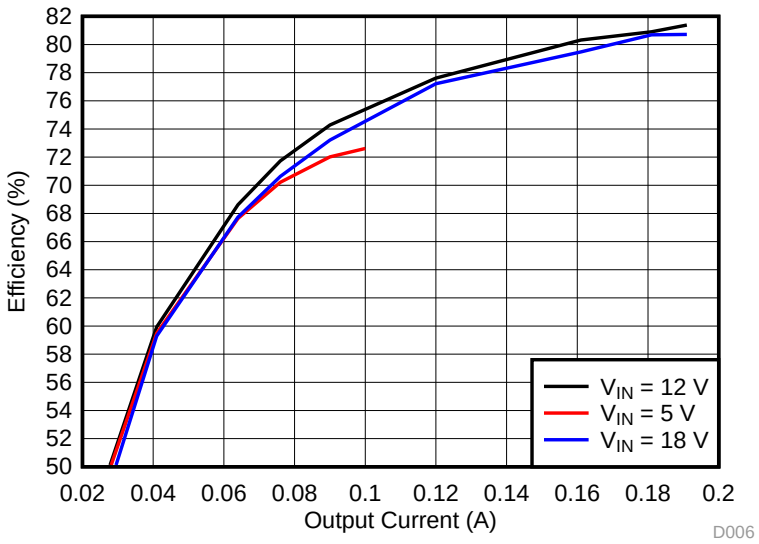


From top to bottom: CH2: switch node 20 V/div, CH3: output voltage ripple 100 mV/div, 5 µs/div

3.2.2.4 Efficiency

図 73 shows the measured efficiency of the flyback converter designed with the TPS40210-Q1 device over the full load range. As can be seen, around 81.5% peak efficiency is achieved with the input voltages of 5 V, 12 V, and 18 V, respectively.

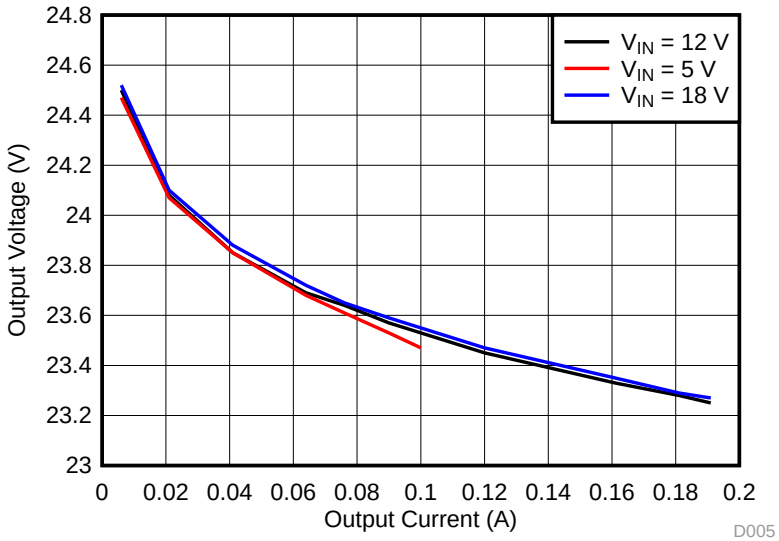
図 73. Measured Efficiency Under Input Voltages of 5 V, 12 V, and 18 V (Bias Supply With TPS40210-Q1)



3.2.2.5 Load Regulation

Load regulation measurements show the % deviation from nominal output voltage as a function of output current. 図 74 shows the measured result of the flyback converter designed with the TPS40210-Q1 device. The load regulation is measured with the input voltages of 5 V, 12 V, and 18 V, respectively.

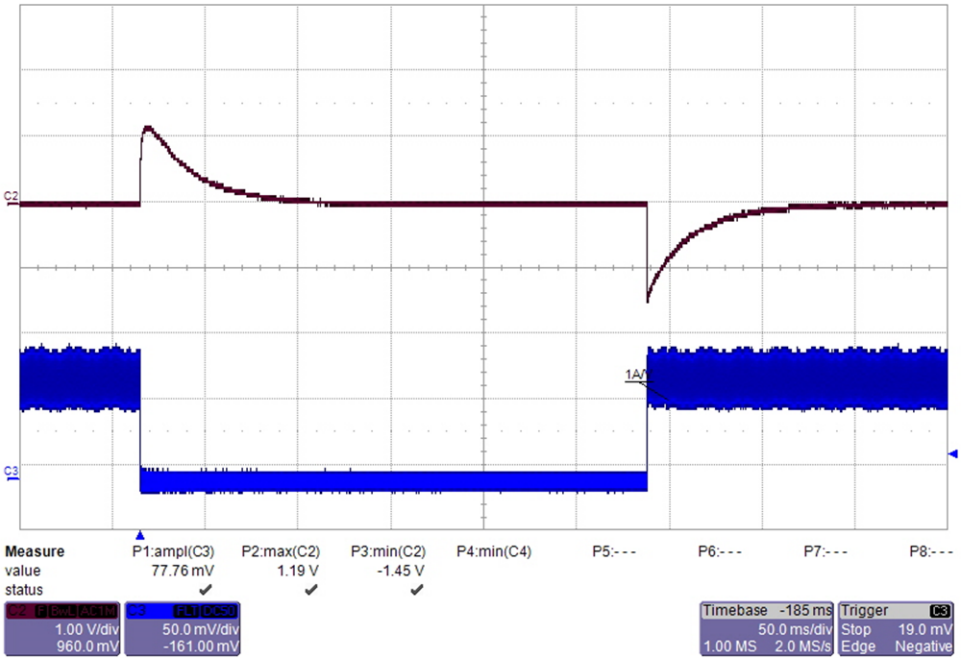
図 74. Load Regulation Under Input Voltages of 5 V, 12 V, and 18 V (Bias Supply With TPS40210-Q1)



3.2.2.6 Load Transients

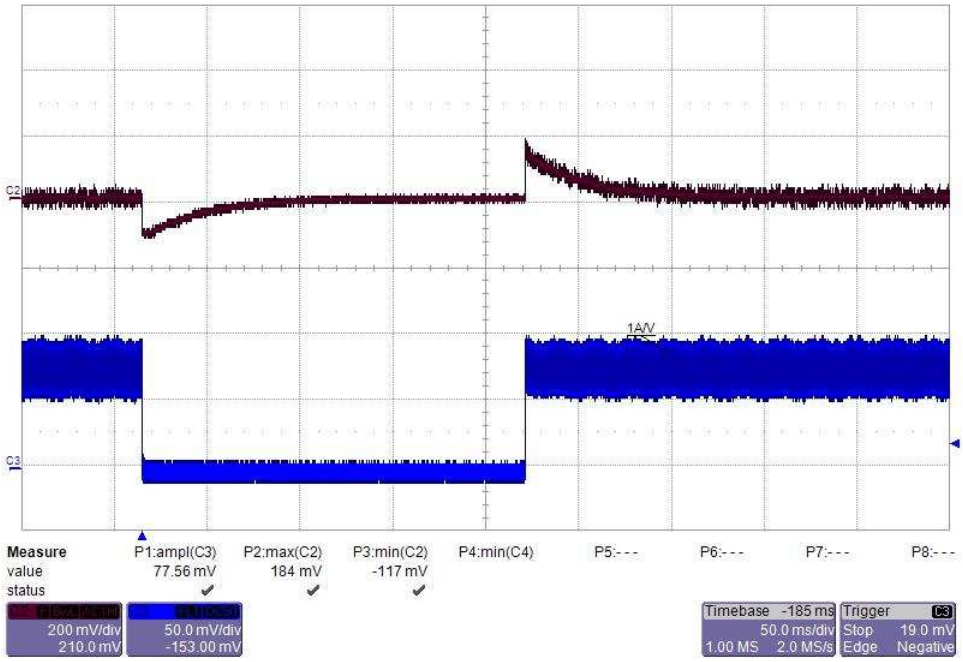
This section shows load transient measurements of the flyback converter designed with the TPS40210-Q1 device. Load transient response presents how well a power supply copes with the changes in the load-current demand. During the test, the load is switching from 0 to full, under input voltages of 5 V, 12 V, and 18 V, respectively.

図 75. Load Transient Response of the 15-V Rail Under V_{IN} = 5 V and I_{OUT} Switching Between 0 and 80 mA (Bias Supply With TPS40210-Q1)



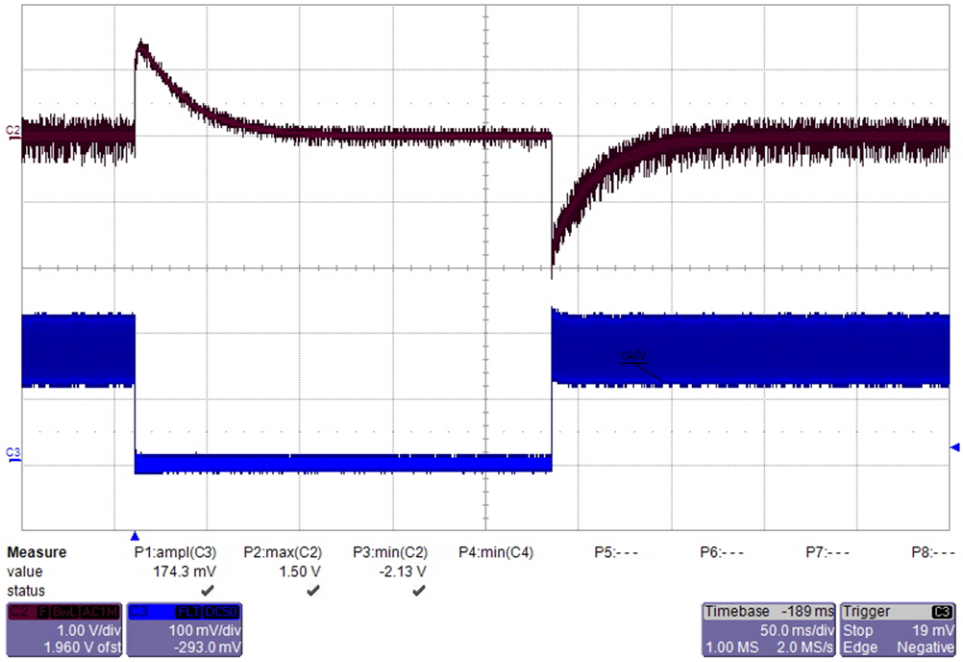
From top to bottom: CH2: output voltage 1 V/div, CH3: load current 500 mA/div, 50 ms/div

図 76. Load Transient Response of the –9-V rail Under V_{IN} = 5 V and I_{OUT} Switching Between 0 and 80 mA (Bias Supply With TPS40210-Q1)



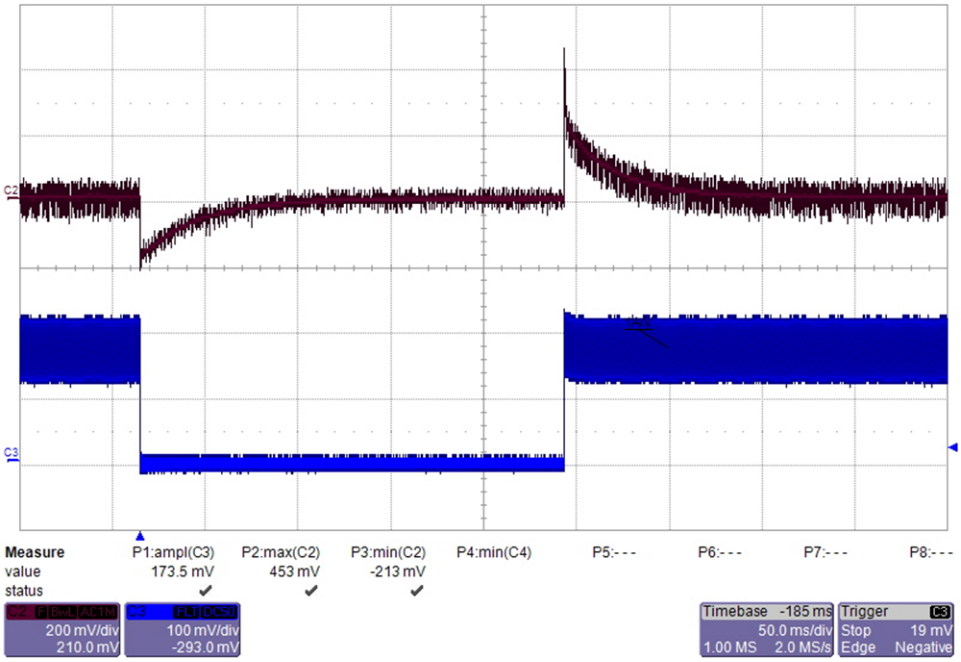
From top to bottom: CH2: output voltage 200 mV/div, CH3: load current 500 mA/div, 50 ms/div

図 77. Load Transient Response of the 15-V Rail Under V_{IN} = 12 V and I_{OUT} Switching Between 0 and 180 mA (Bias Supply With TPS40210-Q1)



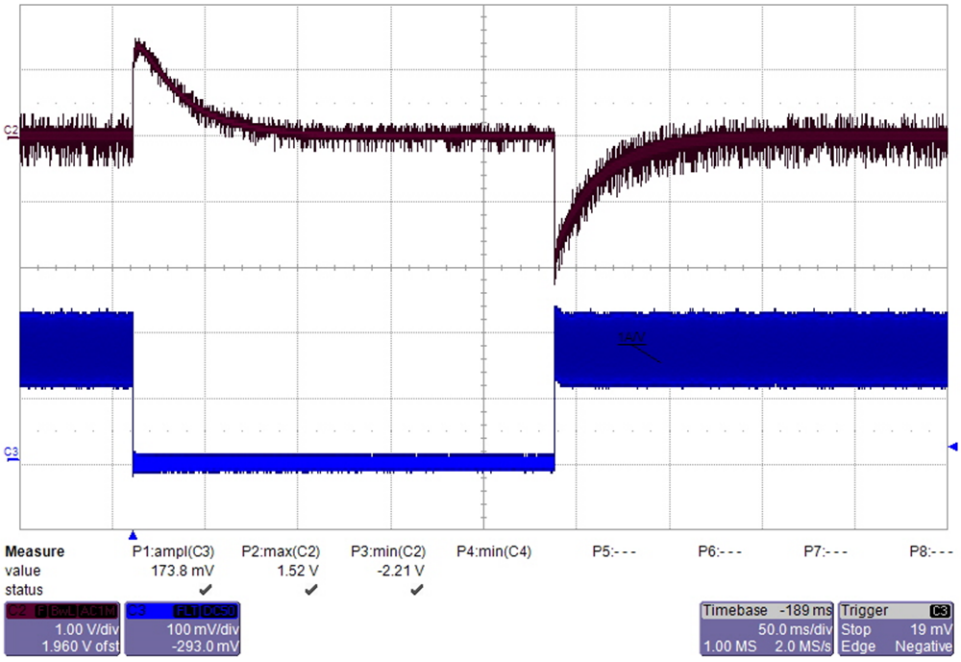
From top to bottom: CH2: output voltage 1 V/div, CH3: load current 1 A/div, 50 ms/div

図 78. Load Transient Response of the –9-V Rail Under V_{IN} = 12 V and I_{OUT} Switching Between 0 and 180 mA (Bias Supply With TPS40210-Q1)



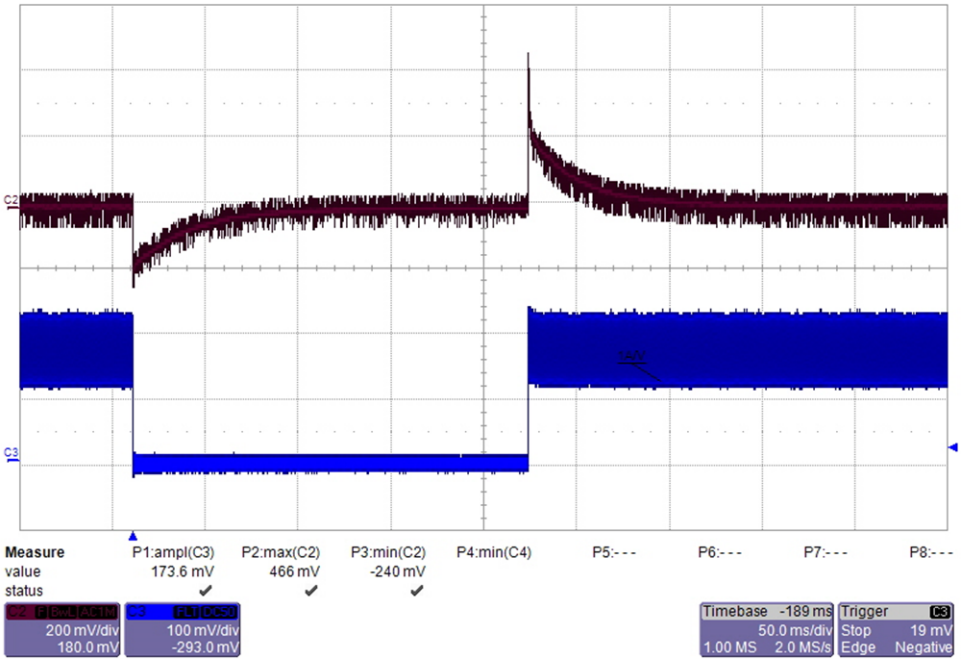
From top to bottom: CH2: output voltage 200 mV/div, CH3: load current 1 A/div, 50 ms/div

図 79. Load Transient Response of the 15-V Rail Under V_{IN} = 18 V and I_{OUT} Switching Between 0 and 180 mA (Bias Supply With TPS40210-Q1)



From top to bottom: CH2: output voltage 1 V/div, CH3: load current 1 A/div, 50 ms/div

図 80. Load Transient Response of the –9-V Rail Under V_{IN} = 18 V and I_{OUT} Switching Between 0 and 180 mA (Bias Supply With TPS40210-Q1)

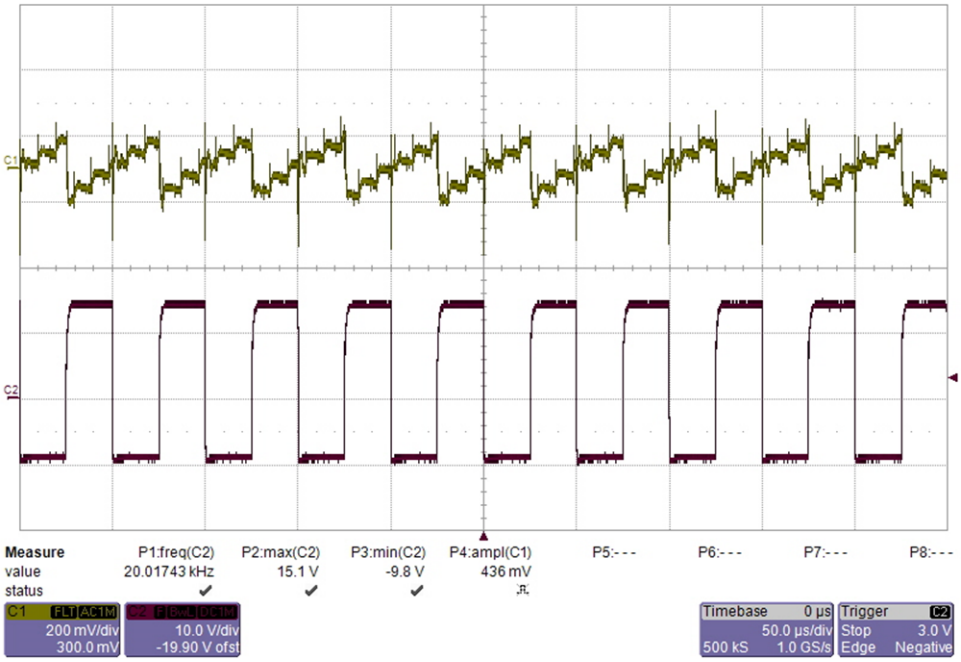


From top to bottom: CH2: output voltage 200 mV/div, CH3: load current 1 A/div, 50 ms/div

3.2.2.7 Voltage Ripple While Switching IGBT

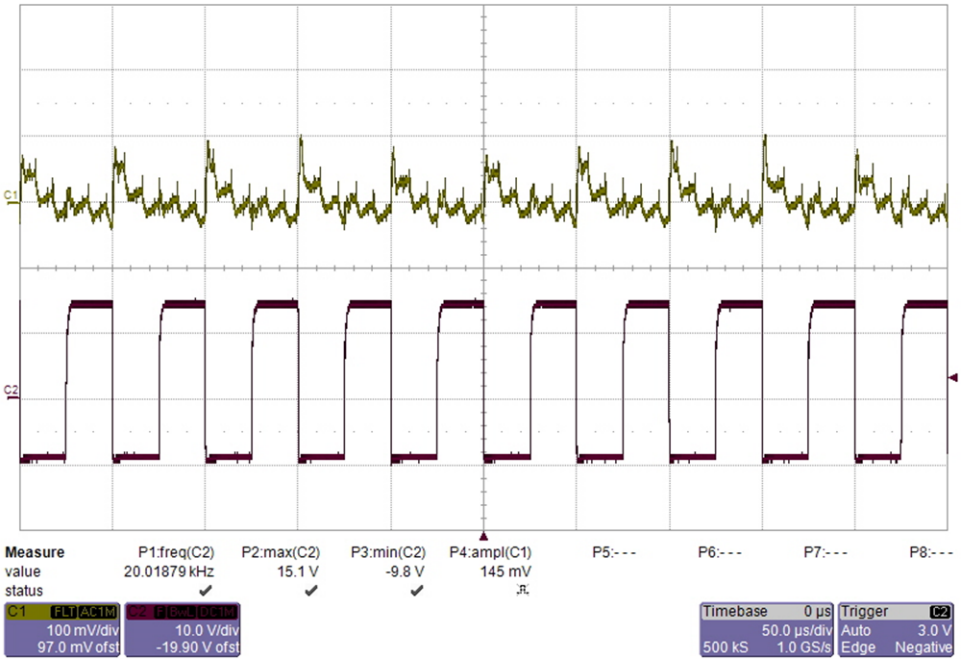
The flyback converter designed with the TPS40210-Q1 device is connected to the isolated gate drivers (ISO5852S-Q1) and the 1200-V IGBT module (FF150R12MS4G) for checking the voltage ripple during the switching transients. The IGBTs are switched at 20- and 50-kHz frequencies, respectively.

図 81. Voltage Ripple of the 15-V Rail While Switching the IGBT Module at 20 kHz (Bias Supply With TPS40210-Q1)



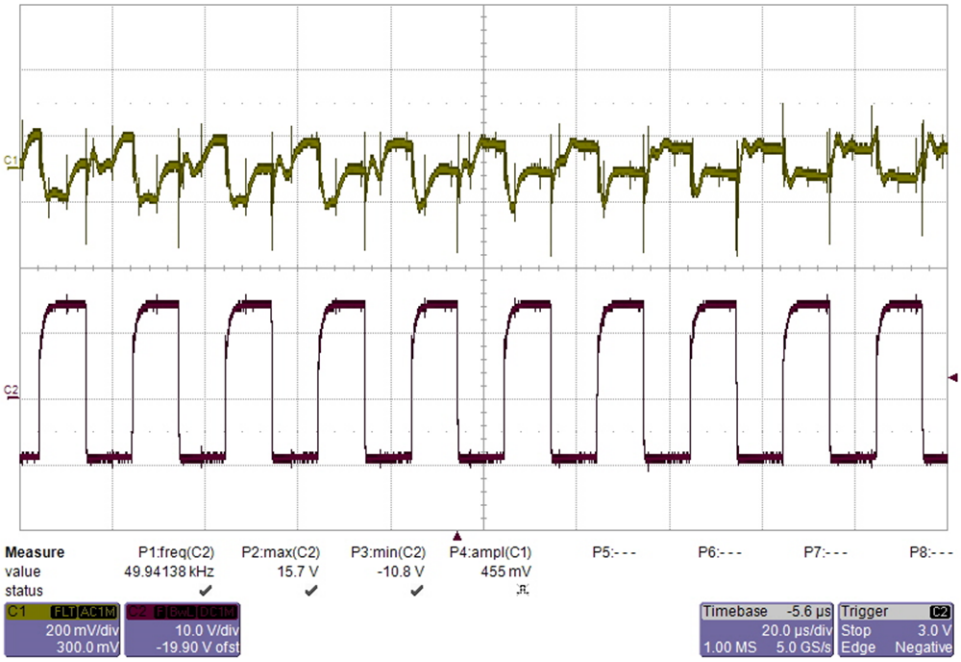
From top to bottom: CH1: output voltage 200 mV/div, CH2: gate PWM signal 10 V/div, 50 µs/div

図 82. Voltage Ripple of the –9-V Rail While Switching the IGBT Module at 20 kHz (Bias Supply With TPS40210-Q1)



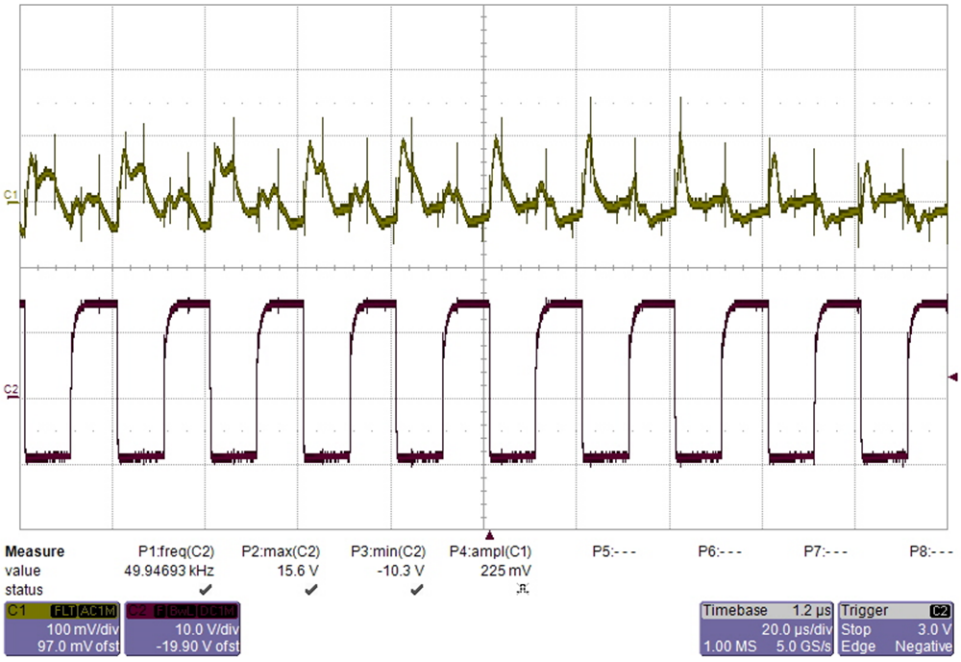
From top to bottom: CH1: output voltage 100 mV/div, CH2: gate PWM signal 10 V/div, 50 µs/div

図 83. Voltage Ripple of the 15-V Rail While Switching the IGBT Module at 50 kHz (Bias Supply With TPS40210-Q1)



From top to bottom: CH1: output voltage 200 mV/div, CH2: gate PWM signal 10 V/div, 20 µs/div

図 84. Voltage Ripple of the –9-V Rail While Switching the IGBT Module at 50 kHz (Bias Supply With TPS40210-Q1)

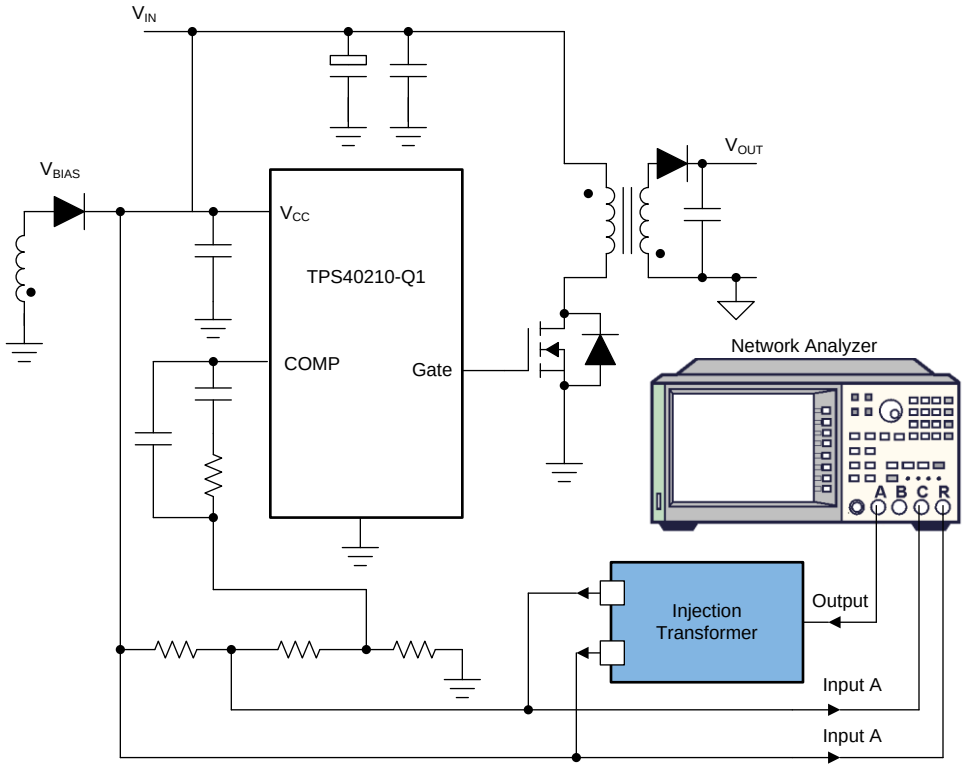


From top to bottom: CH1: output voltage 100 mV/div, CH2: gate PWM signal 10 V/div, 20 µs/div

3.2.2.8 Control-Loop Frequency Response

The control loop frequency response represents the stability of the power-supply system. The TPS40210-Q1-based flyback converter loop frequency response is measured under various loads and input voltages, respectively. The measurement setup is shown in 図 85. The output of the network analyzer is connected to the injection resistor. The outputs are also connected to the input channel A and channel B, respectively.

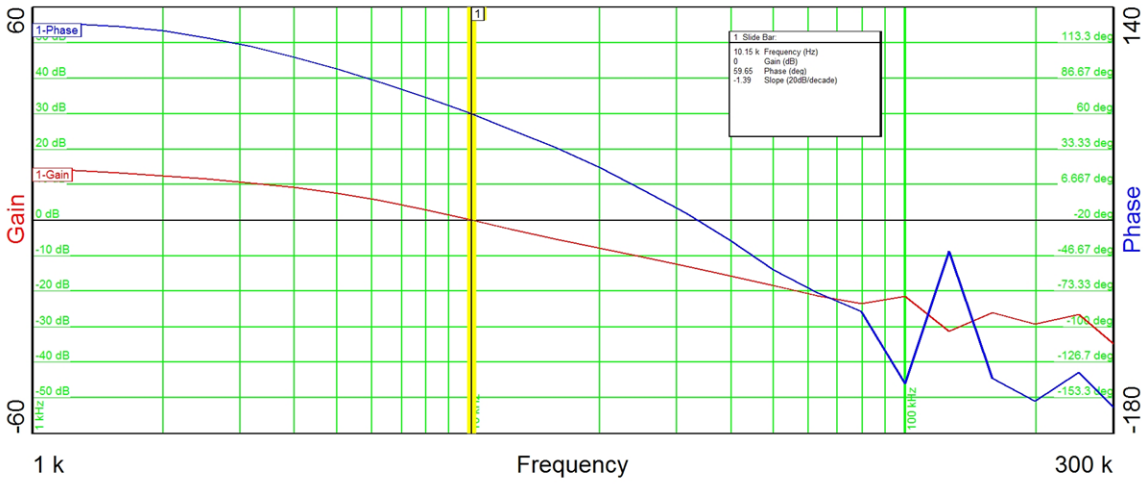
図 85. Control-Loop Frequency Response Measurement Setup



For TPS40210-Q1 based flyback converter only

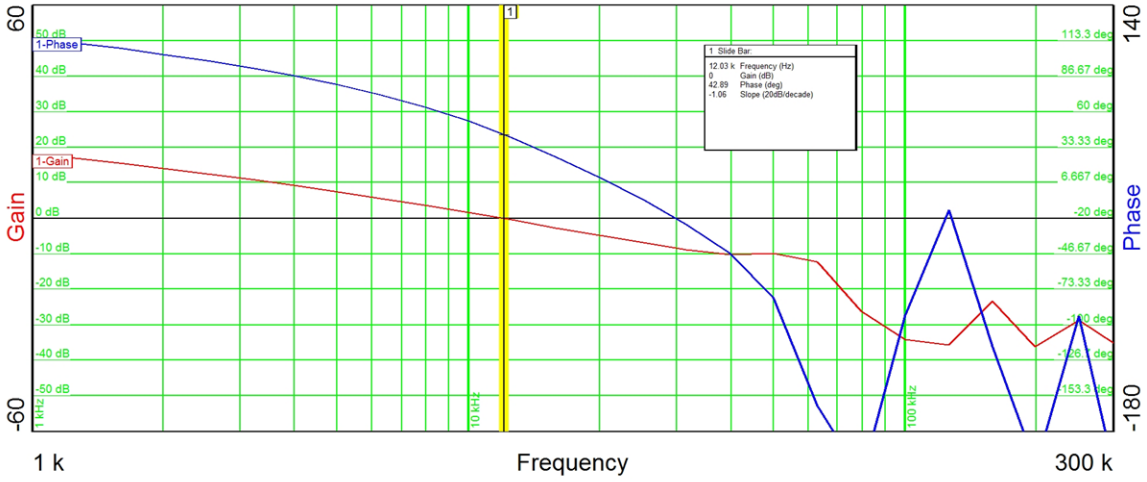
The loop frequency response of the buck converter is tested under various conditions. The measured results are shown from 図 86 to 図 91.

図 86. Loop Frequency Response With V_{IN} = 5 V and I_{OUT} = 10 mA (Bias Supply With TPS40210-Q1)



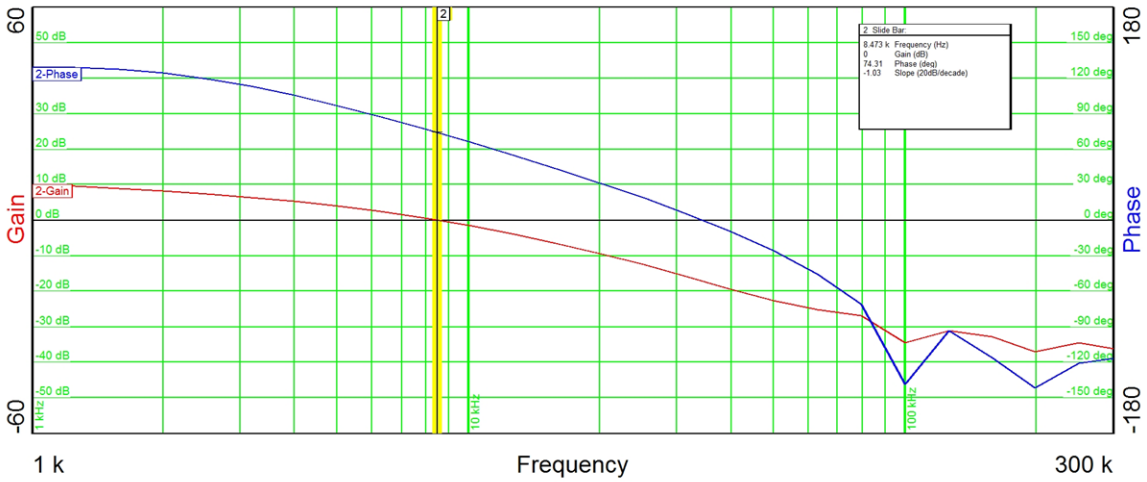
Crossover frequency: 10.15 kHz, achieved phase margin: 59 deg, achieved gain margin: 15 dB

図 87. Loop Frequency Response With V_{IN} = 5 V and I_{OUT} = 80 mA (Bias Supply With TPS40210-Q1)



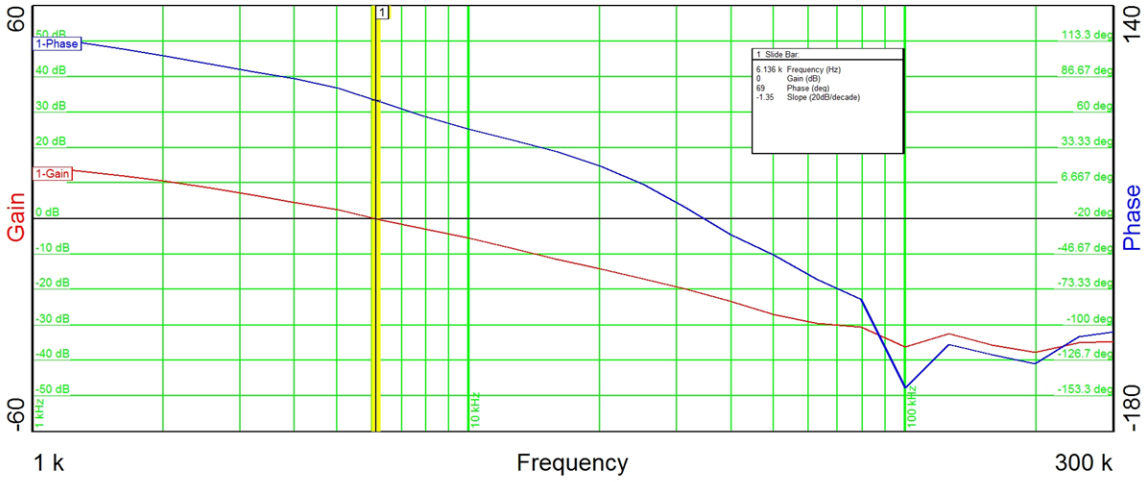
Crossover frequency: 12.03 kHz, achieved phase margin: 42.9 deg, achieved gain margin: 10 dB

図 88. Loop Frequency Response With V_{IN} = 12 V and I_{OUT} = 10 mA (Bias Supply With TPS40210-Q1)



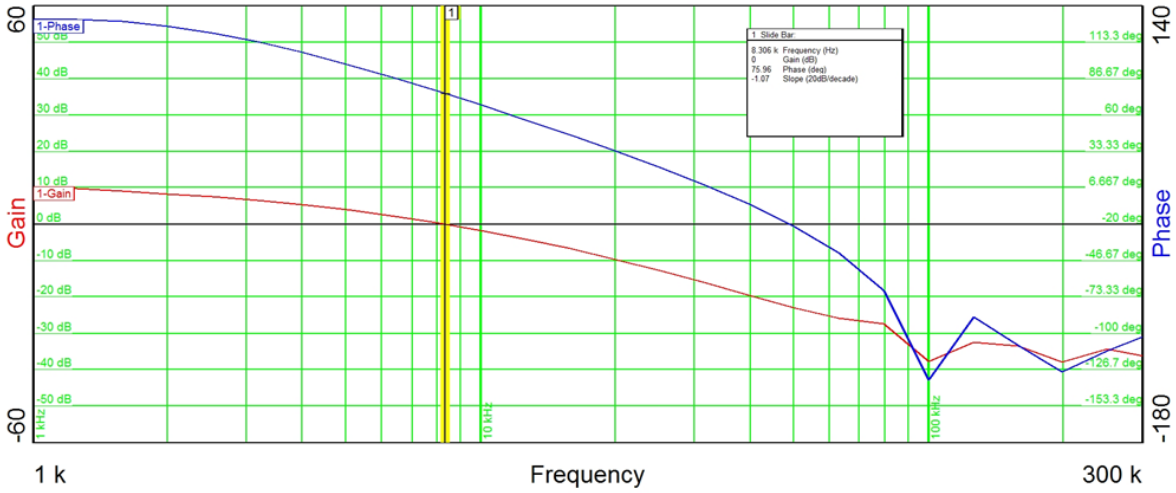
Crossover Frequency: 8.5 kHz, achieved phase margin: 74.3 deg, achieved gain margin: 18 dB

図 89. Loop Frequency Response With V_{IN} = 12 V and I_{OUT} = 180 mA (Bias Supply With TPS40210-Q1)



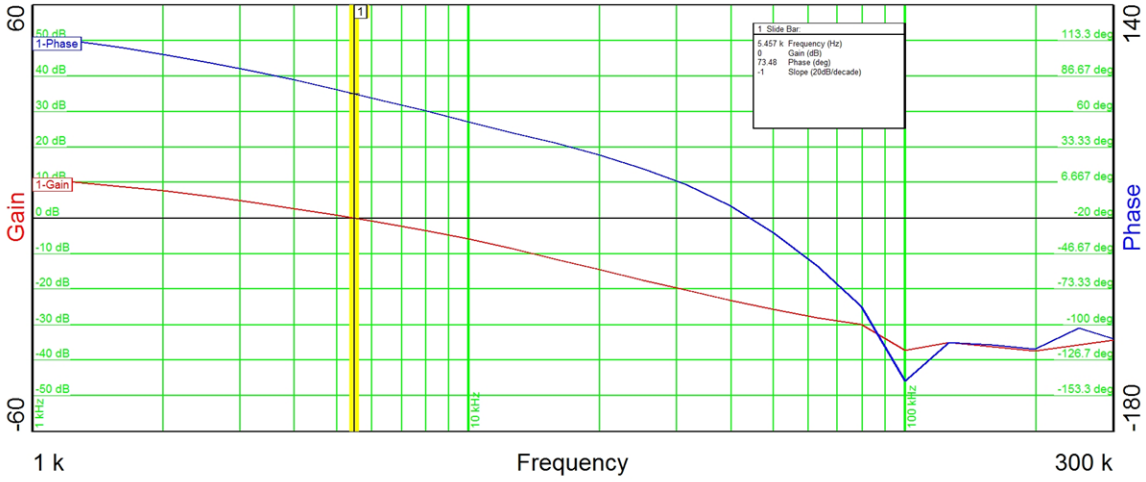
Crossover frequency: 6.1 kHz, achieved phase margin: 69 deg, achieved gain margin: 23 dB

図 90. Loop Frequency Response With V_{IN} = 18 V and I_{OUT} = 10 mA (Bias Supply With TPS40210-Q1)



Crossover frequency: 8.3 kHz, achieved phase margin: 76 deg, achieved gain margin: 23 dB

図 91. Loop Frequency Response With V_{IN} = 18 V and I_{OUT} = 180 mA (Bias Supply With TPS40210-Q1)

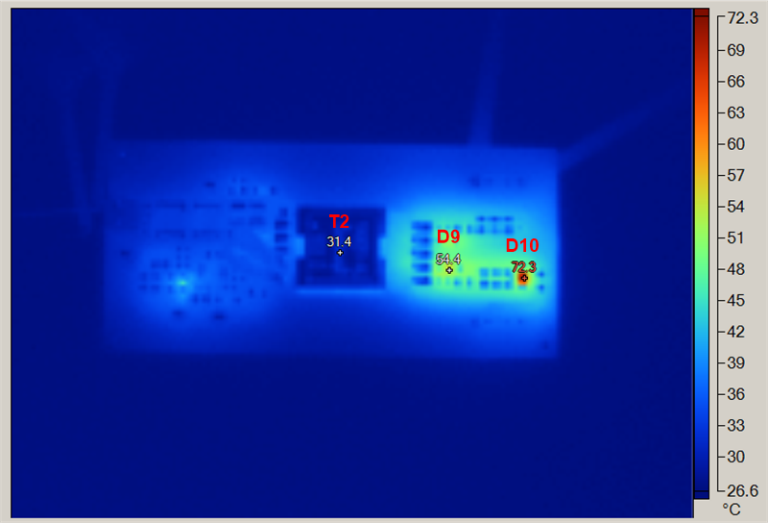


Crossover frequency: 5.5 kHz, achieved phase margin: 73.4 deg, achieved gain margin: 25 dB

3.2.2.9 Thermal Image

The thermal of the flyback converter designed with the TPS40210-Q1 device is measured under the full-load conditions. The circuit runs at the room temperature for 30 minutes. A 12-V nominal voltage is applied. The converter is loaded with 180 mA. 図 92 shows the thermal image of the board.

図 92. Thermal Image With V_{IN} = 12 V and I_{OUT} = 180 mA (Bias Supply With TPS40210-Q1)



T2: Flyback transformer, D9: secondary rectification diode, D10: output Zener diode

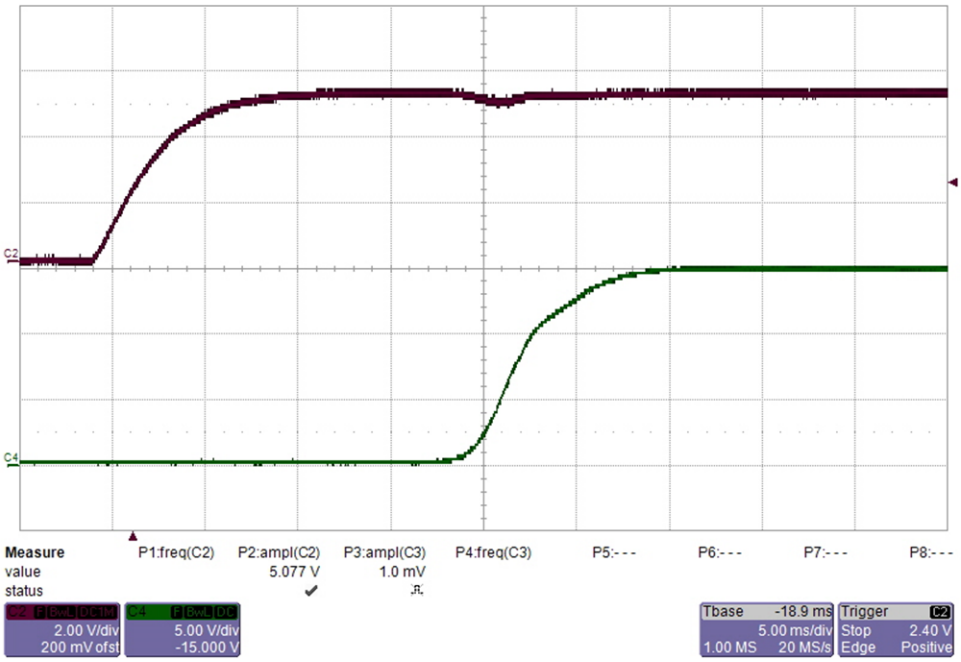
3.2.3 Low Voltage Tests on Buck With Push-Pull Transformer Driver Supply

This section presents the experimental results of the bias supply solution 3 which is the buck converter plus the push-pull transformer driver supply based on the LM46002-Q1 and SN6505-Q1 devices.

3.2.3.1 Startup

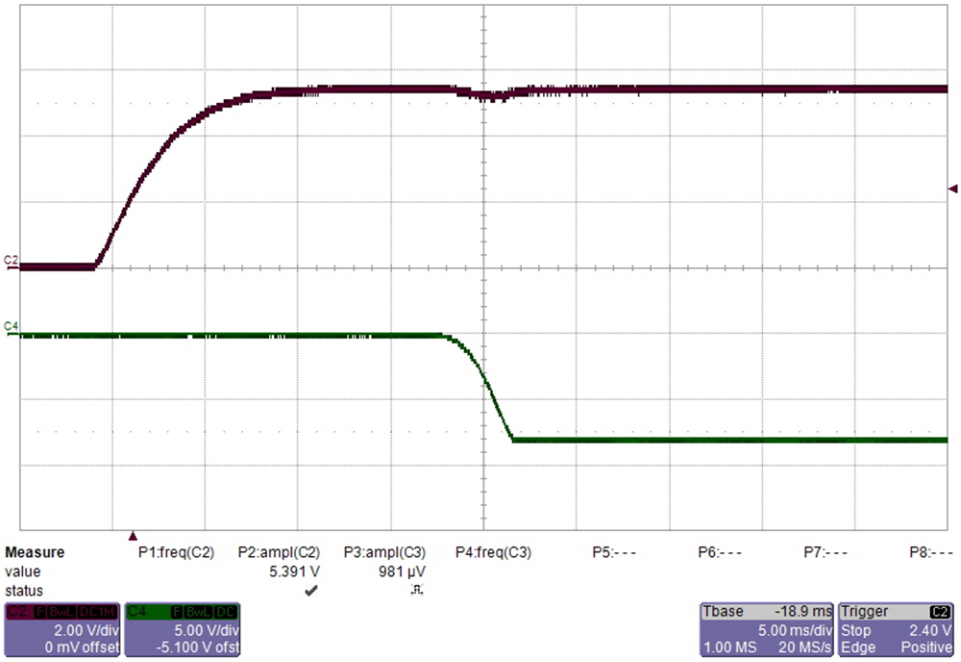
The start-up waveforms of the buck with push-pull transformer driver supply are measured under 5- and 12-V inputs, respectively. The +15-V and –9-V rails are measured separately.

図 93. Start-up Waveform of the 15-V Rail With V_{IN} = 5 V and no Load (Bias Supply With Buck and Push Pull)



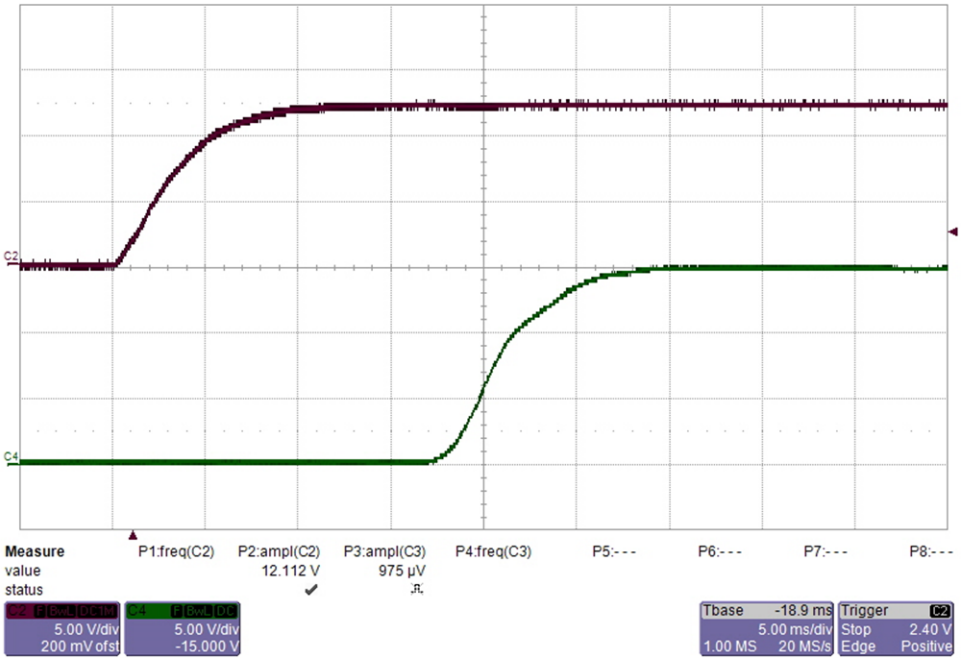
From top to bottom: CH2: input voltage 2 V/div, CH4: output voltage 5 V/div, 5 ms/div

図 94. Start-up Waveform of the –9-V Rail With V_{IN} = 5V and no Load (Bias Supply With Buck and Push Pull)



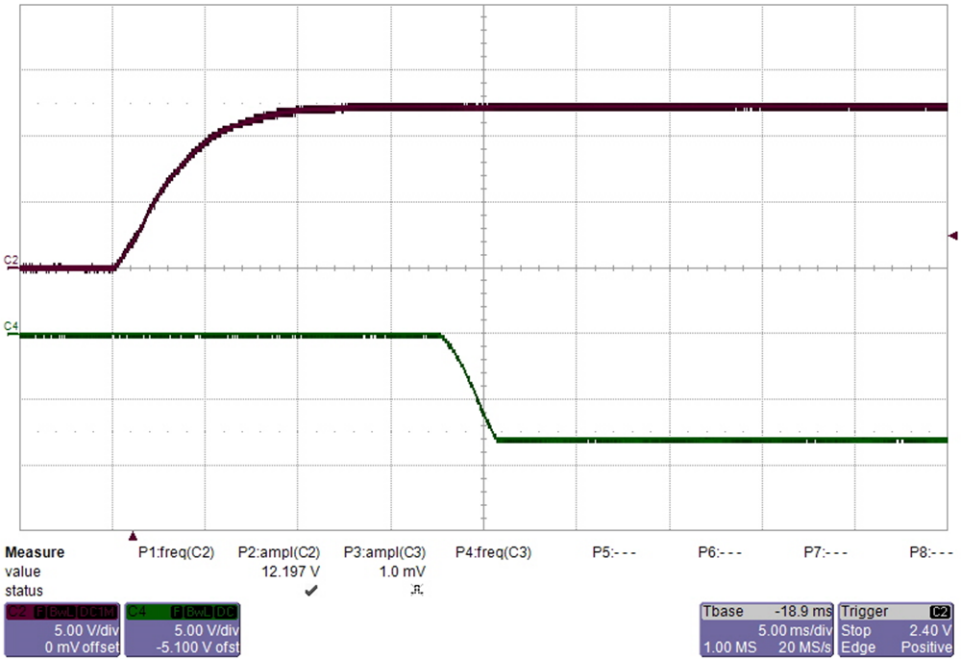
From top to bottom: CH2: input voltage 2 V/div, CH4: output voltage 5 V/div, 5 ms/div

図 95. Start-up Waveform of the 15-V Rail With V_{IN} = 12 V and 180-mA Load (Bias Supply With Buck and Push Pull)



From top to bottom: CH2: input voltage 5 V/div, CH4: output voltage 5 V/div, 5 ms/div

図 96. Start-up Waveform of the –9-V Rail With V_{IN} = 12 V and 180-mA Load (Bias Supply With Buck and Push Pull)

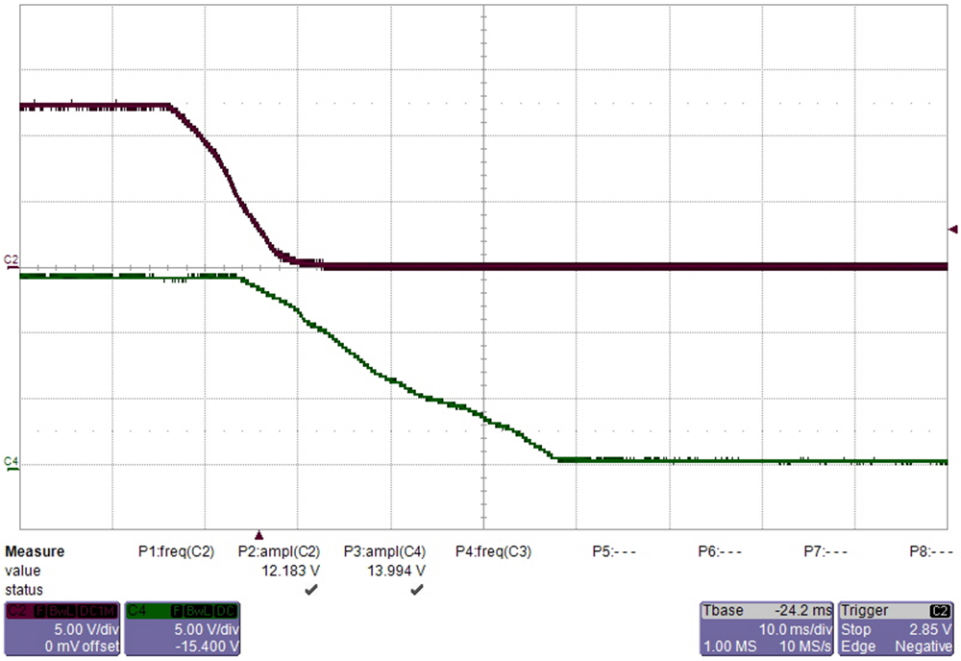


From top to bottom: CH2: input voltage 5 V/div, CH4: output voltage 5 V/div, 5 ms/div

3.2.3.2 Power Down

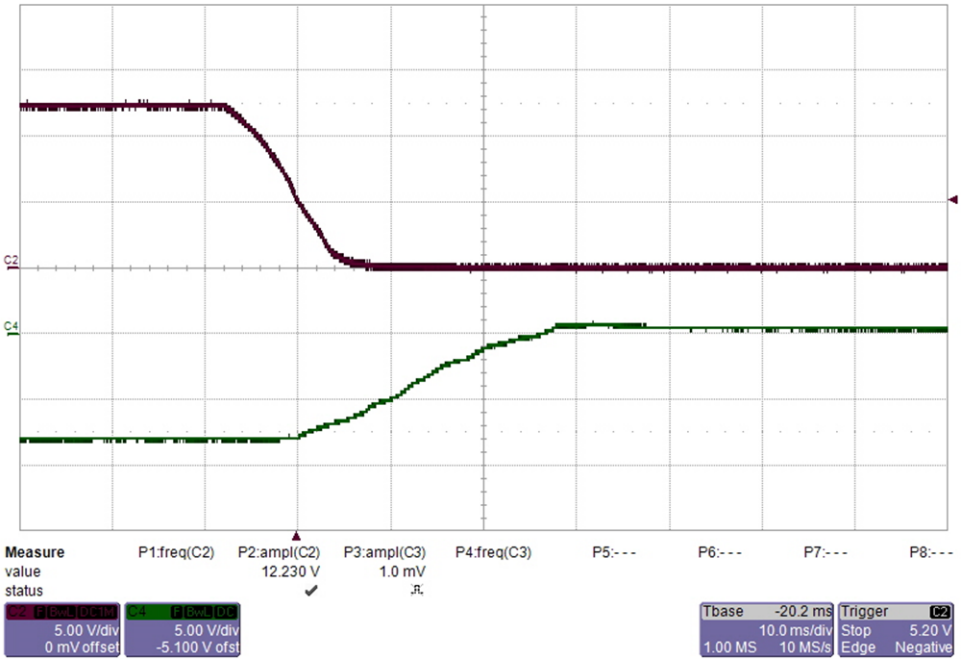
The power down waveforms of the buck with push-pull transformer driver supply are measured under 12-V input. The +15-V and –9-V rails are measured separately.

図 97. Power-Down Waveform of the 15-V Rail With V_{IN} = 12 V and no Load (Bias Supply With Buck and Push Pull)



From top to bottom: CH2: input voltage 5 V/div, CH4: output voltage 5 V/div, 10 ms/div

図 98. Power-Down Waveform of the –9-V Rail With V_{IN} = 12 V and no Load (Bias Supply With Buck and Push Pull)

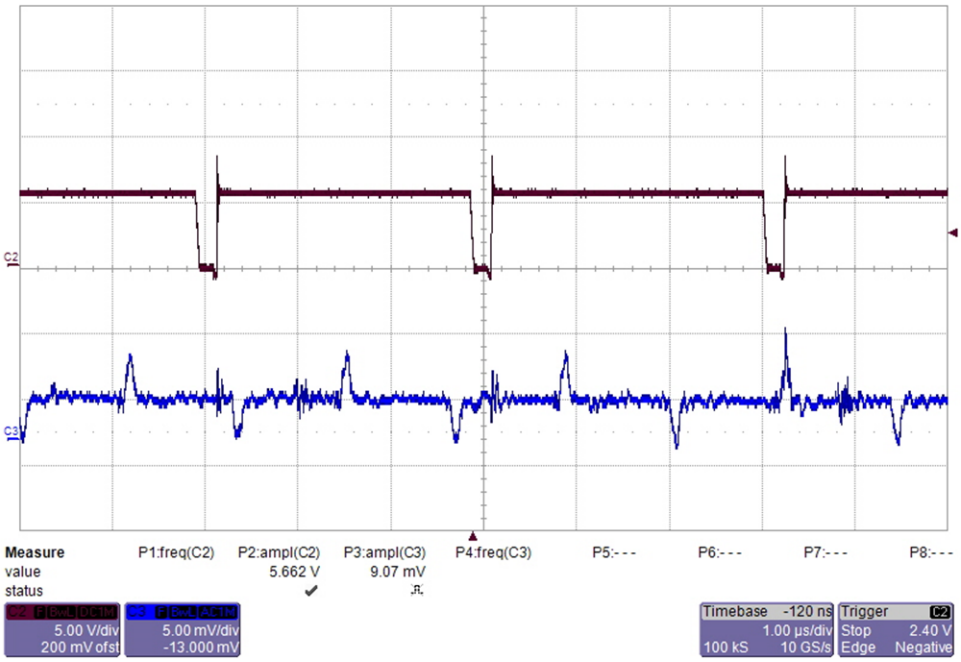


From top to bottom: CH2: input voltage 5 V/div, CH4: output voltage 5 V/div, 10 ms/div

3.2.3.3 Switch Node and Output Voltage Ripple

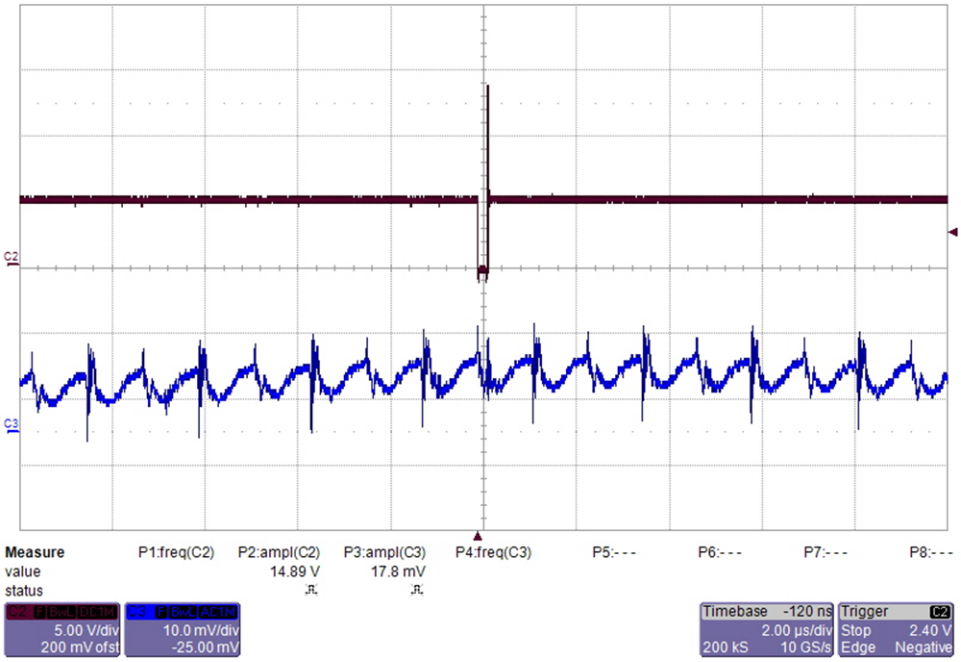
The switch node of the buck converter and output voltage ripple of the push-pull converter are measured under 5-, 12-, and 18-V inputs, respectively. The +15-V and –9-V rails are measured separately.

図 99. Switch Node and Output Ripple of the 15-V Rail With V_{IN} = 5 V and no Load (Bias Supply With Buck and Push Pull)



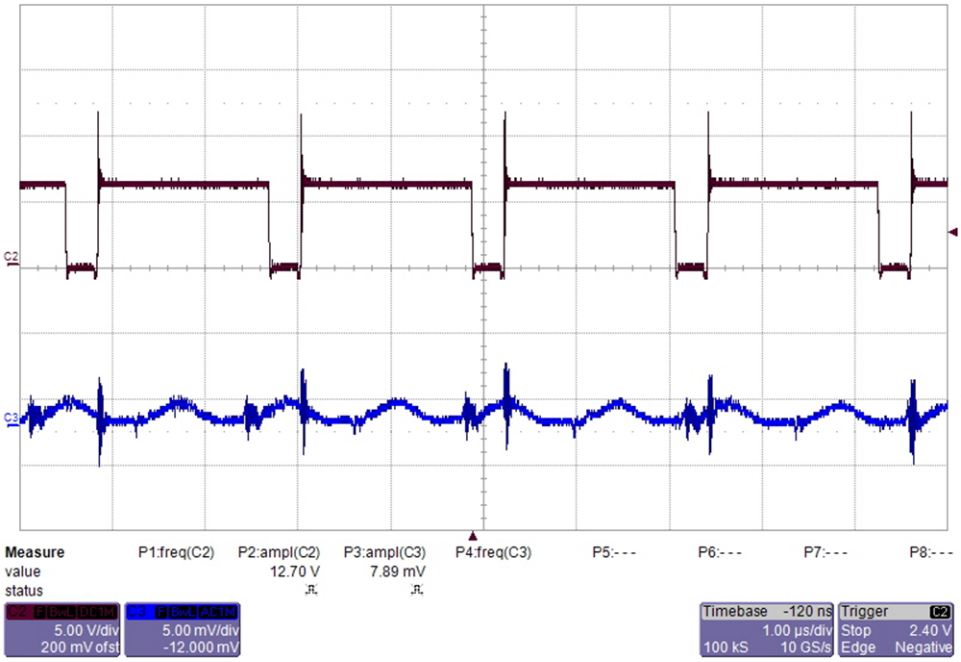
From top to bottom: CH2: switch node 5 V/div, CH3: output voltage ripple 5 mV/div, 1 µs/div

図 100. Switch Node and Output Ripple of the 15-V Rail With V_{IN} = 5 V and 180-mA Load (Bias Supply With Buck and Push Pull)



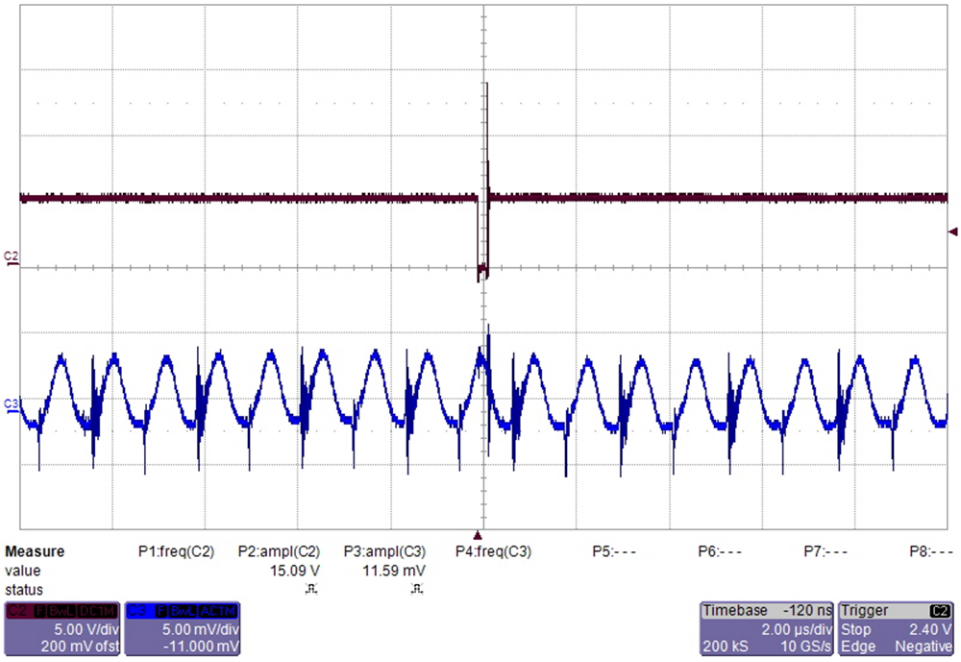
From top to bottom: CH2: switch node 5 V/div, CH3: output voltage ripple 10 mV/div, 2 µs/div

図 101. Switch Node and Output Ripple of the –9-V Rail With V_{IN} = 5 V and no Load (Bias Supply With Buck and Push Pull)



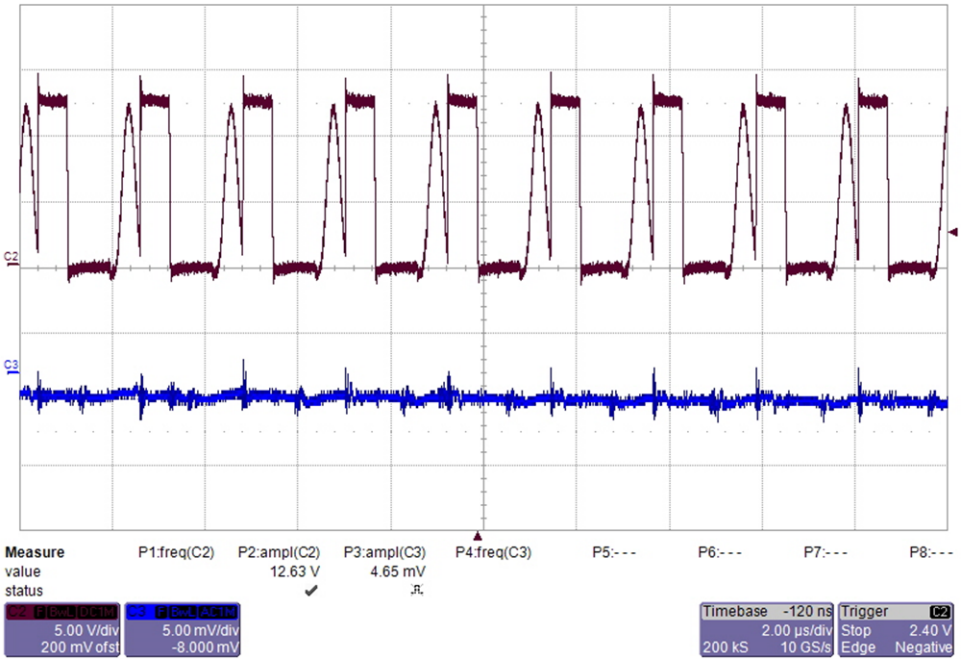
From top to bottom: CH2: switch node 5 V/div, CH3: output voltage ripple 5 mV/div, 1 µs/div

図 102. Switch Node and Output Ripple of the –9-V Rail With V_{IN} = 5 V and 180-mA Load (Bias Supply With Buck and Push Pull)



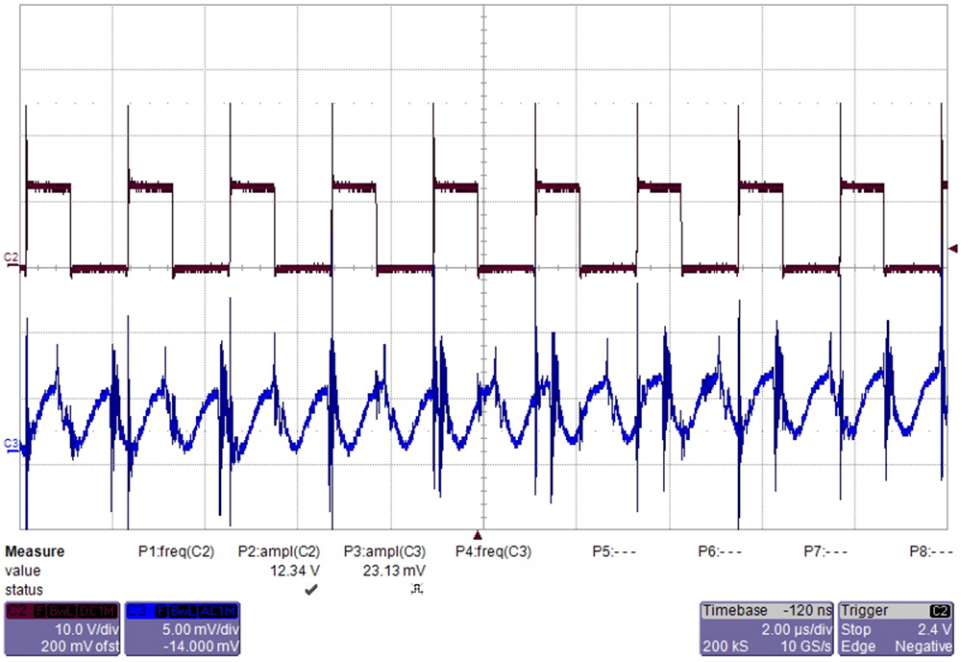
From top to bottom: CH2: switch node 5 V/div, CH3: output voltage ripple 5 mV/div, 2 µs/div

図 103. Switch Node and Output Ripple of the 15-V Rail With V_{IN} = 12 V and no Load (Bias Supply With Buck and Push Pull)



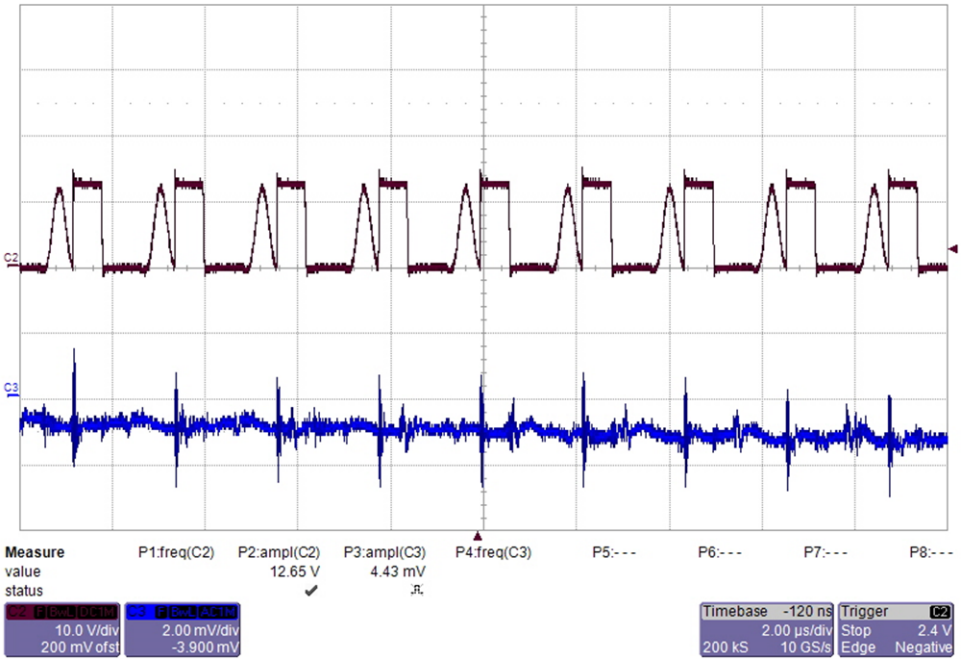
From top to bottom: CH2: switch node 5 V/div, CH3: output voltage ripple 5 mV/div, 2 µs/div

図 104. Switch Node and Output Ripple of the 15-V Rail With V_{IN} = 12 V and 180-mA Load (Bias Supply With Buck and Push Pull)



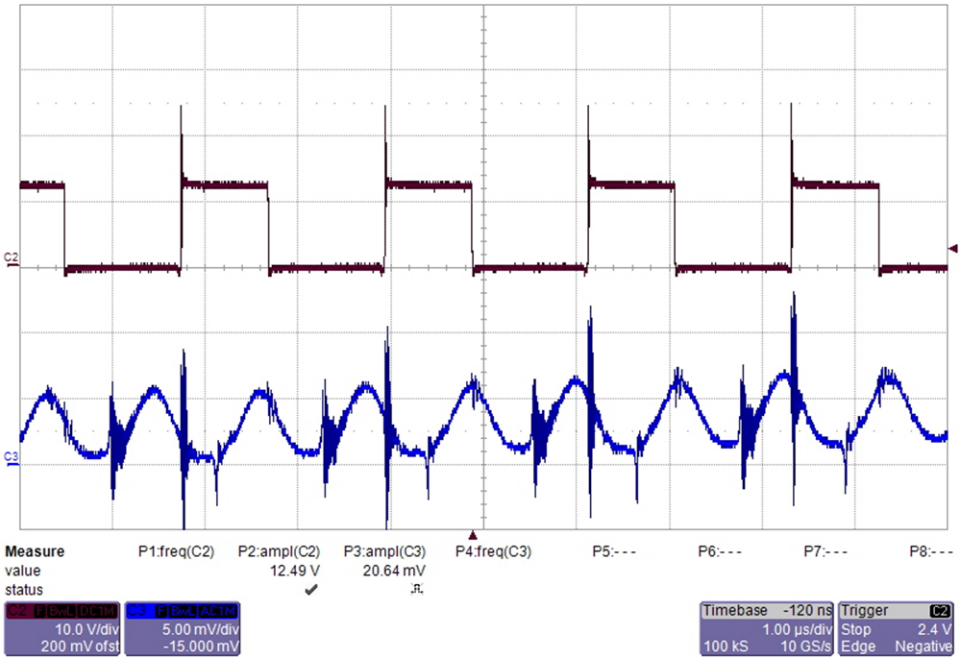
From top to bottom: CH2: switch node 10 V/div, CH3: output voltage ripple 5 mV/div, 2 µs/div

図 105. Switch Node and Output Ripple of the –9-V Rail With V_{IN} = 12 V and no Load (Bias Supply With Buck and Push Pull)



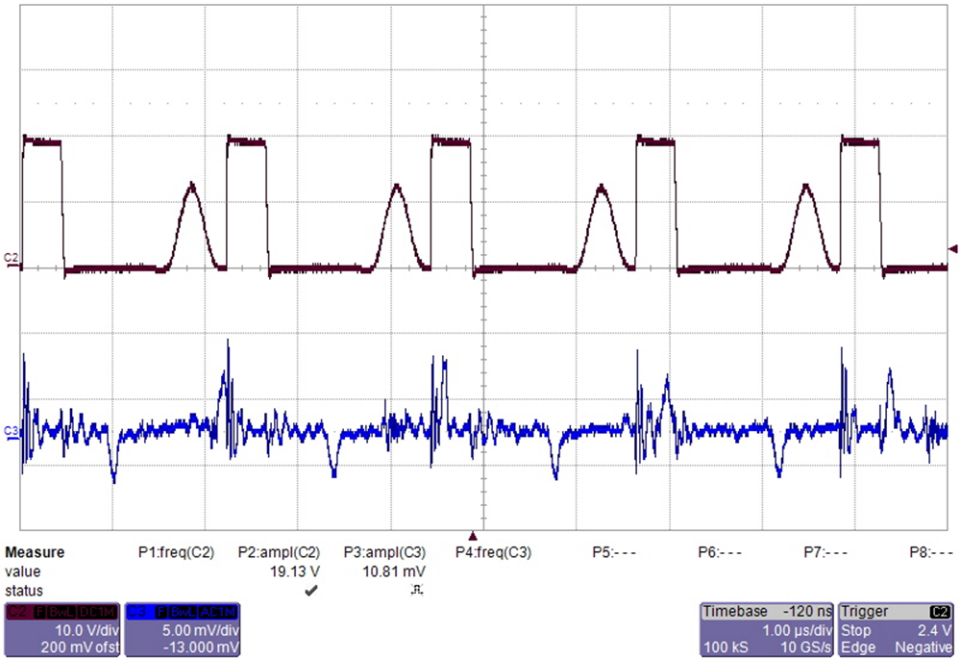
From top to bottom: CH2: switch node 10 V/div, CH3: output voltage ripple 2 mV/div, 2 µs/div

図 106. Switch Node and Output Ripple of the –9-V Rail With V_{IN} = 12 V and 180-mA Load (Bias Supply With Buck and Push Pull)



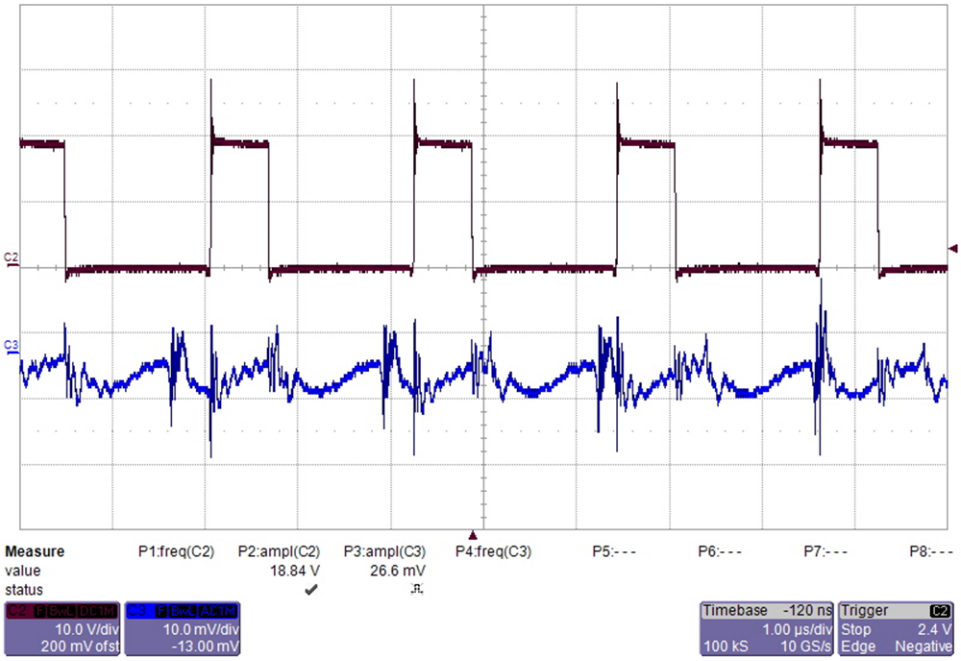
From top to bottom: CH2: switch node 10 V/div, CH3: output voltage ripple 5 mV/div, 1 µs/div

図 107. Switch Node and Output Ripple of the 15-V Rail With V_{IN} = 18 V and no Load (Bias Supply With Buck and Push Pull)



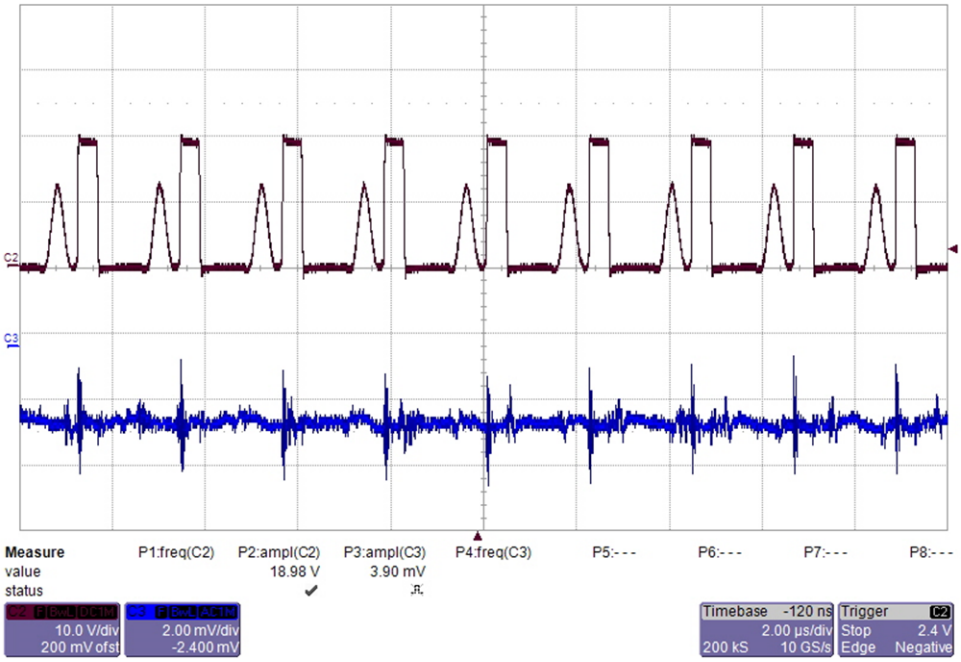
From top to bottom: CH2: switch node 10 V/div, CH3: output voltage ripple 5 mV/div, 1 µs/div

図 108. Switch Node and Output Ripple of the 15-V Rail With V_{IN} = 18 V and 180-mA Load (Bias Supply With Buck and Push Pull)



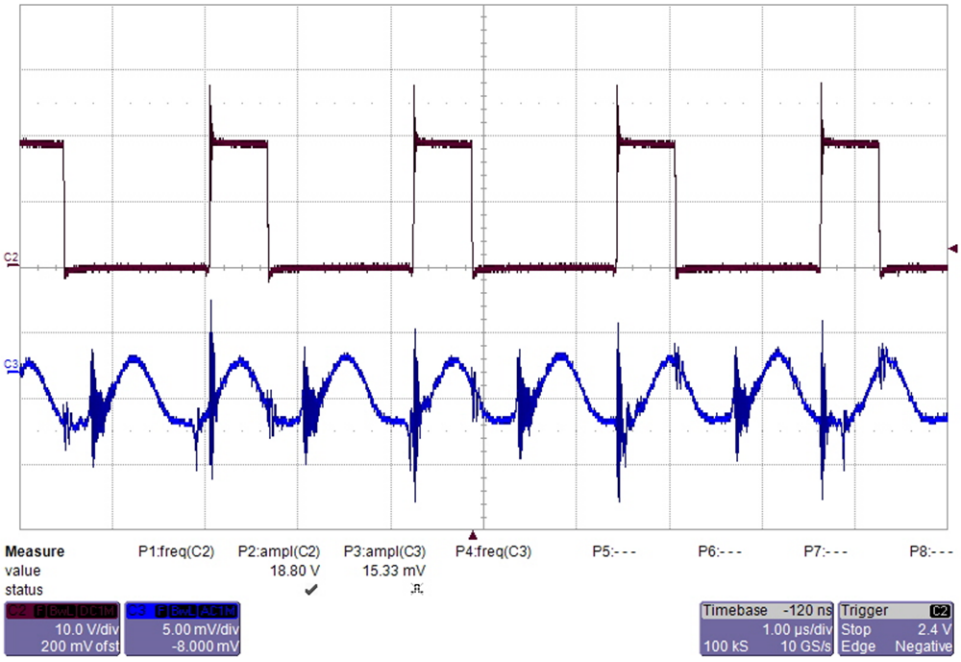
From top to bottom: CH2: switch node 10 V/div, CH3: output voltage ripple 10 mV/div, 1 µs/div

図 109. Switch Node and Output Ripple of the –9-V Rail With V_{IN} = 18 V and no Load (Bias Supply With Buck and Push Pull)



From top to bottom: CH2: switch node 10 V/div, CH3: output voltage ripple 2 mV/div, 2 µs/div

図 110. Switch Node and Output Ripple of the –9-V Rail With V_{IN} = 18 V and 180-mA Load (Bias Supply With Buck and Push Pull)

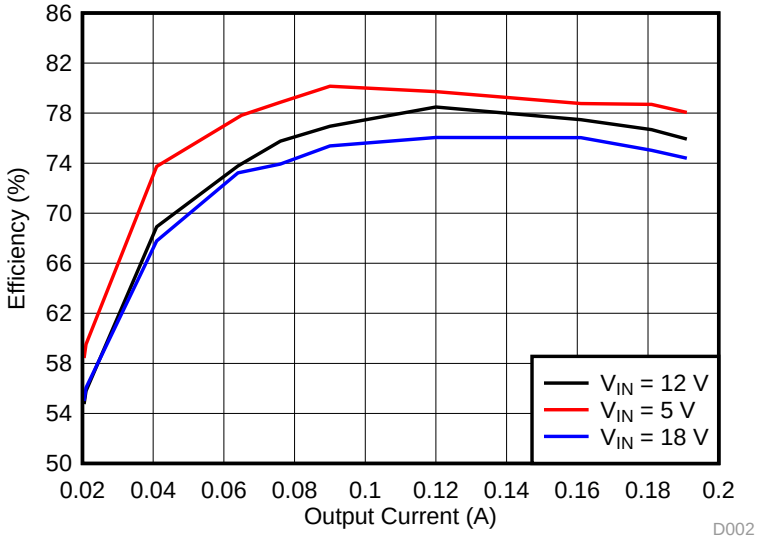


From top to bottom: CH2: switch node 10 V/div, CH3: output voltage ripple 5 mV/div, 1 µs/div

3.2.3.4 Efficiency

図 111 shows the measured efficiency of the buck with push-pull transformer driver supply over the full load range. As can be seen around 80% peak efficiency is achieved with the input voltages of 5 V, 12 V, and 18 V, respectively.

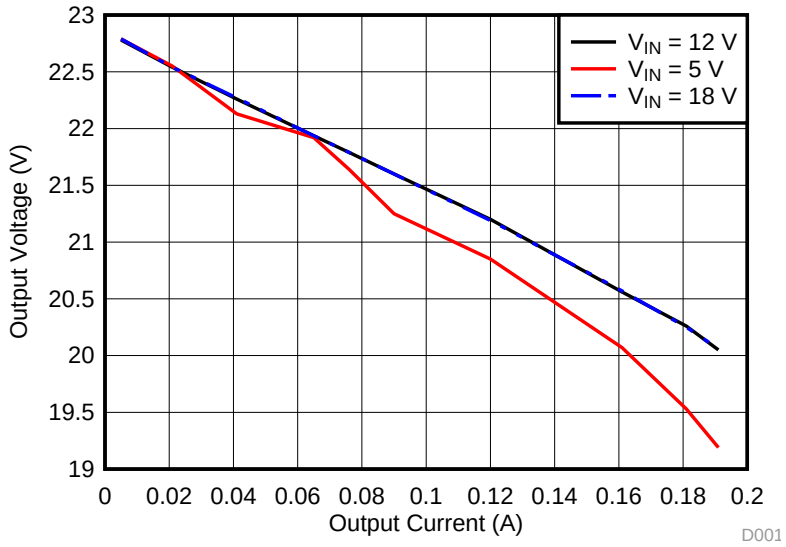
図 111. Measured Efficiency Under Input Voltages of 5 V, 12 V, and 18 V (Bias Supply With Buck and Push Pull)



3.2.3.5 Load Regulation

Load regulation measurements show the % deviation from nominal output voltage as a function of output current. 図 112 shows the measured result of the buck with push-pull transformer driver supply. The load regulation is measured with the input voltages of 5 V, 12 V, and 18 V, respectively.

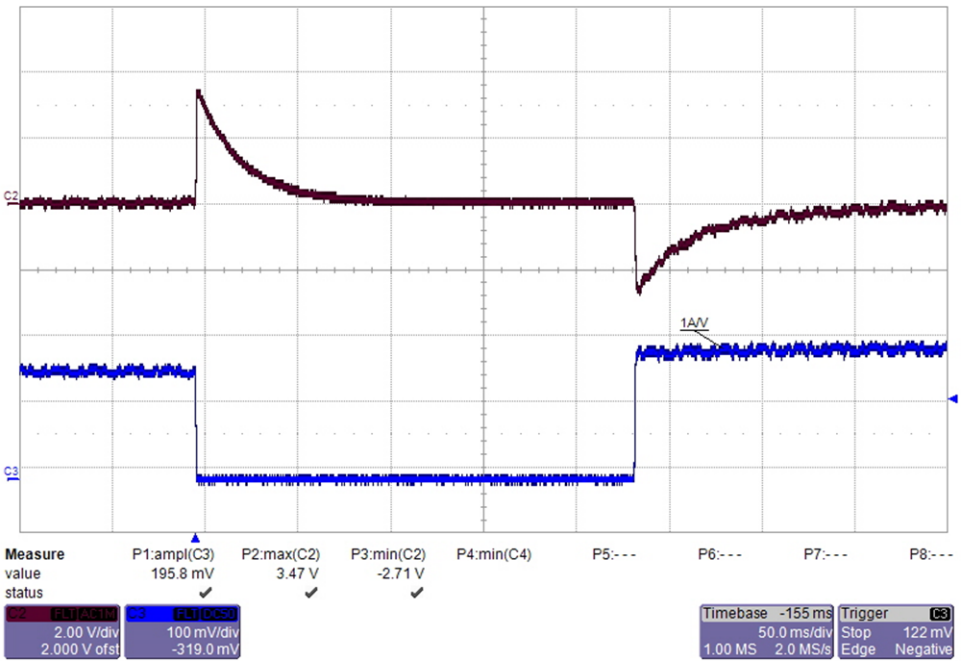
図 112. Load Regulation Under Input Voltages of 5 V, 12 V, and 18 V (Bias Supply With Buck and Push Pull)



3.2.3.6 Load Transients

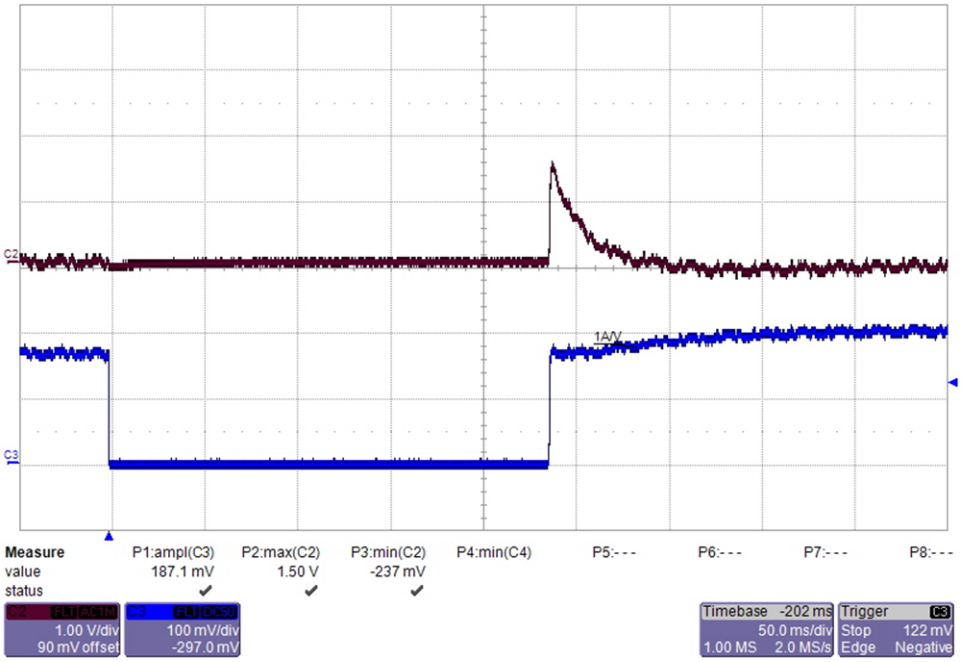
This section shows load transient measurements of the buck with push-pull transformer driver supply. Load transient response presents how well a power supply copes with the changes in the load current demand. During the test, the load is switching from 0 to full under input voltages of 5 V, 12 V, and 18 V, respectively.

図 113. Load Transient Response of the 15-V Rail Under V_{IN} = 5 V and I_{OUT} Switching Between 0 and 180 mA (Bias Supply With Buck and Push Pull)



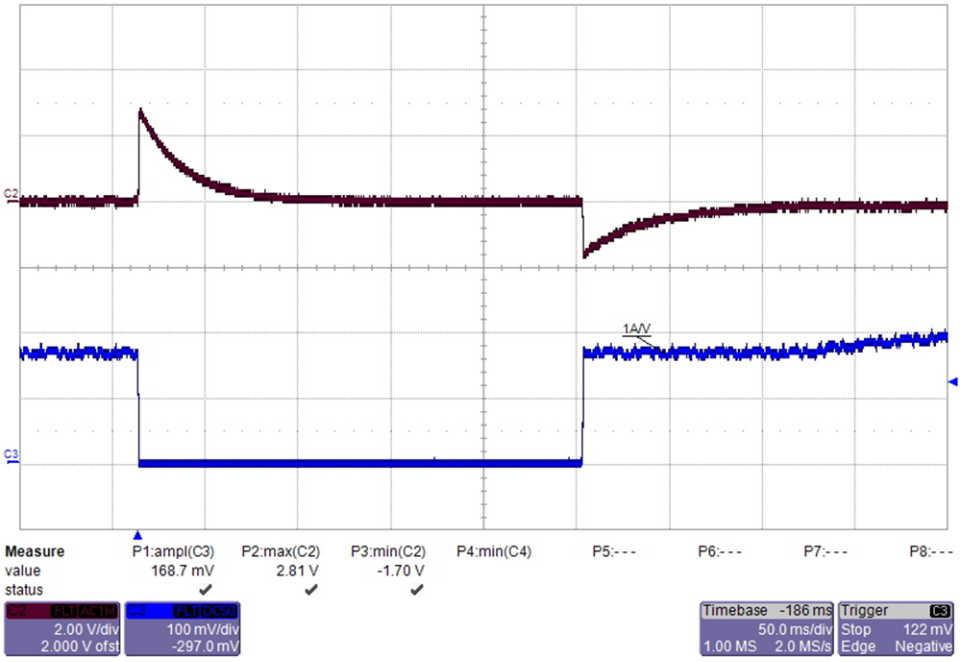
From top to bottom: CH2: output voltage 2 V/div, CH3: load current 1 A/div, 50 ms/div

図 114. Load Transient Response of the –9-V Rail Under V_{IN} = 5 V and I_{OUT} Switching Between 0 and 180 mA (Bias Supply With Buck and Push Pull)



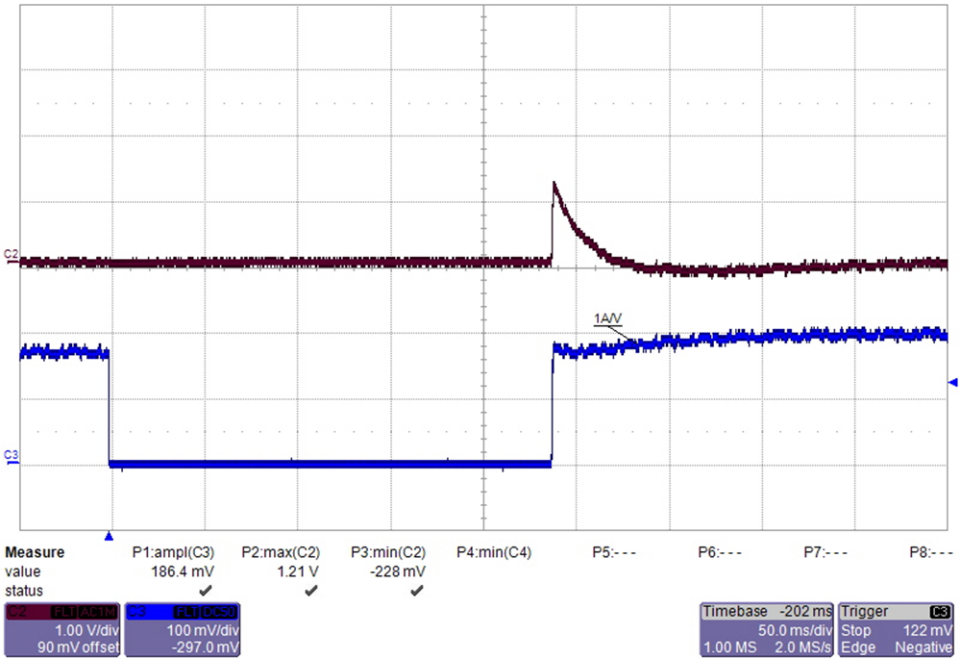
From top to bottom: CH2: output voltage 1 V/div, CH3: load current 1 A/div, 50 ms/div

図 115. Load Transient Response of the 15-V Rail Under V_{IN} = 12 V and I_{OUT} Switching Between 0 and 180 mA (Bias Supply With Buck and Push Pull)



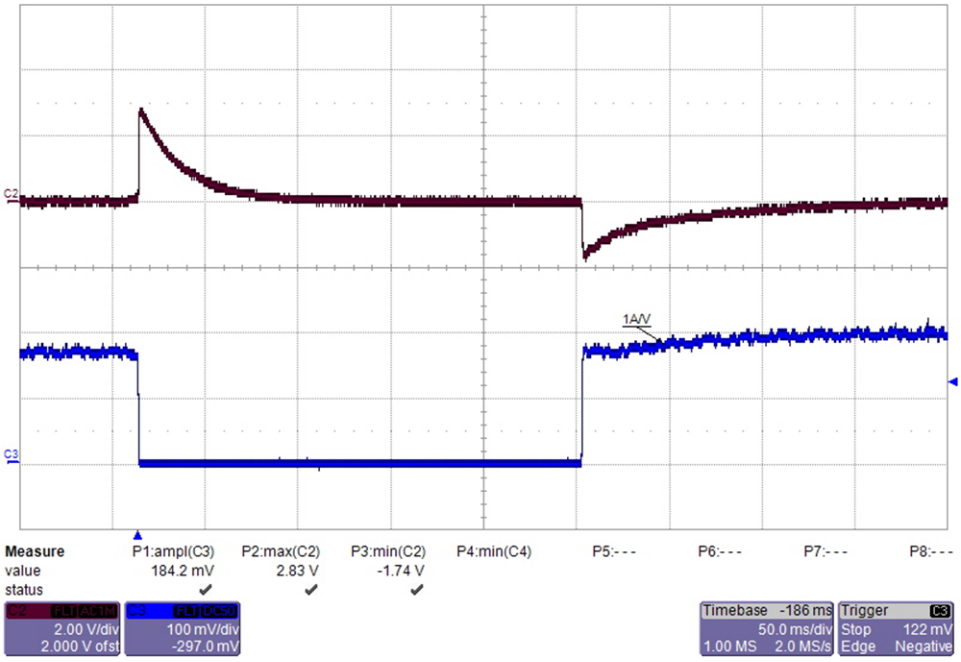
From top to bottom: CH2: output voltage 2 V/div, CH3: load current 1 A/div, 50 ms/div

図 116. Load Transient Response of the –9-V Rail Under V_{IN} = 12 V and I_{OUT} Switching Between 0 and 180 mA (Bias Supply With Buck and Push Pull)



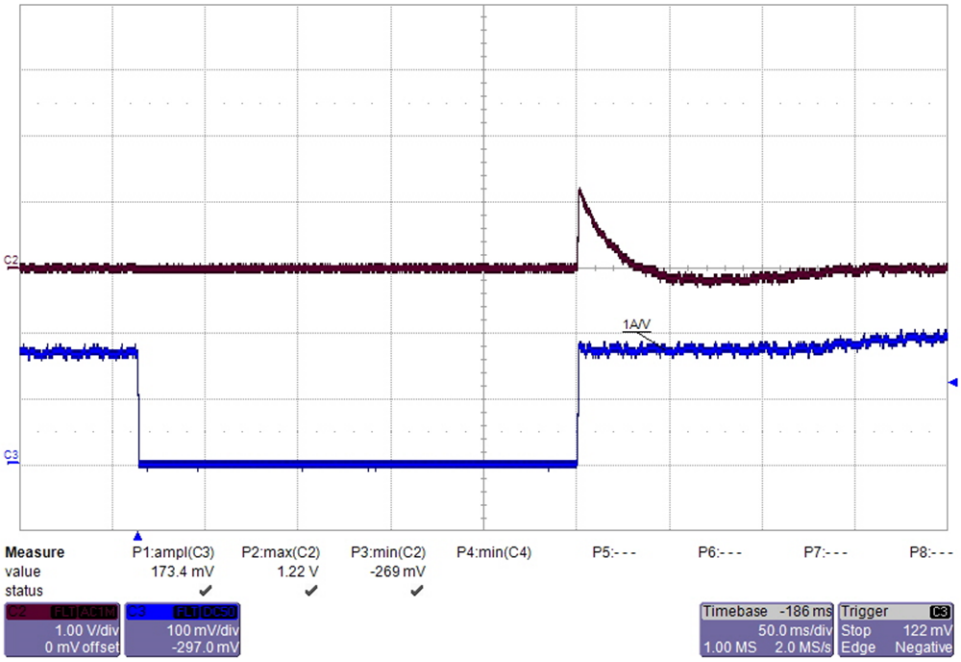
From top to bottom: CH2: output voltage 1 V/div, CH3: load current 1 A/div, 50 ms/div

図 117. Load Transient Response of the 15-V Rail Under V_{IN} = 18 V and I_{OUT} Switching Between 0 and 180 mA (Bias Supply With Buck and Push Pull)



From top to bottom: CH2: output voltage 2 V/div, CH3: load current 1 A/div, 50 ms/div

図 118. Load Transient Response of the –9-V Rail Under V_{IN} = 18 V and I_{OUT} Switching Between 0 and 180 mA (Bias Supply With Buck and Push Pull)

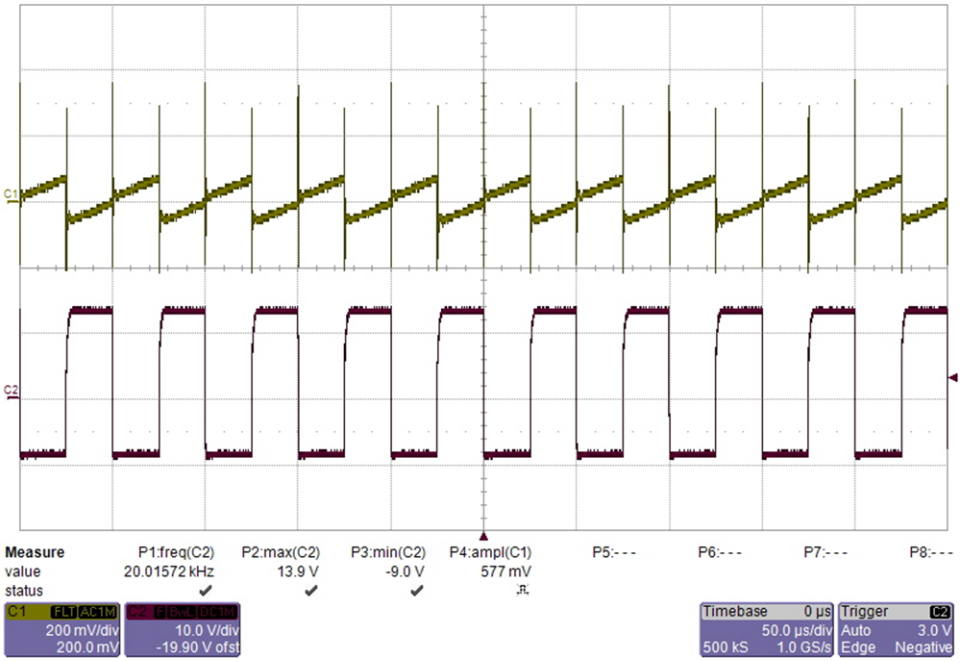


From top to bottom: CH2: output voltage 1 V/div, CH3: load current 1 A/div, 50 ms/div

3.2.3.7 Voltage Ripple While Switching IGBT

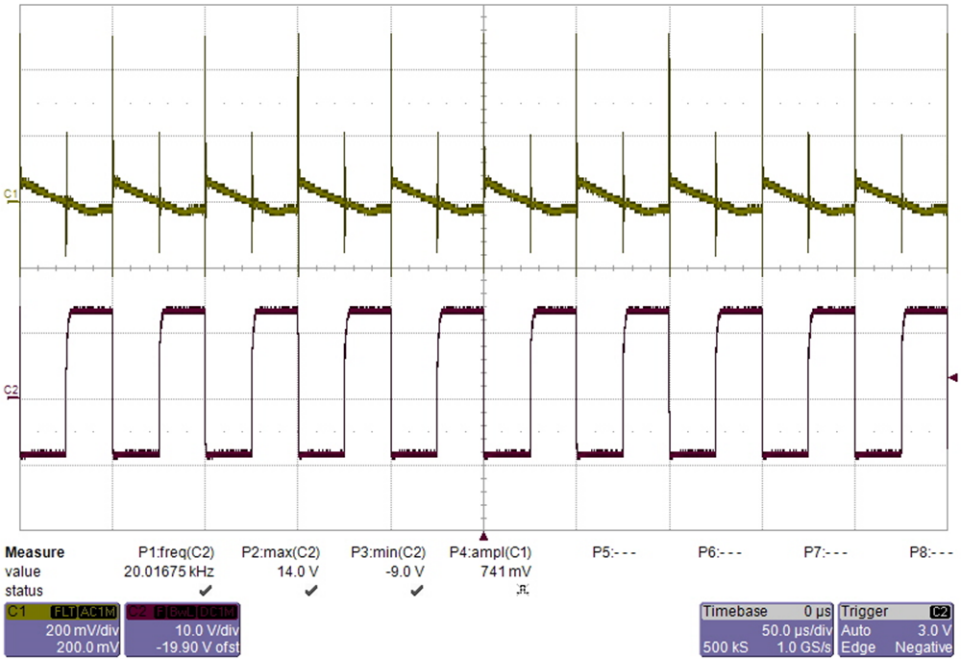
The buck converter with push-pull transformer driver supply is connected to the isolated gate drivers (ISO5852S-Q1) and the 1200-V IGBT module (FF150R12MS4G) for checking the voltage ripple during the switching transients. The IGBTs are switched at 20- and 50-kHz frequencies, respectively.

図 119. Voltage Ripple of the 15-V Rail While Switching the IGBT Module at 20 kHz (Bias Supply With Buck and Push Pull)



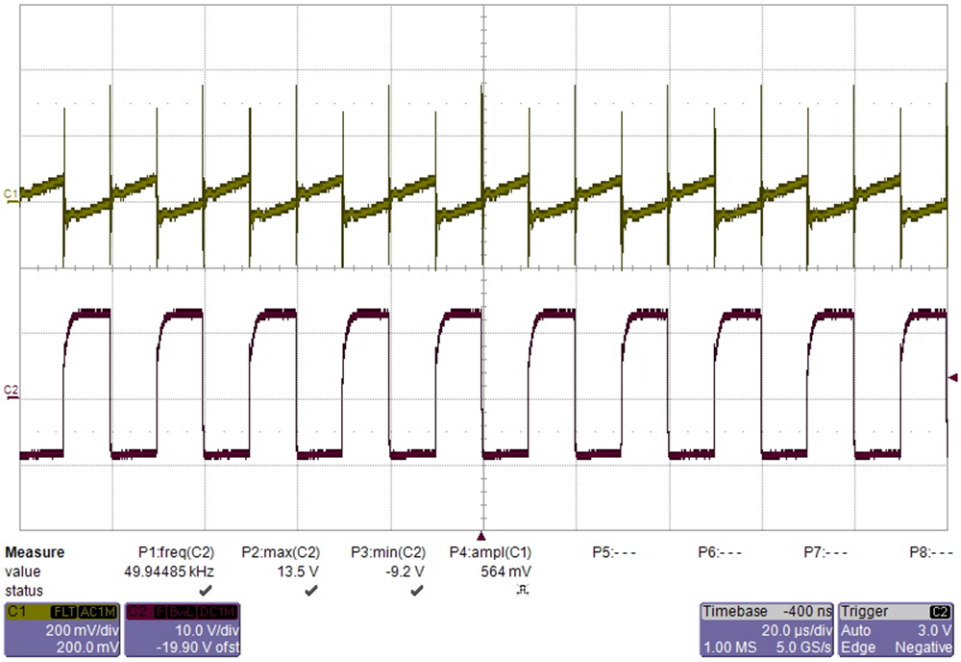
From top to bottom: CH1: output voltage 200 mV/div, CH2: Gate PWM signal 10 V/div, 50 µs/div

図 120. Voltage Ripple of the –9-V Rail While Switching the IGBT Module at 20 kHz (Bias Supply With Buck and Push Pull)



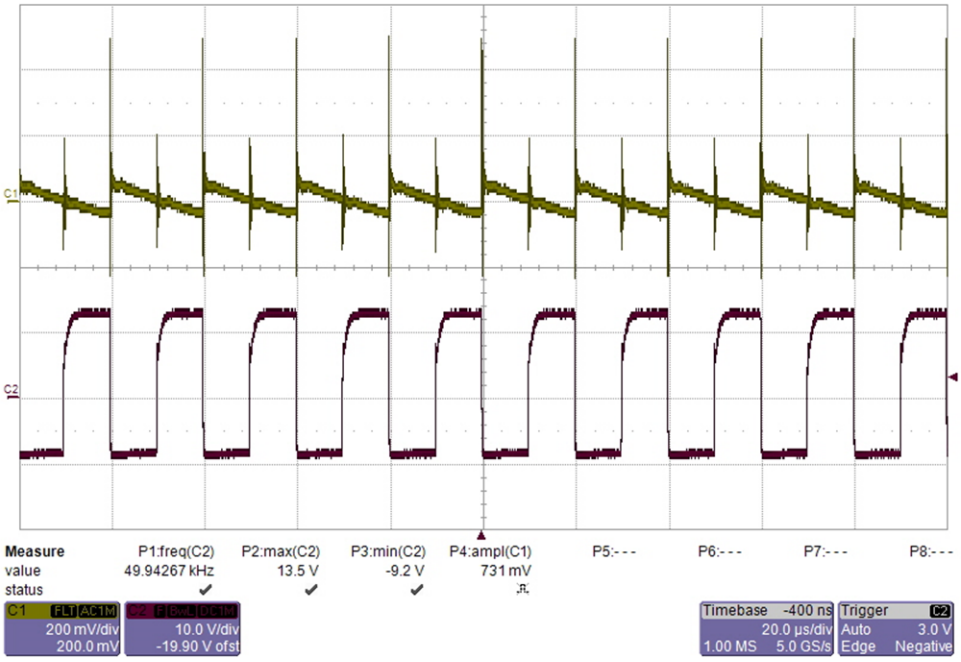
From top to bottom: CH1: output voltage 200 mV/div, CH2: Gate PWM signal 10 V/div, 50 µs/div

図 121. Voltage Ripple of the 15-V Rail While Switching the IGBT Module at 50 kHz (Bias Supply With Buck and Push Pull)



From top to bottom: CH1: output voltage 200 mV/div, CH2: Gate PWM signal 10 V/div, 20 µs/div

図 122. Voltage Ripple of the –9-V Rail While Switching the IGBT Module at 50 kHz (Bias Supply With Buck and Push Pull)

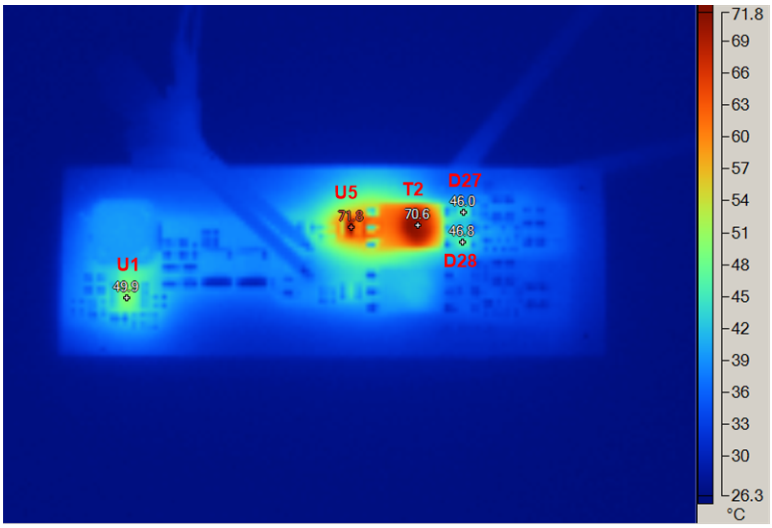


From top to bottom: CH1: output voltage 200 mV/div, CH2: Gate PWM signal 10 V/div, 20 µs/div

3.2.3.8 Thermal Image

The thermal of the buck converter with a push-pull transformer driver supply is measured under the full-load conditions. The circuit runs at the room temperature for 30 minutes. A 12-V nominal voltage is applied. The converter is loaded with 180 mA. 図 123 shows the thermal image of the board.

図 123. Thermal Image With V_{IN} = 12 V and I_{OUT} = 180 mA (Bias Supply With Buck and Push Pull)



U1: LM46002-Q1, T2: push-pull converter transformer, U5: SN6505-Q1, D27 and D28: secondary rectification diode of the push-pull converter

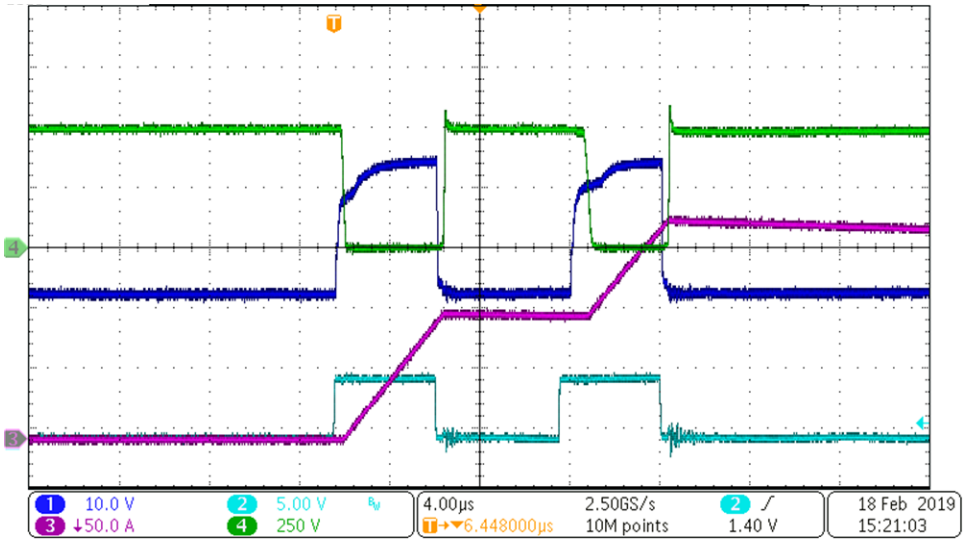
3.2.4 High-Voltage Testing With the IGBT Power Stage

3.2.4.1 Double Pulse Test

The double pulse test is performed under high voltage to evaluate the switching parameters of the IGBT and the performance of the gate driver. The test is considered as one periodical snapshot of the system, and it is done with a purely inductive load. The driver parameters of switching speed, thermal, and oscillation or no oscillation can be observed.

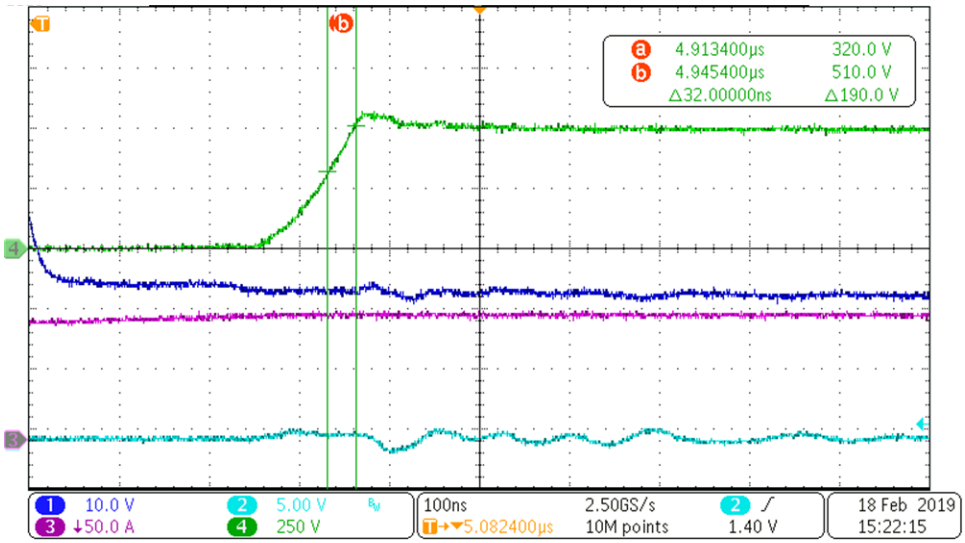
A 500-V voltage is applied on the DC bus. The pulse train consists of two pulses with a repetition frequency of about 100 kHz. The widths of two pulses are both 4.5 µs. The delay is set to be 5.5 µs for the voltage and currents to settle out. The rise and fall time of the pulses are set as 5 ns.

図 124. Double Pulse Test on the Power Stage



From top to bottom: CH4: IGBT Vds voltage 250 V/div, CH1: IGBT gate signal, 10 V/div, CH2: PWM signal at ISO5852s-Q1 input, 5 V/div, CH3: Inductor current, 50 A/div, 4 µs/div

図 125. Generated dv/dt at the IGBT Vds Voltage Turn-off Transient (6 V/ns)



CH4: IGBT Vds voltage 250 V/div, 100 ns/div

3.2.4.2 CMTI Test

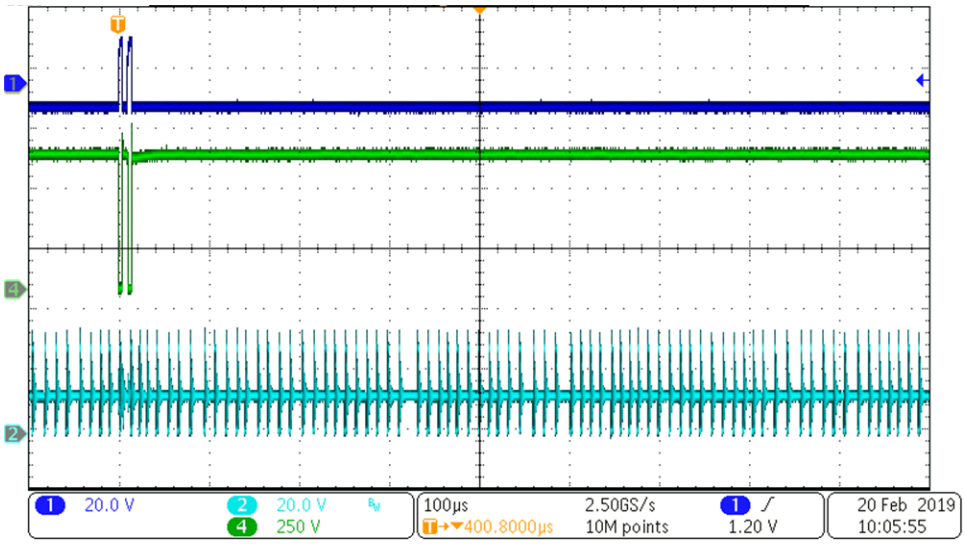
This reference design is connected to a high-voltage DC bus for high-voltage dv/dt immunity test. Common-mode transient immunity (CMTI) is a maximum tolerable rate of rise or fall of the common-mode voltage applied between two isolated circuits. The unit is normally in kV/us or V/ns. High CMTI means that the two isolated circuits, both transmitter side and receiver side, function well when striking the insulation barrier with very high rise (positive) slew rate, or high fall (negative) slew rate. For CMTI testing, the peak common-mode voltage should not exceed the allowed maximum repetitive working voltage between the two isolated circuits.

For CMTI testing, 570-V DC bus voltage is applied on the DC bus (limited by the DC link capacitor). 20-µH air core inductor is connected between DC bus+ and IGBT half bridge neutral to by pass the high side IGBT. The DC bus– terminal is connected to the low-voltage ground at the bias supply primary side. The low-side IGBT is pulsed twice. Hence, a pulsed high voltage is imposed between the primary and secondary grounds of the high-side bias supply. The switch node of the high-side bias supply is measured.

3.2.4.2.1 LM5180-Q1 Flyback Converter

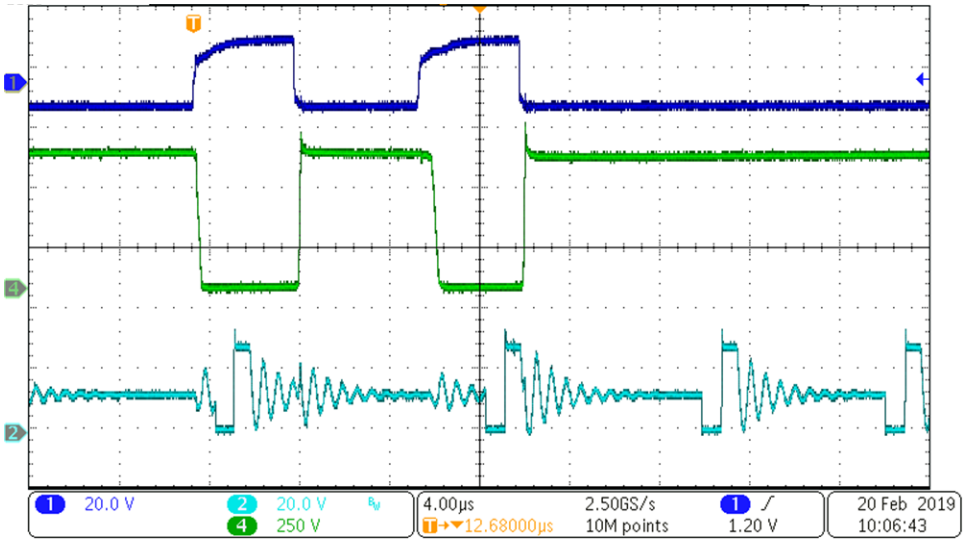
This section shows the CMTI test with LM5180-Q1 based supply. The bias supply is connected to the power stage. The IGBT is switched with 570-V DC bus voltage and at 10.8 V/ns speed of dv/dt. 図 126 through 図 128 illustrate that the supply operates smoothly without interruption.

図 126. CMTI Test on the Bias Supply Solution 1 (Bias Supply With LM5180-Q1)



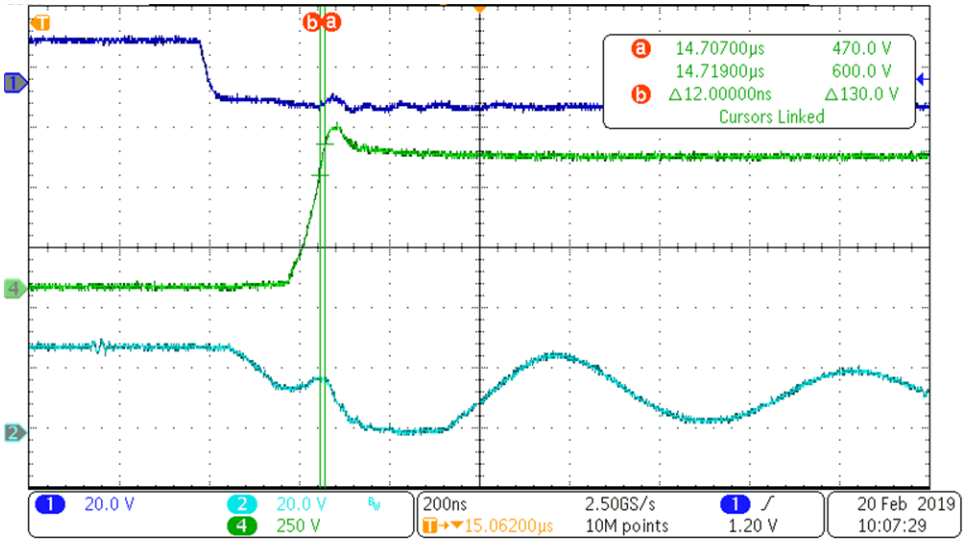
From top to bottom: CH1: IGBT gate signal, 20 V/div, CH4: IGBT Vds voltage, 250 V/div, CH2: LM5180-Q1 switch node voltage, 20 V/div, 100 µs/div

図 127. CMTI Test Waveform Zoom in (Bias Supply With LM5180-Q1)



From top to bottom: CH1: IGBT gate signal, 20 V/div, CH4: IGBT Vds voltage, 250 V/div, CH2: LM5180-Q1 switch node voltage, 20 V/div, 4 µs/div

図 128. dv/dt Transient of the CMTI -- 10.8 V/ns (Bias Supply With LM5180-Q1)

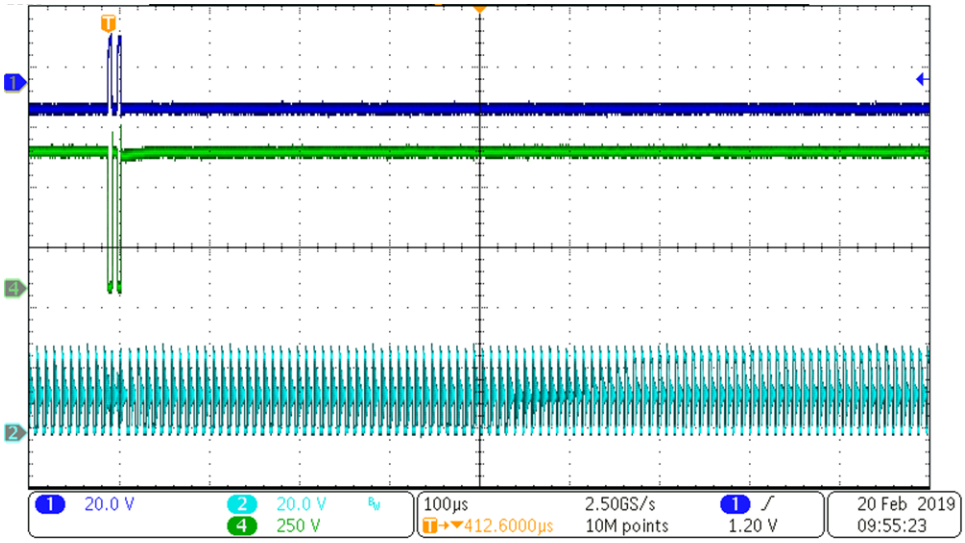


From top to bottom: CH1: IGBT gate signal, 20 V/div, CH4: IGBT Vds voltage, 250 V/div, CH2: LM5180-Q1 switch node voltage, 20 V/div, 200 ns/div

3.2.4.2.2 TPS40210-Q1 Flyback Converter

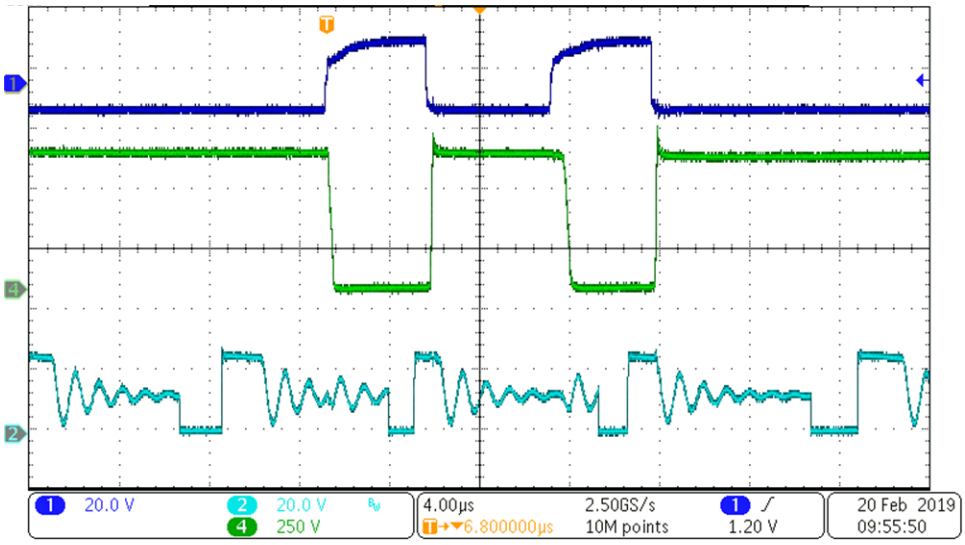
This section shows the CMTI test with TPS40210-Q1 based supply. The bias supply is connected to the power stage. The IGBT is switched with 570 V DC bus voltage and at 9.16 V/ns speed of dv/dt. 図 129 through 図 131 show that the supply operates smoothly without interruption.

図 129. CMTI Test on the Bias Supply Solution 2 (Bias Supply With TPS40210-Q1)



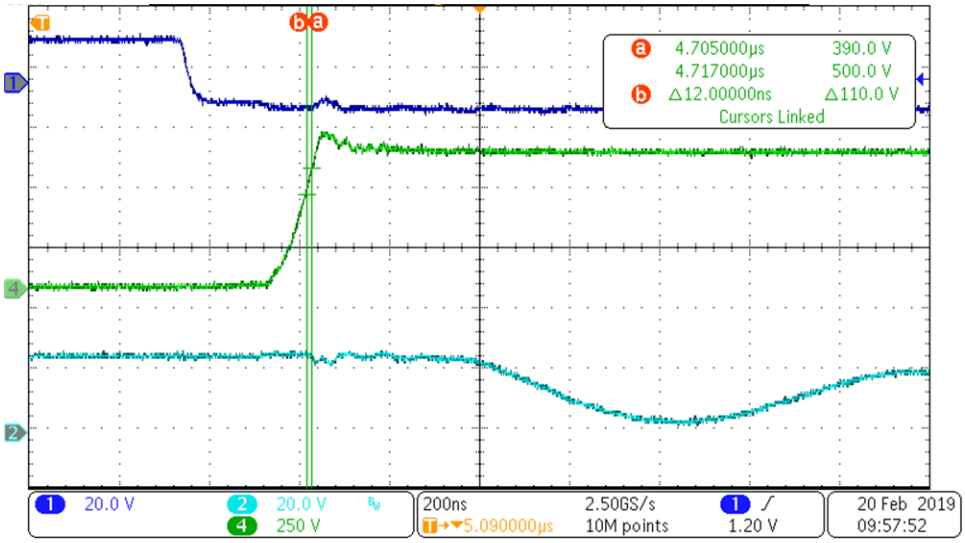
From top to bottom: CH1: IGBT gate signal, 20 V/div, CH4: IGBT Vds voltage, 250 V/div, CH2: TPS40210-Q1 switch node voltage, 20 V/div, 100 µs/div

図 130. CMTI Test Waveform Zoomed in (Bias Supply With TPS40210-Q1)



From top to bottom: CH1: IGBT gate signal, 20 V/div, CH4: IGBT Vds voltage, 250 V/div, CH2: TPS40210-Q1 switch node voltage, 20 V/div, 4 µs/div

図 131. dv/dt Transient of the CMTI -- 9.16 V/ns (Bias Supply With TPS40210-Q1)

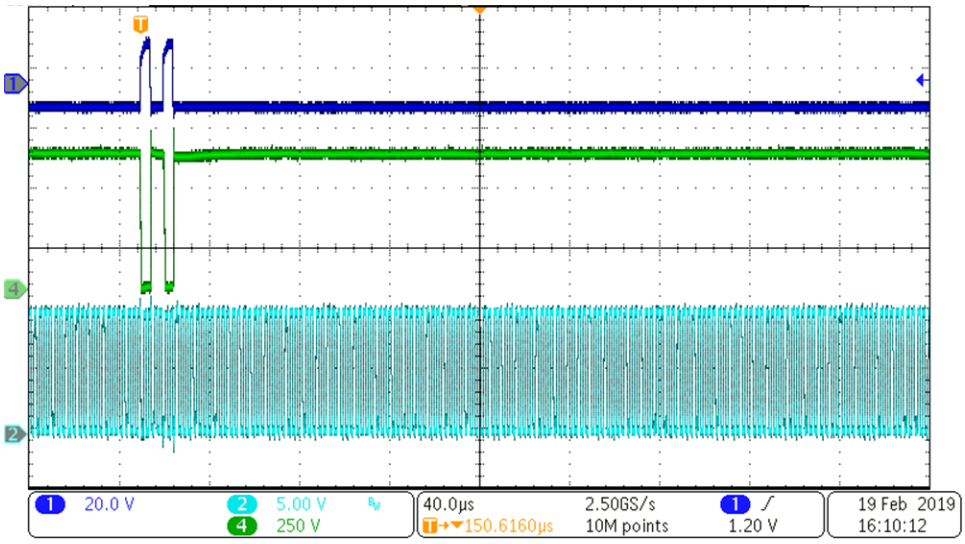


From top to bottom: CH1: IGBT gate signal, 20 V/div, CH4: IGBT Vds voltage, 250 V/div, CH2: TPS40210-Q1 switch node voltage, 20 V/div, 200 ns/div

3.2.4.2.3 SN6505-Q1 Push-Pull Converter

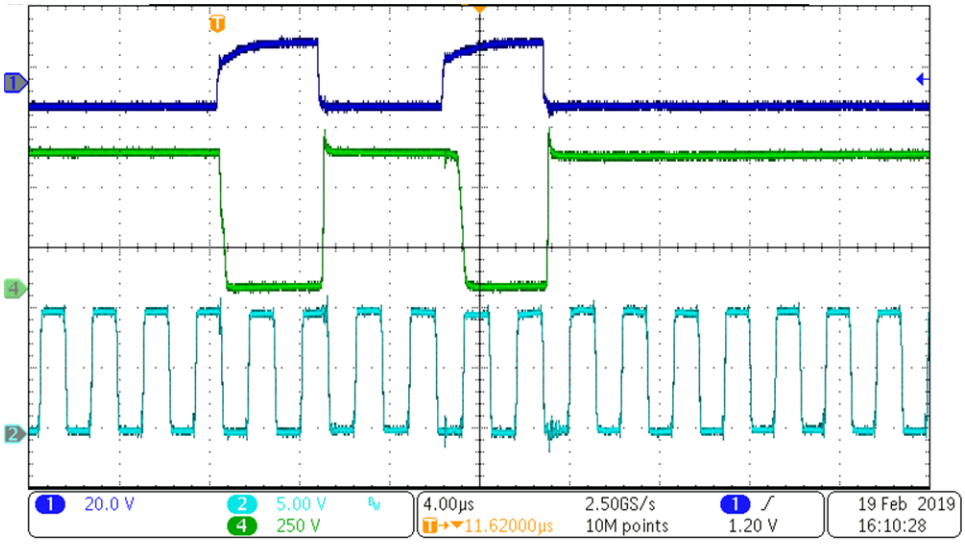
This section shows the CMTI test with SN6505-Q1-based supply. The bias supply is connected to the power stage. The IGBT is switched with 570 V DC bus voltage and at 10.26 V/ns speed of dv/dt. 図 132 through 図 134 illustrate that the supply operates smoothly without interruption.

図 132. CMTI Test on the Bias Supply Solution 3 (Bias Supply With Buck and Push Pull)



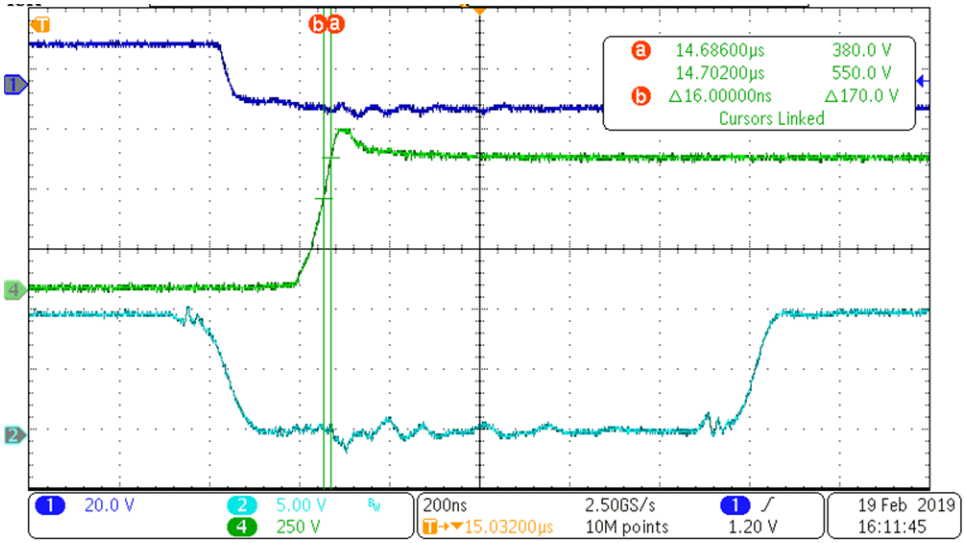
From top to bottom: CH1: IGBT gate signal, 20 V/div, CH4: IGBT Vds voltage, 250 V/div, CH2: SN6505-Q1 switch node voltage, 5 V/div, 40 µs/div

図 133. CMTI Test Waveform Zoomed in (Bias Supply With Buck and Push Pull)



From top to bottom: CH1: IGBT gate signal, 20 V/div, CH4: IGBT Vds voltage, 250 V/div, CH2: SN6505-Q1 switch node voltage, 5 V/div, 4 µs/div

図 134. dv/dt Transient of the CMTI -- 10.26 V/ns (Bias Supply With Buck and Push Pull)



From top to bottom: CH1: IGBT gate signal, 20 V/div, CH4: IGBT Vds voltage, 250 V/div, CH2: SN6505-Q1 switch node voltage, 5 V/div, 200 ns/div

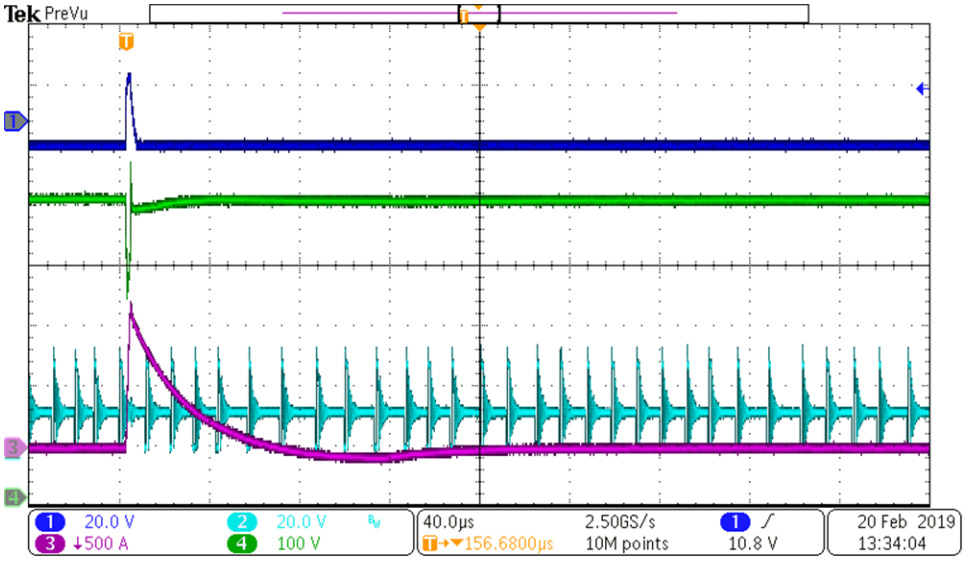
3.2.4.3 Short-Circuit Test

The IGBT module is turned on into short to measure the performance of power stage and the immunity of bias supplies to the high di/dt. The high side IGBT is shorted with low impedance cable. A 500-V DC bus voltage is applied. The low-side IGBT is pulsed once and turned on into short. Switch node of the high side bias supplies are measured.

3.2.4.3.1 LM5180-Q1 Flyback Converter

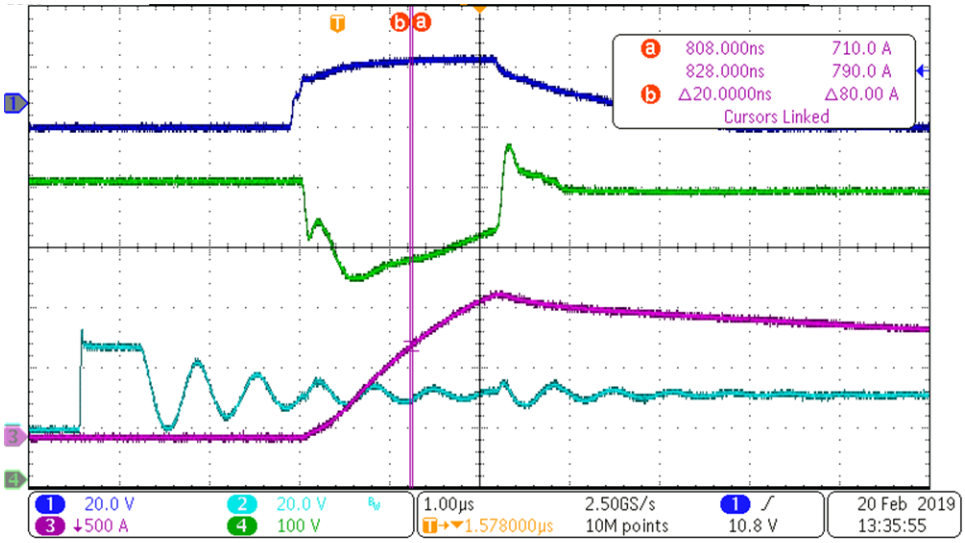
This section shows the short-circuit test with LM5180-Q1 based supply. The IGBT is switched with 500-V DC bus voltage and at 4 A/ns speed of di/dt. As can been the supply operates smoothly without interruption.

図 135. Short-Circuit Test Waveforms (Bias Supply With LM5180-Q1 Flyback)



From top to bottom: CH1: IGBT gate signal, 20 V/div, CH4: IGBT Vds voltage, 100 V/div, CH2: LM5180-Q1 switch node voltage, 20/div, CH3: Load current flowing from drain to source of the IGBT, 500 A/div, 40 µs/div

図 136. di/dt Transient During Short Circuit (Bias Supply With LM5180-Q1 Flyback)

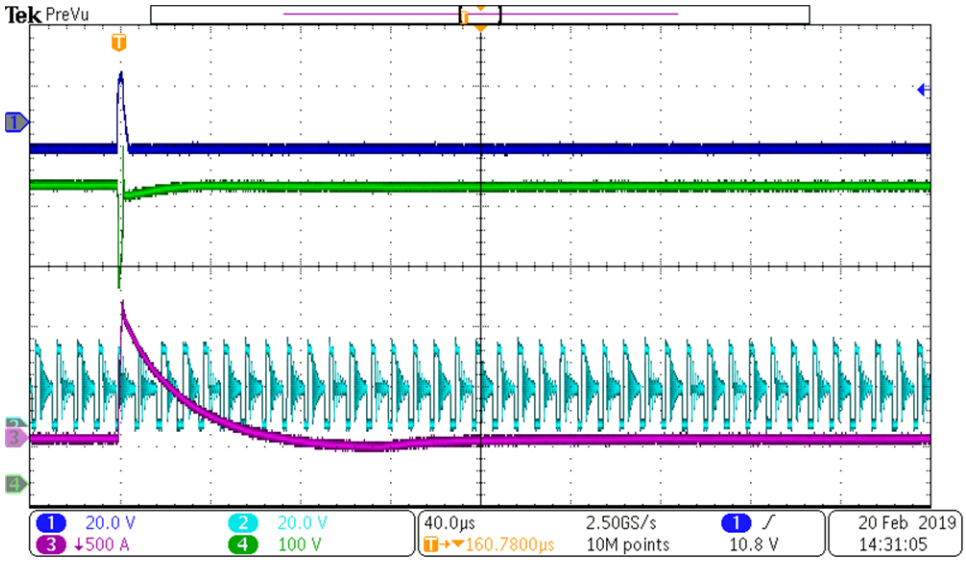


From top to bottom: CH1: IGBT gate signal, 20 V/div, CH4: IGBT Vds voltage, 100 V/div, CH2: LM5180-Q1 switch node voltage, 20/div, CH3: Load current flowing from drain to source of the IGBT, 500 A/div, 1 µs/div

3.2.4.3.2 TPS40210-Q1 Flyback Converter

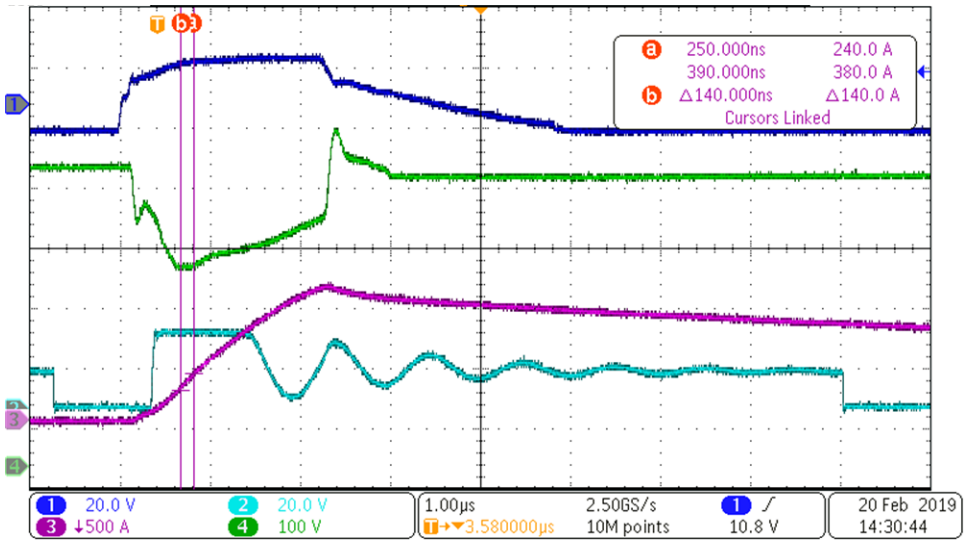
This section shows the short-circuit test with TPS40210-Q1 based supply. The bias supply is connected to the power stage. The IGBT is switched with 500 V DC bus voltage and at 1 A/ns speed of di/dt. 図 137 and 図 138 illustrate that the supply operates smoothly without interruption.

図 137. Short-Circuit Test Waveforms (Bias Supply With TPS40210-Q1 Flyback)



From top to bottom: CH1: IGBT gate signal, 20 V/div, CH4: IGBT Vds voltage, 100 V/div, CH2: LM5180-Q1 switch node voltage, 20/div, CH3: Load current flowing from drain to source of the IGBT, 500 A/div, 40 µs/div

図 138. di/dt Transient During Short-Circuit (Bias Supply With TPS40210-Q1 Flyback)

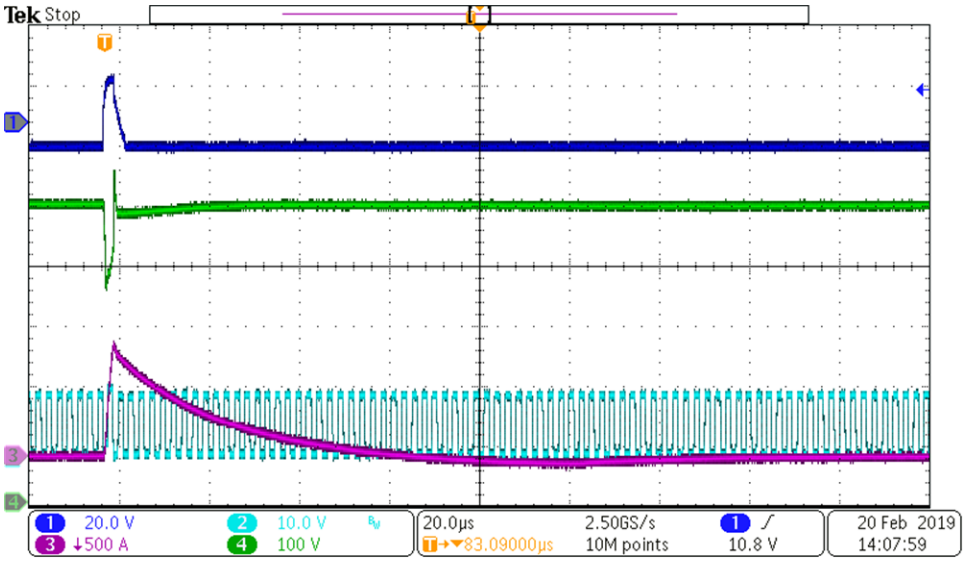


From top to bottom: CH1: IGBT gate signal, 20 V/div, CH4: IGBT Vds voltage, 100 V/div, CH2: TPS40210-Q1 switch node voltage, 20/div, CH3: Load current flowing from drain to source of the IGBT, 500 A/div, 1 µs/div

3.2.4.3.3 SN6505-Q1 Push-Pull Converter

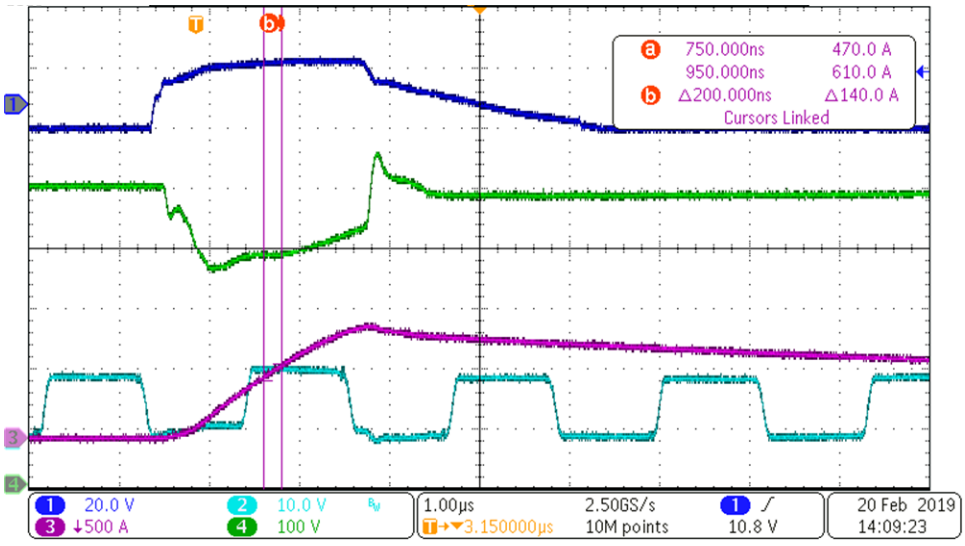
This section shows the short-circuit test with SN6505-Q1-based supply. The bias supply is connected to the power stage. The IGBT is switched with 500-V DC bus voltage and at 0.7 A/ns speed of di/dt. The waveforms in 図 139 and 図 140 illustrate that the supply operates smoothly without interruption.

図 139. Short-Circuit Test Waveforms (Bias Supply With Buck and Push Pull)



From top to bottom: CH1: IGBT gate signal, 20 V/div, CH4: IGBT Vds voltage, 100 V/div, CH2: SN6505-Q1 switch node voltage, 20/div, CH3: Load current flowing from drain to source of the IGBT, 500 A/div, 20 µs/div

図 140. di/dt Transient During Short Circuit (Bias Supply With Buck and Push Pull)



From top to bottom: CH1: IGBT gate signal, 20 V/div, CH4: IGBT Vds voltage, 100 V/div, CH2: SN6505-Q1 switch node voltage, 20/div, CH3: Load current flowing from drain to source of the IGBT, 500 A/div, 1 µs/div

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-020014.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-020014.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

The power stage of TIDA-020014 implements a 4-layer PCB. All bias supplies of TIDA-020014 implement 2-layer PCBs. To download the layer plots, see the design files at TIDA-020014.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-020014.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-020014.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-020014.

5 Software Files

To download the software files, see the design files at TIDA-020014.

6 Related Documentation

1. Texas Instruments, Automotive Wide V_{IN} Front-End Power Reference Design w/Cold Crank Operation & Transient Protection
2. Texas Instruments, 4.5V to 65V input bias supply with power stage reference design for automotive IGBT/SiC gate drivers
3. Texas Instruments, 98.6% Efficiency, 6.6-kW Totem-Pole PFC Reference Design for HEV/EV Onboard Charger
4. Texas Instruments, Automotive Dual Channel SiC MOSFET Gate Driver Reference Design with Two Level Turn-off Protection

6.1 商標

6.2 Third-Party Products Disclaimer

7 Terminology

AFE— Analog Front End

AEC— Automotive Electronics Council

ESR— Equivalent Series Resistance

EMI— Electromagnetic Interference

EMC— Electromagnetic Compatibility

DM— Differential Mode

CM— Common Mode

UVLO— Undervoltage Lockout

MOSFET— Metal Oxide Semiconductor Field Effect Transistor

CISPR— International Special Committee on Radio Interference

PE— Protective Earth

RMS— Root Mean Square

ISO— International Organization for Standardization

BOM— Bill of Material

OEM— Original Equipment Manufacturer

AN— Artificial Network

LISN— line impedance stabilization network

EUT— Equipment Under Test

PCB— Printed Circuit Board

HEV— Hybrid Electric Vehicle

EV— Electric Vehicle

8 About the Author

Xun Gong is an Automotive Systems Engineer at Texas Instruments, where he is responsible for developing reference design solutions for HEV/EV powertrain applications. Xun brings to this role expertise in the field of onboard charger, DC/DC converter, and traction inverter with IGBT and SiC (Silicon Carbide) power transistors. Xun achieved his Ph.D. in electrical engineering from Delft University of Technology in Delft, Netherlands. Xun Gong has more than 10 technical paper publications and he won the 1st prize paper of the *Academic Journal IEEE Transactions on Power Electronics* in 2014.

Xiong Li is a systems engineer from the high power drivers team. Xiong is responsible for defining high-voltage isolated gate drivers for high-power IGBTs and SiC MOSFETs. Prior joining TI, Xiong completed his PhD degree from the University of Texas at Dallas in electrical engineering with focus on power electronics. Xiong did summer internship with Tesla Motors in 2015 and Emerson Network Power in 2011.

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